Intel® Open Source HD Graphics, Intel Iris™ Graphics, and Intel Iris™ Pro Graphics

Programmer's Reference Manual

For the 2015 - 2016 Intel Core™ Processors, Celeron™ Processors, and Pentium™ Processors based on the "Skylake" Platform

Volume 4: Configurations

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Configurations Overview

The Intel "Gen" Graphics Architecture was first introduced to the market in 2004. Since that time, the architecture and implementation have evolved to add many new features, increase performance, and improve power efficiency.

Each product generation has its own configurations chapter. Each chapter has a section for each project, and each project contains the following subsections:

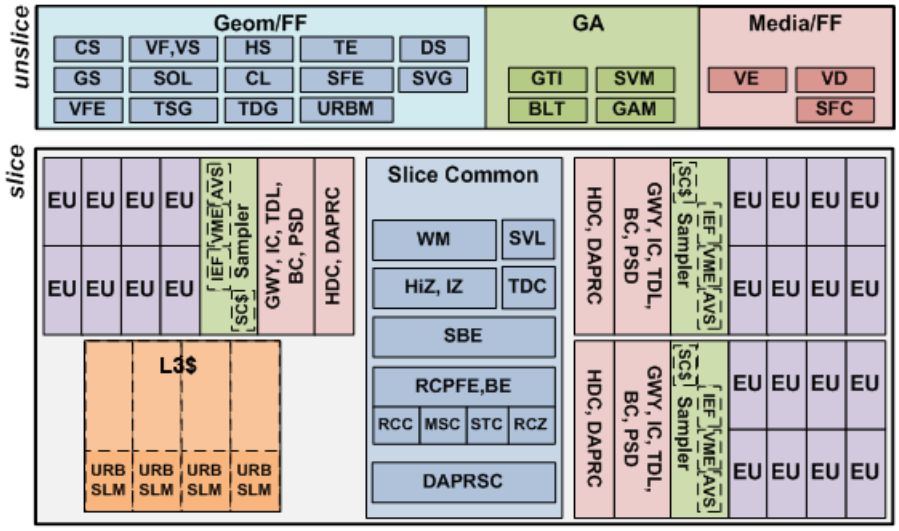
- Top Level Block Diagrams - Show basic feature blocks of the project's graphics architecture, for GT configurations.
- Device Attributes - List details of the graphics configuration options for each project.
- Steppings and Device IDs - Lists all of the current unique GT Die / Packages for a specific project.

Top Level Block

The diagrams below show basic feature blocks of the Skylake (SKL) graphics architecture, for GT2 and GT3 configurations.

GT2 Configuration

The GT2 configuration contains one Unslice, one Slice, and media with separate power domains for each, although they share a single clock domain.



This diagram is based on the following functional partitions:

(a) Geometry Fixed Functions (Geom/FF)

(b) Media Fixed Functions (Media/FF)

(c) Global Assets and GT Interface (GA)

(d) One or more Subslices (three shown)

(e) A Slice Common block

(f) An L3 Cache (L3$) block

Note that the combination of (a), (b), and (c) is typically referred to as the "unslice", while a combination of (d), (e), and (f) is referred to as a compute "slice".

The functionality in each of these groupings is further broken down as follows:

- Unslice – Fixed function pipelines for 3D, GPGPU, and Media operations, and interface to the outside world.
    - The 3D Geometry / Fixed Function (Geom/FF) block consisting of:
        - 3D fixed function pipeline (Command Stream-CS, Vertex Fetch-VF, Vertex Shader-VS, Hull Shader-HS, Tessellation Engine-TE, Domain Shader-DS, Geometry Shader-GS, Stream Output Logic-SOL, Clipper-CL, Strip/Fan Engine-SF, State Variable Global-SVG)
        - Video Front-End unit (VFE)
        - Thread Spawner unit (TSG) and the global Thread Dispatcher unit (TDG)
        - Unified Return Buffer Manager (URBM)
    - Media fixed function assets:
        - Video Decode (VD) Box
        - Video Encode (VE) Box
        - SFC
    - The Global Assets (GA) block as the primary interface and memory stream gateway to the outside world, consisting of:
        - GT Interface (GTI)
        - State Variable Manager (SVM)
        - Blitter (BLT)
        - Graphics Arbiter (GAM)
- Subslice (three shown) – A compute unit with supporting fixed- or shared-function assets sufficient for the EU capability.
    - A bank of Execution Units (EUs) – eight per subslice shown
    - Sampler, supporting both media and 3D functions
    - Gateway (GWY)
    - Instruction cache (IC)
    - Local Thread Dispatcher (TDL)
    - Barycentric Calculator (BC)
    - Pixel Shader Dispatcher (PSD)
    - Data Cluster (HDC)
    - Dataport Render Cache (DAPRC) - two per subslice
- Slice Common – Scalable fixed function assets which support the compute horsepower provided two or more subslices.
    - 3D Fixed Function:
        - Windower/Mask unit (WM)
        - Hi-Z (HZ) and Intermediate Z (IZ)
        - Setup Backend (SBE)

        - RCPFE, BE
        - 3D stream caches (RCC, MSC, STC, RCZ)
    - Media Fixed Functions:
        - DAPRSC
        - SVL
        - TDC
- L3 Cache – backing L3 cache for certain memory streams emanating from subslices.
    - L3 Data cache with support for data, URB, and shared local memory (SLM)

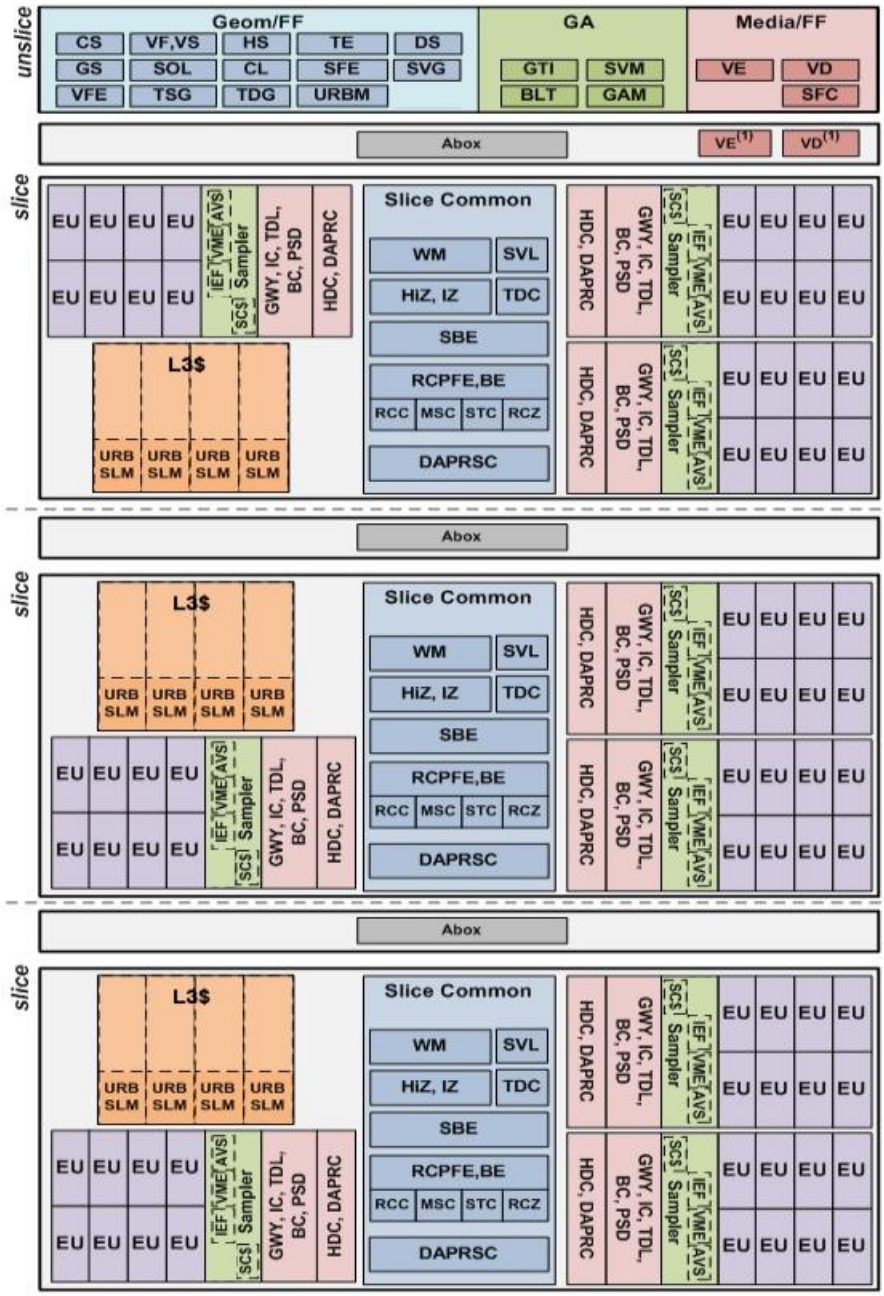
GT3 Configuration

The GT3 configuration has an identical Unslice to GT2, except that it contains two compute slices. The L3 caches of each Slice combine to provide an aggregate L3 cache of the twice the size and twice the bandwidth of a single instance. GT3 also has an additional media slice w/ one additional instance of VEBOX and VDBOX each.

Separate clock domains for the Unslice and Slice may be available depending on SKU. See the "Steppings and Device IDs" section for more information.

GT4 Configuration

The GT4 configuration has an identical Unslice to GT2, but contains three compute slices. The L3 caches of each Slice combine to provide an aggregate L3 cache of three times the size and three times the bandwidth of a single instance. GT4 also has an additional media slice with one additional instance of VEBOX and VDBOX each.



Device Attributes

The following table lists detailed GT device attributes for proposed SKUs.

Product Configuration Attribute Table					
Product Family	**SKL**				
Architectural Name *	**1x2x6**	**1x3x6**	**1x3x8**	**2x3x8**	**3x3x8**
SKU Name	**GT1F**	**GT1.5F**	**GT2**	**GT3**	**GT4**
Global Attributes					
Slice count	1	1	1	2	3
Subslice Count	2	3	3	6	9
EU/Subslice	6	6	8	8	8
EU count (total)	12	18	23 / 24 [a]	47 / 48 [a]	71 / 72 [a]
Thread Count	7	7	7	7	7
Thread Count (Total)	84	126	161 / 168	329 / 336	497 / 504
FLOPs/Clk - Half Precision, MAD (peak)	384	576	736 / 768	1504 / 1536	2272 / 2304
FLOPs/Clk - Single Precision, MAD (peak)	192	288	368 / 384	752 / 768	1136 / 1152
FLOPs/Clk - Double Precision, MAD (peak)	48	72	92 / 96	188 / 192	284 / 288
Unslice clocking (coupled/decoupled from Cr slice)	coupled	coupled	coupled	coupled	coupled decoupled [b]
GTI / Ring Interfaces	1	1	1	1	1
GTI bandwidth (bytes/unslice-clk)	64: R	64: R	64: R	64: R	64: R
	64: W	64: W	64: W	64: W	64: W
eDRAM Support	N/A	N/A	N/A	0, 64MB	0, 128MB
Graphics Virtual Address Range	48 bit	48 bit	48 bit	48 bit	48 bit
Graphics Physical Address Range	39 bit	39 bit	39 bit	39 bit	39 bit
Caches & Dedicated Memories					
L3 Cache, total size (bytes)	384K	768K	768K	1536K	2304K
L3 Cache, bank count	2	4	4	8	12
L3 Cache, bandwidth (bytes/clk)	2x 64: R 2x 64: W	4x 64: R 4x 64: W	4x 64: R 4x 64: W	8x 64: R 8x 64: W	12x 64: R 12x 64: W
L3 Cache, D$ Size (Kbytes)	192K - 256K	512K	512K	1024K	1536K
URB Size (kbytes)	128K - 192K	384K	384K	768K	1008K
SLM Size (kbytes)	0, 128K	0, 192K	0, 192K	0, 384K	0, 576K
LLC/L4 size (bytes)	~2MB/CPU core	~2MB/CPU core	~2MB/CPU core	~2MB/CPU core	~2MB/CPU core
Instruction Cache (IC, bytes)	2x 48K	3x 48K	3x 48K	6x 48K	9x 48K

Product Configuration Attribute Table					
Color Cache (RCC, bytes)	24K	24K	24K	2x 24K	3x 24K
MSC Cache (MSC, bytes)	16K	16K	16K	2x 16K	3x 16K
HiZ Cache (HZC, bytes)	12K	12K	12K	2x 12K	2x 12K
Z Cache (RCZ, bytes)	32K	32K	32K	2x 32K	3x 32K
Stencil Cache (STC, bytes)	8K	8K	8K	2x 8K	3x 8K
Instruction Issue Rates					
FMAD, SP (ops/EU/clk)	8	8	8	8	8
FMUL, SP (ops/EU/clk)	8	8	8	8	8
FADD, SP (ops/EU/clk)	8	8	8	8	8
MIN,MAX, SP (ops/EU/clk)	8	8	8	8	8
CMP, SP (ops/EU/clk)	8	8	8	8	8
INV, SP (ops/EU/clk)	2	2	2	2	2
SQRT, SP (ops/EU/clk)	2	2	2	2	2
RSQRT, SP (ops/EU/clk)	2	2	2	2	2
LOG, SP (ops/EU/clk)	2	2	2	2	2
EXP, SP (ops/EU/clk)	2	2	2	2	2
POW, SP (ops/EU/clk)	1	1	1	1	1
IDIV, SP (ops/EU/clk)	1-6	1-6	1-6	1-6	1-6
TRIG, SP (ops/EU/clk)	2	2	2	2	2
FDIV, SP (ops/EU/clk)	1	1	1	1	1
Load/Store					
Data Ports (HDC)	2	3	3	6	9
L3 Load/Store (bytes/clk)	2x 64	3x 64	3x 64	6x 64	9x 64
SLM Load/Store (bytes/clk)	2x 64	3x 64	3x 64	6x 64	9x 64
Atomic Inc, 32b - sequential addresses (bytes/clk)	2x 64	3x 64	3x 64	6x 64	9x 64
Atomic Inc, 32b - same address (bytes/clk)	2x 4	3x 4	3x 4	6x 4	9x 4
Atomic CmpWr, 32b - sequential addresses (bytes/clk)	2x 32	3x 32	3x 32	6x 32	9x 32
Atomic CmpWr, 32b - same address (bytes/clk)	2x 4	3x 4	3x 4	6x 4	9x 4
3D Attributes					
Geometry pipes	1	1	1	1	1
Samplers (3D)	2	3	3	6	9
Texel Rate, point, 32b (tex/clk)	8	12	12	24	36
Texel Rate, point, 64b (tex/clk)	8	12	12	24	36
Texel Rate, point, 128b (tex/clk)	8	12	12	24	36

Product Configuration Attribute Table					
Texel Rate, bilinear, 32b (tex/clk)	8	12	12	24	36
Texel Rate, bilinear, 64b (tex/clk)	8	12	12	24	36
Texel Rate, bilinear, 128b (tex/clk)	2	3	3	6	9
Texel Rate, trilinear, 32b (tex/clk)	4	6	6	12	18
Texel Rate, trilinear, 64b (tex/clk)	2	3	3	6	9
Texel Rate, trilinear, 128b (tex/clk)	1	1.5	1.5	3	4.5
Texel Rate, aniso 2x, 32b (tex/clk)	2	3	3	6	9
Texel Rate, aniso 4x, 32b (tex/clk)	1	1.5	1.5	3	4.5
Texel Rate, ansio 8x, 32b (tex/clk)	0.5	0.75	0.75	1.5	2.25
Texel Rate, ansio 16x, 32b (tex/clk)	0.25	0.375	0.375	0.75	1.125
HiZ Rate, (ppc)	64	64	64	2x 64	3x 64
IZ Rate, (ppc)	16	16	16	2x 16	3x 16
Stencil Rate (ppc)	64	64	64	2x 64	3x 64
(500 MHz, DDR-2400 or eDRAM; Range depends on dynamic compression ratio)					
Pixel Rate, fill, 32bpp (pix/clk, RCC hit)	8	8	8	16	24
Pixel Rate, fill, 32bpp (pix/clk, LLC hit @ 1.0x unslice clk)					
Pixel Rate, fill, 32bpp (pix/clk, LLC hit, @ 1.5x unslice clk)	N/A	N/A	N/A		
Pixel Rate, fill, 32bpp (pix/clk, memory, @ 1.0x unslice clk)					
Pixel Rate, fill, 32bpp (pix/clk, memory, @ 1.5x unslice clk)	N/A	N/A	N/A		
(500 MHz, DDR-2400 or eDRAM; Range depends on dynamic compression ratio)					
Pixel Rate, blend, 32bpp (p/clk, RCC hit)	8	8	8	16	24
Pixel Rate, blend, 32bpp (p/clk, LLC hit, @ 1.0x unslice clk)					
Pixel Rate, blend, 32bpp (p/clk, LLC hit, @ 1.5x unslice clk)	N/A	N/A	N/A		
Pixel Rate, blend, 32bpp (pix/clk, memory, @ 1.0x unslice clk)					
Pixel Rate, blend, 32bpp (pix/clk, memory, @ 1.5x unslice clk)	N/A	N/A	N/A		
Media Attributes					
Samplers (media)	2	3	3	6	9
VDBox Instances	1	1	1	2	2
VEBox Instances	1	1	1	2	2

Product Configuration Attribute Table					
SFC Instances	1	1	1	1	1

Notes:

* Architectural Name = Slice Count x Subslice Count x EUs per Subslice

[a] Particular SKUs produced by Intel may have one EU disabled.

[b] In the GT4 SKU, a decoupled unslice feature is supported, where the slice and unslice may operate on independent voltage planes (if supported by the platform), and may have independent clocking.

A brief explanation of the listed SKUs is as follows:

- GT1F has one slice containing two subslices with two (of eight) EUs fused out in each subslice for a total of 2 x 6 = 12 EUs.
- GT1.5F has one slice containing three subslices with two (of eight) EUs fused out in each subslice for a total of 3 x 6 = 18 EUs.
- GT2 has one slice containing three subslices of eight EUs each, for a total of 3 x 8 = 24 EUs, with one EU reserved for die recovery in case of errors.
- GT3 has two slices containing three subslices of eight EUs each, for a total of 2 x 3 x 8 = 48 EUs, with one EU reserved for die recovery in case of errors.
- GT4 has three slices containing three subslices of eight EUs each, for a total of 3 x 3 x 8 = 72 EUs, with one EU reserved for die recovery in case of errors.

Steppings and Device IDs

Skylake GT Unique Devices

The following table lists all currently proposed GT Die / Packages for SKL. Prior to manufacturing, this information is subject to change at any time.

CPU SKU*	GT SKU	Total EUs	CPU Stepping	GT/Disp Stepping	Native Device2 ID	GT Device2 Revision ID	Description / Comments
SKL 4+2 DT	**GT2**	**24**	**R0**	**G0**	**0x191B**	**0x6**	Production devices: Intel® HD Graphics 530
SKL 2+2 DT	**GT2**	**24**	**S0**	**G0**	**0x1912**	**0x6**	Production devices: Intel® HD Graphics 530
SKL 4+2 DT	**GT2**	**24**	**R0**	**G0**	**0x1912**	**0x6**	Production devices: Intel® HD Graphics 530
SKL WKS 4+2	**GT2**	**24**	**R1**	**G1**	**0x191D**	**0x6**	Production devices: Intel® HD Graphics P530
SKL 2+1F DT	**GT1F**	**12**	**S0**	**G0**	**0x1902**	**0x6**	Production devices: Intel® HD Graphics 510
SKL U – ULT 2+2	**GT2**	**24**	**D0**	**H0**	**0x1916**	**0x7**	Production devices: Intel® HD Graphics 520
SKL Y – ULX 2+2	**GT2**	**24**	**D0**	**H0**	**0x191E**	**0x7**	Production devices: Intel® HD Graphics 515
SKL U - ULT 2+1F	**GT1F**	**12**	**D0**	**H0**	**0x1906**	**0x7**	Production devices: Intel® HD Graphics 510
SKL - H 4+1F	**GT1F**	**12**	**D0**	**H0**	**0x190B**	**0x7**	Production devices: Intel® HD Graphics 510
SKL U – ULT 2+3E (15W)	**GT3e**	**48**	**K1**	**I1**	**0x1926**	**0xA**	Production devices: Iris™ Graphics 540
SKL U - ULT 2+3E (28W)	**GT3e**	**48**	**K1**	**I1**	**0x1927**	**0xA**	Production Devices: Iris™ Graphics 550
SKL U - ULT 2+3	**GT3**	**48**	**K1**	**I1**	**0x1923**	**0xA**	Production Devices: Intel® HD Graphics 535
SKL H Halo 4+4E	**GT4e**	**72**	**N0**	**J0**	**0x193B**	**0x9**	Production devices: Iris™ Pro Graphics P580
SKL Media Server 4+3FE	**GT3e**	**48**	**N0**	**J0**	**0x192D**	**0x9**	Production devices: Iris™ Graphics P555
SKL WKS 4+4E	**GT4e**	**72**	**N0**	**J0**	**0x193D**	**0x9**	Production devices: Iris™ Pro Graphics P580

* Column heading explanations are as follows:

- CPU SKU is a brief description of the CPU / GT combination, where the first number at the end is the number of CPU cores and the final number refers to the GT SKU. See the Device Attributes page for details on each GT SKU type.

- GT SKU is the full GT SKU name.
- Total EUs is the total number of graphics execution units.
- CPU Stepping refers to the CPU design stepping.
- GT/Disp Stepping refers to the GT design stepping.
- Device0 ID is the PCI device ID that identifies the CPU type for driver software.
- Native Device2 ID is the PCI device ID that identifies the GT SKU for driver software.
- GT Device2 Revision ID identifies the silicon stepping for driver software.
- Description / Comments explain the development status of the proposed SKU, or other relevant information.

Some SKUs with these device IDs may have a reduced number of EUs. Please see the Device Attributes Table.

Device IDs

The following table lists valid Skylake Device IDs, with brief explanations of the intended usage and product type.

Device2 ID	Description	Comments / SKU String	Number of EUs
1902	Desktop - GT1	Intel® HD Graphics 510	12
1906	Mobile - GT1	Intel® HD Graphics 510	12
190B	Halo - GT1F	Intel® HD Graphics 510	12
1912	Desktop - GT2	Intel® HD Graphics 530	24
1916	Mobile - GT2	Intel® HD Graphics 520	24
191B	Mobile - GT2	Intel® HD Graphics 520, 530	24
191D	Mobile Xeon - GT2	Intel® HD Graphics P530	24
191E	Mobile - GT2	Intel® HD Graphics 510, 515	24
1923	GT3	Intel® HD Graphics 535	48
1926	GT3e	Iris™ Graphic 540	48
1927	GT3e	Iris™ Graphics 550	48
192D	Media Server - GT3fe	Iris™ Graphics P555	48
193B	Halo - GT4e	Iris™ Pro Graphics P580	72
193D	Workstation - GT4e	Iris™ Pro Graphics P580	72

Some SKUs with these device IDs may have a reduced number of EUs. Please see the Device Attributes Table.