Intel® Open Source HD Graphics, Intel Iris™ Graphics, and Intel Iris™ Pro Graphics

Programmer's Reference Manual

For the 2015 - 2016 Intel Core™ Processors, Celeron™ Processors, and Pentium™ Processors based on the "Skylake" Platform

Volume 2c: Command Reference: Registers
Part 1 – Registers A through L

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Notices and Disclaimers

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Active Head Pointer Register

ACTHD - Active Head Pointer Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	02074h-02077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_RCSUNIT
Address:	12074h-12077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_VCSUNIT0
Address:	1A074h-1A077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_VECSUNIT
Address:	1C074h-1C077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_VCSUNIT1
Address:	22074h-22077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_BCSUNIT

This register contains the address details of the data dword being parsed by command streamer.

- When the commands are being executed from a batch buffer this register contains the Dword aligned Graphics Memory Address.
- When the commands are being executed from a ring buffer this register contains the Dword aligned offset in to the ring buffer (offset from Ring Buffer start address).

DWord	Bit	Description
0	31:2	**Head Pointer** Format: GraphicsAddress[31:2] • When the commands are being executed from a batch buffer this register contains the Dword aligned Graphics Memory Address. • When the commands are being executed from a ring buffer this register contains the Dword aligned offset in to the ring buffer (offset from Ring Buffer start address).
	1:0	**Reserved** Format: MBZ

Advanced Scheduler Reset Request Messages

ASSRREQ - Advanced Scheduler Reset Request Messages

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	0810Ch

Hardware (CS, VCS) initiated Advanced Scheduler reset request messages.

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:6	**Reserved** Access: RO Reserved
	5	**SFC1 gracefull reset request message (2nd Vbox)** Access: R/W Set SFC1 gracefull Reset Request Message for 2nd Vbox: '1' : cmsfc Reset Requested - This bit is cleared by the CP upon completion of the reset request '0' : cmsfc Reset Not Requested
	4	**SFC0 gracefull reset request message (1st Vbox)** Access: R/W Set SFC0 gracefull Reset Request Message for 1st Vbox: '1' : cmsfc Reset Requested - This bit is cleared by the CP upon completion of the reset request '0' : cmsfc Reset Not Requested
	3	**VINunit cmfxrst reset request message (2nd Vbox)** Access: R/W Set CMFX Reset Request Message from the VINunit in 2nd Vbox: '1' : CMFX Reset Requested - This bit is cleared by the CP upon completion of the reset request '0' : CMFX Reset Not Requested

ASSRREQ - Advanced Scheduler Reset Request Messages

	2	**VINunit cmfxrst Reset Request message** Access: R/W Set CMFX Reset Request Message from the VINunit: '1' : CMFX Reset Requested - This bit is cleared by the CP upon completion of the reset request '0' : CMFX Reset Not Requested
	1	**Render AS Reset Request Message** Access: R/W Set Render AS Reset Request Message from the CSunit: '1' : Render AS Reset Requested - This bit is cleared by the CP upon completion of the reset request '0' : Render AS Reset Not Requested
	0	**Media AS Reset Request Message** Access: R/W Set Media AS Reset Request Message from the VCSunit: '1' : Media AS Reset Requested - This bit is cleared by the CP upon completion of the reset request '0' : Media AS Reset Not Requested

Aggregate Perf Counter A0

OAPERF_A0 - Aggregate Perf Counter A0	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02800h
This register reflects the count value of the OA Performance counter A0. DefaultValue="00000000h"	

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A0 Upper DWord

OAPERF_A0_UPPER - Aggregate Perf Counter A0 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02804h

This register enables the current live value of performance counter A0 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A1

OAPERF_A1 - Aggregate Perf Counter A1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02808h	
This register reflects the count value of the OA Performance counter A1. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A1 Upper DWord

OAPERF_A1_UPPER - Aggregate Perf Counter A1 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0280Ch

This register enables the current live value of performance counter A1 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A2

OAPERF_A2 - Aggregate Perf Counter A2		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02810h	
This register reflects the count value of the OA Performance counter A2. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A2 Upper DWord

OAPERF_A2_UPPER - Aggregate Perf Counter A2 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02814h

This register enables the current live value of performance counter A2 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A3

OAPERF_A3 - Aggregate Perf Counter A3		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02818h	
This register reflects the count value of the OA Performance counter A3. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A3 Upper DWord

OAPERF_A3_UPPER - Aggregate Perf Counter A3 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0281Ch

This register enables the current live value of performance counter A3 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A4

OAPERF_A4 - Aggregate Perf Counter A4		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02820h	
This register reflects the count value of the OA Performance counter A4. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A4 Lower DWord Free

OAPERF_A4_LOWER_FREE - Aggregate Perf Counter A4 Lower DWord Free	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02960h

This register counts the same event as counter A4 however is not affected by context ID or other conditions that prevent A4 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted used this register.

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A4 Upper DWord

OAPERF_A4_UPPER - Aggregate Perf Counter A4 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02824h

This register enables the current live value of performance counter A4 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A4 Upper DWord Free

OAPERF_A4_UPPER_FREE - Aggregate Perf Counter A4 Upper DWord Free

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02964h

This register counts the same event as counter A4 however is not affected by context ID or other conditions that prevent A4 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted using this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A5

OAPERF_A5 - Aggregate Perf Counter A5		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02828h	
This register reflects the count value of the OA Performance counter A5. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A5 Upper DWord

OAPERF_A5_UPPER - Aggregate Perf Counter A5 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0282Ch

This register enables the current live value of performance counter A5 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A6

OAPERF_A6 - Aggregate Perf Counter A6		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02830h	
This register reflects the count value of the OA Performance counter A6. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A6 Lower DWord Free

OAPERF_A6_LOWER_FREE - Aggregate Perf Counter A6 Lower DWord Free	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02968h

This register counts the same event as counter A6 however is not affected by context ID or other conditions that prevent A6 from incrementing. his counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted used this register.

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A6 Upper DWord

OAPERF_A6_UPPER - Aggregate Perf Counter A6 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02834h

This register enables the current live value of performance counter A6 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A6 Upper DWord Free

OAPERF_A6_UPPER_FREE - Aggregate Perf Counter A6 Upper DWord Free

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0296Ch

This register counts the same event as counter A6 however is not affected by context ID or other conditions that prevent A6 from incrementing. his counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted using this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A7

OAPERF_A7 - Aggregate Perf Counter A7		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02838h	
This register reflects the count value of the OA Performance counter A7. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A7 Upper DWord

OAPERF_A7_UPPER - Aggregate Perf Counter A7 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0283Ch

This register enables the current live value of performance counter A7 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A8

OAPERF_A8 - Aggregate Perf Counter A8		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02840h	
This register reflects the count value of the OA Performance counter A8. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A8 Upper DWord

OAPERF_A8_UPPER - Aggregate Perf Counter A8 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02844h

This register enables the current live value of performance counter A8 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A9

OAPERF_A9 - Aggregate Perf Counter A9		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02848h	
This register reflects the count value of the OA Performance counter A9. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A9 Upper DWord

OAPERF_A9_UPPER - Aggregate Perf Counter A9 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0284Ch

This register enables the current live value of performance counter A9 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A10

OAPERF_A10 - Aggregate Perf Counter A10		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02850h	
This register reflects the count value of the OA Performance counter A10. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A10 Upper DWord

OAPERF_A10_UPPER - Aggregate Perf Counter A10 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02854h

This register enables the current live value of performance counter A10 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A11

OAPERF_A11 - Aggregate Perf Counter A11		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02858h	
This register reflects the count value of the OA Performance counter A11. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A11 Upper DWord

OAPERF_A11_UPPER - Aggregate Perf Counter A11 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0285Ch

This register enables the current live value of performance counter A11 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A12

OAPERF_A12 - Aggregate Perf Counter A12		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02860h	
This register reflects the count value of the OA Performance counter A12. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A12 Upper DWord

OAPERF_A12_UPPER - Aggregate Perf Counter A12 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02864h

This register enables the current live value of performance counter A12 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A13

OAPERF_A13 - Aggregate Perf Counter A13		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02868h	
This register reflects the count value of the OA Performance counter A13. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A13 Upper DWord

OAPERF_A13_UPPER - Aggregate Perf Counter A13 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0286Ch

This register enables the current live value of performance counter A13 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A14

OAPERF_A14 - Aggregate Perf Counter A14		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02870h	
This register reflects the count value of the OA Performance counter A14. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A14 Upper DWord

OAPERF_A14_UPPER - Aggregate Perf Counter A14 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02874h

This register enables the current live value of performance counter A14 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A15

OAPERF_A15 - Aggregate Perf Counter A15		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02878h	
This register reflects the count value of the OA Performance counter A15. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A15 Upper DWord

OAPERF_A15_UPPER - Aggregate Perf Counter A15 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0287Ch

This register enables the current live value of performance counter A15 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A16

OAPERF_A16 - Aggregate Perf Counter A16	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02880h
This register reflects the count value of the OA Performance counter A16. DefaultValue="00000000h"	

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A16 Upper DWord

OAPERF_A16_UPPER - Aggregate Perf Counter A16 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02884h

This register enables the current live value of performance counter A16 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A17

OAPERF_A17 - Aggregate Perf Counter A17		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02888h	
This register reflects the count value of the OA Performance counter A17. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A17 Upper DWord

OAPERF_A17_UPPER - Aggregate Perf Counter A17 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0288Ch

This register enables the current live value of performance counter A17 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A18

OAPERF_A18 - Aggregate Perf Counter A18		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02890h	
This register reflects the count value of the OA Performance counter A9. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A18 Upper DWord

OAPERF_A18_UPPER - Aggregate Perf Counter A18 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02894h

This register enables the current live value of performance counter A18 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A19

OAPERF_A19 - Aggregate Perf Counter A19		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02898h	
This register reflects the count value of the OA Performance counter A19. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A19 Lower DWord Free

OAPERF_A19_LOWER_FREE - Aggregate Perf Counter A19 Lower DWord Free	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02970h

This register counts the same event as counter A19 however is not affected by context ID or other conditions that prevent A19 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted used this register.

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A19 Upper DWord

OAPERF_A19_UPPER - Aggregate Perf Counter A19 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0289Ch

This register enables the current live value of performance counter A19 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A19 Upper DWord Free

OAPERF_A19_UPPER_FREE - Aggregate Perf Counter A19 Upper DWord Free

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02974h

This register counts the same event as counter A19 however is not affected by context ID or other conditions that prevent A19 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted using this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A20

OAPERF_A20 - Aggregate Perf Counter A20		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	028A0h	
This register reflects the count value of the OA Performance counter A20. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A20 Lower DWord Free

OAPERF_A20_LOWER_FREE - Aggregate Perf Counter A20 Lower DWord Free	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02978h

This register counts the same event as counter A20 however is not affected by context ID or other conditions that prevent A20 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted used this register.

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A20 Upper DWord

OAPERF_A20_UPPER - Aggregate Perf Counter A20 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028A4h

This register enables the current live value of performance counter A20 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A20 Upper DWord Free

OAPERF_A20_UPPER_FREE - Aggregate Perf Counter A20 Upper DWord Free

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0297Ch

This register counts the same event as counter A20 however is not affected by context ID or other conditions that prevent A20 from incrementing. his counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted using this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A21

OAPERF_A21 - Aggregate Perf Counter A21		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	028A8h	
This register reflects the count value of the OA Performance counter A21. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A21 Upper DWord

OAPERF_A21_UPPER - Aggregate Perf Counter A21 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028ACh

This register enables the current live value of performance counter A21 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A22

OAPERF_A22 - Aggregate Perf Counter A22		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	028B0h	
This register reflects the count value of the OA Performance counter A22. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A22 Upper DWord

OAPERF_A22_UPPER - Aggregate Perf Counter A22 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028B4h

This register enables the current live value of performance counter A22 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A23

OAPERF_A23 - Aggregate Perf Counter A23		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	028B8h	
This register reflects the count value of the OA Performance counter A23. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A23 Upper DWord

OAPERF_A23_UPPER - Aggregate Perf Counter A23 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028BCh

This register enables the current live value of performance counter A23 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A24

OAPERF_A24 - Aggregate Perf Counter A24		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	028C0h	
This register reflects the count value of the OA Performance counter A24. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A24 Upper DWord

OAPERF_A24_UPPER - Aggregate Perf Counter A24 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028C4h

This register enables the current live value of performance counter A24 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A25

OAPERF_A25 - Aggregate Perf Counter A25		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	028C8h	
This register reflects the count value of the OA Performance counter A25. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A25 Upper DWord

OAPERF_A25_UPPER - Aggregate Perf Counter A25 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028CCh

This register enables the current live value of performance counter A25 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A26

OAPERF_A26 - Aggregate Perf Counter A26		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	028D0h	
This register reflects the count value of the OA Performance counter A26. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A26 Upper DWord

OAPERF_A26_UPPER - Aggregate Perf Counter A26 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028D4h

This register enables the current live value of performance counter A26 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A27

OAPERF_A27 - Aggregate Perf Counter A27		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	028D8h	
This register reflects the count value of the OA Performance counter A27. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A27 Upper DWord

OAPERF_A27_UPPER - Aggregate Perf Counter A27 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028DCh

This register enables the current live value of performance counter A27 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A28

OAPERF_A28 - Aggregate Perf Counter A28		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	028E0h	
This register reflects the count value of the OA Performance counter A28. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A28 Upper DWord

OAPERF_A28_UPPER - Aggregate Perf Counter A28 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028E4h

This register enables the current live value of performance counter A28 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A29

OAPERF_A29 - Aggregate Perf Counter A29		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	028E8h	
This register reflects the count value of the OA Performance counter A29. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A29 Upper DWord

OAPERF_A29_UPPER - Aggregate Perf Counter A29 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028ECh

This register enables the current live value of performance counter A29 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A30

OAPERF_A30 - Aggregate Perf Counter A30		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	028F0h	
This register reflects the count value of the OA Performance counter A30. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A30 Upper DWord

OAPERF_A30_UPPER - Aggregate Perf Counter A30 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028F4h

This register enables the current live value of performance counter A30 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A31

OAPERF_A31 - Aggregate_Perf_Counter_A31

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028F8h

This register reflects the count value of the OA Performance counter A31

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A31 Upper DWord

OAPERF_A31_UPPER - Aggregate Perf Counter A31 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028FCh

This register enables the current live value of performance counter A31 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A32

OAPERF_A32 - Aggregate_Perf_Counter_A32	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02900h

This register reflects the count value of the OA Performance counter A32

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A33

OAPERF_A33 - Aggregate_Perf_Counter_A33		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02904h	
This register reflects the count value of the OA Performance counter A33		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A34

OAPERF_A34 - Aggregate_Perf_Counter_A34

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02908h

This register reflects the count value of the OA Performance counter A34

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A35

OAPERF_A35 - Aggregate_Perf_Counter_A35			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Address:	0290Ch		
This register reflects the count value of the OA Performance counter A35			
DWord	**Bit**	**Description**	
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.	

All Engine Fault Register

FAULT_REG - All Engine Fault Register

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04094h

DWord	Bit	Description
0	31:1	**All Engine Fault Register** Default Value: 00000000000000000000000000000000b Access: R/W Bit[31:15]: Reserved. Bit[14:12]: Engine ID: 000b - GFX. 001b - MFX0. 010b - MFX1. 011b - VEBX. 100b - BLT. 110b - Reserved. Bit[11]: Reserved. Bit[10:3]: SRCID of Fault. This is the Source ID of the unit that requested the cycle that generated the First Page fault for this engine. This value is locked and not updated on subsequent faults, until the valid bit of this register is cleared by SW. Bit[2:1]: Fault Type (GFX_FT): Type of Fault recorded: 00b - Invalid PTE Fault. 01b - Invalid PDE Fault. 10b - Invalid PDPE Fault. 11b - Invalid PML4E Fault. This value is locked and not updated on subsequent faults, until the valid bit of this register is cleared by SW. All bits are only valid with bit[0]=1.
	0	**Valid Bit** Default Value: 0b Access: R/W This bit indicates that the first fault for this engine has been recorded. It can only be cleared by SW, which also clears the other fields.

ARB_CTL

ARB_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0E661056
Access:	R/W
Size (in bits):	32
Address:	45000h-45003h
Name:	Display Arbitration Control 1
ShortName:	ARB_CTL
Power:	PG0
Reset:	soft

DWord	Bit	Description
0	31	**Reserved**
	30	**Reserved**
	29	**Reserved**
	28:26	**HP Queue Watermark** Default Value: 011b 4 entries The value in this register indicates the number of entries the high priority queue should have before it can be read. The value is zero based.
	25:24	**LP Write Request Limit** The value in this register indicates the maximum number of back to back LP write requests that will be accepted from a single client before re-arbitrating. Value / Name: 00b: 1 01b: 2 10b: 4 **[Default]** 11b: 8
	23:20	**TLB Request Limit** The value in this register indicates the maximum number of TLB requests that can be made in an arbitration loop. Zero is not a valid programming. Value / Name: 0110b: 6 **[Default]** [1,15]:
	19:16	**TLB Request InFlight Limit** The value in this register indicates the maximum number of TLB (or VTd) requests that can be in flight at any given time. Zero is not a valid programming.

ARB_CTL

	Value	Name
	0110b	6 **[Default]**
	[1,15]	

15 — FBC Watermark Disable

Setting this bit disables the FBC watermarks.

Value	Name
0b	Enable
1b	Disable

14:13 — Tiled Address Swizzling

DRAM configuration registers show if memory address swizzling is needed.

Value	Name	Description
00b	No Display	No display request address swizzling
01b	Reserved	Address bit[6] swizzling for tiled surfaces is not used
10b	Reserved	
11b	Reserved	

12:8 — HP Page Break Limit

The value in this register represents the maximum number of page breaks allowed in a HP request chain. Zero is not a valid programming.

Value	Name
10000b	16 **[Default]**
[1,31]	

7 — Reserved

6:0 — HP Data Request Limit

The value in this register represents the maximum number of cachelines allowed in a HP request chain.

Value	Name
1010110b	86 **[Default]**
[1,127]	

Restriction
This value must always be programmed greater than 8.

ARB_CTL2

ARB_CTL2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x20000600
Access:	R/W
Size (in bits):	32
Address:	45004h-45007h
Name:	Display Arbitration Control 2
ShortName:	ARB_CTL2
Power:	PG0
Reset:	soft

DWord	Bit	Description
0	31	**Reserved**
	30	**Reserved** Format: MBZ
	29:28	**LP WD Write Request Limit** The value in this register indicates the maximum number of back to back LP write requests that will be accepted from WD before re-arbitrating. 00b: 1 01b: 2 10b: 4 **[Default]** 11b: 8
	27:25	**Reserved** Format: MBZ
	24:20	**Reserved** Format: MBZ
	19:16	**Reserved** Format: MBZ
	15	**Reserved** Format: MBZ
	14	**Reserved** Format: MBZ
	13	**Reserved**

ARB_CTL2

12	**Arbiter Trickle Feed Allow On HP Request** If enabled, Arbiter will allow trickle feed request from all clients if any of the client sends a high priority request This field must be kept at default value. **Value** / **Name** 0b – Disable **[Default]** 1b – Enable
11	**Reserved**
10:9	**Inflight LP Read Request Limit** The value in this register represents the maximum number of LP read request transactions that can be inflight at any given time. **Value** / **Name** 00b – 1 LP 01b – 2 LP 10b – 3 LP 11b – 4 LP **[Default]**
8	**Reserved** Format: MBZ
7	**Reserved**
6	**Reserved** Format: MBZ
5:4	**Inflight HP Read Request Limit** The value in this register represents the maximum number of HP read request transactions that can be inflight at any given time. **Value** / **Name** 00b – 128 HP 01b – 64 HP 10b – 32 HP 11b – 16 HP
3	**Enable IPC** Enables the Isochronous Priority Control. If enabled, Display sends demoted requests once the transition watermark is reached. If transition watermark is not enabled, Display sends demoted requests when the display buffer is full. **Value** / **Name** 0b – Disable 1b – Enable
2	**Reserved** Format: MBZ

ARB_CTL2

	1:0	**RTID FIFO Watermark** The value in this register represents the watermark value for the RTID FIFO. HP transactions will start only when the FIFO level is above or equal the watermark.

Value	Name
00b	8 RTIDs
01b	16 RTIDs
10b	32 RTIDs
11b	Reserved

Arbiter Control Register

GARBCNTLREG - Arbiter Control Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x29124100
Size (in bits):	32
Address:	0B004h

DWord	Bit	Description
0	31	**Reserved**
	30	**Disables hashing function** Access: R/W Disables hashing function to generate bank_id[1:0] for L3$ bank accessing, and forces the use of address[7:6] for bank_id[1:0]. 0: (default) Hash function enabled to generate L3$ bank IDs. 1: L3$ address[7:6] used as L3$ bank IDs. lncf_csr_l3bankidhashdis. (This bit needs to set corresponding bit lpfcon_csr_l3bankidhashdis in LPFC.)
	29:28	**Arbitration priority order between RCC and MSC** Default Value: 10b Access: R/W Arbitration priority order between RCC and MSC. 00b/11b: Invalid; default setting used. 10b: Default setting; RCC MSC (i.e., MSC has higher priority). 01b: RCC MSC (i.e., RCC has higher priority). lncf_csr_rcc_msc_pri[1:0].
	27:22	**Arbitration priority order between RCZ, STC, and HIZ** Default Value: 100100b Access: R/W Arbitration priority order between RCZ, STC, and HIZ. 100100b: Default setting; RCZ STC HIZ. (i.e., RCZ has lowest priority; HIZ has highest priority). 100001b: RCZ ; HIZ ; STC. 011000b: STC ; RCZ ; HIZ. 010010b: STC ; HIZ ; RCZ. 001001b: HIZ ; RCZ ; STC. 000110b: HIZ ; STC ; RCZ. Note: Others settings are invalid, and result in use of default. lncf_csr_rcz_stc_hiz_pri[5:0].

GARBCNTLREG - Arbiter Control Register

21:19	**Write data port arbitration priority between Z client writes and L3$ evictions** Default Value: 010b Access: R/W Z Max Write Request Limit Count (GFXC_MRLC). This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (both Slice 0 and 1). Minimum count value must be = 1. Incf_csr_wdpagapz[2:0].
18:16	**Write data port arbitration priority between C client writes and Z/L3$ writes/evictions** Default Value: 010b Access: R/W C Max Request Limit Count (GFXZ_MRLC). This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (both Slice 0 and 1). Minimum count value must be = 1. Incf_csr_wdpagapc[2:0].
15	**Reserved** Access: RO
14:12	**L3 Max Write Request Limit Count** Default Value: 100b Access: R/W L3 Max Write Request Limit Count (GFXL3_MRLC). This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1. Incf_csr_wdpagapl3[2:0].
11:9	**Reserved** Access: RO
8	**GAPs_fixarb_en** Default Value: 1b Access: R/W Incf_csr_gaps_fixarb_en.
7	**GAPS TSV Credit fix Enable** Access: R/W Disables GAPS TSV fix for credit signal 0 (default): GAPS TSV fix for credit signal is disabled 1: GAPS TSV fix for credit signal is enabled This bit always needs to be programmed to 1 as part of the BIOS sequence Incf_csr_gaps_tsvfix_en.
6:0	**Reserved** Access: RO

Arbiter Mode Control Register

ARB_MODE - Arbiter Mode Control Register

Register Space: MMIO: 0/2/0
Default Value: 0x00000000
Size (in bits): 32

Address: 04030h

DWord	Bit	Description
0	31:16	**Mask Bits** Default Value: 0000000000000000b Access: RO Mask Bits act as Write Enables for the bits[15:0] of this register.
	15	**Extra Register Bit 15** Default Value: 0b Access: R/W Bit 15 toggles (XOR) the meaning of Per Client Write Drop Enables (Register 40b4); If 0, drop per client happens as stated in register 40b4 definition; If 1, the meaning changes, and a 1 on a bit in register 40b4 means dont drop while 0 means drop. In this case, the default (for clients not included in 40b4) will be drop enabled.
	14	**Extra Register Bit 14** Default Value: 0b Access: R/W Reserved.
	13	**DC GDR** Default Value: 0b Access: R/W
	12	**HIZ GDR** Default Value: 0b Access: R/W
	11	**STC GDR** Default Value: 0b Access: R/W
	10	**BLB GDR** Default Value: 0b Access: R/W
	9	**GAM PD GDR** Default Value: 0b Access: R/W

ARB_MODE - Arbiter Mode Control Register

8	**Extra Register Bit 8** Default Value: 0b Access: R/W **Description** Reserved.
7:6	**Cacheability Attribute Override** Default Value: 00b Access: R/W 00b No override. 01b UC (LLC/eLLC) - Allocation age is don't care. 10b WT in LLC/eLLC - Aged is 3. 11b WB in LLC/eLLC - Aged is 3. The above conditions apply for the following conditions only: 1. Register overwrite except for GTT, CFG and L3 coherent wcil cycles 2. Read- GTTRD, CFGRD 3. Write- GTTWR, CFGWR, DMWR (with gam_ci_wcoherenttype[2:0]="001" WCIL* w/self snoop)
5	**Extra Register Bit 5** Default Value: 0b Access: R/W Reserved.
4	**VMC GDR Enable** Default Value: 0b Access: R/W When this bit is set, data requested from the VMC client is generated by the GDR Algorithm.
3	**Texture Cache (MT) GDR Enable Bit** Default Value: 0b Access: R/W When this bit is set, data requested from the Texture Cache (MT) client is generated by the GDR algorithm.
2	**Depth (RCZ) Cache GDR Enable bit** Default Value: 0b Access: R/W Depth Cache GDR enable bit. Project: All. Format: U1. When this bit is set, data requested from the Depth Cache client is generated by the GDR algorithm (See GDR algorithm in xxx section).

ARB_MODE - Arbiter Mode Control Register

	1	**Color Cache (RCC) GDR Enable Bit** Default Value: 0b Access: R/W When this bit is set, data requested from the Color Cache (RCC) client is generated by the GDR algorithm.
	0	**GTT Accesses GDR** Default Value: 0b Access: R/W When this bit is enabled along with the Client's GDR bit, PPGTT and GGTT requests for this memory access are also tagged as GDR to SQ.

ASL Storage

ASLS_0_2_0_PCI - ASL Storage

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	000FCh

This is a software scratch register. The exact bit register usage must be worked out in common between System BIOS and driver software. For each device, the ASL control method requires two bits for DOD (BIOS detectable yes or no, VGA/NonVGA), one bit for DGS (enable/disable requested), and two bits for DCS (enabled now/disabled now, connected or not).

DWord	Bit	Description
0	31:0	**Device Switching Storage** Default Value: 00000000000000000000000000000000b Access: R/W Software controlled usage to support device switching.

ATS Capability

ATS_CAP_0_2_0_PCI - ATS Capability

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000020
Size (in bits):	16
Address:	00204h

ATS Capability reports support for Device-TLBs on Device-2, compliant to PCI Express ATS specification.

DWord	Bit	Description
0	5	**Page Aligned Request** Default Value: 1b Access: RO Hardwired to 1, the Untranslated Address is always aligned to a 4096 byte boundary. Processor Graphics reports value of 1b indicating all VT-d and SVM translations are page-aligned.
	4:0	**Invalidate Queue Depth** Default Value: 00000b Access: RO The number of Invalidate Requests that the endpoint can accept before putting back pressure on the upstream connection. Hardwired to 0h, the function can accept 32 Invalidate Requests.

ATS Control

ATS_CTRL_0_2_0_PCI - ATS Control

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	16
Address:	00206h

DWord	Bit	Description
0	15	**ATS Enable** Default Value: 0b Access: R/W When Set, the function is enabled to cache translations. Processor graphics ignores this field, as GT uses GTLB as IOTLB and only pretends to software that it has a Device-TLB. Software is expected to Set this field before configuring extended context-entry for Device2 with Page Request Enable field Set. For compatibility, this field is implemeted as RW as software can read it to determine ATS enable status.
	14:5	**Reserved** Format: MBZ
	4:0	**Smallest Translation Unit** Default Value: 00000b Access: R/W This value indicates to the Endpoint the minimum number of 4096-byte blocks that is indicated in a Translation Completion or Invalidate Request. This is a power of 2 multiple and the number of blocks is 2^STU. A value of 0 indicates one block and value 1F indicates 2^31 blocks. For IGD this must be programmed to 0h for 4KB as smallest translation unit.

ATS Extended Capability Header

ATS_EXTCAP_0_2_0_PCI - ATS Extended Capability Header

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x3001000F
Size (in bits):	32
Address:	00200h

ATS Capability reports support for Device-TLBs on Device-2, compliant to PCI Express ATS specification.

DWord	Bit	Description
0	31:20	**Next Capability Offset** Default Value: 001100000000b Access: RO This is a hardwired pointer to the next item in the capabilities list. Value 300h in this field provides the offset for Page-Request Capability.
	19:16	**Version** Default Value: 0001b Access: RO Hardwired to capability version 1.
	15:0	**Capability ID** Default Value: 0000000000001111b Access: RO Hardwired to the ATS Extended Capability ID

AUD_CONFIG

AUD_CONFIG

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0070FA60
Access:	R/W
Size (in bits):	32
Address:	65000h-65003h
Name:	Audio Configuration Transcoder A
ShortName:	AUD_TCA_CONFIG
Power:	off/on
Reset:	soft
Address:	65100h-65103h
Name:	Audio Configuration Transcoder B
ShortName:	AUD_TCB_CONFIG
Power:	off/on
Reset:	soft
Address:	65200h-65203h
Name:	Audio Configuration Transcoder C
ShortName:	AUD_TCC_CONFIG
Power:	off/on
Reset:	soft

This register configures the audio output. There is one instance of this register per transcoder A/B/C. Each Transcoder is independent of the other.

DWord	Bit	Description
0	31:30	**Reserved**
	29	**N value Index** Value / Name / Description 0b / HDMI **[Default]** / N value read on bits 27:20 and 15:4 reflects HDMI N value. Bits 27:20 and 15:4 are programmable to any N value. Default h7FA6 when bit 28 is not set. 1b / DisplayPort / N value read on bits 27:20 and 15:4 reflects DisplayPort N value. Set this bit to 1 before programming N value register. When this bit is set to 1, 27:20 and 15:4 will reflect the current N value. Default is h8000 when bit 28 is not set.
	28	**N programming enable** This bit enables programming of N values for non-CEA modes. Please note that the transcoder to which audio is attached must be disabled when changing this field.

AUD_CONFIG

	27:20	**Upper N value** Default Value: 00000111b These are bits [19:12] of programmable N values for non-CEA modes. Bit 29 of this register must also be written in order to enable programming. Please note that the transcoder to which audio is attached must be disabled when changing this field. See bit 29 description for default values.
	19:16	**Pixel Clock HDMI** This is the target frequency of the CEA/HDMI video mode to which the audio stream is added. This value is used for generating N_CTS packets. This refers to only HDMI Pixel clock and does not refer to DisplayPort Link clock. DisplayPort Link clock does not require this programming. Note: The transcoder on which audio is attached must be disabled when changing this field.

Value	Name	Description
0b	**[Default]**	
0000b	25.2 / 1.001 MHz	25.2 / 1.001 MHz
0001b	25.2 MHz	25.2 MHz (Program this value for pixel clocks not listed in this field)
0010b	27 MHz	27 MHz
0011b	27 * 1.001 MHz	27 * 1.001 MHz
0100b	54 MHz	54 MHz
0101b	54 * 1.001 MHz	54 * 1.001 MHz
0110b	74.25 / 1.001 MHz	74.25 / 1.001 MHz
0111b	74.25 MHz	74.25 MHz
1000b	148.5 / 1.001 MHz	148.5 / 1.001 MHz
1001b	148.5 MHz	148.5 MHz
Others	Reserved	Reserved

	15:4	**Lower N value** Default Value: 111110100110b These are bits [11:0] of programmable N values for non-CEA modes. Bit 29 of this register must also be written in order to enable programming. Please note that the transcoder to which audio is attached must be disabled when changing this field. See bit 29 description for default values
	3	**Reserved**
	2:0	**Reserved**

AUD_DIP_ELD_CTRL_ST

AUD_DIP_ELD_CTRL_ST

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00005400
Access:	R/W
Size (in bits):	32
Address:	650B4h-650B7h
Name:	Audio Control State for DIP and ELD Transcoder A
ShortName:	AUD_TCA_DIP_ELD_CTRL_ST
Power:	off/on
Reset:	soft
Address:	651B4h-651B7h
Name:	Audio Control State for DIP and ELD Transcoder B
ShortName:	AUD_TCB_DIP_ELD_CTRL_ST
Power:	off/on
Reset:	soft
Address:	652B4h-652B7h
Name:	Audio Control State for DIP and ELD Transcoder C
ShortName:	AUD_TCC_DIP_ELD_CTRL_ST
Power:	off/on
Reset:	soft

There is one instance of this register per transcoder A/B/C.

DWord	Bit	Description
0	31	**Reserved** Format: MBZ
	30:29	**DIP Port Select** Access: RO This read-only bit reflects which port is used to transmit the DIP data. This can only change when DIP is disabled. If one or more audio-related DIP packets is enabled and audio is enabled on a digital port, these bits will reflect the digital port to which audio is directed. For DP MST, this is the device select/pipe select.

Value	Name	Description
00b	Reserved **[Default]**	Reserved
01b	Digital Port B	Digital Port B
10b	Digital Port C	Digital Port C
11b	Digital Port D	Digital Port D

AUD_DIP_ELD_CTRL_ST

28:25 **Reserved**

Format:	MBZ

24:21 **DIP type enable status**

Access:	RO

These bits reflect the DIP types enabled. It can be updated while the port is enabled. Within 2 vblank periods, the DIP is guaranteed to have been transmitted. Disabling a DIP type results in setting the contents of that DIP buffer to zero. A reserved setting reflects a disabled DIP.

Value	Name	Description
0000b	**[Default]**	
XXX0b	DIP Disable	Audio DIP disabled
XXX1b	DIP Enable	Audio DIP enabled
XX0Xb	ACP Disable	Generic 1 (ACP) DIP disabled
XX1Xb	ACP Enable	Generic 1 (ACP) DIP enabled
X0XXb	Generic 2 Disable	Generic 2 DIP disabled
X1XXb	Generic 2 Enable	Generic 2 DIP enabled, can be used by ISRC1 or ISRC2
1XXXb	Reserved	Reserved

20:18 **DIP buffer index**

This field is used during read of different DIPs, and during read or write of ELD data. These bits are used as an index to their respective DIP or ELD buffers. When the index is not valid, the contents of the DIP will return all 0s.

Value	Name	Description
000b	Audio **[Default]**	Audio DIP (31 bytes of address space, 31 bytes of data)
001b	Gen 1	Generic 1 (ACP) Data Island Packet (31 bytes of address space, 31 bytes of data)
010b	Gen 2	Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data)
011b	Gen 3	Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data)
Others	Reserved	Reserved

AUD_DIP_ELD_CTRL_ST

17:16 DIP transmission frequency

Access:	RO

These bits reflect the frequency of DIP transmission for the DIP buffer type designated in bits 20:18. When writing DIP data, this value is also latched when the first DW of the DIP is written. When read, this value reflects the DIP transmission frequency for the DIP buffer designated in bits 20:18.

Value	Name	Description
00b	Disable **[Default]**	Disabled
01b	Reserved	Reserved
10b	Send Once	Send Once
11b	Best Effort	Best effort (Send at least every other vsync)

15 Reserved

Format:	MBZ

14:10 ELD buffer size

Default Value:	10101b
Access:	RO

This field reflects the size of the ELD buffer in DWORDs (84 Bytes of ELD)

9:5 ELD access address

Selects the DWORD address for access to the ELD buffer (84 bytes). The value wraps back to zero when incremented past the max addressing value 0x1F. This field change takes effect immediately after being written. The read value indicates the current access address.

4 ELD ACK

Acknowledgement from the audio driver that ELD read has been completed

3:0 DIP access address

Selects the DWORD address for access to the DIP buffers. The value wraps back to zero when it incremented past the max addressing value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.

AUD_EDID_DATA

AUD_EDID_DATA	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	65050h-65053h
Name:	Audio EDID Data Block Transcoder A
ShortName:	AUD_TCA_EDID_DATA
Power:	off/on
Reset:	soft
Address:	65150h-65153h
Name:	Audio EDID Data Block Transcoder B
ShortName:	AUD_TCB_EDID_DATA
Power:	off/on
Reset:	soft
Address:	65250h-65253h
Name:	Audio EDID Data Block Transcoder C
ShortName:	AUD_TCC_EDID_DATA
Power:	off/on
Reset:	soft

These registers contain the HDMI/DP data block from the EDID. The graphics driver reads the EDID and writes the structure to these registers. The vendor specific data block may be longer than 8 bytes, but the driver must not write more than 48 bytes to the buffer. The EDID format is Version 3 within the CEA-861B specification. The HDMI/DP Vendor Specific Data Block is described in version 1.1 of the HDMI specification. These values are returned from the device as the HDMI/DP Vendor Specific Data Block response to a Get HDMI/DP Widget command. Writing sequence:

- Video software sets ELD invalid, and sets the ELD access address to 0, or to the desired DWORD to be written.
- Video software writes ELD data 1 DWORD at a time. The ELD access address autoincrements with each DWORD write, wrapping around to address 0 when the max buffer address size of 0xF has been reached.
- Please note that software must write an entire DWORD at a time.
- Please note that the audio driver checks the valid bit with each byte read of the ELD. This means that the video driver can unilaterally write ELD irrespective of audio driver ELD read status.

Reading sequence:

- Video software sets the ELD access address to 0, or to the desired DWORD to be read.
- Video software reads ELD data 1 DWORD at a time. The ELD access address autoincrements with each

AUD_EDID_DATA

DWORD read, wrapping around to address 0 when the max buffer address size of 0xF has been reached.

There is one instance of this register per transcoder A/B/C.

DWord	Bit	Description
0	31:0	**EDID Data Block** Please note that the contents of this buffer are not cleared when ELD is disabled. The contents of this buffer are cleared during FLR.

AUD_FREQ_CNTRL

AUD_FREQ_CNTRL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000010
Access:	R/W
Size (in bits):	32
Address:	65900h-65903h
Name:	Audio BCLK Frequency Control
ShortName:	AUD_FREQ_CNTRL
Power:	off/on
Reset:	soft

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15	**T-Mode** Indicates whether SDI is operating in 1T mode or 2T mode. BIOS or System Software must pre-program the T-mode register. a. before the iDISPLAY Audio Link is brought out from Link Reset, b. to a value which is consistent with the value of the its counterpart T-mode bit in the Audio Controller (inside the Skylake PCH). c. to a value which is within the electrical capabilities of the platform. Note that 2T mode is prohibited from being used with any BCLK frequency which has an odd number of bit cells. Example, 2T mode is incompatible with BCLK=6MHz (125 bit cells). Value / Name / Description 0b / Enable **[Default]** / 2T mode with sdi data held for 2 bit clks. 1b / Disable / 1T Mode with sdi data held for 1 bit clock only.
	14:5	**Reserved** Format: MBZ
	4	**96MHz BCLK** Default Value: 1b Indicates that iDISPLAY Audio Link will run at 96MHz. This bit is defaulted to 1. BIOS or System Software must pre-program B96 before the iDISPLAY Audio Link is brought out from reset.
	3	**48MHz BCLK** Default Value: 0b Indicates that iDISPLAY Audio Link will run at 48MHz. This bit is defaulted to 0. BIOS or System Software must pre-program B96 before the iDISPLAY Audio Link is brought out from reset.
	2:0	**Reserved** Format: MBZ

AUD_INFOFR

AUD_INFOFR	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	65054h-65057h
Name:	Audio Widget Data Island Packet Transcoder A
ShortName:	AUD_TCA_INFOFR
Power:	off/on
Reset:	soft
Address:	65154h-65157h
Name:	Audio Widget Data Island Packet Transcoder B
ShortName:	AUD_TCB_INFOFR
Power:	off/on
Reset:	soft
Address:	65254h-65257h
Name:	Audio Widget Data Island Packet Transcoder C
ShortName:	AUD_TCC_INFOFR
Power:	off/on
Reset:	soft

When the IF type or dword index is not valid, the contents of the DIP will return all 0s.
These values are programmed by the audio driver in an HDMI/DP Widget Set command. They are returned one byte at a time from the device on the HD audio bus as the HDMI/DP DIP response to a Get HDMI/DP Widget command. To fetch a specific byte, the audio driver should send an HDMI/DP Widget HDMI/DP DIP Index Pointer Set command to set the index, then fetch the indexed byte using the HDMI/DP DIP get.

DWord	Bit	Description
0	31:0	**Data Island Packet Data** This reflects the contents of the DIP indexed by the DIP access address. The contents of this buffer are cleared during function reset or HD audio link reset.

AUD_M_CTS_ENABLE

AUD_M_CTS_ENABLE

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	65028h-6502Bh
Name:	Audio M and CTS Programming Enable Transcoder A
ShortName:	AUD_TCA_M_CTS_ENABLE
Power:	off/on
Reset:	soft
Address:	65128h-6512Bh
Name:	Audio M and CTS Programming Enable Transcoder B
ShortName:	AUD_TCB_M_CTS_ENABLE
Power:	off/on
Reset:	soft
Address:	65228h-6522Bh
Name:	Audio M and CTS Programming Enable Transcoder C
ShortName:	AUD_TCC_M_CTS_ENABLE
Power:	off/on
Reset:	soft

There is one instance of this register per transcoder A/B/C.

DWord	Bit	Description
0	31:22	**Reserved**
	21	**CTS M value Index** Value / Name / Description 0b / CTS **[Default]** / CTS value read on bits 19:0 reflects CTS value. Bit 19:0 is programmable to any CTS value. default is 0 1b / M / M value read on bits 19:0 reflects DisplayPort M value. Set this bit to 1 before programming M value register. When this is set to 1 19:0 will reflect the current M value
	20	**Enable CTS or M prog** When set will enable CTS or M programming.
	19:0	**CTS programming** These are bits [19:0] of programmable CTS values for non-CEA modes. Bit 21 of this register must also be written in order to enable programming. Please note that the transcoder to which audio is attached must be disabled when changing this field.

AUD_MISC_CTRL

AUD_MISC_CTRL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000044
Access:	R/W
Size (in bits):	32
Address:	65010h-65013h
Name:	Audio Converter 1 Misc Control
ShortName:	AUD_C1_MISC_CTRL
Power:	off/on
Reset:	soft
Address:	65110h-65113h
Name:	Audio Converter 2 Misc Control
ShortName:	AUD_C2_MISC_CTRL
Power:	off/on
Reset:	soft
Address:	65210h-65213h
Name:	Audio Converter 3 Misc Control
ShortName:	AUD_C3_MISC_CTRL
Power:	off/on
Reset:	soft

There is one instance of this register per audio converter 1/2/3.

DWord	Bit	Description
0	31:9	**Reserved** Format: MBZ
	8	**Reserved**
	7:4	**Output Delay** Default Value: 0100b The number of samples between when the sample is received from the HD Audio link and when it appears as an analog signal at the pin.
	3	**Reserved** Format: MBZ

AUD_MISC_CTRL

2 — Sample Fabrication EN bit

Access:	R/W

This bit indicates whether internal fabrication of audio samples is enabled during a link underrun.

Value	Name	Description
0b	Disable	Audio fabrication disabled
1b	Enable **[Default]**	Audio fabrication enabled

1 — Pro Allowed

Access:	R/W

By default, the audio device is configured to consumer mode and does not allow the mode to be changed to professional mode by an HD Audio verb. When Pro is allowed by setting this configuration bit, the HD Audio codec allows a verb to set the device into professional mode.
Note: Setting this configuration bit does not change the default Pro bit value to be 1. Pro must be set to 1 through the normal process, using a verb.

Value	Name	Description
0b	Consumer **[Default]**	Consumer use only
1b	Professional	Professional use allowed

0 — Reserved

Format:	MBZ

AUD_PIN_ELD_CP_VLD

AUD_PIN_ELD_CP_VLD

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	650C0h-650C3h
Name:	Audio Pin ELD and CP Ready Status
ShortName:	AUD_PIN_ELD_CP_VLD
Power:	off/on
Reset:	soft

DWord	Bit	Description
0	31:12	**Reserved**
	11	**Audio InactiveC** Inactive: When this bit is set, a digital display sink device has been attached but not active for streaming audio.

Value	Name	Description
0b	Disable	Device is active for streaming audio data
1b	Enable	Device is connected but not active

	10	**Audio Output EnableC** This bit directs audio to the device connected to this transcoder. When enabled along with Inactive set to 0 and audio data is available, the audio data will be combined with the video data and sent over this transcoder. The audio unit uses the status of this bit to indicate presence of the HDMI/DP output to the audio driver.

Value	Name	Description
0b	Disable	No Audio output
1b	Valid	Audio is enabled

	9	**CP ReadyC** This R/W bit reflects the state of CP request from the audio unit. When an audio CP request has been serviced, it must be reset to 1 by the video software to indicate that the CP request has been serviced. This is transcoder based. Software should add a delay of 1ms before updating the CP ready bit. This is needed to make sure that all the pending unsolicited responses are cleared (transmitted to HD audio) before CP ready unsolicited responses is generated. This is needed in case of DP MST is enabled and when many changes to PD, ELDV and CP ready bits are done during mode set.

Value	Name	Description
0b	Pending or Not Ready	CP request pending or not ready to receive requests
1b	Ready	CP request ready

AUD_PIN_ELD_CP_VLD

8	**ELD validC** This R/W bit reflects the state of the ELD data written to the ELD RAM. After writing the ELD data, the video software must set this bit to 1 to indicate that the ELD data is valid. At audio codec initialization, or on a hotplug event, this bit is set to 0 by the video software. This bit is reflected in the audio pin complex widget as the ELD valid status bit. This is transcoder based.

Value	Name	Description
0b	Invalid	ELD data invalid (default, when writing ELD data, set 0 by software)
1b	Valid	ELD data valid (Set by video software only)

7	**Audio InactiveB** Inactive: When this bit is set, a digital display sink device has been attached but not active for streaming audio.

Value	Name	Description
0b	Disable	Device is active for streaming audio data
1b	Enable	Device is connected but not active

6	**Audio Output EnableB** This bit directs audio to the device connected to this transcoder. When enabled along with Inactive set to 0 and audio data is available, the audio data will be combined with the video data and sent over this transcoder. The audio unit uses the status of this bit to indicate presence of the HDMI/DP output to the audio driver. This is transcoder based.

Value	Name	Description
0b	Disable	No audio output
1b	Enable	Audio is enabled

5	**CP ReadyB** See CP_ReadyC description.

Value	Name	Description
0b	Not Ready	CP request pending or not ready to receive requests
1b	Ready	CP request ready

4	**ELD validB** See ELD_validC descripion.

Value	Name	Description
0b	Invalid	ELD data invalid (default, when writing ELD data, set 0 by software)
1b	Valid	ELD data valid (Set by video software only)

3	**Audio InactiveA** Inactive: When this bit is set, a digital display sink device has been attached but not active for streaming audio.

Value	Name	Description
0b	Disable	Device is active for streaming audio data
1b	Enable	Device is connected but not active

AUD_PIN_ELD_CP_VLD

	2	**Audio Output EnableA** This bit directs audio to the device connected to this transcoder. When enabled along with Inactive set to 0 and audio data is available, the audio data will be combined with the video data and sent over this transcoder. The audio unit uses the status of this bit to indicate presence of the HDMI/DP output to the audio driver. This is transcoder based.

Value	Name	Description
0b	Disable	No audio output
1b	Enable	Audio is enabled

	1	**CP ReadyA** See CP_ReadyC description.

Value	Name	Description
0b	Not Ready	CP request pending or not ready to receive requests
1b	Ready	CP request ready

	0	**ELD validA** See ELD_validC descripion.

Value	Name	Description
0b	Invalid	ELD data invalid (default, when writing ELD data, set 0 by software)
1b	Valid	ELD data valid (Set by video software only)

AUD_PIN_PIPE_CONN_ENTRY_LNGTH

AUD_PIN_PIPE_CONN_ENTRY_LNGTH	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000001
Access:	RO
Size (in bits):	32
Address:	650A8h-650ABh
Name:	Audio Connection List Entry and Length Transcoder A
ShortName:	AUD_TCA_PIN_PIPE_CONN_ENTRY_LNGTH_RO
Power:	off/on
Reset:	soft
Address:	651A8h-651ABh
Name:	Audio Connection List Entry and Length Transcoder B
ShortName:	AUD_TCB_PIN_PIPE_CONN_ENTRY_LNGTH_RO
Power:	off/on
Reset:	soft
Address:	652A8h-652ABh
Name:	Audio Connection List Entry and Length Transcoder C
ShortName:	AUD_TCC_PIN_PIPE_CONN_ENTRY_LNGTH_RO
Power:	off/on
Reset:	soft

These values are returned from the device as the Connection List Length response to a Get Pin Widget command or Get Device Widget command if DP MST. There is one instance of this register per transcoder A/B/C.

DWord	Bit	Description
0	31:16	**Reserved**
	15:8	**Connection List Entry** Connection to Convertor Widget Node 0x03
	7	**Long Form** This bit indicates whether the items in the connection list are long form or short form. This bit is hardwired to 0 (items in connection list are short form)
	6:0	**Connection List Length** Default Value: 0000001b This field indicates the number of items in the connection list. If this field is 2, there is only one hardwired input possible, which is read from the Connection List, and there is no Connection Select Control.

AUD_PIPE_CONN_SEL_CTRL

AUD_PIPE_CONN_SEL_CTRL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00030303
Access:	RO
Size (in bits):	32
Address:	650ACh-650AFh
Name:	Audio Pipe Connection Select Control
ShortName:	AUD_PIN_PIPE_CONN_SEL_CTRL_RO
Power:	off/on
Reset:	soft

These values are returned from the device as the Connection List Length response to a Get Pin Widget command or Get Device Widget command for DP MST.

DWord	Bit	Description
0	31:24	**Reserved**
	23:16	**Connection select Control D** Connection Index Currently Set [Default 0x00], Port D Widget is set to 0x02 Value: 03h — Name: **[Default]**
	15:8	**Connection select Control C** Connection Index Currently Set [Default 0x00], Port C Widget is set to 0x01 Value: 03h — Name: **[Default]**
	7:0	**Connection select Control B** Connection Index Currently Set [Default 0x00], Port B Widget is set to 0x00 Value: 03h — Name: **[Default]**

AUD_PWRST

AUD_PWRST

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0FFFFFFF
Access:	RO
Size (in bits):	32
Address:	6504Ch-6504Fh
Name:	Audio Power State Read Only
ShortName:	AUD_PWRST_RO
Power:	off/on
Reset:	soft

These values are returned from the device as the Power State response to a Get Audio Function Group command.

DWord	Bit	Description
0	31:28	**Reserved**
	27:26	**Func Grp Dev PwrSt Curr** Format: **Audio Power State Format** Function Group Device current power state Value: 11b Name:
	25:24	**Func Grp Dev PwrSt Set** Format: **Audio Power State Format** Function Group Device power state that was set Value: 11b Name:
	23:22	**Converter3 Widget PwrSt Curr** Format: **Audio Power State Format** Converter3 Widget current power state Value: 11b Name:
	21:20	**Converter3 Widget PwrSt Req** Format: **Audio Power State Format** Converter3 Widget power state that was requested by audio software Value: 11b Name:

AUD_PWRST

	19:18	**Convertor2 Widget PwrSt Curr** Format: **Audio Power State Format** Converor2 Widget current power state **Value** / **Name** 11b /
	17:16	**Convertor2 Widget PwrSt Req** Format: **Audio Power State Format** Converter2 Widget power state that was requested by audio software **Value** / **Name** 11b /
	15:14	**Convertor1 Widget PwrSt Curr** Format: **Audio Power State Format** Converter1 Widget current power state **Value** / **Name** 11b /
	13:12	**Convertor1 Widget PwrSt Req** Format: **Audio Power State Format** Converter1 Widget power state that was requested by audio software **Value** / **Name** 11b /
	11:10	**PinD Widget PwrSt Curr** Format: **Audio Power State Format** PinD Widget current power stateFor DP MST this represents Device3 power state **Value** / **Name** 11b /
	9:8	**PinD Widget PwrSt Set** Format: **Audio Power State Format** PinD Widget power state that was setFor DP MST this represents Device3 power state **Value** / **Name** 11b /
	7:6	**PinC Widget PwrSt Curr** Format: **Audio Power State Format** PinC Widget current power stateFor DP MST this represents Device2 power state **Value** / **Name** 11b /

AUD_PWRST

	5:4	**PinC Widget PwrSt Set** Format: **Audio Power State Format** PinC Widget power state that was setFor DP MST this represents Device2 power state **Value** / **Name** 11b
	3:2	**PinB Widget PwrSt Curr** Format: **Audio Power State Format** PinB Widget current power stateFor DP MST this represents Device1 power state **Value** / **Name** 11b
	1:0	**PinB Widget PwrSt Set** Format: **Audio Power State Format** PinB Widget power state that was setFor DP MST this represents Device1 power state **Value** / **Name** 11b

AUD_RID

AUD_RID	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00100000
Access:	RO
Size (in bits):	32
Address:	65024h-65027h
Name:	Audio Revision ID Read Only
ShortName:	AUD_RID_RO
Power:	off/on
Reset:	soft

These values are returned from the device as the Revision ID response to a Get Root Node command.

DWord	Bit	Description
0	31:24	**Reserved**
	23:20	**Major Revision** Default Value: 1h The major revision number (left of the decimal) of the HD Audio Spec to which the codec is fully compliant. This field is hardwired within the device.
	19:16	**Minor Revision** Default Value: 0h The minor revision number (rights of the decimal) or dot number of the HD Audio Spec to which the codec is fully compliant. This field is hardwired within the device.
	15:8	**Revision ID** Default Value: 00h The vendor revision number for this given Device ID. This field is hardwired within the device.
	7:0	**Stepping ID** Default Value: 00h An optional vendor stepping number within the given Revision ID. This field is hardwired within the device.

AUD_VID_DID

AUD_VID_DID

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x80862809
Access:	RO
Size (in bits):	32
Address:	65020h-65023h
Name:	Audio Vendor ID / Device ID Read Only
ShortName:	AUD_VID_DID_RO
Power:	off/on
Reset:	soft

These values are returned from the device as the Vendor ID/ Device ID response to a Get Root Node command.

DWord	Bit	Description
0	31:16	**Vendor ID** Default Value: 8086h Used to identify the codec within the PnP system. This field is hardwired within the device.
	15:0	**Device ID** Constant used to identify the codec within the PnP system. This field is set by the device hardware. Value: 2809h — Name: Skylake **[Default]**

AUD_WNIC_PCR_CNTRL

AUD_WNIC_PCR_CNTRL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000001
Access:	R/W
Size (in bits):	32
Address:	659A8h-659ABh
Name:	Audio WNIC PCR Control
ShortName:	AUD_WNIC_PCR_CNTRL
Power:	off/on
Reset:	soft

DWord	Bit	Description
0	31	**PCRupdate_ENABLE** Enable to send the PCR updates to the WNIC.

Value	Name	Description
1b	Enable	When set to 1, the Audio engine will capture the PCR value from Display counter depending on the programmed select value below and send the captured PCR value to the WNIC as a message.
0b	Disable **[Default]**	When set to 0, PCR updates are not sent to the WNIC.

DWord	Bit	Description
	30:3	**Reserved**

Format:	MBZ

DWord	Bit	Description
	2:0	**PCR counter bit select**

Value	Name	Description
001b	4.8ms **[Default]**	When set the PCR value is capture whenever the bit 17 of the counter changes.
010b	9.6ms	When set the PCR value is capture whenever the bit 18 of the counter changes.
100b	19.2ms	When set the PCR value is capture whenever the bit 19 of the counter changes.
Others	Reserved	Cannot have two or more bits set at the same time. If set then behavior is unpredictable.

Audio Codec Interrupt Definition

Audio Codec Interrupt Definition		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	44480h-4448Fh	
Name:	Audio Codec Interrupts	
ShortName:	AUD_INTERRUPT	
Power:	PG0	
Reset:	soft	

This table indicates which events are mapped to each bit of the Audio Codec Interrupt registers.
0x44480 = ISR
0x44484 = IMR
0x44488 = IIR
0x4448C = IER

DWord	Bit	Description
0	31	**Audio_Power_State_change_DDI_D** The ISR is an active high pulse when there is a power state change for audio for DDI D.
	30	**Audio_Power_State_change_DDI_C** The ISR is an active high pulse when there is a power state change for audio for DDI C.
	29	**Audio_Power_State_change_DDI_B** The ISR is an active high pulse when there is a power state change for audio for DDI B.
	28	**Audio_Power_State_change_WD_0** Description: The ISR is an active high pulse when there is a power state change for audio for WD 0.
	27	**Spare 27**
	26	**Spare 26**
	25	**Spare 25**
	24	**Spare 24**
	23	**Spare 23**
	22	**Spare 22**
	21	**Spare 21**
	20	**Spare 20**
	19	**Spare 19**
	18	**Spare 18**
	17	**Spare 17**
	16	**Spare 16**

Audio Codec Interrupt Definition		
	15	**Spare 15**
	14	**Reserved**
	13	**Reserved**
	12	**Spare 12**
	11	**Spare 11**
	10	**Reserved**
	9	**Reserved**
	8:7	**Unused_Int_8_7** These interrupts are currently unused.
	6	**Reserved**
	5	**Reserved**
	4:3	**Unused_Int_4_3** These interrupts are currently unused.
	2	**Reserved**
	1	**Reserved**
	0	**Spare 0**

Auto Draw End Offset

3DPRIM_END_OFFSET - Auto Draw End Offset	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02420h-02423h

DWord	Bit	Description
0	31:0	**End Offset** Format: U32 This register is used to store the end offset value used by the Vertex Fetch to determine when to stop processing the 3D_PRIMITIVE command. This register is valid when the End Offset Enable is set in the 3D_PRIMITIVE command.

AVC GAM Slave Counter High part

AVC_GAM_SLAVE_CTR_H - AVC GAM Slave Counter High part

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	048A0h
Name:	AVC slave counter high for VDBOX0
ShortName:	AVC_VDBOX0_CTR_H
Address:	048A4h
Name:	AVC slave counter high for VDBOX1
ShortName:	AVC_VDBOX1_CTR_H
Address:	048A8h
Name:	AVC slave counter high for VDBOX2
ShortName:	AVC_VDBOX2_CTR_H
Address:	048ACh
Name:	AVC slave counter high for VDBOX3
ShortName:	AVC_VDBOX3_CTR_H
Address:	048B0h
Name:	AVC slave counter high for VDBOX4
ShortName:	AVC_VDBOX4_CTR_H
Address:	048B4h
Name:	AVC slave counter high for VDBOX5
ShortName:	AVC_VDBOX5_CTR_H
Address:	048B8h
Name:	AVC slave counter high for VDBOX6
ShortName:	AVC_VDBOX6_CTR_H
Address:	048BCh
Name:	AVC slave counter high for VDBOX7
ShortName:	AVC_VDBOX7_CTR_H

DWord	Bit	Description
0	31:0	**AVC GAM SLave Counter High** Default Value: 00000000h Access: R/W AVC GAM Slave counter[63:32]

AVC GAM Slave Counter Low part

AVC_GAM_SLAVE_CTR_L - AVC GAM Slave Counter Low part	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04860h
Name:	AVC slave counter low for VDBOX0
ShortName:	AVC_VDBOX0_CTR_L
Address:	04864h
Name:	AVC slave counter low for VDBOX1
ShortName:	AVC_VDBOX1_CTR_L
Address:	04868h
Name:	AVC slave counter low for VDBOX2
ShortName:	AVC_VDBOX2_CTR_L
Address:	0486Ch
Name:	AVC slave counter low for VDBOX3
ShortName:	AVC_VDBOX3_CTR_L
Address:	04870h
Name:	AVC slave counter low for VDBOX4
ShortName:	AVC_VDBOX4_CTR_L
Address:	04874h
Name:	AVC slave counter low for VDBOX5
ShortName:	AVC_VDBOX5_CTR_L
Address:	04878h
Name:	AVC slave counter low for VDBOX6
ShortName:	AVC_VDBOX6_CTR_L
Address:	0487Ch
Name:	AVC slave counter low for VDBOX7
ShortName:	AVC_VDBOX7_CTR_L

DWord	Bit	Description
0	31:0	**AVC GAM SLave Counter Low** Default Value: 00000000h Access: R/W AVC GAM Slave counter[31:0]

Base Data of Stolen Memory

BDSM_0_0_0_PCI - Base Data of Stolen Memory

Register Space:	PCI: 0/0/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	000B0h

This register contains the base address of graphics data stolen DRAM memory.

DWord	Bit	Description
0	31:20	**Graphics Base of Stolen Memory** Default Value: 000000000000b Access: R/W Lock This register contains bits 31 to 20 of the base address of stolen DRAM memory. BIOS determines the base of graphics stolen memory by subtracting the graphics stolen memory size (PCI Device 0 offset 52 bits 6:4) from TOLUD (PCI Device 0 offset BC bits 31:20).
	19:1	**Reserved** Format: MBZ
	0	**Lock** Default Value: 0b Access: R/W Key Lock This bit will lock all writeable settings in this register, including itself.

Base of GTT Stolen Memory

BGSM_0_0_0_PCI - Base of GTT Stolen Memory

Register Space:	PCI: 0/0/0
Source:	BSpec
Default Value:	0x00100000
Size (in bits):	32
Address:	000B4h

This register contains the base address of stolen DRAM memory for the GTT.

DWord	Bit	Description
0	31:20	**Graphics Base of GTT Stolen Memory** Default Value: 000000000001b Access: R/W Lock This register contains the base address of stolen DRAM memory for the GTT. BIOS determines the base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI Device 0 offset 52 bits 11:8) from the Graphics Base of Data Stolen Memory (PCI Device 0 offset B0 bits 31:20).
	19:1	**Reserved** Format: MBZ
	0	**Lock** Default Value: 0b Access: R/W Key Lock This bit will lock all writeable settings in this register, including itself.

Batch Address Difference Register

BB_ADDR_DIFF - Batch Address Difference Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32

Address:	02154h-02157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_RCSUNIT

Address:	12154h-12157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_VCSUNIT0

Address:	1A154h-1A157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_VECSUNIT

Address:	1C154h-1C157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_VCSUNIT1

Address:	22154h-22157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_BCSUNIT

This register contains the difference between the start of the last batch and where the last initiated Batch Buffer is currently fetching commands.

Programming Notes

Programming Restriction:
This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:2	**Batch Buffer Address Difference** Format: GraphicsAddress[31:2] This field specifies the DWord-aligned difference between the starting address of the batch buffer and where the last initiated Batch Buffer is currently fetching commands.
	1:0	**Reserved** Format: MBZ

Batch Buffer Head Pointer Preemption Register

BB_PREEMPT_ADDR - Batch Buffer Head Pointer Preemption Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02148h-0214Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_RCSUNIT
Address:	12148h-1214Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_VCSUNIT0
Address:	1A148h-1A14Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_VECSUNIT
Address:	1C148h-1C14Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_VCSUNIT1
Address:	22148h-2214Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_BCSUNIT

Description

This register gets updated with the DWord-aligned graphics memory address of the PREEMPTABLE command in the batch buffer on which preemption has occurred.
This register gets updated with the DWord-aligned graphics memory address of the command following the MI_BATCH_START corresponding to the second level batch buffer, when the preemption has occurred in the second level batch buffer.
This register value should be looked at only when the preemption has occurred in the batch buffer. This is indicated by "Ring/Batch Indicator" in "RING_BUFFER_HEAD_PREEMPT_REG". This register value retains its previous value and doesn't change when the preemption occurs on a preemptable command in ring buffer.
Preemption is triggered by valid UHPTR in ring buffer mode of scheduling and by a pending execlist in Exec-List mode of scheduling.
This is a global register and context save/restored as part of power context image.

Preemptable Commands	Source

BB_PREEMPT_ADDR - Batch Buffer Head Pointer Preemption Register

MI_ARB_CHECK 3D_PRIMITIVE GPGPU_WALKER MEDIA_STATE_FLUSH PIPE_CONTROL (Only in GPGPU mode of pipeline selection) MI_ATOMIC (Post Sync Operation set in GPGPU mode of pipeline selection) MI_SEMAPHORE_SIGNAL (Post Sync Operation set in GPGPU mode of pipeline selection)	RenderCS

Preemptable Commands	Source
MI_ARB_CHECK	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS

Programming Notes

Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:2	**Batch Buffer Head Pointer** Format: GraphicsAddress[31:2] This field specifies the DWord-aligned Graphics Memory Address of the PREEMPTABLE command in a batch buffer where the Preemption has occurred.
	1:0	**Reserved** Format: MBZ

Batch Buffer Head Pointer Register

BB_ADDR - Batch Buffer Head Pointer Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	02140h-02143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_RCSUNIT
Address:	12140h-12143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_VCSUNIT0
Address:	1A140h-1A143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_VECSUNIT
Address:	1C140h-1C143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_VCSUNIT1
Address:	22140h-22143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_BCSUNIT

This register contains the current DWord Graphics Memory Address of the last-initiated batch buffer.

Programming Notes

Programming Restriction: This register should NEVER be programmed by driver. This is for HW internal use only.

DWord	Bit	Description
0	31:2	**Batch Buffer Head Pointer** Format: GraphicsAddress[31:2] This field specifies the DWord-aligned Graphics Memory Address where the last initiated Batch Buffer is currently fetching commands. If no batch buffer is currently active, the Valid bit will be 0 and this field will be meaningless.
	1	**Reserved** Format: MBZ

BB_ADDR - Batch Buffer Head Pointer Register

	0	**Valid** Format: U1 **Value** / **Name** / **Description** 0h / Invalid **[Default]** / Batch buffer Invalid 1h / Valid / Batch buffer Valid

Batch Buffer Per Context Pointer

BB_PER_CTX_PTR - Batch Buffer Per Context Pointer

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1

Address:	021C0h-021C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_RCSUNIT

Address:	121C0h-121C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VCSUNIT0

Address:	1A1C0h-1A1C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VECSUNIT

Address:	1C1C0h-1C1C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VCSUNIT1

Address:	221C0h-221C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_BCSUNIT

This register is used to program the batch buffer address to be executed between context restore and execution of ring/execution list if enabled. This will only get executed due to regular context save/restore and not during power restore. This register is part of the execution list context and will be executed per context. Only supported if execution list is enabled. There is no preempting workloads within the Per Context Batch Buffer.

Programming Notes	Source
BlitterCS/VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be programmed for these command streamers.	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS
Render CS: Per Context Batch Buffer execution must not look at the MI_RS_CONTROL or Wait For Event status that are restored for the corresponding context. Ex: A context with MI_RS_CONTROL status with RS disabled doesn't stop Render CS from triggering Resource Streamer to execute Per Context Batch Buffer when "**RS Enabled Batch Buffer Per Context**" is set.	RenderCS

BB_PER_CTX_PTR - Batch Buffer Per Context Pointer

RenderCS: The following commands are not supported within a Per Context Batch Buffer:

Command Name
MI_WAIT_FOR_EVENT
MI_ARB_CHECK
MI_RS_CONTROL
MI_REPORT_HEAD
MI_URB_ATOMIC_ALLOC
MI_SUSPEND_FLUSH
MI_TOPOLOGY_FILTER
MI_RS_CONTEXT
MI_SET_CONTEXT
MI_URB_CLEAR
MI_SEMAPHORE_WAIT (Memory Poll Mode). Note: MI_SEMAPHORE_WAIT in register poll mode is supported.
MI_SEMAPHORE_SIGNAL
MI_BATCH_BUFFER_START
MI_CONDITIONAL_BATCH_BUFFER_END
MEDIA_OBJECT_WALKER
GPGPU_WALKER
3DPRIMITIVE
3DSTATE_BINDING_TABLE_POINTERS_VS
3DSTATE_BINDING_TABLE_POINTERS_HS
3DSTATE_BINDING_TABLE_POINTERS_DS
3DSTATE_BINDING_TABLE_POINTERS_GS
3DSTATE_BINDING_TABLE_POINTERS_PS
3DSTATE_GATHER_CONSTANT_VS
3DSTATE_GATHER_CONSTANT_GS
3DSTATE_GATHER_CONSTANT_HS
3DSTATE_GATHER_CONSTANT_DS
3DSTATE_GATHER_CONSTANT_PS
3DSTATE_DX9_CONSTANTF_VS
3DSTATE_DX9_CONSTANTF_HS
3DSTATE_DX9_CONSTANTF_DS
3DSTATE_DX9_CONSTANTF_GS
3DSTATE_DX9_CONSTANTF_PS
3DSTATE_DX9_CONSTANTI_VS
3DSTATE_DX9_CONSTANTI_HS
3DSTATE_DX9_CONSTANTI_DS
3DSTATE_DX9_CONSTANTI_GS
3DSTATE_DX9_CONSTANTI_PS
3DSTATE_DX9_CONSTANTB_VS
3DSTATE_DX9_CONSTANTB_HS
3DSTATE_DX9_CONSTANTB_DS
3DSTATE_DX9_CONSTANTB_GS
3DSTATE_DX9_CONSTANTB_PS
3DSTATE_DX9_LOCAL_VALID_VS
3DSTATE_DX9_LOCAL_VALID_DS

RenderCS

DWord	Bit	Description
0	31:12	**Batch Buffer Per Context Address** Format: U20 Pointer to the Context in memory to be executed as a batch.
	11:3	**Reserved** Format: MBZ
	2	**Reserved**
	1	**RS Enabled Batch Buffer Per Context** Format: U1 If set, the command stream will enable the RS to parse commands. **Programming Notes** This must be set when programming the resource streamer pool commands (3DSTATE_BINDING_TABLE_POOL_ALLOC, 3DSTATE_GATHER_POOL_ALLOC, and 3DSTATE_DX9_CONSTANT_BUFFER_POOL_ALLOC) in order for the pool alloc fields to be valid in both the render engine and resource streamer.
	0	**Batch Buffer Per Context Valid** Format: U1 If set, the command stream will execute the context from the **Batch Buffer Per Context Address** prior to the execution of actual submitted workloads.

Batch Buffer Start Head Pointer Register

BB_START_ADDR - Batch Buffer Start Head Pointer Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02150h-02153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_RCSUNIT
Address:	12150h-12153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_VCSUNIT0
Address:	1A150h-1A153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_VECSUNIT
Address:	1C150h-1C153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_VCSUNIT1
Address:	22150h-22153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_BCSUNIT

This register contains the address specified in the last MI_START_BATCH_BUFFER command.

Programming Notes

Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:2	**Batch Buffer Start Head Pointer** Format: GraphicsAddress[31:2] This field specifies the DWord-aligned Graphics Memory Address where the last initiated Batch Buffer starting address.
	1:0	**Reserved** Format: MBZ

Batch Buffer Start Upper Head Pointer Register

BB_START_ADDR_UDW - Batch Buffer Start Upper Head Pointer Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02170h-02173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_RCSUNIT
Address:	12170h-12173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_VCSUNIT0
Address:	1A170h-1A173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_VECSUNIT
Address:	1C170h-1C173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_VCSUNIT1
Address:	22170h-22173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_BCSUNIT

This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space specified in the last MI_START_BATCH_BUFFER command.

Programming Notes

Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Batch Buffer Start Head Pointer Upper DWORD** Format: GraphicsAddress[47:32] This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space for the last initiated Batch Buffer starting address.

Batch Buffer State Register

BB_STATE - Batch Buffer State Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32

Address:	02110h-02113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_RCSUNIT

Address:	12110h-12113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_VCSUNIT0

Address:	1A110h-1A113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_VECSUNIT

Address:	1C110h-1C113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_VCSUNIT1

Address:	22110h-22113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_BCSUNIT

This register contains the attributes of the current batch buffer initiated from the Ring Buffer.

This register should not be written by software. These fields should only get written by a context restore. Software should always set these fields via the MI_BATCH_BUFFER_START command when initiating a batch buffer. This register is saved and restored with context.

Programming Notes

Contents of this register are valid only when "Valid" bit in BB_ADDR register is set.

DWord	Bit	Description
0	31:10	**Reserved** Format: MBZ
	9:8	**Reserved**
	7	**Reserved** Source: BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS Format: MBZ

BB_STATE - Batch Buffer State Register

	7	**Resource Streamer Enable** Source: RenderCS Format: U1 When this bit is set, the Resource Streamer will execute the batch buffer. When this bit is clear the Resource Streamer will not execute the batch buffer.
	6	**Reserved** Source: BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS Format: MBZ
	6	**Reserved**
	5	**Address Space Indicator** Note: This field reflects the effective address space indicator security level and may not be the same as the Address Space Indicator written using MI_BATCH_BUFFER_START. **Value** / **Name** / **Description** 0h / GGTT **[Default]** / This Batch buffer is located in GGTT memory and is privileged 1h / PPGTT / This Batch buffer is located in PPGTT memory and is non-privileged.
	4	**Reserved**
	4	**Reserved** Source: BlitterCS Exists If: //BCS Format: MBZ
	3:0	**Reserved** Format: MBZ

Batch Buffer Upper Head Pointer Preemption Register

BB_PREEMPT_ADDR_UDW - Batch Buffer Upper Head Pointer Preemption Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32

Address:	0216Ch-0216Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_RCSUNIT

Address:	1216Ch-1216Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_VCSUNIT0

Address:	1A16Ch-1A16Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_VECSUNIT

Address:	1C16Ch-1C16Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_VCSUNIT1

Address:	2216Ch-2216Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_BCSUNIT

This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the last preempted batch buffer. This register follows the same rules as the BB_PREEMPT_ADDR register.

Programming Notes

Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Batch Buffer Head Pointer Upper DWORD** Format: GraphicsAddress[47:32] This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the last preempted batch buffer.

Batch Buffer Upper Head Pointer Register

BB_ADDR_UDW - Batch Buffer Upper Head Pointer Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	02168h-0216Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_RCSUNIT
Address:	12168h-1216Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_VCSUNIT0
Address:	1A168h-1A16Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_VECSUNIT
Address:	1C168h-1C16Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_VCSUNIT1
Address:	22168h-2216Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_BCSUNIT

This register contains the current Upper DWord of Graphics Memory Address of the last-initiated batch buffer.
Programming Restriction:
This register should NEVER be programmed by driver. This is for HW internal use only.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Batch Buffer Head Pointer Upper DWORD** Format: GraphicsAddress[47:32] This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space where the last initiated Batch Buffer is currently fetching commands. If no batch buffer is currently active, the Valid bit in BB_ADDR will be 0 and this field is meaningless.

Batch Offset Register

BB_OFFSET - Batch Offset Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000001
Access:	R/W
Size (in bits):	32
Address:	02158h-0215Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_RCSUNIT
Address:	12158h-1215Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_VCSUNIT0
Address:	1A158h-1A15Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_VECSUNIT
Address:	1C158h-1C15Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_VCSUNIT1
Address:	22158h-2215Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_BCSUNIT

Description	Source
This register contains the offset value to be added to the Batch Buffer Start Address in the MI_BATCH_BUFFER_START command when the Enable Offset bit in MI_BATCH_BUFFER_START command is set.	

Preemptable Commands	Source
• MI_ARB_CHECK • 3D_PRIMITIVE • GPGPU_WALKER • MEDIA_STATE_FLUSH • PIPE_CONTROL (Only in GPGPU mode of pipeline selection) • MI_ATOMIC (Post Sync Operation set in GPGPU mode of pipeline selection) • MI_SEMAPHORE_SIGNAL (Post Sync Operation set in GPGPU mode of pipeline selection)	RenderCS

RenderCS

BB_OFFSET - Batch Offset Register

Preemptable Commands	Source	
MI_ARB_CHECK	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS

Programming Notes

On preemption occurring whith in a primary/chain batch buffer this register is loaded with the offset value of the preempted command header from the batch start address when the Enable Load is set. Preemption of 3D or GP_GPU workloads can only occur on preemptable commands. Batch buffer offset always points to the preemptable command if preempted on preemption or the immediate command following it if not preempted on preemption. EX: Preemption occurs on 3D_PRIMITVE command

- If the 3D_PRIMTIVE command is completely processed by render pipe then the BB_OFFSET points to the command following 3D_PRIMITIVE
- If the 3D_PRIMTIVE command is not completely processed by render pipe then the BB_OFFSET points to the 3D_PRIMITIVE command.

DWord	Bit	Description
0	31:2	**Batch Buffer Offset** Format: GraphicsAddress[31:2] This field specifies the DWord-aligned offset between the starting address of the batch buffer and where the last initiated Batch Buffer is currently fetching commands.
	1	**Reserved** Format: MBZ
	0	**Enable Load** Default Value: 1 Format: Enable **Description** If this bit is set then the Batch Buffer Offset is loaded with the preempted command offset or the following command whenever a batch buffer is ended due to a Preemptable command.

BCS Context Sizes

BCS_CXT_SIZE - BCS Context Sizes

Register Space:	MMIO: 0/2/0
Source:	BlitterCS
Default Value:	0x00000000
Access:	Read/32 bit Write Only
Size (in bits):	32
Address:	221A8h

DWord	Bit	Description
0	31:13	**Reserved** Format: MBZ
	12:8	**BCS Context Size** Format: U5
	7:5	**Reserved** Format: MBZ
	4:0	**Execlist Context Size** Format: U5

BCS Ring Buffer Next Context ID Register

BCS_RNCID - BCS Ring Buffer Next Context ID Register	
Register Space:	MMIO: 0/2/0
Source:	BlitterCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	22198h-2219Fh

This register contains the *next* ring context ID associated with the ring buffer.

Programming Notes

The current context (RCCID) register can be updated indirectly from this register on a context switch event. Note that the only time a context switch can occur is when MI_ARB_CHECK enables preemption or the current context runs dry (head pointer becomes equal to tail pointer).

DWord	Bit	Description
0	63:0	**Unnamed** See Context Descriptor for BCS

BCS SW Control

BCS_SWCTRL - BCS SW Control

Register Space:	MMIO: 0/2/0
Source:	BlitterCS
Default Value:	0x00000000
Access:	r/w
Size (in bits):	32
Trusted Type:	1
Address:	22200h

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask
	15:4	**Reserved** Format: MBZ
	3	**Shrink Blitter Cache** Format: U1 This bit is primarily used for validation purposes to speed up the test time. The full cache depth of 128 CLs should be used for production. This bit is part of the context save/restore. **Value** / **Name** / **Description** 0 / **[Default]** / Blitter/BCS flush will flush and invalidate all cachelines in the Blitter/BLB cache (default). 1 / / Blitter Cache depth will be shortened from 128 CLs to 16 CLs.
	2	**Not Invalidate Blitter Cache on BCS Flush** Format: U1 Programming this bit allows optimal/maximal cache hit usage, when the destination surface of a Fast Copy Blit, is to be used as the Source for a follow on Fast Copy blit, even if the destination surface is flushed out for Display coherency reasons (where the destination surface is also needed to be Displayed). Such a flush with clean cacheline state is suggested when the intermediate blit operation results are being required to maintain memory coherency. The legacy method of cache invalidation on flush can be still pursued at the end of all blit operations or when switching happens due to other prescribed legacy reasons, or when switching from the new Fast Copy Engine blit, to legacy Engine blits. This bit should be programmed set only when used with Fast Copy Blit commands. This bit is part of the context save/restore. **Value** / **Name** / **Description** 0 / **[Default]** / Blitter/BLB Cache will be 128 cache lines in depth (default). 1 / / BCS flush will put all dirty CL in the Blitter cache in the clean state. Any CL already in the clean state will remain clean.

BCS_SWCTRL - BCS SW Control

	1	**Tile Y Destination** Format: U1 Programming this bit makes the HW treat all destination surfaces as Tile Y. This bit over-rides the setting of the destination format in the packet provided to the blitter command streamer. SW is required to flush the HW before changing the polarity of this bit. This bit is part of the context save/restore.
	0	**Tile Y Source** Format: U1 Programming this bit makes the HW treat all source surfaces as Tile Y. This bit over-rides the setting of the source format in the packet provided to the blitter command streamer. SW is required to flush the HW before changing the polarity of this bit. This bit is part of the context save/restore.

BITPLANE CYCLE CONTROL REGISTER

BITPLANE_CTRL - BITPLANE CYCLE CONTROL REGISTER

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32

Bitplane Cycle Control Register

DWord	Bit	Description
0	30:19	**Reserved** Default Value: 000000000000b Access: RO

Bitstream Output Bit Count for the last Syntax Element Report Register

MFC_BITSTREAM_SE_BITCOUNT_SLICE - Bitstream Output Bit Count for the last Syntax Element Report Register	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	128D4h
Name:	VDBOX1

This register stores the count of number of bits in the bitstream for the last syntax element before padding. The bit count is before the byte-aligned alignment padding insertion, but includes the stop-one-bit. This register is part of the context save and restore.

DWord	Bit	Description
0	31:0	**MFC Bitstream Syntax Element Bit Count** Total number of bits in the bitstream output before padding. This count is updated each time the internal counter is incremented.

Bitstream Output Byte Count Per Slice Report Register

MFC_BITSTREAM_BYTECOUNT_SLICE - Bitstream Output Byte Count Per Slice Report Register	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	128D0h

This register stores the count of bytes of the bitstream output. This register is part of the context save and restore.

DWord	Bit	Description
0	31:0	**MFC Bitstream Byte Count** Total number of bytes in the bitstream output from the encoder. This count is updated for every time the internal bitstream counter is incremented.

Bitstream Output Minimal Size Padding Count Report Register

MFC_AVC_MINSIZE_PADDING_COUNT - Bitstream Output Minimal Size Padding Count Report Register

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12814h
Name:	VDBOX1

This register stores the count in bytes of **minimal size padding insertion. It is primarily provided for statistical data gathering.** This register is part of the context save and restore.

DWord	Bit	Description
0	31:0	**MFC AVC MinSize Padding Count** Total number of bytes in the bitstream output contributing to minimal size padding operation. This count is updated each time when the padding count is incremented.

BLC_PWM_CTL

BLC_PWM_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	48250h-48253h
Name:	Backlight PWM Control
ShortName:	BLC_PWM_CTL
Power:	PG0
Reset:	soft

This register controls the backlight PWM logic going to the display utility pin on the CPU.

DWord	Bit	Description
0	31	**PWM Enable** This bit enables the PWM logic. Value / Name / Description: 0b / Disable / PWM disabled 1b / Enable / PWM enabled Restriction: The display utility pin must be configured correctly to output the PWM. Program the frequency and duty cycle before enabling PWM.
	30:29	**Pipe Select** This field selects which vertical blank will be used for backlight blinking. Value / Name / Description: 00b / Pipe A / Use Pipe A 01b / Pipe B / Use Pipe B 10b / Pipe C / Use Pipe C
	28	**Blinking Enable** This bit enables backlight blinking. When enabled, the backlight will be driven on at the programmed brightness during vertical blank and driven off during vertical active. Value / Name: 0b / Disable 1b / Enable

BLC_PWM_CTL

	27	**PWM Granularity** This field controls the granularity (minimum increment) of the PWM backlight control counter. **Value** / **Name** / **Description** 0b / 128 / PWM frequency adjustment on 128 clock increments 1b / 8 / PWM frequency adjustment on 8 clock increments
	26:0	**Reserved**

BLC_PWM_DATA

BLC_PWM_DATA		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	48254h-48257h	
Name:	Backlight PWM Data	
ShortName:	BLC_PWM_DATA	
Power:	PG0	
Reset:	soft	
DWord	**Bit**	**Description**
0	31:16	**Backlight Frequency** This field determines the number of time base events in total for a complete cycle of modulated backlight control. This field is programmed based on the frequency of the clock that is being used and the desired PWM frequency. This value represents the period of the PWM stream in CD clocks multiplied by 128 (default increment) or 8 (alternate increment selected by BLC_PWM_CTL PWM_Granularity).
	15:0	**Backlight Duty Cycle** This field determines the number of time base events for the active portion of the PWM backlight control. A value of zero will turn the backlight off. A value equal to the backlight modulation frequency field will be full on. Updates will take affect at the end of the current PWM cycle. This value represents the active time of the PWM stream in CD clock periods multiplied by 128 (default increment) or 8 (alternate increment selected by BLC_PWM_CTL PWM_Granularity). **Restriction** This should never be larger than the frequency field.

Blitter MOCS Register0

BLT_MOCS_0 - Blitter MOCS Register0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030
Size (in bits):	32
Address:	0CC00h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_0 - Blitter MOCS Register0

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register1

BLT_MOCS_1 - Blitter MOCS Register1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034
Size (in bits):	32
Address:	0CC04h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_1 - Blitter MOCS Register1

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register2

BLT_MOCS_2 - Blitter MOCS Register2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038
Size (in bits):	32
Address:	0CC08h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_2 - Blitter MOCS Register2

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register3

BLT_MOCS_3 - Blitter MOCS Register3

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031
Size (in bits):	32
Address:	0CC0Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_3 - Blitter MOCS Register3

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register4

BLT_MOCS_4 - Blitter MOCS Register4

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CC10h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_4 - Blitter MOCS Register4

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register5

BLT_MOCS_5 - Blitter MOCS Register5

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CC14h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_5 - Blitter MOCS Register5

	Default Value:	0b
	Access:	R/W

Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM).
0: Allocate on MISS (normal cache behavior)
1: Do NOT allocate on MISS

5:4 **LRU management**

Default Value:	11b
Access:	R/W

This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches.
11: Good chance of generating hits.
10: Poor chance of generating hits
01: Don't change the LRU if it is a HIT
00: Reserved

3:2 **Target Cache**

Default Value:	01b
Access:	R/W

This field allows the choice of LLC vs eLLC for caching
00: eLLC Only
01: LLC Only
10: LLC/eLLC Allowed
11: LLC/eLLC Allowed

1:0 **LLC/eDRAM cacheability control**

Default Value:	10b
Access:	R/W

Memory type information used in LLC/eDRAM.
00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)
01: Uncacheable (UC) - non-cacheable
10: Writethrough (WT)
11: Writeback (WB)

Blitter MOCS Register6

BLT_MOCS_6 - Blitter MOCS Register6

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CC18h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_6 - Blitter MOCS Register6

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register7

BLT_MOCS_7 - Blitter MOCS Register7

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CC1Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_7 - Blitter MOCS Register7

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register8

BLT_MOCS_8 - Blitter MOCS Register8

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CC20h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_8 - Blitter MOCS Register8

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register9

BLT_MOCS_9 - Blitter MOCS Register9

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CC24h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_9 - Blitter MOCS Register9

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register10

BLT_MOCS_10 - Blitter MOCS Register10

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CC28h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_10 - Blitter MOCS Register10

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register11

BLT_MOCS_11 - Blitter MOCS Register11

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CC2Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_11 - Blitter MOCS Register11

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register12

BLT_MOCS_12 - Blitter MOCS Register12

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CC30h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_12 - Blitter MOCS Register12

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register13

BLT_MOCS_13 - Blitter MOCS Register13

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CC34h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_13 - Blitter MOCS Register13

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register14

BLT_MOCS_14 - Blitter MOCS Register14

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CC38h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_14 - Blitter MOCS Register14

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register15

BLT_MOCS_15 - Blitter MOCS Register15

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CC3Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_15 - Blitter MOCS Register15

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register16

BLT_MOCS_16 - Blitter MOCS Register16

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030
Size (in bits):	32
Address:	0CC40h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_16 - Blitter MOCS Register16

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register17

BLT_MOCS_17 - Blitter MOCS Register17

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034
Size (in bits):	32
Address:	0CC44h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_17 - Blitter MOCS Register17

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register18

BLT_MOCS_18 - Blitter MOCS Register18

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038
Size (in bits):	32
Address:	0CC48h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_18 - Blitter MOCS Register18

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register19

BLT_MOCS_19 - Blitter MOCS Register19

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031
Size (in bits):	32
Address:	0CC4Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_19 - Blitter MOCS Register19

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register20

BLT_MOCS_20 - Blitter MOCS Register20

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CC50h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_20 - Blitter MOCS Register20

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register21

BLT_MOCS_21 - Blitter MOCS Register21

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CC54h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_21 - Blitter MOCS Register21

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register22

BLT_MOCS_22 - Blitter MOCS Register22

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CC58h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_22 - Blitter MOCS Register22

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register23

BLT_MOCS_23 - Blitter MOCS Register23

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CC5Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_23 - Blitter MOCS Register23

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register24

BLT_MOCS_24 - Blitter MOCS Register24

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CC60h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_24 - Blitter MOCS Register24

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register25

BLT_MOCS_25 - Blitter MOCS Register25

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CC64h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_25 - Blitter MOCS Register25

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register26

BLT_MOCS_26 - Blitter MOCS Register26

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CC68h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_26 - Blitter MOCS Register26

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register27

BLT_MOCS_27 - Blitter MOCS Register27

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CC6Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_27 - Blitter MOCS Register27

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register28

BLT_MOCS_28 - Blitter MOCS Register28

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CC70h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_28 - Blitter MOCS Register28

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register29

BLT_MOCS_29 - Blitter MOCS Register29

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CC74h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_29 - Blitter MOCS Register29

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register30

BLT_MOCS_30 - Blitter MOCS Register30

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CC78h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_30 - Blitter MOCS Register30

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register31

BLT_MOCS_31 - Blitter MOCS Register31

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CC7Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss**

BLT_MOCS_31 - Blitter MOCS Register31

		Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register32

BLT_MOCS_32 - Blitter MOCS Register32

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030
Size (in bits):	32
Address:	0CC80h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_32 - Blitter MOCS Register32

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register33

BLT_MOCS_33 - Blitter MOCS Register33

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034
Size (in bits):	32
Address:	0CC84h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_33 - Blitter MOCS Register33

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register34

BLT_MOCS_34 - Blitter MOCS Register34

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038
Size (in bits):	32
Address:	0CC88h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_34 - Blitter MOCS Register34

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register35

BLT_MOCS_35 - Blitter MOCS Register35

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031
Size (in bits):	32
Address:	0CC8Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_35 - Blitter MOCS Register35

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register36

BLT_MOCS_36 - Blitter MOCS Register36

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CC90h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_36 - Blitter MOCS Register36

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register37

BLT_MOCS_37 - Blitter MOCS Register37

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CC94h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_37 - Blitter MOCS Register37

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register38

BLT_MOCS_38 - Blitter MOCS Register38

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CC98h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_38 - Blitter MOCS Register38

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register39

BLT_MOCS_39 - Blitter MOCS Register39

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CC9Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_39 - Blitter MOCS Register39

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register40

BLT_MOCS_40 - Blitter MOCS Register40

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CCA0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_40 - Blitter MOCS Register40

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register41

BLT_MOCS_41 - Blitter MOCS Register41

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CCA4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_41 - Blitter MOCS Register41

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register42

BLT_MOCS_42 - Blitter MOCS Register42

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CCA8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_42 - Blitter MOCS Register42

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register43

BLT_MOCS_43 - Blitter MOCS Register43

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CCACh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_43 - Blitter MOCS Register43

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register44

BLT_MOCS_44 - Blitter MOCS Register44

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CCB0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_44 - Blitter MOCS Register44

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register45

BLT_MOCS_45 - Blitter MOCS Register45

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CCB4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_45 - Blitter MOCS Register45

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register46

BLT_MOCS_46 - Blitter MOCS Register46

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CCB8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_46 - Blitter MOCS Register46

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register47

BLT_MOCS_47 - Blitter MOCS Register47

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CCBCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_47 - Blitter MOCS Register47

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register48

BLT_MOCS_48 - Blitter MOCS Register48

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030
Size (in bits):	32
Address:	0CCC0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_48 - Blitter MOCS Register48

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register49

BLT_MOCS_49 - Blitter MOCS Register49

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034
Size (in bits):	32
Address:	0CCC4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_49 - Blitter MOCS Register49

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register50

BLT_MOCS_50 - Blitter MOCS Register50

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038
Size (in bits):	32
Address:	0CCC8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_50 - Blitter MOCS Register50

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register51

BLT_MOCS_51 - Blitter MOCS Register51

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031
Size (in bits):	32
Address:	0CCCCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_51 - Blitter MOCS Register51

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register52

BLT_MOCS_52 - Blitter MOCS Register52

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CCD0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_52 - Blitter MOCS Register52

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register53

BLT_MOCS_53 - Blitter MOCS Register53

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CCD4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_53 - Blitter MOCS Register53

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register54

BLT_MOCS_54 - Blitter MOCS Register54

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CCD8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_54 - Blitter MOCS Register54

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register55

BLT_MOCS_55 - Blitter MOCS Register55

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CCDCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_55 - Blitter MOCS Register55

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register56

BLT_MOCS_56 - Blitter MOCS Register56

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CCE0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_56 - Blitter MOCS Register56

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register57

BLT_MOCS_57 - Blitter MOCS Register57

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CCE4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_57 - Blitter MOCS Register57

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register58

BLT_MOCS_58 - Blitter MOCS Register58

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CCE8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_58 - Blitter MOCS Register58

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register59

BLT_MOCS_59 - Blitter MOCS Register59

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CCECh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_59 - Blitter MOCS Register59

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register60

BLT_MOCS_60 - Blitter MOCS Register60

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CCF0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_60 - Blitter MOCS Register60

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register61

BLT_MOCS_61 - Blitter MOCS Register61

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CCF4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_61 - Blitter MOCS Register61

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register62

BLT_MOCS_62 - Blitter MOCS Register62

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CCF8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_62 - Blitter MOCS Register62

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register63

BLT_MOCS_63 - Blitter MOCS Register63

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CCFCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

BLT_MOCS_63 - Blitter MOCS Register63

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter TLB Control Register

BTCR - Blitter TLB Control Register

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0426Ch

DWord	Bit	Description
0	31:1	**Reserved** Default Value: 00000000000000000000000000000000b Access: RO
	0	**Invalidate TLBs on the corresponding Engine** Default Value: 0b Access: R/W SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. This bit is self clear.

BLT Context Element Descriptor (High Part)

BLT_CTX_EDR_H - BLT Context Element Descriptor (High Part)		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04504h	
DWord	**Bit**	**Description**
0	31:0	**BLT Context Element Descriptor (High Part)** Default Value: 00000000h Access: R/W

BLT Context Element Descriptor (Low Part)

BLT_CTX_EDR_L - BLT Context Element Descriptor (Low Part)		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000009	
Size (in bits):	32	
Address:	04500h	
DWord	**Bit**	**Description**
0	31:0	**BLT Context Element Descriptor (Low Part)** Default Value: 00000009h Access: R/W

BLT Context Element Descriptor (Low Part)

BLT_CTX_EDR_L - BLT Context Element Descriptor (Low Part)		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000009	
Size (in bits):	32	
Address:	04500h	
DWord	**Bit**	**Description**
0	31:0	**BLT Context Element Descriptor** Default Value: 00000009h Access: R/W

BLT Fault Counter

BLT_FAULT_CNTR - BLT Fault Counter		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	045B8h	
DWord	**Bit**	**Description**
0	31:0	**BLT Fault Counter** Default Value: 00000000h Access: RO This counter only applies to advance context when fault and stream mode is selected.

BLT Fixed Counter

BLT_FIXED_CNTR - BLT Fixed Counter		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	045BCh	
DWord	**Bit**	**Description**
0	31:0	**BLT Fixed Counter** Default Value: 00000000h Access: RO This counter only applies to advance context when fault and stream mode is selected.

BLT PDP0/PML4/PASID Descriptor (High Part)

BLT_CTX_PDP0_H - BLT PDP0/PML4/PASID Descriptor (High Part)

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0450Ch

DWord	Bit	Description
0	31:0	**BLT PDP0/PML4/PASID Descriptor (High Part)** Default Value: 00000000h Access: R/W

BLT PDP0/PML4/PASID Descriptor (Low Part)

BLT_CTX_PDP0_L - BLT PDP0/PML4/PASID Descriptor (Low Part)

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04508h

DWord	Bit	Description
0	31:0	**BLT PDP0/PML4/PASID Descriptor (Low Part)** Default Value: 00000000h Access: R/W

BLT PDP1 Descriptor Register (High Part)

BLT_CTX_PDP1_H - BLT PDP1 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04514h	
DWord	**Bit**	**Description**
0	31:0	**BLT PDP1 Descriptor Register (High Part)** Default Value: 00000000h Access: R/W

BLT PDP1 Descriptor Register (Low Part)

BLT_CTX_PDP1_L - BLT PDP1 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04510h	
DWord	**Bit**	**Description**
0	31:0	**BLT PDP1 Descriptor Register (Low Part)** Default Value: 00000000h Access: R/W

BLT PDP2 Descriptor Register (High Part)

BLT_CTX_PDP2_H - BLT PDP2 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0451Ch	
DWord	**Bit**	**Description**
0	31:0	**BLT PDP2 Descriptor Register (High Part)** Default Value: 00000000h Access: R/W

BLT PDP2 Descriptor Register (Low Part)

BLT_CTX_PDP2_L - BLT PDP2 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04518h	
DWord	**Bit**	**Description**
0	31:0	**BLT PDP2 Descriptor Register (Low Part)** Default Value: 00000000h Access: R/W

BLT PDP3 Descriptor Register (High Part)

BLT_CTX_PDP3_H - BLT PDP3 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04524h	
DWord	**Bit**	**Description**
0	31:0	**BLT PDP3 Descriptor Register (High Part)** Default Value: 00000000h Access: R/W

BLT PDP3 Descriptor Register (Low Part)

BLT_CTX_PDP3_L - BLT PDP3 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04520h	
DWord	**Bit**	**Description**
0	31:0	**BLT PDP3 Descriptor Register (Low Part)** Default Value: 00000000h Access: R/W

Boolean_Counter_B0

OAPERF_B0 - Boolean_Counter_B0	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02920h

This register enables the current live value of performance counter B0 to be read. Since what conditions cause B0 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Boolean_Counter_B1

OAPERF_B1 - Boolean_Counter_B1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02924h

This register enables the current live value of performance counter B1 to be read. Since what conditions cause B1 to increment are defined by the programming of CEC1-0/CEC1-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Boolean_Counter_B2

OAPERF_B2 - Boolean_Counter_B2	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02928h

This register enables the current live value of performance counter B2 to be read. Since what conditions cause B2 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Boolean_Counter_B3

OAPERF_B3 - Boolean_Counter_B3

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0292Ch

This register enables the current live value of performance counter B3 to be read. Since what conditions cause B3 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Boolean_Counter_B4

OAPERF_B4 - Boolean_Counter_B4	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02930h

This register enables the current live value of performance counter B4 to be read. Since what conditions cause B4 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Boolean_Counter_B5

OAPERF_B5 - Boolean_Counter_B5

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02934h

This register enables the current live value of performance counter B5 to be read. Since what conditions cause B5 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Boolean_Counter_B6

OAPERF_B6 - Boolean_Counter_B6	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02938h

This register enables the current live value of performance counter B6 to be read. Since what conditions cause B6 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Boolean_Counter_B7

OAPERF_B7 - Boolean_Counter_B7	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0293Ch

This register enables the current live value of performance counter B7 to be read. Since what conditions cause B7 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

BOOT VECTOR

BOOTMSG - BOOT VECTOR

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	08504h

Boot Message Register
This register gets locked by the Hardware once written and is cleared only during the reset. This is extra protection given against Illegal Programming.

DWord	Bit	Description
0	31:0	**Boot Vector Message** Access: R/W Lock Boot vector is pass through. MBC gets the boot message from GPMunit and forwards it to MSQC. Breakdown of message is done in MSQC. Details: if b[26] = 1 C6SliceA = b[20:17]; C6SliceB= d[13:10] C6Way = 0 C6Area = 0 if b[26] = 0 C6Way = b[25:21], C6Slice = d[20:17]; C6Area = d[17:10] Context Restore = b[6] Reset Type = b[6:5] Ring Stop ID = b[4:0]

BTB Not Consumed By RCS

BTP_PRODUCE_COUNT - BTB Not Consumed By RCS

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	02480h

This register keeps track of the outstanding BTP produced by RS which are not yet consumed by Render Command Streamer. This register is part of the render context save and restore.

Programming Notes

This register should not be programmed by SW.

DWord	Bit	Description
0	31:0	**BTP Produce Count** This register keeps track of the outstanding BTP produced by RS which are not yet consumed by Render Command Streamer. This register is part of the render context save and restore.

BTP Commands Parsed By RCS

BTP_PARSE_COUNT - BTP Commands Parsed By RCS

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	02490h

This register keeps track of the BTP commands parsed by RCS prior to encountering the Draw Call in an RS enabled Batch Buffer which has BTP Pool Alloc Valid. BTP parse count should be less then equal to the BTP produce count for Command Streamer to make progress on a 3D_PRIMITIVE command. BTP Parse count is subtracted from the BTP Produce Count upon parsing 3D_PRIMITIVE command. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0	31:0	**BTP Parse Count** This register keeps track of the BTP commands parsed by RCS prior to encountering the Draw Call in an RS enabled Batch Buffer which has BTP Pool Alloc Valid. BTP parse count should be less then equal to the BTP produce count for Command Streamer to make progress on a 3D_PRIMITIVE command. BTP Parse count is subtracted from the BTP Produce Count upon parsing 3D_PRIMITIVE command.

Built In Self Test

BIST_0_2_0_PCI - Built In Self Test

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	8
Address:	0000Fh

This register is used for control and status of Built In Self Test (BIST).

DWord	Bit	Description
0	7	**BIST Supported** Default Value: 0b Access: RO BIST is not supported. This bit is hardwired to 0.
	6:0	**Reserved** Format: MBZ

Cache Line Size

CLS_0_2_0_PCI - Cache Line Size		
Register Space:	PCI: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	8	
Address:	0000Ch	
DWord	**Bit**	**Description**
0	7:0	**Cache Line Size** Default Value: 00000000b Access: R/W This register is not reset by FLR. Implemented for PCIe compliant devices for legacy compatibility but has no effect on any PCIe device behavior.

Cache Mode Register 0

CACHE_MODE_0 - Cache Mode Register 0

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	07000h

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask[15:0] A 1 in a bit in this field allows the modification of the corresponding bit in Bits 15:0.
	15	**Sampler L2 Disable** Access: r/w Format: Disable **Value 0h [Default]**: Sampler L2 Cache Enabled. **Value 1h**: Sampler L2 Cache Disabled. All accesses are treated as misses.
	14:12	**MSAA Compression Plane Number Threshold for eLLC** Access: r/w **Value 0h threshold0 [Default]**: Cache only planeID = 0 in eLLC. **Value 1h threshold1**: Cache only planeID = 0, 1 in eLLC. **Value 2h threshold2**: Cache only planeID = 0..2 in eLLC. **Value 3h threshold3**: Cache only planeID = 0..3 in eLLC. **Value 4h threshold4**: Cache only planeID = 0..4 in eLLC. **Value 5h threshold5**: Cache only planeID = 0..5 in eLLC. **Value 6h threshold6**: Cache only planeID = 0..6 in eLLC. **Value 7h threshold7**: Cache only planeID = 0..7 in eLLC. **Programming Notes** This bit-field is programmed based on MSAA. When MSAA compression is enabled, these settings affect HW, else it is ignored. For 16X MSAA only lower 8 planes can be cached in eLLC.

CACHE_MODE_0 - Cache Mode Register 0

11 Sampler Set Remmapping for 3D Disable

Access:	r/w

Value	Name	Description
0h	Enable Set Remap **[Default]**	Set remapping for 3d enabled
1h	Disable Set Remap	Set remapping for 3d disabled

10 Reserved

Access:	r/w
Format:	PBC

9 Sampler L2 TLB Prefetch Enable

Access:	r/w

Value	Name	Description
0h	**[Default]**	TLB Prefetch Disabled
1h		TLB Prefetch Enabled

8 Reserved

7:6 Sampler L2 Request Arbitration

Access:	r/w
Format:	U2

Value	Name	Description
00b		Round Robin
01b		Fetch are Highest Priority
10b		Constants are Highest Priority
11b		Reserved

5 STC PMA Optimization Enable

Access:	r/w
Format:	Enable

Clearing this bit will force the STC cache to wait for pending retirement of pixels at the HZ-read stage and do the STC-test for Non-promoted, R-computed and Computed depth modes instead of postponing the STC-test to RCPFE.

Value	Name	Description
0h	Disable **[Default]**	STC PMA optimization is disabled.
1h	Enable	STC PMA optimization is enabled.

Programming Notes
STC_TEST_EN = (3DSTATE_STENCIL_BUFFER::STENCIL_BUFFER_ENABLE) && (3DSTATE_WM_DEPTH_STENCIL::StencilTestEnable) STC_WRITE_EN =

CACHE_MODE_0 - Cache Mode Register 0

(3DSTATE_STENCIL_BUFFER::STENCIL_BUFFER_ENABLE) && (3DSTATE_WM_DEPTH_STENCIL::Stencil Buffer Write Enable && 3DSTATE_DEPTH_BUFFER::STENCIL_WRITE_ENABLE) COMP_STC_EN = STC_TEST_EN && 3DSTATE_PS_EXTRA::PixelShaderComputesStencil SW parses the pipeline states to generate the following logical signal indicating if PMA FIX can be enabled. STC_PMA_OPT = 3DSTATE_WM::ForceThreadDispatch != 1 && !(3DSTATE_RASTER::ForceSampleCount != NUMRASTSAMPLES_0) && (3DSTATE_DEPTH_BUFFER::SURFACE_TYPE != NULL) && (3DSTATE_DEPTH_BUFFER:: HIZ Enable) && ! (3DSTATE_WM::EDSC_Mode == 2) && (3DSTATE_PS_EXTRA::PixelShaderValid) && !(3DSTATE_WM_HZ_OP::DepthBufferClear || 3DSTATE_WM_HZ_OP::DepthBufferResolve || 3DSTATE_WM_HZ_OP::Hierarchical Depth Buffer Resolve Enable || 3DSTATE_WM_HZ_OP::StencilBufferClear) && (COMP_STC_EN || STC_WRITE_EN) && ((3DSTATE_PS_EXTRA::PixelShaderKillsPixels || 3DSTATE_WM::ForceKillPix == ON || 3DSTATE_PS_EXTRA:: oMask Present to RenderTarget || 3DSTATE_PS_BLEND::AlphaToCoverageEnable || 3DSTATE_PS_BLEND::AlphaTestEnable || 3DSTATE_WM_CHROMAKEY::ChromaKeyKillEnable) || (3DSTATE_PS_EXTRA:: Pixel Shader Computed Depth mode != PSCDEPTH_OFF))
Whenever the value of this bit needs to be changed, there are several synchronization steps required. The exact sequence is described in Synchronization of 3D pipeline section under PIPE_CONTROL command

4 **RCC Eviction Policy**

Access:	r/w
Format:	Disable

If this bit is set, RCCunit will have LRA as replacement policy. The default value i.e. (when this bit is reset) indicates that non-LRA eviction policy. This bit must be reset. LRA replacement policy is not supported.

Programming Notes
If this bit is set to "1", bit 7 of 0x7010h must also be set to "1".

3 **Reserved**

2 **Hierarchical Z RAW Stall Optimization Disable**

Access:	r/w
Format:	U1

The Hierarchical Z RAW Stall Optimization allows non-overlapping polygons in the same 8x4 pixel/sample area to be processed without stalling waiting for the earlier ones to write to Hierarchical Z buffer.

Value	Name	Description
0h	Enable **[Default]**	Enables the hierarchical Z RAW Stall Optimization.
1h	Disable	Disables the hierarchical Z RAW Stall Optimization.

Programming Notes
This bit must be set to 1 to disable the Hierarchical Z RAW stall optimization.

CACHE_MODE_0 - Cache Mode Register 0

	1	**Disable clock gating in the pixel backend** Access: r/w Format: Disable MCL related clock gating is disabled in the pixel backend. Before setting this bit to 1, the instruction/state caches must be invalidated. [DevGT:{WKA}]
	0	**Null tile fix disable** Access: r/w Instead of dropping non dirty cachelines at alloc point, we allow the cacheline till the mem wrbk point, so that null status can be reset.

Value	Name	Description
0	**[Default]**	Null tile fix enabled
1		Null tile fix disable

Cache Mode Register 1

CACHE_MODE_1 - Cache Mode Register 1

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00002980
Access:	R/W
Size (in bits):	32
Address:	07004h

Description
RegisterType: MMIO_SVL
Before changing the value of this register, GFX pipeline must be idle; i.e., full flush is required. This Register is saved and restored as part of Context.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Mask: MASK Format: Mask[15:0] Must be set to modify corresponding data bit. Reads to this field returns zero.
	15	**Color Compression Disable** Access: r/w Setting this bit causes Lossless Render Target Color Compression to be disabled in Classic Clear (1x) Mode of Operation. Default value, i.e. resetting this bit, Enables Color Compression in Classic Clear Mode (1x) when CCS is Enabled. Value: 0h – Name: Enable **[Default]** Value: 1h – Name: Disable **Programming Notes** The Below programming forces Color Compression to be disabled for MSAA modes explicitly as a HW WA. When switching from 1x ==> MSAA. Program this bit to 1 When switching from MSAA ==> 1x. Program this bit to 0
	14	**Blend Optimization Fix Disable** This bit when reset, enables blend optimization fix. If this bit is set, it disables the blend optimization fix and may exhibit corruption on alpha components in the render target under some conditions. Value: 0 – Name: **[Default]** Value: 1 – Name:

CACHE_MODE_1 - Cache Mode Register 1

13 **NP EARLY Z FAILS DISABLE**

Access:	r/w

Value	Name	Description
0h	Disable	When NP PMA FIX ENABLE = 1, clearing this bit disables IZ to conservatively fail pixels.
1h	Enable **[Default]**	When NP PMA FIX ENABLE = 1, IZ does conservatively fail any NP pixels.

Programming Notes
This bit must be set when NP PMA FIX ENABLE = 1
This bit must not be set when NP PMA FIX ENABLE = 0

12 **HIZ Eviction Policy**

Access:	r/w
Format:	U1

If this bit is set, Hizunit will have LRA as replacement policy. The default value i.e. (when this bit is reset) indicates the non-LRA eviction policy. For performance reasons, this bit must be reset.

Value	Name	Description
0h	**[Default]**	Non-LRA eviction Policy
1h		LRA eviction Policy

Programming Notes
If this bit is set to "1", bit 3 of 0x7010h must also be set to "1"

11 **NP PMA FIX ENABLE**

Access:	r/w

Value	Name	Description
0h	Disable	Enables stalling PMA behavior for NP depth pixels in the early depth pipeline. (Legacy behavior)
1h	Enable **[Default]**	Enables non-stalling PMA behavior for NP depth pixels in the early depth pipeline.

Programming Notes
PMA Optimization Enable bit can be programmed to 0 to disable this optimization.

10 **Reserved**

9 **MSC RAW Hazard Avoidance Bit**

Access:	r/w
Format:	Enable

When this field is set, MSC will enable RAW Hazard prevention mechanism, when lossless

CACHE_MODE_1 - Cache Mode Register 1

compression is enabled.

Value	Name	Programming Notes
0h	**[Default]**	
1h		This field should be programmed to 1 only if need arise to avoid RAW hazard when lossless compression is enabled

8:7 **Sampler Cache Set XOR selection**

Access:	r/w
Format:	U2

These bits have an impact only when the Sampler cache is configured in 16 way set associative mode. If the cache is being used for immediate data or for blitter data these bits have no effect.

Value	Name	Description
00b	None	No XOR.
01b	Scheme 1	New_set_mask[3:0] = Tiled_address[16:13]. New_set[3:0] less than or = New_set_mask[3:0] ^Old_set[3:0]. Rationale: These bits can distinguish among 16 different equivalent classes of virtual pages. These bits also represent the lsb for tile rows ranging from a pitch of 1 tile to 16 tiles.
10b	Scheme 2	New_set_mask[3] = Tiled_address[17] ^ Tiled_address[16]. New_set_mask[2] = Tiled_address[16] ^ Tiled_address[15]. New_set_mask[1] = Tiled_address[15] ^ Tiled_address[14]. New_set_mask[0] = Tiled_address[14] ^ Tiled_address[13]. New_set[3:0] less than or = New_set_mask[3:0] ^ Old_set[3:0]. Rationale: More bits on each XOR can give better statistical uniformity on sets and since two lsbs are taken for each tile row size, it reduces the chance of aliasing on sets.
11b	Scheme 3 **[Default]**	New_set_mask[3] = Tiled_address[22] ^ Tiled_address[21] ^ Tiled_address[20] ^ Tiled_address[19]. New_set_mask[2] = Tiled_address[18] ^ Tiled_address[17] ^ Tiled_address[16]. New_set_mask[1] = Tiled_address[15] ^ Tiled_address[14]. New_set_mask[0] = Tiled_address[13]. New_set[3:0] less than or = New_set_mask[3:0] ^ Old_set[3:0]. Rationale: More bits on each XOR can give better statistical uniformity on sets and since each XOR has different bits, it reduces the chance of aliasing on sets even more.

Programming Notes
This field should be programmed as "00b" corresponding to NO XOR option when the 3D map performance fix in MT is enabled using the field "**Sampler Set Remmapping for 3D Disable"** in **CACHE_MODE_0 - Cache Mode Register 0.**

6 **4X4 RCPFE-STC Optimization Disable**

CACHE_MODE_1 - Cache Mode Register 1

Access:	r/w
Format:	Disable

Value	Name	Description
0h	**[Default]**	Enables two contiguous 4x2s to be collected as 4X4 access for STC interface. This allows for less bank collision and less RAM power on STC.
1h		Disables this optimization and therefore only one valid 4x2 is sent to STC on the 4X4 interface.

Restriction
Restriction : This bit must be set.

5 **MCS Cache Disable**

Access:	r/w
Format:	Disable

For Programming restrictions please refer to the 3D Pipeline.

Value	Name	Description
0h	**[Default]**	MCS cache enabled. It allows RTs with MCS buffer enabled to be rendered using either MSAA compression for MSRT OR with color clear feature for non MSRT.
1h		MCS cache is disabled. Hence no MSAA compression for MSRT and no color clear for non-MSRT.

4 **Float Blend Optimization Enable**

Access:	r/w
Format:	Enable

Value	Name	Description
0h	**[Default]**	Disables blend optimization for floating point RTs.
1h		Enables blend optimization for floating point RTs.

3 **Depth Read Hit Write-Only Optimization Disable**

Access:	r/w
Format:	Disable

Value	Name	Description
0h	**[Default]**	Read Hit Write-only optimization is enabled in the Depth cache (RCZ).
1h		Read Hit Write-only optimization is disabled in the Depth cache (RCZ).

2 **RCZ Read after expansion control fix 2**

Access:	r/w
Format:	Enable

CACHE_MODE_1 - Cache Mode Register 1

Value	Name	Description
0h	**[Default]**	RCZ will suppress the read request to memory if it was allocated as a expansion Cacheline
1h		RCZ will always issue a read request to memory, even if it was previously allocated as expansion Cacheline

1 **Partial Resolve Disable in VC**

Access:	r/w
Format:	Disable

Value	Name	Description
0h	**[Default]**	Partial resolve in the Victim Cache enabled.
1h		Partial evictions of cachelines with compression disabled from pixel backend (RCC) will not be resolved in the Victim Cache in CC in order to extend the resolve queue in GAM. Compression enabled cases will ignore this bit and will always be resolved in the VC.

Programming Notes
Recomendation is to set this field to 1 always. Programming it to default value of 0, may have -ve impact on performance for MSAA WLs

0 **Reserved**

Capabilities A

CAPID0_A_0_0_0_PCI - Capabilities A

Register Space:	PCI: 0/0/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	000E4h

DWord	Bit	Description
0	31	**Display HD Audio Disable** Default Value: 0b Access: R/W Key Firmware Only
	30	**PEG12 Disable** Default Value: 0b Access: R/W Key Firmware Only
	29	**PEG11 Disable** Default Value: 0b Access: R/W Key Firmware Only
	28	**PEG10 Disable** Default Value: 0b Access: R/W Key Firmware Only
	27	**PCI Express Link Width Upconfig Disable** Default Value: 0b Access: R/W Firmware Only
	26	**DMI Width** Default Value: 0b Access: R/W Firmware Only
	25	**ECC Disable** Default Value: 0b Access: R/W Firmware Only
	24	**Force DRAM ECC Enabled** Default Value: 0b Access: R/W Firmware Only
	23	**VTd Disable** Default Value: 0b Access: R/W Key Firmware Only 0: Enable VTd 1: Disable VTd

CAPID0_A_0_0_0_PCI - Capabilities A

22	**DMI Gen 2 Disable**	
	Default Value:	0b
	Access:	R/W Firmware Only
21	**PEG Gen 2 Disable**	
	Default Value:	0b
	Access:	R/W Firmware Only
20:19	**DDR Size**	
	Default Value:	00b
	Access:	R/W Firmware Only
18	**SPARE18**	
	Default Value:	0b
	Access:	R/W Firmware Only
17	**Disable 1N Mode**	
	Default Value:	0b
	Access:	R/W Firmware Only
16	**Full ULT Fuse Read Disable**	
	Default Value:	0b
	Access:	R/W Firmware Only
15	**Camarillo Device Disable**	
	Default Value:	0b
	Access:	R/W Key Firmware Only
14	**2 DIMMS per Channel Disable**	
	Default Value:	0b
	Access:	R/W Firmware Only
13	**X2APIC Enabled**	
	Default Value:	0b
	Access:	R/W Firmware Only
12	**Performance Dual Channel Disable**	
	Default Value:	0b
	Access:	R/W Firmware Only

CAPID0_A_0_0_0_PCI - Capabilities A

	11	**Internal Graphics Disable** Default Value: 0b Access: R/W Key Firmware Only 0b: There is a graphics engine within this CPU. Internal Graphics Device (Device 2) is enabled and all of its memory and I/O spaces are accessable. Configuration cycles to Device 2 will be completed within the CPU. All non-SMM memory and IO accesses to VGA will be handled based on Memory and IO enables of Device 2 and IO registers within Device 2 and VGA Enable of the PCI to PCI bridge control (If PCI Express GFX attach is supported). A selected amount of Graphics Memory space is pre-allocated from the main memory based on Graphics Mode Select (GMS in the GGC Register). Graphics Memory is pre-allocated above TSEG Memory. 1b: There is no graphics engine within this CPU. Internal Graphics Device (Device 2) and all of its memory and I/O functions are disabled. Configuration cycle targeted to Device 2 will be passed on. All non-SMM memory and IO accesses to VGA will be handled based on VGA Enable of the PCI to PCI bridge control. Device 2 is disabled and hidden.
	10	**Reserved**
	9	**Reserved**
	8	**SPARE8** Default Value: 0b Access: R/W Firmware Only
	7:4	**Compatibility Rev ID** Default Value: 0000b Access: R/W Firmware Only This is an 8-bit value that indicates the revision identification number for the Host Device 0.
	3	**DDR Overclocking** Default Value: 0b Access: R/W Firmware Only
	2	**IA Overclocking Enabled by DSKU** Default Value: 0b Access: R/W Firmware Only
	1	**DDR Write VRef** Default Value: 0b Access: R/W Firmware Only
	0	**DDR3L Enable** Default Value: 0b Access: R/W Firmware Only

Capabilities B

CAPID0_B_0_0_0_PCI - Capabilities B

Register Space:	PCI: 0/0/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	000E8h

DWord	Bit	Description	
0	31	**IMGU Disable**	
		Default Value:	0b
		Access:	R/W Key Firmware Only
	30	**SPARE30**	
		Default Value:	0b
		Access:	R/W Firmware Only
	29	**IA Overclocking Enable**	
		Default Value:	0b
		Access:	R/W Firmware Only
	28	**SMT Capability**	
		Default Value:	0b
		Access:	R/W Firmware Only
	27:25	**Cache Size Capability**	
		Default Value:	000b
		Access:	R/W Firmware Only
	24	**SPARE24**	
		Default Value:	0b
		Access:	R/W Firmware Only
	23:21	**DDR3 Maximum Frequency Capability with 100 Memory**	
		Default Value:	000b
		Access:	R/W Firmware Only
	20	**Gen3 Disable Fuse for PCIe PEG Controllers**	
		Default Value:	0b
		Access:	R/W Firmware Only
	19	**Package Type**	
		Default Value:	0b
		Access:	R/W Firmware Only

CAPID0_B_0_0_0_PCI - Capabilities B

	18	**Additive Graphics Enabled** Default Value: 0b Access: R/W Firmware Only 0 - Additive Graphics Disabled 1- Additive Graphics Enabled
	17	**Additive Graphics Capable** Default Value: 0b Access: R/W Firmware Only 0 - Capable of Additive Graphics 1 - Not capable of Additive Graphics
	16	**Primary PEG Port x16 Disable** Default Value: 0b Access: R/W Firmware Only
	15	**DMIG3 Disable** Default Value: 0b Access: R/W Firmware Only
	14:12	**SPARE14_12** Default Value: 000b Access: R/W Firmware Only
	11	**Reserved**
	10:9	**SPARE10_9** Default Value: 00b Access: R/W Firmware Only
	8	**GMM Disable** Default Value: 0b Access: R/W Key Firmware Only
	7	**Reserved**
	6:4	**DDR3 Maximum Frequency Capability** Default Value: 000b Access: R/W Firmware Only
	3	**SPARE3** Default Value: 0b Access: R/W Firmware Only
	2	**DDR4 DSKU Enable** Default Value: 0b Access: R/W Firmware Only

CAPID0_B_0_0_0_PCI - Capabilities B

	1	**Dual PEG Force x1 when VGA Enabled** Default Value: 0b Access: R/W Firmware Only
	0	**Single PEG Force x1 when VGA Enabled** Default Value: 0b Access: R/W Firmware Only

Capabilities Control

CAPCTRL0_0_2_0_PCI - Capabilities Control		
Register Space:	PCI: 0/2/0	
Source:	BSpec	
Default Value:	0x0000010C	
Size (in bits):	16	
Address:	00042h	
DWord	**Bit**	**Description**
0	11:8	**CAPID Version** Default Value: 0001b Access: RO This field is hardwired to the value 1h to identify the first revision of the CAPID register definition.
	7:0	**CAPID Length** Default Value: 00001100b Access: RO This field is hardwired to the value 0Ch to indicate the structure length (12 bytes).

Capabilities Pointer

CAPPOINT_0_2_0_PCI - Capabilities Pointer

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000040
Size (in bits):	8
Address:	00034h

This register points to a linked list of capabilities implemented by this device.

DWord	Bit	Description
0	7:0	**Capabilities Pointer Value** Default Value: 01000000b Access: RO This field contains an offset into the function's PCI Configuration Space for the first item in the New Capabilities Linked List, the CAPID0 register at offset 40h.

Capability Identifier

CAPID0_0_2_0_PCI - Capability Identifier		
Register Space:	PCI: 0/2/0	
Source:	BSpec	
Default Value:	0x00007009	
Size (in bits):	16	
Address:	00040h	
DWord	**Bit**	**Description**
0	15:8	**Next Capability Pointer** Default Value: 01110000b Access: RO This field is hardwired to point to the next PCI Capability structure, the PCIe Capabilities structure at 70h.
	7:0	**Capability Identifier** Default Value: 00001001b Access: RO This field is hardwired to the value 09h to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.

CDCLK_CTL

CDCLK_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x080002A1
Access:	R/W
Size (in bits):	32
Address:	46000h-46003h
Name:	CD Clock Control
ShortName:	CDCLK_CTL
Power:	PG0
Reset:	global

This register is not reset by the device 2 FLR.

Restriction
These fields should only be changed as part of the Display Sequences for Changing CD Clock Frequency.

DWord	Bit	Description
0	31:28	**Reserved** Format: MBZ
	27:26	**CD Frequency Select** This field, together with the DPLL0 VCO setting, selects the frequency for CD clock. The DPLL0 VCO setting is programmed through DPLL_CTRL1.

Value	Name	Description
00b	450 or 432 MHz	If DPLL0 VCO 8100 (450 MHz CD, 900 MHz CD2X); If DPLL0 VCO 8640 (432 MHz CD, 864 MHz CD2X);
01b	540 MHz	540 MHz CD, 1080 MHz CD2X
10b	337.5 or 308.57 MHz **[Default]**	If DPLL0 VCO 8100 (337.5 MHz CD, 675 MHz CD2X); If DPLL0 VCO 8640 (308.57 MHz CD, 617.14 MHz CD2X);
11b	675 or 617.14 MHz	If DPLL0 VCO 8100 (675 MHz CD, 1350 MHz CD2X); If DPLL0 VCO 8640 (617.14 MHz CD, 1234.28 MHz CD2X);

Restriction
The Display CD Clock Frequency Limit fuse indicates the maximum allowed CD clock frequency. Software must not select any frequency higher than the maximum that is allowed. If software incorrectly selects a higher frequency, hardware will override to the lowest frequency.

	25:20	**Reserved** Format: MBZ
	19	**Reserved**

CDCLK_CTL

	18	**Reserved**
	17	**Reserved**
	16	**SSA Precharge Enable** This field is unused. **Value** / **Name** 0b / Disable
	15:11	**Reserved** Format: MBZ
	10:0	**CD Frequency Decimal** Format: U10.1 This field selects the decimal value of the frequency for CD clock, which is used to generate divided down clocks for some display engine timers. This value is represented in a 10.1 format with 10 integer bits and 1 fractional bit. Program this field to match the CD frequency chosen by the CD Frequency Select (considering the DPLL0 VCO that is being used), minus one.

Value	Name
01 0011 0011 1b	308.57 MHz CD
01 0101 0000 1b	337.5 MHz CD **[Default]**
01 1010 1111 0b	432 MHz CD
01 1100 0001 0b	450 MHz CD
10 0001 1011 0b	540 MHz CD
10 0110 1000 0b	617.14 MHz CD
10 1010 0010 0b	675 MHz CD

CGE_CTRL

CGE_CTRL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank
Address:	49080h-49083h
Name:	Pipe Color Gamut Enhancement Control
ShortName:	CGE_CTRL_A
Power:	PG1
Reset:	soft
Address:	49180h-49183h
Name:	Pipe Color Gamut Enhancement Control
ShortName:	CGE_CTRL_B
Power:	PG2
Reset:	soft
Address:	49280h-49283h
Name:	Pipe Color Gamut Enhancement Control
ShortName:	CGE_CTRL_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31	**CGE Enable** This bit enables the Color Gamut Enhancement logic. Value: 0b — Name: Disable Value: 1b — Name: Enable
	30:0	**Reserved** Format: MBZ

CGE_WEIGHT

CGE_WEIGHT

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000
Access:	R/W
Size (in bits):	160

Address:	49090h-490A3h
Name:	Pipe Color Gamut Enhancement Weights
ShortName:	CGE_WEIGHT_A
Power:	PG1
Reset:	soft

Address:	49190h-491A3h
Name:	Pipe Color Gamut Enhancement Weights
ShortName:	CGE_WEIGHT_B
Power:	PG2
Reset:	soft

Address:	49290h-492A3h
Name:	Pipe Color Gamut Enhancement Weights
ShortName:	CGE_WEIGHT_C
Power:	PG2
Reset:	soft

These are the weights contained in the lookup up table (LUT) used in pipe color gamut enhancement. LUT index 0 contains the weight for the least saturated colors, and LUT index 16 contains the weight for the most saturated colors. Weight values can range from 00000b (100% of the enhanced output color is from the pipe gamma and CSC output corrected color) to 100000b (100% of the enhanced output color is from the pipe gamma and CSC input color).

Restriction
The weight values should only be changed while color gamut enhancement is disabled, otherwise screen artifacts may show temporarily.

DWord	Bit	Description
0	31:30	**Reserved** Format: MBZ
	29:24	**CGE Weight Index 3** This is the weight value for this color gamut enhancement LUT index.
	23:22	**Reserved** Format: MBZ

CGE_WEIGHT		
	21:16	**CGE Weight Index 2** This is the weight value for this color gamut enhancement LUT index.
	15:14	**Reserved** Format: MBZ
	13:8	**CGE Weight Index 1** This is the weight value for this color gamut enhancement LUT index.
	7:6	**Reserved** Format: MBZ
	5:0	**CGE Weight Index 0** This is the weight value for this color gamut enhancement LUT index.
1	31:30	**Reserved** Format: MBZ
	29:24	**CGE Weight Index 7** This is the weight value for this color gamut enhancement LUT index.
	23:22	**Reserved** Format: MBZ
	21:16	**CGE Weight Index 6** This is the weight value for this color gamut enhancement LUT index.
	15:14	**Reserved** Format: MBZ
	13:8	**CGE Weight Index 5** This is the weight value for this color gamut enhancement LUT index.
	7:6	**Reserved** Format: MBZ
	5:0	**CGE Weight Index 4** This is the weight value for this color gamut enhancement LUT index.
2	31:30	**Reserved** Format: MBZ
	29:24	**CGE Weight Index 11** This is the weight value for this color gamut enhancement LUT index.
	23:22	**Reserved** Format: MBZ
	21:16	**CGE Weight Index 10** This is the weight value for this color gamut enhancement LUT index.
	15:14	**Reserved** Format: MBZ
	13:8	**CGE Weight Index 9** This is the weight value for this color gamut enhancement LUT index.

CGE_WEIGHT

	7:6	**Reserved** Format: MBZ
	5:0	**CGE Weight Index 8** This is the weight value for this color gamut enhancement LUT index.
3	31:30	**Reserved** Format: MBZ
	29:24	**CGE Weight Index 15** This is the weight value for this color gamut enhancement LUT index.
	23:22	**Reserved** Format: MBZ
	21:16	**CGE Weight Index 14** This is the weight value for this color gamut enhancement LUT index.
	15:14	**Reserved** Format: MBZ
	13:8	**CGE Weight Index 13** This is the weight value for this color gamut enhancement LUT index.
	7:6	**Reserved** Format: MBZ
	5:0	**CGE Weight Index 12** This is the weight value for this color gamut enhancement LUT index.
4	31:6	**Reserved** Format: MBZ
	5:0	**CGE Weight Index 16** This is the weight value for this color gamut enhancement LUT index.

Class Code

CC_0_2_0_PCI - Class Code

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00030000
Size (in bits):	24
Address:	00009h

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

DWord	Bit	Description
0	23:16	**Base Class Code** Default Value: 00000011b Access: RO Variant This is an 8-bit value that indicates the base class code. When MGGC0[VAMEN] is 0 this code has the value 03h, indicating a Display Controller. When MGGC0[VAMEN] is 1 this code has the value 04h, indicating a Multimedia Device.
	15:8	**Sub-Class Code** Default Value: 00000000b Access: RO Variant When MGGC0[VAMEN] is 0 this value will be determined based on Device 0 GGC register, GMS and IVD fields. 00h: VGA compatible 80h: Non VGA (GMS = "00h" or IVD = "1b") When MGGC0[VAMEN] is 1, this value is 80h, indicating other multimedia device.
	7:0	**Programming Interface** Default Value: 00000000b Access: RO When MGGC0[VAMEN] is 0 this value is 00h, indicating a Display Controller. When MGGC0[VAMEN] is 1 this value is 00h, indicating a NOP.

Clipper Invocation Counter

CL_INVOCATION_COUNT - Clipper Invocation Counter	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02338h
Valid Projects:	

This register stores the count of objects entering the Clipper stage. This register is part of the context save and restore.

DWord	Bit	Description
0	63:32	**CL Invocation Count Report UDW** Number of objects entering the clipper stage. Updated only when Statistics Enable is set in CLIP_STATE (see the Clipper Chapter in the 3D Volume.)
	31:0	**CL Invocation Count Report LDW** Number of objects entering the clipper stage. Updated only when Statistics Enable is set in CLIP_STATE (see the Clipper Chapter in the 3D Volume.)

Clipper Primitives Counter

CL_PRIMITIVES_COUNT - Clipper Primitives Counter	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02340h
Valid Projects:	

This register reflects the total number of primitives that have been output by the clipper. This register is part of the context save and restore.

DWord	Bit	Description
0	63:32	**Clipped Primitives Output Count UDW** Total number of primitives output by the clipper stage. This count is updated for every primitive output by the clipper stage, as long as Statistics Enable is set in SF_STATE (see the Clipper and SF Chapters in the 3D Volume.)
	31:0	**Clipped Primitives Output Count LDW** Total number of primitives output by the clipper stage. This count is updated for every primitive output by the clipper stage, as long as Statistics Enable is set in SF_STATE (see the Clipper and SF Chapters in the 3D Volume.)

Clock Gating Messages

CGMSG - Clock Gating Messages

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	08104h

Clock Gating Messages Register

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:10	**Reserved** Access: RO Reserved
	9	**Media sampler Clock gating control message** Access: R/W Gate Media sampler Clock Message : '0' : Clock Un-gate Request (un-gates the scmsclk clock) '1' : Clock Gate Request (gates the scmsclk clock)
	8	**SFC 1 Clock gating control message** Access: R/W Gate SFC 1 (2nd Vbox) Clock gate Message : '0' : SFC 1 Clock Un-gate Request (un-gates the cmclk clock in the 2nd Media block) '1' : SFC 1 Clock Gate Request (gates the cmclk clockin the 2nd Media block)
	7	**SFC 0 Clock gating control message** Access: R/W Gate SFC 0 (1st Vbox) Clock gate Message : '0' : SFC 0 Clock Un-gate Request (un-gates the cmclk clock in the 1st Media block) '1' : SFC 0 Clock Gate Request (gates the cmclk clockin the 1st Media block)

CGMSG - Clock Gating Messages

	6	**Media 1 Clock gating control message** Access: R/W Gate Media 1 (2nd Vbox) Clock Message : '0' : Media 1 Clock Un-gate Request (un-gates the cmclk clock in the 2n Media block) '1' : Media 1 Clock Gate Request (gates the cmclk clockin the 2nd Media block)
	5	**Reserved**
	4	**Reserved**
	3	**Fix Function Clock gating Control Message** Access: R/W Gate Fix Clock Message : '0' : Fix Clock Un-gate Request (un-gates the cfclk/cf2xclk clock) '1' : Fix Clock Gate Request (gates the cfclk/cf2xclk clock)
	2	**VEbox Clock gating Control message** Access: R/W Gate VE-box Clock Message : '0' : VEbox Clock Un-gate Request (un-gates the cvclk clock) '1' : VEbox Clock Gate Request (gates the cvclk clock)
	1	**Media 0 Clock Gating Control Message** Access: R/W Gate Media Clock Message : '0' : Media 0 Clock Un-gate Request (un-gates the cmclk clock) '1' : Media 0 Clock Gate Request (gates the cmclk clock)
	0	**Row Clock Gating Control Message** Access: R/W Gate Row Clocks Message : '0' : Row Clock Un-gate Request (un-gates the crclk and cr2xclk clocks) '1' : Row Clock Gate Request (gates the crclk and cr2xclk clocks)

Color/Depth Write FIFO Watermarks

CZWMRK - Color/Depth Write FIFO Watermarks

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	04060h

This register is directly mapped to the current Virtual Addresses in the MTTLB (Texture and constant cache TLB).

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:18	**Color Wr Burst Size** This is the maximum size of the requests burst, from the last High Watermark trip, before reevaluating the High Watermark again.
	17:16	**Reserved** Format: MBZ
	15:12	**Color Wr FIFO High Watermark** This is the number of accumulated Color writes that will trigger a Burst of Z Writes.
	11:6	**Z Wr Burst Size** This is the maximum size of the requests burst, from the last High Watermark trip, before reevaluating the High Watermark again.
	5:4	**Reserved** Format: MBZ
	3:0	**Z Wr FIFO High Watermark** This is the number of accumulated Depth writes that will trigger a Burst of Z Writes.

Config to MCI HI

CFGTOMCIDFTHI - Config to MCI HI			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	098A0h		
Config to MCI and DFT Ring			
DWord	**Bit**	**Description**	
0	31	**CFG to MCI HI dispatch**	
		Access:	R/WC
	30	**CFG to MCI HI error clear**	
		Access:	R/WC
	29:20	**RSVD_29_20**	
		Access:	R/WC
	19:0	**MCI DFT Ring Write data**	
		Access:	R/WC

Config to MCI LO

CFGTOMCIDFTLO - Config to MCI LO			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0989Ch		
Config to MCI and DFT Ring			
DWord	**Bit**	**Description**	
0	31	**CFG to MCI LO dispatch**	
		Access:	R/WC
	30:0	**MCI DFT Ring Write data**	
		Access:	R/WC

Config to MCI STATUS1

CFGTOMCIDFTSTATUS1 - Config to MCI STATUS1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	098A4h	
Config to MCI and DFT Ring		
DWord	**Bit**	**Description**
0	31:5	**RSVD_31_5** Access: RO
	4	**Report fifo empty** Access: RO
	3	**Reserved**
	2	**Reserved**
	1	**mci fifo overflow** Access: RO
	0	**Report fifo overflow** Access: RO

Configuration Register0 for RPMunit

CONFIG0 - Configuration Register0 for RPMunit

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	00D00h

Lock bit LOCK applies to all RW/L fields in this register. Lock is overridden during context restore.

DWord	Bit	Description
0	31	**Lock for RW/L Fields in this Register** Access: R/W Lock 0 = Bits of CONFIG0 register are R/W. 1 = All bits of CONFIG0 register are RO (including this lock bit). Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). Lock is reset on a restore after context is captured.
	30	**Engineering Sample/Pre-Production part Indicator** Access: R/W Lock Bit30 will be written by BIOS to indicate production/ES sample indication - polarity matches the CPU MSR SR 0xce[27] 1'b0 - production part. 1'b1 - engineering sample/pre-production part.
	29:5	**Placeholder Bits** Access: R/W Lock Placeholder bits for implementation or ECO loops.
	4	**Prevent PowerGate Disable Config Bit** Access: R/W Lock Prevents Powergate License disabling config programming 0xD30[1] 'b0 - PowerGate License handshake enabled /disabled as per 0xD30[1] (default) 'b1 - PowerGate License disable config programming with bit 0xD30[0] is disabled. PowerGate license handshake is always enabled. This bit is is supported from SKLJ0 Stepping.
	3	**Reserved**
	2	**Reserved**
	1	**Reserved**
	0	**Disable TSC Synchronization** Access: R/W Lock 'b0 - TSC synchronization enabled in GT (default) 'b1 - TSC synchronization DISABLED in GT

Configuration Register1 for RPMunit

CONFIG1 - Configuration Register1 for RPMunit

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	00D04h

Lock bit LOCK applies to all RW/L fields in this register. Lock is overridden during context restore.

DWord	Bit	Description
0	31	**Lock for RW/L Fields in this Register** Access: R/W Lock 0 = Bits of CONFIG0 register are R/W. 1 = All bits of CONFIG0 register are RO (including this lock bit). Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). Lock is reset on a restore after context is captured.
	30:9	**Placeholder Bits** Access: R/W Lock Placeholder bits for implementation or ECO loops.
	8:0	**Placeholder Bits** Access: R/W Lock Placeholder bits for implementation or ECO loops.

Configuration Register for RCPunit

RCPCONFIG - Configuration Register for RCPunit

Register Space: MMIO: 0/2/0
Default Value: 0x0000000F
Size (in bits): 32

Address: 00D08h

Unit Level Clock Gating Control Registers

DWord	Bit	Description
0	31:5	**Placeholder Bits** Access: R/W Lock Placeholder bits for implementation or ECO loops.
	4	**Reserved**
	3	**RPMunit Clock Gating Disable in Uncore Well** Default Value: 1b Access: R/W Clock Gating Disable Control: '0': Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality). '1': Clock Gating Disabled. (i.e., clocks are toggling, always) (DEFAULT).
	2	**MGSRunit Clock Gating Disable in Uncore Well** Default Value: 1b Access: R/W Clock Gating Disable Control: '0': Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality). '1': Clock Gating Disabled. (i.e., clocks are toggling, always) (DEFAULT).
	1	**MDRBunit Clock Gating Disable in Uncore Well** Default Value: 1b Access: R/W Clock Gating Disable Control: '0': Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality). '1': Clock Gating Disabled. (i.e., clocks are toggling, always) (DEFAULT).
	0	**MCRunit Clock Gating Disable in Uncore Well** Default Value: 1b Access: R/W Clock Gating Disable Control: '0': Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality). '1': Clock Gating Disabled. (i.e., clocks are toggling, always) (DEFAULT).

Context Load Protocol Register BLT

BLT_CTX_LD_PRTCL - Context Load Protocol Register BLT

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04014h

DWord	Bit	Description
0	31:16	**Mask Bits** Default Value: 0000h Access: RO
	15	**Context Load Protocol Register - BCS 15** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	14	**Context Load Protocol Register - BCS 14** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	13	**Context Load Protocol Register - BCS 13** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	12	**Context Load Protocol Register - BCS 12** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	11	**Context Load Protocol Register - BCS 11** Default Value: 0b Access: R/W For Future Use. This bit is self clear.

BLT_CTX_LD_PRTCL - Context Load Protocol Register BLT

	10	**Context Load Protocol Register - BCS 10** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	9	**Context Load Protocol Register - BCS 9** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	8	**Context Load Protocol Register - BCS 8** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	7	**Context Load Protocol Register - BCS 7** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	6	**Context Load Protocol Register - BCS 6** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	5	**Context Load Protocol Register - BCS 5** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	4	**Context Load Protocol Register - BCS 4** Default Value: 0b Access: R/W For Future Use. This bit is self clear.

BLT_CTX_LD_PRTCL - Context Load Protocol Register BLT

	3	**Context Load Protocol Register - BCS 3** Default Value: 0b Access: R/W Bit 3 = Context Complete. Only valid with Bit 2 asserted and indicates whether the context switching out as complete vs. incomplete. This bit is self clear.
	2	**Context Load Protocol Register - BCS 2** Default Value: 0b Access: R/W Context Load Protocol Register (Written by BCS) Bit 2 = Request from BCS to GAM for context save readiness. GAM will acknowledge appropriated steps taken. This bit is self clear.
	1	**Context Load Protocol Register - BCS 1** Default Value: 0b Access: R/W Context Load Protocol Register (Written by BCS) Bit 1 = Context Launched. This bit is self clear.
	0	**Context Load Protocol Register - BCS 0** Default Value: 0b Access: R/W Context Load Protocol Register (Written by BCS) Bit 0 = Context Available. This bit is self clear.

Context Load Protocol Register CS

GFX_CTX_LD_PRTCL - Context Load Protocol Register CS

Register Space: MMIO: 0/2/0
Default Value: 0x00000000
Size (in bits): 32

Address: 04004h

DWord	Bit	Description
0	31:16	**Mask Bits** Default Value: 0000h Access: RO
	15	**Context Load Protocol Register - CS 15** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	14	**Context Load Protocol Register - CS 14** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	13	**Context Load Protocol Register - CS 13** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	12	**Context Load Protocol Register - CS 12** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	11	**Context Load Protocol Register - CS 11** Default Value: 0b Access: R/W For Future Use. This bit is self clear.

GFX_CTX_LD_PRTCL - Context Load Protocol Register CS

	10	**Context Load Protocol Register - CS 10** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	9	**Context Load Protocol Register - CS 9** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	8	**Context Load Protocol Register - CS 8** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	7	**Context Load Protocol Register - CS 7** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	6	**Context Load Protocol Register - CS 6** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	5	**Context Load Protocol Register - CS 5** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	4	**Context Load Protocol Register - CS 4** Default Value: 0b Access: R/W For Future Use. This bit is self clear.

GFX_CTX_LD_PRTCL - Context Load Protocol Register CS

	3	**Context Load Protocol Register - CS 3** Default Value: 0b Access: R/W Bit 3 = Context Complete. Only valid with Bit 2 asserted and indicates whether the context switching out as complete vs. incomplete. This bit is self clear.
	2	**Context Load Protocol Register - CS 2** Default Value: 0b Access: R/W Context Load Protocol Register (Written by CS) Bit 2 = Request from CS to GAM for context save readiness. GAM will acknowledge appropriated steps taken. This bit is self clear.
	1	**Context Load Protocol Register - CS 1** Default Value: 0b Access: R/W Context Load Protocol Register (Written by CS) Bit 1 = Context Launched. This bit is self clear.
	0	**Context Load Protocol Register - CS 0** Default Value: 0b Access: R/W Context Load Protocol Register (Written by CS) Bit 0 = Context Available. This bit is self clear.

Context Load Protocol Register VCS0

MFX0_CTX_LD_PRTCL - Context Load Protocol Register VCS0

Register Space: MMIO: 0/2/0
Default Value: 0x00000000
Size (in bits): 32

Address: 04008h

DWord	Bit	Description
0	31:16	**Mask Bits** Default Value: 0000h Access: RO
	15	**Context Load Protocol Register - VCS0 15** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	14	**Context Load Protocol Register - VCS0 14** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	13	**Context Load Protocol Register - VCS0 13** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	12	**Context Load Protocol Register - VCS0 12** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	11	**Context Load Protocol Register - VCS0 11** Default Value: 0b Access: R/W For Future Use. This bit is self clear.

MFX0_CTX_LD_PRTCL - Context Load Protocol Register VCS0

10	**Context Load Protocol Register - VCS0 10** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
9	**Context Load Protocol Register - VCS0 9** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
8	**Context Load Protocol Register - VCS0 8** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
7	**Context Load Protocol Register - VCS0 7** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
6	**Context Load Protocol Register - VCS0 6** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
5	**Context Load Protocol Register - VCS0 5** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
4	**Context Load Protocol Register - VCS0 4** Default Value: 0b Access: R/W For Future Use. This bit is self clear.

MFX0_CTX_LD_PRTCL - Context Load Protocol Register VCS0

	3	**Context Load Protocol Register - VCS0 3** Default Value: 0b Access: R/W Bit 3 = Context Complete. Only valid with Bit 2 asserted and indicates whether the context switching out as complete vs. incomplete. This bit is self clear.
	2	**Context Load Protocol Register - VCS0 2** Default Value: 0b Access: R/W Context Load Protocol Register (Written by VCS0) Bit 2 = Request from VCS0 to GAM for context save readiness. GAM will acknowledge appropriated steps taken. This bit is self clear.
	1	**Context Load Protocol Register - VCS0 1** Default Value: 0b Access: R/W Context Load Protocol Register (Written by VCS0) Bit 1 = Context Launched. This bit is self clear.
	0	**Context Load Protocol Register - VCS0 0** Default Value: 0b Access: R/W Context Load Protocol Register (Written by VCS0) Bit 0 = Context Available. This bit is self clear.

Context Load Protocol Register VCS1

MFX1_CTX_LD_PRTCL - Context Load Protocol Register VCS1

Register Space: MMIO: 0/2/0
Default Value: 0x00000000
Size (in bits): 32

Address: 0400Ch

DWord	Bit	Description
0	31:16	**Mask Bits** Default Value: 0000h Access: RO
	15	**Context Load Protocol Register - VCS1 15** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	14	**Context Load Protocol Register - VCS1 14** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	13	**Context Load Protocol Register - VCS1 13** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	12	**Context Load Protocol Register - VCS1 12** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	11	**Context Load Protocol Register - VCS1 11** Default Value: 0b Access: R/W For Future Use. This bit is self clear.

MFX1_CTX_LD_PRTCL - Context Load Protocol Register VCS1

	10	**Context Load Protocol Register - VCS1 10** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	9	**Context Load Protocol Register - VCS1 9** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	8	**Context Load Protocol Register - VCS1 8** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	7	**Context Load Protocol Register - VCS1 7** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	6	**Context Load Protocol Register - VCS1 6** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	5	**Context Load Protocol Register - VCS1 5** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	4	**Context Load Protocol Register - VCS1 4** Default Value: 0b Access: R/W For Future Use. This bit is self clear.

MFX1_CTX_LD_PRTCL - Context Load Protocol Register VCS1

	3	**Context Load Protocol Register - VCS1 3** Default Value: 0b Access: R/W Bit 3 = Context Complete. Only valid with Bit 2 asserted and indicates whether the context switching out as complete vs. incomplete. This bit is self clear.
	2	**Context Load Protocol Register - VCS1 2** Default Value: 0b Access: R/W Context Load Protocol Register (Written by VCS1) Bit 2 = Request from VCS1 to GAM for context save readiness. GAM will acknowledge appropriated steps taken. This bit is self clear.
	1	**Context Load Protocol Register - VCS1 1** Default Value: 0b Access: R/W Context Load Protocol Register (Written by VCS1) Bit 1 = Context Launched This bit is self clear.
	0	**Context Load Protocol Register - VCS1 0** Default Value: 0b Access: R/W Context Load Protocol Register (Written by VCS1) Bit 0 = Context Available. This bit is self clear.

Context Load Protocol Register VEBX

VEBX_CTX_LD_PRTCL - Context Load Protocol Register VEBX

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04010h

DWord	Bit	Description
0	31:16	**Mask Bits** Default Value: 0000h Access: RO
	15	**Context Load Protocol Register - VEBX 15** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	14	**Context Load Protocol Register - VEBX 14** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	13	**Context Load Protocol Register - VEBX 13** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	12	**Context Load Protocol Register - VEBX 12** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	11	**Context Load Protocol Register - VEBX 11** Default Value: 0b Access: R/W For Future Use. This bit is self clear.

VEBX_CTX_LD_PRTCL - Context Load Protocol Register VEBX

	10	**Context Load Protocol Register - VEBX 10** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	9	**Context Load Protocol Register - VEBX 9** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	8	**Context Load Protocol Register - VEBX 8** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	7	**Context Load Protocol Register - VEBX 7** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	6	**Context Load Protocol Register - VEBX 6** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	5	**Context Load Protocol Register - VEBX 5** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	4	**Context Load Protocol Register - VEBX 4** Default Value: 0b Access: R/W For Future Use. This bit is self clear.

VEBX_CTX_LD_PRTCL - Context Load Protocol Register VEBX

	3	**Context Load Protocol Register - VEBX 3** Default Value: 0b Access: R/W Bit 3 = Context Complete. Only valid with Bit 2 asserted and indicates whether the context switching out as complete vs. incomplete. This bit is self clear.
	2	**Context Load Protocol Register - VEBX 2** Default Value: 0b Access: R/W Context Load Protocol Register (Written by VEBX) Bit 2 = Request from VEBX to GAM for context save readiness. GAM will acknowledge appropriated steps taken. This bit is self clear.
	1	**Context Load Protocol Register - VEBX 1** Default Value: 0b Access: R/W Context Load Protocol Register (Written by VEBX) Bit 1 = Context Launched. This bit is self clear.
	0	**Context Load Protocol Register - VEBX 0** Default Value: 0b Access: R/W Context Load Protocol Register (Written by VEBX) Bit 0 = Context Available. This bit is self clear.

Context Restore Request To TDL

TDL_CONTEXT_RESTORE - Context Restore Request To TDL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	WO
Size (in bits):	32
Address:	0E440h
Valid Projects:	

DWord	Bit	Description
0	31:17	**Reserved** Format: MBZ
	16	**Context Restore Mask** Value: 1 — Name: — Description: Bit 0 and bit 16 both need to be 1 for Context restore request
	15:1	**Reserved** Format: MBZ
	0	**Context Restore** Value: 1 — Name: — Description: Bit 0 and bit 16 both need to be 1 for Context restore request

Context Save Request To TDL

TDL_CONTEXT_SAVE - Context Save Request To TDL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	WO
Size (in bits):	32
Address:	0E4FCh
Valid Projects:	

DWord	Bit	Description
0	31:17	**Reserved** Format: MBZ
	16	**Context Save Mask** Value: 1 — Name: — Description: Bit 0 and Bit 16 both need to be '1' for Context Save Request
	15:1	**Reserved** Format: MBZ
	0	**Context Save** Value: 1 — Name: — Description: Bit 0 and Bit 16 both need to be '1' for Context Save Request

Context Sizes

CXT_SIZE - Context Sizes

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x015E6600
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	021A8h

The actual size of a logical rendering context is the amount of data stored/restored during a context switch and is measured in 64B cache lines.

This register will be power context save/restored. Note that this register will default to the correct value, so software should not have to modify it.

DWord	Bit	Description
0	31:28	**Reserved** Format: MBZ
	27:16	**Render Engine Context Size** This field indicates the size of the render engine context data that needs to be save/restored when extended mode is not enabled for a context; this excludes URB context size. Note that this excludes the ring context image size and the engine context saved by CSFE. Value: 15Eh — Name: **[Default]**
	15:8	**SOL Context Offset** This field indicates the cacheline aligned offset of the SOL context in the render context image starting from Ring Context. Note that in execlist of scheduling Ring context itself is at 4KB offset from LRCA. Value: 66h — Name: **[Default]**
	7:0	**Reserved** Format: MBZ

Context Status1 for RCS-BE

CS_CONTEXT_STATUS1 - Context Status1 for RCS-BE

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	r/w
Size (in bits):	32
Trusted Type:	1
Address:	02184h
Valid Projects:	

This register is for maintaining HW internal state of RCS-BE per context. This register is context save/restore per context. This register should not be written by SW.

DWord	Bit	Description
0	31:16	**Mask Bits** Access: WO Format: Mask Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:8	**Reserved** Format: PBC
	7	**Preempted Batch Buffer RS Control Stop Flag** Format: Flag This field specifies RS Control Stop Flag when a batch buffer is preempted. This is for HW internal use and should not be written by SW. This bit gets reset when RS_PREEMPTED field of RS_PREEMPT_STATUS is written Zero. This bit is set by: • Ctx restore of this bit • MI_RS_CONTROL_STOP (except for the ctx restore command) This bit is cleared by: • MI_RS_CONTROL_START • Any Batch start except resubmitted RS batch • A batch end that doesn't include preemption • Ctx save Writing 0 to bit[0] of the RS STATUS register
	6	**Pending Indirect State Dirty Bit** Format: U1 This field keeps track of whether or not an indirect state pointer command has been parsed in the current context. Clears either on a context save or explicitly through a flush command.

CS_CONTEXT_STATUS1 - Context Status1 for RCS-BE

	5:0	**Pending Indirect State Counter** Access: RO Format: U6 This field keeps track of the maximum number of indirect state pointers pending in the system. When the register is saved/restored, it saves either a value of 1 or 0.

Context Status Buffer Contents

CTXT_ST_BUF - Context Status Buffer Contents

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000
Access:	R/W
Size (in bits):	384
Trusted Type:	1
Address:	02370h-0239Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_RCSUNIT
Address:	12370h-1239Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_VCSUNIT0
Address:	1A370h-1A39Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_VECSUNIT
Address:	1C370h-1C39Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_VCSUNIT1
Address:	22370h-2239Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_BCSUNIT

Contents of the Execlist 0 in HW.

Programming Notes

This structure contains the Context Switch status locations Context Status 0 to Context Status 5.

DWord	Bit	Description
0	63:32	**Context Status 0 UDW** Format: Context Status
	31:0	**Context Status 0 LDW** Format: Context Status
1	63:32	**Context Status 1 UDW** Format: Context Status
	31:0	**Context Status 1 LDW** Format: Context Status

CTXT_ST_BUF - Context Status Buffer Contents		
2	63:32	**Context Status 2 UDW** Format: Context Status
	31:0	**Context Status 2 LDW** Format: Context Status
3	63:32	**Context Status 3 UDW** Format: Context Status
	31:0	**Context Status 3 LDW** Format: Context Status
4	63:32	**Context Status 4 UDW** Format: Context Status
	31:0	**Context Status 4 LDW** Format: Context Status
5	63:32	**Context Status 5 UDW** Format: Context Status
	31:0	**Context Status 5 LDW** Format: Context Status

Context Timestamp Count

CTX_TIMESTAMP - Context Timestamp Count	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	023A8h-023ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_RCSUNIT
Address:	123A8h-123ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_VCSUNIT0
Address:	1A3A8h-1A3ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_VECSUNIT
Address:	1C3A8h-1C3ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_VCSUNIT1
Address:	223A8h-223ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_BCSUNIT

This register provides a mechanism to obtain cumulative run time of a GPU context on HW. This register gets context save/restored on a context switch. SW must reset this register on very first submission of a context to HW, then afterwards gets context save/restored maintaining the cumulative run time of the corresponding context. This register (effectively) counts at a constant frequency by adjusting the increment amount according to the actual reference clock frequency. SW therefore does not need to know the reference clock frequency. This register gets reset on an engine reset.

This register is context save restore on a context switch.

DWord	Bit	Description
0	31:0	**Timestamp Value** Format: U32 The granularity of this toggle is at the rate of the bit 3 in the "Reported Timestamp Count" register(0x2358).. The toggle will be 8 times slower that "Reported Timestamp Count". The granularity of the time stamp base unit for "Reported Timestamp Count" is defined in the “Timestamp Bases” subsection in Power Management chapter.

Control Register for Fault and Halt

FH_MODE - Control Register for Fault and Halt

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	042A4h

This register is used to control the different fault and halt modes.

DWord	Bit	Description
0	31	**Disable Blocking Page Fault** Default Value: 0b Access: R/W When disabled h/w would not set the "blocking fault" bit in the streaming page fault descriptor for the fault and halt generated page faults. FH_MODE: 0: Enable "blocking page fault" indicator for Fault and Halt 1: Disable "blocking page fault" indicator for Fault and Halt
	30	**Enable Forward Progress under F and H based page faults - Render engine only** Default Value: 0b Access: R/W Once set, the page walker will not wait for accesses that are hitting page faults on fault and halt cases, and marking accesses as "invalid" making forward progress. Such case may corrupt the frame or may require TDR if surface is CRITICAL. Invalid accesses will return garbage content. GFX Driver can set this bit in the middle of an active context, h/w should clear the bit when an active context completes. Usage model will be as driver hits a fault and halt and interrupts the driver, driver will set this bit is it needs forward progress. The behavior should only be applicable to the running context. FWDPROG: 0: Forwards progress under fault and halt is only possible with page response. 1: Enable forward progress under falt and halt w/o the need of paging services.
	29	**Enable Interrupt Generation** Default Value: 0b Access: R/W Enable interrupt generation on fault and halt page when resume mode is enabled: An interrupt can be generated on page fault with the fault and halt mode when hardware is programmed to resume(rather than wait/halt). The generation of interrupt needs to be explicitly enabled via this register bit. ENINTR: 0: No interrupt is generated on fault and halt page fault. 1: Enable interrupt generation for fault and halt based page faults when h/w is programmed to resume.

FH_MODE - Control Register for Fault and Halt

	28:0	**Reserved FH_MODE Bits 28** Default Value: 00000000000000000000000000000b Access: R/W Future Use.

Count Active Channels Dispatched

TS_GPGPU_THREADS_DISPATCHED - Count Active Channels Dispatched

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02290h

This register is used to count the number of active channels that TS sends for dispatch. For each dispatch the active bits in the execution mask are summed and added to this register. This register is reset when a write occurs to 2290h

DWord	Bit	Description
0	63:32	**GPGPU_THREADS_DISPATCHED UDW** Format: U32 This count is increased by the number of active bits in the execution mask each time the TS sends a GPGPU dispatch.
	31:0	**GPGPU_THREADS_DISPATCHED LDW** Format: U32 This count is increased by the number of active bits in the execution mask each time the TS sends a GPGPU dispatch.

CSC_COEFF

CSC_COEFF	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000
Access:	Double Buffered
Size (in bits):	192
Double Buffer Update Point:	Start of vertical blank after armed
Double Buffer Armed By:	Write to CSC_MODE
Address:	49010h-49027h
Name:	Pipe CSC Coefficients
ShortName:	CSC_COEFF_A
Power:	PG1
Reset:	soft
Address:	49110h-49127h
Name:	Pipe CSC Coefficients
ShortName:	CSC_COEFF_B
Power:	PG2
Reset:	soft
Address:	49210h-49227h
Name:	Pipe CSC Coefficients
ShortName:	CSC_COEFF_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:16	**RY** Format: CSC COEFFICIENT FORMAT
	15:0	**GY** Format: CSC COEFFICIENT FORMAT
1	31:16	**BY** Format: CSC COEFFICIENT FORMAT
	15:0	**Reserved** Format: MBZ
2	31:16	**RU** Format: CSC COEFFICIENT FORMAT

CSC_COEFF		
	15:0	**GU** Format: CSC COEFFICIENT FORMAT
3	31:16	**BU** Format: CSC COEFFICIENT FORMAT
	15:0	**Reserved** Format: MBZ
4	31:16	**RV** Format: CSC COEFFICIENT FORMAT
	15:0	**GV** Format: CSC COEFFICIENT FORMAT
5	31:16	**BV** Format: CSC COEFFICIENT FORMAT
	15:0	**Reserved** Format: MBZ

CSC_MODE

CSC_MODE

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank

Address:	49028h-4902Bh
Name:	Pipe CSC Mode
ShortName:	CSC_MODE_A
Power:	PG1
Reset:	soft

Address:	49128h-4912Bh
Name:	Pipe CSC Mode
ShortName:	CSC_MODE_B
Power:	PG2
Reset:	soft

Address:	49228h-4922Bh
Name:	Pipe CSC Mode
ShortName:	CSC_MODE_C
Power:	PG2
Reset:	soft

Description
Writes to this register arm CSC registers for this pipe.

DWord	Bit	Description
0	31:2	**Reserved**
	1	**CSC Position** Selects the CSC position in the pipe. This is ignored when split gamma mode is selected in the pipe config register.

Value	Name	Description
0b	CSC After	CSC is after gamma
1b	CSC Before	CSC is before gamma

0	**Reserved**

Format:	MBZ

CSC_POSTOFF

CSC_POSTOFF

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000, 0x00000000, 0x00000000
Access:	Double Buffered
Size (in bits):	96
Double Buffer Update Point:	Start of vertical blank after armed
Double Buffer Armed By:	Write to CSC_MODE

Address:	49040h-4904Bh
Name:	Pipe CSC Post-Offsets
ShortName:	CSC_POSTOFF_A
Power:	PG1
Reset:	soft

Address:	49140h-4914Bh
Name:	Pipe CSC Post-Offsets
ShortName:	CSC_POSTOFF_B
Power:	PG2
Reset:	soft

Address:	49240h-4924Bh
Name:	Pipe CSC Post-Offsets
ShortName:	CSC_POSTOFF_C
Power:	PG2
Reset:	soft

The post-offset is intended to add an offset from 0 on the Y or RGB channels and to convert UV channels from 2's complement to excess 0.5 as they exit pipe color space conversion (CSC).

DWord	Bit	Description
0	31:13	**Reserved** Format: MBZ
	12:0	**PostCSC High Offset** This value is used to give an offset to the high color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
1	31:13	**Reserved** Format: MBZ

CSC_POSTOFF		
	12:0	**PostCSC Medium Offset** This value is used to give an offset to the medium color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
2	31:13	**Reserved** Format: MBZ
	12:0	**PostCSC Low Offset** This value is used to give an offset to the low color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).

CSC_PREOFF

CSC_PREOFF

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000, 0x00000000, 0x00000000
Access:	Double Buffered
Size (in bits):	96
Double Buffer Update Point:	Start of vertical blank after armed
Double Buffer Armed By:	Write to CSC_MODE

Address:	49030h-4903Bh
Name:	Pipe CSC Pre-Offsets
ShortName:	CSC_PREOFF_A
Power:	PG1
Reset:	soft

Address:	49130h-4913Bh
Name:	Pipe CSC Pre-Offsets
ShortName:	CSC_PREOFF_B
Power:	PG2
Reset:	soft

Address:	49230h-4923Bh
Name:	Pipe CSC Pre-Offsets
ShortName:	CSC_PREOFF_C
Power:	PG2
Reset:	soft

The pre-offset is intended to remove an offset from 0 on the Y or RGB channels and to convert UV channels from excess 0.5 to 2's complement as they enter pipe color space conversion (CSC).

DWord	Bit	Description
0	31:13	**Reserved** Format: MBZ
	12:0	**PreCSC High Offset** This value is used to give an offset to the high color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
1	31:13	**Reserved** Format: MBZ

CSC_PREOFF		
	12:0	**PreCSC Medium Offset** This value is used to give an offset to the medium color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
2	31:13	**Reserved** Format: MBZ
	12:0	**PreCSC Low Offset** This value is used to give an offset to the low color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).

CSPREEMPT

CSPREEMPT - CSPREEMPT

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1

Address:	024B0h
Name:	CSPREEMPT
ShortName:	CSPREEMPT

Address:	224B0h
Name:	BCSPREEMPT
ShortName:	BCSPREEMPT

Address:	124B0h
Name:	VCSPREEMPT
ShortName:	VCSPREEMPT

Address:	1C4B0h
Name:	VCS2PREEMPT
ShortName:	VCS2PREEMPT
Valid Projects:	[SKL:GT3, SKL:GT4]

Address:	1A4B0h
Name:	VECSPREEMPT
ShortName:	VECSPREEMPT

Programming Notes

This is for HW internal usage and must not be written by SW.

DWord	Bit	Description
0	31:16	**Mask Bits** Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:1	**Reserved** Format: MBZ

CSPREEMPT - CSPREEMPT		
	0	**Unnamed** Format: Disable This is a message bit written by the cross CS in case of GT4-CBR/SFR mode of operation. To set this bit both bit[0] and bit[16] (mask) needs to be set. This bit set indicates CS in other GT has reached a preemption point. This bit gets reset by CS when preemption takes place.

CTX REG 1

CTXREG1 - CTX REG 1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x0000026E [SKL:GT2, SKL:GT3, SKL:GT4]	
Size (in bits):	32	
Address:	00FF4h-00FF7h	
DWord	**Bit**	**Description**
0	31:0	**CTXSIZE** Default Value: 0000026Eh Project: DevSKL:GT2, DevSKL:GT3, DevSKL:GT4 Access: RO Register to store value for number of CTX DWORD.

CTX reg 2

CTXREG2 - CTX reg 2		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00FFCh-00FFFh	
DWord	**Bit**	**Description**
0	31:1	**CTX Register 2** Access: R/W RSVD
	0	**CTXRESTOREDONE** Access: R/W CTX restore done bit. Will be written to 1 during the last CTX restore cycle.

CUR_BASE

CUR_BASE

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled

Address:	70084h-70087h
Name:	Cursor Base Address
ShortName:	CUR_BASE_A
Power:	PG1
Reset:	soft

Address:	71084h-71087h
Name:	Cursor Base Address
ShortName:	CUR_BASE_B
Power:	PG2
Reset:	soft

Address:	72084h-72087h
Name:	Cursor Base Address
ShortName:	CUR_BASE_C
Power:	PG2
Reset:	soft

Writes to this register arm cursor registers for this pipe.

DWord	Bit	Description
0	31:12	**Cursor Base 31 12** Format: GraphicsAddress[31:12] This field specifies bits 31:12 of the graphics address of the base of the cursor for hi-res mode. When performing 180 degree rotation, this address does not need to change, hardware will internally offset to start from the last pixel of the last line of the cursor. **Workaround** To prevent false VT-d type 6 errors, use 64KB address alignment and allocate an extra 2 Page Table Entries (PTEs) beyond the end of the displayed surface. Only the PTEs will be used, not the pages themselves. **Restriction**

CUR_BASE		
		The cursor surface address must be 4K byte aligned. The cursor must be in linear memory, it cannot be tiled.
	11:7	**Reserved**
	6:4	**Reserved**
	3	**Reserved**
	2	**Reserved**
	1:0	**Reserved**

CUR_CTL

CUR_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to CUR_BASE or cursor not enabled

Address:	70080h-70083h
Name:	Cursor Control
ShortName:	CUR_CTL_A
Power:	PG1
Reset:	soft

Address:	71080h-71083h
Name:	Cursor Control
ShortName:	CUR_CTL_B
Power:	PG2
Reset:	soft

Address:	72080h-72083h
Name:	Cursor Control
ShortName:	CUR_CTL_C
Power:	PG2
Reset:	soft

The cursor is enabled by programming a valid cursor mode in the cursor mode select fields. The cursor is disabled by programming all 0s in the cursor mode select fields.

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Reserved**
	26	**Gamma Enable** This bit enables pipe gamma correction for the cursor pixel data. In VGA pop-up operation, the cursor data will always bypass gamma. Value: 0b — Name: Disable Value: 1b — Name: Enable
	25	**Reserved**

CUR_CTL

	24	**Pipe CSC Enable** This bit enables pipe color space conversion for the cursor pixel data. **Value** / **Name** 0b – Disable 1b – Enable
	23	**Allow Double Buffer Update Disable** Access: R/W This field controls whether double buffer updates are allowed to be disabled for this cursor. The DOUBLE_BUFFER_CTL register can be configured to globally disable double buffer updates for resources that allow them to be disabled. **Value** / **Name** 0b – Not Allowed 1b – Allowed
	22:16	**Reserved**
	15	**180 Rotation** This mode causes the cursor image to be rotated 180 degrees. In addition to setting this bit, the cursor position must be adjusted to match the physical orientation of the display. **Value** / **Name** 0b – No rotation 1b – 180 degree rotation **Restriction** Only 32 bits per pixel cursors can be rotated. This field must be zero when the cursor format is 2 bits per pixel.
	14	**Trickle Feed Enable** **Value** / **Name** 0b – Enable 1b – Disable **Restriction** Do not program this field to 1b.
	13:12	**Reserved**

CUR_CTL

11:10 **Force Alpha Plane Select**

This field selects which planes the cursor alpha value will be forced for. It is used together with the Force Alpha Value field.

Value	Name	Description
00b	Disable	Disable alpha forcing
01b	Pipe CSC Enabled	Enable alpha forcing where cursor overlaps a plane that has enabled pipe CSC
10b	Pipe CSC Disabled	Enable alpha forcing where cursor overlaps plane that has disabled pipe CSC
11b	Reserved	Reserved

9:8 **Force Alpha Value**

This field controls the behavior of cursor when alpha blending onto certain plane pixels. It is used together with the Force Alpha Plane Select field.

Value	Name	Description
00b	Disable	Cursor pixels alpha blend normally over any plane.
01b	50	Cursor pixels with alpha >= 50% are made fully opaque where they overlap the selected plane(s). Cursor pixels with alpha < 50% are made fully transparent where they overlap the selected plane(s).
10b	75	Cursor pixels with alpha >= 75% are made fully opaque where they overlap the selected plane(s). Cursor pixels with alpha < 75% are made fully transparent where they overlap the selected plane(s).
11b	100	Cursor pixels with alpha = 100% are made fully opaque where they overlap the selected plane(s). Cursor pixels with alpha < 100% are made fully transparent where they overlap the selected plane(s).

Restriction
Force Alpha is only for use with ARGB cursor formats.

7:6 **Reserved**

5:0 **Cursor Mode Select**

This field selects the cursor mode. Cursor is disabled when the selection is 000000b and enabled when the selection is any other value. The cursor vertical size can be overriden by the size reduction mode.

Value	Name	Description
000000b	Disable	Cursor is disabled
000010b	128x128 32bpp AND/INV	128x128 32bpp AND/INVERT
000011b	256x256 32bpp AND/INV	256x256 32bpp AND/INVERT
000100b	64x64 2bpp 3-color	64x64 2bpp Indexed 3-color and transparency
000101b	64x64 2bpp 2-color	64x64 2bpp Indexed AND/XOR 2-color
000110b	64x64 2bpp 4-color	64x64 2bpp Indexed 4-color
000111b	64x64 32bpp AND/INV	64x64 32bpp AND/INVERT

CUR_CTL

100010b	128x128 32bpp ARGB	128x128 32bpp ARGB (8:8:8:8 MSB-A:R:G:B)
100011b	256x256 32bpp ARGB	256x256 32bpp ARGB (8:8:8:8 MSB-A:R:G:B)
100100b	64x64 32bpp AND/XOR	64x64 32bpp AND/XOR
100101b	128x128 32bpp AND/XOR	128x128 32bpp AND/XOR
100110b	256x256 32bpp AND/XOR	256x256 32bpp AND/XOR
100111b	64x64 32bpp ARGB	64x64 32bpp ARGB (8:8:8:8 MSB-A:R:G:B)
Others	Reserved	Reserved

Programming Notes

INVERT, XOR, and alpha blends may not look as expected when the plane underlying the cursor is YUV or extended range RGB. Out of range RGB values will be clamped prior to alpha blending, INVERT, or XOR with cursor. It is recommended to use Force Alpha when cursor is alpha blending onto an plane of a different color space or extended gamut.

The AND/INVERT format uses the most significant byte (MSB) to control the color. If MSB is 0xFF: Cursor is opaque. Show cursor color from three least significant bytes. If MSB is 0x00: Cursor is transparent. Three least significant bytes must be zero. If MSB is not 0x00 or 0xFF: Cursor inverts the color of the surface underneath.

The AND/XOR format uses the most significant byte (MSB) to control the color. If MSB is 0xFF: Cursor is opaque. Show cursor color from three least significant bytes. If MSB is 0x00: Cursor is transparent. Three least significant bytes must be zero. If MSB is not 0x00 or 0xFF: The three least significant bytes are XOR'd with the color of the surface underneath.

Restriction

The cursor and the top most plane cannot both be enabled at the same time on the same pipe.

CUR_FBC_CTL

CUR_FBC_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to CUR_BASE or cursor not enabled
Address:	700A0h-700A3h
Name:	Cursor FBC Control
ShortName:	CUR_FBC_CTL_A
Power:	PG1
Reset:	soft
Address:	710A0h-710A3h
Name:	Cursor FBC Control
ShortName:	CUR_FBC_CTL_B
Power:	PG2
Reset:	soft
Address:	720A0h-720A3h
Name:	Cursor FBC Control
ShortName:	CUR_FBC_CTL_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31	**Size Reduction Enable** This enables cursor size reduction logic. The cursor engine will fetch and display the programmed reduced number of lines, then go transparent for the rest of the frame. **Value** / **Name** 0b – Disable 1b – Enable **Restriction** Cursor size reduction is not allowed with 2bpp cursor formats or cursor 180 degree rotation. The reduced scan lines field must be programmed with a valid value when cursor size reduction is

CUR_FBC_CTL		
		enabled.
	30:8	**Reserved**
	7:0	**Reduced Scan Lines** This specifies the number of scan lines of cursor data to fetch and display when cursor size reduction is enabled. The value programmed is the size minus one. **Restriction** The minimum size is 8 lines, programmed as 07h. The maximum size can not be greater than the normal size when size reduction is not enabled.

CUR_PAL

CUR_PAL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled
Address:	70090h-7009Fh
Name:	Cursor A Palette
ShortName:	CUR_PAL_A_*
Power:	PG1
Reset:	soft
Address:	71090h-7109Fh
Name:	Cursor B Palette
ShortName:	CUR_PAL_B_*
Power:	PG2
Reset:	soft
Address:	72090h-7209Fh
Name:	Cursor C Palette
ShortName:	CUR_PAL_C_*
Power:	PG2
Reset:	soft

The cursor palette provides color information when using the indexed cursor modes. There are 4 instances of this register format per cursor. The table below describes how the cursor mode and index value will select between the cursor palette colors, AND/XOR, transparency, and destination invert.

Index Value	2 color mode	3 color mode	4 color mode
00	CUR_PAL 0	CUR_PAL 0	CUR_PAL 0
01	CUR_PAL 1	CUR_PAL 1	CUR_PAL 1
10	Transparent	Transparent	CUR_PAL 2
11	Invert Destination	CUR_PAL 3	CUR_PAL 3

DWord	Bit	Description
0	31:24	**Reserved**
	23:16	**Palette Red** This field is the cursor palette red value
	15:8	**Palette Green** This field is the cursor palette green value.

CUR_PAL		
	7:0	**Palette Blue** This field is the cursor palette blue value.

CUR_POS

CUR_POS

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled

Address:	70088h-7008Bh
Name:	Cursor Position
ShortName:	CUR_POS_A
Power:	PG1
Reset:	soft

Address:	71088h-7108Bh
Name:	Cursor Position
ShortName:	CUR_POS_B
Power:	PG2
Reset:	soft

Address:	72088h-7208Bh
Name:	Cursor Position
ShortName:	CUR_POS_C
Power:	PG2
Reset:	soft

This register specifies the screen position of the cursor. The origin of the cursor position is always the upper left corner of the display pipe source image area. When performing 180 degree rotation, the cursor image is rotated by hardware, but the position is not, so it should be adjusted if it is desired to maintain the same apparent position on a physically rotated display.

Restriction
The cursor must have at least a single pixel positioned over the pipe source area.

DWord	Bit	Description
0	31	**Y Position Sign** This specifies the sign of the vertical position of the cursor upper left corner.
	30:28	**Reserved** Format: MBZ
	27:16	**Y Position Magnitude** This specifies the magnitude of the vertical position of the cursor upper left corner in lines.

CUR_POS		
	15	**X Position Sign** This specifies the sign of the horizontal position of the cursor upper left corner.
	14:13	**Reserved** Format: MBZ
	12:0	**X Position Magnitude** This specifies the magnitude of the horizontal position of the cursor upper left corner in pixels.

CUR_SURFLIVE

CUR_SURFLIVE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	700ACh-700AFh
Name:	Cursor Live Base Address
ShortName:	CUR_SURFLIVE_A
Power:	PG1
Reset:	soft
Address:	710ACh-710AFh
Name:	Cursor Live Base Address
ShortName:	CUR_SURFLIVE_B
Power:	PG2
Reset:	soft
Address:	720ACh-720AFh
Name:	Cursor Live Base Address
ShortName:	CUR_SURFLIVE_C
Power:	PG2
Reset:	soft

There is one instance of this register for each pipe.

DWord	Bit	Description
0	31:12	**Live Surface Base Address** This gives the live value of the surface base address as being currently used for the cursor.
	11:0	**Reserved** Format: MBZ

Current Context Register

CCID - Current Context Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02180h-02183h
Name:	Current Context Register
ShortName:	CCID_RCSUNIT
Address:	12180h-12183h
Name:	Current Context Register
ShortName:	CCID_VCSUNIT0
Address:	1A180h-1A183h
Name:	Current Context Register
ShortName:	CCID_VECSUNIT
Address:	1C180h-1C183h
Name:	Current Context Register
ShortName:	CCID_VCSUNIT1
Address:	22180h-22183h
Name:	Current Context Register
ShortName:	CCID_BCSUNIT

Description	Source
This register contains the 4 KB-aligned Graphics Memory Address to which the engine must save/restore its state during IDLE sequencing. This register should be programmed only in ringbuffer mode of scheduling.	
On SKL and its derivatives context address programmed should support a memory surface of size 4KB and with memory surface initialized to zeros (0x0).	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS

Programming Notes	Source
The CCID register must be written directly (via MMIO) or MI_LOAD_REGISTER_IMMEDIATE command as part of the initialization sequence of the command streamer in ring buffer mode of scheduling.	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS
The CCID register must not be written directly (via MMIO) unless the Command Streamer is completely idle (i.e., the Ring Buffer is empty and the pipeline is idle). Note that, under normal conditions, the CCID register should only be updated from the command stream using the MI_SET_CONTEXT command.	RenderCS

DWord	Bit	Description

CCID - Current Context Register

0	31:12	**Context Address** Format: GraphicsAddress[31:12] This field contains the 4 KB-aligned Graphics Memory Address to which the engine must save/restore its state during IDLE sequencing.
	11:10	**Reserved** Source: RenderCS, BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS Format: MBZ
	9	**HD DVD Context** Source: RenderCS Value / Name / Description: 0h – Regular Context 1h – HD DVD Context – Special considerations for TDP allow for higher voltage and frequency.
	9	**Reserved** Source: BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS Format: MBZ
	8	**Reserved8** Source: RenderCS, BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS Format: U1
	7:4	**Reserved** Default Value: 0 Source: RenderCS, BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS
	3	**Extended State Save Enable** Source: RenderCS Format: Enable If set, the extended state identified in the Logical Context Data section of the Memory Data Formats chapter, is saved as part of switching away from this logical context.
	3	**Reserved** Source: BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS Format: MBZ
	2	**Extended State Restore Enable** Source: RenderCS Format: Enable If set, the extended state identified in the Logical Context Data section of the Memory Data Formats chapter, was loaded (or restored) as part of switching to this logical context.

CCID - Current Context Register

	2	**Reserved** Source: BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS Format: MBZ
	1	**Reserved** Source: RenderCS, BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS Format: MBZ
	0	**Valid** Format: U1

Value	Name	Description
0h	Invalid **[Default]**	The other fields of this register are invalid.
1h	Valid	The other fields of this register are valid.

Customizable Event Creation 0-0

CEC0-0 - Customizable Event Creation 0-0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02770h

This register is used to define custom counter event 0, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Format: U11 The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. **Value** / **Name** / **Description** / **Programming Notes** 0b / Pass-through / Input bit is passed through to comparator as is / 1b / Negated / Input bit is negated before passing to comparator / If the input bit is negated using any bit in this field, then the corresponding Consderations bit in the CEC0-1 register must also be set.
	20:19	**Source Select** Format: U2 Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). **Value** / **Name** / **Description** 01b / Prev Event / Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block 11b / Reserved /
	18:3	**Compare Value** Format: U16 The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

CEC0-0 - Customizable Event Creation 0-0

2:0 **Compare Function**

Format:	U3

This field selects the function used by the CEC0 comparator when comparing the compare value to the value active on the CEC0 conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

Customizable Event Creation 1-0

CEC1-0 - Customizable Event Creation 1-0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02778h

This register is used to define custom counter event 1, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Format: U11 The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. **Value / Name / Description / Programming Notes** 0b / Pass-through / Input bit is passed through to comparator as is / 1b / Negated / Input bit is negated before passing to comparator / If the input bit is negated using any bit in this field, then the corresponding Consderations bit in the CEC1-1 register must also be set.
	20:19	**Source Select** Format: U2 Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). **Value / Name / Description** 01b / Prev Event / Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block 11b / Reserved /
	18:3	**Compare Value** Format: U16 The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

CEC1-0 - Customizable Event Creation 1-0

	2:0	**Compare Function** Format: U3 This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

Customizable Event Creation 1-1

CEC1-1 - Customizable Event Creation 1-1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0277Ch

This register configures the input conditioning portion of CEC (custom event creation) block 1, bit definitions in this register refer to the CEC block diagram.

DWord	Bit	Description
0	31:16	**Considerations** This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.

Value	Name	Description
0b	Live	Input bit is not delayed by 1 clock before event calculation
1b	Delayed	Input bit is delayed by 1 clock before event calculation

DWord	Bit	Description
0	15:0	**Mask** This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.

Value	Name	Description
0b	Unmasked	Input bit is considered in event calculation
1b	Masked	Input bit is ignored in event calculation

Customizable Event Creation 2-0

CEC2-0 - Customizable Event Creation 2-0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02780h

This register is used to define custom counter event 2, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Format: U11 The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. **Value / Name / Description / Programming Notes** 0b / Pass-through / Input bit is passed through to comparator as is / 1b / Negated / Input bit is negated before passing to comparator / If the input bit is negated using any bit in this field, then the corresponding Consderations bit in the CEC2-1 register must also be set.
	20:19	**Source Select** Format: U2 Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). **Value / Name / Description** 01b / Prev Event / Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block 11b / Reserved /
	18:3	**Compare Value** Format: U16 The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

CEC2-0 - Customizable Event Creation 2-0

	2:0	**Compare Function** Format: U3 This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

Customizable Event Creation 2-1

CEC2-1 - Customizable Event Creation 2-1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02784h

This register configures the input conditioning portion of CEC (custom event creation) block 2, bit definitions in this register refer to the CEC block diagram.

DWord	Bit	Description
0	31:16	**Considerations** This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.

Value	Name	Description
0b	Live	Input bit is not delayed by 1 clock before event calculation
1b	Delayed	Input bit is delayed by 1 clock before event calculation

DWord	Bit	Description
0	15:0	**Mask** This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.

Value	Name	Description
0b	Unmasked	Input bit is considered in event calculation
1b	Masked	Input bit is ignored in event calculation

Customizable Event Creation 3-0

CEC3-0 - Customizable Event Creation 3-0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02788h

This register is used to define custom counter event 3, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Format: U11 The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. **Value / Name / Description / Programming Notes** 0b / Pass-through / Input bit is passed through to comparator as is / 1b / Negated / Input bit is negated before passing to comparator / If the input bit is negated using any bit in this field, then the corresponding Consderations bit in the CEC3-1 register must also be set.
	20:19	**Source Select** Format: U2 Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). **Value / Name / Description** 01b / Prev Event / Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block 11b / Reserved /
	18:3	**Compare Value** Format: U16 The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

CEC3-0 - Customizable Event Creation 3-0

2:0 **Compare Function**

Format:	U3

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

Customizable Event Creation 3-1

CEC3-1 - Customizable Event Creation 3-1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0278Ch

This register configures the input conditioning portion of CEC (custom event creation) block 3, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:16	**Considerations** This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.

Value	Name	Description
0b	Live	Input bit is not delayed by 1 clock before event calculation
1b	Delayed	Input bit is delayed by 1 clock before event calculation

DWord	Bit	Description
	15:0	**Mask** This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.

Value	Name	Description
0b	Unmasked	Input bit is considered in event calculation
1b	Masked	Input bit is ignored in event calculation

Customizable Event Creation 4-0

CEC4-0 - Customizable Event Creation 4-0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02790h

This register is used to define custom counter event 4, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

<table>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td>0</td><td>31:21</td><td>Negate
Format: U11
The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th><th>Programming Notes</th></tr>
<tr><td>0b</td><td>Pass-through</td><td>Input bit is passed through to comparator as is</td><td></td></tr>
<tr><td>1b</td><td>Negated</td><td>Input bit is negated before passing to comparator</td><td>If the input bit is negated using any bit in this field, then the corresponding Consderations bit in the CEC4-1 register must also be set.</td></tr>
</table></td></tr>
<tr><td></td><td>20:19</td><td>Source Select
Format: U2
Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).
<table>
<tr><th>Value</th><th>Name</th><th>Description</th></tr>
<tr><td>01b</td><td>Prev Event</td><td>Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block</td></tr>
<tr><td>11b</td><td>Reserved</td><td></td></tr>
</table></td></tr>
<tr><td></td><td>18:3</td><td>Compare Value
Format: U16
The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.</td></tr>
</table>

CEC4-0 - Customizable Event Creation 4-0

	2:0	**Compare Function** Format: U3 This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

Customizable Event Creation 5-0

CEC5-0 - Customizable Event Creation 5-0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02798h

This register is used to define custom counter event 5, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

<table>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td>0</td><td>31:21</td><td>Negate
Format: U11
The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th><th>Programming Notes</th></tr>
<tr><td>0b</td><td>Pass-through</td><td>Input bit is passed through to comparator as is</td><td></td></tr>
<tr><td>1b</td><td>Negated</td><td>Input bit is negated before passing to comparator</td><td>If the input bit is negated using any bit in this field, then the corresponding Consderations bit in the CEC5-1 register must also be set.</td></tr>
</table></td></tr>
<tr><td></td><td>20:19</td><td>Source Select
Format: U2
Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).
<table>
<tr><th>Value</th><th>Name</th><th>Description</th></tr>
<tr><td>01b</td><td>Prev Event</td><td>Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block</td></tr>
<tr><td>11b</td><td>Reserved</td><td></td></tr>
</table></td></tr>
<tr><td></td><td>18:3</td><td>Compare Value
Format: U16
The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.</td></tr>
</table>

CEC5-0 - Customizable Event Creation 5-0

2:0 **Compare Function**

Format:	U3

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

Customizable Event Creation 5-1

CEC5-1 - Customizable Event Creation 5-1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0279Ch

This register configures the input conditioning portion of CEC (custom event creation) block 5, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:16	**Considerations** This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.
	15:0	**Mask** This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.

Bit 31:16 — Considerations

Value	Name	Description
0b	Live	Input bit is not delayed by 1 clock before event calculation
1b	Delayed	Input bit is delayed by 1 clock before event calculation

Bit 15:0 — Mask

Value	Name	Description
0b	Unmasked	Input bit is considered in event calculation
1b	Masked	Input bit is ignored in event calculation

Customizable Event Creation 6-0

CEC6-0 - Customizable Event Creation 6-0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	027A0h

This register is used to define custom counter event 6, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Format: U11 The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. **Value / Name / Description / Programming Notes** 0b / Pass-through / Input bit is passed through to comparator as is / 1b / Negated / Input bit is negated before passing to comparator / If the input bit is negated using any bit in this field, then the corresponding Consderations bit in the CEC6-1 register must also be set.
	20:19	**Source Select** Format: U2 Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). **Value / Name / Description** 01b / Prev Event / Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block 11b / Reserved /
	18:3	**Compare Value** Format: U16 The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

CEC6-0 - Customizable Event Creation 6-0

	2:0	**Compare Function** Format: U3 This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

Customizable Event Creation 6-1

CEC6-1 - Customizable Event Creation 6-1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	027A4h

This register configures the input conditioning portion of CEC (custom event creation) block 6, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:16	**Considerations** This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.
	15:0	**Mask** This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.

Value	Name	Description
0b	Live	Input bit is not delayed by 1 clock before event calculation
1b	Delayed	Input bit is delayed by 1 clock before event calculation

Value	Name	Description
0b	Unmasked	Input bit is considered in event calculation
1b	Masked	Input bit is ignored in event calculation

Customizable Event Creation 7-0

CEC7-0 - Customizable Event Creation 7-0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	027A8h

This register is used to define custom counter event 7, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Format: U11 The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. **Value / Name / Description / Programming Notes** 0b / Pass-through / Input bit is passed through to comparator as is / 1b / Negated / Input bit is negated before passing to comparator / If the input bit is negated using any bit in this field, then the corresponding Consderations bit in the CEC7-1 register must also be set.
	20:19	**Source Select** Format: U2 Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). **Value / Name / Description** 01b / Prev Event / Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block 11b / Reserved /
	18:3	**Compare Value** Format: U16 The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

CEC7-0 - Customizable Event Creation 7-0

2:0 **Compare Function**

Format:	U3

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

Customizable Event Creation 7-1

CEC7-1 - Customizable Event Creation 7-1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	027ACh

This register configures the input conditioning portion of CEC (custom event creation) block 3, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:16	**Considerations** This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.

Value	Name	Description
0b	Live	Input bit is not delayed by 1 clock before event calculation
1b	Delayed	Input bit is delayed by 1 clock before event calculation

DWord	Bit	Description
	15:0	**Mask** This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.

Value	Name	Description
0b	Unmasked	Input bit is considered in event calculation
1b	Masked	Input bit is ignored in event calculation

CVS TLB LRA 0

CVS_TLB_LRA_0 - CVS TLB LRA 0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x3F201F00 [SKL:GT1, SKL:GT1.5, SKL:GT2:C, SKL:GT2:D, SKL:GT2:F, SKL:GT2:G, SKL:GT3, SKL:GT4]
Size (in bits):	32
Address:	04A20h

DWord	Bit	Description
0	31	**Reserved** Default Value: 0b Access: RO
	30:24	**CVS LRA1 Max** Default Value: 0111111b Access: R/W Maximum value of programmable LRA1.
	23	**Reserved** Default Value: 0b Access: RO
	22:16	**CVS LRA1 Min** Default Value: 0100000b Access: R/W Minimum value of programmable LRA1.
	15	**Reserved** Default Value: 0b Access: RO
	14:8	**CVS LRA0 Max** Default Value: 0011111b Access: R/W Maximum value of programmable LRA0.
	7	**Reserved** Default Value: 0b Access: RO
	6:0	**CVS LRA0 Min** Default Value: 0000000b Access: R/W Minimum value of programmable LRA0.

CVS TLB LRA 1

CVS_TLB_LRA_1 - CVS TLB LRA 1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x7F717040
Size (in bits):	32
Address:	04A24h

DWord	Bit	Description
0	31	**Reserved** Default Value: 0b Access: RO
	30:24	**CVS LRA3 Max** Default Value: 1111111b Access: R/W If CVSLRA3Min == CVSLRA3Max , GATR LRA is disabled, GATR cycles are mapped to CVSLRA0 If CVSLRA3Min == CVSLRA3Max , GATR LRA is disabled, CVSLRA2Max will default to CVSLRA3Max to reuse GATR entries
	23	**Reserved** Default Value: 0b Access: RO
	22:16	**CVS LRA3 Min** Default Value: 1110001b Access: R/W For Future Use.
	15	**Reserved** Default Value: 0b Access: RO
	14:8	**CVS LRA2 Max** Default Value: 1110000b Access: R/W Maximum value of programmable LRA2.
	7	**Reserved** Default Value: 0b Access: RO

CVS_TLB_LRA_1 - CVS TLB LRA 1

	6:0	**CVS LRA2 Min** Default Value: 1000000b Access: R/W Minimum value of programmable LRA2.

CVS TLB LRA 2

CVS_TLB_LRA_2 - CVS TLB LRA 2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000031A
Size (in bits):	32
Address:	04A28h

DWord	Bit	Description
0	31:10	**Reserved** Default Value: 00000000000000000000b Access: RO
	9:8	**GATR LRA** Default Value: 11b Access: R/W Which LRA should RS use
	7:6	**RS LRA** Default Value: 00b Access: R/W Which LRA should RS use
	5:4	**CS LRA** Default Value: 01b Access: R/W Which LRA should CS use.
	3:2	**SOL LRA** Default Value: 10b Access: R/W Which LRA should SOL use.
	1:0	**VF LRA** Default Value: 10b Access: R/W Which LRA should VF use.

DATAM

DATAM	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	60030h-60033h
Name:	Transcoder A Data M Value 1
ShortName:	TRANS_DATAM1_A
Valid Projects:	
Power:	PG2
Reset:	soft
Address:	61030h-61033h
Name:	Transcoder B Data M Value 1
ShortName:	TRANS_DATAM1_B
Valid Projects:	
Power:	PG2
Reset:	soft
Address:	62030h-62033h
Name:	Transcoder C Data M Value 1
ShortName:	TRANS_DATAM1_C
Valid Projects:	
Power:	PG2
Reset:	soft
Address:	6F030h-6F033h
Name:	Transcoder EDP Data M Value 1
ShortName:	TRANS_DATAM1_EDP
Valid Projects:	
Power:	PG1
Reset:	soft

Description

There is one instance of this register for each transcoder A/B/C/EDP. This register is double buffered to update on the next MSA after LINKN is written.

DWord	Bit	Description
0	31	**Reserved** Format: MBZ

DATAM		
	30:25	**TU or VCpayload Size** In DisplayPort SST mode this field is the size of the transfer unit, minus one. Typically it is programmed with a value of 63 for TU size of 64. In DisplayPort MST mode this field is the Virtual Channel payload size, minus one. **Restriction** In DisplayPort MST mode the Virtual Channel payload size must not be programmed greater than 62 (resulting payload size of 63). In DisplayPort MST mode the Virtual Channel payload size must not be changed while the Virtual Channel is enabled, even after a transcoder has been disabled.
	24	**Reserved** Format: MBZ
	23:0	**Data M value** This field is the data M value for internal use.

DATAN

DATAN	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	60034h-60037h
Name:	Transcoder A Data N Value 1
ShortName:	TRANS_DATAN1_A
Valid Projects:	
Power:	PG2
Reset:	soft
Address:	61034h-61037h
Name:	Transcoder B Data N Value 1
ShortName:	TRANS_DATAN1_B
Valid Projects:	
Power:	PG2
Reset:	soft
Address:	62034h-62037h
Name:	Transcoder C Data N Value 1
ShortName:	TRANS_DATAN1_C
Valid Projects:	
Power:	PG2
Reset:	soft
Address:	6F034h-6F037h
Name:	Transcoder EDP Data N Value 1
ShortName:	TRANS_DATAN1_EDP
Valid Projects:	
Power:	PG1
Reset:	soft

Description
There is one instance of this register for each transcoder A/B/C/EDP. This register is double buffered to update on the next MSA after LINKN is written.

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ

DATAN		
	23:0	**Data N value** This field is the data N value for internal use.

DBUF_CTL

DBUF_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	45008h-4500Bh
Name:	DBUF Control
ShortName:	DBUF_CTL
Power:	PG0
Reset:	soft

DWord	Bit	Description
0	31	**DBUF Power Request** Access: R/W This field requests DBUF power to enable or disable. Value / Name: 0b – Disable 1b – Enable **Programming Notes** DBUF power must be enabled prior to using internal display engine features. Enable power by programming the power request to 1, then wait for the power state to indicate it is enabled.
	30	**DBUF Power State** Access: RO This field indicates the status of DBUF power. Value / Name: 0b – Disabled 1b – Enabled
	29:28	**Reserved** Format: MBZ
	27	**Reserved**
	26	**Reserved** Format: MBZ
	25:24	**Reserved**
	23:5	**Reserved** Format: MBZ

DBUF_CTL		
	4:0	**Reserved**

DBUF_ECC_STAT

DBUF_ECC_STAT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/WC
Size (in bits):	32
Address:	45010h-45013h
Name:	DBUF ECC Status
ShortName:	DBUF_ECC_STAT
Power:	PG0
Reset:	soft

Each of these fields is a sticky bit that gives the ECC error status for a particular memory bank. A '1' in a bit indicates that ECC detected an error. A write of '1' to a bit will clear the bit. Single errors are corrected by ECC. Double errors are not correctable.

DWord	Bit	Description
0	31	**Double Error Bank 15**
	30	**Double Error Bank 14**
	29	**Double Error Bank 13**
	28	**Double Error Bank 12**
	27	**Double Error Bank 11**
	26	**Double Error Bank 10**
	25	**Double Error Bank 9**
	24	**Double Error Bank 8**
	23	**Double Error Bank 7**
	22	**Double Error Bank 6**
	21	**Double Error Bank 5**
	20	**Double Error Bank 4**
	19	**Double Error Bank 3**
	18	**Double Error Bank 2**
	17	**Double Error Bank 1**
	16	**Double Error Bank 0**
	15	**Single Error Bank 15**
	14	**Single Error Bank 14**
	13	**Single Error Bank 13**
	12	**Single Error Bank 12**
	11	**Single Error Bank 11**

DBUF_ECC_STAT		
	10	**Single Error Bank 10**
	9	**Single Error Bank 9**
	8	**Single Error Bank 8**
	7	**Single Error Bank 7**
	6	**Single Error Bank 6**
	5	**Single Error Bank 5**
	4	**Single Error Bank 4**
	3	**Single Error Bank 3**
	2	**Single Error Bank 2**
	1	**Single Error Bank 1**
	0	**Single Error Bank 0**

DC_STATE_EN

DC_STATE_EN

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	45504h-45507h
Name:	Display C State Enable
ShortName:	DC_STATE_EN
Valid Projects:	
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:10	**Reserved**
	9	**In CSR Flow** Value: 0b — Name: Not In CSR Value: 1b — Name: In CSR Restriction: This field is used for hardware communication. Software must not change this field.
	8	**Block Outbound Traffic** Access is read/write, but hardware can also clear the value based on the PM Request. Value: 0b — Name: Do Not Block Value: 1b — Name: Block Restriction: This field is used for hardware communication. Software must not change this field.
	7:5	**Reserved**
	4	**Mask Poke** This field masks the poke signal that would otherwise be generated by a write to the DC_STATE_SEL register. Value: 0b — Name: Unmask Value: 1b — Name: Mask

DC_STATE_EN

		Restriction This field is used for hardware communication. Software must not change this field.
	3	**Reserved**
	2	**Reserved**
	1:0	**Dynamic DC State Enable** This field enables hardware to dynamically enter and exit Display C states. **Value** / **Name** 00b – Disable 01b – Enable up to DC5 10b – Enable up to DC6 **Restriction** The Display CSR code must be loaded before this field is enabled.

DDI_AUX_CTL

DDI_AUX_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000023F
Access:	R/W
Size (in bits):	32
Address:	64010h-64013h
Name:	DDI A AUX Channel Control
ShortName:	DDI_AUX_CTL_A
Valid Projects:	
Power:	PG1
Reset:	soft
Address:	64110h-64113h
Name:	DDI B AUX Channel Control
ShortName:	DDI_AUX_CTL_B
Valid Projects:	
Power:	PG2
Reset:	soft
Address:	64210h-64213h
Name:	DDI C AUX Channel Control
ShortName:	DDI_AUX_CTL_C
Valid Projects:	
Power:	PG2
Reset:	soft
Address:	64310h-64313h
Name:	DDI D AUX Channel Control
ShortName:	DDI_AUX_CTL_D
Valid Projects:	
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31	**Send Busy** Access: R/W Set Writing this bit with 1b initiates the transaction, when read this bit will be a 1b until the transmission completes. The transaction is completed when the response is received or when a timeout occurs. This is a sticky bit. Write a 1b to this bit to set it and initiate the transaction. Hardware will clear it when the transaction completes.

DDI_AUX_CTL

	Restriction Do not change any fields while Send Busy is asserted. Do not write a 1b again until transaction completes. Restriction : Mutex must be acquired through DDI_AUX_MUTEX before initiating an AUX channel transaction.
30	**Done** Access: R/WC A sticky bit that indicates the transaction has completed. Write a 1 to this bit to clear the event 0b: Not done 1b: Done
29	**Interrupt on Done** Access: R/W Enable an interrupt when the transaction completes or times out. 0b: Enable 1b: Disable
28	**Time out error** Access: R/WC A sticky bit that indicates the transaction has timed out. Write a 1 to this bit to clear the event. 0b: Not error 1b: Error
27:26	**Time out timer value** Access: R/W Used to determine how long to wait for receiver response before timing out. 00b: 400us: Do not use this setting. 01b: 600us 10b: 800us 11b: 1600us

DDI_AUX_CTL

25	**Receive error** Access: R/WC A sticky bit that indicates that the data received was corrupted, not in multiples of a full byte, or more than 20 bytes. Write a 1 to this bit to clear the event. Value: 0b — Name: Not Error Value: 1b — Name: Error
24:20	**Message Size** Access: Write/Read Status The value written to this field indicates the total number bytes to transmit (including the header). The value read from this field indicates the number of bytes received, including the header, in the last transaction transaction. Sync/Stop are not part of the message or the message size. Reads of this field will give the response message size. The read value will not be valid while Send/Busy bit 31 is asserted. Restriction: Message sizes of 0 or >20 are not allowed. Reads and writes are valid only when the done bit is set and timeout or receive error has not occurred.
19:16	**Reserved**
15	**Reserved**
14	**Reserved**
13	**Reserved**
12	**Reserved**
11	**Reserved**
10	**Reserved**
9:5	**Fast Wake Sync Pulse Count** Default Value: 1 0001b 18 pulses Access: R/W This field determines the total number of SYNC pulses sent during the SYNC phase of a fast wake transaction. The value programmed is the number of pulses minus 1. When this is field is set to "n" the aux controller will send "n+1" SYNC pulses before transmitting the STOP pattern.
4:0	**Sync Pulse Count** Default Value: 1 1111b 32 pulses Access: R/W This field determines the total number of SYNC pulses sent during the SYNC phase of a standard transaction. The value programmed is the number of pulses minus 1. When this is field is set to "n" the aux controller will send "n+1" SYNC pulses before transmitting the STOP pattern. Restriction: This field must be programmed to at least 25 decimal to send the minimum amount of pulses required for a standard transaction.

DDI_AUX_DATA

DDI_AUX_DATA	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Write/Read Status
Size (in bits):	32
Address:	64014h-64027h
Name:	DDI A AUX Channel Data
ShortName:	DDI_AUX_DATA_A_*
Valid Projects:	
Power:	PG1
Reset:	soft
Address:	64114h-64127h
Name:	DDI B AUX Channel Data
ShortName:	DDI_AUX_DATA_B_*
Valid Projects:	
Power:	PG2
Reset:	soft
Address:	64214h-64227h
Name:	DDI C AUX Channel Data
ShortName:	DDI_AUX_DATA_C_*
Valid Projects:	
Power:	PG2
Reset:	soft
Address:	64314h-64327h
Name:	DDI D AUX Channel Data
ShortName:	DDI_AUX_DATA_D_*
Valid Projects:	
Power:	PG2
Reset:	soft

There are 5 DWords of this register format per instance.

DWord	Bit	Description
0	31:0	**AUX CH DATA** This field contains a DWord of the AUX message. Writes to this register give the data to transmit during the transaction. The MSbyte is transmitted first. Reads to this register will give the response data after transaction complete. The read value will not be valid while the Aux Channel Control Register Send/Busy bit is asserted

DDI_AUX_MUTEX

DDI_AUX_MUTEX	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6402Ch-6402Fh
Name:	DDI A AUX Channel MUTEX
ShortName:	DDI_AUX_MUTEX_A
Valid Projects:	
Power:	PG1
Reset:	soft
Address:	6412Ch-6412Fh
Name:	DDI B AUX Channel MUTEX
ShortName:	DDI_AUX_MUTEX_B
Valid Projects:	
Power:	PG2
Reset:	soft
Address:	6422Ch-6422Fh
Name:	DDI C AUX Channel MUTEX
ShortName:	DDI_AUX_MUTEX_C
Valid Projects:	
Power:	PG2
Reset:	soft
Address:	6432Ch-6432Fh
Name:	DDI D AUX Channel MUTEX
ShortName:	DDI_AUX_MUTEX_D
Valid Projects:	
Power:	PG2
Reset:	soft

Programming Notes
Follow programming sequence from DDI Aux Channel page.

DWord	Bit	Description

DDI_AUX_MUTEX

0	31	**Mutex Enable** Access: R/W This field enables the Mutex. When enabled, mutex allows only one source to use the Aux controller at a time. **Value** / **Name** 1b: Enable 0b: Disable
	30	**Mutex Status** Access: Write/Read Status This field indicates the Mutex status. Software must acquire mutex before initiating an Aux transaction. Sticky bit set to 1 after a read to this register when Mutex is enabled. Clear by writing with a 1. **Value** / **Name** 0b: Mutex not yet acquired 1b: Mutex already acquired **Restriction** **After completing an Aux channel transaction with mutex enabled, write this bit with a 1 to clear it so hardware can use Aux for other purposes.**
	29:0	**Reserved**

DDI_BUF_CTL

DDI_BUF_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	64000h-64003h
Name:	DDI A Buffer Control
ShortName:	DDI_BUF_CTL_A
Valid Projects:	
Power:	PG1
Reset:	soft
Address:	64100h-64103h
Name:	DDI B Buffer Control
ShortName:	DDI_BUF_CTL_B
Valid Projects:	
Power:	PG1
Reset:	soft
Address:	64200h-64203h
Name:	DDI C Buffer Control
ShortName:	DDI_BUF_CTL_C
Valid Projects:	
Power:	PG1
Reset:	soft
Address:	64300h-64303h
Name:	DDI D Buffer Control
ShortName:	DDI_BUF_CTL_D
Valid Projects:	
Power:	PG1
Reset:	soft
Address:	64400h-64403h
Name:	DDI E Buffer Control
ShortName:	DDI_BUF_CTL_E
Valid Projects:	
Power:	PG1
Reset:	soft

DDI_BUF_CTL

There is one DDI Buffer Control per each DDI A/B/C/D/E/F.

DWord	Bit	Description
0	31	**DDI Buffer Enable** This bit enables the DDI buffer. Value: 0b = Disable; 1b = Enable
	30	**Reserved** Format: MBZ
	29:28	**Reserved**
	27:24	**DP Vswing Emp Sel** Description: These bits are used to select the voltage swing and emphasis for DisplayPort. This field is ignored for HDMI and DVI. The values programmed in DDI_BUF_TRANS determine the voltage swing and emphasis for each selection. Value: 0000b-1000b = Select 0 - Select 8 (Select from buffer translations 0 through 8. Valid with all DDIs.); 1001b = Select 9 (Select buffer translation 9. Valid only with DDIA and DDIE.)
	23:17	**Reserved** Format: MBZ
	16	**Port Reversal** This field enables lane reversal within the port. Lane reversal swaps the data on the lanes as they are output from the port. Value: 0b = Not reversed; 1b = Reversed **Programming Notes**: DDI B, C, D, and F reversal always swaps the four lanes, so lane 0 is swapped with lane 3, and lane 1 is swapped with lane 2. If DDIA Lane Capability Control selects DDIA x2, then DDI A reversal swaps the two lanes, so lane 0 is swapped with lane 1. If DDIA Lane Capability Control selects DDIA x4, then DDI A reversal swaps the four lanes, so lane 0 is swapped with lane 3, and lane 1 is swapped with lane 2. **Restriction**: This field must not be changed while the DDI is enabled. DDI E does not support reversal.

DDI_BUF_CTL

15:8 Reserved

Format:	MBZ

7 DDI Idle Status

Access:	RO

This bit indicates when the DDI buffer is idle.

Value	Name
0b	Buffer Not Idle
1b	Buffer Idle

6:5 Reserved

Format:	MBZ

4 DDIA Lane Capability Control

This bit selects how lanes are shared between DDI A and DDI E. This field is only used in the DDI A instance of this register. See the DDI A and DDI E lane mapping table in the Introduction section.

Value	Name	Description
0b	DDIA x2	DDI A supports 2 lanes and DDI E supports 2 lanes
1b	DDIA x4	DDI A supports 4 lanes and DDI E is not used

Restriction
This field must be programmed at system boot based on board configuration and may not be changed afterwards.

3:1 DP Port Width Selection

Description
This bit selects the number of lanes to be enabled on the DDI link for DisplayPort.
This field is ignored for HDMI and DVI which always use all 4 lanes.

Value	Name	Description
000b	x1	x1 Mode
001b	x2	x2 Mode
011b	x4	x4 Mode Not allowed with DDI E, some restrictions with DDI A
Others	Reserved	Reserved

Programming Notes
DDI E only supports x1 and x2 when DDI_BUF_CTL_A DDIA Lane Capability Control is set to DDIA x2, otherwise DDI E is not supported. DDI A (EDP) supports x1, x2, and x4 when DDI_BUF_CTL_A DDIA Lane Capability Control is set to DDIA x4, otherwise DDI A only supports x1 and x2.

DDI_BUF_CTL

		Restriction When in DisplayPort mode the value selected here must match the value selected in the DDI Buffer Control register for the DDI attached to this pipe. This field must not be changed while the DDI is enabled.
	0	**Init Display Detected** Access: RO **Description** Strap indicating whether a display was detected on this port during initialization. It signifies the level of the port detect pin at boot. This bit is only informative. It does not prevent this port from being enabled in hardware. This field only indicates the DDIA detection. Detection for other ports is read from SFUSE_STRAP.

Value	Name	Description
0b	Not Detected	Digital display not detected during initialization
1b	Detected	Digital display detected during initialization

DDI_BUF_TRANS

DDI_BUF_TRANS	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000018, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	64E00h-64E4Fh
Name:	DDI A Buffer Translation
ShortName:	DDI_BUF_TRANS_A_*
Power:	PG1
Reset:	global
Address:	64E60h-64EAFh
Name:	DDI B Buffer Translation
ShortName:	DDI_BUF_TRANS_B_*
Power:	PG1
Reset:	global
Address:	64EC0h-64F0Fh
Name:	DDI C Buffer Translation
ShortName:	DDI_BUF_TRANS_C_*
Power:	PG1
Reset:	global
Address:	64F20h-64F6Fh
Name:	DDI D Buffer Translation
ShortName:	DDI_BUF_TRANS_D_*
Power:	PG1
Reset:	global
Address:	64F80h-64FCFh
Name:	DDI E Buffer Translation
ShortName:	DDI_BUF_TRANS_E_*
Power:	PG1
Reset:	global

Description
These registers define the DDI buffer settings required for different voltage swing and emphasis selections. In HDMI or DVI mode the HDMI/DVI translation registers are automatically selected.
In DisplayPort mode the DDI Buffer Control register programming will select which of these registers is used to drive the buffer. For each DDI A/B/C/D/E there are 10 instances of this 2 DWord register format. For DDI B/C/D,

DDI_BUF_TRANS

the first 9 instances (18 Dwords) are entries 0-8 which are used for DisplayPort, and the last instance (2 Dwords) is entry 9 which is used for HDMI and DVI. For DDI A and DDI E, the 10 instances (20 DWords) are entries 0-9 which are used for DisplayPort.

Programming Notes

The recommended values are listed below this table.

Restriction

These registers must be programmed with valid values prior to enabling DDI_BUF_CTL.

DWord	Bit	Description
0	31	**Balance Leg Enable** This field controls the Balance Leg enable for the DDI buffer. Value: 0b — Name: Disable Value: 1b — Name: Enable
	30:18	**Reserved** Format: MBZ
	17:0	**DeEmp Level** Default Value: 00018h This field controls the De-emphasis level for the DDI buffer.
1	31:21	**Reserved** Format: MBZ
	20:16	**VRef Sel** This field controls the voltage reference select for the DDI buffer. Value: 00000b — Name: **[Default]**
	15:11	**Reserved** Format: MBZ
	10:0	**Vswing** Default Value: 00000000000b This field controls the voltage swing for the DDI buffer.

DE_PIPE_INTERRUPT

DE_PIPE_INTERRUPT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	44400h-4440Fh
Name:	Display Engine Pipe A Interrupts
ShortName:	DE_PIPE_INTERRUPT_A
Valid Projects:	
Power:	PG1
Reset:	soft
Address:	44410h-4441Fh
Name:	Display Engine Pipe B Interrupts
ShortName:	DE_PIPE_INTERRUPT_B
Valid Projects:	
Power:	PG2
Reset:	soft
Address:	44420h-4442Fh
Name:	Display Engine Pipe C Interrupts
ShortName:	DE_PIPE_INTERRUPT_C
Valid Projects:	
Power:	PG2
Reset:	soft

Description

This table indicates which events are mapped to each bit of the Display Engine Pipe Interrupt registers. The IER enabled Display Engine Pipe Interrupt IIR (sticky) bits are ORed together to generate the DE_Pipe Interrupts Pending bit in the Master Interrupt Control register. There is one full set of Display Engine Pipe interrupts per display pipes A/B/C. The STEREO3D_EVENT_MASK selects between left eye and right eye reporting of vertical blank, vertical sync, and scanline events in stereo 3D modes.

0x44400 = ISR A, 0x44410 = ISR B, 0x44420 = ISR C
0x44404 = IMR A, 0x44414 = IMR B, 0x44424 = IMR C
0x44408 = IIR A, 0x44418 = IIR B, 0x44428 = IIR C
0x4440C = IER A, 0x4441C = IER B, 0x4442C = IER C

DWord	Bit	Description
0	31	**Underrun** The ISR is an active high pulse when there is an underrun on the transcoder attached to this pipe.

DE_PIPE_INTERRUPT		
	30	**Unused_Int_30** These interrupts are currently unused.
	29	**Reserved**
	28	**Reserved**
	27:20	**Unused_Int_27_20** These interrupts are currently unused.
	19	**Reserved**
	18	**Reserved**
	17	**Reserved**
	16	**Reserved**
	15:13	**Unused_Int_15_13** These interrupts are currently unused.
	12	**DPST_Histogram_event** The ISR is an active high pulse on the DPST Histogram event on this pipe.
	11	**Cursor_GTT_Fault_Status** The ISR is an active high pulse when a GTT fault is detected for the cursor on this pipe.
	10	**Plane4_GTT_Fault_Status** **Description** The ISR is an active high pulse when a GTT fault is detected for plane 4 on this pipe. Not all pipes a have plane 4.
	9	**Plane3_GTT_Fault_Status** **Description** The ISR is an active high pulse when a GTT fault is detected for plane 3 on this pipe. Not all pipes a have plane 3.
	8	**Plane2_GTT_Fault_Status** The ISR is an active high pulse when a GTT fault is detected for plane 2 on this pipe.
	7	**Plane1_GTT_Fault_Status** The ISR is an active high pulse when a GTT fault is detected for plane 1 on this pipe.
	6	**Plane4_Flip_Done** **Description** The ISR is an active high pulse when the flip is done for plane 4 on this pipe. Not all pipes have a plane 4.
	5	**Plane3_Flip_Done** **Description** The ISR is an active high pulse when the flip is done for plane 3 on this pipe. Not all pipes have a plane 3.
	4	**Plane2_Flip_Done** The ISR is an active high pulse when the flip is done for plane 2 on this pipe.

DE_PIPE_INTERRUPT		
	3	**Plane1_Flip_Done** The ISR is an active high pulse when the flip is done for plane 1 on this pipe.
	2	**Scan_Line_Event** The ISR is an active high pulse on the scan line event of the transcoder attached to this pipe.
	1	**Vsync** The ISR is an active high level for the duration of the vertical sync of the transcoder attached to this pipe.
	0	**Vblank** The ISR is an active high level for the duration of the vertical blank of the transcoder attached to this pipe.

DE_RR_DEST

DE_RR_DEST

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	44058h-4405Bh
Name:	Render Response Destination
ShortName:	DE_RR_DEST
Valid Projects:	
Power:	PG0
Reset:	soft

This register selects the destination of certain render responses that may go to CS, BCS, or both. In order for a response to be sent to a particular destination, the event most occur, the event must be unmasked, and that destination must be selected.

DWord	Bit	Description
0	31:6	**Reserved** Format: MBZ
	5:4	**Pipe C Vertical Blank Destination** This field selects the destination for the render response sent on pipe C start of vertical blank. 00b: CS 01b: BCS 10b,11b: Both CS and BCS
	3:2	**Pipe B Vertical Blank Destination** This field selects the destination for the render response sent on pipe B start of vertical blank. 00b: CS 01b: BCS 10b,11b: Both CS and BCS

DE_RR_DEST

	1:0	**Pipe A Vertical Blank Destination** This field selects the destination for the render response sent on pipe A start of vertical blank.

Value	Name
00b	CS
01b	BCS
10b,11b	Both CS and BCS

DE_RRMR

DE_RRMR	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x2077EFEF
Access:	R/W
Size (in bits):	32
Address:	44050h-44053h
Name:	Render Response Mask
ShortName:	DE_RRMR
Power:	PG0
Reset:	soft

This register contains a bit mask which selects which events cause and are reported in the render response message. See the render response message definition table to find the source event for each bit. The render response message is sent from the display engine to the render command streamer (CS) or blitter command streamer (BCS). The message is used to inform CS and BCS of certain display events. This register is used to control which render response message bits are masked or unmasked. Unmasked bits will cause a render response message to be sent and will be reported in that message. Masked bits will not be reported and will not cause a render response message to be sent. Vertical blank events occur periodically while the associated display pipe timing generator is running and will be reported in a render response to CS or BCS (depending on DE_RR_DEST destination selection) if un-masked here. Scanline events occur after they have been initiated through MMIO writes or LRI to the Display Load Scan Lines register. A flip event will be reported in a render response to CS if un-masked here and the Display Load Scanline source is CS. A flip event will be reported in a render response to BCS if un-masked here and the Display Load Scanline source is BCS. Flip done events occur after they have been initiated through MI_DISPLAY_FLIP or MMIO write to plane surface address registers. A flip event will be reported in a render response to CS if un-masked here and the flip source is CS. A flip event will be reported in a render response to BCS if un-masked here and the flip source is BCS.

Programming Notes

Programming this register can be done through MMIO or a command streamer LOAD_REGISTER_IMMEDIATE (LRI) command. When using LRI care must be taken to follow all the programming rules for LRI targetting the display engine. Unmasked events will wake GT as they occur, so for improved power savings it is recommended to only unmask events that are required.

Restriction

Events must be unmasked prior to waiting for them with a MI_WAIT_FOR_EVENT ring command, or in the case of flips or scanlines, prior to starting the flip or loading the scanline.

DWord	Bit	Description
0	31:30	**Reserved** Format: MBZ

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	29	**Mask 29** Value: 0b — Not Masked Value: 1b — Masked **[Default]**
	28:23	**Reserved**
	22	**Mask 22** Value: 0b — Not Masked Value: 1b — Masked **[Default]**
	21	**Mask 21** Value: 0b — Not Masked Value: 1b — Masked **[Default]**
	20	**Mask 20** Value: 0b — Not Masked Value: 1b — Masked **[Default]**
	19	**Reserved**
	18	**Mask 18** Value: 0b — Not Masked Value: 1b — Masked **[Default]**
	17	**Mask 17** Value: 0b — Not Masked Value: 1b — Masked **[Default]**
	16	**Mask 16** Value: 0b — Not Masked Value: 1b — Masked **[Default]**
	15	**Mask 15** Value: 0b — Not Masked Value: 1b — Masked **[Default]**

DE_RRMR

	14	**Mask 14** Value: 0b – Not Masked Value: 1b – Masked **[Default]**
	13	**Mask 13** Value: 0b – Not Masked Value: 1b – Masked **[Default]**
	12	**Reserved**
	11	**Mask 11** Value: 0b – Not Masked Value: 1b – Masked **[Default]**
	10	**Mask 10** Value: 0b – Not Masked Value: 1b – Masked **[Default]**
	9	**Mask 9** Value: 0b – Not Masked Value: 1b – Masked **[Default]**
	8	**Mask 8** Value: 0b – Not Masked Value: 1b – Masked **[Default]**
	7	**Mask 7** Value: 0b – Not Masked Value: 1b – Masked **[Default]**
	6	**Mask 6** Value: 0b – Not Masked Value: 1b – Masked **[Default]**

DE_RRMR

	5	**Mask 5** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	4	**Reserved**
	3	**Mask 3** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	2	**Mask 2** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	1	**Mask 1** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	0	**Mask 0** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**

Decouple Register 0 DW0

DECOUPREG0DW0 - Decouple Register 0 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00F00h-00F03h	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg0DW0Data** Access: R/W Decouple Register 0 DW0 Data.

Decouple Register 0 DW1

DECOUPREG0DW1 - Decouple Register 0 DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00F04h-00F07h	
DWord	**Bit**	**Description**
0	31	**DecoupReg0DW1GO** Access: R/W Decouple Register 0 DW1 Go_Status Bit, Software writes this bit to 1 when it is ready for the command to be processed, Hardware clears this bit to 0 when the command is complete, Software must not read data or write the next command when this bit is 1.
	29:28	**DecoupReg0DW1PD** Access: R/W Decouple Register 0 DW1, 00 = GTI/Bliteer, 01 = Render, 10= Media , 11= All Domains, Identifies the target power domain that must be awake before proceeding with the cycle.
	27:24	**DecoupReg0DW1OP** Access: R/W Decouple Register 0 DW1, 0000 = Write, 0001 = Read, All others undefined (GT will ignore command and set go/status=0) Decouple Register.
	23:20	**DecoupReg0DW1BE** Access: R/W Decouple Register 0 DW1, Decoupled byte enables. Provided for legacy/workaround purposes only; GT only supports full dword accesses.
	17:0	**DecoupReg0DW1Addr** Access: R/W Decouple Register 0 DW1, Decoupled Address.

Decouple Register 1 DW0

DECOUPREG1DW0 - Decouple Register 1 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00F08h-00F0Bh	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg1DW0Data** Access: R/W Decouple Register 1 DW0 Data.

Decouple Register 1 DW1

DECOUPREG1DW1 - Decouple Register 1 DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00F0Ch-00F0Fh	
DWord	**Bit**	**Description**
0	31	**DecoupReg1DW1GO** Access: R/W Decouple Register 1 DW1 Go_Status Bit, Software writes this bit to 1 when it is ready for the command to be processed, Hardware clears this bit to 0 when the command is complete, Software must not read data or write the next command when this bit is 1.
	29:28	**DecoupReg1DW1PD** Access: R/W Decouple Register 1 DW1, 00 = GTI/Bliteer, 01 = Render, 10= Media , 11= All Domains, Identifies the target power domain that must be awake before proceeding with the cycle.
	27:24	**DecoupReg1DW1OP** Access: R/W Decouple Register 1 DW1, 0000 = Write, 0001 = Read, All others undefined (GT will ignore command and set go/status=0) Decouple Register.
	23:20	**DecoupReg1DW1BE** Access: R/W Decouple Register 1 DW1, Decoupled byte enables. Provided for legacy/workaround purposes only; GT only supports full dword accesses.
	17:0	**DecoupReg1DW1Addr** Access: R/W Decouple Register 1 DW1, Decoupled Address.

Decouple Register 2 DW0

DECOUPREG2DW0 - Decouple Register 2 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00F10h-00F13h	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg2DW0Data** Access: R/W Decouple Register 2 DW0 Data.

Decouple Register 2 DW1

DECOUPREG2DW1 - Decouple Register 2 DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00F14h-00F17h	
DWord	**Bit**	**Description**
0	31	**DecoupReg2DW1GO** Access: R/W Decouple Register 2 DW1 Go_Status Bit, Software writes this bit to 1 when it is ready for the command to be processed, Hardware clears this bit to 0 when the command is complete, Software must not read data or write the next command when this bit is 1.
	29:28	**DecoupReg2DW1PD** Access: R/W Decouple Register 2 DW1, 00 = GTI/Bliteer, 01 = Render, 10= Media , 11= All Domains, Identifies the target power domain that must be awake before proceeding with the cycle.
	27:24	**DecoupReg2DW1OP** Access: R/W Decouple Register 2 DW1, 0000 = Write, 0001 = Read, All others undefined (GT will ignore command and set go/status=0) Decouple Register.
	23:20	**DecoupReg2DW1BE** Access: R/W Decouple Register 2 DW1, Decoupled byte enables. Provided for legacy/workaround purposes only; GT only supports full dword accesses.
	17:0	**DecoupReg2DW1Addr** Access: R/W Decouple Register 2 DW1, Decoupled Address.

Decouple Register 3 DW0

DECOUPREG3DW0 - Decouple Register 3 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00F18h-00F1Bh	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg3DW0Data** Access: R/W Decouple Register 3 DW0 Data.

Decouple Register 3 DW1

DECOUPREG3DW1 - Decouple Register 3 DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00F1Ch-00F1Fh	
DWord	**Bit**	**Description**
0	31	**DecoupReg3DW1GO** Access: R/W Decouple Register 3 DW1 Go_Status Bit, Software writes this bit to 1 when it is ready for the command to be processed, Hardware clears this bit to 0 when the command is complete, Software must not read data or write the next command when this bit is 1.
	29:28	**DecoupReg3DW1PD** Access: R/W Decouple Register 3 DW1, 00 = GTI/Bliteer, 01 = Render, 10= Media , 11= All Domains, Identifies the target power domain that must be awake before proceeding with the cycle.
	27:24	**DecoupReg3DW1OP** Access: R/W Decouple Register 3 DW1, 0000 = Write, 0001 = Read, All others undefined (GT will ignore command and set go/status=0) Decouple Register.
	23:20	**DecoupReg3DW1BE** Access: R/W Decouple Register 3 DW1, Decoupled byte enables. Provided for legacy/workaround purposes only; GT only supports full dword accesses.
	17:0	**DecoupReg3DW1Addr** Access: R/W Decouple Register 3 DW1, Decoupled Address.

Decouple Register 4 DW0

DECOUPREG4DW0 - Decouple Register 4 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00F20h-00F23h	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg4DW0Data** Access: R/W Decouple Register 4 DW0 Data.

Decouple Register 4 DW1

DECOUPREG4DW1 - Decouple Register 4 DW1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	00F24h-00F27h

DWord	Bit	Description
0	31	**DecoupReg4DW1GO** Access: R/W Decouple Register 4 DW1 Go_Status Bit, Software writes this bit to 1 when it is ready for the command to be processed, Hardware clears this bit to 0 when the command is complete, Software must not read data or write the next command when this bit is 1.
	29:28	**DecoupReg4DW1PD** Access: R/W Decouple Register 4 DW1, 00 = GTI/Bliteer, 01 = Render, 10= Media , 11= All Domains, Identifies the target power domain that must be awake before proceeding with the cycle.
	27:24	**DecoupReg4DW1OP** Access: R/W Decouple Register 4 DW1, 0000 = Write, 0001 = Read, All others undefined (GT will ignore command and set go/status=0) Decouple Register.
	23:20	**DecoupReg4DW1BE** Access: R/W Decouple Register 4 DW1, Decoupled byte enables. Provided for legacy/workaround purposes only; GT only supports full dword accesses.
	17:0	**DecoupReg4DW1Addr** Access: R/W Decouple Register 4 DW1, Decoupled Address.

Decouple Register 5 DW0

DECOUPREG5DW0 - Decouple Register 5 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00F28h-00F2Bh	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg5DW0Data** Access: R/W Decouple Register 5 DW0 Data.

Decouple Register 5 DW1

DECOUPREG5DW1 - Decouple Register 5 DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00F2Ch-00F2Fh	
DWord	**Bit**	**Description**
0	31	**DecoupReg5DW1GO** Access: R/W Decouple Register 5 DW1 Go_Status Bit, Software writes this bit to 1 when it is ready for the command to be processed, Hardware clears this bit to 0 when the command is complete, Software must not read data or write the next command when this bit is 1.
	29:28	**DecoupReg5DW1PD** Access: R/W Decouple Register 5 DW1, 00 = GTI/Bliteer, 01 = Render, 10= Media , 11= All Domains, Identifies the target power domain that must be awake before proceeding with the cycle.
	27:24	**DecoupReg5DW1OP** Access: R/W Decouple Register 5 DW1, 0000 = Write, 0001 = Read, All others undefined (GT will ignore command and set go/status=0) Decouple Register.
	23:20	**DecoupReg5DW1BE** Access: R/W Decouple Register 5 DW1, Decoupled byte enables. Provided for legacy/workaround purposes only; GT only supports full dword accesses.
	17:0	**DecoupReg5DW1Addr** Access: R/W Decouple Register 5 DW1, Decoupled Address.

Decouple Register 6 DW0

DECOUPREG6DW0 - Decouple Register 6 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00F30h-00F33h	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg6DW0Data** Access: R/W Decouple Register 6 DW0 Data.

Decouple Register 6 DW1

DECOUPREG6DW1 - Decouple Register 6 DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00F34h-00F37h	
DWord	**Bit**	**Description**
0	31	**DecoupReg6DW1GO** Access: R/W Decouple Register 6 DW1 Go_Status Bit, Software writes this bit to 1 when it is ready for the command to be processed, Hardware clears this bit to 0 when the command is complete, Software must not read data or write the next command when this bit is 1.
	29:28	**DecoupReg6DW1PD** Access: R/W Decouple Register 6 DW1, 00 = GTI/Bliteer, 01 = Render, 10= Media , 11= All Domains, Identifies the target power domain that must be awake before proceeding with the cycle.
	27:24	**DecoupReg6DW1OP** Access: R/W Decouple Register 6 DW1, 0000 = Write, 0001 = Read, All others undefined (GT will ignore command and set go/status=0) Decouple Register.
	23:20	**DecoupReg6DW1BE** Access: R/W Decouple Register 6 DW1, Decoupled byte enables. Provided for legacy/workaround purposes only; GT only supports full dword accesses.
	17:0	**DecoupReg6DW1Addr** Access: R/W Decouple Register 6 DW1, Decoupled Address.

Decouple Register 7 DW0

DECOUPREG7DW0 - Decouple Register 7 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00F38h-00F3Bh	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg7DW0Data** Access: R/W Decouple Register 7 DW0 Data.

Decouple Register 7 DW1

DECOUPREG7DW1 - Decouple Register 7 DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00F3Ch-00F3Fh	
DWord	**Bit**	**Description**
0	31	**DecoupReg7DW1GO** Access: R/W Decouple Register 7 DW1 Go_Status Bit, Software writes this bit to 1 when it is ready for the command to be processed, Hardware clears this bit to 0 when the command is complete, Software must not read data or write the next command when this bit is 1.
	29:28	**DecoupReg7DW1PD** Access: R/W Decouple Register 7 DW1, 00 = GTI/Bliteer, 01 = Render, 10= Media , 11= All Domains, Identifies the target power domain that must be awake before proceeding with the cycle.
	27:24	**DecoupReg7DW1OP** Access: R/W Decouple Register 7 DW1, 0000 = Write, 0001 = Read, All others undefined (GT will ignore command and set go/status=0) Decouple Register.
	23:20	**DecoupReg7DW1BE** Access: R/W Decouple Register 7 DW1, Decoupled byte enables. Provided for legacy/workaround purposes only; GT only supports full dword accesses.
	17:0	**DecoupReg7DW1Addr** Access: R/W Decouple Register 7 DW1, Decoupled Address.

Decouple Register 8 DW0

DECOUPREG8DW0 - Decouple Register 8 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00F40h-00F43h	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg8DW0Data** Access: R/W Decouple Register 8 DW0 Data.

Decouple Register 8 DW1

DECOUPREG8DW1 - Decouple Register 8 DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00F44h-00F47h	
DWord	**Bit**	**Description**
0	31	**DecoupReg8DW1GO** Access: R/W Decouple Register 8 DW1 Go_Status Bit, Software writes this bit to 1 when it is ready for the command to be processed, Hardware clears this bit to 0 when the command is complete, Software must not read data or write the next command when this bit is 1.
	29:28	**DecoupReg8DW1PD** Access: R/W Decouple Register 8 DW1, 00 = GTI/Bliteer, 01 = Render, 10= Media , 11= All Domains, Identifies the target power domain that must be awake before proceeding with the cycle.
	27:24	**DecoupReg8DW1OP** Access: R/W Decouple Register 8 DW1, 0000 = Write, 0001 = Read, All others undefined (GT will ignore command and set go/status=0) Decouple Register.
	23:20	**DecoupReg8DW1BE** Access: R/W Decouple Register 8 DW1, Decoupled byte enables. Provided for legacy/workaround purposes only; GT only supports full dword accesses.
	17:0	**DecoupReg8DW1Addr** Access: R/W Decouple Register 8 DW1, Decoupled Address.

Decouple Register 9 DW0

DECOUPREG9DW0 - Decouple Register 9 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00F48h-00F4Bh	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg9DW0Data** Access: R/W Decouple Register 9 DW0 Data.

Decouple Register 9 DW1

DECOUPREG9DW1 - Decouple Register 9 DW1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	00F4Ch-00F4Fh

DWord	Bit	Description
0	31	**DecoupReg9DW1GO** Access: R/W Decouple Register 9 DW1 Go_Status Bit, Software writes this bit to 1 when it is ready for the command to be processed, Hardware clears this bit to 0 when the command is complete, Software must not read data or write the next command when this bit is 1.
	29:28	**DecoupReg9DW1PD** Access: R/W Decouple Register 9 DW1, 00 = GTI/Bliteer, 01 = Render, 10= Media , 11= All Domains, Identifies the target power domain that must be awake before proceeding with the cycle.
	27:24	**DecoupReg9DW1OP** Access: R/W Decouple Register 9 DW1, 0000 = Write, 0001 = Read, All others undefined (GT will ignore command and set go/status=0) Decouple Register.
	23:20	**DecoupReg9DW1BE** Access: R/W Decouple Register 9 DW1, Decoupled byte enables. Provided for legacy/workaround purposes only; GT only supports full dword accesses.
	17:0	**DecoupReg9DW1Addr** Access: R/W Decouple Register 9 DW1, Decoupled Address.

Decouple Register 10 DW0

DECOUPREG10DW0 - Decouple Register 10 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00F50h-00F53h	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg10DW0Data** Access: R/W Decouple Register 10 DW0 Data.

Decouple Register 10 DW1

DECOUPREG10DW1 - Decouple Register 10 DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00F54h-00F57h	
DWord	**Bit**	**Description**
0	31	**DecoupReg10DW1GO** Access: R/W Decouple Register 10 DW1 Go_Status Bit, Software writes this bit to 1 when it is ready for the command to be processed, Hardware clears this bit to 0 when the command is complete, Software must not read data or write the next command when this bit is 1.
	29:28	**DecoupReg10DW1PD** Access: R/W Decouple Register 10 DW1, 00 = GTI/Bliteer, 01 = Render, 10= Media , 11= All Domains, Identifies the target power domain that must be awake before proceeding with the cycle.
	27:24	**DecoupReg10DW1OP** Access: R/W Decouple Register 10 DW1, 0000 = Write, 0001 = Read, All others undefined (GT will ignore command and set go/status=0) Decouple Register.
	23:20	**DecoupReg10DW1BE** Access: R/W Decouple Register 10 DW1, Decoupled byte enables. Provided for legacy/workaround purposes only; GT only supports full dword accesses.
	17:0	**DecoupReg10DW1Addr** Access: R/W Decouple Register 10 DW1, Decoupled Address.

Decouple Register 11 DW0

DECOUPREG11DW0 - Decouple Register 11 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00F58h-00F5Bh	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg11DW0Data** Access: R/W Decouple Register 11 DW0 Data.

Decouple Register 11 DW1

DECOUPREG11DW1 - Decouple Register 11 DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00F5Ch-00F5Fh	
DWord	**Bit**	**Description**
0	31	**DecoupReg11DW1GO** Access: R/W Decouple Register 11 DW1 Go_Status Bit, Software writes this bit to 1 when it is ready for the command to be processed, Hardware clears this bit to 0 when the command is complete, Software must not read data or write the next command when this bit is 1.
	29:28	**DecoupReg11DW1PD** Access: R/W Decouple Register 11 DW1, 00 = GTI/Bliteer, 01 = Render, 10= Media , 11= All Domains, Identifies the target power domain that must be awake before proceeding with the cycle.
	27:24	**DecoupReg11DW1OP** Access: R/W Decouple Register 11 DW1, 0000 = Write, 0001 = Read, All others undefined (GT will ignore command and set go/status=0) Decouple Register.
	23:20	**DecoupReg11DW1BE** Access: R/W Decouple Register 11 DW1, Decoupled byte enables. Provided for legacy/workaround purposes only; GT only supports full dword accesses.
	17:0	**DecoupReg11DW1Addr** Access: R/W Decouple Register 11 DW1, Decoupled Address.

Decouple Register 12 DW0

DECOUPREG12DW0 - Decouple Register 12 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00F60h-00F63h	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg12DW0Data** Access: R/W Decouple Register 12 DW0 Data.

Decouple Register 12 DW1

DECOUPREG12DW1 - Decouple Register 12 DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00F64h-00F67h	
DWord	**Bit**	**Description**
0	31	**DecoupReg12DW1GO** Access: R/W Decouple Register 12 DW1 Go_Status Bit, Software writes this bit to 1 when it is ready for the command to be processed, Hardware clears this bit to 0 when the command is complete, Software must not read data or write the next command when this bit is 1.
	29:28	**DecoupReg12DW1PD** Access: R/W Decouple Register 12 DW1, 00 = GTI/Bliteer, 01 = Render, 10= Media , 11= All Domains, Identifies the target power domain that must be awake before proceeding with the cycle.
	27:24	**DecoupReg12DW1OP** Access: R/W Decouple Register 12 DW1, 0000 = Write, 0001 = Read, All others undefined (GT will ignore command and set go/status=0) Decouple Register.
	23:20	**DecoupReg12DW1BE** Access: R/W Decouple Register 12 DW1, Decoupled byte enables. Provided for legacy/workaround purposes only; GT only supports full dword accesses.
	17:0	**DecoupReg12DW1Addr** Access: R/W Decouple Register 12 DW1, Decoupled Address.

Decouple Register 13 DW0

DECOUPREG13DW0 - Decouple Register 13 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00F68h-00F6Bh	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg13DW0Data** Access: R/W Decouple Register 13 DW0 Data.

Decouple Register 13 DW1

DECOUPREG13DW1 - Decouple Register 13 DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00F6Ch-00F6Fh	
DWord	**Bit**	**Description**
0	31	**DecoupReg13DW1GO** Access: R/W Decouple Register 13 DW1 Go_Status Bit, Software writes this bit to 1 when it is ready for the command to be processed, Hardware clears this bit to 0 when the command is complete, Software must not read data or write the next command when this bit is 1.
	29:28	**DecoupReg13DW1PD** Access: R/W Decouple Register 13 DW1, 00 = GTI/Bliteer, 01 = Render, 10= Media , 11= All Domains, Identifies the target power domain that must be awake before proceeding with the cycle.
	27:24	**DecoupReg13DW1OP** Access: R/W Decouple Register 13 DW1, 0000 = Write, 0001 = Read, All others undefined (GT will ignore command and set go/status=0) Decouple Register.
	23:20	**DecoupReg13DW1BE** Access: R/W Decouple Register 13 DW1, Decoupled byte enables. Provided for legacy/workaround purposes only; GT only supports full dword accesses.
	17:0	**DecoupReg13DW1Addr** Access: R/W Decouple Register 13 DW1, Decoupled Address.

Decouple Register 14 DW0

DECOUPREG14DW0 - Decouple Register 14 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00F70h-00F73h	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg14DW0Data** Access: R/W Decouple Register 14 DW0 Data.

Decouple Register 14 DW1

DECOUPREG14DW1 - Decouple Register 14 DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00F74h-00F77h	
DWord	**Bit**	**Description**
0	31	**DecoupReg14DW1GO** Access: R/W Decouple Register 14 DW1 Go_Status Bit, Software writes this bit to 1 when it is ready for the command to be processed, Hardware clears this bit to 0 when the command is complete, Software must not read data or write the next command when this bit is 1.
	29:28	**DecoupReg14DW1PD** Access: R/W Decouple Register 14 DW1, 00 = GTI/Bliteer, 01 = Render, 10= Media , 11= All Domains, Identifies the target power domain that must be awake before proceeding with the cycle.
	27:24	**DecoupReg14DW1OP** Access: R/W Decouple Register 14 DW1, 0000 = Write, 0001 = Read, All others undefined (GT will ignore command and set go/status=0) Decouple Register.
	23:20	**DecoupReg14DW1BE** Access: R/W Decouple Register 14 DW1, Decoupled byte enables. Provided for legacy/workaround purposes only; GT only supports full dword accesses.
	17:0	**DecoupReg14DW1Addr** Access: R/W Decouple Register 14 DW1, Decoupled Address.

Decouple Register 15 DW0

DECOUPREG15DW0 - Decouple Register 15 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00F78h-00F7Bh	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg15DW0Data** Access: R/W Decouple Register 15 DW0 Data.

Decouple Register 15 DW1

DECOUPREG15DW1 - Decouple Register 15 DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00F7Ch-00F7Fh	
DWord	**Bit**	**Description**
0	31	**DecoupReg15DW1GO** Access: R/W Decouple Register 15 DW1 Go_Status Bit, Software writes this bit to 1 when it is ready for the command to be processed, Hardware clears this bit to 0 when the command is complete, Software must not read data or write the next command when this bit is 1.
	29:28	**DecoupReg15DW1PD** Access: R/W Decouple Register 15 DW1, 00 = GTI/Bliteer, 01 = Render, 10= Media , 11= All Domains, Identifies the target power domain that must be awake before proceeding with the cycle.
	27:24	**DecoupReg15DW1OP** Access: R/W Decouple Register 15 DW1, 0000 = Write, 0001 = Read, All others undefined (GT will ignore command and set go/status=0) Decouple Register.
	23:20	**DecoupReg15DW1BE** Access: R/W Decouple Register 15 DW1, Decoupled byte enables. Provided for legacy/workaround purposes only; GT only supports full dword accesses.
	17:0	**DecoupReg15DW1Addr** Access: R/W Decouple Register 15 DW1, Decoupled Address.

DE Misc Interrupt Definition

DE Misc Interrupt Definition	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	44460h-4446Fh
Name:	Display Engine Miscellaneous Interrupts
ShortName:	DE_MISC_INTERRUPT
Power:	PG0
Reset:	soft

This table indicates which events are mapped to each bit of the Display Engine Miscellaneous Interrupt registers.
0x44460 = ISR
0x44464 = IMR
0x44468 = IIR
0x4446C = IER

DWord	Bit	Description
0	31	**Poison** The ISR is an active high pulse on receiving the poison response to a memory transaction.
	30	**ECC_Double_Error** The ISR is an active high level while any of the ECC Double Error status bits are set.
	29	**Invalid_GTT_page_table_entry** The ISR is an active high pulse on receiving the iMPH invalid GTT page table entry indication.
	28	**Invalid_page_table_entry_data** The ISR is an active high pulse on receiving the iMPH invalid page table entry data indication.
	27	**GSE** The ISR is an active high pulse on the GSE system level event.
	26	**Camera Interrupt Event** This interrupt is no longer used.
	25	**Reserved**
	24	**Reserved**
	23	**WD0_Interrupts_Combined** The ISR is an active high level while any of the WD0_IIR bits are set.
	22	**SVM Device Mode PRQ Event** The ISR is an active high pulse on receiving the iMPH SVM Device Mode PRQ event indication. This event indicates that a GT advanced context encountered a recoverable page fault.
	21	**SVM Device Mode VTD Fault** The ISR is an active high pulse on receiving the iMPH SVM Device Mode VT-d fault indication. This event indicates GT encountered a non-recoverable translation fault.

DE Misc Interrupt Definition		
	20	**SVM Device Mode Wait Descriptor Completion** The ISR is an active high pulse on receiving the iMPH SVM Device Mode Wait Descriptor Completion indication. This event indicates that IMPH completed Invalidation Wait Descriptor.
	19	**SRD_Interrupts_Combined** The ISR is an active high level while any of the SRD_IIR bits are set.
	18	**Reserved** Format: MBZ
	17:16	**Reserved** Format: MBZ
	15	**GTC_Interrupts_Combined** The ISR is an active high level while any of the GTC_IIR bits are set.
	14:9	**Reserved** Format: MBZ
	7:1	**Reserved** Format: MBZ

DE Port Interrupt Definition

DE Port Interrupt Definition	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	44440h-4444Fh
Name:	Display Engine Port Interrupts
ShortName:	DE_PORT_INTERRUPT
Power:	PG0
Reset:	soft

This table indicates which events are mapped to each bit of the Display Engine Port Interrupt registers.
0x44440 = ISR
0x44444 = IMR
0x44448 = IIR
0x4444C = IER

DWord	Bit	Description
0	31	**Reserved**
	30	**Reserved**
	29	**Reserved**
	28	**Reserved**
	27	**AUX Channel D** The ISR is an active high pulse on the AUX DDI D done event. This event will not occur for SRD AUX done.
	26	**AUX Channel C** The ISR is an active high pulse on the AUX DDI C done event. This event will not occur for SRD AUX done.
	25	**AUX Channel B** The ISR is an active high pulse on the AUX DDI B done event. This event will not occur for SRD AUX done.
	24:23	**Reserved**
	22:12	**Reserved**
	11:10	**Reserved**
	9:8	**Reserved**
	7:6	**Reserved**
	5	**DDI C Hotplug** The ISR gives the live state of the DDI HPD pin when the HPD input is enabled. The IIR is set if a short or long pulse is detected when HPD input is enabled. This field is unused in projects that have a PCH.

DE Port Interrupt Definition		
	4	**DDI B Hotplug** The ISR gives the live state of the DDI HPD pin when the HPD input is enabled. The IIR is set if a short or long pulse is detected when HPD input is enabled. This field is unused in projects that have a PCH.
	3	**DDI A Hotplug** The ISR gives the live state of the DDI HPD pin when the HPD input is enabled. The IIR is set if a short or long pulse is detected when HPD input is enabled. This field is unused in projects that have a PCH.
	2	**Reserved**
	1	**Reserved**
	0	**AUX_Channel_A** The ISR is an active high pulse on the AUX DDI A done event. This event will not occur for SRD AUX done.

Depth/Early Depth TLB Partitioning Register

ZSHR - Depth/Early Depth TLB Partitioning Register

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000020
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	04050h

This register is used to determine the number of TLB entries from the total of 64 available to be used by the Depth partition of the TLB. The rest of the entries are used for the Early Depth/Stencil TLB.

DWord	Bit	Description
0	31:6	**Reserved** Format: MBZ
	5:0	**Number of TLB Entries Out of 64 used for Depth TLB** Default Value: 32 The rest are be used for Early Depth/Stencil TLB. Default value is 32.

Device 2 Control

DEV2CTL_0_2_0_PCI - Device 2 Control		
Register Space:	PCI: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	8	
Address:	00058h	
DWord	**Bit**	**Description**
0	0	**Reserved**

Device Enable

DEVEN_0_0_0_PCI - Device Enable

Register Space:	PCI: 0/0/0
Source:	BSpec
Default Value:	0x000084BF
Size (in bits):	32
Address:	00054h

All the bits in this register are LT Lockable.

DWord	Bit	Description
0	15	**Device 8 Enable** Default Value: 1b Access: R/W Lock
	14	**Chap Enable** Default Value: 0b Access: R/W
	13	**Device 6 Enable** Default Value: 0b Access: R/W
	12:11	**Reserved** Format: MBZ
	10	**Device 5 Enable** Default Value: 1b Access: R/W Lock
	9:8	**Reserved** Format: MBZ
	7	**Device 4 Enable** Default Value: 1b Access: R/W Lock
	6	**Reserved** Format: MBZ
	5	**Device 3 enable for Display HD Audio** Default Value: 1b Access: R/W Lock

DEVEN_0_0_0_PCI - Device Enable

	4	**Internal Graphics Engine** Default Value: 1b Access: R/W Lock 0: Bus 0 Device 2 is disabled and hidden 1: Bus 0 Device 2 is enabled and visible This bit will be set to 0b and remain 0b if Device 2 capability is disabled.
	3	**PEG10 Enable** Default Value: 1b Access: R/W Lock
	2	**PEG11 Enable** Default Value: 1b Access: R/W Lock
	1	**PEG12 Enable** Default Value: 1b Access: R/W Lock
	0	**Host Bridge** Default Value: 1b Access: RO

Device Identification

DID2_0_2_0_PCI - Device Identification

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00001916
Size (in bits):	16
Address:	00002h

This register combined with the Vendor Identification register uniquely identifies any PCI device.

DWord	Bit	Description
0	15:8	**Device Identification Number MSB** Default Value: 00011001b Access: R/W Firmware Only This is the upper part of a 16 bit value assigned to the Graphics device.
	7:0	**Device Identification Number SKU** Default Value: 00010110b Access: RO Variant Firmware Only These are bits 7:0 of the 16 bit value assigned to the Graphics device.

DFSDONE

DFSDONE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	51080h-51083h
Name:	Display Fuse Done
ShortName:	DFSDONE
Power:	PG0
Reset:	global

This register is not reset by FLR.

DWord	Bit	Description
0	31:1	**Reserved** Format: MBZ
	0	**Download Done** This field indicates when fuse download is complete. 0b – Note Done 1b – Done

DFSM

DFSM

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	51000h-51003h
Name:	Display Fuse
ShortName:	DFSM
Power:	PG0
Reset:	global

This register contains fuse and strap settings for display. This register is not reset by FLR.

DWord	Bit	Description
0	31	**Internal Graphics Disable** This bit indicates whether internal graphics capability is disabled. Value: 0b, Name: Enable, Description: Internal Graphics Enabled Value: 1b, Name: Disable, Description: Internal Graphics Disabled
	30	**Internal Display Disable** This bit indicates whether the display pipe A (first pipe) capability is disabled. Value: 0b, Name: Enable, Description: Pipe A Capability Enabled Value: 1b, Name: Disable, Description: Pipe A Capability Disabled
	29	**Reserved**
	28	**Display PipeC Disable** This bit indicates whether the display pipe C (third pipe) capability is disabled. Value: 0b, Name: Enable, Description: Pipe C Capability Enabled Value: 1b, Name: Disable, Description: Pipe C Capability Disabled
	27	**Display PM Disable** This bit indicates whether the display power management FBC and DPST capabilities are disabled. Value: 0b, Name: Enable, Description: PM Capability Enabled Value: 1b, Name: Disable, Description: PM Capability Disabled

DFSM

26	**Display eDP Disable** This bit indicates whether the display embedded DisplayPort eDP DDIA capability is disabled. **Value** / **Name** / **Description** 0b / Enable / eDP Capability Enabled 1b / Disable / eDP Capability Disabled
25	**Reserved**
24:23	**Display CDCLK Limit** This field indicates the maximum allowed CD clock frequency. **Value** / **Name** / **Description** 00b / 675 MHz / Maximum frequency is 675 MHz. All frequencies are allowed. 01b / 540 MHz / Maximum frequency is 540 MHz. 10b / 450 MHz / Maximum frequency is 450 MHz. 11b / 337.5 MHz / Maximum frequency is 337.5 MHz. **Restriction** Display software should not select any frequency higher than the maximum that is allowed. If software incorrectly selects a higher frequency, display hardware will internally override the selection to the lowest frequency.
22	**Display Spare**
21	**Spare 21** This bit indicates whether the display pipe B (second pipe) capability is disabled. **Value** / **Name** 0b / Pipe B Capability Enabled 1b / Pipe B Capability Disabled
20	**Display WD Disable** This bit indicates whether the display WD Video capability is disabled. **Value** / **Name** / **Description** 0b / Enable / WD Capability Enabled 1b / Disable / WD Capability Disabled
19	**Spare 19**
18	**Spare 18**
17	**Spare 17**
16	**Spare 16**
15	**Spare 15**
14	**Spare 14**
13	**Spare 13**
12	**Spare 12**
11	**Spare 11**

DFSM

	10	**Spare 10**
	9	**Spare 9**
	8	**Spare 8**
	7	**Spare 7**
	6	**Display RSB Enable** This bit indicates whether the remote screen blanking feature is enabled in the display engine.
	5	**Spare 5**
	4	**Spare 4**
	3	**Spare 3**
	2	**Spare 2**
	1	**Reserved**
	0	**Display Audio Codec Disable** This bit indicates whether the display audio codec capability is disabled.

Value	Name	Description
0b	Disable	RSB Capability Disabled
1b	Enable	RSB Capability Enabled

Value	Name	Description
0b	Enable	Audio Codec Capability Enabled
1b	Disable	Audio Codec Capability Disabled

DISPIO_CR_TX_BMU_CR0

DISPIO_CR_TX_BMU_CR0	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6C00Ch-6C00Fh
Name:	DISPIO_CR_TX_BMU_CR0
ShortName:	DISPIO_CR_TX_BMU_CR0
Power:	PG0
Reset:	global

The tx_blnclegsctl values are only used when tx_blnclegdisbl==0x00 and DDI_BUF_TRANS dword 0 bit 31==0x1 for the associated DDI.

DWord	Bit	Description
0	31:29	**digital_analog** Display software must not change this field.
	28	**tx_glb_vs_loc_vref_sel** Display software must not change this field.
	27:23	**tx_blnclegdisbl** Disable balance leg
	22:20	**tx_blnclegsctl_4** Balance leg select DDI4 (DDIE)
	19:17	**tx_blnclegsctl_3** Balance leg select DDI3 (DDID)
	16:14	**tx_blnclegsctl_2** Balance leg select DDI2 (DDIC)
	13:11	**tx_blnclegsctl_1** Balance leg select for DDI1 (DDIB)
	10:8	**tx_blnclegsctl_0** Balance leg select for DDI0 (DDIA)
	7:0	**tx_h_mode** Display software must not change this field.

Display CSR Program

Display CSR Program	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000, 0x00000000,

Display CSR Program
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Display CSR Program	
	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	98304
Address:	80000h-82FFFh
Name:	Display CSR Program
Power:	PG0
Reset:	global

This address range is used to store the display context save and restore program.

DWord	Bit	Description
0..3071	31:0	**Program**

Display Message Forward Status Register

DISPLAY_MESSAGE_FORWARD_STATUS - Display Message Forward Status Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	022E8h-022EBh
Name:	Display Message Forward Status Register
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_RCSUNIT
Address:	122E8h-122EBh
Name:	Display Message Forward Status Register
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_VCSUNIT0
Address:	1A2E8h-1A2EBh
Name:	Display Message Forward Status Register
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_VECSUNIT
Address:	1C2E8h-1C2EBh
Name:	Display Message Forward Status Register
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_VCSUNIT1
Address:	222E8h-222EBh
Name:	Display Message Forward Status Register
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_BCSUNIT

This register stores the internal HW status flags related to display message forward logic. This register should not be accessed by SW. This register is part of power context image. Note: Even though this register exists in VideoCS and VideoEnhancementCS, individual bit driven functionality is not supported.

DWord	Bit	Description
0	31:30	**Reserved** Source: RenderCS, BlitterCS Format: MBZ
	29:28	**Reserved**
	27:26	**Reserved**
	25:24	**Reserved**
	23:22	**Reserved**
	21:20	**Reserved**
	19:18	**Reserved**

DISPLAY_MESSAGE_FORWARD_STATUS - Display Message Forward Status Register

	17:16	**Reserved**
	15:14	**Reserved**
	13:12	**Reserved**
	11:10	**Reserved**
	9:8	**Reserved**
	7:6	**Reserved**
	5:4	**Reserved**
	3:2	**Reserved**
	31:0	**Reserved** Source: VideoCS, VideoCS2, VideoEnhancementCS Format: MBZ
	1:0	**Reserved**

DOUBLE_BUFFER_CTL

DOUBLE_BUFFER_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	44500h-44503h
Name:	Double Buffer Control
ShortName:	DOUBLE_BUFFER_CTL
Power:	PG0
Reset:	soft

This register together with the Allow Double Buffer Disable fields in the plane control registers allows for the double buffer update of registers in multiple resources to be synchronized together for an atomic update.

Programming Notes

Sequence for synchronizing the double buffer updates of multiple resources:
1. Set the Allow Double Buffer Update Disable field for each resource to be synchronized together and write the appropriate register to arm and trigger the update. Set the Global Double Buffer Update Disable field. The order in which these fields are set does not matter.
2. Program the registers that need to be synchronized together.
3. Clear the Global Double Buffer Update Disable field. Any pending updates will take place at the next periodic udate event.
4. If a resource no longer needs to be synchronized, clear the Allow Double Buffer Update Disable field for that resource and write the appropriate register to arm and trigger the update. If the resource will continue to be synchronized, the field can remain set and does not need to be set again when returning to step 1 of this sequence.

DWord	Bit	Description
0	31:1	**Reserved** Format: MBZ
	0	**Global Double Buffer Update Disable** This field controls whether the double buffer update is disabled for the resources which have allowed it to be disabled. This only disables the double buffer update for periodic events, like the start of vertical blank. It does not change the behavior for constant events, like pipe not enabled. This applies to MMIO register updates as well as command streamer initiated flips. When the double buffer update is disabled, the values written into the double buffered registers will not take effect at the periodic update event. After the double buffer update is no longer disabled, any pending updates will take place at the next periodic update event. Asynchronous flips initiated by MMIO or command streamers are not effected by disabling double buffering. Synchronous flips (regular and stereo 3D) initiated by MMIO or command streamers will not

DOUBLE_BUFFER_CTL

complete or give the flip done indication while double buffering is disabled for a plane. They will complete and give the flip done at the next start of vertical blank (selectable right or left eye vertical blank when using stereo 3D) after the double buffering is re-enabled.

Value	Name
0b	Not Disabled
1b	Disabled

DP_TP_CTL

DP_TP_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	64040h-64043h
Name:	DDI A DisplayPort Transport Control
ShortName:	DP_TP_CTL_A
Power:	PG1
Reset:	soft
Address:	64140h-64143h
Name:	DDI B DisplayPort Transport Control
ShortName:	DP_TP_CTL_B
Power:	PG2
Reset:	soft
Address:	64240h-64243h
Name:	DDI C DisplayPort Transport Control
ShortName:	DP_TP_CTL_C
Power:	PG2
Reset:	soft
Address:	64340h-64343h
Name:	DDI D DisplayPort Transport Control
ShortName:	DP_TP_CTL_D
Power:	PG2
Reset:	soft
Address:	64440h-64443h
Name:	DDI E DisplayPort Transport Control
ShortName:	DP_TP_CTL_E
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31	**Transport Enable** This bit enables the DisplayPort transport function. Value: 0b — Name: Disable

DP_TP_CTL

	1b	Enable

30:28 Reserved

Format:	MBZ

27 Transport Mode Select

Description
This bit selects between DisplayPort SST and MST modes of operation. This bit is ignored by DDI A (EDP) and DDI E since they do not support multistreaming.

Value	Name	Description
0b	SST mode	DisplayPort SST mode
1b	MST mode	DisplayPort MST mode

Restriction
The DisplayPort mode (SST or MST) selected here must match the mode selected in the Transcoder DDI Function Control registers for the transcoders attached to this transport. This field must not be changed while the DDI function is enabled.

26 Reserved

Format:	MBZ

25 Force ACT

Description
This bit forces DisplayPort MST ACT to be sent one time at the next link frame boundary. After ACT is sent, as indicated in the ACT sent status bit, this bit can be cleared and set again to send ACT again. This bit is ignored by DDI A (EDP) and DDI E since they do not support multistreaming.

Value	Name	Description
0b	Do not force	Do not force ACT to be sent
1b	Force	Force ACT to be sent one time

24:21 Reserved

Format:	MBZ

20:19 Reserved

Format:	MBZ

DP_TP_CTL

18 Enhanced Framing Enable

Description
This bit selects enhanced framing for DisplayPort SST.
Hardware internally enables enhanced framing for DisplayPort MST.

Value	Name
0b	Disabled
1b	Enabled

Restriction
In DisplayPort MST mode this bit must be set to Disabled. This field must not be changed while the DDI function is enabled.

17:16 Reserved

Format:	MBZ

15 Reserved

Format:	MBZ

14:11 Reserved

Format:	MBZ

10:8 DP Link Training Enable

These bits are used for DisplayPort link initialization as defined in the DisplayPort specification. DP_TP_STATUS has an indication that the required number of idle patterns has been sent.

Value	Name	Description
000b	Pattern 1	Training Pattern 1 enabled
001b	Pattern 2	Training Pattern 2 enabled
010b	Idle	Idle Pattern enabled
011b	Normal	Link not in training: Send normal pixels
100b	Pattern 3	Training Pattern 3 enabled
Others	Reserved	Reserved

Restriction
When enabling the port, it must be turned on with pattern 1 enabled. When retraining a link, the port must be disabled, then re-enabled with pattern 1 enabled.

7 Reserved

DP_TP_CTL

	6	**Alternate SR Enable** This bit enables the DisplayPort Alternate Scrambler Reset, intended for use only with embedded DisplayPort receivers. **Value** / **Name** 0b — Disable 1b — Enable **Restriction** This field must not be changed while the DDI function is enabled.
	5:0	**Reserved** Format: MBZ

DP_TP_STATUS

DP_TP_STATUS	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	64144h-64147h
Name:	DDI B DisplayPort Transport Status
ShortName:	DP_TP_STATUS_B
Valid Projects:	
Power:	PG2
Reset:	soft
Address:	64244h-64247h
Name:	DDI C DisplayPort Transport Status
ShortName:	DP_TP_STATUS_C
Valid Projects:	
Power:	PG2
Reset:	soft
Address:	64344h-64347h
Name:	DDI D DisplayPort Transport Status
ShortName:	DP_TP_STATUS_D
Valid Projects:	
Power:	PG2
Reset:	soft
Address:	64444h-64447h
Name:	DDI E DisplayPort Transport Status
ShortName:	DP_TP_STATUS_E
Valid Projects:	
Power:	PG2
Reset:	soft

There is one DisplayPort Transport Status register per each DDI B/C/D/E/F. DDI A does not have a status register.

DWord	Bit	Description	
0	31:28	**Reserved**	
		Format:	MBZ

DP_TP_STATUS

27 Idle Link Frame Status

Access:	R/WC

This bit indicates if a link frame boundary has been sent in idle pattern. This is a sticky bit, cleared by writing 1b to it.

Value	Name
0b	Idle link frame not sent
1b	Idle link frame sent

26 Active Link Frame Status

Access:	R/WC

This bit indicates if a link frame boundary has been sent in active (at least one VC enabled). This is a sticky bit, cleared by writing 1b to it.

Value	Name
0b	Active link frame not sent
1b	Active link frame sent

25 Min Idles Sent

Access:	RO

This bit indicates that the minimum required number of idle patterns has been sent when DP_TP_CTL is set to send idle patterns. This bit will clear itself when DP_TP_CTL is not longer set to send idle patterns.

Value	Name
0b	Min idles not sent
1b	Min idles sent

24 ACT Sent Status

Access:	R/WC

This bit indicates if DisplayPort MST ACT has been sent. This is a sticky bit, cleared by writing 1b to it.

Value	Name
0b	ACT not sent
1b	ACT sent

23 Mode Status

Access:	RO

This bit indicates what mode the transport is currently in.

Value	Name	Description
0b	SST	Single-stream mode
1b	MST	Multi-stream mode

22:18 Reserved

Format:	MBZ

DP_TP_STATUS

17:16 Streams Enabled

Access:	RO

This field indicates the number of streams (transcoders) enabled on this port during multistream operation. This field should be ignored in single stream mode.

Value	Name	Description
00b	Zero	Zero streams enabled
01b	One	One stream enabled
10b	Two	Two streams enabled
11b	Three	Three streams enabled

15:13 Reserved

Format:	MBZ

12 Reserved

Format:	MBZ

11:10 Reserved

Format:	MBZ

9:8 Payload Mapping VC2

Access:	RO

This field indicates which transcoder is mapped to Virtual Channel 2 during multistream operation. This field should be ignored if the number of streams enabled is less than three. This field should be ignored in single stream mode.

Value	Name	Description
00b	A	Transcoder A mapped to this VC
01b	B	Transcoder B mapped to this VC
10b	C	Transcoder C mapped to this VC
11b	Reserved	Reserved

7:6 Reserved

Format:	MBZ

5:4 Payload Mapping VC1

Access:	RO

This field indicates which transcoder is mapped to Virtual Channel 1 during multistream operation. This field should be ignored if the number of streams enabled is less than two. This field should be ignored in single stream mode.

Value	Name	Description
00b	A	Transcoder A mapped to this VC
01b	B	Transcoder B mapped to this VC
10b	C	Transcoder C mapped to this VC
11b	Reserved	Reserved

DP_TP_STATUS

	3:2	**Reserved** Format: MBZ
	1:0	**Payload Mapping VC0** Access: RO This field indicates which transcoder is mapped to Virtual Channel 0 during multistream operation. This field should be ignored if the number of streams enabled is less than one. This field should be ignored in single stream mode.

Value	Name	Description
00b	A	Transcoder A mapped to this VC
01b	B	Transcoder B mapped to this VC
10b	C	Transcoder C mapped to this VC
11b	Reserved	Reserved

DPLL_CFGCR1

DPLL_CFGCR1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6C040h-6C043h
Name:	DPLL1_CFGCR1
ShortName:	DPLL1_CFGCR1
Power:	PG0
Reset:	global
Address:	6C048h-6C04Bh
Name:	DPLL2_CFGCR1
ShortName:	DPLL2_CFGCR1
Power:	PG0
Reset:	global
Address:	6C050h-6C053h
Name:	DPLL3_CFGCR1
ShortName:	DPLL3_CFGCR1
Power:	PG0
Reset:	global

This register, together with DPLL_CFGCR2, is used to configure the frequency for DPLL1, DPLL2, and DPLL3, when DPLL_CTRL1 override is enabled and set to HDMI mode.
This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31	**Frequency Enable** Programmable HDMI/DVI frequency enable Value: 0b = Disable; 1b = Enable
	30:24	**Reserved** Format: MBZ
	23:9	**DCO Fraction** (DCO Frequency/24 - INT(DCO Frequency/24)) * 2^15
	8:0	**DCO Integer** INT (DCO Frequency/24)

DPLL_CFGCR2

DPLL_CFGCR2	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6C044h-6C047h
Name:	DPLL1_CFGCR2
ShortName:	DPLL1_CFGCR2
Power:	PG0
Reset:	global
Address:	6C04Ch-6C04Fh
Name:	DPLL2_CFGCR2
ShortName:	DPLL2_CFGCR2
Power:	PG0
Reset:	global
Address:	6C054h-6C057h
Name:	DPLL3_CFGCR2
ShortName:	DPLL3_CFGCR2
Power:	PG0
Reset:	global

This register, together with DPLL_CFGCR1, is used to configure the frequency for DPLL1, DPLL2, and DPLL3, when DPLL_CTRL1 override is enabled and set to HDMI mode.
This register is not reset by the device 2 FLR.

Programming Notes
P0 is P, P1 is Q, P2 is K. The post divider is P*Q*K (P0*P1*P2).

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:8	**Qdiv Ratio** This field specifies the Q (P1) divider ratio. This field is only used when Qdiv Mode is set to Enable to get a divider value other than 1.

DPLL_CFGCR2

7 — Qdiv Mode

This field enables the Q (P1) divider when the ratio is not 1.

Value	Name	Description
0b	Disable	Q divider = 1
1b	Enable	Q divider = Qdiv Ratio

Restriction
If K (P2) is not 2, Q (P1) MUST be 1 to ensure 50% duty cycle.

6:5 — Kdiv

This field specifies the K (P2) divider ratio.

Value	Name
00b	5
01b	2
10b	3
11b	1

4:2 — Pdiv

This field specifies the P (P0) divider ratio.

Value	Name	Programming Notes
000b	1	P (P0) can only be 1 if Q (P1) is also 1.
001b	2	
010b	3	
100b	7	

1:0 — Central Frequency

This field specifies the center frequency.

Value	Name
00b	9600 MHz
01b	9000 MHz
10b	Reserved
11b	8400 MHz

DPLL_CTRL1

DPLL_CTRL1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6C058h-6C05Bh
Name:	DPLL_CTRL1
ShortName:	DPLL_CTRL1
Power:	PG0
Reset:	global

This register controls the DPLL mode, rate, and SSC.
This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31:28	**Reserved** Format: MBZ
	27	**Reserved**
	26	**Reserved**
	25	**Reserved**
	24	**Reserved**
	23	**DPLL3 HDMI Mode** Select between DP and HDMI mode Value / Name / Description: 0b / DP mode / Frequency and SSC programmed in this register. 1b / HDMI mode / Frequency is programmed in DPLL*_CFGCR* registers.
	22	**DPLL3 SSC** SSC enable Value / Name: 0b / Disable 1b / Enable
	21:19	**DPLL3 Link Rate** Link rate for DP mode Value / Name / Description: 000b / 2700 / 2700 MHz (DP 5.4 GHz) - VCO 8100 001b / 1350 / 1350 MHz (DP 2.7 GHz) - VCO 8100 010b / 810 / 810 MHz (DP 1.62 GHz) - VCO 8100

DPLL_CTRL1

011b	1620	1620 MHz (DP 3.24 GHz) - VCO 8100
100b	1080	1080 MHz (DP 2.16 GHz) - VCO 8640
101b	2160	2160 MHz (DP 4.32 GHz) - VCO 8640
110b	Reserved	Reserved
111b	Reserved	Reserved

18 **DPLL3 Override**

Programming enable

Value	Name
0b	Disable
1b	Enable

17 **DPLL2 HDMI Mode**

Select between DP and HDMI mode

Value	Name	Description
0b	DP mode	Frequency and SSC programmed in this register.
1b	HDMI mode	Frequency is programmed in DPLL*_CFGCR* registers.

16 **DPLL2 SSC**

SSC enable

Value	Name
0b	Disable
1b	Enable

15:13 **DPLL2 Link Rate**

Link rate for DP mode

Value	Name	Description
000b	2700	2700 MHz (DP 5.4 GHz) - VCO 8100
001b	1350	1350 MHz (DP 2.7 GHz) - VCO 8100
010b	810	810 MHz (DP 1.62 GHz) - VCO 8100
011b	1620	1620 MHz (DP 3.24 GHz) - VCO 8100
100b	1080	1080 MHz (DP 2.16 GHz) - VCO 8640
101b	2160	2160 MHz (DP 4.32 GHz) - VCO 8640
110b	Reserved	Reserved
111b	Reserved	Reserved

12 **DPLL2 Override**

Programming enable

Value	Name
0b	Disable
1b	Enable

DPLL_CTRL1

11 — DPLL1 HDMI Mode

Select between DP and HDMI mode

Value	Name	Description
0b	DP mode	Frequency and SSC programmed in this register.
1b	HDMI mode	Frequency is programmed in DPLL*_CFGCR* registers.

10 — DPLL1 SSC

SSC enable

Value	Name
0b	Disable
1b	Enable

9:7 — DPLL1 Link Rate

Link rate for DP mode

Value	Name	Description
000b	2700	2700 MHz (DP 5.4 GHz) - VCO 8100
001b	1350	1350 MHz (DP 2.7 GHz) - VCO 8100
010b	810	810 MHz (DP 1.62 GHz) - VCO 8100
011b	1620	1620 MHz (DP 3.24 GHz) - VCO 8100
100b	1080	1080 MHz (DP 2.16 GHz) - VCO 8640
101b	2160	2160 MHz (DP 4.32 GHz) - VCO 8640
110b	Reserved	Reserved
111b	Reserved	Reserved

6 — DPLL1 Override

Programming enable

Value	Name
0b	Disable
1b	Enable

5 — Reserved

4 — Reserved

3:1 — DPLL0 Link Rate

Link rate for DP mode

Value	Name	Description
000b	2700	2700 MHz (DP 5.4 GHz) - VCO 8100
001b	1350	1350 MHz (DP 2.7 GHz) - VCO 8100
010b	810	810 MHz (DP 1.62 GHz) - VCO 8100
011b	1620	1620 MHz (DP 3.24 GHz) - VCO 8100
100b	1080	1080 MHz (DP 2.16 GHz) - VCO 8640
101b	2160	2160 MHz (DP 4.32 GHz) - VCO 8640

DPLL_CTRL1

		110b	Reserved	Reserved
		111b	Reserved	Reserved
	0	**DPLL0 Override** Programming enable		

Value	Name
0b	Disable
1b	Enable

DPLL_CTRL2

DPLL_CTRL2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6C05Ch-6C05Fh
Name:	DPLL_CTRL2
ShortName:	DPLL_CTRL2
Power:	PG0
Reset:	global

This register controls the mapping of DPLL to port.
This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23	**Reserved**
	22	**Reserved**
	21	**Reserved**
	20	**Reserved**
	19	**DDIE Clock Off** DDIE (DDI4, EDP2) gate the clock going to the port 0b: On 1b: Off
	18	**DDID Clock Off** DDID (DDI3) gate the clock going to the port 0b: On 1b: Off
	17	**DDIC Clock Off** DDIC (DDI2) gate the clock going to the port 0b: On 1b: Off
	16	**DDIB Clock Off** DDIB (DDI1) gate the clock going to the port

DPLL_CTRL2

Value	Name
0b	On
1b	Off

15 **DDIA Clock Off**

DDIA (DDI0, EDP) gate the clock going to the port

Value	Name
0b	On
1b	Off

14:13 **DDIE Clock Select**

DDIE (DDI4, EDP2) port mux select

Value	Name
00b	DPLL0
01b	DPLL1
10b	DPLL2
11b	DPLL3

12 **DDIE Select Override**

DDIE (DDI4, EDP2) programming enable

Value	Name
0b	Disable
1b	Enable

11:10 **DDID Clock Select**

DDID (DDI3) port mux select

Value	Name
00b	DPLL0
01b	DPLL1
10b	DPLL2
11b	DPLL3

9 **DDID Select Override**

DDID (DDI3) programming enable

Value	Name
0b	Disable
1b	Enable

8:7 **DDIC Clock Select**

DDIC (DDI2) port mux select

Value	Name
00b	DPLL0
01b	DPLL1

DPLL_CTRL2

10b	DPLL2
11b	DPLL3

6 — DDIC Select Override

DDIC (DDI2) programming enable

Value	Name
0b	Disable
1b	Enable

5:4 — DDIB Clock Select

DDIB (DDI1) port mux select

Value	Name
00b	DPLL0
01b	DPLL1
10b	DPLL2
11b	DPLL3

3 — DDIB Select Override

DDIB (DDI1) programming enable

Value	Name
0b	Disable
1b	Enable

2:1 — DDIA Clock Select

DDIA (DDI0, EDP) port mux select

Value	Name
00b	DPLL0
01b	DPLL1
10b	DPLL2
11b	DPLL3

0 — DDIA Select Override

DDIA (DDI0, EDP) programming enable

Value	Name
0b	Disable
1b	Enable

DPLL_STATUS

DPLL_STATUS

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6C060h-6C063h
Name:	DPLL_STATUS
ShortName:	DPLL_STATUS
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28	**DPLL3 SEM Done** Access: RO Value: 0b – Not Done Value: 1b – Done
	27:25	**Reserved** Format: MBZ
	24	**DPLL3 Lock** Access: RO Value: 0b – Not Locked Value: 1b – Locked
	23:21	**Reserved** Format: MBZ
	20	**DPLL2 SEM Done** Access: RO Value: 0b – Not Done Value: 1b – Done

DPLL_STATUS

	19:17	**Reserved** Format: MBZ
	16	**DPLL2 Lock** Access: RO Value: 0b — Name: Not Locked Value: 1b — Name: Locked
	15:13	**Reserved** Format: MBZ
	12	**DPLL1 SEM Done** Access: RO Value: 0b — Name: Not Done Value: 1b — Name: Done
	11:9	**Reserved** Format: MBZ
	8	**DPLL1 Lock** Access: RO Value: 0b — Name: Not Locked Value: 1b — Name: Locked
	7:5	**Reserved** Format: MBZ
	4	**DPLL0 SEM Done** Access: RO Value: 0b — Name: Not Done Value: 1b — Name: Done
	3:1	**Reserved** Format: MBZ
	0	**DPLL0 Lock** Access: RO

DPLL_STATUS

Value	Name
0b	Not Locked
1b	Locked

DPST_BIN

DPST_BIN	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank
Address:	490C4h-490C7h
Name:	Pipe DPST Bin Data
ShortName:	DPST_BIN_A
Power:	PG1
Reset:	soft
Address:	491C4h-491C7h
Name:	Pipe DPST Bin Data
ShortName:	DPST_BIN_B
Power:	PG2
Reset:	soft
Address:	492C4h-492C7h
Name:	Pipe DPST Bin Data
ShortName:	DPST_BIN_C
Power:	PG2
Reset:	soft

Access to this address are steered to the correct register by programming the Bin Register Function Select and the Bin Register Index. Updates take place at the start of vertical blank.

DWord	Bit	Description
0	31	**Busy Bit** If (DPST_CTL:Bin Register Function Select = Threshold Count) {This is a read only bit. If set, the engine is busy and the rest of the register is undefined. If clear, the register contains valid data.} Else (Image Enhancement) {This bit is reserved.}
	30:24	**Reserved**

DPST_BIN		
	23:0	**Data** If (DPST_CTL : Bin Register Function Select = Threshold Count) {Bits 23:0 are read only bits. They indicate the total number of pixels in this bin. The bin value is updated when guardband interrupt delay is met, and is not valid until after a histogram event has occurred. The bin value will stop incrementing once the maximum has been reached.} Else (Image Enhancement) {Bits 23:10 are reserved and should be written as zeroes. Bits 9:0 are R/W double-buffered and program the correction value for this bin. Writes to this register are double buffered on the next vblank. The value written here is the 10bit corrected channel value for the lowest point of the bin.}

DPST_CTL

DPST_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	490C0h-490C3h
Name:	Pipe DPST Control
ShortName:	DPST_CTL_A
Power:	PG1
Reset:	soft
Address:	491C0h-491C3h
Name:	Pipe DPST Control
ShortName:	DPST_CTL_B
Power:	PG2
Reset:	soft
Address:	492C0h-492C3h
Name:	Pipe DPST Control
ShortName:	DPST_CTL_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31	**IE Histogram Enable** This bit enables the Image Enhancement histogram logic to collect data. The collected data will be valid after a histogram event has occurred. **Value** / **Name** 0b – Disable 1b – Enable **Programming Notes** If histogram is enabled while no planes are enabled on the pipe, it may get an incorrect pixel count for a frame.
	30:28	**Reserved**

DPST_CTL

27	**IE Modification Table Enable** This bit enables the Image Enhancement modification table. When enabled, modifications begin after the next vertical blank.

Value	Name
0b	Disable
1b	Enable

26:25	**Reserved**
24	**Histogram Mode Select**

Value	Name	Description
0b	YUV	YUV Luma Mode
1b	HSV	HSV Intensity Mode

23:16	**Reserved**
15	**IE Table Value Format** This field indicates what format is used for the image enhancement table values.

Value	Name	Description
0b	1.9	1 integer and 9 fractional bits
1b	2.8	2 integer and 8 fractional bits

14:13	**Enhancement mode**

Value	Name	Description
00b	Direct	Direct look up mode
01b	Additive	Additive mode
10b	Multiplicative	Multiplicative mode
11b	Reserved	Reserved

12	**Reserved**
11	**Bin Register Function Select** This field indicates what data is being written to or read from the bin data register.

Value	Name	Description
0b	TC	Threshold Count. A read from the bin data register returns that bin's threshold value from the most recent vblank load event (guardband threshold trip). Valid range for the Bin Index is 0 to 31.
1b	IE	Image Enhancement Value. Valid range for the Bin Index is 0 to 32

10:7	**Reserved**
6:0	**Bin Register Index** This field indicates the bin number whose data can be accessed through the bin data register. This value is automatically incremented by a read or a write to the bin data register if the busy bit is not set.

DPST_GUARD

DPST_GUARD

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank

Address:	490C8h-490CBh
Name:	Pipe DPST Threshold Guardband
ShortName:	DPST_GUARD_A
Power:	PG1
Reset:	soft

Address:	491C8h-491CBh
Name:	Pipe DPST Threshold Guardband
ShortName:	DPST_GUARD_B
Power:	PG2
Reset:	soft

Address:	492C8h-492CBh
Name:	Pipe DPST Threshold Guardband
ShortName:	DPST_GUARD_C
Power:	PG2
Reset:	soft

Updates take place at the start of vertical blank.

DWord	Bit	Description
0	31	**Histogram Interrupt enable** Value / Name / Description 0b / Disable / Disabled 1b / Enable / This generates a histogram interrupt once a Histogram event occurs.
	30	**Histogram Event status** Access: R/WC When a Histogram event has occurred, this will get set by the hardware. For any more Histogram events to occur, clear this bit by writing a '1'. Value / Name / Description 0b / Not Occurred / Histogram event has not occurred 1b / Occured / Histogram event has occurred

DPST_GUARD		
	29:22	**Guardband Interrupt Delay** An interrupt is always generated after this many consecutive frames of the guardband threshold being surpassed. This value is double buffered on start of vblank. **Restriction** A value of 0 is invalid.
	21:0	**Threshold Guardband** This value is used to determine the guardband for the threshold interrupt generation. This single value is used for all the segments. This value is double buffered on start of vblank. This value is shifted left 2 bits (multiplied by 4) for use with the 24 bit bin values.

Driver Media Force Wake Ack

DRIVER_MEDIA_FWAKE_ACK - Driver Media Force Wake Ack

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	00D88h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].
To set bit0, for example, the data would be 0x0001_0001.
To clear bit0, for example, the data would be 0x0001_0000.
Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO
	15:0	**GPM Driver Media ForceWake Ack** Access: R/W 1'b0 : GT Media Can be powered down (default) 1'b1 : GT Media cannot be powered down

Driver Render Force Wake Ack

DRIVER_RENDER_FWAKE_ACK - Driver Render Force Wake Ack

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	00D84h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].
To set bit0, for example, the data would be 0x0001_0001.
To clear bit0, for example, the data would be 0x0001_0000.
Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO
	15:0	**GPM Driver ForceWake Ack** Access: R/W 1'b0 : GT Render Can be powered down (default) 1'b1 : GT Render cannot be powered down

DS Invocation Counter

DS_INVOCATION_COUNT - DS Invocation Counter	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02308h

This register stores the number of domain points shaded by the DS threads. Domain points which hit in the DS cache will not cause this register to increment. Note that the spawning of a DS thread which shades two domain points will cause this counter to increment by two.This register is part of the context save and restore.

DWord	Bit	Description
0	63:32	**DS Invocation Count UDW** Number of domain points shaded by the DS threads. Updated only when DS Function Enable and Statistics Enable are set in 3DSTATE_DS
	31:0	**DS Invocation Count LDW** Number of domain points shaded by the DS threads. Updated only when DS Function Enable and Statistics Enable are set in 3DSTATE_DS

DSSM

DSSM	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	51004h-51007h
Name:	Display Strap State
ShortName:	DSSM
Power:	PG0
Reset:	global

This register contains fuse and strap settings for display. This register is not reset by FLR.

DWord	Bit	Description
0	31	**Spare 31**
	30	**Spare 30**
	29	**Spare 29**
	28	**Spare 28**
	27	**Spare 27**
	26	**Spare 26**
	25	**Spare 25**
	24	**Spare 24**
	23	**Spare 23**
	22	**Spare 22**
	21	**Spare 21**
	20	**Spare 20**
	19	**Spare 19**
	18	**Spare 18**
	17	**Spare 17**
	16	**Spare 16**
	15	**Spare 15**
	14	**Spare 14**
	13	**Spare 13**
	12	**Spare 12**
	11	**Spare 11**
	10	**Spare 10**

DSSM

	9	**Spare 9**
	8	**Spare 8**
	7	**Spare 7**
	6	**Spare 6**
	5	**Spare 5**
	4	**Spare 4**
	3	**Spare 3**
	2	**LCPLL Unavail** This bit specifies the availability of some LCPLL output frequencies.

Value	Name	Description
0b	Available	LCPLL available
1b	Not available	LCPLL not available

	1	**Spare 1**
	0	**DisplayPort A Present** This bit specifies whether the port was present during initalization. This strap state can also be read in the DDI_BUF_CTL_A 0x64000 register bit 0.

Value	Name	Description
0b	Not Present	Port not present
1b	Present	Port present

DX9 Constants Not Consumed By RCS

DX9CONST_PRODUCE_COUNT - DX9 Constants Not Consumed By RCS

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	02484h

This register keeps track of the outstanding DX9 Constants produced by RS which are not yet consumed by Render Command Streamer. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0	31:0	**DX9 Constants Produce Count** This register keeps track of the outstanding DX9 Constants produced by RS which are not yet consumed by Render Command Streamer. This register is part of the render context save and restore.

DX9 Constants Prsed By RCS

DX9CONST_PARSE_COUNT - DX9 Constants Prsed By RCS

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	02494h

This register keeps track of the DX9 Constant commands parsed by RCS prior to encountering the Draw Call in an RS enabled Batch Buffer which has DX9 Pool Alloc Valid. DX9 parse count should be less then equal to the DX9 produce count for Command Streamer to make progress on a 3D_PRIMITIVE command. DX9 Parse count is subtracted from the DX9 Produce Count upon parsing 3D_PRIMITIVE command. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0	31:0	**DX9 Constants Produce Count** This register keeps track of the DX9 Constant commands parsed by RCS prior to encountering the Draw Call in an RS enabled Batch Buffer which has DX9 Pool Alloc Valid. DX9 parse count should be less then equal to the DX9 produce count for Command Streamer to make progress on a 3D_PRIMITIVE command. DX9 Parse count is subtracted from the DX9 Produce Count upon parsing 3D_PRIMITIVE command.

ECO reg 1

ECOREG1 - ECO reg 1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00FF8h-00FFBh	
DWord	**Bit**	**Description**
0	31	**Lock Bit** Access: R/W Lock Lock bit for this register
	30:0	**Reserved**

ECO Reserved

ECORESRV - ECO Reserved			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	09898h		
ECO Reserved bits			
DWord	**Bit**	**Description**	
0	31:16	**ECO Reserved Bits**	
		Access:	R/WC
	15:0	**Ita p-value config**	
		Access:	R/WC

Element Descriptor Register

ELEM_DESCRIPTOR - Element Descriptor Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000, 0x00000000
Access:	RO
Size (in bits):	64
Address:	04500h
Name:	BCS Element Descriptor Register
ShortName:	BCS_ELEM_DESCRIPTOR
Address:	04400h
Name:	RCS Element Descriptor Register
ShortName:	RCS_ELEM_DESCRIPTOR
Address:	04440h
Name:	VCS Element Descriptor Register
ShortName:	VCS_ELEM_DESCRIPTOR
Address:	044C0h
Name:	VECS Element Descriptor Register
ShortName:	VECS_ELEM_DESCRIPTOR
Element Information: The register is populated by command streamer and consumed by GAM	

DWord	Bit	Description
0	63:32	**Context ID** Context identification number assigned to separate this context from others. Context IDs needs to be recycled in such a way that there could not be two active context with the same ID. This is a unique identification number by which a context is identified and referenced
	31:12	**LRCA** Command Streamer Only
	11:9	**Function Number** GFX device is considered to be on Bus0 with device number of 2. Function number is normally assigned as "0" however for gfx virtualization; there would be different function numbers which needs to be attached to context. Not used in Gen8.

ELEM_DESCRIPTOR - Element Descriptor Register

8	**Privileged Context / GGTT vs PPGTT mode** In Legacy Context: Defines the page tables to be used. This is how page walker come to know PPGTT vs GGTT selection for the entire context. In Advanced Context: Defines the privilege level for the context

Value	Name	Description
0h	**[Default]**	Use Global GTT (In Legacy Context) User Mode Context (In Advanced Context)
1h		Use Per-Process GTT (In Legacy Context) Supervisor Mode Context (In Advanced Context)

7:6	**Reserved**
5	**Deeper IA coherency Support** In Advanced Context: Defines the level of IA coherency

Value	Name	Description
0h	**[Default]**	IA coherency is provided at LLC level for all streams of GPU (i.e. gen7.5 like mode)
1h		IA coherency is provided at L3 level for EU data accesses of GPU

4	**A and D Support / 32 and 64b Address Support** In Legacy Context: Defines 32b vs 64b (48b canonical) addressing format In Advanced Context: Defines A/D bit support

Value	Name	Description
0h	**[Default]**	32b addressing format (In Legacy Context) A/D bit management in page tables is NOT supported (In Advanced Context)
1h		64b (48b canonical) addressing format (In Legacy Context) A/D bit management in page tables is supported (In Advanced Context)

3	**Context Type: Legacy vs Advanced** Defines the context type. Note that: Bits [8:4] differs in functions when legacy vs advanced context modes are selected.

Value	Name	Description
0h	**[Default]**	Advanced Context: Defines the rest of the advanced capabilities (i.e. OS page table support, fault models...). Note that advanced context is not bounded to GPGPU.
1h		Legacy Context: Defines the context as legacy mode which is similar to prior generations of gen8.

2	**FR** Command Streamer Specific
1	**Scheduling Mode**

Value	Name	Description
0h	**[Default]**	Indicates execlist mode of scheduling.
1h		Indicates Ring Buffer mode of scheduling.

ELEM_DESCRIPTOR - Element Descriptor Register		
	0	**Valid** Indicates that element descriptor is valid. If GAM is programmed with an invalid descriptor, it will continue but flag an error.

EMRR Mask LSB

EMRRMASK_LSB - EMRR Mask LSB			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	09208h		
EMRR Mask Value			
DWord	**Bit**	**Description**	
0	31:12	**EMRR_MASK_LSB**	
		Access:	RO
		EMRR MASK VALUE.	
	11	**EMRR ENABLE**	
		Access:	RO
		EMRR Enable.	
	10	**EMRR LOCK**	
		Access:	RO
		EMRR LOCK bit.	
	9:0	**Spares**	
		Access:	RO

EMRR Mask MSB

EMRRMASK_MSB - EMRR Mask MSB			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0920Ch		
EMRR Mask Value			
DWord	**Bit**	**Description**	
0	31:7	**Spares**	
		Access:	RO
	6:0	**EMRR_MASK_MSB**	
		Access:	RO
		EMRR MASK VALUE.	

Error Identity Register

EIR - Error Identity Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	r/w
Size (in bits):	32

Address:	020B0h-020B3h
Name:	Error Identity Register
ShortName:	EIR_RCSUNIT

Address:	120B0h-120B3h
Name:	Error Identity Register
ShortName:	EIR_VCSUNIT0

Address:	1A0B0h-1A0B3h
Name:	Error Identity Register
ShortName:	EIR_VECSUNIT

Address:	1C0B0h-1C0B3h
Name:	Error Identity Register
ShortName:	EIR_VCSUNIT1

Address:	220B0h-220B3h
Name:	Error Identity Register
ShortName:	EIR_BCSUNIT

The EIR register contains the persistent values of Hardware-Detected Error Condition bits. Any bit set in this register will cause the Master Error bit in the ISR to be set. The EIR register is also used by software to clear detected errors (by writing a 1 to the appropriate bit(s)), except for the unrecoverable bits described.)

Restriction
Restriction https://vthsd.iind.intel.com/hsd/gen9lp/bug_de/default.aspx?bug_de_id=2131892 : EIR register contents are not power or render context save/restored. EIR register contents of an engine will get lost when the corresponding graphics engine (Render, Video, Vidoe Enhancement, Blitter) is power down.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask

EIR - Error Identity Register

	15:0	**Error Identity Bits** Format: Array of Error condition bits See the table titled Hardware-Detected Error Bits. This register contains the persistent values of ESR error status bits that are unmasked via the EMR register. (See Table Table 3-3. Hardware-Detected Error Bits). The logical OR of all (defined) bits in this register is reported in the Master Error bit of the Interrupt Status Register. In order to clear an error condition, software must first clear the error by writing a 1 to the appropriate bit(s) in this field. If required, software should then proceed to clear the Master Error bit of the IIR. Reserved bits are RO.

Value	Name
1h	Error occurred

Programming Notes
Writing a 1 to a set bit will cause that error condition to be cleared. However, neither the Page Table Error bit (Bit 4) nor the Instruction Error bit (Bit 0) can be cleared except by reset (i.e., it is a fatal error).

Error Mask Register

EMR - Error Mask Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x000000FF
Access:	R/W
Size (in bits):	32

Address:	020B4h-020B7h
Name:	Error Mask Register
ShortName:	EMR_RCSUNIT

Address:	120B4h-120B7h
Name:	Error Mask Register
ShortName:	EMR_VCSUNIT0

Address:	1A0B4h-1A0B7h
Name:	Error Mask Register
ShortName:	EMR_VECSUNIT

Address:	1C0B4h-1C0B7h
Name:	Error Mask Register
ShortName:	EMR_VCSUNIT1

Address:	220B4h-220B7h
Name:	Error Mask Register
ShortName:	EMR_BCSUNIT

The EMR register is used by software to control which Error Status Register bits are masked or unmasked. Unmasked bits will be reported in the EIR, thus setting the Master Error ISR bit and possibly triggering a CPU interrupt, and will persist in the EIR until cleared by software. Masked bits will not be reported in the EIR and therefore cannot generate Master Error conditions or CPU interrupts. Reserved bits are RO.

Workaround	Source
Workaround https://vthsd.iind.intel.com/hsd/gen9lp/default.aspx#bug_de/default.aspx?bug_de_id=2132899 : “Command Privilege Violation Error” (bit2) is not dependable and must not be unmasked.	CommandStreamer

DWord	Bit	Description
0	31:8	**Reserved** Format: Must Be One **Programming Notes** These bits are not implemented in HW and must be set to '1'

EMR - Error Mask Register

	7:0	**Error Mask Bits** Format: Array of error condition mask bits See the table titled Hardware-Detected Error Bits. This register contains a bit mask that selects which error condition bits (from the ESR) are reported in the EIR.

Value	Name	Description
FFh	**[Default]**	
0h	Not Masked	Will be reported in the EIR
1h	Masked	Will not be reported in the EIR

Error Reporting Register

ERR - Error Reporting Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	0B42Ch

DWord	Bit	Description
0	31:5	**Reserved** Access: RO Reserved.
	4	**First Content Buffer Ready 0** Access: R/W First Content Buffer Ready 0 (FRSNTBFR0). First Content Buffer Ready: This bit gets set by the HW when the buffer is completely filled up and cleared by the driver when the contents of this buffer are copied out of memory. Is set by lpfc_lpconf_buffer0_ready (pulse). lpconf_lpfc_buffer0_ready (static signal to lpfc).
	3	**Second Buffer ready slice 0** Access: R/W Second Content Buffer Ready slice 0 (SCNBFR0). Second Content Buffer Ready: This bit gets set by the HW when the buffer is completely filled up and cleared by the driver when the contents of this buffer are copied out of memory. Is set by lpfc_lpconf_buffer1_ready (pulse). lpconf_lpfc_buffer1_ready (static signal to lpfc).
	2	**Write Expire Error Slice 0** Access: R/W Write Expired Error slice 0 (WEERR0). Write Expired Error: If DMA controller could not get a chance to push the write of 64Bytes to LTISEQ and data gets clobbered with the new expiration of the save timer, this error bit is set to indicate something went wrong. Signal -lpfc_lpconf_wrexp_error.
	1	**Buffer full Error Slice 0** Access: R/W Buffer full Error Slice 0 (BFFLERR0). Set by lpfc_lpconf_error_buffer_full. When all buffers are full lpfc sets this bit or if only 1 buffer is enabled then lpfc sets this bit when the buffer is full.
	0	**Reserved** Access: RO Reserved.

Error Status Register

ESR - Error Status Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	020B8h-020BBh
Name:	Error Status Register
ShortName:	ESR_RCSUNIT
Address:	120B8h-120BBh
Name:	Error Status Register
ShortName:	ESR_VCSUNIT0
Address:	1A0B8h-1A0BBh
Name:	Error Status Register
ShortName:	ESR_VECSUNIT
Address:	1C0B8h-1C0BBh
Name:	Error Status Register
ShortName:	ESR_VCSUNIT1
Address:	220B8h-220BBh
Name:	Error Status Register
ShortName:	ESR_BCSUNIT

The ESR register contains the current values of all Hardware-Detected Error condition bits (these are all by definition persistent). The EMR register selects which of these error conditions are reported in the persistent EIR (i.e., set bits must be cleared by software) and thereby causing a Master Error interrupt condition to be reported in the ISR.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Error Status Bits** Format: Array of error condition bits See the table titled Hardware-Detected Error Bits. This register contains the non-persistent values of all hardware-detected error condition bits. Value: 1h — Name: Error Condition Detected

EU_STALL PER SUBSLICE

EUMETRICS_EVENT0 - EU_STALL PER SUBSLICE		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00D8Ch	
This register mirrors an accumulating count for EU Metric Event0. It is enabled by configuration bits in GPMunit and SPMunits. Note that count is never cleared and delta should be calculated by sampling the initial register value at the start and subtracting that value off from the final sample value.		
DWord	**Bit**	**Description**
0	31:0	**EU Metric Event Count** Access: RO

EU Mask Programming

TD_PM_MODE_EUCOUNT - EU Mask Programming

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	WO
Size (in bits):	32
Address:	0E4F8h
Name:	EU Mask Programming Slice 0
ShortName:	TD_PM_MODE_EUCOUNT_S0
Valid Projects:	
Address:	0E5F8h
Name:	EU Mask Programming Slice 1
ShortName:	TD_PM_MODE_EUCOUNT_S1
Valid Projects:	
Address:	0E6F8h
Name:	EU Mask Programming Slice 2
ShortName:	TD_PM_MODE_EUCOUNT_S2
Valid Projects:	

DWord	Bit	Description
0	31	**SubSlice 3 EU 7 Enable** Format: Enable Value / Name: 0 – Enabled **[Default]** 1 – Disabled
	30	**SubSlice 3 EU 6 Enable** Format: Enable Value / Name: 0 – Enabled **[Default]** 1 – Disabled

TD_PM_MODE_EUCOUNT - EU Mask Programming

	29	**SubSlice 3 EU 5 Enable** Format: Enable Value: 0 — Enabled **[Default]**; 1 — Disabled
	28	**SubSlice 3 EU 4 Enable** Format: Enable Value: 0 — Enabled **[Default]**; 1 — Disabled
	27	**SubSlice 3 EU 3 Enable** Format: Enable Value: 0 — Enabled **[Default]**; 1 — Disabled
	26	**SubSlice 3 EU 2 Enable** Format: Enable Value: 0 — Enabled **[Default]**; 1 — Disabled
	25	**SubSlice 3 EU 1 Enable** Format: Enable Value: 0 — Enabled **[Default]**; 1 — Disabled
	24	**SubSlice 3 EU 0 Enable** Format: Enable Value: 0 — Enabled **[Default]**; 1 — Disabled

TD_PM_MODE_EUCOUNT - EU Mask Programming

	23	**SubSlice 2 EU 7 Enable** Format: Enable **Value** / **Name** 0 — Enabled **[Default]** 1 — Disabled
	22	**SubSlice 2 EU 6 Enable** Format: Enable **Value** / **Name** 0 — Enabled **[Default]** 1 — Disabled
	21	**SubSlice 2 EU 5 Enable** Format: Enable **Value** / **Name** 0 — Enabled **[Default]** 1 — Disabled
	20	**SubSlice 2 EU 4 Enable** Format: Enable **Value** / **Name** 0 — Enabled **[Default]** 1 — Disabled
	19	**SubSlice 2 EU 3 Enable** Format: Enable **Value** / **Name** 0 — Enabled **[Default]** 1 — Disabled
	18	**SubSlice 2 EU 2 Enable** Format: Enable **Value** / **Name** 0 — Enabled **[Default]** 1 — Disabled

TD_PM_MODE_EUCOUNT - EU Mask Programming

	17	**SubSlice 2 EU 1 Enable** Format: Enable Value: 0 — Enabled **[Default]**; 1 — Disabled
	16	**SubSlice 2 EU 0 Enable** Format: Enable Value: 0 — Enabled **[Default]**; 1 — Disabled
	15	**SubSlice 1 EU 7 Enable** Format: Enable Value: 0 — Enabled **[Default]**; 1 — Disabled
	14	**SubSlice 1 EU 6 Enable** Format: Enable Value: 0 — Enabled **[Default]**; 1 — Disabled
	13	**SubSlice 1 EU 5 Enable** Format: Enable Value: 0 — Enabled **[Default]**; 1 — Disabled
	12	**SubSlice 1 EU 4 Enable** Format: Enable Value: 0 — Enabled **[Default]**; 1 — Disabled

TD_PM_MODE_EUCOUNT - EU Mask Programming

	11	**SubSlice 1 EU 3 Enable** Format: Enable Value / Name 0 Enabled **[Default]** 1 Disabled
	10	**SubSlice 1 EU 2 Enable** Format: Enable Value / Name 0 Enabled **[Default]** 1 Disabled
	9	**SubSlice 1 EU 1 Enable** Format: Enable Value / Name 0 Enabled **[Default]** 1 Disabled
	8	**SubSlice 1 EU 0 Enable** Format: Enable Value / Name 0 Enabled **[Default]** 1 Disabled
	7	**SubSlice 0 EU 7 Enable** Format: Enable Value / Name 0 Enabled **[Default]** 1 Disabled
	6	**SubSlice 0 EU 6 Enable** Format: Enable Value / Name 0 Enabled **[Default]** 1 Disabled

TD_PM_MODE_EUCOUNT - EU Mask Programming

	5	**SubSlice 0 EU 5 Enable** Format: Enable Value: 0 — Enabled **[Default]**; 1 — Disabled
	4	**SubSlice 0 EU 4 Enable** Format: Enable Value: 0 — Enabled **[Default]**; 1 — Disabled
	3	**SubSlice 0 EU 3 Enable** Format: Enable Value: 0 — Enabled **[Default]**; 1 — Disabled
	2	**SubSlice 0 EU 2 Enable** Format: Enable Value: 0 — Enabled **[Default]**; 1 — Disabled
	1	**SubSlice 0 EU 1 Enable** Format: Enable Value: 0 — Enabled **[Default]**; 1 — Disabled
	0	**SubSlice 0 EU 0 Enable** Format: Enable Value: 0 — Enabled **[Default]**; 1 — Disabled

EU NOT IDLE PER SUBSLICE

EUMETRICS_EVENT4 - EU NOT IDLE PER SUBSLICE		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00D9Ch	
This register mirrors an accumulating count for EU Metric Event4. It is enabled by configuration bits in GPMunit and SPMunits. Note that count is never cleared and delta should be calculated by sampling the initial register value at the start and subtracting that value off from the final sample value.		
DWord	**Bit**	**Description**
0	31:0	**EU Metric Event Count** Access: RO

EU PAIR 0 PGFET control register with lock

PFETCTL - EU PAIR 0 PGFET control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0001000A
Size (in bits):	32
Address:	24608h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of EU PAIR 0 PGFETCTL register are R/W 1 = All bits of EU PAIR 0 PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:21	**Reserved** Access: RO Reserved
	20	**Reserved**
	19	**Reserved**
	18:16	**Delay from enabling secondary PFETs to power good.** Default Value: 001b Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 320ns 3'b100: 640ns 3'b101: 1280ns 3'b110: 2560ns 3'b111: 5120ns
	15:13	**Time period last primay pfet strobe to secondary pfet strobe** Access: R/W Lock Time period last primay pfet strobe to secondary pfet strobe 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)

PFETCTL - EU PAIR 0 PGFET control register with lock

	12:10	**Time period b/w two adjacent strobes** Access: R/W Lock Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	9:7	**FET setup margin from enable to strobe** Access: R/W Lock Setup margin in design before sampling enable event at the first pre-charge sequencer/shift register flop 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	6:0	**Number of flops to enable primary FETs** Default Value: 0001010b Access: R/W Lock Number of flops to enable primary FETs. For a setting of N there will be N+1 total strobes generated 7'b0000000: 10 Flops to be strobed 7'b0000001: 11 Flops to be strobed 7'b0000010: 12 Flops to be strobed 7'b0001111: 26 Flops to be strobed

EU PAIR 0 Power Context Save request

PGCTXREQ - EU PAIR 0 Power Context Save request

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	24604h

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO Reserved
	9	**Power context save request** Access: R/W Set Power Context Save Request 1'b0 : Power context save is not being requested <default> 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

EU PAIR 0 Power Down FSM control register with lock

POWERDNFSMCTL - EU PAIR 0 Power Down FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000088
Size (in bits):	32
Address:	24610h

DWord	Bit	Description
0	31	**power down control Lock** Access: R/W Lock 0 = Bits of EU PAIR 0 POWERDNFSMCTL register are R/W 1 = All bits of EU PAIR 0 POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Reserved
	12	**Leave firewall disabled** Access: R/W Lock When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e dont firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e dont assert reset, but complete logical flow

POWERDNFSMCTL - EU PAIR 0 Power Down FSM control register with lock

	10	**Leave CLKs ON** Access: R/W Lock When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e dont clock gate, but complete logical flow
	9	**Leave FET On** Access: R/W Lock When This bit is set SPC will not turn off the PFET eventhough it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e dont power off pfet, but complete logical flow Programming note : This bit should be programmed before the powerup sequence is initiated for SSM
	8:6	**Power Down state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks
	5:3	**Power Down state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON

POWERDNFSMCTL - EU PAIR 0 Power Down FSM control register with lock

	2:0	**Power Down state 1** Default Value: 000b Access: R/W Lock This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Assert Reset

EU PAIR 0 Power Gate Control Request

PGCTLREQ - EU PAIR 0 Power Gate Control Request

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	24600h

Clock Gating Messages Register

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Reserved
	1	**CLK RST FWE Request** Access: R/W EU PAIR 0 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Reserved**

EU PAIR 0 Power on FSM control register with lock

POWERUPFSMCTL - EU PAIR 0 Power on FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000088
Size (in bits):	32
Address:	2460Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock 0 = Bits of EU PAIR 0 POWERUPFSMCTL register are R/W 1 = All bits of EU PAIR 0 POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Reserved
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Firewall OFF

POWERUPFSMCTL - EU PAIR 0 Power on FSM control register with lock

	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

EU PAIR 1 PGFET control register with lock

PFETCTL - EU PAIR 1 PGFET control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0001000A
Size (in bits):	32
Address:	24688h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of EU PAIR 1 PGFETCTL register are R/W 1 = All bits of EU PAIR 1 PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:21	**Reserved** Access: RO Reserved
	20	**Reserved**
	19	**Reserved**
	18:16	**Delay from enabling secondary PFETs to power good.** Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 320ns 3'b100: 640ns 3'b101: 1280ns 3'b110: 2560ns 3'b111: 5120ns **Value** / **Name**: 001b / **[Default]**
	15:13	**Time period last primay pfet strobe to secondary pfet strobe** Access: R/W Lock Time period last primay pfet strobe to secondary pfet strobe 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	12:10	**Time period b/w two adjacent strobes**

PFETCTL - EU PAIR 1 PGFET control register with lock

		Access: R/W Lock Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	9:7	**FET setup margin from enable to strobe** Access: R/W Lock Setup margin in design before sampling enable event at the first pre-charge sequencer/shift register flop 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	6:0	**Number of flops to enable primary FETs** Default Value: 0001010b Access: R/W Lock Number of flops to enable primary FETs. For a setting of N there will be N+1 total strobes generated 7'b0000000: 10 Flops to be strobed 7'b0000001: 11 Flops to be strobed 7'b0000010: 12 Flops to be strobed 7'b0001111: 26 Flops to be strobed

EU PAIR 1 Power Context Save request

PGCTXREQ - EU PAIR 1 Power Context Save request

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	24684h

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO Reserved
	9	**Power context save request** Access: R/W Set Power Context Save Request 1'b0 : Power context save is not being requested <default> 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

EU PAIR 1 Power Down FSM control register with lock

POWERDNFSMCTL - EU PAIR 1 Power Down FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000088
Size (in bits):	32
Address:	24690h

DWord	Bit	Description
0	31	**power down control Lock** Access: R/W Lock 0 = Bits of EU PAIR 1 POWERDNFSMCTL register are R/W 1 = All bits of EU PAIR 1 POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Reserved
	12	**Leave firewall disabled** Access: R/W Lock When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e dont firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e dont assert reset, but complete logical flow
	10	**Leave CLKs ON** Access: R/W Lock When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e dont clock gate, but complete logical flow

POWERDNFSMCTL - EU PAIR 1 Power Down FSM control register with lock

	9	**Leave FET On** Access: R/W Lock When This bit is set SPC will not turn off the PFET eventhough it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e dont power off pfet, but complete logical flow Programming note : This bit should be programmed before the powerup sequence is initiated for EUP1
	8:6	**Power Down state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks
	5:3	**Power Down state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON
	2:0	**Power Down state 1** Default Value: 000b Access: R/W Lock This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Assert Reset

EU PAIR 1 Power Gate Control Request

PGCTLREQ - EU PAIR 1 Power Gate Control Request

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	24680h

Clock Gating Messages Register

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Reserved
	1	**CLK RST FWE Request** Access: R/W EU PAIR 1 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Reserved**

EU PAIR 1 Power on FSM control register with lock

POWERUPFSMCTL - EU PAIR 1 Power on FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000088
Size (in bits):	32
Address:	2468Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock 0 = Bits of EU PAIR 1 POWERUPFSMCTL register are R/W 1 = All bits of EU PAIR 1 POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Reserved
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Firewall OFF

POWERUPFSMCTL - EU PAIR 1 Power on FSM control register with lock

	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

EU PAIR 2 PGFET control register with lock

PFETCTL - EU PAIR 2 PGFET control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0001000A
Size (in bits):	32
Address:	24708h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of EU PAIR 2 PGFETCTL register are R/W 1 = All bits of EU PAIR 2 PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:21	**Reserved** Access: RO Reserved
	20	**Reserved**
	19	**Reserved**
	18:16	**Delay from enabling secondary PFETs to power good.** Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 320ns 3'b100: 640ns 3'b101: 1280ns 3'b110: 2560ns 3'b111: 5120ns Value: 001b — Name: **[Default]**
	15:13	**Time period last primay pfet strobe to secondary pfet strobe** Access: R/W Lock Time period last primay pfet strobe to secondary pfet strobe 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	12:10	**Time period b/w two adjacent strobes**

PFETCTL - EU PAIR 2 PGFET control register with lock

		Access: R/W Lock Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	9:7	**FET setup margin from enable to strobe** Access: R/W Lock Setup margin in design before sampling enable event at the first pre-charge sequencer/shift register flop 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	6:0	**Number of flops to enable primary FETs** Default Value: 0001010b Access: R/W Lock Number of flops to enable primary FETs. For a setting of N there will be N+1 total strobes generated 7'b0000000: 10 Flops to be strobed 7'b0000001: 11 Flops to be strobed 7'b0000010: 12 Flops to be strobed 7'b0001111: 26 Flops to be strobed

EU PAIR 2 Power Context Save request

PGCTXREQ - EU PAIR 2 Power Context Save request

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	24704h

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO Reserved
	9	**Power context save request** Access: R/W Set Power Context Save Request 1'b0 : Power context save is not being requested <default> 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

EU PAIR 2 Power Down FSM control register with lock

POWERDNFSMCTL - EU PAIR 2 Power Down FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000088
Size (in bits):	32
Address:	24710h

DWord	Bit	Description
0	31	**power down control Lock** Access: R/W Lock 0 = Bits of EU PAIR 2 POWERDNFSMCTL register are R/W 1 = All bits of EU PAIR 2 POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Reserved
	12	**Leave firewall disabled** Access: R/W Lock When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e dont firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e dont assert reset, but complete logical flow
	10	**Leave CLKs ON** Access: R/W Lock When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e dont clock gate, but complete logical flow

POWERDNFSMCTL - EU PAIR 2 Power Down FSM control register with lock

	9	**Leave FET On** Access: R/W Lock When This bit is set SPC will not turn off the PFET eventhough it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e dont power off pfet, but complete logical flow Programming note : This bit should be programmed before the powerup sequence is initiated for EUP2
	8:6	**Power Down state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks
	5:3	**Power Down state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON
	2:0	**Power Down state 1** Default Value: 000b Access: R/W Lock This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Assert Reset

EU PAIR 2 Power Gate Control Request

PGCTLREQ - EU PAIR 2 Power Gate Control Request		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	24700h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Reserved
	1	**CLK RST FWE Request** Access: R/W EU PAIR 2 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Reserved**

EU PAIR 2 Power on FSM control register with lock

POWERUPFSMCTL - EU PAIR 2 Power on FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000088
Size (in bits):	32
Address:	2470Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock 0 = Bits of EU PAIR 2 POWERUPFSMCTL register are R/W 1 = All bits of EU PAIR 2 POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Reserved
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Firewall OFF

POWERUPFSMCTL - EU PAIR 2 Power on FSM control register with lock

	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

EU PAIR 3 PGFET control register with lock

PFETCTL - EU PAIR 3 PGFET control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0001000A
Size (in bits):	32
Address:	24788h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of EU PAIR 3 PGFETCTL register are R/W 1 = All bits of EU PAIR 3 PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:21	**Reserved** Access: RO Reserved
	20	**Reserved**
	19	**Reserved**
	18:16	**Delay from enabling secondary PFETs to power good.** Default Value: 001b Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 320ns 3'b100: 640ns 3'b101: 1280ns 3'b110: 2560ns 3'b111: 5120ns
	15:13	**Time period last primay pfet strobe to secondary pfet strobe** Access: R/W Lock Time period last primay pfet strobe to secondary pfet strobe 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)

PFETCTL - EU PAIR 3 PGFET control register with lock

	12:10	**Time period b/w two adjacent strobes** Access: R/W Lock Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	9:7	**FET setup margin from enable to strobe** Access: R/W Lock Setup margin in design before sampling enable event at the first pre-charge sequencer/shift register flop 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	6:0	**Number of flops to enable primary FETs** Default Value: 0001010b Access: R/W Lock Number of flops to enable primary FETs. For a setting of N there will be N+1 total strobes generated 7'b0000000: 10 Flops to be strobed 7'b0000001: 11 Flops to be strobed 7'b0000010: 12 Flops to be strobed 7'b0001111: 26 Flops to be strobed

EU PAIR 3 Power Context Save request

PGCTXREQ - EU PAIR 3 Power Context Save request

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	24784h

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO Reserved
	9	**Power context save request** Access: R/W Set Power Context Save Request 1'b0 : Power context save is not being requested <default> 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

EU PAIR 3 Power Down FSM control register with lock

POWERDNFSMCTL - EU PAIR 3 Power Down FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000088
Size (in bits):	32
Address:	24790h

DWord	Bit	Description
0	31	**power down control Lock** Access: R/W Lock 0 = Bits of EU PAIR 3 POWERDNFSMCTL register are R/W 1 = All bits of EU PAIR 3 POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Reserved
	12	**Leave firewall disabled** Access: R/W Lock When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e dont firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e dont assert reset, but complete logical flow

POWERDNFSMCTL - EU PAIR 3 Power Down FSM control register with lock

	10	**Leave CLKs ON** Access: R/W Lock When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e dont clock gate, but complete logical flow
	9	**Leave FET On** Access: R/W Lock When This bit is set SPC will not turn off the PFET eventhough it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e dont power off pfet, but complete logical flow Programming note : This bit should be programmed before the powerup sequence is initiated for EUP3
	8:6	**Power Down state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks
	5:3	**Power Down state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON

POWERDNFSMCTL - EU PAIR 3 Power Down FSM control register with lock

	2:0	**Power Down state 1** Default Value: 000b Access: R/W Lock This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Assert Reset

EU PAIR 3 Power Gate Control Request

PGCTLREQ - EU PAIR 3 Power Gate Control Request		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	24780h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Reserved
	1	**CLK RST FWE Request** Access: R/W EU PAIR 3 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Reserved**

EU PAIR 3 Power on FSM control register with lock

POWERUPFSMCTL - EU PAIR 3 Power on FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000088
Size (in bits):	32
Address:	2478Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock 0 = Bits of EU PAIR 3 POWERUPFSMCTL register are R/W 1 = All bits of EU PAIR 3 POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Reserved
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Firewall OFF

POWERUPFSMCTL - EU PAIR 3 Power on FSM control register with lock

	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

Event selection and base counters

LPFCREG2 - Event selection and base counters		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B00Ch	
DWord	**Bit**	**Description**
0	31:24	**Counter 7 client** Access: R/W lncf_lpfc_cnt7_client[7:0]. Client Encoding (hex): GAFS Rd 00 GAFS Wr 01 HDC0 Data Rd 02 HDC0 Const Rd 03 HDC0 URB Rd 04 HDC0 Data Wr 05 HDC0 URB Wr 06 HDC1 Data Rd 07 HDC1 Const Rd 08 HDC1 URB Rd 09 HDC1 Data Wr 0A HDC1 URB Wr 0B TDL0 Rd 0C TDL1 Rd 0D Tex0 Rd 0E Tex1 Rd 0F Tex2 Rd (reserved) 10 Tex3 Rd (reserved) 11 SBE Rd 12 IC0 Rd 13 IC1 Rd 14 SARB Rd 15 Aggregated Tex 16 SLM0 Rd 17 SLM1 Rd 18 SLM0 Wr 19 SLM1 Wr 1A SLM0 Atomics 1B SLM1 Atomics 1C Reserved 1D Reserved 1E Reserved 1F

LPFCREG2 - Event selection and base counters

		FF Stalls 20 HDC Stalls 21 TDL Stalls 22 Texture Stalls 23 IC Stalls 24 SBE Stalls 25 SLM Stalls 26 Bank0 Total Hits 40 Bank0 Total Cycles 41 Bank0 Total Rds 42 Bank0 Total Wrs 43 Bank0 FF Rds 44 Bank0 FF Wrs 45 Bank0 DC Rds 46 Bank0 DC Wrs 47 Bank0 DC Hits 48 rsvd 49 Bank0 Tex Rds 4A Bank0 Tex Hits 4B Bank0 IC Rds 4C Bank0 IC Hits 4D Reserved 4E Reserved 4F Bank1 Events 50-5F (except 59-reserved) Bank2 Events 60-6F(except 69-reserved) Bank3 Events 70-7F(except 79-reserved) MSC Rd 80 MSC Wr 81 STC Rd 82 STC Wr 83 Hiz Rd 84 Hiz Wr 85 RCZ Rd 86 RCZ Wr 87 RCC Rd 88 RCC Wr 89 LTCD0 Err Corr EE LTCD1 Err Corr EF LTCD2 Err Corr F0 LTCD3 Err Corr F1 LTCD0 Err UnCorr F2 LTCD1 Err UnCorr F3 LTCD2 Err UnCorr F4 LTCD3 Err UnCorr F5 Counter#7 Client Selection: This field controls which client's request stream is observed in counter#7.

LPFCREG2 - Event selection and base counters		
	23:16	**Counter 6 client** Access: R/W lncf_lpfc_cnt6_client[7:0]. Counter#6 Client Selection: This field controls which client's request stream is observed in counter#6.
	15:8	**Counter 5 client** Access: R/W lncf_lpfc_cnt5_client[7:0]. Counter#5 Client Selection: This field controls which client's request stream is observed in counter#5.
	7:0	**Counter 4 client** Access: R/W lncf_lpfc_cnt4_client[7:0]. Counter#4 Client Selection: This field controls which client's request stream is observed in counter#4.

Event Selection and Base Counters1

LPFCREG1 - Event Selection and Base Counters1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B010h	
DWord	**Bit**	**Description**
0	31:24	**Counter 3 client** Access: R/W Incf_lpfc_cnt3_client[7:0]. Counter#3 Client Selection: This field controls which client's request stream is observed in counter#3.
	23:16	**Counter 2 client** Access: R/W Incf_lpfc_cnt2_client[7:0]. Counter#2 Client Selection: This field controls which client's request stream is observed in counter#2.
	15:8	**Counter 1 Client** Access: R/W Incf_lpfc_cnt1_client[7:0]. Counter#1 Client Selection: This field controls which client's request stream is observed in counter#1.
	7:0	**Counter0 Client** Access: R/W Incf_lpfc_cnt0_client[7:0]. Counter#0 Client Selection: This field controls which client's request stream is observed in counter#0.

Execlist 0 Contents

EXECLIST0_CONTENTS - Execlist 0 Contents	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000, 0x00000000, 0x00000000, 0x00000000
Access:	R/W
Size (in bits):	128
Trusted Type:	1
Address:	02250h-0225Fh
Name:	Execlist 0 Contents
ShortName:	EXECLIST0_CONTENTS_RCSUNIT
Address:	12250h-1225Fh
Name:	Execlist 0 Contents
ShortName:	EXECLIST0_CONTENTS_VCSUNIT0
Address:	1A250h-1A25Fh
Name:	Execlist 0 Contents
ShortName:	EXECLIST0_CONTENTS_VECSUNIT
Address:	1C250h-1C25Fh
Name:	Execlist 0 Contents
ShortName:	EXECLIST0_CONTENTS_VCSUNIT1
Address:	22250h-2225Fh
Name:	Execlist 0 Contents
ShortName:	EXECLIST0_CONTENTS_BCSUNIT

Contents of the Execlist 0 in HW.

DWord	Bit	Description
0	31:0	**Element 0 Low DWord** Format: ContextDescriptorHigh
1	31:0	**Element 0 High DWord** Format: ContextDescriptorLow
2	31:0	**Element 1 Low DWord** Format: ContextDescriptorHigh
3	31:0	**Element 1 High DWord** Format: ContextDescriptorLow

Execlist 1 Contents

EXECLIST1_CONTENTS - Execlist 1 Contents	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000, 0x00000000, 0x00000000, 0x00000000
Access:	R/W
Size (in bits):	128
Trusted Type:	1
Address:	02260h-0226Fh
Name:	Execlist 1 Contents
ShortName:	EXECLIST1_CONTENTS_RCSUNIT
Address:	12260h-1226Fh
Name:	Execlist 1 Contents
ShortName:	EXECLIST1_CONTENTS_VCSUNIT0
Address:	1A260h-1A26Fh
Name:	Execlist 1 Contents
ShortName:	EXECLIST1_CONTENTS_VECSUNIT
Address:	1C260h-1C26Fh
Name:	Execlist 1 Contents
ShortName:	EXECLIST1_CONTENTS_VCSUNIT1
Address:	22260h-2226Fh
Name:	Execlist 1 Contents
ShortName:	EXECLIST1_CONTENTS_BCSUNIT

Contents of the Execlist 1 in HW.

DWord	Bit	Description
0	31:0	**Element 0 Low DWord** Format: ContextDescriptorHigh
1	31:0	**Element 0 High DWord** Format: ContextDescriptorLow
2	31:0	**Element 1 Low DWord** Format: ContextDescriptorHigh
3	31:0	**Element 1 High DWord** Format: ContextDescriptorLow

Execlist Status

EXECLIST_STATUS - Execlist Status	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000001, 0x00000000
Access:	RO
Size (in bits):	64
Address:	02234h-0223Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_RCSUNIT
Address:	12234h-1223Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_VCSUNIT0
Address:	1A234h-1A23Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_VECSUNIT
Address:	1C234h-1C23Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_VCSUNIT1
Address:	22234h-2223Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_BCSUNIT

This register contains the pointers and full indicator for the Execlist Queue and the context ID of the currently running context. DefaultValue = UUUU UUU1h (4:0 default to 00001b, others UNDEFINED).

DWord	Bit	Description
0	63:32	**Current Context ID** Format: U32 Contains the context ID of the currently running context.
	31:30	**Reserved** Format: MBZ
	29:28	**Reserved** Format: MBZ
	27	**Reserved** Format: MBZ
	26:19	**Reserved** Format: MBZ

EXECLIST_STATUS - Execlist Status

	18	**Reserved**
	17	**Reserved**
	16	**Arbitration Enable** Format: U1 This field reflects the Arbitration Flag set by the MI_ARB_ON_OFF command in Command Streamer.
	15:14	**Current Active Element Status** Format: U2 Points at the element being executed in current Execlist (if there is one). 00b: No Active Element being executed 01b: Element0 of current execlist being executed 10b: Element1 of current execlist being executed 11b: Reserved
	13:5	**Last Context Switch Reason** Access: R/W Format: U9 This field contains the switch reason for the last context to switch away, as captured in the Context Status Dword, bits 8:0. **Programming Notes** This field should not written by SW.
	4	**Execlist 0 Valid** Format: Flag This bit is set when the first DW for this Execlist port 0 is written through the submission port, and will not be cleared till the CSB is updated and the command stream is switching to the next execution list. If no execution list is pending, the transition of this bit from one to zero guarentees there will be no preemption on the next submission. 0: Invalid **[Default]** 1: Valid

EXECLIST_STATUS - Execlist Status

3 — Execlist 1 Valid

Format:	Flag

This bit is set when the first DW for this Execlist port 1 is written through the submission port, and will not be cleared till the CSB is updated and the command stream is switching to the next execution list. If no execution list is pending, the transition of this bit from one to zero guarentees there will be no preemption on the next submission.

Value	Name
0	Invalid **[Default]**
1	Valid

2 — Execlist Queue Full

When [Execlist Write Pointer] and [Current Execlist Pointer] are equal, this bit differentiates between Queue Full and Queue Empty.

Value	Name	Description
0	Execlist Queue Empty **[Default]**	
1	Execlist Queue Full	There is a current and a pending execlist.

1 — Execlist Write Pointer

Format:	ExeclistContentsIndex

Determines which Execlist will be the next submitted to. When a new execlist is submitted, this pointer increments to point to the next execlist slot.

0 — Current Execlist Pointer

Default Value:	1h
Format:	ExeclistContentsIndex

Points at the currently executing Execlist (if there is one). This pointer advances when the first context of new execlist is restored.

Execlist Submit Port Register

EXECLIST_SUBMITPORT - Execlist Submit Port Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	WO
Size (in bits):	32
Address:	02230h-02233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_RCSUNIT
Address:	12230h-12233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VCSUNIT0
Address:	1A230h-1A233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VECSUNIT
Address:	1C230h-1C233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VCSUNIT1
Address:	22230h-22233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_BCSUNIT

SW should submit a new pending execlist to this register. The DWs of the context descriptors must be written in a specific order: Element 1 must be written first and then Element 0. For each Element, DW1 must be written first followed by DW0. Context descriptors for both the elements must be written even if only one context are being submitted. The valid bits of the unused context descriptors should be set to 0.

Order of DW Submission to the Execlist Port
Element 1, High Dword
Element 1, Low Dword
Element 0, High Dword
Element 0, Low Dword

If a execlist of only one element is being submitted, it must be submitted in Element 0. It is UNDEFINED to submit a execlist with the valid bit of Element 0 clear (an "empty" execlist). It is possible that one or all of the contexts submitted in a execlists are "empty"; that is, have head and tail pointers equal to each other indicating no commands to be run. All of the valid bits in the Execlist Element Status Registers for the "about to be submitted" execlist will be cleared when the first DW (DW1 of Element 1) is written to the submit port. Submission of the Element 0 Context Descriptor low Dword with the valid bit set is interpreted as a request to switch (as soon as possible) to the new execlist, i.e., a pre-emption request.
If a submitted Execlist's Element 0 Context Descriptor LRCA matches the LRCA of the currently executing context,

EXECLIST_SUBMITPORT - Execlist Submit Port Register

then the newly submitted execlist will become the currently executing execlist without any context switch and without any impact to the executing context except that it will re-sample the tail pointer from the context image. This is done in case more commands have been inserted into its ring buffer between the first execlist submission and the 2nd.

Programming Notes

SW must ensure the contexts submitted to the both the context descriptors in the execlist are different, i.e SW must not submit the same context descriptor to both the elements of the execlist.

DWord	Bit	Description
0	31:0	**Context Descriptor DW** Format: Context Descriptor See "Context Descriptor Format" for format. The element that this DW is submitted as and whether it is the high DW or the low DW is determined by order. This register must be written to 4 times in order to submit a execlist.

Execute Condition Code Register

EXCC - Execute Condition Code Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	r/w
Size (in bits):	32
Trusted Type:	1

Address:	02028h-0202Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_RCSUNIT

Address:	12028h-1202Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_VCSUNIT0

Address:	1A028h-1A02Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_VECSUNIT

Address:	1C028h-1C02Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_VCSUNIT1

Address:	22028h-2202Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_BCSUNIT

This register contains user defined and hardware generated conditions that are used by MI_WAIT_FOR_EVENT commands. An MI_WAIT_FOR_EVENT instruction excludes the executing ring from arbitration if the selected event evaluates to a 1, while instruction is discarded if the condition evaluates to a 0. Once excluded a ring is enabled into arbitration when the selected condition evaluates to a 0. This register also contains control for the invalidation of indirect state pointers on context restore.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask These bits serves as a write enable for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.
	15	**Reserved** Format: MBZ

EXCC - Execute Condition Code Register

	14	**Context Wait for V-blank on Pipe-C** Source: RenderCS, BlitterCS This field when set indicates the corresponding context has executed MI_WAIT_FOR_EVENT with "Display Pipe C Vertical Blank Wait Enable" set. This is an internal HW flag and should not be accessed by SW.
	13	**Context Wait for V-blank on Pipe-B** Source: RenderCS, BlitterCS This field when set indicates the corresponding context has executed MI_WAIT_FOR_EVENT with "Display Pipe B Vertical Blank Wait Enable" set. This is an internal HW flag and should not be accessed by SW.
	14:12	**Reserved** Source: VideoCS, VideoCS2, VideoEnhancementCS Format: MBZ
	12	**Context Wait for V-blank on Pipe-A** Source: RenderCS, BlitterCS This field when set indicates the corresponding context has executed MI_WAIT_FOR_EVENT with "Display Pipe A Vertical Blank Wait Enable" set. This is an internal HW flag and should not be accessed by SW.
	11:5	**Reserved** Format: MBZ
	4:0	**User Defined Condition Codes** Source: RenderCS The software may signal a Stream Semaphore by setting the Mask bit and Signal Bit together to match the bit field specified in a WAIT_FOR_EVENT (Semaphore).
	4:0	**Reserved** Source: BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS Format: MBZ

FAULT_TLB_RD_DATA0 Register

FAULT_TLB_RD_DATA0 - FAULT_TLB_RD_DATA0 Register		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B10h	
DWord	**Bit**	**Description**
0	31:0	**FAULT_TLB_READ_DATA0 Register** Default Value: 00000000h Access: RO Fault cycle Virtual address [43:12]

FAULT_TLB_RD_DATA1 Register

FAULT_TLB_RD_DATA1 - FAULT_TLB_RD_DATA1 Register		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B14h	
DWord	**Bit**	**Description**
0	31:0	**FAULT_TLB_READ_DATA1 Register** Default Value: 00000000h Access: RO Bit[31:5] Reserved Bit[4] Cycle GTT SEL (1-GGTT Cycle, 0-PPGTT Cycle) Bit[3:0] Fault cycle Virtual address [47:44]

Fault Mode Control

FLTMODECTL - Fault Mode Control		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0404Ch	
DWord	**Bit**	**Description**
0	31:1	**Reserved** Default Value: 00000000000000000000000000000000b Access: RO
	0	**Fault Halt Enable Bit** Default Value: 0b Access: R/W When set, it would enable the Fault and Halt behavior for streamable clients. Page walker will no longer use Fault and Stream mode for any client, instead it will downgrade the fault treatment to fault and halt. This behavior is applicable to HDC/Sampler/I$ given they are the only page fault streamable interfaces. This bit is only applicable under advanced context when PFM is selected for Fault and Stream.

Fault Mode Control

FAULT_MODE_CONTROL - Fault Mode Control		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0404Ch	
DWord	**Bit**	**Description**
0	31:1	**Reserved** Format: MBZ
	0	**Fault and Halt Enable** Format: Enable When set, it would enable the Fault and Halt behavior for streamable clients. Page walker will no longer use Fault and Stream mode for any client, instead it will downgrade the fault treatment to Fault and Halt. This behavior is applicable to HDC/Sampler/I$ given they are the only page fault streamable interfaces. *This bit is only applicable under advanced context when PFM is selected for Fault and Stream.*

Fault Switch Out

FAULT_SO - Fault Switch Out		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04590h	
DWord	**Bit**	**Description**
0	31:0	**Fault Switch Out** Default Value: 00000000h Access: R/W

FBC_CFB_BASE

FBC_CFB_BASE

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	43200h-43203h
Name:	FBC Compressed Buffer Address
ShortName:	FBC_CFB_BASE
Valid Projects:	
Power:	PG1
Reset:	soft

Restriction

The contents of this register must not be changed while compression is enabled.

DWord	Bit	Description
0	31:28	**Reserved** Format: MBZ
	27:12	**CFB Offset Address** This register specifies bits 27:12 of the offset of the Compressed Frame Buffer from the base of stolen memory. **Programming Notes** The buffer must not overlap the top 8 MB of stolen memory. **Restriction** The buffer must be 4K byte aligned. The offset must be greater than 4K bytes, avoiding the first 4KB of stolen memory.
	11:0	**Reserved** Format: MBZ

FBC_CTL

FBC_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	43208h-4320Bh
Name:	FBC Control
ShortName:	FBC_CTL
Power:	PG1
Reset:	soft

Description

FBC is tied to Plane 1 A.

Programming Notes

Frame Buffer Compression is only supported with surfaces up to 4096 pixels x 4096 lines. FBC is optimized to work best with surfaces up to 4096 pixels x 2560 lines.

Restriction

The contents of this register must not be changed, except the enable bit, while compression is enabled. Frame Buffer Compression is only supported with 16bpp and 32bpp 8:8:8 RGB plane source pixel formats. It is not supported with any other format. The 16bpp format requires the compression ratio to be set to 2:1 or 4:1.

Frame Buffer Compression is not supported with interlaced fetch.
With plane 90/270 rotation, all frame buffer modifications will result in full frame invalidation and recompression. FBC should not be enabled with RGB 16bpp plane formats when plane 90/270 rotation is enabled.
Frame Buffer Compression is not supported when the plane width is smaller than 35 pixels.

DWord	Bit	Description
0	31	**Enable FBC** This bit is used to globally enable FBC function at the next Vertical Blank start. FBC should not be enabled when the pipe is disabled.

Value	Name
0b	Disable
1b	Enable

Workaround

If FBC is enabled with a linear surface, the surface stride programmed in the PLANE_STRIDE register must be multiple of 8 cache lines (512 bytes).

When FBC is enabled and the plane surface format is in linear, tile Y legacy or tile YF, the

FBC_CTL

		display register 4208Ch bit 13 must be set to 1b and bits 12:0 must be programmed with the compressed buffer stride value. The compressed buffer stride must be calculated using the following equation: Compressed buffer stride = ceiling [(at least plane width in pixels) / (32 * compression limit factor)] * 8 At least plane width = a value greater than or equal to the width of the plane. Software may choose to use a greater value in order to handle cases where the plane width is changing from frame to frame. Compression limit factor is either 1, 2 or 4 based on the Compression Limit field. If the limit is 2:1, the compression limit factor to be used is 2. Ceiling function rounds up any non-integer value to next greater number. Example ceiling [0.3] = 1, ceiling[2.1] = 3, ceiling[4.8] = 5, ceiling[4] = 4. **Restriction** The compressed buffer stride value programmed in the display register 4208Ch cannot be changed when FBC is enabled.
	30:29	**Reserved** Format: MBZ
	28	**CPU Fence Enable** Value / Name / Description 0b / No CPU Disp Buf / Display Buffer is not in a CPU fence. No modifications are allowed from CPU to the Display Buffer. 1b / CPU Disp Buf / Display Buffer exists in a CPU fence.
	27:25	**Reserved** Format: MBZ
	24:16	**Reserved**
	15	**Reserved**
	14:11	**Reserved** Format: MBZ
	10	**Reserved**
	9:8	**Reserved**

FBC_CTL

7:6 **Compression Limit**

This register sets a minimum limit on compression. This determines the maximum size of the compressed frame buffer. Display lines that do not meet the compression limit will not be compressed, so the best compression will be achieved with a 1:1 ratio.

Compression Ratio 1, Pixel Format 16 bpp - Not Supported
Compression Ratio 1, Pixel Format 32 bpp - Supported (CFB=FB)
Compression Ratio 1/2, Pixel Format 16 bpp - Supported (CFB=FB)
Compression Ratio 1/2, Pixel Format 32 bpp - Supported (CFB=1/2 FB)
Compression Ratio 1/4, Pixel Format 16 bpp - Supported (CFB=1/2 FB)
Compression Ratio 1/4, Pixel Format 32 bpp - Supported (CFB=1/4 FB)

FB = Frame Buffer Size
CFB = Compressed Frame Buffer Size

Value	Name	Description
00b	1:1	Compressed buffer is the same size as the uncompressed buffer.
01b	2:1	Compressed buffer is one half the size of the uncompressed buffer.
10b	4:1	Compressed buffer is one quarter the size of the uncompressed buffer.
11b	Reserved	Reserved

5:4 **Write Back Watermark**

The compressed data write back engine waits for this number of entries to be ready before writing the data out to memory.

Value	Name	Description
00b	4	4 entries
01b	8	8 entries
10b	16	16 entries
11b	32	32 entries

3:0 **CPU Fence Number**

Value	Name
0000b	Fence 0

Restriction
This field must be programmed to 0000b.

FBC_RT_BASE_ADDR_REGISTER

FBC_RT_BASE_ADDR_REGISTER - FBC_RT_BASE_ADDR_REGISTER

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	07020h

This Register is saved and restored as part of Context.

DWord	Bit	Description
0	31:12	**FBC RT Base Address** Access: R/W Format: PPGraphicsAddress[31:12] 4KB aligned Base Address as mapped in the PPGTT or in the GGTT for the render target. This base address must be the one that is either front buffer or the back-buffer (a flip target). It must be programmed before any draw call binding that render target base address.
	11:2	**Reserved** Access: R/W Format: PBC
	1	**FBC Front Buffer Target** Access: R/W Format: Enable

Value	Name	Description
0h	**[Default]**	FBC is targeting the Back Buffer for compression. This buffer can be cached in the MLC/LLC, so a GFDT flush is required before FBC can begin compression.
1h		FBC is targeting the Font Buffer for compression. This buffer cannot be cached in the MLC/LLC. FBC compression can begin after any RC flush.

	0	**PPGTT Render Target Base Address Valid for FBC** Access: R/W Format: Enable

Value	Name	Description
0h	**[Default]**	Base address in this register [31:12] is not valid and therefore FBC will not get any modifications from rendering.
1h		Base address in this register [31:12] is valid and HW needs to compare the current render target base address with this base address to provide modifications to FBC.

FBC_RT_BASE_ADDR_REGISTER_UPPER

FBC_RT_BASE_ADDR_REGISTER_UPPER - FBC_RT_BASE_ADDR_REGISTER_UPPER

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	07024h

This Register is saved and restored as part of Context.

DWord	Bit	Description
0	31:16	**Reserved** Access: R/W Format: PBC
	15:0	**FBC RT Base Address High** Access: R/W Format: BaseAddress[47:32] Must be set to modify corresponding data bit. Reads to this field returns zero. Upper 4KB aligned Base Address as mapped in the PPGTT or in the GGTT for the render target. This base address must be the one that is either front buffer or the back-buffer (a flip target). It can be only programmed once per context. **Programming Notes** It must be programmed before any draw call binding that render target base address.

Fence Control Register

MFCR - Fence Control Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00070000
Size (in bits):	32
Address:	09070h

Fence Control Register

DWord	Bit	Description
0	31	**Fuse Override Lock** Access: R/W Lock SW Fuse Override Lock Bit
	30:25	**ECORSVD** Access: R/W ECO purposes Reserved
	24:23	**GT VBOX DISABLE FUSE OVERRIDE** Access: R/W Lock S/W GT Vbox Disable Fuse Override Bits
	22	**Reserved**
	21:19	**GT SUBSLICE DISABLE FUSE OVERRIDE** Access: R/W Lock SW GT SubSlice Disable Fuse Override Bits
	18:16	**GT SLICE ENABLE FUSE OVERRIDE** Default Value: 111b Access: R/W Lock SW GT Slice Enable Fuse Override Bits
	15:5	**RSVD** Access: RO
	4	**Reserved**
	3	**Reserved**

MFCR - Fence Control Register

	2	**Write/Read Port Block** Access: R/W 0 - Dont Block the R/W port when Query is started. 1 - Block the R/W port until the Memory Fence is completed. This is applicable for only Memory Fence.
	1	**LLC Query Enable** Access: R/W 0 - Query for 16 Ways. 1 - Query for 32 Ways. No Flexing.
	0	**Fence Controller GFDT Mode** Access: R/W Fence Controller GFDT Mode. 0 - Single bit GFDT mode. 1 - Two bit GFDT mode.

FF Performance

FF_PERF - FF Performance

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	06B1Ch
Valid Projects:	

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:11	**Reserved** Access: r/w Format: PBC
	10:8	**Throttle counter value** Access: r/w Format: Disable Counter value defining how many clocks the interface needs to be slowed down. Value: 0h — Name: **[Default]** — Description: Masked by default.
	7:3	**Reserved** Access: r/w Format: PBC
	2	**Enable throttling for SF-WM interface** Access: r/w Format: Disable Value: 0h — Name: Disable — Description: No throttling Value: 1h — Name: Enable — Description: Enable throttling in all SF-WM interfaces

FF_PERF - FF Performance

	1	**Enable throttling for SF-SBE interface** Access: r/w Format: Disable **Value / Name / Description** 0h / Disable / No throttling 1h / Enable / Enable throttling in all SF-SBE interfaces
	0	**Enable throttling for CL-SF interface** Access: r/w Format: Disable **Value / Name / Description** 0h / Disable / No throttling 1h / Enable / Enable throttling in all CL-SF interfaces **Restriction** This bit must not be set for SKL. SW may choose to use SF-SBE throttle interface(bit 1) to achive the same effect.

First Buffer Size and Start

FBSS - First Buffer Size and Start

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	0B420h

LPFCREG02 - First Buffer Size and Start

DWord	Bit	Description
0	31:16	**First Virtual Buffer Base** Access: R/W First Virtual Buffer Base: Programmed by driver to allocate a memory space for performance data storage. The buffer size should be aligned to the size of the memory allocated so it naturally aligns to the base (i.e. for 128KB bit[16]=0, 256KB bit[17:16]=0, 512KB bit[18:16]=0). Signal - lpconf_lpfc_virtual_base0 [31:16].
	15:12	**First Buffer Size** Access: R/W First Buffer Size: Determines the allowed buffer size for performance data storage. 0000b: 64KB. 0001b: 128KB. 0010b: 256KB. 0011b: 512KB. ... 1111b: 2GB. Signal - lpconf_lpfc_buffer_size0 [3:0].
	11:4	**Reserved** Access: RO Reserved.
	3	**reserved1** Access: RO RESERVED

FBSS - First Buffer Size and Start

	2	**Frame count and Draw call enable** Access: R/W Enables the replacement of a specific L3 performance counter value in the reported data with a 16-bit tag created from the concatenation of the "Frame Count" and "Draw Call Number" programmable bitfields in the "Frame Count and Draw Call Number" register. The exact counter replaced is dependent on the programmed value of the "Counter Enabling Selection" bitfield. The replaced counter is always the last one, except in the case only a single performance counter is enabled for reporting (in which no replacement occurs): **CNTRENSEL Value** / **Replaced Event Counter** 00 / No Replacement 01 / Counter 1 10 / Counter 3 11 / Counter 7
	1	**Reserved**
	0	**Master Counter Enable** Access: R/W Master Counter Enable: This is the global enable for performance tracking. Once set, it kicks off all performance tracking mechanism. Signal - lpconf_lpfc_master_cnt_en. This bit is used by all slices.

Flexible EU Event Control 0

EU_PERF_CNT_CTL0 - Flexible EU Event Control 0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0E458h

This register configures flexible EU event 0/1. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:20	**Fine Event Filter Select EU event 1** Format: U4 This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 1. Note that the fine event filter is logically applied after the coarse event filter.
	19:16	**Coarse Event Filter Select EU event 1** Format: U4 This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 1. Note that the coarse event filter is logically applied before the fine event filter.
	15:12	**Increment Event for EU event 1** Format: U4 This field controls which increment event provides the basis for flexible EU event 1.
	11:8	**Fine Event Filter Select EU event 0** Format: U4 This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 0. Note that the fine event filter is logically applied after the coarse event filter.
	7:4	**Coarse Event Filter Select EU event 0** Format: U4 This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 0. Note that the coarse event filter is logically applied before the fine event filter.

EU_PERF_CNT_CTL0 - Flexible EU Event Control 0		
	3:0	**Increment Event for EU event 0** Format: U4 This field controls which increment event provides the basis for flexible EU event 0.

Flexible EU Event Control 1

EU_PERF_CNT_CTL1 - Flexible EU Event Control 1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0E558h

This register configures flexible EU event 2/3. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:20	**Fine Event Filter Select EU event 3** Format: U4 This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 3. Note that the fine event filter is logically applied after the coarse event filter.
	19:16	**Coarse Event Filter Select EU event 3** Format: U4 This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 3. Note that the coarse event filter is logically applied before the fine event filter.
	15:12	**Increment Event for EU event 3** Format: U4 This field controls which increment event provides the basis for flexible EU event 3.
	11:8	**Fine Event Filter Select EU event 2** Format: U4 This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 2. Note that the fine event filter is logically applied after the coarse event filter.
	7:4	**Coarse Event Filter Select EU event 2** Format: U4 This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 2. Note that the coarse event filter is logically applied before the fine event filter.

EU_PERF_CNT_CTL1 - Flexible EU Event Control 1		
	3:0	**Increment Event for EU event 2** Format: U4 This field controls which increment event provides the basis for flexible EU event 2.

Flexible EU Event Control 2

EU_PERF_CNT_CTL2 - Flexible EU Event Control 2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0E658h

This register configures flexible EU event 4/5. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:20	**Fine Event Filter Select EU event 5** Format: U4 This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 5. Note that the fine event filter is logically applied after the coarse event filter.
	19:16	**Coarse Event Filter Select EU event 5** Format: U4 This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 5. Note that the coarse event filter is logically applied before the fine event filter.
	15:12	**Increment Event for EU event 5** Format: U4 This field controls which increment event provides the basis for flexible EU event 5.
	11:8	**Fine Event Filter Select EU event 4** Format: U4 This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 4. Note that the fine event filter is logically applied after the coarse event filter.
	7:4	**Coarse Event Filter Select EU event 4** Format: U4 This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 4. Note that the coarse event filter is logically applied before the fine event filter.

EU_PERF_CNT_CTL2 - Flexible EU Event Control 2		
	3:0	**Increment Event for EU event 4** Format: U4 This field controls which increment event provides the basis for flexible EU event 4.

Flexible EU Event Control 3

EU_PERF_CNT_CTL3 - Flexible EU Event Control 3

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0E758h

This register configures flexible EU event 6/7. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:20	**Fine Event Filter Select EU event 7** Format: U4 This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 7. Note that the fine event filter is logically applied after the coarse event filter.
	19:16	**Coarse Event Filter Select EU event 7** Format: U4 This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 7. Note that the coarse event filter is logically applied before the fine event filter.
	15:12	**Increment Event for EU event 7** Format: U4 This field controls which increment event provides the basis for flexible EU event 7.
	11:8	**Fine Event Filter Select EU event 6** Format: U4 This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 6. Note that the fine event filter is logically applied after the coarse event filter.
	7:4	**Coarse Event Filter Select EU event 6** Format: U4 This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 6. Note that the coarse event filter is logically applied before the fine event filter.

EU_PERF_CNT_CTL3 - Flexible EU Event Control 3		
	3:0	**Increment Event for EU event 6** Format: U4 This field controls which increment event provides the basis for flexible EU event 6.

Flexible EU Event Control 4

EU_PERF_CNT_CTL4 - Flexible EU Event Control 4

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0E45Ch

This register configures flexible EU event 8/9. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:20	**Fine Event Filter Select EU event 9** Format: U4 This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 9. Note that the fine event filter is logically applied after the coarse event filter.
	19:16	**Coarse Event Filter Select EU event 9** Format: U4 This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 9. Note that the coarse event filter is logically applied before the fine event filter.
	15:12	**Increment Event for EU event 9** Format: U4 This field controls which increment event provides the basis for flexible EU event 9.
	11:8	**Fine Event Filter Select EU event 8** Format: U4 This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 8. Note that the fine event filter is logically applied after the coarse event filter.
	7:4	**Coarse Event Filter Select EU event 8** Format: U4 This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 8. Note that the coarse event filter is logically applied before the fine event filter.

EU_PERF_CNT_CTL4 - Flexible EU Event Control 4		
	3:0	**Increment Event for EU event 8** Format: U4 This field controls which increment event provides the basis for flexible EU event 8.

Flexible EU Event Control 5

EU_PERF_CNT_CTL5 - Flexible EU Event Control 5

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0E55Ch

This register configures flexible EU event 10/11. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:20	**Fine Event Filter Select EU event 11** Format: U4 This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 11. Note that the fine event filter is logically applied after the coarse event filter.
	19:16	**Coarse Event Filter Select EU event 11** Format: U4 This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 11. Note that the coarse event filter is logically applied before the fine event filter.
	15:12	**Increment Event for EU event 11** Format: U4 This field controls which increment event provides the basis for flexible EU event 11.
	11:8	**Fine Event Filter Select EU event 10** Format: U4 This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 10. Note that the fine event filter is logically applied after the coarse event filter.
	7:4	**Coarse Event Filter Select EU event 10** Format: U4 This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 10. Note that the coarse event filter is logically applied before the fine event filter.

EU_PERF_CNT_CTL5 - Flexible EU Event Control 5		
	3:0	**Increment Event for EU event 10** Format: U4 This field controls which increment event provides the basis for flexible EU event 10.

Flexible EU Event Control 6

EU_PERF_CNT_CTL6 - Flexible EU Event Control 6

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0E65Ch

This register configures flexible EU event 12/13. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:20	**Fine Event Filter Select EU event 13** Format: U4 This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 13. Note that the fine event filter is logically applied after the coarse event filter.
	19:16	**Coarse Event Filter Select EU event 13** Format: U4 This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 13. Note that the coarse event filter is logically applied before the fine event filter.
	15:12	**Increment Event for EU event 13** Format: U4 This field controls which increment event provides the basis for flexible EU event 13.
	11:8	**Fine Event Filter Select EU event 12** Format: U4 This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 12. Note that the fine event filter is logically applied after the coarse event filter.
	7:4	**Coarse Event Filter Select EU event 12** Format: U4 This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 12. Note that the coarse event filter is logically applied before the fine event filter.

EU_PERF_CNT_CTL6 - Flexible EU Event Control 6		
	3:0	**Increment Event for EU event 12** Format: U4 This field controls which increment event provides the basis for flexible EU event 12.

FORCE_TO_NONPRIV

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00002094
Access:	R/W
Size (in bits):	32
Address:	024D0h-024D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_RCSUNIT
Address:	024D4h-024D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_RCSUNIT
Address:	024D8h-024DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_RCSUNIT
Address:	024DCh-024DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_RCSUNIT
Address:	024E0h-024E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_RCSUNIT
Address:	024E4h-024E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_RCSUNIT
Address:	024E8h-024EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_RCSUNIT
Address:	024ECh-024EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_RCSUNIT
Address:	024F0h-024F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_RCSUNIT
Address:	024F4h-024F7h
Name:	FORCE_TO_NONPRIV

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
ShortName:	FORCE_TO_NONPRIV_9_RCSUNIT
Address:	024F8h-024FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_RCSUNIT
Address:	024FCh-024FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_RCSUNIT
Address:	124D0h-124D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VCSUNIT0
Address:	124D4h-124D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VCSUNIT0
Address:	124D8h-124DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VCSUNIT0
Address:	124DCh-124DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VCSUNIT0
Address:	124E0h-124E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VCSUNIT0
Address:	124E4h-124E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VCSUNIT0
Address:	124E8h-124EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VCSUNIT0
Address:	124ECh-124EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VCSUNIT0
Address:	124F0h-124F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VCSUNIT0
Address:	124F4h-124F7h

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VCSUNIT0
Address:	124F8h-124FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VCSUNIT0
Address:	124FCh-124FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VCSUNIT0
Address:	1A4D0h-1A4D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VECSUNIT
Address:	1A4D4h-1A4D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VECSUNIT
Address:	1A4D8h-1A4DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VECSUNIT
Address:	1A4DCh-1A4DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VECSUNIT
Address:	1A4E0h-1A4E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VECSUNIT
Address:	1A4E4h-1A4E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VECSUNIT
Address:	1A4E8h-1A4EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VECSUNIT
Address:	1A4ECh-1A4EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VECSUNIT
Address:	1A4F0h-1A4F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VECSUNIT

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Address:	1A4F4h-1A4F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VECSUNIT
Address:	1A4F8h-1A4FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VECSUNIT
Address:	1A4FCh-1A4FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VECSUNIT
Address:	1C4D0h-1C4D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VCSUNIT1
Address:	1C4D4h-1C4D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VCSUNIT1
Address:	1C4D8h-1C4DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VCSUNIT1
Address:	1C4DCh-1C4DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VCSUNIT1
Address:	1C4E0h-1C4E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VCSUNIT1
Address:	1C4E4h-1C4E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VCSUNIT1
Address:	1C4E8h-1C4EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VCSUNIT1
Address:	1C4ECh-1C4EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VCSUNIT1
Address:	1C4F0h-1C4F3h
Name:	FORCE_TO_NONPRIV

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
ShortName:	FORCE_TO_NONPRIV_8_VCSUNIT1
Address:	1C4F4h-1C4F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VCSUNIT1
Address:	1C4F8h-1C4FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VCSUNIT1
Address:	1C4FCh-1C4FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VCSUNIT1
Address:	224D0h-224D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_BCSUNIT
Address:	224D4h-224D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_BCSUNIT
Address:	224D8h-224DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_BCSUNIT
Address:	224DCh-224DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_BCSUNIT
Address:	224E0h-224E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_BCSUNIT
Address:	224E4h-224E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_BCSUNIT
Address:	224E8h-224EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_BCSUNIT
Address:	224ECh-224EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_BCSUNIT
Address:	224F0h-224F3h

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV

Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_BCSUNIT
Address:	224F4h-224F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_BCSUNIT
Address:	224F8h-224FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_BCSUNIT
Address:	224FCh-224FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_BCSUNIT

These registers are privilege registers and are not allowed to be written from non-privilege batch buffer. These are global registers and power context save/restored.

DWord	Bit	Description
0	31	**Reseved** Format: MBZ
	30:26	**Reserved** Format: MBZ
	25:2	**Non Privilege Register Address** Format: MmioAddress[25:2] **Description** This field contains the MMIO offset of a register. MMIO offset programmed in this field will be treated as a non-privilege register by render command streamer while processing register writes from a non-privilege batch buffer. This register provides programmability is to extend the non-privilege register table mentioned in MI_BATCH_BUFFER_START command in render command streamer. **Value** / **Name** 825h / **[Default]**
	1:0	**Reserved** Format: MBZ

Frame Buffer Cache Definition Register

FBCDR - Frame Buffer Cache Definition Register

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04068h

DWord	Bit	Description
0	31:25	**Reserved** Default Value: 0000000b Access: R/W
	24:23	**Arbitration of LLCWBInv v/s Memory Writes** Default Value: 00b Access: R/W A round robin is enabled to inject LLCWbInv cycles to memory write stream. The conflicts are handled with programming the round robin mechanism. 00b: 1 memory write and 1 LLCWbInv. 01b: 2 memory writes and 1 LLCWbInv 10b: 4 memory writes and 1 LLCWbInv 11b: 8 memory writes and 1 LLCWbInv
	22:18	**Inside CBO** Default Value: 00000b Access: R/W CBO ID is added in LLC to separate the banks of LLC in a given slice. GFX driver will set the corresponding bits to enable the toggling of CBOID during flushing [22]: Enable h/w to toggle of CBOID[4] during flush. [21]: Enable h/w to toggle of CBOID[3] during flush. [20]: Enable h/w to toggle of CBOID[2] during flush. [19]: Enable h/w to toggle of CBOID[1] during flush. [18]: Enable h/w to toggle of CBOID[0] during flush. Setting the corresponding bit would mean h/w has to permute the corresponding bit for CBOID during flush, else h/w will keep the corresponding bit as "0" Note: For SKL 2-core system, only bit[18] needs to be set. For SKL 4-core system, bits [19:18] needs to be set.

FBCDR - Frame Buffer Cache Definition Register

	17:16	**Inside CBOID Enable** Default Value: 00b Access: R/W Inside CBO ID is added in LLC to separate the banks of LLC in a given slice. GFX driver will set the corresponding bits to enable the toggling of Inside CBOID during flushing: [17]: Enable h/w to toggle of InsideCBOID[1] during flush. [16]: Enable h/w to toggle of InsideCBOID[0] during flush. Setting the corresponding bit would mean h/w has to permute the corresponding bit for InsideCBOID during flush, else h/w will keep the corresponding bit as "0". Note: For SKL client this field needs to be programmed as "01"
	15:0	**Frame Buffer Caching enabled ways** Default Value: 0000h Access: R/W The Last Level cache is a 16 way structure where some of the ways are armed to allocate Frame Buffer Data. This determination is done via assigning a QOS value for Frame Buffer and QOS assignments for ways. Each bit corresponds to a way in this definition. Bit[15]: Way#15 is enabled to allocate Frame Buffer Data. Bit[14]: Way#14 is enabled to allocate Frame Buffer Data. Bit[13]: Way#13 is enabled to allocate Frame Buffer Data. Bit[12]: Way#12 is enabled to allocate Frame Buffer Data. Bit[11]: Way#11 is enabled to allocate Frame Buffer Data. Bit[10]: Way#10 is enabled to allocate Frame Buffer Data. Bit[9]: Way#9 is enabled to allocate Frame Buffer Data. Bit[8]: Way#8 is enabled to allocate Frame Buffer Data. Bit[7]: Way#7 is enabled to allocate Frame Buffer Data. Bit[6]: Way#6 is enabled to allocate Frame Buffer Data. Bit[5]: Way#5 is enabled to allocate Frame Buffer Data. Bit[4]: Way#4 is enabled to allocate Frame Buffer Data. Bit[3]: Way#3 is enabled to allocate Frame Buffer Data. Bit[2]: Way#2 is enabled to allocate Frame Buffer Data. Bit[1]: Way#1 is enabled to allocate Frame Buffer Data. Bit[0]: Way#0 is enabled to allocate Frame Buffer Data.

Frame count and Draw call number

FCDCN - Frame count and Draw call number

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	0B430h

DWord	Bit	Description
0	31:16	**Reserved** Access: RO
	15:8	**Frame Number** Access: R/W Frame number is the first of two reporting tags that software (i.e. driver) may populate in order to provide reference points during L3 performance reporting modes. Should the "Frame Count and Draw Call Enable" bit (FCDCE) in the "First Buffer Size and Start" register be set, LPFC will selectively replace one of the reporting events with this programmable tag (in addition to the "Draw Call Number" field below). Software may use this to provide reference points for L3 performance counts when parsing the resulting data stream to align reported counts to higher-level operations. The original incarnation called for software to increment this value with each frame, however, the field is generic and may be used for any tagging purpose.
	7:0	**Draw call number** Access: R/W The draw call number is the second programmable reporting tag provided by LPFC. With this second programmable tag, a more granular sampling boundary may be created by software, or it may be used to provide an alternative reference point for tracking L3 performance. The original incarnation called for software to increment this value with every draw call, but the field is generic and may be used for any similar purpose.

FUSE_STATUS

FUSE_STATUS	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	42000h-42003h
Name:	Fuse Status
ShortName:	FUSE_STATUS
Power:	PG0
Reset:	global

This register is on the ungated clock and the chip reset, not the FLR.

DWord	Bit	Description
0	31	**Fuse Download Status** Access: RO This field indicates the status of fuse and strap download to the Display Engine. After fuse and strap download, fuses will be distributed within the Display Engine. Value / Name: 0b – Not Done 1b – Done
	30:28	**Reserved**
	27	**Reserved**
	26	**Reserved**
	25	**Reserved**
	24:0	**Reserved**

GAB Arbitration Programmable

GAB_AP - GAB Arbitration Programmable		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	040F0h	
DWord	**Bit**	**Description**
0	31:0	**Reserved**

GAB LRA 0

GAB_LRA_0 - GAB LRA 0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x1F100F00
Size (in bits):	32
Address:	04A70h

DWord	Bit	Description
0	31:29	**Reserved** Default Value: 000b Access: RO
	28:24	**GAB LRA1 Max** Default Value: 11111b Access: R/W Maximum value of programmable LRA1.
	23:21	**Reserved** Default Value: 000b Access: RO
	20:16	**GAB LRA1 Min** Default Value: 10000b Access: R/W Minimum value of programmable LRA1.
	15:13	**Reserved** Default Value: 000b Access: RO
	12:8	**GAB LRA0 Max** Default Value: 01111b Access: R/W Maximum value of programmable LRA0.
	7:5	**Reserved** Default Value: 000b Access: RO
	4:0	**GABLRA0 Min** Default Value: 00000b Access: R/W Minimum value of programmable LRA0.

GAB LRA 1

GAB_LRA_1 - GAB LRA 1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000001
Size (in bits):	32
Address:	04A74h

DWord	Bit	Description
0	31:4	**Reserved** Default Value: 0000000h Access: RO
	3:2	**BLB** Default Value: 00b Access: R/W Which LRA should BLB use.
	1:0	**BCS** Default Value: 01b Access: R/W Which LRA should BCS use.

GAB unit Control Register

GAB_CTL_REG - GAB unit Control Register

Register Space:	MMIO: 0/2/0
Source:	BlitterCS
Default Value:	0x000000BF
Access:	R/W
Size (in bits):	32
Address:	24000h

DefaultValue=FF0000BFh Trusted Type = 1

DWord	Bit	Description
0	31:9	**Reserved**
	8	**Continue after Page Fault** Value / Name / Description: 1 / GAB Set / Ipon receiving a page fault when requesting an address translation, GAB will set address bit 39 to 1 and continue. 0 / GAB Hang / GAB will hang on a page fault. Default = b0.
	7:6	**PPGTT BCS TLB LRA MIN** Default Value: 10b TLB Depth Partitioning Register In PP GTT Mode.
	5:4	**GAB write request priority signal value used in GAC arbitration** Default Value: 11b
	3:2	**GAB read only request priority signal value used in GAC arbitration** Default Value: 11b
	1:0	**GAB read request priority signal value used in GAC arbitration** Default Value: 11b

GAC_GAM Arbitration Counters Register 0

ARB_GAC_GAM_REQCNTS0 - GAC_GAM Arbitration Counters Register 0		
Register Space:	MMIO: 0/2/0	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043A8h	
DWord	**Bit**	**Description**
0	31:22	**Reserved**
	21:16	**Number of GAC WR requests to be accumulated before applying the arbitration**
	15:14	**Reserved**
	13:8	**Number of GAC R requests to be accumulated before applying the arbitration**
	7:6	**Reserved**
	5:0	**Number of GAC RO requests to be accumulated before applying the arbitration**

GAC_GAM Arbitration Counters Register 1

ARB_GAC_GAM_REQCNTS1 - GAC_GAM Arbitration Counters Register 1		
Register Space:	MMIO: 0/2/0	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043ACh	
DWord	**Bit**	**Description**
0	31:22	**Reserved**
	21:16	**Number of GAC WR requests to be accumulated before applying the arbitration**
	15:14	**Reserved**
	13:8	**Number of GAC R requests to be accumulated before applying the arbitration**
	7:6	**Reserved**
	5:0	**Number of GAC RO requests to be accumulated before applying the arbitration**

GAC_GAM R Arbitration Register 0

ARB_R_GAC_GAM0 - GAC_GAM R Arbitration Register 0	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	043E0h

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 1**
	26:24	**Goto field for entry 1 when request vector is 11b**
	23:21	**Goto field for entry 1 when request vector is 10b**
	20:18	**Goto field for entry 1 when request vector is 01b**
	17:15	**Goto field for entry 1 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 0**
	11:9	**Goto field for entry 0 when request vector is 11b**
	8:6	**Goto field for entry 0 when request vector is 10b**
	5:3	**Goto field for entry 0 when request vector is 01b**
	2:0	**Goto field for entry 0 when request vector is 00b**

GAC_GAM R Arbitration Register 1

ARB_R_GAC_GAM1 - GAC_GAM R Arbitration Register 1	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	043E4h

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 3**
	26:24	**Goto field for entry 3 when request vector is 11b**
	23:21	**Goto field for entry 3 when request vector is 10b**
	20:18	**Goto field for entry 3 when request vector is 01b**
	17:15	**Goto field for entry 3 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 2**
	11:9	**Goto field for entry 2 when request vector is 11b**
	8:6	**Goto field for entry 2 when request vector is 10b**
	5:3	**Goto field for entry 2 when request vector is 01b**
	2:0	**Goto field for entry 2 when request vector is 00b**

GAC_GAM R Arbitration Register 2

ARB_R_GAC_GAM2 - GAC_GAM R Arbitration Register 2	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	043E8h

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 5**
	26:24	**Goto field for entry 5 when request vector is 11b**
	23:21	**Goto field for entry 5 when request vector is 10b**
	20:18	**Goto field for entry 5 when request vector is 01b**
	17:15	**Goto field for entry 5 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 4**
	11:9	**Goto field for entry 4 when request vector is 11b**
	8:6	**Goto field for entry 4 when request vector is 10b**
	5:3	**Goto field for entry 4 when request vector is 01b**
	2:0	**Goto field for entry 4 when request vector is 00b**

GAC_GAM R Arbitration Register 3

ARB_R_GAC_GAM3 - GAC_GAM R Arbitration Register 3	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	043ECh

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 7**
	26:24	**Goto field for entry 7 when request vector is 11b**
	23:21	**Goto field for entry 7 when request vector is 10b**
	20:18	**Goto field for entry 7 when request vector is 01b**
	17:15	**Goto field for entry 7 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 6**
	11:9	**Goto field for entry 6 when request vector is 11b**
	8:6	**Goto field for entry 6 when request vector is 10b**
	5:3	**Goto field for entry 6 when request vector is 01b**
	2:0	**Goto field for entry 6 when request vector is 00b**

GAC_GAM RO Arbitration Register 0

ARB_RO_GAC_GAM0 - GAC_GAM RO Arbitration Register 0	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	043D0h

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 1**
	26:24	**Goto field for entry 1 when request vector is 11b**
	23:21	**Goto field for entry 1 when request vector is 10b**
	20:18	**Goto field for entry 1 when request vector is 01b**
	17:15	**Goto field for entry 1 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 01**
	11:9	**Goto field for entry 01 when request vector is 11b**
	8:6	**Goto field for entry 01 when request vector is 10b**
	5:3	**Goto field for entry 01 when request vector is 01b**
	2:0	**Goto field for entry 01 when request vector is 00b**

GAC_GAM RO Arbitration Register 1

ARB_RO_GAC_GAM1 - GAC_GAM RO Arbitration Register 1	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	043D4h

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 3**
	26:24	**Goto field for entry 3 when request vector is 11b**
	23:21	**Goto field for entry 3 when request vector is 10b**
	20:18	**Goto field for entry 3 when request vector is 01b**
	17:15	**Goto field for entry 3 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 2**
	11:9	**Goto field for entry 2 when request vector is 11b**
	8:6	**Goto field for entry 2 when request vector is 10b**
	5:3	**Goto field for entry 2 when request vector is 01b**
	2:0	**Goto field for entry 2 when request vector is 00b**

GAC_GAM RO Arbitration Register 2

ARB_RO_GAC_GAM2 - GAC_GAM RO Arbitration Register 2	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	043D8h

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 5**
	26:24	**Goto field for entry 5 when request vector is 11b**
	23:21	**Goto field for entry 5 when request vector is 10b**
	20:18	**Goto field for entry 5 when request vector is 01b**
	17:15	**Goto field for entry 5 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 4**
	11:9	**Goto field for entry 4 when request vector is 11b**
	8:6	**Goto field for entry 4 when request vector is 10b**
	5:3	**Goto field for entry 4 when request vector is 01b**
	2:0	**Goto field for entry 4 when request vector is 00b**

GAC_GAM RO Arbitration Register 3

ARB_RO_GAC_GAM3 - GAC_GAM RO Arbitration Register 3	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	043DCh

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 7**
	26:24	**Goto field for entry 7 when request vector is 11b**
	23:21	**Goto field for entry 7 when request vector is 10b**
	20:18	**Goto field for entry 7 when request vector is 01b**
	17:15	**Goto field for entry 7 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 6**
	11:9	**Goto field for entry 6 when request vector is 11b**
	8:6	**Goto field for entry 6 when request vector is 10b**
	5:3	**Goto field for entry 6 when request vector is 01b**
	2:0	**Goto field for entry 6 when request vector is 00b**

GAC_GAM WR Arbitration Register 0

ARB_WR_GAC_GAM0 - GAC_GAM WR Arbitration Register 0	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	043F0h

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 1**
	26:24	**Goto field for entry 1 when request vector is 11b**
	23:21	**Goto field for entry 1 when request vector is 10b**
	20:18	**Goto field for entry 1 when request vector is 01b**
	17:15	**Goto field for entry 1 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 0**
	11:9	**Goto field for entry 0 when request vector is 11b**
	8:6	**Goto field for entry 0 when request vector is 10b**
	5:3	**Goto field for entry 0 when request vector is 01b**
	2:0	**Goto field for entry 0 when request vector is 00b**

GAC_GAM WR Arbitration Register 1

ARB_WR_GAC_GAM1 - GAC_GAM WR Arbitration Register 1	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	043F4h

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 3**
	26:24	**Goto field for entry 3 when request vector is 11b**
	23:21	**Goto field for entry 3 when request vector is 10b**
	20:18	**Goto field for entry 3 when request vector is 01b**
	17:15	**Goto field for entry 3 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 2**
	11:9	**Goto field for entry 2 when request vector is 11b**
	8:6	**Goto field for entry 2 when request vector is 10b**
	5:3	**Goto field for entry 2 when request vector is 01b**
	2:0	**Goto field for entry 2 when request vector is 00b**

GAC_GAM WR Arbitration Register 2

ARB_WR_GAC_GAM2 - GAC_GAM WR Arbitration Register 2	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	043F8h

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 5**
	26:24	**Goto field for entry 5 when request vector is 11b**
	23:21	**Goto field for entry 5 when request vector is 10b**
	20:18	**Goto field for entry 5 when request vector is 01b**
	17:15	**Goto field for entry 5 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 4**
	11:9	**Goto field for entry 4 when request vector is 11b**
	8:6	**Goto field for entry 4 when request vector is 10b**
	5:3	**Goto field for entry 4 when request vector is 01b**
	2:0	**Goto field for entry 4 when request vector is 00b**

GAC_GAM WR Arbitration Register 3

ARB_WR_GAC_GAM3 - GAC_GAM WR Arbitration Register 3	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	043FCh

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 7**
	26:24	**Goto field for entry 7 when request vector is 11b**
	23:21	**Goto field for entry 7 when request vector is 10b**
	20:18	**Goto field for entry 7 when request vector is 01b**
	17:15	**Goto field for entry 7 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 6**
	11:9	**Goto field for entry 6 when request vector is 11b**
	8:6	**Goto field for entry 6 when request vector is 10b**
	5:3	**Goto field for entry 6 when request vector is 01b**
	2:0	**Goto field for entry 6 when request vector is 00b**

GAFS MAX URB READ EVENT

GAFS_MAX_URBRD - GAFS MAX URB READ EVENT	
Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	00DB4h

This register mirrors an accumulating count for Unslice FF control It is enabled by configuration bits in GPMunit and SPMunits. Note that count is never cleared and delta should be calculated by sampling the initial register value at the start and subtracting that value off from the final sample value.

DWord	Bit	Description
0	31:0	**Unslice FF Event Count** Access: RO

GAM and SA Communication Register

GAMSACOMREG - GAM and SA Communication Register

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	042A0h

DWord	Bit	Description
0	31:16	**Mask Bits** Default Value: 0000h Access: RO Mask Bits act as Write Enables for the bits[15:0] of this register.
	15	**GAM and SA Communication Register 15** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	14	**GAM and SA Communication Register 14** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	13	**GAM and SA Communication Register 13** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	12	**GAM and SA Communication Register 12** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	11	**GAM and SA Communication Register 11** Default Value: 0b Access: R/W For Future Use. This bit is self clear.

GAMSACOMREG - GAM and SA Communication Register

	10	**GAM and SA Communication Register 10** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	9	**GAM and SA Communication Register 9** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	8	**GAM and SA Communication Register 8** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	7	**GAM and SA Communication Register 7** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	6	**GAM and SA Communication Register 6** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	5	**GAM and SA Communication Register 5** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	4	**GAM and SA Communication Register 4** Default Value: 0b Access: R/W For Future Use. This bit is self clear.

GAMSACOMREG - GAM and SA Communication Register

	3	**GAM and SA Communication Register 3** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	2	**GAM and SA Communication Register 2** Default Value: 0b Access: R/W Bit2 - Root Table Address Update Request. This bit is self clear.
	1	**GAM and SA Communication Register 1** Default Value: 0b Access: R/W Bit1 - Queued Descriptor Request. This bit is self clear.
	0	**GAM and SA Communication Register 0** Default Value: 0b Access: R/W Bit0 - Context Cache Invalidator Request. This bit is self clear.

GAM Context Save

GAM_CTX - GAM Context Save

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04FFCh

DWord	Bit	Description
0	31:16	**Mask Bits** Default Value: 0000h Access: RO
	15:2	**Reserved** Default Value: 0000h Access: RO Reserved Bits for future use
	1	**Context Save Start - Chunk2** Default Value: 0b Access: R/W Context Save start for chunk2 Bit[1] Context Save Request start 1'b0 : Context save is not being requested 1'b1 : Context save is being requested When a 1 is written to this bit , with the corresponding mask bit set, it will kick off a context save. Once the save is complete the bit will be cleared. GAMunit on receiving this message sends the Chunk-2 (Cachelines following Chunk1) of context image to CS
	0	**Context Save Start - Chunk1** Default Value: 0b Access: R/W Context Save start for chunk1 Bit[1] Context Save Request start 1'b0 : Context save is not being requested 1'b1 : Context save is being requested When a 1 is written to this bit , with the corresponding mask bit set, it will kick off a context save. Once the save is complete the bit will be cleared. GAMunit on receiving this message sends the Chunk-1 (first 8 Cachelines of its context image) of context image to CS

GAM Context Save Register

GAM_CTX - GAM Context Save Register

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	04FFCh

This register is used to send messages to enable context saving. This register may not be written from CPU. Bits [0] and [1] getting set are mutually exclusive.

DWord	Bit	Description
0	31:16	**Masks** Format: Mask[15:0] A 1 in a bit in this field allows the modification of the corresponding bit in bits 15:0.
	15:2	**Reserved** Format: MBZ
	1	**Context Save Start - Chunk2** Format: Enable When a 1 is written to this bit , with the corresponding mask bit set, it will kick off a context save. Once the save is complete the bit will be cleared. GAMunit on receiving this message sends the Chunk-2 (Cachelines following Chunk1) of context image to CS.
	0	**Context Save Start - Chunk1** Format: Enable When a 1 is written to this bit with the corresponding mask bit set, it will kick off a context save. Once the save is complete the bit will be cleared. GAMunit on receiving this message sends the Chunk-1 (first 8 Cachelines of its context image) of context image to CS.

Gam Fub Done1 Lookup Register

DONE1_REG - Gam Fub Done1 Lookup Register		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0407Ch	
DWord	**Bit**	**Description**
0	31:0	**Gam Fub Done1 Lookup Reg** Default Value: 00000000h Access: RO GAM Done1 signals.

Gam Fub Done Lookup Register

DONE_REG - Gam Fub Done Lookup Register		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	040B0h	
DWord	**Bit**	**Description**
0	31:0	**Gam Fub Done Lookup Reg** Default Value: 00000000h Access: RO 31 CVS Credit Fifo is empty. 30 CVS TLB does not have any cycles. 29 Z Credit fifo is empty. 28 ZTLB does not have any cycles. 27 RCC Credit Fifo is empty. 26 RCC TLB does not have any cycles. 25 L3 Credit fifo is empty. 24 L3 TLB does not have any cycles. 23 VLF Credit fifo is empty. 22 VLF TLB does not have any cycles. 21 CASC Credit fifo empty. 20 CASC TLB does not have any cycles. 19 Miss Fub Done. 18 Read Stream Done. 17 Read Steam Fifo is empty. 16 Recycle Fifo in rstrm is empty. 15 TLB Pend Done. 14 TLB Pend PQ Array is done. 13 TLB pend PB Array is done. 12 Read route fub is done. 11 Gafm Data fifo is empty. 10 GAP data fifo is empty. 9 GAC data fifo is empty. 8 Wrdp is done with all the cycles. 7 Wrdp RID fifo is empty. 6 No hold from midarb to RTSTRM. 5 No hold from TLBPEND to MIDARB. 3 Tied to "1" - to be defined. 2 Fence FSM are IDLE. 1 Non PD Load Done. 0 Tied to "1" - to be defined.

GAMMA_MODE

GAMMA_MODE

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank

Address:	4A480h-4A483h
Name:	Pipe Gamma Mode
ShortName:	GAMMA_MODE_A
Power:	PG1
Reset:	soft

Address:	4AC80h-4AC83h
Name:	Pipe Gamma Mode
ShortName:	GAMMA_MODE_B
Power:	PG2
Reset:	soft

Address:	4B480h-4B483h
Name:	Pipe Gamma Mode
ShortName:	GAMMA_MODE_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:16	**Reserved**
	15	**Reserved**
	14:2	**Reserved**
	1:0	**Gamma Mode** This field selects which mode the pipe palette/gamma correction logic works in. Other gamma units, such as in the planes, are unaffected by this bit.

Value	Name	Description
00b	8 bit	8-bit Legacy Palette Mode
01b	10 bit	10-bit Precision Palette Mode
10b	12 bit	12-bit Interpolated Gamma Mode
11b	Split	Split Gamma Mode (separate pipe gamma functions before and after pipe CSC)

GAM Put Delay

GAM_PUT_DLY - GAM Put Delay		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0401Ch	
Number of clocks to wait between puts		
DWord	**Bit**	**Description**
0	31:0	**GAM PUT DELAY** Default Value: 00000000h Access: R/W

GAMT_DONE Register

GAMT_DONE - GAMT_DONE Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04AC0h

DWord	Bit	Description
0	31:0	**GAMT_DONE Register** Default Value: 00000000h Access: RO 31: vebxtlb_all_done_f 30: cvstlb_all_done_f 29: ztlb_all_done_f 28: l3tlb_all_done_f 27: rcctlb_all_done_f 26: mfxtlb_all_done_f 25: vlftlb_all_done_f 24: bwgtlb_all_done_f 23: gamwrrb_all_done_f 22: mfxsl1tlb_all_done_f 21: vlfsl1tlb_all_done_f 20: bwgtlb_fifo_empty 19: l3tlb_fifo_empty 18: ztlb_fifo_empty 17: rcctlb_fifo_empty 16: cvstlb_fifo_empty 15: vebxtlb_fifo_empty 14: mfxtlb_fifo_empty 13: mfxsl1tlb_fifo_empty 12: vlfsl1tlb_fifo_empty 11: vlftlb_fifo_empty 10: wrdp_gafm_fifo_empty 9: wrdp_gap_fifo_empty 8: wrdp_gacfg_fifo_empty 7: wrdp_cs_fifo_empty 6: wrdp_vecs_fifo_empty 5: wrdp_oacs_fifo_empty 4: wrdp_gacv_fifo_empty 3: Tied to 1 2: Tied to 1 1: Tied to 1 0: Tied to 1

GAMT_ECO_REG_RO_IA

GAMT_ECO_REG_RO_IA - GAMT_ECO_REG_RO_IA	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04AB4h

DWord	Bit	Description
0	31:0	**GAMTECO_REG_RO_IA** Default Value: 00000000h Access: RO This register is for ECO usage. RO register with IA Access Type on DEV reset.

GAMT_ECO_REG_RW_IA

GAMT_ECO_REG_RW_IA - GAMT_ECO_REG_RW_IA

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000AB1B
Size (in bits):	32
Address:	04AB0h

Programmable Request Count - VEBX and BLT

DWord	Bit	Description
0	31:0	**GAMTECO_REG_RW_IA** Default Value: 0000AB1Bh Access: R/W Bit[31:16] = Reserved. Bit[15:8] = Number of max outstanding cycles (Misses and Hits not present) that can be allowed to potentially fault = 171. Bit[7:6] = Reserved. Bit[5:0] = Number of max outstanding misses that can be allowed to potentially fault = 27.

GAMT Arbiter Mode Control

GAMTARBMODE - GAMT Arbiter Mode Control

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04A08h

DWord	Bit	Description
0	31:16	**Mask Bits** Default Value: 0000h Access: RO
	15	**GAMT Arbiter Mode Control 15** Default Value: 0b Access: R/W For Future Use
	14	**GAMT Arbiter Mode Control 14** Default Value: 0b Access: R/W 0 - Cache the TLB even if there is a FAULT in GAMW read return. 1 - Don't Cache the TLB if there is a fault in GAMW return.
	13	**GAMT Arbiter Mode Control 13** Default Value: 0b Access: R/W 0 - VEBXTLB clock gate enabled. 1 - VEBXTLB clock gate disabled.
	12	**GAMT Arbiter Mode Control 12** Default Value: 0b Access: R/W 0 - MFXSL1TLB clock gate enabled. 1 - MFXSL1TLB clock gate disabled.
	11	**GAMT Arbiter Mode Control 11** Default Value: 0b Access: R/W 0 - VLFSL1TLB clock gate enabled. 1 - VLFSL1TLB clock gate disabled.

GAMTARBMODE - GAMT Arbiter Mode Control

	10	**GAMT Arbiter Mode Control 10** Default Value: 0b Access: R/W 0 - gamwrrb clock gate enabled. 1 - gamwrrb clock gate disabled.
	9	**GAMT Arbiter Mode Control 9** Default Value: 0b Access: R/W 0 - BWGTLB clock gate enabled. 1 - BWGTLB clock gate disabled.
	8	**GAMT Arbiter Mode Control 8** Default Value: 0b Access: R/W 0 - VLFTLB clock gate enabled. 1 - VLFTLB clock gate disabled.
	7	**GAMT Arbiter Mode Control 7** Default Value: 0b Access: R/W 0 - MFXTLB clock gate enabled. 1 - MFXTLB clock gate disabled.
	6	**GAMT Arbiter Mode Control 6** Default Value: 0b Access: R/W 0 - RCCTLB clock gate enabled. 1 - RCCTLB clock gate disabled.
	5	**GAMT Arbiter Mode Control 5** Default Value: 0b Access: R/W 0 - L3TLB clock gate enabled. 1 - L3TLB clock gate disabled. Bit[5] needs to be set as a workaround due to recent gacb. To update bit 5, a value of 0x00200020 needs to be written.

GAMTARBMODE - GAMT Arbiter Mode Control

	4	**GAMT Arbiter Mode Control 4** Default Value: 0b Access: R/W 0 - ZTLB clock gate enabled. 1 - ZTLB clock gate disabled.
	3	**GAMT Arbiter Mode Control 3** Default Value: 0b Access: R/W 0 - CVS clock gate enabled. 1 - CVS clock gate disabled.
	2	**GAMT Arbiter Mode Control 2** Default Value: 0b Access: R/W 0 - No reg_hdc_inval_ack_force - take the value from client. 1 - reg_hdc_inval_ack_force - force value to 1 - disregard client value.
	1	**GAMT Arbiter Mode Control 1** Default Value: 0b Access: R/W Bit [1]: Address Swizzling for Tiled Surfaces. This register location is updated via GFX Driver prior to enabling DRAM accesses. Driver needs to obtain the need for memory address swizzling via DRAM configuration registers and set the following bits (in Display Engine and Render/Media access streams). 0: No address Swizzling. 1: Address bit[1] needs to be swizzled for tiled surfaces.
	0	**GAMT Arbiter Mode Control 0** Default Value: 0b Access: R/W Bit[0]: GAM to Bypass GTT Translation. GAM to Bypass GTT Translation and pass logical addresses through with 0's padded on the MSBs to form the Physical Address.

GAMW_ECO_BUS_RO_IA

GAMW_ECO_BUS_RO_IA - GAMW_ECO_BUS_RO_IA		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0408Ch	
DWord	**Bit**	**Description**
0	31:0	**GAMWECO_BUS_RO_IA** Default Value: 00000000h Access: RO This register is for ECO usage. RO register with IA Access Type on BUS reset.

GAMW_ECO_BUS_RW_IA

GAMW_ECO_BUS_RW_IA - GAMW_ECO_BUS_RW_IA		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04084h	
DWord	**Bit**	**Description**
0	31:0	**GAMWECO_BUS_RW_IA** Default Value: 00000000h Access: R/W This register is for ECO usage. RW register with IA Access Type on BUS reset.

GAMW_ECO_DEV_RO_IA

GAMW_ECO_DEV_RO_IA - GAMW_ECO_DEV_RO_IA		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04088h	
DWord	**Bit**	**Description**
0	31:0	**GAMWECO_DEV_RO_IA** Default Value: 00000000h Access: RO This register is for ECO usage. RO register with IA Access Type on DEV reset.

GAMW_ECO_DEV_RW_IA

GAMW_ECO_DEV_RW_IA - GAMW_ECO_DEV_RW_IA		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04080h	
DWord	**Bit**	**Description**
0	31:0	**GAMWECO_DEV_RW_IA** Default Value: 00000000h Access: R/W This register is for ECO usage. RW register with IA Access Type on DEV reset.

GAMW Power Context Save

PWRCTXSAVE - GAMW Power Context Save

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04000h

DWord	Bit	Description
0	31:16	**Mask Bits** Default Value: 0000h Access: RO Mask Bits act as Write Enables for the bits[15:0] of this register.
	15	**Extra Bits15** Default Value: 0b Access: R/W Extra Bits for future use.
	14	**Extra Bits14** Default Value: 0b Access: R/W Extra Bits for future use.
	13	**Extra Bits13** Default Value: 0b Access: R/W Extra Bits for future use.
	12	**Extra Bits12** Default Value: 0b Access: R/W Extra Bits for future use.
	11	**Extra Bits11** Default Value: 0b Access: R/W Extra Bits for future use.
	10	**Extra Bits10** Default Value: 0b Access: R/W Extra Bits for future use.

PWRCTXSAVE - GAMW Power Context Save

	9	**Power Context Save Request** Default Value: 0b Access: R/W Power Context Save Bit[9] Power Context Save Request 1'b0: Power context save is not being requested (default). 1'b1: Power context save is being requested. Unit needs to self-clear this bit upon sampling. This bit is self clear.
	8:0	**Power Context Save Quad Word Credits** Default Value: 000000000b Access: R/W Power Context Save Bits[8:0] QWord Credits for Power Context Save Request An initial length packet is required per power context save session, but that packet does not consume a credit. See protocol description for more details. Minimum Credits = 1: Unit may send 1 QWord pair. Maximum Credits = 511: Unit may send 511 QWord pairs. A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Only valid with PWRCTX_SAVE_REQ (Bit9).

Gather Constants Not Consumed By RCS

GATHER_CONST_PRODUCE_COUNT - Gather Constants Not Consumed By RCS	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	0248Ch

This register keeps track of the outstanding Gather Constants produced by RS which are not yet consumed by Render Command Streamer. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0	31:0	**Gather Constants Produce Count** This register keeps track of the outstanding Gather Constants produced by RS which are not yet consumed by Render Command Streamer. This register is part of the render context save and restore.

GDR Per Client Write Drop Enables

WR_DROP_MODE - GDR Per Client Write Drop Enables

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	040B4h

DWord	Bit	Description
0	31:0	**GDR Per Client Write Drop Enables** Default Value: 00000000h Access: R/W 31 RSVD: Future use. 30 MBC write drop disable (0) or enable (1). 29 CS write drop disable (0) or enable (1). 28 SOL write drop disable (0) or enable (1). 27 RS write drop disable (0) or enable (1). 26 RCC write drop disable (0) or enable (1). 25 MSC write drop disable (0) or enable (1). 24 All L3 clients write drop disable (0) or enable (1). 23 STC write drop disable (0) or enable (1). 22 HIZ write drop disable (0) or enable (1). 21 RCZ write drop disable (0) or enable (1). 20 GAFS write drop disable (0) or enable (1). 19 GPM write drop disable (0) or enable (1). 18 GCP write drop disable (0) or enable (1). 17 VCS write drop disable (0) or enable (1). 16 BSP write drop disable (0) or enable (1). 15 VCR write drop disable (0) or enable (1). 14 VMX_RS write drop disable (0) or enable (1). 13 VMX_BS write drop disable (0) or enable (1). 12 VMX_RA write drop disable (0) or enable (1). 11 VMX_VDS write drop disable (0) or enable (1). 10 VLF_RS write drop disable (0) or enable (1). 9 VLF_FW write drop disable (0) or enable (1). 8 VECS write drop disable (0) or enable (1). 7 VEO write drop disable (0) or enable (1). 5 uC (DMA) write drop disable (0) or enable (1). 4 BCS write drop disable (0) or enable (1). 3 BLB write drop disable (0) or enable (1). 2 W_BSP write drop disable (0) or enable (1). 1 W_VMX_RS write drop disable (0) or enable (1). 0 W_VMX_BS write drop disable (0) or enable (1).

GDR Per Client Write Drop Enables-2

WR_DROP_MODE2 - GDR Per Client Write Drop Enables-2

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	040B8h

DWord	Bit	Description
0	31:0	**GDR Per Client Write Drop Enables-2** Default Value: 00000000h Access: R/W 31:23 RSVD: Future use. 22 BLB2 write drop disable (0) or enable (1). 21 HLF_FW write drop disable (0) or enable (1). 20 HLF_RS write drop disable (0) or enable (1). 19 HPP write drop disable (0) or enable (1). 18 HUC_DMA write drop disable (0) or enable (1). 17 HHI_IndirectHeader write drop disable (0) or enable (1). 16 HHI_Streamout write drop disable (0) or enable (1). 15 HHI_Bitstream write drop disable (0) or enable (1). 14 MFL_VLF_FW write drop disable (0) or enable (1). 13 MFL_VLF_RS write drop disable (0) or enable (1). 12 MFL_VMX_RA write drop disable (0) or enable (1). 11 MFL_VMX_RS write drop disable (0) or enable (1). 10 VD_ENC_SO write drop disable (0) or enable (1). 9 VD_ENC_RS write drop disable (0) or enable (1). 8 SFC_FW_VE write drop disable (0) or enable (1). 7 SFC_LB_VE write drop disable (0) or enable (1). 6 SFC_FW_VD write drop disable (0) or enable (1). 5 SFC_LB_VD write drop disable (0) or enable (1). 4 VOP write drop disable (0) or enable (1). 3 VDS write drop disable (0) or enable (1). 2 OA write drop disable (0) or enable (1). 1 VFE write drop disable (0) or enable (1). 0 VF write drop disable (0) or enable (1).

GDR Write Drop

GDR_WR_DRP - GDR Write Drop

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04020h

DWord	Bit	Description
0	31:0	**GDR_WRITE_DROP** Access: R/W Value: 00000000h — Name: **[Default]**

General Purpose Register1

CS_GPR - General Purpose Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64

Address:	02600h-02607h
Name:	General Purpose Register
ShortName:	CS_GPR_RCSUNIT

Address:	12600h-12607h
Name:	General Purpose Register
ShortName:	CS_GPR_VCSUNIT0

Address:	1A600h-1A607h
Name:	General Purpose Register
ShortName:	CS_GPR_VECSUNIT

Address:	1C600h-1C607h
Name:	General Purpose Register
ShortName:	CS_GPR_VCSUNIT1

Address:	22600h-22607h
Name:	General Purpose Register
ShortName:	CS_GPR_BCSUNIT

Description	Source
This is a General Purpose Register bank of sixteen 64bit registers, which will be used as temporary storage by MI_MATH command to do ALU operations.	

GPR Index	MMIO Offset	Source
R_0	0x2600	RenderCS
R_1	0x2608	
R_2	0x2610	
R_3	0x2618	
R_4	0x2620	
R_5	0x2628	
R_6	0x2630	
R_7	0x2638	
R_8	0x2640	
R_9	0x2648	

CS_GPR - General Purpose Register

R_10	0x2650
R_11	0x2658
R_12	0x2660
R_13	0x2668
R_14	0x2670
R_15	0x2678

DWord	Bit	Description
0	63:0	**CS_GPR_DATA** Source: CommandStreamer This register is a temporary register for ALU operations. See MI_MATH command for more details.

GFX Arbiter Client Priority Control

GFX_PRIO_CTRL - GFX Arbiter Client Priority Control

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x880A2D10
Size (in bits):	32
Address:	04A00h

DWord	Bit	Description
0	31:27	**Read Rstrm Max Reject** Default Value: 10001b Access: R/W
	26:21	**Extra Bits** Default Value: 000000b Access: R/W
	20:18	**sol_gam_priority** Default Value: 010b Access: R/W Client Priority Control Bits - Lowest Bit [18] is NOT Used.
	17:15	**veo_gam_priority** Default Value: 100b Access: R/W Client Priority Control Bits - Lowest Bit [15] is NOT Used.
	14:12	**vfw_gam_priority** Default Value: 010b Access: R/W Client Priority Control Bits - Lowest Bit [12] is NOT Used.
	11:9	**gapc_gam_c_priority** Default Value: 110b Access: R/W Client Priority Control Bits - Lowest Bit [9] is NOT Used.
	8:6	**gapc_gam_z_priority** Default Value: 100b Access: R/W Client Priority Control Bits - Lowest Bit [6] is NOT Used.

GFX_PRIO_CTRL - GFX Arbiter Client Priority Control

	5:3	**gapc_gam_l3_priority** Default Value: 010b Access: R/W Client Priority Control Bits - Lowest Bit [3] is NOT Used.
	2:0	**csrsvf_gam_priority** Default Value: 000b Access: R/W Client Priority Control Bits - Lowest Bit [0] is NOT Used.

GFX Context Element Descriptor (High Part)

GFX_CTX_EDR_H - GFX Context Element Descriptor (High Part)

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04404h

DWord	Bit	Description
0	31:0	**GFX Context Element Descriptor (High Part)** Default Value: 00000000h Access: R/W Bit[63:32] - Context ID: Context identification number assigned to separate this context from others. Context IDs need to be recycled in such a way that there cannot be two active contexts with the same ID. This is a unique identification number by which a context is identified and referenced.

GFX Context Element Descriptor (Low Part)

GFX_CTX_EDR_L - GFX Context Element Descriptor (Low Part)

Register Space:	MMIO: 0/2/0
Default Value:	0x00000009
Size (in bits):	32
Address:	04400h

DWord	Bit	Description
0	31:0	**GFX Context Element Descriptor (Low Part)** Default Value: 00000009h Access: R/W Bit[31:12] - LRCA: Command Streamer Only. Bit[8] - Privileged Context / GGTT vs PPGTT mode: Differs in legacy vs advanced context modes: In Legacy Context: Defines the page tables to be used. This is how page walker comes to know PPGTT vs GGTT selection for the entire context. 0: Use Global GTT. 1: Use Per-Process GTT. In Advanced Context: Defines the privilege level for the context. 0: User mode context. 1: Supervisor mode context. Bit[5] - Deeper IA coherency Support: In Advanced Context: Defines the level of IA coherency. 0: IA coherency is provided at LLC level for all streams of GPU (i.e. Gen7.5 like mode). 1: IA coherency is provided at L3 level for EU data accesses of GPU. Bit[4] - A and D Support / 32 and 64b Address Support: Differs in legacy vs advanced context modes: In Legacy Context: Defines 32b vs 64b (48b canonical) addressing format: 0: 32b addressing format. 1: 64b (48b canonical) addressing format. In Advanced Context: Defines A and D bit support: 0: A and D bit management in page tables is NOT supported. 1: A and D bit management in page tables is supported. Bit[3] - Context Type: Legacy vs Advanced: Defines the context type 0: Advanced Context: Defines the rest of the advanced capabilities (i.e. OS page table support, fault models). Note that advanced context is not bounded to GPGPU. 1: Legacy Context: Defines the context as legacy mode which is similar to prior generations of Gen8. Note that: Bits [8:4] differs in functions when legacy vs advanced context modes are selected. Bit[2] - FR: Command streamer specific. Bit[1] - Scheduling Mode: 1: Indicates execlist mode of scheduling.

GFX_CTX_EDR_L - GFX Context Element Descriptor (Low Part)		
		0: Indicates Ring Buffer mode of scheduling. Bit[0] - Valid: Indicates that element descriptor is valid. If GAM is programmed with an invalid descriptor, it continues but flags an error.

GFX Context Element Descriptor (Low Part)

GFX_CTX_EDR_L - GFX Context Element Descriptor (Low Part)

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000009
Size (in bits):	32
Address:	04400h

DWord	Bit	Description
0	31:0	**GFX Context Element Descriptor** Default Value: 00000009h Access: R/W Bit[31:12] - LRCA: Command Streamer Only. Bit[8] - Privileged Context / GGTT vs PPGTT mode: Differs in legacy vs advanced context modes: In Legacy Context: Defines the page tables to be used. This is how page walker comes to know PPGTT vs GGTT selection for the entire context. 0: Use Global GTT. 1: Use Per-Process GTT. In Advanced Context: Defines the privilege level for the context. 0: User mode context. 1: Supervisor mode context. Bit[7:6] - Reserved: 00b: Reserved 01b: Reserved 10b: Reserved 11b: Reserved Bit[5] - Deeper IA coherency Support: In Advanced Context: Defines the level of IA coherency. 0: IA coherency is provided at LLC level for all streams of GPU (i.e. Gen7.5 like mode). 1: IA coherency is provided at L3 level for EU data accesses of GPU. Bit[4] - A and D Support / 32 and 64b Address Support: Differs in legacy vs advanced context modes: In Legacy Context: Defines 32b vs 64b (48b canonical) addressing format: 0: 32b addressing format. 1: 64b (48b canonical) addressing format. In Advanced Context: Defines A and D bit support: 0: A and D bit management in page tables is NOT supported. 1: A and D bit management in page tables is supported. Bit[3] - Context Type: Legacy vs Advanced: Defines the context type 0: Advanced Context: Defines the rest of the advanced capabilities (i.e. OS page table support, fault models). Note that advanced context is not bounded to GPGPU.

GFX_CTX_EDR_L - GFX Context Element Descriptor (Low Part)

		1: Legacy Context: Defines the context as legacy mode which is similar to prior generations of Gen8. Note that: Bits [8:4] differs in functions when legacy vs advanced context modes are selected. Bit[2] - FR: Command streamer specific.
		Bit[1] - Scheduling Mode: 1: Indicates execlist mode of scheduling. 0: Indicates Ring Buffer mode of scheduling. Bit[0] - Valid: Indicates that element descriptor is valid. If GAM is programmed with an invalid descriptor, it continues but flags an error.

GFX Fault Counter

GFX_FAULT_CNTR - GFX Fault Counter		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	045A0h	
DWord	**Bit**	**Description**
0	31:0	**GFX Fault Counter** Default Value: 00000000h Access: RO This counter only applies to advance context when fault and stream mode is selected.

GFX Fixed Counter

GFX_FIXED_CNTR - GFX Fixed Counter

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	045A4h

DWord	Bit	Description
0	31:0	**GFX Fixed Counter** Default Value: 00000000h Access: RO This counter only applies to advance context when fault and stream mode is selected.

GFX PDP0/PML4/PASID Descriptor (High Part)

GFX_CTX_PDP0_H - GFX PDP0/PML4/PASID Descriptor (High Part)

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0440Ch

DWord	Bit	Description
0	31:0	**GFX PDP0/PML4/PASID Descriptor (High Part)** Default Value: 00000000h Access: R/W PDP0/PML4/PASID: This register can contain three values which depend on the element descriptor definition. PASID[19:0]: Populated in the first 20bits of the register and selected when Advanced Context flag is set. PML4[38:12]: Pointer to base address of PML4 and selected when Legacy Context flag is set and 64b address support is selected. PDP0[38:12]: Pointer to one of the four page directory pointer (lowest) and defines the first 0-1GB of memory mapping. Note: This is a guest physical address.

GFX PDP0/PML4/PASID Descriptor (Low Part)

GFX_CTX_PDP0_L - GFX PDP0/PML4/PASID Descriptor (Low Part)

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04408h

DWord	Bit	Description
0	31:0	**GFX PDP0/PML4/PASID Descriptor (Low Part)** Default Value: 00000000h Access: R/W PDP0/PML4/PASID: This register can contain three values which depend on the element descriptor definition. PASID[19:0]: Populated in the first 20 bits of the register and selected when Advanced Context flag is set. PML4[38:12]: Pointer to base address of PML4 and selected when Legacy Context flag is set and 64b address support is selected. PDP0[38:12]: Pointer to one of the four page directory pointer (lowest) and defines the first 0-1GB of memory mapping. Note: This is a guest physical address.

GFX PDP1 Descriptor Register (High Part)

GFX_CTX_PDP1_H - GFX PDP1 Descriptor Register (High Part)

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04414h

DWord	Bit	Description
0	31:0	**GFX PDP1 Descriptor Register (High Part)** Default Value: 00000000h Access: R/W Pointer to one of the four page directory pointer (lowest+1) and defines the first 1-2GB of memory mapping. Note: This is a guest physical address.

GFX PDP1 Descriptor Register (Low Part)

GFX_CTX_PDP1_L - GFX PDP1 Descriptor Register (Low Part)

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04410h

DWord	Bit	Description
0	31:0	**GFX PDP1 Descriptor Register (Low Part)** Default Value: 00000000h Access: R/W Pointer to one of the four page directory pointer (lowest+1) and defines the first 1-2GB of memory mapping. Note: This is a guest physical address.

GFX PDP2 Descriptor Register (High Part)

GFX_CTX_PDP2_H - GFX PDP2 Descriptor Register (High Part)

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0441Ch

DWord	Bit	Description
0	31:0	**GFX PDP2 Descriptor Register (High Part)** Default Value: 00000000h Access: R/W Pointer to one of the four page directory pointer (lowest+2) and defines the first 2-3GB of memory mapping. Note: This is a guest physical address.

GFX PDP2 Descriptor Register (Low Part)

GFX_CTX_PDP2_L - GFX PDP2 Descriptor Register (Low Part)

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04418h

DWord	Bit	Description
0	31:0	**GFX PDP2 Descriptor Register (Low Part)** Default Value: 00000000h Access: R/W Pointer to one of the four page directory pointer (lowest+2) and defines the first 2-3GB of memory mapping. Note: This is a guest physical address.

GFX PDP3 Descriptor Register (High Part)

GFX_CTX_PDP3_H - GFX PDP3 Descriptor Register (High Part)

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04424h

DWord	Bit	Description
0	31:0	**GFX PDP3 Descriptor Register (High Part)** Default Value: 00000000h Access: R/W Pointer to one of the four page directory pointer (lowest+3) and defines the first 3-4GB of memory mapping. Note: This is a guest physical address.

GFX PDP3 Descriptor Register (Low Part)

GFX_CTX_PDP3_L - GFX PDP3 Descriptor Register (Low Part)

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04420h

DWord	Bit	Description
0	31:0	**GFX PDP3 Descriptor Register (Low Part)** Default Value: 00000000h Access: R/W Pointer to one of the four page directory pointer (lowest+3) and defines the first 3-4GB of memory mapping. Note: This is a guest physical address.

Global Invalidation Register

GLBLINVL - Global Invalidation Register		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B404h	
DWord	**Bit**	**Description**
0	31:3	**Reserved** Access: RO Reserved.
	2	**Cross sync read disable** Access: R/W lpconf_crs_sync_dis: Cross Sync Read Disable (CSRD). Cross Sync Read Disable (CSRD): Cross Sync Read Disable: upon a SYNC from HDC, follow with a write to cross SYNC Push and read to the same address. When set read is disabled. In SKL, this bit needs to be programmed to 1 to disable fence operation for GSYNC. This is a workaround for GSYNC fence cycle encountering page fault.
	1	**Disables hashing function** Access: R/W Disables hashing function (DISHHF): Disables hashing function to generate bank_id[1:0] for L3$ bank accessing, and forces the use of address[7:6] for bank_id[1:0]. 0: (default) Hash function enabled to generate L3$ bank IDs. 1: L3$ address[7:6] used as L3$ bank IDs. lpconf_csr_l3bankidhashdis. (This bit needs to set corresponding bit lncf_csr_l3bankidhashdis in LNCF.)
	0	**Reserved**

Global System Interrupt Routine

EU_GLOBAL_SIP - Global System Interrupt Routine

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0E42Ch

DWord	Bit	Description
0	31:3	**Global SIP** Format: GraphicsAddress[31:3] Specifies the base address for System Interrupt Routine that over-rides the SIP set by the state (STATE_SIP).
	2:1	**Reserved** Format: MBZ
	0	**Global SIP Enable** The bit specifies if the System Routine starts from the Global SIP provided by the DW OR the SIP provided by the state (STATE_SIP) Value / Name: 0 – SIP used is from STATE_EIP 1 – SIP used is from MMIO register

GMBUS0

GMBUS0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	C5100h-C5103h
Name:	GMBUS0 Clock/Port Select
ShortName:	GMBUS0
Power:	Always on
Reset:	soft

The GMBUS0 register controls the clock rate of the serial bus and the device the controller is connected to. This register should be configured before the first data valid bit is set.

DWord	Bit	Description
0	31:12	**Reserved** Format: MBZ
	11	**Reserved**
	10:8	**GMBUS Rate Select** These two bits select the rate that the GMBUS will run at. It also defines the AC timing parameters used. Value / Name: 000b: 100 KHz 001b: 50 KHz Others: Reserved Restriction: It should only be changed between transfers when the GMBUS is idle.
	7:3	**Reserved** Format: MBZ
	2:0	**Pin Pair Select** This field selects a GMBUS pin pair for use in the GMBUS communication. See the table of GPIO Pin Usages to determine which pin pairs are supported and their intended functions. Value / Name: 000b: None (Disabled) 100b: DDIC 101b: DDIB 110b: DDID

GMBUS1

GMBUS1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W Protect
Size (in bits):	32
Address:	C5104h-C5107h
Name:	GMBUS1 Command/Status
ShortName:	GMBUS1
Power:	Always on
Reset:	soft

This register lets the software indicate to the GMBUS controller the slave device address, register index, and indicate when the data write is complete. When the SW_CLR_INT bit is asserted, all writes to the GMBUS2, GMBUS3, and GMBUS4 registers are discarded. The GMBUS1 register writes to any other bit except the SW_CLR_INT are also lost. Reads to these registers always work normally regardless of the state of the SW_CLR_INT bit.

DWord	Bit	Description
0	31	**Software Clear Interrupt** Access: R/W (SW_CLR_INT) This bit must be clear for normal operation. Setting the bit then clearing it acts as local reset to the GMBUS controller. This bit is commonly used by software to clear a BUS_ERROR when a slave device delivers a NACK. **Value** / **Name** / **Description** 0b / Clear HW_RDY / If this bit is written as a zero when its current state is a one, will clear the HW_RDY bit and allows register writes to be accepted to the GMBUS registers (Write Protect Off). This bit is cleared to zero when an event causes the HW_RDY bit transition to occur. 1b / Assert HW_RDY / Asserted by software after servicing the GMBUS interrupt. Setting this bit causes the INT status bit to be cleared. Setting (1) this bit also asserts the HW_RDY bit (until this bit is written with a 0). When this bit is set, no writes to GMBUS registers will cause the contents to change with the exception of this bit which can be written.
	30	**Software Ready** (SW_RDY) Data handshake bit used in conjunction with HW_RDY bit. **Value** / **Name** / **Description** 0b / De-Assert / De-asserted via the assertion event for HW_RDY bit 1b / SW Assert / When asserted by software, results in de-assertion of HW_RDY bit

GMBUS1

29 Enable Timeout

(ENT) Enables timeout for slave response. When this bit is enabled and the slave device response has exceeded the timeout period, the GMBUS Slave Stall Timeout Error interrupt bit is set.

Value	Name
0b	Disable
1b	Enable

28 Reserved

Format:	MBZ

27:25 Bus Cycle Select

GMBUS cycle will always consist of a START followed by Slave Address, followed by an optional read or write data phase. A read cycle with an index will consist of a START followed by a Slave Address a WRITE indication and the INDEX and then a RESTART with a Slave Address and an optional read data phase. The GMBUS cycle will terminate either with a STOP or by entering a wait state. The WAIT state is exited by generating a STOP or by starting another GMBUS cycle. This can only cause a STOP to be generated if a GMBUS cycle is generated, the GMBUS is currently in a data phase, or it is in a WAIT phase. The three bits can be decoded as follows: 27 = STOP generated 26 = INDEX used 25 = Cycle ends in a WAIT

Value	Name	Description
000b	No cycle	No GMBUS cycle is generated
001b	No Index, No Stop, Wait	GMBUS cycle is generated without an INDEX, with no STOP, and ends with a WAIT
010b	Reserved	Reserved
011b	Index, No Stop, Wait	GMBUS cycle is generated with an INDEX, with no STOP, and ends with a WAIT
100b	Gen Stop	Generates a STOP if currently in a WAIT or after the completion of the current byte if active
101b	No Index, Stop	GMBUS cycle is generated without an INDEX and with a STOP
110b	Reserved	Reserved
111b	Index, Stop	GMBUS cycle is generated with an INDEX and with a STOP

24:16 Total Byte Count

This determines the total number of bytes to be transferred during the DATA phase of a GMBUS cycle. The DATA phase can be prematurely terminated by generating a STOP while in the DATA phase (see Bus Cycle Select).

Restriction
Do not change the value of this field during GMBUS cycles transactions. The byte count must not be zero.

GMBUS1

	15:8	**8 bit Slave Register Index** (INDEX) This field specifies the 8-bits of index to be used for the generated bus write transaction or the index used for the WRITE portion of the WRITE/READ pair. It only has an effect if the enable Index bit is set. **Restriction** Do not change the value of this field during GMBUS cycles transactions.
	7:0	**Slave Address And Direction** Bits 7:1 = 7-bit GMBUS Slave Address (SADDR): When a GMBUS cycle is to be generated using the Bus Cycle Select field, this field specifies the value of the slave address that is to be sent out. For use with 10-bit slave address devices, set this value to 11110XXb (where the last two bits (XX) are the two MSBs of the 10-bit address) and the slave direction bit to a write. This is followed by the first data byte being the 8 LSBs of the 10-bit slave address. Bit 0 = Slave Direction Bit: When a GMBUS cycle is to be generated based on the Bus Cycle Select, this bit determines if the operation will be a read or a write. A read operation with the index enabled will perform a write with just the index followed by a re-start and a read. A 1 indicates that a Read from the slave device operation is to be performed. A 0 indicates that a Write to the slave device operation is to be performed.

Value	Name
00000001b	General Call Address
00000000b	Start Byte
0000001Xb	CBUS Address
11110XXXb	10-Bit Addressing
Others	Reserved

GMBUS2

GMBUS2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000800
Access:	R/W Protect
Size (in bits):	32
Address:	C5108h-C510Bh
Name:	GMBUS2 Status
ShortName:	GMBUS2
Power:	Always on
Reset:	soft

When the SW_CLR_INT bit is asserted, all writes to this registet are discarded. Reads to this register always work normally regardless of the state of the SW_CLR_INT bit.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15	**INUSE** Software wishing to arbitrate for the GMBUS resource can poll this bit until it reads a zero and will then own usage of the GMBUS controller. This bit has no effect on the hardware, and is only used as semaphore among various independent software threads. Writing a one to this bit is software's indication that the software use of this resource is now terminated and it is available for other clients.
	14	**Hardware Wait Phase** Access: RO Once in a WAIT_PHASE, the software can now choose to generate a STOP cycle or a repeated start (RESTART) cycle followed by another GMBUS transaction. Wait phase is entered at the end of the current transaction when that transaction is selected not to terminate with a STOP.

Value	Name	Description
0b	GMBUS is Acquired	Read operation that contains a zero in this bit position indicates that the GMBUS engine is now acquired and the subsequent reads of this register will now have this bit set. Writing a 0 to this bit has no effect.
1b	GMBUS in Use	Read operation that contains a one for this bit indicates that the GMBUS is currently allocated to someone else and "In use". Once set, a write of a 1 to this bit indicates that the software has relinquished the GMBUS resource and will reset the value of this bit to a 0.

Value	Name
0b	Not in a wait phase
1b	In wait phase

GMBUS2

13 **Slave Stall Timeout Error**

Access:	RO

This bit indicates that a slave stall timeout has occurred. It is tied to the Enable Timeout (ENT) bit.

Value	Name
0b	No Slave Timeout
1b	Slave Timeout

12 **GMBUS Interrupt Status**

Access:	RO

This bit indicates that an event that causes a GMBUS interrupt has occurred. The interrupt can be caused by one of the interrupt types enabled in the GMBUS4 register

Value	Name
0b	No Interrupt
1b	Interrupt

11 **Hardware Ready**

Access:	RO

(HW_RDY) This provides a method of detecting when the current software client routine can proceed with the next step in a sequence of GMBUS operations. This data handshake bit is used in conjunction with the SW_RDY bit. When this bit is asserted by the GMBUS controller, it results in the de-assertion of the SW_RDY bit. This bit resumes to normal operation when the SW_CLR_INT bit is written to a 0.

Value	Name	Description
0b	0	Condition required for assertion has not occurred or when this bit is a one and: - SW_RDY bit has been asserted - During a GMBUS read transaction, after the each read of the data register - During a GMBUS write transaction, after each write of the data register - SW_CLR_INT bit has been cleared
1b	1 **[Default]**	This bit is asserted under the following conditions: - After a reset or when the transaction is aborted by the setting of the SW_CLR_INT bit - When an active GMBUS cycle has terminated with a STOP - When during a GMBUS write transaction, the data register needs and can accept another four bytes of data - During a GMBUS read transaction, this bit is asserted when the data register has four bytes of new data or the read transaction DATA phase is complete and the data register contains the last few bytes of the read data

10 **NAK Indicator**

Access:	RO

MAK is indicated by hardware if any expected device acknowledge is not received from the slave within the timeout.

Value	Name
0b	No bus error
1b	NAK occurred

GMBUS2

	9	**GMBUS Active** Access: RO (GA) This is a status bit that indicates whether the GMBUS controller is in an IDLE state or not. Active states are the START, ADDRESS, INDEX, DATA, WAIT, or STOP Phase. **Value** / **Name** 0b – Idle 1b – Active
	8:0	**Current Byte Count** Access: RO Can be used to determine the number of bytes currently transmitted/received by the GMBUS controller hardware. Hardware sets it to zero at the start of a GMBUS transaction data transfer and incremented after the completion of each byte of the data phase. Note that because reads have internal storage, the byte count on a read operation may be ahead of the data that has been accepted from the data register.

GMBUS3

GMBUS3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W Protect
Size (in bits):	32
Double Buffer Update Point:	HW_RDY
Address:	C510Ch-C510Fh
Name:	GMBUS3 Data Buffer
ShortName:	GMBUS3
Power:	Always on
Reset:	soft

This is the data read/write register. This register is double buffered. Bit 0 is the first bit sent or read, bit 7 is the 8th bit sent or read, all the way through bit 31 being the 32nd bit sent or read. For GMBUS write operations with a non-zero byte count, this register should be written with the data before the GMBUS cycle is initiated. For byte counts that are greater than four bytes, this register will be written with subsequent data only after the HW_RDY status bit is set indicating that the register is now ready for additional data. For GMBUS read operations, software should wait until the HW_RDY bit indicates that the register contains the next set of valid read data before reading this register. When the SW_CLR_INT bit is asserted, all writes to this registet are discarded. Reads to this register always work normally regardless of the state of the SW_CLR_INT bit.

DWord	Bit	Description
0	31:24	**Data Byte 3**
	23:16	**Data Byte 2**
	15:8	**Data Byte 1**
	7:0	**Data Byte 0**

GMBUS4

GMBUS4

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W Protect
Size (in bits):	32
Address:	C5110h-C5113h
Name:	GMBUS4 Interrupt Mask
ShortName:	GMBUS4
Power:	Always on
Reset:	soft

When the SW_CLR_INT bit is asserted, all writes to this registet are discarded. Reads to this register always work normally regardless of the state of the SW_CLR_INT bit.

DWord	Bit	Description
0	31:5	**Reserved** Format: MBZ
	4:0	**Interrupt Mask** This field specifies which GMBUS interrupts events may contribute to the setting of GMBUS interrupt status bit in the second level interrupt status register. For writes, the HW Ready (HWRDY) interrupt indicates that software can write the next DWORD. It does NOT mean that the transfer of data to the slave device has completed. The IDLE or HW wait interrupt may be used to detect the end of writing data to the slave device. The HWRDY interrupt may be used for gmbus write cycles only to detect when to write the next DWORD after the first two DWORDs have been written to GMBUS3. For reads, the HWRDY interrupt indicates the arrival of the next dword.

Value	Name
0XXXXb	Slave Stall Timeout Interrupt Disable
1XXXXb	Slave Stall Timeout Interrupt Enable
X0XXXb	NAK Interrupt Disable
X1XXXb	NAK Interrupt Enable
XX0XXb	Idle Interrupt Disable
XX1XXb	Idle Interrupt Enable
XXX0Xb	HW Wait Interrupt (cycle without a stop has completed) Disable
XXX1Xb	W Wait Interrupt (cycle without a stop has completed) Enable
XXXX0b	HW Ready (Data transferred) Interrupt Disable
XXXX1b	HW Ready (Data transferred) Interrupt Enable

GMBUS5

GMBUS5		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	C5120h-C5123h	
Name:	GMBUS5 2 Byte Index	
ShortName:	GMBUS5	
Power:	Always on	
Reset:	soft	

This register provides a method for the software indicate to the GMBUS controller the 2 byte device index.

DWord	Bit	Description
0	31	**2 Byte Index Enable** When this bit is asserted (1), then bits 15:0 are used as the index. Bits 15:8 are used in the first byte which is the most significant index bits. The slave index in the GMBUS1<15:8> are ignored. Bits 7:0 are used in the second byte which is the least significant index bits.
	30:16	**Reserved** Format: MBZ
	15:0	**2 Byte Slave Index** This is the 2 byte index used in all GMBUS accesses when bit 31 is asserted (1).

GMCH Graphics Control

GGC_0_0_0_PCI - GMCH Graphics Control

Register Space:	PCI: 0/0/0
Source:	BSpec
Default Value:	0x00000500
Size (in bits):	16
Address:	00050h

All the bits in this register are LT lockable.

DWord	Bit	Description
0	15:8	**Graphics Mode Select** Default Value: 00000101b Access: R/W Lock This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled. BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0. BIOS Requirement: Given new sizes allow down to 8MB allocation, BIOS has to ensure there is sufficient space for WOPCM and basic GFX Stolen functions. 00h:0MB 01h:32MB 02h:64MB 03h:96MB 04h:128MB 05h:160MB (default) 06h:192MB 07h:224MB 08h:256MB 09h:288MB 0Ah:320MB 0Bh:352MB 0Ch:384MB 0Dh:416MB 0Eh:448MB 0Fh:480MB 10h:512MB 11h - 1Fh: Reserved 20h:1024MB 21h - 2Fh: Reserved 30h:1536MB 31h - 3Fh: Reserved 40h: 2048MB 41h - EFh: Reserved

GGC_0_0_0_PCI - GMCH Graphics Control

		F0h: 4MB F1h: 8MB F2h: 12MB F3h: 16MB F4h: 20MB F5h: 24MB F6h: 28MB F7h: 32MB F8h: 36MB F9h: 40MB FAh: 44MB FBh: 48MB FCh: 52MB FDh: 56MB FEh: 60MB FFh: Reserved Hardware functionality in case of programming this value to Reserved is not guaranteed.
	7:6	**GTT Graphics Memory Size** Default Value: 00b Access: R/W Lock This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware will derive the base of GSM from DSM only using the GSM size programmed in the register. Hardware functionality in case of programming this value to Reserved is not guaranteed. 0x0: No Preallocated Memory 0x1: 2MB of Preallocated Memory 0x2: 4MB of Preallocated Memory 0x3: 8MB of Preallocated Memory
	5:3	**Reserved** Format: MBZ
	2	**Versatile Acceleration Mode Enable** Default Value: 0b Access: R/W Lock Enables the use of the iGFX engines for Versatile Acceleration. 0 - iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h. 1 - iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 048000h.

GGC_0_0_0_PCI - GMCH Graphics Control

	1	**IGD VGA Disable** Default Value: 0b Access: R/W Lock 0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub- Class Code field within Device 2 function 0 Class Code register is 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field pre-allocates no memory. This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override (CAPID0_A[IGD] = 1) or via a register (DEVEN[3] = 0).
	0	**GGC Lock** Default Value: 0b Access: R/W Key Lock When set to 1b, this bit will lock all bits in this register.

Go Protocol GAM Request

GO_GAM_REQ - Go Protocol GAM Request

Register Space: MMIO: 0/2/0
Default Value: 0x00000000
Size (in bits): 32

Address: 040D0h

DWord	Bit	Description
0	31:16	**Mask Bits** Default Value: 0000h Access: RO Reserved.
	15	**GO_PROTOCOL_GAM_REQUEST15** Default Value: 0b Access: R/W Go Protocol Request Reasons: 1'b0: Engine will NOT be resetting. 1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset). Preparation for FLR (device) reset (cdevrst_b).
	14	**GO_PROTOCOL_GAM_REQUEST14** Default Value: 0b Access: R/W Go Protocol Request Reasons: 1'b0: Engine will NOT be resetting. 1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset). Preparation for Media1 reset (vcs1unit).
	13	**GO_PROTOCOL_GAM_REQUEST13** Default Value: 0b Access: R/W Go Protocol Request Reasons: 1'b0: Engine will NOT be resetting. 1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset). Preparation for Wi-Di reset (winunit).

GO_GAM_REQ - Go Protocol GAM Request

	12	**GO_PROTOCOL_GAM_REQUEST12** Default Value: 0b Access: R/W Go Protocol Request Reasons: 1'b0: Engine will NOT be resetting. 1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset).
	11	**GO_PROTOCOL_GAM_REQUEST11** Default Value: 0b Access: R/W Go Protocol Request Reasons: 1'b0: Engine will NOT be resetting. 1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset). Preparation for Blitter reset (bcsunit).
	10	**GO_PROTOCOL_GAM_REQUEST10** Default Value: 0b Access: R/W Go Protocol Request Reasons: 1'b0: Engine will NOT be resetting. 1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset). Preparation for VEBox reset (vecsunit).
	9	**GO_PROTOCOL_GAM_REQUEST9** Default Value: 0b Access: R/W Go Protocol Request Reasons: 1'b0: Engine will NOT be resetting. 1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset). Preparation for Media0 reset (vcs0unit).
	8	**GO_PROTOCOL_GAM_REQUEST8** Default Value: 0b Access: R/W Go Protocol Request Reasons: 1'b0: Engine will NOT be resetting. 1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset). Preparation for Render reset (csunit).

GO_GAM_REQ - Go Protocol GAM Request

	7	**GO_PROTOCOL_GAM_REQUEST7** Default Value: 0b Access: R/W GPM to GAM Go Protocol Request. 0: No graphic cycles allowed to memory (default). 1: Allow graphic cycles to memory. Controls OA Cycles (oaunit). GPM currently only ever sends the same GO request for all agents; either all is go=0, or all is go=1.
	6	**GO_PROTOCOL_GAM_REQUEST6** Default Value: 0b Access: R/W GPM to GAM Go Protocol Request. 0: No graphic cycles allowed to memory (default). 1: Allow graphic cycles to memory. Controls Wi-Di Cycles (winunit). GPM currently only ever sends the same GO request for all agents; either all is go=0, or all is go=1.
	5	**Reserved**
	4	**GO_PROTOCOL_GAM_REQUEST4** Default Value: 0b Access: R/W GPM to GAM Go Protocol Request. 0: No graphic cycles allowed to memory (default). 1: Allow graphic cycles to memory. Controls Blitter Cycles (bcsunit). GPM currently only ever sends the same GO request for all agents; either all is go=0, or all is go=1.
	3	**GO_PROTOCOL_GAM_REQUEST3** Default Value: 0b Access: R/W GPM to GAM Go Protocol Request. 0: No graphic cycles allowed to memory (default). 1: Allow graphic cycles to memory. Controls VEBox Cycles (vecsunit). GPM currently only ever sends the same GO request for all agents; either all is go=0, or all is go=1.

GO_GAM_REQ - Go Protocol GAM Request

	2	**GO_PROTOCOL_GAM_REQUEST2** Default Value: 0b Access: R/W GPM to GAM Go Protocol Request. 0: No graphic cycles allowed to memory (default). 1: Allow graphic cycles to memory. Controls Media1 Cycles (vcs1unit). GPM currently only ever sends the same GO request for all agents; either all is go=0, or all is go=1.
	1	**GO_PROTOCOL_GAM_REQUEST1** Default Value: 0b Access: R/W GPM to GAM Go Protocol Request. 0: No graphic cycles allowed to memory (default). 1: Allow graphic cycles to memory. Controls Media0 Cycles (vcs0unit). GPM currently only ever sends the same GO request for all agents; either all is go=0, or all is go=1.
	0	**GO_PROTOCOL_GAM_REQUEST0** Default Value: 0b Access: R/W GPM to GAM Go Protocol Request. 0: No graphic cycles allowed to memory (default). 1: Allow graphic cycles to memory. Controls Render Cycles (csunit). GPM currently only ever sends the same GO request for all agents; either all is go=0, or all is go=1.

GPA to HPA Translation Request

GPA2HPAR - GPA to HPA Translation Request

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0420Ch

DWord	Bit	Description
0	31:16	**Mask Bits** Default Value: 0000h Access: RO Mask Bits act as Write Enables for the bits[15:0] of this register.
	15	**GPA to HPA Translation Request 15** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	14	**GPA to HPA Translation Request 14** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	13	**GPA to HPA Translation Request 13** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	12	**GPA to HPA Translation Request 12** Default Value: 0b Access: R/W For Future Use. This bit is self clear.

GPA2HPAR - GPA to HPA Translation Request

	11	**GPA to HPA Translation Request 11** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	10	**GPA to HPA Translation Request 10** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	9	**GPA to HPA Translation Request 9** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	8	**GPA to HPA Translation Request 8** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	7	**GPA to HPA Translation Request 7** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	6	**GPA to HPA Translation Request 6** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	5	**GPA to HPA Translation Request 5** Default Value: 0b Access: R/W For Future Use. This bit is self clear.

GPA2HPAR - GPA to HPA Translation Request

	4	**GPA to HPA Translation Request 4** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	3	**GPA to HPA Translation Request 3** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	2	**GPA to HPA Translation Request 2** Default Value: 0b Access: R/W Bit[2]: A request for GPA to HPA translation. Note that GPA register should have been written prior to sending the message for the translation. Mask bit[18] needs to be enabled to program the register. This bit is self clear.
	1	**GPA to HPA Translation Request 1** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	0	**GPA to HPA Translation Request 0** Default Value: 0b Access: R/W For Future Use. This bit is self clear.

GPA value for GPA to HPA Translation

GPA2HPAV - GPA value for GPA to HPA Translation		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04210h	
DWord	**Bit**	**Description**
0	31:0	**GPA value for GPA to HPA Translation** Default Value: 00000000h Access: R/W The GPA value of the page that requires the GPA=>HPA translation bits[39:12] map to [28:1] of the register.

GPGPU Context Restore Request To TDL

GPGPU_CTX_RESTORE - GPGPU Context Restore Request To TDL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	WO
Size (in bits):	32
Address:	0E4CCh
Name:	GPGPU Context Restore Request To TDL Slice 0 SubSlice 0
ShortName:	GPGPU_CTX_RESTORE_S0_SS0
Valid Projects:	SKL
Address:	0E5CCh
Name:	GPGPU Context Restore Request To TDL Slice 0 SubSlice 1
ShortName:	GPGPU_CTX_RESTORE_S0_SS1
Valid Projects:	SKL
Address:	0E6CCh
Name:	GPGPU Context Restore Request To TDL Slice 0 SubSlice 2
ShortName:	GPGPU_CTX_RESTORE_S0_SS2
Valid Projects:	SKL
Address:	0E4DCh
Name:	GPGPU Context Restore Request To TDL Slice 1 SubSlice 0
ShortName:	GPGPU_CTX_RESTORE_S1_SS0
Valid Projects:	SKL
Address:	0E5DCh
Name:	GPGPU Context Restore Request To TDL Slice 1 SubSlice 1
ShortName:	GPGPU_CTX_RESTORE_S1_SS1
Valid Projects:	SKL
Address:	0E6DCh
Name:	GPGPU Context Restore Request To TDL Slice 1 SubSlice 2
ShortName:	GPGPU_CTX_RESTORE_S1_SS2
Valid Projects:	SKL
Address:	0E4ECh
Name:	GPGPU Context Restore Request To TDL Slice 2 SubSlice 0
ShortName:	GPGPU_CTX_RESTORE_S2_SS0
Valid Projects:	SKL
Address:	0E5ECh

GPGPU_CTX_RESTORE - GPGPU Context Restore Request To TDL

Name:	GPGPU Context Restore Request To TDL Slice 2 SubSlice 1
ShortName:	GPGPU_CTX_RESTORE_S2_SS1
Valid Projects:	SKL

Address:	0E6ECh
Name:	GPGPU Context Restore Request To TDL Slice 2 SubSlice 2
ShortName:	GPGPU_CTX_RESTORE_S2_SS2
Valid Projects:	SKL

DWord	Bit	Description
0	31:0	**Reserved** Format: MBZ

GPGPU Context Save Request To TDL

GPGPU_CTX_SAVE - GPGPU Context Save Request To TDL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	WO
Size (in bits):	32
Address:	0E4D8h
Valid Projects:	

DWord	Bit	Description
0	31:0	**Reserved** Format: MBZ

GPGPU Dispatch Dimension X

GPGPU_DISPATCHDIMX - GPGPU Dispatch Dimension X		
Register Space:	MMIO: 0/2/0	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02500h	
DWord	**Bit**	**Description**
0	31:0	**Dispatch Dimension X** Format: U32 The number of thread groups to be dispatched in the X dimension (max x + 1). **Value** / **Name** 0, FFFFFFFFh

GPGPU Dispatch Dimension Y

GPGPU_DISPATCHDIMY - GPGPU Dispatch Dimension Y

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02504h

DWord	Bit	Description
0	31:0	**Dispatch Dimension Y** Format: U32 The number of thread groups to be dispatched in the Y dimension (max y + 1 Value: 0, FFFFFFFFh — Name:

GPGPU Dispatch Dimension Z

GPGPU_DISPATCHDIMZ - GPGPU Dispatch Dimension Z		
Register Space:	MMIO: 0/2/0	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02508h	
DWord	**Bit**	**Description**
0	31:0	**Dispatch Dimension Z** Format: U32 The number of thread groups to be dispatched in the Zdimension (max Z + 1) **Value** / **Name** 0, FFFFFFFFh

GPIO_CTL

GPIO_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000808
Access:	R/W
Size (in bits):	32
Address:	C501Ch-C501Fh
Name:	GPIO Control 3
ShortName:	GPIO_CTL_3
Power:	Always on
Reset:	soft
Address:	C5020h-C5023h
Name:	GPIO Control 4
ShortName:	GPIO_CTL_4
Power:	Always on
Reset:	soft
Address:	C5024h-C5027h
Name:	GPIO Control 5
ShortName:	GPIO_CTL_5
Power:	Always on
Reset:	soft

The register controls a pair of pins that can be used for general purpose control, but usually is designated for specific functions according to the requirements of the device and the system that the device is in. Each pin of the two pin pair is designated as a clock or data for descriptive purposes. See the table at the beginning of this section to determine which pins/registers are supported and their intended functions. Board design variations are possible and would affect the usage of these pins. There are multiple instances of this register to support each of the GPIO pin pairs.

DWord	Bit	Description
0	31:13	**Reserved** Format: MBZ
	12	**GPIO Data In** Default Value: Ub Undefined (read only depends on I/O pin) Access: RO This is the value that is sampled on the GPIO_Data pin as an input. This bit is undefined at reset.

GPIO_CTL

11 GPIO Data Value

Default Value:	1b
Access:	R/W

This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if GPIO DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Data DIRECTION VALUE contains a value that will configure the pin as an output. The default of '1' mimics the I2C external pull-ups.

10 GPIO Data Mask

Access:	WO

This is a mask bit to determine whether the GPIO DATA VALUE bit should be written into the register.

Value	Name
0b	Dot NOT write
1b	Write

9 GPIO Data Direction Value

Access:	R/W

This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if GPIO Data DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO DATA VALUE bit.

Value	Name
0b	Input
1b	Output

8 GPIO Data Direction Mask

Access:	WO

This is a mask bit to determine whether the GPIO Data DIRECTION VALUE bit should be written into the register.

Value	Name
0b	Dot NOT write
1b	Write

7:5 Reserved

Format:	MBZ

4 GPIO Clock Data In

Default Value:	Ub Undefined (read only depends on I/O pin)
Access:	RO

This is the value that is sampled on the GPIO Clock pin as an input. This bit is undefined at reset.

GPIO_CTL

3 GPIO Clock Data Value

Default Value:	1b
Access:	R/W

This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if GPIO Clock DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Clock DIRECTION VALUE contains a value that will configure the pin as an output. The default of '1' mimics the I2C external pull-ups.

2 GPIO Clock Data Mask

Access:	WO

This is a mask bit to determine whether the GPIO Clock DATA VALUE bit should be written into the register.

Value	Name
0b	Dot NOT write
1b	Write

1 GPIO Clock Direction Value

Access:	R/W

This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if GPIO Clock DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO Clock DATA VALUE bit.

Value	Name
0b	Input
1b	Output

0 GPIO Clock Direction Mask

Access:	WO

This is a mask bit to determine whether the GPIO Clock DIRECTION VALUE bit should be written into the register.

Value	Name
0b	Dot NOT write
1b	Write

GPM POWERGATE LICENSE REQUEST

GPM_POWERGATE_LICENSE_REQ - GPM POWERGATE LICENSE REQUEST

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	00C0Ch

GPM-RPM PowerGate License Request
RPM Detects change in PowerGate License Request, forwards the request to PCU on C2U Event Bus

DWord	Bit	Description
0	31:0	**PowerGate License Request Data** Access: R/W 31:20 : Not used 19:16 : Render Slice Count 15:11 : Subslice Count 10:8 : Media Count 7:0 : EU Count

GPU_Ticks_Counter

GPU_TICKS - GPU_Ticks_Counter	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02910h
Valid Projects:	

Reading this register returns the live value of the GPU ticks counter that is sampled and included in the performance counter report header.

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the GPU tick counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Graphics Device Reset Control

GDRST - Graphics Device Reset Control

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	0941Ch

Graphics Device Reset Control Registers

DWord	Bit	Description
0	31:10	**Reserved** Access: RO Reserved
	9	**Initiate Graphics SFC1 soft reset** Access: R/W Set Graphics SFC 1 Soft-Reset Control: '1' : Initiate a graphics SFC1 domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP hardware can reset this bit. Note: This is a non-posted register.
	8	**Initiate Graphics SFC0 soft reset** Access: R/W Set Graphics SFC 0 Soft-Reset Control: '1' : Initiate a graphics SFC0 domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP hardware can reset this bit. Note: This is a non-posted register.
	7	**Initiate Graphics Media1 soft reset** Access: R/W Set Graphics Media 1 Soft-Reset Control: '1' : Initiate a graphics Vebox domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.
	6	**Reserved**

GDRST - Graphics Device Reset Control

	5	**Reserved**
	4	**Initiate Graphics Vebox Soft Reset** Access: R/W Set Graphics VEbox Soft-Reset Control: '1' : Initiate a graphics Vebox domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.
	3	**Initiate Graphics Blitter Soft Reset** Access: R/W Set Graphics Blitter Soft-Reset Control: '1' : Initiate a graphics blitter domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.
	2	**Initiate Graphics Media Soft Reset** Access: R/W Set Graphics Media Soft-Reset Control: '1' : Initiate a graphics media 0 domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.
	1	**Initiate Graphics Render Soft Reset** Access: R/W Set Graphics Render Soft-Reset Control: '1' : Initiate a graphics render domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.
	0	**Initiate Graphics Full Soft Reset** Access: R/W Set Graphics Full Soft-Reset Control: '1' : Initiate a full graphics reset (i.e., graphics render, media, and blitter reset). - Cleared by CP once the reset is complete '0' : N/A

GDRST - Graphics Device Reset Control		
		- Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.

Graphics Memory Fence Table Register

FENCE - Graphics Memory Fence Table Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	100000h-100007h
Name:	FENCE_0
Address:	100008h-10000Fh
Name:	FENCE_1
Address:	100010h-100017h
Name:	FENCE_2
Address:	100018h-10001Fh
Name:	FENCE_3
Address:	100020h-100027h
Name:	FENCE_4
Address:	100028h-10002Fh
Name:	FENCE_5
Address:	100030h-100037h
Name:	FENCE_6
Address:	100038h-10003Fh
Name:	FENCE_7
Address:	100040h-100047h
Name:	FENCE_8
Address:	100048h-10004Fh
Name:	FENCE_9
Address:	100050h-100057h
Name:	FENCE_10
Address:	100058h-10005Fh
Name:	FENCE_11
Address:	100060h-100067h
Name:	FENCE_12
Address:	100068h-10006Fh

FENCE - Graphics Memory Fence Table Register	
Name:	FENCE_13
Address:	100070h-100077h
Name:	FENCE_14
Address:	100078h-10007Fh
Name:	FENCE_15
Address:	100080h-100087h
Name:	FENCE_16
Address:	100088h-10008Fh
Name:	FENCE_17
Address:	100090h-100097h
Name:	FENCE_18
Address:	100098h-10009Fh
Name:	FENCE_19
Address:	1000A0h-1000A7h
Name:	FENCE_20
Address:	1000A8h-1000AFh
Name:	FENCE_21
Address:	1000B0h-1000B7h
Name:	FENCE_22
Address:	1000B8h-1000BFh
Name:	FENCE_23
Address:	1000C0h-1000C7h
Name:	FENCE_24
Address:	1000C8h-1000CFh
Name:	FENCE_25
Address:	1000D0h-1000D7h
Name:	FENCE_26
Address:	1000D8h-1000DFh
Name:	FENCE_27
Address:	1000E0h-1000E7h
Name:	FENCE_28
Address:	1000E8h-1000EFh
Name:	FENCE_29
Address:	1000F0h-1000F7h

FENCE - Graphics Memory Fence Table Register

Name:	FENCE_30
Address:	1000F8h-1000FFh
Name:	FENCE_31

The graphics device performs address translation from linear space to tiled space for a CPU access to graphics memory (See Memory Interface Functions chapter for information on these memory layouts) using the fence registers. Note that the fence registers are used only for CPU accesses to gfx memory. Graphics rendering/display pipelines use Per Surface Tiling (PST) parameters (found in SURFACE_STATE - see the Sampling Engine chapter) to access tiled gfx memory.

The intent of tiling is to locate graphics data that are close (in X and Y surface axes) in one physical memory page while still locating some amount of line oriented data sequentially in memory for display efficiency. All 3D rendering is done such that the QWords of any one span are all located in the same memory page, improving rendering performance. Applications view surfaces as linear, hence when the cpu access a surface that is tiled, the gfx hardware must perform linear to tiled address conversion and access the correct physical memory location(s) to get the data.

Tiled memory is supported for rendering and display surfaces located in graphics memory. A tiled memory surface is a surface that has a width and height that are subsets of the tiled region's pitch and height. The device maintains the constants required by the memory interface to perform the address translations. Each tiled region can have a different pitch and size. The CPU-memory interface needs the surface pitch and tile height to perform the address translation. It uses the GMAddr (PCI-BAR) offset address to compare with the fence start and end address, to determine if the rendering surface is tiled. The tiled address is generated based on the tile orientation determined from the matching fence register. Fence ranges are at least 4 KB aligned. Note that the fence registers are used only for CPU accesses to graphics memory.

A Tile represents 4 KB of memory. Tile height is 8 rows for X major tiles and 32 rows for Y major tiles. Tile Pitch is 512Bs for X major tiles and 128Bs for Y major tiles. The surface pitch is programmed in 128B units such that the pitch is an integer multiple of "tile pitch".

Engine restrictions on tile surface usage are detailed in Surface Placement Restrictions (Memory Interface Functions). Note that X major tiles can be used for Sampler, Color, Depth, motion compensation references and motion compensation destination, Display, Overlay, GDI Blt source and destination surfaces. Y major tiles can be used for Sampler, depth, color and motion compensation assuming they do not need to be displayed. GDI Blit operations, overlay and display cannot used Tiled Y orientations.

A "PST" graphics surface that will also be accessed via fence needs its base address to be tile row aligned.

Hardware handles the flushing of any pending cycles when software changes the fence upper/lower bounds.

Fence Table Registers occupy the address range specified above. Each Fence Table Register has the following format.

FENCE registers are not reset by a graphics reset. They will maintain their values unless a full reset is performed.

DWord	Bit	Description
0	63:44	**Fence Upper Bound** Format: GraphicsAddress[31:12] Bits 31:12 of the ending Graphics Address of the fence region. Fence regions must be aligned to a 4KB page. This address represents the last 4KB page of the fence region (Upper Bound is included in the fence region). Graphics Address is the offset within GMADR space.
	43	**Reserved** Format: MBZ

FENCE - Graphics Memory Fence Table Register

42:32 Fence Pitch

Format:	U10-1 Width in 128 bytes

This field specifies the width (pitch) of the fence region in multiple of "tile width". For Tile X this field must be programmed to a multiple of 512B ("003" is the minimum value) and for Tile Y this field must be programmed to a multiple of 128B ("000" is the minimum value).
000h = 128B
001h = 256B
...
3FFh = 128KB
...
7FFh = 256KB

31:12 Fence Lower Bound

Format:	GraphicsAddress[31:12]

Bits 31:12 of the starting Graphics Address of the fence region. Fence regions must be aligned to 4KB. This address represents the first 4KB page of the fence region (Lowe Bound is included in the fence region).
Graphics Address is the offset within GMADR space.

11:2 Reserved

Format:	MBZ

1 Tile Walk

This field specifies the spatial ordering of QWords within tiles.

Value	Name	Description
0h	MI_TILE_XMAJOR	Consecutive SWords (32 Bytes) sequenced in the X direction
1h	MI_TILE_YMAJOR	Consecutive OWords (16 Bytes) sequenced in the Y direction

0 Fence Valid

Format:	MI_FenceValid

This field specifies whether or not this fence register defines a fence region.

Value	Name
0h	MI_FENCE_INVALID
1h	MI_FENCE_VALID

Graphics Memory Range Address

GMADR_0_2_0_PCI - Graphics Memory Range Address

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x0000000C, 0x00000000
Size (in bits):	64
Address:	00018h

GMADR is the PCI aperture used by S/W to access tiled GFX surfaces in a linear fashion.

DWord	Bit	Description
0	63:39	**Reserved for Memory Base Address** Default Value: 0000000000000000000000000b Access: R/W Must be set to 0 since addressing above 512GB is not supported.
	38:32	**Memory Base Address** Default Value: 0000000b Access: R/W Set by the OS, these bits correspond to address signals [38:32].
	31	**4096 MB Address Mask** Default Value: 0b Access: R/W Lock FLR Resettable This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ. RO and forced to 0 when MSAC.APSZ >= 4096MB. (i.e. MSAC.APSZ[4]=1)
	30	**2048 MB Address Mask** Default Value: 0b Access: R/W Lock FLR Resettable This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ. RO and forced to 0 when MSAC.APSZ >= 2048MB. (i.e. MSAC.APSZ[3]=1)
	29	**1024 MB Address Mask** Default Value: 0b Access: R/W Lock FLR Resettable This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ. RO and forced to 0 when MSAC.APSZ >= 1024MB. (i.e. MSAC.APSZ[2]=1)

GMADR_0_2_0_PCI - Graphics Memory Range Address

	28	**512MB Address Mask** Default Value: 0b Access: R/W Lock FLR Resettable This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ. RO and forced to 0 when MSAC.APSZ >= 512MB. (i.e. MSAC.APSZ[1]=1)
	27	**256 MB Address Mask** Default Value: 0b Access: R/W Lock FLR Resettable This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ. RO and forced to 0 when MSAC.APSZ >= 256MB. (i.e. MSAC.APSZ[0]=1)
	26:4	**Address Mask** Default Value: 00000000000000000000000b Access: RO Hardwired to 0s to indicate at least 128MB address range.
	3	**Prefetchable Memory** Default Value: 1b Access: RO Hardwired to 1 to enable prefetching.
	2:1	**Memory Type** Default Value: 10b Access: RO Hardwired to 2h to indicate 64 bit base address.
	0	**Memory/IO Space** Default Value: 0b Access: RO Hardwired to 0 to indicate memory space.

Graphics MOCS Register0

GFX_MOCS_0 - Graphics MOCS Register0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030
Size (in bits):	32
Address:	0C800h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_0 - Graphics MOCS Register0

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2,1, or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register1

GFX_MOCS_1 - Graphics MOCS Register1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034
Size (in bits):	32
Address:	0C804h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_1 - Graphics MOCS Register1

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2,1, or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register2

GFX_MOCS_2 - Graphics MOCS Register2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038
Size (in bits):	32
Address:	0C808h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_2 - Graphics MOCS Register2

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2,1, or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register3

GFX_MOCS_3 - Graphics MOCS Register3

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031
Size (in bits):	32
Address:	0C80Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_3 - Graphics MOCS Register3

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register4

GFX_MOCS_4 - Graphics MOCS Register4

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0C810h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_4 - Graphics MOCS Register4

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register5

GFX_MOCS_5 - Graphics MOCS Register5

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0C814h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_5 - Graphics MOCS Register5

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register6

GFX_MOCS_6 - Graphics MOCS Register6

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0C818h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_6 - Graphics MOCS Register6

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register7

GFX_MOCS_7 - Graphics MOCS Register7

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0C81Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_7 - Graphics MOCS Register7

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register8

GFX_MOCS_8 - Graphics MOCS Register8

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0C820h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_8 - Graphics MOCS Register8

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register9

GFX_MOCS_9 - Graphics MOCS Register9

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0C824h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_9 - Graphics MOCS Register9

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register10

GFX_MOCS_10 - Graphics MOCS Register10

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0C828h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_10 - Graphics MOCS Register10

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register11

GFX_MOCS_11 - Graphics MOCS Register11

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0C82Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_11 - Graphics MOCS Register11

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register12

GFX_MOCS_12 - Graphics MOCS Register12

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0C830h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_12 - Graphics MOCS Register12

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register13

GFX_MOCS_13 - Graphics MOCS Register13

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0C834h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_13 - Graphics MOCS Register13

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register14

GFX_MOCS_14 - Graphics MOCS Register14

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0C838h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_14 - Graphics MOCS Register14

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register15

GFX_MOCS_15 - Graphics MOCS Register15

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0C83Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_15 - Graphics MOCS Register15

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register16

GFX_MOCS_16 - Graphics MOCS Register16

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030
Size (in bits):	32
Address:	0C840h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_16 - Graphics MOCS Register16

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register17

GFX_MOCS_17 - Graphics MOCS Register17

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034
Size (in bits):	32
Address:	0C844h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_17 - Graphics MOCS Register17

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register18

GFX_MOCS_18 - Graphics MOCS Register18

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038
Size (in bits):	32
Address:	0C848h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_18 - Graphics MOCS Register18

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register19

GFX_MOCS_19 - Graphics MOCS Register19

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031
Size (in bits):	32
Address:	0C84Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_19 - Graphics MOCS Register19

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register20

GFX_MOCS_20 - Graphics MOCS Register20

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0C850h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_20 - Graphics MOCS Register20

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register21

GFX_MOCS_21 - Graphics MOCS Register21

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0C854h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_21 - Graphics MOCS Register21

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register22

GFX_MOCS_22 - Graphics MOCS Register22

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0C858h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_22 - Graphics MOCS Register22

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register23

GFX_MOCS_23 - Graphics MOCS Register23

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0C85Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_23 - Graphics MOCS Register23

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register24

GFX_MOCS_24 - Graphics MOCS Register24

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0C860h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_24 - Graphics MOCS Register24

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register25

GFX_MOCS_25 - Graphics MOCS Register25

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0C864h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_25 - Graphics MOCS Register25

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register26

GFX_MOCS_26 - Graphics MOCS Register26

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0C868h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_26 - Graphics MOCS Register26

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register27

GFX_MOCS_27 - Graphics MOCS Register27

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0C86Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_27 - Graphics MOCS Register27

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register28

GFX_MOCS_28 - Graphics MOCS Register28

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0C870h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_28 - Graphics MOCS Register28

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register29

GFX_MOCS_29 - Graphics MOCS Register29

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0C874h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_29 - Graphics MOCS Register29

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register30

GFX_MOCS_30 - Graphics MOCS Register30

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0C878h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_30 - Graphics MOCS Register30

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register31

GFX_MOCS_31 - Graphics MOCS Register31

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0C87Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_31 - Graphics MOCS Register31

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register32

GFX_MOCS_32 - Graphics MOCS Register32

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030
Size (in bits):	32
Address:	0C880h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_32 - Graphics MOCS Register32

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register33

GFX_MOCS_33 - Graphics MOCS Register33

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034
Size (in bits):	32
Address:	0C884h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_33 - Graphics MOCS Register33

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register34

GFX_MOCS_34 - Graphics MOCS Register34

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038
Size (in bits):	32
Address:	0C888h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_34 - Graphics MOCS Register34

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register35

GFX_MOCS_35 - Graphics MOCS Register35

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031
Size (in bits):	32
Address:	0C88Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_35 - Graphics MOCS Register35

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register36

GFX_MOCS_36 - Graphics MOCS Register36

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0C890h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_36 - Graphics MOCS Register36

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register37

GFX_MOCS_37 - Graphics MOCS Register37

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0C894h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_37 - Graphics MOCS Register37

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register38

GFX_MOCS_38 - Graphics MOCS Register38

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0C898h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_38 - Graphics MOCS Register38

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register39

GFX_MOCS_39 - Graphics MOCS Register39

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0C89Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_39 - Graphics MOCS Register39

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register40

GFX_MOCS_40 - Graphics MOCS Register40

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0C8A0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_40 - Graphics MOCS Register40

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register41

GFX_MOCS_41 - Graphics MOCS Register41

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0C8A4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_41 - Graphics MOCS Register41

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register42

GFX_MOCS_42 - Graphics MOCS Register42

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0C8A8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_42 - Graphics MOCS Register42

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register43

GFX_MOCS_43 - Graphics MOCS Register43

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0C8ACh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_43 - Graphics MOCS Register43

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register44

GFX_MOCS_44 - Graphics MOCS Register44

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0C8B0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_44 - Graphics MOCS Register44

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register45

GFX_MOCS_45 - Graphics MOCS Register45

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0C8B4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_45 - Graphics MOCS Register45

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register46

GFX_MOCS_46 - Graphics MOCS Register46

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0C8B8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_46 - Graphics MOCS Register46

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register47

GFX_MOCS_47 - Graphics MOCS Register47

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0C8BCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_47 - Graphics MOCS Register47

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register48

GFX_MOCS_48 - Graphics MOCS Register48

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030
Size (in bits):	32
Address:	0C8C0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_48 - Graphics MOCS Register48

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register49

GFX_MOCS_49 - Graphics MOCS Register49

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034
Size (in bits):	32
Address:	0C8C4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_49 - Graphics MOCS Register49

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register50

GFX_MOCS_50 - Graphics MOCS Register50

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038
Size (in bits):	32
Address:	0C8C8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_50 - Graphics MOCS Register50

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register51

GFX_MOCS_51 - Graphics MOCS Register51

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031
Size (in bits):	32
Address:	0C8CCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_51 - Graphics MOCS Register51

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register52

GFX_MOCS_52 - Graphics MOCS Register52

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0C8D0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_52 - Graphics MOCS Register52

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register53

GFX_MOCS_53 - Graphics MOCS Register53

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0C8D4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_53 - Graphics MOCS Register53

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register54

GFX_MOCS_54 - Graphics MOCS Register54

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0C8D8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_54 - Graphics MOCS Register54

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register55

GFX_MOCS_55 - Graphics MOCS Register55

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0C8DCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_55 - Graphics MOCS Register55

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register56

GFX_MOCS_56 - Graphics MOCS Register56

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0C8E0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_56 - Graphics MOCS Register56

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register57

GFX_MOCS_57 - Graphics MOCS Register57

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0C8E4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_57 - Graphics MOCS Register57

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register58

GFX_MOCS_58 - Graphics MOCS Register58

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0C8E8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_58 - Graphics MOCS Register58

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register59

GFX_MOCS_59 - Graphics MOCS Register59

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0C8ECh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_59 - Graphics MOCS Register59

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register60

GFX_MOCS_60 - Graphics MOCS Register60

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0C8F0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_60 - Graphics MOCS Register60

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register61

GFX_MOCS_61 - Graphics MOCS Register61

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0C8F4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_61 - Graphics MOCS Register61

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register62

GFX_MOCS_62 - Graphics MOCS Register62

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0C8F8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_62 - Graphics MOCS Register62

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register63

GFX_MOCS_63 - Graphics MOCS Register63

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0C8FCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

GFX_MOCS_63 - Graphics MOCS Register63

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics Mode Register

GFX_MODE - Graphics Mode Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	r/w
Size (in bits):	32
Trusted Type:	1

Address:	0229Ch-0229Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_RCSUNIT

Address:	1229Ch-1229Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_VCSUNIT0

Address:	1A29Ch-1A29Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_VECSUNIT

Address:	1C29Ch-1C29Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_VCSUNIT1

Address:	2229Ch-2229Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_BCSUNIT

This register contains a control bit for the new execlist and 2-level PPGTT functions.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)

GFX_MODE - Graphics Mode Register

15 — Execlist Enable

Mask:	MMIO#31

When set, software can utilize the execlist registers to load a context into hardware. MI_SET_CONTEXT and MI_ARB_CHECK commands will be converted to NOOP if parsed. When this bit is clear, the Execlist mechanism cannot be used. The context must be loaded via MI_SET_CONTEXT and the ring must be loaded via MMIO access.

Programming Notes

This bit is *not* intended to be changed dynamically. Changing the value of this bit while rendering is in progress will have UNDEFINED results. This bit should be changed only after a full reset and before submitting *any* commands to the device.

14 — Reserved

13:12 — Reserved

Format:	PBC

11 — Reserved

10 — Reserved

Format:	PBC

9 — Per-Process GTT Enable

Format:	Enable

Per-Process GTT Enable

Value	Name	Description
0h	PPGTT Disable **[Default]**	When clear, the Global GTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.
1h	PPGTT Enable	When set, the PPGTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.

Programming Notes

This bit is used for enabling PPGTT access in Ring Buffer mode of scheduling. Privilege field in context descriptor states the same in Execlist Mode of scheduling. This field should be set before programming PDP0/1/2/3 registers in order to set the PPGTT translation of memory access.
Programming this bit doesn't enable or disable the PPGTT translation of memory access immediately; the change comes in to affect only when the Page Directory registers are programmed. Programming this bit must be followed by programming Page Directory Registers in order to enable or disable the PPGTT translation of memory access.

8 — Reserved

8 — Reserved

Source:	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS
Format:	PBC

GFX_MODE - Graphics Mode Register

7 — 64Bit Virtual Addressing Enable

Format:	Enable

64Bit Virtual Addressing Enable

Value	Name	Description
0h	64Bit Virtual Addressing Disable **[Default]**	When clear indicates GFX operating in 32bit Virtual Addressing for PPGTT based memory access.
1h	64Bit Virtual Addressing Enable	When Set indicates GFX operating in 64bit (48bit Canonical) Virtual Addressing for PPGTT based memory access.

Programming Notes

This bit is only valid when PPGTT is enabled in ring buffer mode of scheduling. Context Descriptor has a similar bit to control 64bit virtual addressing in execlist mode of scheduling. Whether this field is set or clear virtual addresses translated through GGTT are always 32Bit. This field should be programmed before enabling PPGTT access. When this field is not set or for GGTT virtual addresses, Graphics Address [47:32] field of any commands or register exercised by SW should be programmed to 0x0.

6:5 — Reserved

4 — Reserved

3 — Reserved

Format:	MBZ

2:1 — Reserved

Format:	PBC

0 — Privilege Check Disable

Format:	Enable

This field when set, disables Privilege Violation checks on non-privileged batch buffers. When set Privileged commands are allowed to be executed from non-privileged batch buffers.

Workaround

Workaround https://vthsd.iind.intel.com/hsd/gen9lp/default.aspx#bug_de/default.aspx?bug_de_id=2130715 : Irrespective of "Privilege Check Disable" bit set, HW enforces chained or second level batch buffer "Address Space Indicator" to be PPGTT if the parent batch buffer Address Space Indicator is PPGTT.

Graphics System Event

GSE_0_2_0_PCI - Graphics System Event			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	000E4h		
This register can be accessed by either Byte, Word, or Dword PCI config cycles. A write to this register will cause the Graphics System Event display interrupt if it is enabled and unmasked in the display interrupt registers.			
DWord	**Bit**	**Description**	
0	31:24	**GSE Scratch Trigger 3**	
		Default Value:	00000000b
		Access:	R/W
	23:16	**GSE Scratch Trigger 2**	
		Default Value:	00000000b
		Access:	R/W
	15:8	**GSE Scratch Trigger 1**	
		Default Value:	00000000b
		Access:	R/W
	7:0	**GSE Scratch Trigger 0**	
		Default Value:	00000000b
		Access:	R/W

Graphics Translation Table Memory Mapped Range Address

GTTMMADR_0_2_0_PCI - Graphics Translation Table Memory Mapped Range Address

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000004, 0x00000000
Size (in bits):	64
Address:	00010h

This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. The range requires 16 MB combined for MMIO and Global GTT aperture, with 2MB of that used by MMIO, 6MB reserved, and 8MB used by GTT. GTTADR will begin at (GTTMMADR + 8 MB) while the MMIO base address will be the same as GTTMMADR. The region between (GTTMMADR + 2MB) - (GTTMMADR + 8MB) is reserved. For the Global GTT, this range is defined as a memory BAR in graphics device config space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT memory area. The device snoops writes to this region in order to invalidate any cached translations within the various TLB's implemented on-chip. The allocation is for 16MB and the base address is defined by bits [38:24]. Note: Per PCI enumeration requirements, to determine the size of a BAR software should write all 1s to the BAR, read it back and see how many of the lower bits read as 0 (meaning that they didn't take the 1s). This indicates the size of the BAR. In order for this to work bits 63 down to the size of the BAR need to be writable to 1s.

DWord	Bit	Description
0	63:39	**Reserved for Memory Base Address** Default Value: 0000000000000000000000000b Access: R/W Must be set to 0 since addressing above 512GB is not supported.
	38:24	**Memory Base Address** Default Value: 000000000000000b Access: R/W Set by the OS, these bits correspond to address signals [38:24].
	23:4	**Address Mask** Default Value: 00000000000000000000b Access: RO Hardwired to 0s to indicate at least 16MB address range.
	3	**Prefetchable Memory** Default Value: 0b Access: RO Hardwired to 0 to prevent prefetching.

GTTMMADR_0_2_0_PCI - Graphics Translation Table Memory Mapped Range Address

	2:1	**Memory Type** Default Value: 10b Access: RO Hardwired to 2h to indicate 64 bit base address.
	0	**Memory/IO Space** Default Value: 0b Access: RO Hardwired to 0 to indicate memory space.

GSA_AUDIO_BDF

GSA_AUDIO_BDF

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00100000
Access:	R/W
Size (in bits):	32
Address:	1300B0h-1300B3h
Name:	GSA Audio BDF
ShortName:	GSA_AUDIO_BDF
Power:	PG0
Reset:	global

BIOS must program this register with the PCI Bus, Device, and Function of the PCH audio device and set the lock. Access is a variant of RW-L. When Lock is not set (bit 0 = 0) the register can be written by any source. After lock is set (bit 0 = 1), only writes from firmware (cfgspace 0x11111 and srcID 0x10) will update the register values. Writes from other sources will complete without updating the register values. Any source can read the register. **This register is not reset by the device 2 FLR.**

DWord	Bit	Description
0	31:24	**Bus** Default Value: 00000000b Access is RW-L. This field specifies the PCI bus number of the PCH audio device.
	23:19	**Device** Default Value: 00010b Access is RW-L. This field specifies the PCI device number of the PCH audio device.
	18:16	**Function** Default Value: 000b Access is RW-L. This field specifies the PCI function number of the PCH audio device.
	15:1	**Reserved** Format: MBZ
	0	**Lock** Access is RW-KL. This field locks all writeable settings in this register, including itself. Value: 0b — Name: Unlock Value: 1b — Name: Lock

GSA_TOUCH_BDF

GSA_TOUCH_BDF

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00100000
Access:	R/W
Size (in bits):	32
Address:	1300B4h-1300B7h
Name:	GSA Touch BDF
ShortName:	GSA_TOUCH_BDF
Power:	PG0
Reset:	global

BIOS must program this register with the PCI Bus, Device, and Function that the Display Engine should use for communication with the PCH touch device, and set the lock. Access is a variant of RW-L. When Lock is not set (bit 0 = 0) the register can be written by any source. After lock is set (bit 0 = 1), only writes from firmware (cfgspace 0x11111 and srcID 0x10) will update the register values. Writes from other sources will complete without updating the register values. Any source can read the register. **This register is not reset by the device 2 FLR.**

DWord	Bit	Description
0	31:24	**Bus** Default Value: 00000000b Access is RW-L. This field specifies the PCI bus number.
	23:19	**Device** Default Value: 00010b Access is RW-L. This field specifies the PCI device number.
	18:16	**Function** Default Value: 000b Access is RW-L. This field specifies the PCI function number.
	15:1	**Reserved** Format: MBZ
	0	**Lock** Access is RW-KL. This field locks all writeable settings in this register, including itself. Value: 0b — Name: Unlock Value: 1b — Name: Lock

GS Invocation Counter

GS_INVOCATION_COUNT - GS Invocation Counter	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02328h

This register stores the number of objects that are part of geometry shader threads. This register is part of the context save and restore.

DWord	Bit	Description
0	63:32	**GS Invocation Count UDW** Number of objects that are dispatched as a geometry shader threads invoked by the GS stage. Updated only when **Statistics Enable** is set in GS_STATE (see the Geometry Shader Chapter in the 3D Volume.)
	31:0	**GS Invocation Count LDW** Number of objects that are dispatched as a geometry shader threads invoked by the GS stage. Updated only when **Statistics Enable** is set in GS_STATE (see the Geometry Shader Chapter in the 3D Volume.)

GS Primitives Counter

GS_PRIMITIVES_COUNT - GS Primitives Counter		
Register Space:	MMIO: 0/2/0	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	02330h	
This register reflects the total number of primitives that have been output by the Geometry Shader stage. This register is part of the context save and restore.		
DWord	**Bit**	**Description**
0	63:32	**GS Primitives Count UDW** Total number of primitives output by the geometry stage. Updated only when Statistics Enable is set in GS_STATE (see the Geometry Shader Chapter in the 3D Volume.)
	31:0	**GS Primitives Count LDW** Total number of primitives output by the geometry stage. Updated only when Statistics Enable is set in GS_STATE (see the Geometry Shader Chapter in the 3D Volume.)

GT4 Mode Control Register

GT4MODECTL - GT4 Mode Control Register		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	09038h	
GT4 Mode Control Register		
DWord	**Bit**	**Description**
0	31:18	**RSVD** Access: R/W
	17:10	**Reserved**
	9:2	**Reserved**
	1:0	**GT4 Mode Control** Access: R/W GT4 Usage mode: 00b: Non-GT4. 01b: GT4 is used in Alternate Frame rendering Mode (AFR). 10b: Basic Split Frame rendering Mode (SFR). 11b: Complex Split Frame rendering Mode (SFR w/ CBR).

GTC_CTL

GTC_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	67000h-67003h
Name:	Global Time Code Control
ShortName:	GTC_CTL
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31	**GTC Function Enable** This bit enables the GTC counter. Value / Name: 0b Disable; 1b Enable Restriction: Enable this bit before enabling GTC controller operation on a port with a GTC capable device.
	30:29	**Reserved** Format: MBZ
	28:13	**Reserved**
	12:1	**Reserved** Format: MBZ
	0	**Reserved**

GTC_DDA_M

GTC_DDA_M		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	67010h-67013h	
Name:	Global Time Code DDA M	
ShortName:	GTC_DDA_M	
Power:	PG1	
Reset:	soft	
DWord	**Bit**	**Description**
0	31:24	**Reserved**
	23:0	**GTC DDA M** This field is used to program the M value of the GTC DDA. The ratio of M to N programmed depends on the GTC reference clock. The DDA programmed values are related by the following formula: 1/(accumulator increment) = Reference Clock * DDA_M / DDA_N

GTC_DDA_N

GTC_DDA_N		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	67014h-67017h	
Name:	Global Time Code DDA N	
ShortName:	GTC_DDA_N	
Power:	PG1	
Reset:	soft	
DWord	**Bit**	**Description**
0	31:24	**GTC Accum Inc** Format: U7.1 This field is the GTC accumulator increment value in nanoseconds each time the DDA trips. It is programmed in 7.1 fixed point binary format where the LSB represents 0.5ns increment.
	23:0	**GTC DDA N** This field is used to program the N value of the GTC DDA. The ratio of M to N programmed depends on the GTC reference clock and should not result in any accumulation error in any 10ms interval period. The DDA programmed values are related by the following formula: 1/(accumulator increment) = Reference Clock * DDA_M / DDA_N

GTC_IIR

GTC_IIR	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/WC
Size (in bits):	32
Address:	67058h-6705Bh
Name:	Global Time Code Interrupt Identity
ShortName:	GTC_IIR
Power:	PG1
Reset:	soft

See the GTC interrupt bit definition to find the source event for each interrupt bit.

DWord	Bit	Description
0	31:0	**Interrupt Identity Bits** This field holds the persistent values of the GTC interrupt bits which are unmasked by the GTC_IMR. Bits set in this register will propagate to the GTC interrupt in the Display Engine Miscellaneous Interrupts. Bits set in this register will remain set (persist) until the interrupt condition is cleared by writing a '1' to the appropriate bits.

Value	Name
0b	Condition Not Detected
1b	Condition Detected

GTC_IMR

GTC_IMR	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0xFFFFFFFF
Access:	R/W
Size (in bits):	32
Address:	67054h-67057h
Name:	Global Time Code Interrupt Mask
ShortName:	GTC_IMR
Power:	PG1
Reset:	soft

See the GTC interrupt bit definition to find the source event for each interrupt bit.

DWord	Bit	Description
0	31:0	**Interrupt Mask Bits** This field contains a bit mask which selects which GTC events are reported int the GTC IIR.

Value	Name
0b	Not Masked
1b	Masked
FFFFFFFFh	All interrupts masked **[Default]**

GTC_LIVE

GTC_LIVE		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	67020h-67023h	
Name:	Global Time Code Live	
ShortName:	GTC_LIVE	
Power:	PG1	
Reset:	soft	
DWord	**Bit**	**Description**
0	31:0	**GTC Live Value** This field contains the live current value of the GTC. It is inactive when the GTC controller function is disabled. This register also samples and holds the live GTC value following a Audio Time Capture (ATC) event until software reads this register. A subsequent read of this register will reflect the live value.

GTC_PORT_CTL

GTC_PORT_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	64070h-64073h
Name:	DDI A GTC Port Control
ShortName:	GTC_PORT_CTL_A
Power:	PG1
Reset:	soft
Address:	64170h-64173h
Name:	DDI B GTC Port Control
ShortName:	GTC_PORT_CTL_B
Power:	PG2
Reset:	soft
Address:	64270h-64273h
Name:	DDI C GTC Port Control
ShortName:	GTC_PORT_CTL_C
Power:	PG2
Reset:	soft
Address:	64370h-64373h
Name:	DDI D GTC Port Control
ShortName:	GTC_PORT_CTL_D
Power:	PG2
Reset:	soft

Description
There is one instance of this register per port A, B, C, D and F.

DWord	Bit	Description
0	31	**Port Global Time Code Enable** This bit enables the GTC controller to start lock acquisition phase with remote GTC sink connected to this port. This bit has no effect if the GTC controller is disabled.

Value	Name
0b	Disable
1b	Enable

GTC_PORT_CTL

		Restriction The Maintenance Phase Enable bit must be initially written as '0' when this bit is set.
	30:25	**Reserved**
	24	**Maintenance Phase Enable** This bit is used by software to transition from lock acquisition to lock maintenance phase. The GTC controller generates an interrupt at the end of the lock phase as determined by lock acquisition duration field. Software shall read the sink device GTC lock done bit. If set, software shall set this bit to '1' after first writing the GTC skew value to the RX GTC skew DPCD offset with GTC skew enable bit set to '1'. **Value** / **Name** / **Description** 0b / Lock / Lock acquisition phase. The controller writes or reads GTC every 1ms. 1b / Maintain / Lock maintenance phase. The controller writes or reads GTC every 10ms.
	23:1	**Reserved**
	0	**Port RX Lock Done** This bit indicates the remote GTC sink has achieved lock. This bit shall be written by software after reading remote GTC sink DPCD register. This bit shall be cleared by software when GTC controller is reset from lock maintenance mode to lock acquisition mode or when the controller is disabled. **Value** / **Name** 0b / Not Locked 1b / Locked

GTC_PORT_MISC

GTC_PORT_MISC	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00034A00
Access:	R/W
Size (in bits):	32
Address:	64094h-64097h
Name:	DDI A GTC Port Miscellaneous
ShortName:	GTC_PORT_MISC_A
Power:	PG1
Reset:	soft
Address:	64194h-64197h
Name:	DDI B GTC Port Miscellaneous
ShortName:	GTC_PORT_MISC_B
Power:	PG2
Reset:	soft
Address:	64294h-64297h
Name:	DDI C GTC Port Miscellaneous
ShortName:	GTC_PORT_MISC_C
Power:	PG2
Reset:	soft
Address:	64394h-64397h
Name:	DDI D GTC Port Miscellaneous
ShortName:	GTC_PORT_MISC_D
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:22	**Reserved** Format: MBZ
	21:12	**GTC Update Message Delay** Default Value: 00110100b 52 nanoseconds This field programs the absolute delay in nanoseconds between the GTC at the aux sync point event and the corresponding GTC value at the capture point. It represents the delay between the GTC values at the aux sync point and capture point introduced due to synchronization and glitch suppression.

GTC_PORT_MISC

	11:8	**Min Lock Duration** Default Value: 1010b 10ms This field determines the minimum duration in milliseconds of lock acquisition and maintenance phase after which software is notified through interrupt. The GTC interrupt enable and mask register must be enabled beforehand. Software may also poll the interrupt identity bit in IIR.
	7:0	**Reserved** Format: MBZ

GTC_PORT_TX_CURR

GTC_PORT_TX_CURR	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	64078h-6407Bh
Name:	DDI A GTC Port TX Current
ShortName:	GTC_PORT_TX_CURR_A
Power:	PG1
Reset:	soft
Address:	64178h-6417Bh
Name:	DDI B GTC Port TX Current
ShortName:	GTC_PORT_TX_CURR_B
Power:	PG2
Reset:	soft
Address:	64278h-6427Bh
Name:	DDI C GTC Port TX Current
ShortName:	GTC_PORT_TX_CURR_C
Power:	PG2
Reset:	soft
Address:	64378h-6437Bh
Name:	DDI D GTC Port TX Current
ShortName:	GTC_PORT_TX_CURR_D
Power:	PG2
Reset:	soft

Description
There is one instance of this register per port A, B, C, and D.

DWord	Bit	Description
0	31:0	**Global Time Code Port TX Current** This field contains the local GTC value sampled at the Aux sync point of the response message from the remote GTC sink following software read of the remote sink GTC DPCD register.

GTC_PORT_TX_PREV

GTC_PORT_TX_PREV	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	64080h-64083h
Name:	DDI A GTC Port TX Previous
ShortName:	GTC_PORT_TX_PREV_A
Power:	PG1
Reset:	soft
Address:	64180h-64183h
Name:	DDI B GTC Port TX Previous
ShortName:	GTC_PORT_TX_PREV_B
Power:	PG2
Reset:	soft
Address:	64280h-64283h
Name:	DDI C GTC Port TX Previous
ShortName:	GTC_PORT_TX_PREV_C
Power:	PG2
Reset:	soft
Address:	64380h-64383h
Name:	DDI D GTC Port TX Previous
ShortName:	GTC_PORT_TX_PREV_D
Power:	PG2
Reset:	soft

Description
There is one instance of this register per port A, B, C, D and F.

DWord	Bit	Description
0	31:0	**Global Time Code Port TX Previous** This field contains the previous local GTC value sampled at Aux sync point. It is transferred from the GTC_PORT_TX_CURR register when the current value is updated.

GTFORCEAWAKE

GTFORCEAWAKE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	130090h-130093h
Name:	GT Force Awake
ShortName:	GTFORCEAWAKE
Power:	PG0
Reset:	soft

DWord	Bit	Description
0	31:1	**Reserved**
	0	**Force Awake** This field is no longer used. The multiple force wake mechanism has replaced it. Refer to MULTIFORCEWAKE 0xA188 register description for the usage.

GT Function Level Reset Control Message

FLRCTLMSG - GT Function Level Reset Control Message

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	08100h

GT FLR Control Register

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:1	**Reserved** Access: RO Reserved
	0	**Initiate GT Function Level Reset Message** Access: R/W Set GT Function Level Reset (FLR) 1: Initiate GT FLR - This is a Non-Posted message to reset Render, Media, Blitter and GTI-Device domains. - This bit is cleared by the CPunit upon completion of the reset.

GT Interrupt 0 Definition

GT Interrupt 0 Definition	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	44300h-4430Fh
Name:	GT 0 Interrupts
ShortName:	GT_0_INTERRUPT
Power:	PG0
Reset:	soft

This table indicates which events are mapped to each bit of the GT Interrupt 0 registers.
Bits 15:0 are used for Render CS.
Bits 31:16 are used for Blitter CS.
The IER enabled Render Interrupt IIR (sticky) bits are ORed together to generate the Render Interrupts Pending bit in the Master Interrupt Control register.
The IER enabled Blitter Interrupt IIR (sticky) bits are ORed together to generate the Blitter Interrupts Pending bit in the Master Interrupt Control register.
0x44300 = ISR
0x44304 = IMR
0x44308 = IIR
0x4430C = IER

DWord	Bit	Description
0	31	**Spare 31**
	30	**Spare 30**
	29	**Spare 29**
	28	**Spare 28**
	27	**BCS Wait On Semaphore**
	26	**Spare 26**
	25	**Spare 25**
	24	**BCS Context Switch Interrupt**
	23	**Spare 23**
	22	**Spare 22**
	21	**Spare 21**
	20	**BCS MI Flush DW Notify**
	19	**BCS Error Interrupt**
	18	**Spare 18**
	17	**Spare 17**
	16	**BCS MI User Interrupt**

GT Interrupt 0 Definition		
	15	**Spare 15**
	14	**Spare 14**
	13	**Spare 13**
	12	**Spare 12**
	11	**CS Wait On Semaphore**
	10	**CS L3 Counter Save**
	9	**CS TR Invalid Tile Detection**
	8	**CS Context Switch Interrupt**
	7	**Page Fault Interrupt** This interrupt is for handling Legacy Page Fault interface for all Command Streamers [BCS, RCS, VCS, VECS]. When Fault Repair Mode is enabled, Interrupt mask register value is not looked at to generate interrupt due to page fault. Please refer to vol1c "page fault support" section for more details.
	6	**CS Watchdog Counter Expired**
	5	**Spare 5**
	4	**CS PIPE_CONTROL Notify**
	3	**CS Error Interrupt**
	2	**Spare 2**
	1	**Reserved**
	0	**CS MI User Interrupt**

GT Interrupt 1 Definition

GT Interrupt 1 Definition	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	44310h-4431Fh
Name:	GT 1 Interrupts
ShortName:	GT_1_INTERRUPT
Valid Projects:	
Power:	PG0
Reset:	soft

This table indicates which events are mapped to each bit of the GT Interrupt 1 registers.
Bits 15:0 are used for VCS1.
Bits 31:16 are used for VCS2.
The VCS1 Interrupt IIR (sticky) bits are ORed together to generate the VCS1 Interrupts Pending bit in the Master Interrupt Control register.
The VCS2 Interrupt IIR (sticky) bits are ORed together to generate the VCS2 Interrupts Pending bit in the Master Interrupt Control register.
0x44310 = ISR
0x44314 = IMR
0x44318 = IIR
0x4431C = IER

DWord	Bit	Description
0	31	**Spare 31**
	30	**Spare 30**
	29	**Spare 29**
	28	**Spare 28**
	27	**VCS2 Wait On Semaphore**
	26	**Spare 26**
	25	**Reserved**
	24	**VCS2 Context Switch Interrupt**
	23	**Spare 23**
	22	**VCS2 Watchdog Counter Expired**
	21	**Reserved**
	20	**VCS2 MI Flush DW Notify**
	19	**VCS2 Error Interrupt**
	18	**Spare 18**
	17	**Spare 17**

GT Interrupt 1 Definition		
	16	**VCS2 MI User Interrupt**
	15	**Spare 15**
	14	**Spare 14**
	13	**Spare 13**
	12	**Spare 12**
	11	**VCS1 Wait On Semaphore**
	10	**Spare 10**
	9	**Reserved**
	8	**VCS1 Context Switch Interrupt**
	7	**Spare 7**
	6	**VCS1 Watchdog Counter Expired**
	5	**Reserved**
	4	**VCS1 MI Flush DW Notify**
	3	**VCS1 Error Interrupt**
	2	**Spare 2**
	1	**Spare 1**
	0	**VCS1 MI User Interrupt**

GT Interrupt 2 Definition

GT Interrupt 2 Definition	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	44320h-4432Fh
Name:	GT 2 Interrupts
ShortName:	GT_2_INTERRUPT
Valid Projects:	
Power:	PG0
Reset:	soft

This table indicates which events are mapped to each bit of the GT Interrupt 2 registers.
Bits 15:0 are used for GTPM.
The IER enabled GTPM Interrupt IIR (sticky) bits are ORed together to generate the GTPM Interrupts Pending bit in the Master Interrupt Control register.
0x44320 = ISR
0x44324 = IMR
0x44328 = IIR
0x4432C = IER

DWord	Bit	Description
0	31	**Reserved**
	30	**Reserved**
	29	**Reserved**
	28	**Reserved**
	27	**Reserved**
	26	**Reserved**
	25	**Reserved**
	24	**Reserved**
	23	**Reserved**
	22	**Reserved**
	21	**Reserved**
	20	**Reserved**
	19	**Reserved**
	18	**Reserved**
	17	**Reserved**
	16	**Reserved**
	15	**Spare 15**

GT Interrupt 2 Definition		
	14	**Spare 14**
	13	**Unslice Frequency Control Up Interrupt**
	12	**Unslice Frequency Control Down Interrupt**
	11	**NFADFL Frequency Up Interrupt**
	10	**NFADFL Frequency Down Interrupt**
	9	**Reserved**
	8	**GTPM Engines Idle Interrupt**
	7	**GTPM Uncore to Core Trap Interrupt**
	6	**GTPM Render Frequency Downwards Timeout During RC6 Interrupt**
	5	**GTPM Render P-State Up Threshold Interrupt**
	4	**GTPM Render P-State Down Threshold Interrupt**
	3	**Spare 3**
	2	**GTPM Render Geyserville Up Evaluation Interval Interrupt**
	1	**GTPM Render Geyserville Down Evaluation Interval Interrupt**
	0	**Spare 0**

GT Interrupt 3 Definition

GT Interrupt 3 Definition	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	44330h-4433Fh
Name:	GT 3 Interrupts
ShortName:	GT_3_INTERRUPT
Power:	PG0
Reset:	soft

This table indicates which events are mapped to each bit of the GT Interrupt 3 registers.
Bits 15:0 are used for VEBox.
Bits 27:16 are Reserved
Bits 31:28 are used for OACS.
The VEBox Interrupt IIR (sticky) bits are ORed together to generate the VEBox Interrupts Pending bit in the Master Interrupt Control register.
0x44330 = ISR
0x44334 = IMR
0x44338 = IIR
0x4433C = IER

DWord	Bit	Description
0	31	**Spare 31**
	30	**Spare 30**
	29	**Spare 29**
	28	**Performance Monitoring Buffer Half-Full Interrupt** For internal trigger (timer event based) reporting, this interrupt is generated if the report buffer crosses the half full limit.
	27	**Spare 27**
	26	**Spare 26**
	25	**Spare 25**
	24	**Spare 24**
	23	**Spare 23**
	22	**Spare 22**
	21	**Spare 21**
	20	**Spare 20**
	19	**Spare 19**
	18	**Spare 18**
	17	**Reserved**

GT Interrupt 3 Definition		
	16	**Reserved**
	15	**Spare 15**
	14	**Spare 14**
	13	**Spare 13**
	12	**Spare 12**
	11	**VECS Wait On Semaphore**
	10	**Spare 10**
	9	**Spare 9**
	8	**VECS Context Switch Interrupt**
	7	**Spare 7**
	6	**Reserved**
	5	**Spare 5**
	4	**VECS MI Flush DW Notify**
	3	**VECS Error Interrupt**
	2	**Spare 2**
	1	**Spare 1**
	0	**VECS MI User Interrupt**

GTI PGFET control register with lock

PFETCTL - GTI PGFET control register with lock

Register Space: MMIO: 0/2/0
Source: BSpec
Default Value: 0x0004005A

Size (in bits): 32

Address: 24008h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of GTI PGFETCTL register are R/W 1 = All bits of GTI PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:23	**Reserved** Access: RO Reserved
	22	**Leave firewall disabled** Access: R/W Lock When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e dont firewall the gated domain, but complete logical flow
	21	**Leave FET On** Access: R/W Lock When This bit is set SPC will not turn off the PFET eventhough it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e dont power off pfet, but complete logical flow Programming note : This bit should be programmed before the powerup sequence is initiated for GTI
	20	**Reserved**
	19	**Reserved**

PFETCTL - GTI PGFET control register with lock

	18:16	**Delay from enabling secondary PFETs to power good.** Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 320ns 3'b100: 640ns 3'b101: 1280ns 3'b110: 2560ns 3'b111: 5120ns Value: 100b — Name: **[Default]**
	15:13	**Time period last primay pfet strobe to secondary pfet strobe** Access: R/W Lock Time period last primay pfet strobe to secondary pfet strobe 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	12:10	**Time period b/w two adjacent strobes** Access: R/W Lock Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	9:7	**FET setup margin from enable to strobe** Access: R/W Lock Setup margin in design before sampling enable event at the first pre-charge sequencer/shift register flop 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)

PFETCTL - GTI PGFET control register with lock

	6:0	**Number of flops to enable primary FETs** Access: R/W Lock Number of flops to enable primary FETs. For a setting of N there will be N+1 total strobes generated 7'b0000000: 10 Flops to be strobed 7'b0000001: 11 Flops to be strobed 7'b0000010: 12 Flops to be strobed 7'b0001111: 26 Flops to be strobed

Value	Name
1011010b	**[Default]**

GTI Power Gate Control Request

PGCTLREQ - GTI Power Gate Control Request		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	24000h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:1	**Reserved** Access: RO Reserved
	0	**Reserved**

GT Mode Register

GT_MODE - GT Mode Register

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000 [SKL:GT2:A, SKL:GT2:B, SKL:GT2:C, SKL:GT2:D, SKL:GT2:F, SKL:GT2:G, SKL:GT3:A, SKL:GT3:C, SKL:GT3:F, SKL:GT3:G, SKL:GT4:E, SKL:GT4:F, SKL:GT4:G]
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	07008h
Valid Projects:	

This Register is used to control the 6EU and 12EU configuration for GT. Writing 0x01FF01FF to this register enables the 6EU mode.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15	**EU Local Thread Checking Enable** Access: r/w This field configures the EU local thread checking. If enable the stateless access will be checked against the local thread's scratch space size and start address. Value / Name / Description: 0h / Disable **[Default]** / EU local thread checking is disabled. 1h / Enable / EU local thread checking is enabled. **Restriction**: SKL configurations do not properly support Per-Thread Scratch Space checking when headerless Data Port messages are used. The workaround is either to disable this control, or not use SFID_DP_DC0 or SFID_DP_DC2 headerless messages.
	14:13	**SFR mode** Access: r/w Format: U2 This field must be zero when not in GT4(SFR) configuration i.e GTB_rendermode fuse set to SFR.
	12:11	**Cross Slice Hashing Mode** Access: r/w Format: U2

GT_MODE - GT Mode Register

Value	Name	Description	Programming Notes
0h	Normal Mode **[Default]**	GT3: 16x16 Hashing enabled GT2 or lower modes: No cross slice hashing	
1h	Reserved		
2h	32x16 Hahsing	32x16 Pixel hashing across slices	
3h	32X32 hashing	32X32 pixel hashing across slices	This setting must be used when sub-slice hashing mode is 16x16.

Programming Notes
Normal mode of operation in GT3 mode will be to use either 16x16 Hashing or 32x32 Hashing.

10 **Reserved**

Access:	r/w
Format:	PBC

9:8 **Subslice Hashing Mode**

Access:	r/w
Format:	U2

This field defines hashing modes across subslices.

Value	Name	Description
0h	**[Default]**	8X8 hashing
1h		16x4 hashing
2h		8x4 hashing
3h		16x16 hashing

7 **Reserved**

Access:	r/w
Format:	PBC

5:4 **Slice2 IZ Hashing: 7 EU subslice encoding**

Access:	r/w

These bits control 3-way sub-slice hashing by conveying which sub-slice has 7 EUs.

Value	Name	Description
0h	**[Default]**	All subslices have equal number of EUs.
1h		Subslice 2 has 7 EUs.
2h		Subslice 1 has 7 EU.
3h		Subslice 0 has 7 EUs.

Programming Notes
SW must program these bits based on EU Disable Fuses in Slice 2.

GT_MODE - GT Mode Register

3:2 **Slice1 IZ Hashing: 7 EU subslice encoding**

Access:	r/w

These bits control 3-way sub-slice hashing by conveying which sub-slice has 7 EUs.

Value	Name	Description
0h	**[Default]**	All subslices have equal number of EUs.
1h		Subslice 2 has 7 EUs.
2h		Subslice 1 has 7 EUs.
3h		Subslice 0 has 7 EUs.

Programming Notes
SW must program these bits based on EU Disable Fuses in Slice 1.

1:0 **Slice 0 IZ Hashing: 7 EU subslice encoding**

Access:	r/w

These bits control 3-way sub-slice hashing by conveying which sub-slice has 7 EUs.

Value	Name	Description
0h	**[Default]**	All subslices have equal number of EUs.
1h		Subslice 2 has 7 EUs.
2h		Subslice 1 has 7 EUs.
3h		Subslice 0 has 7 EUs.

Programming Notes
SW must program these bits based on EU Disable Fuses in Slice 0.

GTSCRATCH

GTSCRATCH	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	4F100h-4F11Fh
Name:	GT Scratchpad
ShortName:	GTSCRATCH_*
Valid Projects:	
Power:	PG0
Reset:	soft

There are 8 instances of this register format.

Restriction

These registers are used by hardware and must not be used by software.

DWord	Bit	Description
0	31:0	**GT Sratchpad** GT Scratchpad

GTSP0

GTSP0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	130040h-130043h	
Name:	GT Scratchpad 0	
ShortName:	GTSP0	
Power:	PG0	
Reset:	soft	
DWord	**Bit**	**Description**
0	31:0	**GT scratch pad**

GTSP1

GTSP1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	130044h-130047h	
Name:	GT Scratchpad 1	
ShortName:	GTSP1	
Power:	PG0	
Reset:	soft	
DWord	**Bit**	**Description**
0	31:16	**GT scratch pad**
	15:0	**Multiple Force Wake** GT programs this field with the multiple force wake status. Software reads this field to find the status. Refer to MULTIFORCEWAKE 0xA188 register description for the usage.

GTSP2

GTSP2		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	130048h-13004Bh	
Name:	GT Scratchpad 2	
ShortName:	GTSP2	
Power:	PG0	
Reset:	soft	
DWord	**Bit**	**Description**
0	31:0	**GT scratch pad**

GTSP3

GTSP3		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	13004Ch-13004Fh	
Name:	GT Scratchpad 3	
ShortName:	GTSP3	
Power:	PG0	
Reset:	soft	
DWord	**Bit**	**Description**
0	31:0	**GT scratch pad**

GTSP4

GTSP4		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	130050h-130053h	
Name:	GT Scratchpad 4	
ShortName:	GTSP4	
Power:	PG0	
Reset:	soft	
DWord	**Bit**	**Description**
0	31:0	**GT scratch pad**

GTSP5

GTSP5			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Address:	130054h-130057h		
Name:	GT Scratchpad 5		
ShortName:	GTSP5		
Power:	PG0		
Reset:	soft		
DWord		**Bit**	**Description**
0		31:0	**GT scratch pad**

GTSP6

GTSP6		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	130058h-13005Bh	
Name:	GT Scratchpad 6	
ShortName:	GTSP6	
Power:	PG0	
Reset:	soft	
DWord	**Bit**	**Description**
0	31:0	**GT scratch pad**

GTSP7

GTSP7			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Address:	13005Ch-13005Fh		
Name:	GT Scratchpad 7		
ShortName:	GTSP7		
Power:	PG0		
Reset:	soft		
DWord		**Bit**	**Description**
0		31:1	**GT scratch pad**
		0	**Reserved**

GTT Cache Enable

GTT_CACHE_EN - GTT Cache Enable

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04024h

Enable GTT Cache for respective client(s), A0: Must program/observed this to all 0 due to Big Pages Bug 1898112

DWord	Bit	Description
0	31:0	**GTT Cache Enable for CS** Access: R/W Enable GTT Caching for all the client(s) below: 31: BLIT Engine (overrides individual enables of the units) 30: VEBX Engine (overrides individual enables of the units) 29: MFX Engine (overrides individual enables of the units) 28: GFX Engine (overrides individual enables of the units) 27-15: Reserved 14: VMCunit 13: VLFunit 12: BLBunit 11: VFWunit 10: VEOunit 9: HIZunit 8: RCZunit 7: RCCunit 6: ISCunit 5: DCunit 4: MTunit 3: SOLunit 2: VFunit 1: RSunit 0: CSunit Value: 00000000h — Name: **[Default]**

Hardware Scratch Read Write

HSRW_0_2_0_PCI - Hardware Scratch Read Write

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	16
Address:	00060h

This register is reserved as a HW scratchpad.

DWord	Bit	Description
0	15:0	**Reserved R/W** Default Value: 0000000000000000b Access: R/W Reserved for future usage.

Hardware Status Mask Register

HWSTAM - Hardware Status Mask Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0xFFFFFFFF
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	02098h-0209Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_RCSUNIT
Address:	12098h-1209Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_VCSUNIT0
Address:	1A098h-1A09Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_VECSUNIT
Address:	1C098h-1C09Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_VCSUNIT1
Address:	22098h-2209Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_BCSUNIT

The HWSTAM register has the same format as the Interrupt Control Registers. The bits in this register are mask bits that prevent the corresponding bits in the Interrupt Status Register from generating a Hardware Status Write (PCI write cycle). Any unmasked interrupt bit (HWSTAM bit set to 0) will allow the Interrupt Status Register to be written to the ISR location (within the memory page specified by the Hardware Status Page Address Register) when that Interrupt Status Register bit changes state.

Programming Notes

- To write the interrupt to the HWSP, the corresponding IMR bit must also be clear (enabled).
- At most 1 bit can be unmasked at any given time.

DWord	Bit	Description

HWSTAM - Hardware Status Mask Register

0	31:0	**Hardware Status Mask** Format: Array of Masks Refer to the Interrupt Control Register section for bit definitions. Reserved bits are RO. **Value** / **Name** FFFFFFFFh / **[Default]**

Hardware Status Page Address Register

HWS_PGA - Hardware Status Page Address Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1

Address:	02080h-02083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_RCSUNIT

Address:	12080h-12083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_VCSUNIT0

Address:	1A080h-1A083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_VECSUNIT

Address:	1C080h-1C083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_VCSUNIT1

Address:	22080h-22083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_BCSUNIT

This register is used to program the 4 KB-aligned System Memory address of the Hardware Status Page used to report hardware status into (typically cacheable) System Memory.

DWord	Bit	Description
0	31:12	**Address** Format: GraphicsAddress[31:12] This field is used by SW to specify Bits 31:12 of the 4 KB-aligned System Memory address of the 4 KB page known as the Hardware Status Page. The Global GTT is used to map this page from the graphics virtual address to physical address. **Programming Notes** If the Per-Process Virtual Address Space and Exec List Enable bit is set, HW requires that the status page is programmed to allow for the context switch status to be reported.
	11:0	**Reserved** Format: MBZ

HCP Bitstream Output Minimal Size Padding Count Report Register

HCP_MINSIZE_PADDING_COUNT - HCP Bitstream Output Minimal Size Padding Count Report Register

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E9B4h
Valid Projects:	

This register stores the count in bytes of **minimal size padding insertion. It is primarily provided for statistical data gathering.** This register is part of the context save and restore.

DWord	Bit	Description
0	31:0	**HCP MinSize Padding Count** Format: U32 Total number of bytes in the bitstream output contributing to minimal size padding operation. This count is updated each time when the padding count is incremented.

HCP CABAC Status

HCP_CABAC_STATUS - HCP CABAC Status

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Size (in bits):	32
Trusted Type:	1
Address:	1E904h

HCP CABAC status.

DWord	Bit	Description
0	31:12	**Reserved** Format: MBZ
	11	**Temporal Direction Motion Vector Out-of-Bound Error** Default Value: 0 Access: RO Format: U1 This flag indicates motion vectors calculated from the Temporal Direct Motion vector is larger than the allowed range.
	10:7	**Reserved** Format: MBZ
	6	**Motion Vector Delta SE** Default Value: 0 Access: RO Format: U1 This flag indicates out-of-bound motion vector delta SEs coded in the bit-stream.
	5	**Delta QP SE** Default Value: 0 Access: RO Format: U1 This flag indicates leading-one overflow during CABAC decode of cu_qp_delta_abs.
	4	**Residual Error** Default Value: 0 Access: RO Format: U1 This flag indicates out-of-bound absolute coefficient level SEs coded in the bit-stream.

HCP_CABAC_STATUS - HCP CABAC Status

	3	**Slice and Error** Default Value: 0 Access: RO Format: U1 This flag indicates a pre-mature end to the slice or an inconsistent end of slice on the last Ctb of a slice.
	2:1	**Reserved** Format: MBZ
	0	**Ctb Concealment Flag** Default Value: 0 Access: RO Format: U1 Each pulse from this flag indicates one Ctb is concealed by the HCP.

HCP Decode Status

HCP_DEC_STATUS - HCP Decode Status

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E900h

HCP Decode status.

DWord	Bit	Description
0	31:18	**Number of Ctbs Concealed** Default Value: 0 Format: U14 This 16-bit field indicates the number of Ctbs concealed during the decoding of the current frame. This field is cleared with the HCP_PIPE_MODE_SELECT command.
	17	**Frame Dec Active** Default Value: 0 Format: U1 This flag indicates that the decoder hardware is actively decoding a picture.
	16	**Indirect Bitstream ObjectAccess Upper Bound Error** Default Value: 0 Format: U1 This flag indicates that the upper bound bit-stream address was reached.
	15:0	**Bit-stream Error Flags** Default Value: 0 Format: U16 This 16-bit field indicates the number of bit stream errors detected for each bit field indicated in the CABAC Status register.

HCP Frame BitStream BIN Count

HCP_BIN_CT - HCP Frame BitStream BIN Count

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x723BA5C0
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E980h

This register stores the number of BINs decoded in a frame. This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:0	**HCP Frame Bit-stream BIN Count** Default Value: 723ba5c0h Format: U32 Total number of BINs decoded/ in current frame. This number is used with frame performance count to derive Bin/clk.

HCP Frame Motion Comp Miss Count

HCP_MISS_CT - HCP Frame Motion Comp Miss Count

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E988h
Valid Projects:	

This register stores the total number of cacheline hits occurred in the motion compensation cache per frame.

This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**HCP Frame Motion Comp cache miss Count** Format: U16 Total number of CL misses occurred in the 12KB cache of the motion compensation engine per frame. This number is used along with **HCP Frame Motion Comp Read Count** to derive motion comp cache miss/hit ratio.

HCP Frame Motion Comp Read Count

HCP_READ_CT - HCP Frame Motion Comp Read Count

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E984h
Valid Projects:	

This register stores the total number of reference picture read requests made by the Motion Compensation engine per frame.

This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:20	**Reserved** Format: MBZ
	19:0	**HCP Frame Motion Comp CL read request Count** Format: U20 Total number of reference picture read requests by the motion compensation engine per frame.

HCP Frame Performance Count

HCP_FRAME_PERF_CNT - HCP Frame Performance Count

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E960h
Valid Projects:	

This register stores the number of clock cycles spent decoding/encoding the current frame.

This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:0	**Count** Format: U32 Total number of clocks between frame start and frame end. This count is incremented on crm_clk.

HCP Image Status Control

HCP_IMAGE_STATUS_CONTROL - HCP Image Status Control

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	1E9BCh
Valid Projects:	

DWord	Bit	Description
0	31:24	**Cumulative Frame Delta QIndex** Format: S7 Used for Frame Level Multi-pass Rate Control. cu_qindex = input (first pass) cu_qindex + Cumulative Frame Delta Qindex. Pak does clamping to -127..127 after adding. Bit31 is the sign bit.
	23	**Reserved** Format: MBZ
	22:16	**Cumulative Frame Delta LF** Access: RO Format: S6 Used for Frame Level Multi-pass Rate Control. LF_level = input (first pass) LF_level + Cumulative Frame Delta LF level. Pak does clamping to -63..63 after adding.
	15:12	**Reserved** Format: MBZ
	11:8	**Total Num-Pass** Format: U4
	7:3	**Reserved** Format: MBZ
	2	**Frame Bit Count Violate - under run** Access: RO Format: U1 This can trigger Frame Level Multi-pass Rate Control. Set to 1 if frame bit count is less than or equal to FrameBitRateMin

HCP_IMAGE_STATUS_CONTROL - HCP Image Status Control

	1	**Frame Bit Count Violate - over run** Access: RO Format: U1 This can trigger Frame Level Multi-pass Rate Control. Set to 1 if frame bit count is less than or equal to FrameBitRateMax
	0	**LCU Bit Count Violate- overrun**

HCP Image Status Mask

HCP_IMAGE_STATUS_MASK - HCP Image Status Mask	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E9B8h
Valid Projects:	

This register stores the image status(flags).

DWord	Bit	Description
0	31:3	**Reserved** Format: MBZ
	2	**FrameBitRateMinReportMask** Same as **FrameSzUnderStatusEn** in HCP_PIC_STATE.
	1	**FrameBitRateMaxReportMask** Same as **FrameSzOverStatusEn** in HCP_PIC_STATE.
	0	**FrameLcuMaxReportMask**

HCP Memory Latency Count1

HCP_LAT_CT1 - HCP Memory Latency Count1

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E968h
Valid Projects:	

This register stores the max and min memory latency counts reported on reference read requests.

This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:24	**Max Request Count** Format: U8 This field indicates the maximum number of requests allowed by the memory sub-system channel.
	23:16	**Current Request Count** Format: U8 This field indicates the number of requests currently outstanding in the memory sub-system. This field should report with a value of zero at the end of frame; otherwise the motion compensation engine is most likely hung waiting for read data to be returned from sub-system.
	15:8	**HCP Reference picture read request - Max Latency Count in 8xMedia clock cycles** Format: U8 This field reports the maximum memory latency count on all reference reads requested by the motion compensation engine.
	7:0	**HCP Reference picture read request - Min Latency Count in 8xMedia clock cycles** Format: U8 This field reports the minimum memory latency count on all reference reads requested by the motion compensation engine.

HCP Memory Latency Count2

HCP_LAT_CT2 - HCP Memory Latency Count2

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E96Ch
Valid Projects:	

This register stores the accumulative memory latency count on reference picture read requests.

This register is not part of hardware context save and restore.

DWord	Bit	Description
0	25:0	**HCP Reference picture read request** Format: U26 **Accumulative Memory Latency Count for the entire frame in 8xMedia clock cycles.** The accumulative memory latency count of all reference reads requested by motion compensative engine per frame. This number is used with **HCP Frame Motion Comp Read Count** to derive average memory latency.

HCP Memory Latency Count3

HCP_LAT_CT3 - HCP Memory Latency Count3

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E970h
Valid Projects:	

This register stores the max and min memory latency counts reported on row-stored/bit-stream read requests. Max and current requests into memory sub-system engine.

This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:24	**Max Request Count** Format: U8 This field indicates the maximum number of requests allowed by the memory sub-system channel.
	23:16	**Current Request Count** Format: U8 This field indicates the number of requests currently outstanding in the memory sub-system. This field should report with a value of zero at the end of frame; otherwise the pre-fetch engine most likely hung waiting for read data to be returned from sub-system.
	15:8	**HCP row-stored/bit-stream read request - Max Latency Count in 8xMedia clock cycles** Format: U8 This field reports the maximum memory latency count on all row-stored/bit-stream reads requested by the memory pre-fetch engine.
	7:0	**HCP row-stored/bit-stream read request - Min Latency Count in 8xMedia clock cycles** Format: U8 This field reports the minimum memory latency count on all row-stored/bit-stream reads requested by the memory pre-fetch engine.

HCP Memory Latency Count4

HCP_LAT_CT4 - HCP Memory Latency Count4

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E974h
Valid Projects:	

This register stores the accumulative memory latency count on row-stored/bit-stream read requests.

This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:0	**HCP row-stored/bit-stream read request** Format: U32 **Accumulative Memory Latency Count for the entire frame in 8xMedia clock cycles.** The accumulative memory latency count of all row-stored/bit-stream reads requested by pre-fetch engine per frame. This number is used with **Frame row-stored/bit-stream memory read count** to derive average memory latency.

HCP Memory Latency Count5

HCP_LAT_CT5 - HCP Memory Latency Count5

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E978h
Valid Projects:	

This register stores the max and min memory latency counts reported on PAK Object read requests. Max and current requests into memory sub-system engine.

This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:24	**Max Request Count** Format: U8 This field indicates the maximum number of requests allowed by the memory sub-system channel.
	23:16	**Current Request Count** Format: U8 This field indicates the number of requests currently outstanding in the memory sub-system. This field should report with a value of zero at the end of frame; otherwise the pre-fetch engine most likely hung waiting for read data to be returned from sub-system.
	15:8	**MFX PAK Object read request - Max Latency Count in 8xMedia clock cycles** Format: U8 This field reports the maximum memory latency count on all PAK Object reads requested by the memory pre-fetch engine.
	7:0	**MFX PAK Object read request - Min Latency Count in 8xMedia clock cycles** Format: U8 This field reports the minimum memory latency count on all PAK Object reads requested by the memory pre-fetch engine.

HCP Memory Latency Count6

HCP_LAT_CT6 - HCP Memory Latency Count6

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E97Ch
Valid Projects:	

This register stores the max and min memory latency counts reported on Source Pixel read requests. Max and current requests into memory sub-system engine.

This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:24	**Max Request Count** Format: U8 This field indicates the maximum number of requests allowed by the memory sub-system channel.
	23:16	**Current Request Count** Format: U8 This field indicates the number of requests currently outstanding in the memory sub-system. This field should report with a value of zero at the end of frame; otherwise the pre-fetch engine most likely hung waiting for read data to be returned from sub-system.
	15:8	**FX Source Pixel read request - Max Latency Count in 8xMedia clock cycles** Format: U8 This field reports the maximum memory latency count on all Source Pixel reads requested by the memory pre-fetch engine. .
	7:0	**MFX Source Pixel read request - Min Latency Count in 8xMedia clock cycles** Format: U8 This field reports the minimum memory latency count on all Source Pixel reads requested by the memory pre-fetch engine.

HCP Picture Checksum cIdx0

HCP_PICTURE_CHECKSUM_CIDX0 - HCP Picture Checksum cIdx0

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E91Ch

- The HCP Picture Checksum cIdx0 register reports the 32-bit unsigned picture checksum for cIdx=0 calculated by the HCP hardware and whose algorithm is defined in Annex D of the HEVC standard specification.
- This calculated value is updated at the end of the frame.

DWord	Bit	Description
0	31:0	**Picture checksum cIdx0** Default Value: 0 Format: U32

HCP Picture Checksum cIdx1

HCP_PICTURE_CHECKSUM_CIDX1 - HCP Picture Checksum cIdx1

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E920h

- The HCP Picture Checksum cIdx1 register reports the 32-bit unsigned picture checksum for cIdx=1 calculated by the HCP hardware and whose algorithm is defined in Annex D of the HEVC standard specification.
- This calculated value is updated at the end of the frame.

DWord	Bit	Description
0	31:0	**Picture checksum cIdx1** Default Value: 0 Format: U32

HCP Picture Checksum cIdx2

HCP_PICTURE_CHECKSUM_CIDX2 - HCP Picture Checksum cIdx2

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E924h

- The HCP Picture Checksum cIdx2 register reports the 32-bit unsigned picture checksum for cIdx=2 calculated by the HCP hardware and whose algorithm is defined in Annex D of the HEVC standard specification.
- This calculated value is updated at the end of the frame.

DWord	Bit	Description
0	31:0	**Picture checksum cIdx2** Default Value: 0 Format: U32

HCP Qp Status Count

HCP_QP_STATUS_COUNT - HCP Qp Status Count

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000, 0x00000000
Access:	RO
Size (in bits):	64
Trusted Type:	1
Address:	1E9C0h
Valid Projects:	

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:0	**Cumulative QP** Format: U24 Cumulative QP for all LCU of a Frame (Can be used for computing average QP).
1	31:12	**Reserved**
	11:6	**Frame Max CU QP**
	5:0	**Frame Min CU QP**

HCP Reported Bitstream Output CABAC Bin Count Register

HCP_CABAC_BIN_COUNT_FRAME - HCP Reported Bitstream Output CABAC Bin Count Register

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E9ACh
Valid Projects:	

This register stores the count of number of bins per frame.

DWord	Bit	Description
0	31:0	**HCP Cabac Bin Count** Default Value: 0 Format: U32 Total number of BINs in the bitstream output per frame from the encoder. This count is updated for every time the bin counter is incremented and its reset at image start.

HCP Slice Performance Count

HCP_SLICE_PERF_CNT - HCP Slice Performance Count

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E964h
Valid Projects:	

This register stores the number of clock cycles spent decoding/encoding the current slice.

This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:0	**Count** Format: U32 Total number of clocks between slice start and slice end. This count is incremented on crm_clk.

HCP Unit Done

HCP_UNIT_DONE - HCP Unit Done	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E9D8h
Valid Projects:	

DWord	Bit	Description
0	31:25	**Reserved** Format: MBZ
	24:15	**Reserved** Format: MBZ
	14:11	**Reserved** Format: MBZ
	10:9	**Reserved**
	5	**HLC unit done** Format: U1
	4	**HLE unit done** Format: U1
	3	**HFQ unit done** Format: U1
	2	**HFT unit done** Format: U1
	1	**HRS unit done** Format: U1
	0	**HPO unit done** Format: U1

HDC TLB REQUEST CONTROL REGISTER

HDCTLB_REQ_CTRL - HDC TLB REQUEST CONTROL REGISTER

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32

This is a basic register template

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO

HDPORT_STATE

HDPORT_STATE

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	45050h-45053h
Name:	HDPORT State
ShortName:	HDPORT_STATE
Power:	PG0
Reset:	soft

This register is used to indicate when display resources have been pre-empted by hardware for the HDPORT feature. The usage is set during boot, before BIOS or software is active.
The list of DPLLs and DDIs in this register many not accurately reflect the total number of DPLLs and DDIs supported by display engine. HDPORT will not use any DPLL or DDI not listed here. It will not use any DPLL or DDI that is listed here, but not supported by the particular product or SKU.

Programming Notes

On Skylake, HDPORT will only use DPLL 2, DDI 3 (DDI D), DDI 2 (DDI C), and DDI 1 (DDI B).

Restriction

Display software must not use resources that are marked as being used by HDPORT.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15	**DPLL2 Used** This field indicates whether DPLL 2 is being used by HDPORT. 0b – Not used 1b – Used
	14	**DPLL3 Used** This field indicates whether DPLL 3 is being used by HDPORT. 0b – Not used 1b – Used

HDPORT_STATE

	13	**DPLL1 Used** This field indicates whether DPLL 1 is being used by HDPORT. Value: 0b = Not used; 1b = Used
	12	**DPLL0 Used** This field indicates whether DPLL 0 is being used by HDPORT. Value: 0b = Not used; 1b = Used
	11	**Spare 11**
	10	**Spare 10**
	9	**Spare 9**
	8	**DDI3 Type** This field indicates whether DDI 3 (DDI D) is being used in HDMI or DP mode by HDPORT. Value: 0b = DP; 1b = HDMI
	7	**DDI3 Used** This field indicates whether DDI 3 (DDI D) is being used by HDPORT. Value: 0b = Not used; 1b = Used
	6	**DDI2 Type** This field indicates whether DDI 2 (DDI C) is being used in HDMI or DP mode by HDPORT. Value: 0b = DP; 1b = HDMI
	5	**DDI2 Used** This field indicates whether DDI 2 (DDI C) is being used by HDPORT. Value: 0b = Not used; 1b = Used

HDPORT_STATE

	4	**DDI1 Type** This field indicates whether DDI 1 (DDI B) is being used by the HDPORT in HDMI or DP mode. **Value** / **Name** 0b / DP 1b / HDMI
	3	**DDI1 Used** This field indicates whether DDI 1 (DDI B) is being used by HDPORT. **Value** / **Name** 0b / Not used 1b / Used
	2	**DDI0 Type** This field indicates whether DDI 0 (DDI A and DDI E) is being used in HDMI or DP mode by HDPORT. **Value** / **Name** 0b / DP 1b / HDMI
	1	**DDI0 Used** This field indicates whether DDI 0 (DDI A and DDI E) is being used by HDPORT. **Value** / **Name** 0b / Not used 1b / Used
	0	**HDPORT Enabled** This field indicates whether HDPORT is enabled. **Value** / **Name** 0b / Disabled 1b / Enabled

Header Type

HDR2_0_2_0_PCI - Header Type

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	8
Address:	0000Eh

This register contains the Header Type of the IGD.

DWord	Bit	Description
0	7	**Multi Function Status** Default Value: 0b Access: RO Indicates if the device is a Multi-Function Device. The Value of this register is hardwired to 0, internal graphics is a single function.
	6:0	**Header Code** Default Value: 0000000b Access: RO This is a 7-bit value that indicates the Header Code for the IGD. This code is hardwired to the value 00h, indicating a type 0 configuration space format.

HS Invocation Counter

HS_INVOCATION_COUNT - HS Invocation Counter	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02300h

This register stores the number of patch objects processed by the HS unit. E.g., A PATCHLIST_2 topology with 6 vertices would cause this counter to increment by 3 (there are 3 2-vertex patch objects in that topology).This register is part of the context save and restore.

DWord	Bit	Description
0	63:32	**HS Invocation Count UDW** Number of patch objects processed by the HS stage. Updated only when HS Enable and HS Statistics Enable are set in 3DSTATE_HS
	31:0	**HS Invocation Count LDW** Number of patch objects processed by the HS stage. Updated only when HS Enable and HS Statistics Enable are set in 3DSTATE_HS

IA32 MTRR FIX4K_C0000 High

MTRR_FIX4K_C0000_H - IA32 MTRR FIX4K_C0000 High		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F13Ch	
Fixed MTRR to identify (C0000-C8000h).		
DWord	**Bit**	**Description**
0	31:0	**Range0 to Range7 Memory Type** Default Value: 00000000h Access: R/W Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.

IA32 MTRR FIX4K_C0000 Low

MTRR_FIX4K_C0000_L - IA32 MTRR FIX4K_C0000 Low		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F138h	
Fixed MTRR to identify (C0000-C8000h).		
DWord	**Bit**	**Description**
0	31:0	**Range0 to Range7 Memory Type** Default Value: 00000000h Access: R/W Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.

IA32 MTRR FIX4K_C8000 High

MTRR_FIX4K_C8000_H - IA32 MTRR FIX4K_C8000 High		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F144h	
Fixed MTRR to identify (C8000-D0000h).		
DWord	**Bit**	**Description**
0	31:0	**Range0 to Range7 Memory Type** Default Value: 00000000h Access: R/W Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.

IA32 MTRR FIX4K_C8000 Low

MTRR_FIX4K_C8000_L - IA32 MTRR FIX4K_C8000 Low		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F140h	
Fixed MTRR to identify (C8000-D0000h).		
DWord	**Bit**	**Description**
0	31:0	**Range0 to Range7 Memory Type** Default Value: 00000000h Access: R/W Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.

IA32 MTRR FIX4K_D0000 High

MTRR_FIX4K_D0000_H - IA32 MTRR FIX4K_D0000 High		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F14Ch	
Fixed MTRR to identify (D0000-D8000h)		
DWord	**Bit**	**Description**
0	31:0	**Range0 to Range7 Memory Type** Default Value: 00000000h Access: R/W Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.

IA32 MTRR FIX4K_D0000 Low

MTRR_FIX4K_D0000_L - IA32 MTRR FIX4K_D0000 Low		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F148h	
Fixed MTRR to identify (D0000-D8000h)		
DWord	**Bit**	**Description**
0	31:0	**Range0 to Range7 Memory Type** Default Value: 00000000h Access: R/W Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.

IA32 MTRR FIX4K_D8000 High

MTRR_FIX4K_D8000_H - IA32 MTRR FIX4K_D8000 High		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F154h	
Fixed MTRR to identify (D8000-E0000h)		
DWord	**Bit**	**Description**
0	31:0	**Range0 to Range7 Memory Type** Default Value: 00000000h Access: R/W Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.

IA32 MTRR FIX4K_D8000 Low

MTRR_FIX4K_D8000_L - IA32 MTRR FIX4K_D8000 Low		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F150h	
Fixed MTRR to identify (D8000-E0000h)		
DWord	**Bit**	**Description**
0	31:0	**Range0 to Range7 Memory Type** Default Value: 00000000h Access: R/W Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.

IA32 MTRR FIX4K_E0000 High

MTRR_FIX4K_E0000_H - IA32 MTRR FIX4K_E0000 High		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F15Ch	
Fixed MTRR to identify (E0000-E8000h).		
DWord	**Bit**	**Description**
0	31:0	**Range0 to Range7 Memory Type** Default Value: 00000000h Access: R/W Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.

IA32 MTRR FIX4K_E0000 Low

MTRR_FIX4K_E0000_L - IA32 MTRR FIX4K_E0000 Low		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F158h	
Fixed MTRR to identify (E0000-E8000h).		
DWord	**Bit**	**Description**
0	31:0	**Range0 to Range7 Memory Type** Default Value: 00000000h Access: R/W Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.

IA32 MTRR FIX4K_E8000 High

MTRR_FIX4K_E8000_H - IA32 MTRR FIX4K_E8000 High

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F164h

Fixed MTRR to identify (E8000-F0000h).

DWord	Bit	Description
0	31:0	**Range0 to Range7 Memory Type** Default Value: 00000000h Access: R/W Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.

IA32 MTRR FIX4K_E8000 Low

MTRR_FIX4K_E8000_L - IA32 MTRR FIX4K_E8000 Low		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F160h	
Fixed MTRR to identify (E8000-F0000h).		
DWord	**Bit**	**Description**
0	31:0	**Range0 to Range7 Memory Type** Default Value: 00000000h Access: R/W Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.

IA32 MTRR FIX4K_F0000 High

MTRR_FIX4K_F0000_H - IA32 MTRR FIX4K_F0000 High		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F16Ch	
Fixed MTRR to identify (F0000-F8000h).		
DWord	**Bit**	**Description**
0	31:0	**Range0 to Range7 Memory Type** Default Value: 00000000h Access: R/W Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.

IA32 MTRR FIX4K_F0000 Low

MTRR_FIX4K_F0000_L - IA32 MTRR FIX4K_F0000 Low		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F168h	
Fixed MTRR to identify (F0000-F8000h).		
DWord	**Bit**	**Description**
0	31:0	**Range0 to Range7 Memory Type** Default Value: 00000000h Access: R/W Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.

IA32 MTRR FIX4K_F8000 High

MTRR_FIX4K_F8000_H - IA32 MTRR FIX4K_F8000 High		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F174h	
Fixed MTRR to identify (F8000-100000h).		
DWord	**Bit**	**Description**
0	31:0	**Range0 to Range7 Memory Type** Default Value: 00000000h Access: R/W Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.

IA32 MTRR FIX4K_F8000 Low

MTRR_FIX4K_F8000_L - IA32 MTRR FIX4K_F8000 Low		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F170h	
Fixed MTRR to identify (F8000-100000h).		
DWord	**Bit**	**Description**
0	31:0	**Range0 to Range7 Memory Type** Default Value: 00000000h Access: R/W Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.

IA32 MTRR FIX16K_80000 High

MTRR_FIX16K_80000_H - IA32 MTRR FIX16K_80000 High		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F12Ch	
Fixed MTRR to identify 512K-768K of the main memory (80000-A0000h).		
DWord	**Bit**	**Description**
0	31:0	**Range0 to Range7 Memory Type** Default Value: 00000000h Access: R/W Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.

IA32 MTRR FIX16K_80000 Low

MTRR_FIX16K_80000_L - IA32 MTRR FIX16K_80000 Low		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F128h	
Fixed MTRR to identify 512K-768K of the main memory (80000-A0000h).		
DWord	**Bit**	**Description**
0	31:0	**Range0 to Range7 Memory Type** Default Value: 00000000h Access: R/W Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#.0

IA32 MTRR FIX16K_A0000 High

MTRR_FIX16K_A0000_H - IA32 MTRR FIX16K_A0000 High		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F134h	
Fixed MTRR to identify 768K-1024K of the main memory (A0000-C0000h).		
DWord	**Bit**	**Description**
0	31:0	**Range0 to Range7 Memory Type** Default Value: 00000000h Access: R/W Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.

IA32 MTRR FIX16K_A0000 Low

MTRR_FIX16K_A0000_L - IA32 MTRR FIX16K_A0000 Low		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F130h	
Fixed MTRR to identify 768K-1024K of the main memory (A0000-C0000h).		
DWord	**Bit**	**Description**
0	31:0	**Range0 to Range7 Memory Type** Default Value: 00000000h Access: R/W Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.

IA32 MTRR FIX64K_00000 High

MTRR_FIX64K_00000_H - IA32 MTRR FIX64K_00000 High		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F124h	
Fixed MTRR to identify 0-512K of the main memory (0-80000h).		
DWord	**Bit**	**Description**
0	31:0	**Range0 to Range7 Memory Type** Default Value: 00000000h Access: R/W Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.

IA32 MTRR FIX64K_00000 Low

MTRR_FIX64K_00000_L - IA32 MTRR FIX64K_00000 Low		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F120h	
Fixed MTRR to identify 0-512K of the main memory (0-80000h).		
DWord	**Bit**	**Description**
0	31:0	**Range0 to Range7 Memory Type** Default Value: 00000000h Access: R/W Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.

IA32 MTRR PHYSBASE0 High

MTRR_PHYSBASE0_H - IA32 MTRR PHYSBASE0 High

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F184h

Variable MTRR0

DWord	Bit	Description
0	31:7	**Reserved** Default Value: 00000000000000000000000000b Access: RO
	6:0	**PhysBase** Default Value: 0000000b Access: R/W Physical Base address[38:32] of the variable MTRR.

IA32 MTRR PHYSBASE0 Low

MTRR_PHYSBASE0_L - IA32 MTRR PHYSBASE0 Low

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F180h

Variable MTRR0

DWord	Bit	Description
0	31:12	**PhysBase** Default Value: 00000h Access: R/W Physical Base address[31:0] of the variable MTRR.
	11:8	**Reserved** Default Value: 0000b Access: RO
	7:0	**Memory Type** Default Value: 00h Access: R/W Identifies the memory type 00h-FFh.

IA32 MTRR PHYSBASE1 High

MTRR_PHYSBASE1_H - IA32 MTRR PHYSBASE1 High

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F194h

Variable MTRR1

DWord	Bit	Description
0	31:7	**Reserved** Default Value: 00000000000000000000000000b Access: RO
	6:0	**PhysBase** Default Value: 0000000b Access: R/W Physical Base address[38:32] of the variable MTRR.

IA32 MTRR PHYSBASE1 Low

MTRR_PHYSBASE1_L - IA32 MTRR PHYSBASE1 Low

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F190h

Variable MTRR1

DWord	Bit	Description
0	31:12	**PhysBase** Default Value: 00000h Access: R/W Physical Base address[31:0] of the variable MTRR.
	11:8	**Reserved** Default Value: 0000b Access: RO
	7:0	**Memory Type** Default Value: 00h Access: R/W Identifies the memory type 00h-FFh.

IA32 MTRR PHYSBASE2 High

MTRR_PHYSBASE2_H - IA32 MTRR PHYSBASE2 High

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F1A4h

Variable MTRR2

DWord	Bit	Description
0	31:7	**Reserved** Default Value: 00000000000000000000000000b Access: RO
	6:0	**PhysBase** Default Value: 0000000b Access: R/W Physical Base address[38:32] of the variable MTRR.

IA32 MTRR PHYSBASE2 Low

MTRR_PHYSBASE2_L - IA32 MTRR PHYSBASE2 Low

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F1A0h

Variable MTRR2

DWord	Bit	Description
0	31:12	**PhysBase** Default Value: 00000h Access: R/W Physical Base address[31:0] of the variable MTRR.
	11:8	**Reserved** Default Value: 0000b Access: RO
	7:0	**Memory Type** Default Value: 00h Access: R/W Identifies the memory type 00h-FFh.

IA32 MTRR PHYSBASE3 High

MTRR_PHYSBASE3_H - IA32 MTRR PHYSBASE3 High

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F1B4h

Variable MTRR3

DWord	Bit	Description
0	31:7	**Reserved** Default Value: 00000000000000000000000000b Access: RO
	6:0	**PhysBase** Default Value: 0000000b Access: R/W Physical Base address[38:32] of the variable MTRR.

IA32 MTRR PHYSBASE3 Low

MTRR_PHYSBASE3_L - IA32 MTRR PHYSBASE3 Low

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F1B0h

Variable MTRR3

DWord	Bit	Description
0	31:12	**PhysBase** Default Value: 00000h Access: R/W Physical Base address[31:0] of the variable MTRR.
	11:8	**Reserved** Default Value: 0000b Access: RO
	7:0	**Memory Type** Default Value: 00h Access: R/W Identifies the memory type 00h-FFh.

IA32 MTRR PHYSBASE4 High

MTRR_PHYSBASE4_H - IA32 MTRR PHYSBASE4 High

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F1C4h

Variable MTRR4

DWord	Bit	Description
0	31:7	**Reserved** Default Value: 00000000000000000000000000b Access: RO
	6:0	**PhysBase** Default Value: 0000000b Access: R/W Physical Base address[38:32] of the variable MTRR.

IA32 MTRR PHYSBASE4 Low

MTRR_PHYSBASE4_L - IA32 MTRR PHYSBASE4 Low

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F1C0h

Variable MTRR4

DWord	Bit	Description
0	31:12	**PhysBase** Default Value: 00000h Access: R/W Physical Base address[31:0] of the variable MTRR.
	11:8	**Reserved** Default Value: 0000b Access: RO
	7:0	**Memory Type** Default Value: 00h Access: R/W Identifies the memory type 00h-FFh

IA32 MTRR PHYSBASE5 High

MTRR_PHYSBASE5_H - IA32 MTRR PHYSBASE5 High

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F1D4h

Variable MTRR5

DWord	Bit	Description
0	31:7	**Reserved** Default Value: 00000000000000000000000000b Access: RO
	6:0	**PhysBase** Default Value: 0000000b Access: R/W Physical Base address[38:32] of the variable MTRR.

IA32 MTRR PHYSBASE5 Low

MTRR_PHYSBASE5_L - IA32 MTRR PHYSBASE5 Low

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F1D0h

Variable MTRR5

DWord	Bit	Description
0	31:12	**PhysBase** Default Value: 00000h Access: R/W Physical Base address[31:0] of the variable MTRR.
	11:8	**Reserved** Default Value: 0000b Access: RO
	7:0	**Memory Type** Default Value: 00h Access: R/W Identifies the memory type 00h-FFh.

IA32 MTRR PHYSBASE6 High

MTRR_PHYSBASE6_H - IA32 MTRR PHYSBASE6 High

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F1E4h

Variable MTRR6

DWord	Bit	Description
0	31:7	**Reserved** Default Value: 00000000000000000000000000b Access: RO
	6:0	**PhysBase** Default Value: 0000000b Access: R/W Physical Base address[38:32] of the variable MTRR.

IA32 MTRR PHYSBASE6 Low

MTRR_PHYSBASE6_L - IA32 MTRR PHYSBASE6 Low

Register Space: MMIO: 0/2/0
Default Value: 0x00000000
Size (in bits): 32

Address: 0F1E0h

Variable MTRR6

DWord	Bit	Description
0	31:12	**PhysBase** Default Value: 00000h Access: R/W Physical Base address[31:0] of the variable MTRR.
	11:8	**Reserved** Default Value: 0000b Access: RO
	7:0	**Memory Type** Default Value: 00h Access: R/W Identifies the memory type 00h-FFh.

IA32 MTRR PHYSBASE7 High

MTRR_PHYSBASE7_H - IA32 MTRR PHYSBASE7 High

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F1F4h

Variable MTRR7

DWord	Bit	Description
0	31:7	**Reserved** Default Value: 00000000000000000000000000b Access: RO
	6:0	**PhysBase** Default Value: 0000000b Access: R/W Physical Base address[38:32] of the variable MTRR.

IA32 MTRR PHYSBASE7 Low

MTRR_PHYSBASE7_L - IA32 MTRR PHYSBASE7 Low		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F1F0h	
Variable MTRR7		
DWord	**Bit**	**Description**
0	31:12	**PhysBase** Default Value: 00000h Access: R/W Physical Base address[31:0] of the variable MTRR.
	11:8	**Reserved** Default Value: 0000b Access: RO
	7:0	**Memory Type** Default Value: 00h Access: R/W Identifies the memory type 00h-FFh.

IA32 MTRR PHYSBASE8 High

MTRR_PHYSBASE8_H - IA32 MTRR PHYSBASE8 High

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F204h

Variable MTRR8

DWord	Bit	Description
0	31:7	**Reserved** Default Value: 00000000000000000000000000b Access: RO
	6:0	**PhysBase** Default Value: 0000000b Access: R/W Physical Base address[38:32] of the variable MTRR.

IA32 MTRR PHYSBASE8 Low

MTRR_PHYSBASE8_L - IA32 MTRR PHYSBASE8 Low

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F200h

Variable MTRR8

DWord	Bit	Description
0	31:12	**PhysBase** Default Value: 00000h Access: R/W Physical Base address[31:0] of the variable MTRR
	11:8	**Reserved** Default Value: 0000b Access: RO
	7:0	**Memory Type** Default Value: 00h Access: R/W Identifies the memory type 00h-FFh.

IA32 MTRR PHYSBASE9 High

MTRR_PHYSBASE9_H - IA32 MTRR PHYSBASE9 High

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F214h

Variable MTRR9

DWord	Bit	Description
0	31:7	**Reserved** Default Value: 00000000000000000000000000b Access: RO
	6:0	**PhysBase** Default Value: 0000000b Access: R/W Physical Base address[38:32] of the variable MTRR.

IA32 MTRR PHYSBASE9 Low

MTRR_PHYSBASE9_L - IA32 MTRR PHYSBASE9 Low

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F210h

Variable MTRR9

DWord	Bit	Description
0	31:12	**PhysBase** Default Value: 00000h Access: R/W Physical Base address[31:0] of the variable MTRR.
	11:8	**Reserved** Default Value: 0000b Access: RO
	7:0	**Memory Type** Default Value: 00h Access: R/W Identifies the memory type 00h-FFh.

IA32 MTRR PHYSMASK0 High

MTRR_PHYSMASK0_H - IA32 MTRR PHYSMASK0 High

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F18Ch

Variable MTRR0

DWord	Bit	Description
0	31:7	**Reserved** Default Value: 00000000000000000000000000b Access: RO
	6:0	**PhysMask** Default Value: 0000000b Access: R/W Physical MASK for the address[38:32] of the variable MTRR.

IA32 MTRR PHYSMASK0 Low

MTRR_PHYSMASK0_L - IA32 MTRR PHYSMASK0 Low

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F188h

Variable MTRR0

DWord	Bit	Description
0	31:12	**PhysMask** Default Value: 00000h Access: R/W Physical MASK for the address[31:0] of the variable MTRR.
	11	**Valid** Default Value: 0b Access: R/W Valid bit showing that MTRR decode is active.
	10:0	**Reserved** Default Value: 00000000000b Access: RO

IA32 MTRR PHYSMASK1 High

MTRR_PHYSMASK1_H - IA32 MTRR PHYSMASK1 High

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F19Ch

Variable MTRR1

DWord	Bit	Description
0	31:7	**Reserved** Default Value: 00000000000000000000000000b Access: RO
	6:0	**PhysMask** Default Value: 0000000b Access: R/W Physical MASK for the address[38:32] of the variable MTRR.

IA32 MTRR PHYSMASK1 Low

MTRR_PHYSMASK1_L - IA32 MTRR PHYSMASK1 Low

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F198h

Variable MTRR1

DWord	Bit	Description
0	31:12	**PhysMask** Default Value: 00000h Access: R/W Physical MASK for the address[31:0] of the variable MTRR.
	11	**Valid** Default Value: 0b Access: R/W Valid bit showing that MTRR decode is active.
	10:0	**Reserved** Default Value: 00000000000b Access: RO

IA32 MTRR PHYSMASK2 High

MTRR_PHYSMASK2_H - IA32 MTRR PHYSMASK2 High

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F1ACh

Variable MTRR2

DWord	Bit	Description
0	31:7	**Reserved** Default Value: 00000000000000000000000000b Access: RO
	6:0	**PhysMask** Default Value: 0000000b Access: R/W Physical MASK for the address[38:32] of the variable MTRR.

IA32 MTRR PHYSMASK2 Low

MTRR_PHYSMASK2_L - IA32 MTRR PHYSMASK2 Low

Register Space: MMIO: 0/2/0
Default Value: 0x00000000
Size (in bits): 32

Address: 0F1A8h

Variable MTRR2

DWord	Bit	Description
0	31:12	**PhysMask** Default Value: 00000h Access: R/W Physical MASK for the address[31:0] of the variable MTRR.
	11	**Valid** Default Value: 0b Access: R/W Valid bit showing that MTRR decode is active.
	10:0	**Reserved** Default Value: 00000000000b Access: RO

IA32 MTRR PHYSMASK3 High

MTRR_PHYSMASK3_H - IA32 MTRR PHYSMASK3 High

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F1BCh

Variable MTRR3

DWord	Bit	Description
0	31:7	**Reserved** Default Value: 00000000000000000000000000b Access: RO
	6:0	**PhysMask** Default Value: 0000000b Access: R/W Physical MASK for the address[38:32] of the variable MTRR.

IA32 MTRR PHYSMASK3 Low

MTRR_PHYSMASK3_L - IA32 MTRR PHYSMASK3 Low

Register Space: MMIO: 0/2/0
Default Value: 0x00000000
Size (in bits): 32

Address: 0F1B8h

Variable MTRR3

DWord	Bit	Description
0	31:12	**PhysMask** Default Value: 00000h Access: R/W Physical MASK for the address[31:0] of the variable MTRR.
	11	**Valid** Default Value: 0b Access: R/W Valid bit showing that MTRR decode is active.
	10:0	**Reserved** Default Value: 00000000000b Access: RO

IA32 MTRR PHYSMASK4 High

MTRR_PHYSMASK4_H - IA32 MTRR PHYSMASK4 High

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F1CCh

Variable MTRR4

DWord	Bit	Description
0	31:7	**Reserved** Default Value: 00000000000000000000000000b Access: RO
	6:0	**PhysMask** Default Value: 0000000b Access: R/W Physical MASK for the address[38:32] of the variable MTRR.

IA32 MTRR PHYSMASK4 Low

MTRR_PHYSMASK4_L - IA32 MTRR PHYSMASK4 Low

Register Space: MMIO: 0/2/0
Default Value: 0x00000000
Size (in bits): 32

Address: 0F1C8h

Variable MTRR4

DWord	Bit	Description
0	31:12	**PhysMask** Default Value: 00000h Access: R/W Physical MASK for the address[31:0] of the variable MTRR.
	11	**Valid** Default Value: 0b Access: R/W Valid bit showing that MTRR decode is active.
	10:0	**Reserved** Default Value: 00000000000b Access: RO

IA32 MTRR PHYSMASK5 High

MTRR_PHYSMASK5_H - IA32 MTRR PHYSMASK5 High

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F1DCh

Variable MTRR5

DWord	Bit	Description
0	31:7	**Reserved** Default Value: 00000000000000000000000000b Access: RO
	6:0	**PhysMask** Default Value: 0000000b Access: R/W Physical MASK for the address[38:32] of the variable MTRR.

IA32 MTRR PHYSMASK5 Low

MTRR_PHYSMASK5_L - IA32 MTRR PHYSMASK5 Low		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F1D8h	
Variable MTRR5		
DWord	**Bit**	**Description**
0	31:12	**PhysMask** Default Value: 00000h Access: R/W Physical MASK for the address[31:0] of the variable MTRR.
	11	**Valid** Default Value: 0b Access: R/W Valid bit showing that MTRR decode is active.
	10:0	**Reserved** Default Value: 00000000000b Access: RO

IA32 MTRR PHYSMASK6 High

MTRR_PHYSMASK6_H - IA32 MTRR PHYSMASK6 High

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F1ECh

Variable MTRR6

DWord	Bit	Description
0	31:7	**Reserved** Default Value: 00000000000000000000000000b Access: RO
	6:0	**PhysMask** Default Value: 0000000b Access: R/W Physical MASK for the address[38:32] of the variable MTRR.

IA32 MTRR PHYSMASK6 Low

MTRR_PHYSMASK6_L - IA32 MTRR PHYSMASK6 Low

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F1E8h

Variable MTRR6

DWord	Bit	Description
0	31:12	**PhysMask** Default Value: 00000h Access: R/W Physical MASK for the address[31:0] of the variable MTRR.
	11	**Valid** Default Value: 0b Access: R/W Valid bit showing that MTRR decode is active.
	10:0	**Reserved** Default Value: 00000000000b Access: RO

IA32 MTRR PHYSMASK7 High

MTRR_PHYSMASK7_H - IA32 MTRR PHYSMASK7 High

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F1FCh

Variable MTRR7

DWord	Bit	Description
0	31:7	**Reserved** Default Value: 00000000000000000000000000b Access: RO
	6:0	**PhysMask** Default Value: 0000000b Access: R/W Physical MASK for the address[38:32] of the variable MTRR.

IA32 MTRR PHYSMASK7 Low

MTRR_PHYSMASK7_L - IA32 MTRR PHYSMASK7 Low

Register Space: MMIO: 0/2/0
Default Value: 0x00000000
Size (in bits): 32

Address: 0F1F8h

Variable MTRR7

DWord	Bit	Description
0	31:12	**PhysMask** Default Value: 00000h Access: R/W Physical MASK for the address[31:0] of the variable MTRR.
	11	**Valid** Default Value: 0b Access: R/W Valid bit showing that MTRR decode is active.
	10:0	**Reserved** Default Value: 00000000000b Access: RO

IA32 MTRR PHYSMASK8 High

MTRR_PHYSMASK8_H - IA32 MTRR PHYSMASK8 High

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F20Ch

Variable MTRR8

DWord	Bit	Description
0	31:7	**Reserved** Default Value: 00000000000000000000000000b Access: RO
	6:0	**PhysMask** Default Value: 0000000b Access: R/W Physical MASK for the address[38:32] of the variable MTRR.

IA32 MTRR PHYSMASK8 Low

MTRR_PHYSMASK8_L - IA32 MTRR PHYSMASK8 Low		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F208h	
Variable MTRR8		
DWord	**Bit**	**Description**
0	31:12	**PhysMask** Default Value: 00000h Access: R/W Physical MASK for the address[31:0] of the variable MTRR.
	11	**Valid** Default Value: 0b Access: R/W Valid bit showing that MTRR decode is active.
	10:0	**Reserved** Default Value: 00000000000b Access: RO

IA32 MTRR PHYSMASK9 High

MTRR_PHYSMASK9_H - IA32 MTRR PHYSMASK9 High

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F21Ch

Variable MTRR9

DWord	Bit	Description
0	31:7	**Reserved** Default Value: 00000000000000000000000000b Access: RO
	6:0	**PhysMask** Default Value: 0000000b Access: R/W Physical MASK for the address[38:32] of the variable MTRR.

IA32 MTRR PHYSMASK9 Low

MTRR_PHYSMASK9_L - IA32 MTRR PHYSMASK9 Low

Register Space: MMIO: 0/2/0
Default Value: 0x00000000
Size (in bits): 32

Address: 0F218h

Variable MTRR9

DWord	Bit	Description
0	31:12	**PhysMask** Default Value: 00000h Access: R/W Physical MASK for the address[31:0] of the variable MTRR.
	11	**Valid** Default Value: 0b Access: R/W Valid bit showing that MTRR decode is active.
	10:0	**Reserved** Default Value: 00000000000b Access: RO

IA Vertices Count

IA_VERTICES_COUNT - IA Vertices Count	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02310h
Valid Projects:	

This register stores the count of vertices processed by VF. This register is part of the context save and restore.

DWord	Bit	Description
0	63:32	**IA Vertices Count Report UDW** Total number of vertices fetched by the VF stage. This count is updated for every input vertex as long as Statistics Enable is set in VF_STATE (see the Vertex Fetch Chapter in the 3D Volume.)
	31:0	**IA Vertices Count Report LDW** Total number of vertices fetched by the VF stage. This count is updated for every input vertex as long as Statistics Enable is set in VF_STATE (see the Vertex Fetch Chapter in the 3D Volume.)

IDI Cacheable Register

IDICA - IDI Cacheable Register		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	09014h	
Cacheable		
DWord	**Bit**	**Description**
0	31:30	**LLCWBCA** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.
	29:28	**LLCPRFOCA** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.
	27:26	**LLCPCCA** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.
	25:24	**LLCPDCA** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.
	23:22	**CLFCA** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.
	21:20	**POCA** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.
	19:18	**ITMCA** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.

IDICA - IDI Cacheable Register

	17:16	**WCILFCA** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.
	15:14	**WILCA** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.
	13:12	**WCILCA** Access: R/W >NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.
	11:10	**WBMCA** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.
	9:8	**RFOCA** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.
	7:6	**PORINCA** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.
	5:4	**PRDCA** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.
	3:2	**DRDCA** Access: R/W 00b: Whatever the logic decides (so force feature is disabled) - Default. 01b: Always drive 0. 10b: Always drive 1. 11b: Reserved.
	1:0	**CRDCA** Access: R/W 00b: Whatever the logic decides (so force feature is disabled) - Default. 01b: Always drive 0. 10b: Always drive 1. 11b: Reserved.

IDI Control register

IDICR - IDI Control register		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000181	
Size (in bits):	32	
Address:	09008h	

DWord	Bit	Description
0	31:24	**Spares** Access: R/W ECO purposes and Reserved.
	23:22	**QOS setting for Frame Buffer Caching** Access: R/W The value determines the quality of service setting of Frame Buffers while being cached in Last Level Cache/eDRAM. GFX Driver has to set the value of QOS after enabling Frame Buffer caching and deciding which ways of LLC is allocated for which QOS values. 00 : QOS setting of 00 used for Frame Buffers 01 : QOS setting of 01 used for Frame Buffers 10 : QOS setting of 10 used for Frame Buffers 11 : QOS setting of 11 used for Frame Buffers
	21:16	**IDI HASH MASK** Access: R/W IDI HASH MASK: When a corresponding bit is set, the address line going into HASH for CBO ID calculation is forced to logic0. 21=> Address Bit[11] 20=> Address Bit[10] 19=> Address Bit[9] 18=> Address Bit[8] 17=> Address Bit[7] 16=> Address Bit[6] Note: It is required for GFX Driver to set [19:16] to 1 when eDRAM configuration is enabled. For Skylake, S/W is not needed to program this register as eDRAM is a memory side cache.
	15	**GFX Data regulation** Access: R/W BGF data regulation for incoming streams with chunkID detection.
	14:10	**Reserved**
	9	**RSVD** Access: RO
	8	**Push Write Enable** Default Value: 1b

IDICR - IDI Control register

	Access:	R/W

Push Write Enable: Push writes are a new mechanism to deliver write data to Uncore. It provides two advantages. 1) Reduced TAG pass requirements 2) Only way to allocate into eLLC without going thru LLC.
The downside is the fact that push writes are weakly ordered which means a synchronizing event is required to guarantee consistency of data.

7 **Snoop Request control**

Default Value:	1b
Access:	R/W

1: Snoop is allowed only when there are no Pending response.
0: Means after every 24 u2c response we allow one snoop request to bypass

6:4 **LRUHint**

Access:	R/W

000b: No LRUHint command sent to uncore. It is reserved.
001b: If LRUHint is asserted from SQ with a read or write command, IDI dispatcher chooses to send an LlcPrefData.
101b: If LRUHint is asserted from SQ with a read or write command, IDI dispatcher chooses to send an LLCPrefCode command on the C2U request channel.
010b: If LRUHint is asserted from SQ with a read/write command, IDI dispatcher chooses to send an LlcPrefRFO command on the C2U request channel.
011b: If LRUHint is asserted from SQ with a read, IDI dispatcher chooses to send LlcPrefData command on the C2U request channel. If LRUHint is asserted from SQ with a write, IDI dispatcher chooses to send LlcPrefRFO command on the C2U request channel.
111b: If LRUHint is asserted from SQ with a read, IDI dispatcher chooses to send LLCPrefCode command on the C2U request channel. If LRUHint is asserted from SQ with a write, IDI dispatcher chooses to send LlcPrefRFO command on the C2U request channel.

3 **RSVD**

Access:	RO

2 **Resport 1 disable**

Access:	R/W

0: Default value - Both the Response ports on the BGF side are enabled.
1: Rsp Port1 Disable - Response Port1 is disable on the BGF Side.

1:0 **SQ Grant Counter**

Default Value:	01b
Access:	R/W

SQ grant counter - 2-bit grant counter for SQ requests
00b: 1 grant.
01b: 2 grants.
10b: 4 grants.
11b: 8 grants.

IDI HASH Mask Register

DRBIDI3 - IDI HASH Mask Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	01948h

DWord	Bit	Description
0	31:10	**Reserved** Access: RO Reserved
	9:8	**Reserved**
	7:6	**Reserved** Access: RO Reserved
	5:0	**IDI HASH MASK** Access: R/W When corresponding MASK bit is set, the masked address bit going into HASH calculator is forced to be logic0. 21=> Address Bit[11] 20=> Address Bit[10] 19=> Address Bit[9] 18=> Address Bit[8] 17=> Address Bit[7] 16=> Address Bit[6] For Gen8 with 128MB eDRAM eLLC, bits[5:0] should be set to 001111 (matching 9008[21:16] IDI hash mask) In SKL, it is no longer needed for s/w to program this field given that eDRAM is a memory side cache

IDI Look up Register

IDILK2 - IDI Look up Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	08514h

IDI Look up Register

DWord	Bit	Description
0	31:30	**Spares** Access: R/W Lock
	28	**Colloc bit for Slice 5** Access: R/W Lock Co-located indicates that the Collocated Cbo should receive this request.
	27	**Direction bit for Slice 5** Access: R/W Lock In Half ring uncore topologies this indicates if the 1: Going Up. 0: Going Down.
	26	**Polarity bit for Slice 5** Access: R/W Lock Polarity based on the current core Slice ID and the Destination Cbo ID - should this request be sent to the rings in Even or Odd cycles (this is basically the Distance between the source and destination). 1 - Even. 0 - Odd.
	25	**For Me for Slice 5** Access: R/W Lock The next slice the Target of this request (MyNeigbourId == DestCboId).
	24	**Spares2** Access: R/W Lock Reserved for Slice 4.
	23	**Colloc bit for Slice 4** Access: R/W Lock Co-located indicates that the Collocated Cbo should receive this request.

IDILK2 - IDI Look up Register

	22	**Direction bit for Slice 4** Access: R/W Lock In Half ring uncore topologies this indicates if the 1: Going Up. 0: Going Down.
	21	**Polarity Bit for Slice 4** Access: R/W Lock Polarity based on the current core Slice ID and the Destination Cbo ID - should this request be sent to the rings in Even or Odd cycles (this is basically the Distance between the source and destination). 1 - Even. 0 - Odd.
	20	**For Me bit for Slice 4** Access: R/W Lock The next slice the Target of this request (MyNeigbourId == DestCboId).
	19	**Spare for Slice 3** Access: R/W Lock Reserved for Slice 3.
	18	**Colloc bit for Slice 3** Access: R/W Lock Co-located indicates that the Collocated Cbo should receive this request.
	17	**Direction bit for S3** Access: R/W Lock In Half ring uncore topologies this indicates if the 1: Going Up. 0: Going Down.
	16	**Polarity Bit for Slice 3** Access: R/W Lock Polarity based on the current core Slice ID and the Destination Cbo ID - should this request be sent to the rings in Even or Odd cycles (this is basically the Distance between the source and destination). 1 - Even. 0 - Odd.

IDILK2 - IDI Look up Register

	15	**For Me Bit for Slice 3** Access: R/W Lock The next slice the Target of this request (MyNeigbourId == DestCboId).
	14	**Spare for Slice 2** Access: R/W Lock Reserved for Slice 2.
	13	**Colloc bit for Slice 2** Access: R/W Lock Co-located indicates that the Collocated Cbo should receive this request.
	12	**Direction Bit for Slice 2** Access: R/W Lock In Half ring uncore topologies this indicates if the 1: Going Up. 0: Going Down.
	11	**Polarity Bit for Slice 2** Access: R/W Lock Polarity based on the current core Slice ID and the Destination Cbo ID - should this request be sent to the rings in Even or Odd cycles (this is basically the Distance between the source and destination). 1 - Even. 0 - Odd.
	10	**For me Bit for Slice 2** Access: R/W Lock The next slice the Target of this request (MyNeigbourId == DestCboId).
	9	**Spare for Slice 1** Access: R/W Lock Reserved for Slice 1.
	8	**Colloc Bit for Slice 1** Access: R/W Lock Co-located indicates that the Collocated Cbo should receive this request.

IDILK2 - IDI Look up Register

	7	**Direction Bit for Slice 1** Access: R/W Lock In Half ring uncore topologies this indicates if the 1: Going Up. 0: Going Down.
	6	**Polarity Bit for Slice 1** Access: R/W Lock Polarity based on the current core Slice ID and the Destination Cbo ID - should this request be sent to the rings in Even or Odd cycles (this is basically the Distance between the source and destination). 1 - Even. 0 - Odd.
	5	**For Me Bit for Slice 1** Access: R/W Lock The next slice the Target of this request (MyNeigbourId == DestCboId).
	4	**Spare for Slice 0** Access: R/W Lock Reserved for Slice 0.
	3	**Colloc Bit for Slice 0** Access: R/W Lock Co-located indicates that the Collocated Cbo should receive this request.
	2	**Direction Bit in Slice0** Access: R/W Lock Direction bit for Slice0: In Half ring uncore topologies this indicates if the request needs to be driven on the Up going (1) or the down (0) going ring direction. For Full ring it indicates Clock-wise (1) or counter clock-wise directions. 1: Going Up. 0: Going Down.
	1	**Polarity Bit for Slice 0** Access: R/W Lock Polarity based on the current core Slice ID and the Destination Cbo ID - should this request be sent to the rings in Even or Odd cycles (this is basically the Distance between the source and destination). 1 - Even. 0 - Odd.

IDILK2 - IDI Look up Register

	0	**For Me bit for Slice0** Access: R/W Lock The next slice the Target of this request (MyNeigbourId == DestCboId).

IDILook up Table register

IDILK1 - IDILook up Table register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	08510h

IDI Look Up register I

DWord	Bit	Description
0	31:21	**Spares** Access: R/W Lock
	20:16	**GT Logical ID** Access: R/W Lock Logical ID for GT.
	15:14	**Spares1** Access: R/W Lock Reserved for SA slice.
	13	**Colloc bit for SA Slice** Access: R/W Lock Co-located indicates that the Collocated Cbo should receive this request.
	12	**Direction Bit for SA** Access: R/W Lock In Half ring uncore topologies this indicates if the request needs to be driven on the Up going (1) or the down (0) going ring direction. For Full ring it indicates Clock-wise (1) or counter clock-wise directions. 1: Going Up. 0: Going Down.
	11	**Polarity bit for SA Slice** Access: R/W Lock Polarity based on the current core Slice ID and the Destination Cbo ID - should this request be sent to the rings in Even or Odd cycles (this is basically the Distance between the source and destination). 1 - Even. 0 - Odd.

IDILK1 - IDILook up Table register

	10	**For Me bit for SA** Access: R/W Lock The next slice the Target of this request (MyNeigbourId == DestCboId).
	9:5	**Number of LLC SA Slices** Access: R/W Lock Number of Slice information in the system. This register contains the number of LLC cache slices on the RING. Default: 0000b. Value for SNB is either 2 or 4.
	4:0	**Colocated Slice ID for GT** Access: R/W Lock This register contains the ID of the slice that is servicing GT's co-located cycles. The default is for slice0 to service GT.

IDI MESSAGES

IDIMSG - IDI MESSAGES

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	08500h

IDI Message Register

DWord	Bit	Description
0	31:16	**Mask Bits** Access: RO Reserved.
	15:13	**RSVD** Access: RO
	12	**MCHECK COMPLETE** Access: R/W iMPH writes to this bit to initiate MCHECK COMPLETE Routine (PPPE flow). MBCunit will clear this bit once the PPPE flow is complete
	11	**Spare** Access: R/W Spare Messaging Bit with self-clear.
	10	**MBC Busy ACK** Access: R/W 1 - Busy ACK from GPMunit(Non-Idle). 0 - Non Busy ACK from Gpmunit (Idle). This bit is valid only if 26th Bit is set.
	9	**Reserved**
	8	**Reserved**
	7	**RSVD** Access: RO

IDIMSG - IDI MESSAGES

	6	**Request to Block IDI** Access: R/W Block and Unblock IDI Request - usually done during CPD Entry and Exits. This is valid only if 22nd bit is set. Block IDI - CPD Entry = 1. Unblock IDI CPD Exit = 0.
	5	**Unblock MMIO ack** Access: R/W Unblock MMIO ACK coming from SA. This is valid only if 21st bit is set.
	4	**Mbcunit Arbitration request/Release ACK** Access: R/W Arbitration request is sent during the MAE update. The ack is received from GPMunit. This is valid only if 20th bit is set. Arb req ack = 1. Arb release ack = 0.
	3	**IDI Shutdown request** Access: R/W IDI Shutdown Request from GPM to MBCunit. This is valid only if the 19th bit is set.
	2	**IDI Wakeup Message** Access: R/W IDI wakeup message from PM to MBCunit. This is valid only if 18th bit is set.
	1	**Credit Active De-assertreq ACK** Access: R/W Credit Active De-assertreq ACK - GPMunit sends to the MBCunit. This is valid only if the 17th bit of this register is set.
	0	**Reserved**

IDI Self Snoop Register

IDISLFSNP - IDI Self Snoop Register		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	09018h	
Cacheable		
DWord	**Bit**	**Description**
0	31:30	**LLCWBSNP** Access: R/W 00b: Whatever the logic decides (so force feature is disabled) - Default. 01b: Always drive 0. 10b: Always drive 1. 11b: Reserved.
	29:28	**LLCPRFOSNP** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.
	27:26	**LLCPCSNP** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.
	25:24	**LLCPDSNP** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.
	23:22	**CLFCA** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.
	21:20	**POCA** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.

IDISLFSNP - IDI Self Snoop Register

	19:18	**ITMSNP** Access: R/W 00b: Whatever the logic decides (so force feature is disabled) - Default. 01b: Always drive 0. 10b: Always drive 1. 11b: Reserved.
	17:16	**WCILFSNP** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.
	15:14	**WILSNP** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.
	13:12	**WCILSNP** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.
	11:10	**WBMSNP** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.
	9:8	**RFOSNP** Access: R/W 00b: Whatever the logic decides (so force feature is disabled) - Default. 01b: Always drive 0. 10b: Always drive 1. 11b: Reserved.
	7:6	**PORINSNP** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.
	5:4	**PRDSNP** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.

IDISLFSNP - IDI Self Snoop Register

	3:2	**DRDSNP** Access: R/W 00b: Whatever the logic decides (so force feature is disabled) - Default. 01b: Always drive 0. 10b: Always drive 1. 11b: Reserved.
	1:0	**CRDSP** Access: R/W 00b: Whatever the logic decides (so force feature is disabled) - Default. 01b: Always drive 0. 10b: Always drive 1. 11b: Reserved.

Idle Switch Delay

IDLEDLY - Idle Switch Delay

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0223Ch-0223Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_RCSUNIT
Address:	1223Ch-1223Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_VCSUNIT0
Address:	1A23Ch-1A23Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_VECSUNIT
Address:	1C23Ch-1C23Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_VCSUNIT1
Address:	2223Ch-2223Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_BCSUNIT

The IDLEDLY register contains an Idle Delay field which specifies eight times the time stamp base units allowed for command streamer to wait before a context is switched out leading to IDLE state in Execlist mode, i.e following this context switch there is no active element available in HW to execute. Refer “Time Stamp Bases” subsection in Power Management chapter for time stamp base unit granularity. Example: An IDLE Delay count of “2” with Time stamp base unit value of 80ns would mean an idle delay wait of 1280ns (2*8*80). A default value of 0, means that by default, there is no restriction to wait on a context switch leading to IDLE. This register has no significance when Execlists are not enabled.

DWord	Bit	Description
0	31:21	**Reserved** Format: MBZ
	20:0	**IDLE Delay** Format: U21 Eight times the time stamp base units allowed. Refer “Time Stamp Bases” subsection in Power Management chapter for time stamp base unit granularity. Example: An IDLE Delay count of “2” with Time stamp base unit value of 80ns would mean an idle delay wait of 1280ns (2*8*80).

Indirect Context Offset Pointer

INDIRECT_CTX_OFFSET - Indirect Context Offset Pointer

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000980
Access:	R/W
Size (in bits):	32
Trusted Type:	1

Address:	021C8h-021CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_RCSUNIT

Address:	121C8h-121CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_VCSUNIT0

Address:	1A1C8h-1A1CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_VECSUNIT

Address:	1C1C8h-1C1CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_VCSUNIT1

Address:	221C8h-221CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_BCSUNIT

This register is used to program the offset where commands RCS_INDIRECT_CTX points to will be executed as part of engine context restore.

Programming Notes	Source
BlitterCS/VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be programmed for these command streamers.	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS
Offset of Indirect CS context must be always programmed to a command boundary and cacheline boundary inside the context image.	
Indirect context pointer itself is restored during context restore and hence Indirect Context Offset must not be programmed with value less than 0x5.	

DWord	Bit	Description	
0	31:16	**Reserved**	
		Format:	MBZ

INDIRECT_CTX_OFFSET - Indirect Context Offset Pointer

	15:6	**Offset of Indirect CS Context** Format: U10 This is the cache line offset for the Indirect CS context. This defaults to execute between CS and SVG context. It is not valid to program this to a value that is greater or equal to the starting offset for RS context. If context must be programmed at the end of engine context then program then use BB_PER_CTX_PTR. **Value**: 26h — **Name**: **[Default]**
	5:0	**Reserved** Format: MBZ

Indirect Context Pointer

INDIRECT_CTX - Indirect Context Pointer

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1

Address:	021C4h-021C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_RCSUNIT

Address:	121C4h-121C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_VCSUNIT0

Address:	1A1C4h-1A1C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_VECSUNIT

Address:	1C1C4h-1C1C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_VCSUNIT1

Address:	221C4h-221C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_BCSUNIT

This register is used to program the indirect address to be executed between CS and SVG engine context if enabled. This will only get executed due to regular context save/restore and not during power restore. This register is part of the execution list context and will be executed per context. Only supported if execution list is enabled. There is no preempting workloads within this context.

Programming Notes	Source
BlitterCS/VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be programmed for these command streamers.	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS
The following commands are not supported within Render CS indirect context:	RenderCS

Command Name
MI_WAIT_FOR_EVENT
MI_SEMAPHORE_SIGNAL
MI_ARB_CHECK
MI_RS_CONTROL
MI_REPORT_HEAD

INDIRECT_CTX - Indirect Context Pointer

MI_URB_ATOMIC_ALLOC	
MI_SUSPEND_FLUSH	
MI_TOPOLOGY_FILTER	
MI_RS_CONTEXT	
MI_SET_CONTEXT	
MI_URB_CLEAR	
MI_SEMAPHORE_WAIT in Memory Poll Mode is not supported.	
MI_BATCH_BUFFER_START	
MI_CONDITIONAL_BATCH_BUFFER_END	
MEDIA_OBJECT_WALKER	
GPGPU_WALKER	
3DPRIMITIVE	
3DSTATE_BINDING_TABLE_POINTERS_VS	
3DSTATE_BINDING_TABLE_POINTERS_HS	
3DSTATE_BINDING_TABLE_POINTERS_DS	
3DSTATE_BINDING_TABLE_POINTERS_GS	
3DSTATE_BINDING_TABLE_POINTERS_PS	
3DSTATE_GATHER_CONSTANT_VS	
3DSTATE_GATHER_CONSTANT_GS	
3DSTATE_GATHER_CONSTANT_HS	
3DSTATE_GATHER_CONSTANT_DS	
3DSTATE_GATHER_CONSTANT_PS	
3DSTATE_DX9_CONSTANTF_VS	
3DSTATE_DX9_CONSTANTF_HS	
3DSTATE_DX9_CONSTANTF_DS	
3DSTATE_DX9_CONSTANTF_GS	
3DSTATE_DX9_CONSTANTF_PS	
3DSTATE_DX9_CONSTANTI_VS	
3DSTATE_DX9_CONSTANTI_HS	
3DSTATE_DX9_CONSTANTI_DS	
3DSTATE_DX9_CONSTANTI_GS	
3DSTATE_DX9_CONSTANTI_PS	
3DSTATE_DX9_CONSTANTB_VS	
3DSTATE_DX9_CONSTANTB_HS	
3DSTATE_DX9_CONSTANTB_DS	
3DSTATE_DX9_CONSTANTB_GS	

INDIRECT_CTX - Indirect Context Pointer

3DSTATE_DX9_CONSTANTB_PS
3DSTATE_DX9_LOCAL_VALID_VS
3DSTATE_DX9_LOCAL_VALID_DS
3DSTATE_DX9_LOCAL_VALID_HS
3DSTATE_DX9_LOCAL_VALID_GS
3DSTATE_DX9_LOCAL_VALID_PS
3DSTATE_DX9_GENERATE_ACTIVE_VS
3DSTATE_DX9_GENERATE_ACTIVE_HS
3DSTATE_DX9_GENERATE_ACTIVE_DS
3DSTATE_DX9_GENERATE_ACTIVE_GS
3DSTATE_DX9_GENERATE_ACTIVE_PS
3DSTATE_BINDING_TABLE_EDIT_VS
3DSTATE_BINDING_TABLE_EDIT_GS
3DSTATE_BINDING_TABLE_EDIT_HS
3DSTATE_BINDING_TABLE_EDIT_DS
3DSTATE_BINDING_TABLE_EDIT_PS
3DSTATE_CONSTANT_VS
3DSTATE_CONSTANT_GS
3DSTATE_CONSTANT_PS
3DSTATE_CONSTANT_HS
3DSTATE_CONSTANT_DS
MI_BATCH_BUFFER_END

Workaround

Workaround https://vthsd.iind.intel.com/hsd/gen9lp/default.aspx#bug_de/default.aspx?bug_de_id=2135817 :
RenderCS Only:
Softwar must always program RCS_INDIRECT_CTX buffer with MI_LOAD_REGISTER_IMM command to reset “Disable Gather at Set Shader Common Slice”. "Offset of Indirect CS Context";in INDIRECT_CTX_OFFSET register must be set to default value.

DWord	Bit	Description
0	31:6	**Indirect CS Context Address** Format: GraphicsAddress[31:6] Pointer to the Context in memory to be executed as a batch.

INDIRECT_CTX - Indirect Context Pointer

	5:0	**Size of Indirect CS Context** Format: U6 This is the size of the Indirect Context for CS. This size supports up to 63 cache lines worth of commands where a cache line is 64B. If programmed to zero then the indirect fetch of the CS context is disabled. **Value** / **Name** [0,63]

INF unit Level Clock Gating Control 9560

INFCGCTL9560 - INF unit Level Clock Gating Control 9560

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x000000FF
Size (in bits):	32
Address:	09560h

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31:8	**Reserved** Access: R/W Reserved
	7	**CPMAunit Clock Gating Disable** Default Value: 1b Access: R/W CPMAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	6	**GTFSunit Clock Gating Disable** Default Value: 1b Access: R/W GTFSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	5	**RPMunit Clock Gating Disable** Default Value: 1b Access: R/W RPMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

INFCGCTL9560 - INF unit Level Clock Gating Control 9560

	4	**MBGFUCunit Clock Gating Disable** Default Value: 1b Access: R/W MBGFUCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	3	**CGPSFunit Clock Gating Disable** Default Value: 1b Access: R/W CGPSFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	2	**MDRBunit Clock Gating Disable** Default Value: 1b Access: R/W MDRBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	1	**MGSRunit Clock Gating Disable** Default Value: 1b Access: R/W MGSRunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	0	**MRCunit Clock Gating Disable** Default Value: 1b Access: R/W MRCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Instruction Parser Mode Register

INSTPM - Instruction Parser Mode Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	r/w
Size (in bits):	32
Trusted Type:	1
Address:	020C0h-020C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_RCSUNIT
Address:	120C0h-120C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VCSUNIT0
Address:	1A0C0h-1A0C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VECSUNIT
Address:	1C0C0h-1C0C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VCSUNIT1
Address:	220C0h-220C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_BCSUNIT

The INSTPM register is used to control the operation of the Instruction Parser. Certain classes of instructions can be disabled (ignored) - often useful for detecting performance bottlenecks. Also, Synchronizing Flush operations can be initiated - useful for ensuring the completion (vs. only parsing) of rendering instructions.

Programming Notes

- If an instruction type is disabled, the parser will read those instructions but not process them.
- Error checking will be performed even if the instruction is ignored.
- All Reserved bits are implemented.
- This Register is saved and restored as part of Context.

DWord	Bit	Description

INSTPM - Instruction Parser Mode Register

0	31:16	**Mask** Access: WO Format: Mask Masks: These bits serve as write enables for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.
	15:14	**Reserved** Format: MBZ
	13:12	**Reserved** Format: MBZ
	11	**CLFLUSH Toggle** Source: RenderCS Access: RO Format: U1 This bit changes polarity each time the MI_CLFLUSH command completes. This bit is Read Only.
	11	**Reserved** Source: BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS Format: MBZ
	10	**Reserved**
	9:0	**Reserved** Format: MBZ

Internal GAM State

INTSTATE - Internal GAM State		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	040C0h	
DWord	**Bit**	**Description**
0	31:0	**Reserved**

Interrupt Line

INTRLINE_0_2_0_PCI - Interrupt Line	
Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	8
Address:	0003Ch

This register is used to communicate interrupt line routing information. The device itself does not use this value, rather it is used by device drivers and operating systems to determine priority and vector information.

DWord	Bit	Description
0	7:0	**Interrupt Connection** Default Value: 00000000b Access: R/W Used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates to which input of the system interrupt controller the device's interrupt pin is connected.

Interrupt Mask Register

IMR - Interrupt Mask Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0xFFFFFFFF
Access:	R/W
Size (in bits):	32
Address:	020A8h-020ABh
Name:	Interrupt Mask Register
ShortName:	IMR_RCSUNIT
Address:	120A8h-120ABh
Name:	Interrupt Mask Register
ShortName:	IMR_VCSUNIT0
Address:	1A0A8h-1A0ABh
Name:	Interrupt Mask Register
ShortName:	IMR_VECSUNIT
Address:	1C0A8h-1C0ABh
Name:	Interrupt Mask Register
ShortName:	IMR_VCSUNIT1
Address:	220A8h-220ABh
Name:	Interrupt Mask Register
ShortName:	IMR_BCSUNIT

The IMR register is used by software to control which Interrupt Status Register bits are masked or unmasked. Unmasked bits will be reported in the IIR, possibly triggering a CPU interrupt, and will persist in the IIR until cleared by software. Masked bits will not be reported in the IIR and therefore cannot generate CPU interrupts.

DWord	Bit	Description
0	31:0	**Interrupt Mask Bits** Format: InterruptMask[32] Refer to the Interrupt Control Register section for bit definitions. This field contains a bit mask which selects which interrupt bits (from the ISR) are reported in the IIR. Reserved bits in the Interrupt Control Register are RO.

Value	Name	Description
FFFF FFFFh	**[Default]**	
0h	Not Masked	Will be reported in the IIR
1h	Masked	Will not be reported in the IIR

Interrupt Pin

INTRPIN_0_2_0_PCI - Interrupt Pin

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000001
Size (in bits):	8
Address:	0003Dh

This register tells which interrupt pin the device uses.

DWord	Bit	Description
0	7:0	**Interrupt Pin** Default Value: 00000001b Access: RO As a single function device, the IGD specifies INTA# as its interrupt pin. Hardwired to 01h = INTA#.

I/O Base Address

IOBAR_0_2_0_PCI - I/O Base Address

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000001
Size (in bits):	32
Address:	00020h

This register provides the Base offset of the I/O registers within Device #2. Bits 15:6 are programmable allowing the I/O Base to be located anywhere in 16bit I/O Address Space. Bits 2:1 are fixed and return zero; bit 0 is hardwired to a one indicating that 8 bytes of I/O space are decoded. Access to the 8Bs of IO space is allowed in PM state D0 when IO Enable (PCICMD bit 0) set. Access is disallowed in PM states D1-D3 or if IO Enable is clear or if Device #2 is turned off or if Internal graphics is disabled through the fuse or fuse override mechanisms. Note that access to this IO BAR is independent of VGA functionality within Device #2. If accesses to this IO bar is allowed then all 8, 16 or 32 bit IO cycles from IA cores that falls within the 8B are claimed.

DWord	Bit	Description
0	15:6	**IO Base Address** Default Value: 0000000000b Access: R/W Set by the OS, these bits correspond to address signals [15:6].
	5:3	**Reserved** Format: MBZ
	2:1	**Memory Type** Default Value: 00b Access: RO Hardwired to 0s to indicate 32-bit address.
	0	**Memory/IO Space** Default Value: 1b Access: RO Hardwired to "1" to indicate IO space.

IPC PER SUBSLICE

EUMETRICS_EVENT1 - IPC PER SUBSLICE	
Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	00D90h

This register mirrors an accumulating count for EU Metric Event1.
It is enabled by configuration bits in GPMunit and SPMunits.
Note that count is never cleared and delta should be calculated by sampling the initial register value at the start and subtracting that value off from the final sample value.

DWord	Bit	Description
0	31:0	**EU Metric Event Count** Access: RO

KCR GAM slave counter High part

KCR_CTR_SLAVE_H - KCR GAM slave counter High part		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0482Ch	
DWord	**Bit**	**Description**
0	31:0	**KCR Slave Counter High** Default Value: 00000000h Access: R/W Slave High counter[63:32] for KCR

KCR GAM slave counter Low part

KCR_CTR_SLAVE_L - KCR GAM slave counter Low part		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04828h	
DWord	**Bit**	**Description**
0	31:0	**KCR Slave Counter Low** Default Value: 00000000h Access: R/W Slave Low counter[31:0] for KCR

L3 Bank Status

L3STAT - L3 Bank Status

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	0B128h

L3 Status register

DWord	Bit	Description
0	31	**L3 Fill Access Status bit** Access: RO This register is Hardware Set and Clear. Set condition: set when the first command is seen on LTCC-LTCD interface. Reset condition: reset when the first Pipeline Flush command is seen on the LTCC-LTCD interface. Reset condition: This Flag will be reset only if we have atleast 1 modified line in the cache written by DC client.
	30	**Texture access Status bit** Access: RO This register is Hardware Set and Clear Set condition : set when the first command is seen on LTCC-LTCD interface. Reset condition : reset when the first Pipeline Flush command is seen on the LTCC-LTCD interface.
	29	**Constant access Status bit** Access: RO This register is Hardware Set and Clear Set condition : set when the first command is seen on LTCC-LTCD interface. Reset condition : reset when the first Pipeline Flush command is seen on the LTCC-LTCD interface.
	28	**State access Status bit** Access: RO This register is Hardware Set and Clear Set condition : set when the first command is seen on LTCC-LTCD interface. Reset condition : reset when the first Pipeline Flush command is seen on the LTCC-LTCD interface.
	27	**EU data traffic access Status bit** Access: RO This register is Hardware Set and Clear Set condition : set when the first command is seen on LTCC-LTCD interface. Reset condition : reset when the first Pipeline Flush command is seen on the LTCC-LTCD interface.

L3STAT - L3 Bank Status

	26	**IA coherent access Status bit** Access: RO This register is Hardware Set and Clear Set condition : set when the first command is seen on LTCC-LTCD interface. Reset condition : reset when the first Pipeline Flush command is seen on the LTCC-LTCD interface.
	25:0	**Reserved** Access: RO

L3 Control Register

L3CNTLREG - L3 Control Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000 [SKL:GT2:A, SKL:GT2:B, SKL:GT2:C, SKL:GT2:D, SKL:GT2:F, SKL:GT2:G, SKL:GT3:A, SKL:GT3:C, SKL:GT3:F, SKL:GT3:G, SKL:GT4:E, SKL:GT4:F, SKL:GT4:G]
Access:	R/W
Size (in bits):	32
Address:	07034h

Programming Notes

The L3 allocation programming should assign all ways of the cache with no left over ways. Refer to L3 section for the recommended settings.

Any L3 configuration change that reduces the data cache allocation when strong IA coherency is used requires the full flush of L3 prior to the programming update.
An explicit or implicit flush of L3 (DC Flush) through the command streamer doesn't result in flushing/invalidating the IA Coherent lines from L3. However this can be achieved by setting the "**Pipe line flush Coherent lines**" control bit in the "L3SQCREG4" register.

DWord	Bit	Description
0	31:25	**All L3 Client Pool** Access: R/W Number of ways allocated for the all client pool. This is a combined pool for all clients.

Value	Name	Description	Project
[0h,40h]		Increments of 8KB	DevSKL:GT2
[0h,40h]		Increments of 16KB	DevSKL:GT3
30h	**[Default]**		

Programming Notes

When this field is non-zero, **DC Way Assignment** and **Read Only Client Pool** should be 0KB. Odd number values are not allowed. **Please refer to L3 Section with Allocation and Programming for recommended settings.**

L3CNTLREG - L3 Control Register

24:18 **DC Way Assignment**

Access:	R/W

Number of ways allocated for DC. Note this allocation is only for DC data types.

Value	Name	Description	Project
[0h,40h]	0KB-512KB	Increments of 8KB	DevSKL:GT2
[0h,40h]	0KB-1024KB	Increments of 16KB	DevSKL:GT3

Programming Notes
Note: This field must be 0KB if All L3 Client Pool is non-zero. Odd number values are not allowed. **Please refer to L3 HAS for valid programming values**

17:11 **Read Only Client Pool**

Access:	R/W

Number of ways allocated for Read Only L3 clients. This is a combined pool for all Read Only clients.

Value	Name	Description	Project
[0h,40h]	0KB-512KB	Increments of 8KB	SKL:GT2
[0h,40h]	0KB-1024KB	Increments of 16KB	SKL:GT3

Programming Notes
Note: This field must be 0KB if All L3 Client Pool is non-zero. Odd number values are not allowed. **Please refer to L3 HAS for valid programming values**

10 **Reserved**

Access:	R/W
Format:	PBC

9 **Error Detection Behavior Control**

Access:	R/W
Format:	Enable

The L3 error detection can be enabled to hang the GPU on a non-recoverable error due to SER type events. Such option will be used when corresponding context has data consistency requirements. Once error detection is enabled, s/w has to initialize URB or SLM to all 0's (based on usage model) prior to execution of the workload. Initialization is required to clean up the error detection logic and syndrome tracking.

Value	Name	Description
0h	**[Default]**	RTL does not hang on parity errors or double bit error
1h		RTL enforces a hang on parity errors or double bit error

L3CNTLREG - L3 Control Register

	8	**GPGPU L3 Credit Mode Enable** Access: R/W Format: Enable This bit is required to be enabled under GPGPU workloads to provide the MAX latency coverage from L3 cache. It will override the registers 0xB100[18:14] and 0xB100[23:19], to 0 and the maximum value respectively.
	7:1	**URB Allocation** Access: R/W Number of ways allocated for URB usage

Value	Name	Description	Project
[0h,40h]		Increments of 8KB	SKL:GT2
[0h,40h]		Increments of 16KB	SKL:GT3
30h	**[Default]**		

Programming Notes
Odd number values are not allowed. **Please refer to L3 HAS for valid programming values**

	0	**SLM Mode Enable** Access: R/W Format: Enable When enabled, a 64KB (per bank) region of L3 is reserved for SLM.

L3 Control Register1

L3CNTLREG1 - L3 Control Register1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x8C47FFF0
Size (in bits):	32
Address:	0B10Ch

DWord	Bit	Description
0	31:28	**Data Fifo Depth Control** Access: R/W Data Fifo Depth Control (TS mode). Value cannot be zero for normal operation. lbcf_csr_lc_datafifo_depth[3:0]. Value: 1000b — Name: **[Default]**
	27:24	**Data Clock off time** Default Value: 1100b Access: R/W Data Clock off time (DATACLKOFF): Data Clock off time - Data block is shut off after these many number of clocks programmed in this register bits. lbcf_csr_lc_dataclkoff_time[3:0]. Min value to be 4'h0100. It should be between 4'h4 : 4'hf.
	23:20	**TAG CLK OFF TIME** Default Value: 0100b Access: R/W Description: TAG CLK OFF TIME (TAGCLKOFF): TAG Clock Off time. This is the time, which Clock gating Logic checks before it turns off the clock. lbcf_csr_lc_tagclkoff_time[3:0]. Value can be between 4'h4 - 4'hf.

L3CNTLREG1 - L3 Control Register1

	19	**L3 Aging Disable Bit** Default Value: 0b Access: R/W L3 Aging Disable Bit (L3AGDIS): Aging Disable. lbcf_csr_lc_agingdis.
	18:15	**Fill aging** Default Value: 1111b Access: R/W Fill aging (L3AGF): Aging Counter for Fill. lbcf_csr_lc_fill_aging_cnt[3:0]. If bit B103.19 is 0 then this register value has to be nonzero.
	14:11	**Aging Counter for Read 1 Port** Default Value: 1111b Access: R/W Aging Counter for Read 1 Port (L3AGR1): Aging Counter for Read 1 Port. lbcf_csr_lc_r1_aging_cnt[3:0]. If bit B103.19 is 0 then this register value has to be nonzero.
	10:7	**L3 Aging Counter for R0** Default Value: 1111b Access: R/W L3 Aging Counter for R0 (L3AGR0): Aging Counter for R0 Port. lbcf_csr_lc_r0_aging_cnt[3:0]. If bit B103.19 is 0 then this register value has to be nonzero.
	6:4	**L3 Aging Counter for SNOOP** Default Value: 111b Access: R/W L3 Aging Counter for SNOOP: Aging Counter for Snoop Port. lbcf_csr_lc_snp_aging_cnt[3:0].
	3:0	**Reserved** Default Value: 0000b Access: RO Reserved.

L3 LRA 0

L3_LRA_0 - L3 LRA 0	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0E037C00
Size (in bits):	32
Exists If:	Device[Platform] == 'Client'
Address:	04A10h

DWord	Bit	Description
0	31:30	**L3** Default Value: 00b Access: R/W Which LRA should L3 use.
	29:20	**L3 LRA1 Min** Default Value: 0011100000b Access: R/W Minimum value of programmable LRA1.
	19:10	**L3 LRA0 Max** Default Value: 0011011111b Access: R/W Maximum value of programmable LRA0.
	9:0	**L3 LRA0 Min** Default Value: 0000000000b Access: R/W Minimum value of programmable LRA0.

L3 LRA 0 GPGPU

L3_LRA_0_GPGPU - L3 LRA 0 GPGPU

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x05013C00
Size (in bits):	32
Address:	04DD0h

DWord	Bit	Description
0	31:30	**L3 GPGPU** Default Value: 00b Access: R/W Which LRA should L3 use.
	29:20	**L3 LRA1 Min GPGPU** Default Value: 0001010000b Access: R/W Minimum value of programmable LRA1.
	19:10	**L3 LRA0 Max GPGPU** Default Value: 0001001111b Access: R/W Maximum value of programmable LRA0.
	9:0	**L3 LRA0 Min GPGPU** Default Value: 0000000000b Access: R/W Minimum value of programmable LRA0.

L3 LRA 1

L3_LRA_1 - L3 LRA 1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x67F701BF
Size (in bits):	32
Exists If:	Device[Platform] == 'Client'
Address:	04A14h

DWord	Bit	Description
0	31:30	**DC** Default Value: 01b Access: R/W Which LRA should DC use.
	29:20	**L3 LRA2 Max** Default Value: 1001111111b Access: R/W Maximum value of programmable LRA2.
	19:10	**L3 LRA2 Min** Default Value: 0111000000b Access: R/W Minimum value of programmable LRA2.
	9:0	**L3 LRA1 Max** Default Value: 0110111111b Access: R/W Maximum value of programmable LRA1.

L3 LRA 1 GPGPU

L3_LRA_1_GPGPU - L3 LRA 1 GPGPU

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x67F8721B
Size (in bits):	32
Address:	04DD4h

DWord	Bit	Description
0	31:30	**DC GPGPU** Default Value: 01b Access: R/W Which LRA should DC use.
	29:20	**L3 LRA2 Max GPGPU** Default Value: 1001111111b Access: R/W Maximum value of programmable LRA2.
	19:10	**L3 LRA2 Min GPGPU** Default Value: 1000011100b Access: R/W Minimum value of programmable LRA2.
	9:0	**L3 LRA1 Max GPGPU** Default Value: 1000011011b Access: R/W Maximum value of programmable LRA1.

L3 LRA 2

L3_LRA_2 - L3 LRA 2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000002
Size (in bits):	32
Exists If:	Device[Platform] == 'Client'
Address:	04A18h

DWord	Bit	Description
0	31:2	**Reserved** Default Value: 00000000000000000000000000000000b Access: RO
	1:0	**Texture** Default Value: 10b Access: R/W Which LRA should Texture use.

L3 LRA 2 GPGPU

L3_LRA_2_GPGPU - L3 LRA 2 GPGPU

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000002
Size (in bits):	32
Address:	04DD8h

DWord	Bit	Description
0	31:2	**Reserved** Default Value: 00000000000000000000000000000000b Access: RO
	1:0	**Texture GPGPU** Default Value: 10b Access: R/W Which LRA should Texture use.

L3 LRA 0 3D

L3_LRA_0_3D - L3 LRA 0 3D

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x05013C00
Size (in bits):	32
Address:	04A10h

DWord	Bit	Description
0	31:30	**L3 3D** Default Value: 00b Access: R/W Which LRA should L3 use.
	29:20	**L3 LRA1 Min 3D** Default Value: 0001010000b Access: R/W Minimum value of programmable LRA1.
	19:10	**L3 LRA0 Max 3D** Default Value: 0001001111b Access: R/W Maximum value of programmable LRA0.
	9:0	**L3 LRA0 Min 3D** Default Value: 0000000000b Access: R/W Minimum value of programmable LRA0.

L3 LRA 1 3D

L3_LRA_1_3D - L3 LRA 1 3D

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x66F2D0B3 [SKL:GT1, SKL:GT1.5, SKL:GT2:C, SKL:GT2:D, SKL:GT2:F, SKL:GT2:G, SKL:GT3, SKL:GT4]
Size (in bits):	32
Address:	04A14h

DWord	Bit	Description
0	31:30	**DC 3D** Default Value: 01b Access: R/W Which LRA should DC use.
	29:20	**L3 LRA2 Max 3D** Default Value: 1001101111b Access: R/W Maximum value of programmable LRA2.
	19:10	**L3 LRA2 Min 3D** Default Value: 0010110100b Access: R/W Minimum value of programmable LRA2.
	9:0	**L3 LRA1 Max 3D** Default Value: 0010110011b Access: R/W Maximum value of programmable LRA1.

L3 LRA 2 3D

L3_LRA_2_3D - L3 LRA 2 3D

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x009FE70E
Size (in bits):	32
Address:	04A18h

DWord	Bit	Description
0	31:24	**Reserved** Default Value: 00000000b Access: RO
	23:14	**L3 LRA3 Max 3D** Default Value: 1001111111b Access: R/W Maximum value of programmable LRA2. If L3LRA3Min_3D == L3LRA3Max_3D , GATR LRA is disabled, GATR cycles are mapped to L3LRA0 If L3LRA3Min_3D == L3LRA3Max_3D , GATR LRA is disabled, L3LRA2Max_3D will default to L3LRA3Max_3D to reuse GATR entries
	13:4	**L3 LRA3 Min 3D** Default Value: 1001110000b Access: R/W Minimum value of programmable LRA3.
	3:2	**GATR_3D** Default Value: 11b Access: R/W Which LRA should GATR use.
	1:0	**Texture 3D** Default Value: 10b Access: R/W Which LRA should Texture use.

L3 SLM Register

L3SLMREG - L3 SLM Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x40000000
Size (in bits):	32
Address:	0B110h

DWord	Bit	Description
0	31	**Disable Periodic SLM/SQ slot allocation** Default Value: 0b Access: R/W Disable Periodic SLM/SQ slot allocation: When cfg_lslm_livelock_fairarb_dis=1 lslm unit always has the higher priority and lslm_lsqc_block to lsqcunit is asserted as long as there are requests in SLM FIFO. lbcf_csr_lslm_livelock_fairarb_dis.
	30:26	**LSLM_SQ_PENDING_MAX** Default Value: 10000b Access: R/W If lslmunit has read data to be sent to lcbrunit this cfg register specifies the maximum number of clocks for which LSLMunit can block SQ request from being sent o lcbrunit. Default value = 8. Value cannot be zero. lbcf_csr_lslm_sqpend_max[4:0].
	25	**LSLM address disable** Default Value: 0b Access: R/W 0 - Enable b2b addr matching fix. lslmunit should not block the cycle in fifo if there is a match in the pipeline. 1 - Disable b2b addr matching fix. lslmunit should block the cycle in fifo if there is a match in the pipeline. lbcf_csr_lslm_same_addr_dis. Default = 0.
	24:0	**Reserved** Access: RO

L3 SQC register 4

L3SQCREG4 - L3 SQC register 4		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x40400000	
Size (in bits):	32	
Address:	0B118h	

DWord	Bit	Description
0	31	**Reserved**
	30	**L3SQ URB Read CAM Match Disable** Default Value: 1b Access: R/W L3SQ URB Read CAM Match Disable (SQURBRDCAMDIS): Disables the L3SQ Cam Match ability for URB Reads. By disabling, this allows a performance mode where URB reads are not dependent upon one another but only on any previous URB writes to the same address. This allows many URB reads to the same cacheline at any given time instead of serializing the requests. 1 = URB Read CAM matching is disabled; multiple URB reads to the same cacheline are allowed to be concurrent (default). 0 = URB Read CAM matching is enabled; multiple URB reads to the same cacheline are serialized. lbcf_csr_lsqc_urbrdcam_dis.
	29:28	**Traffic regulation in LSQC for URB lookup traffic** Default Value: 00b Access: R/W Traffic regulation in LSQC for URB lookup traffic (URB lookups are issued to ltcc these many clocks apart). 00b - Continuous. 01b - 4 clocks apart. 10b - 8 clocks apart. 11b - 16 clocks apart. lbcf_lsqc_urb_traffic.
	27	**LQSC RO PERF DIS** Default Value: 0b Access: R/W Default: 0. when set, RO performance mode is disabled and all Reads proceed only after Parent recycles. lbcf_csr_lsqc_roperf_dis.

L3SQCREG4 - L3 SQC register 4

26 Order Cam Snp Reject

Default Value:	0b
Access:	R/W

Default: 0.
when set, all slots resulting in matches to snp addr result in snprsp as REJECT instead of MISS.
lbcf_csr_lsqc_ordercam_snpreject.

25 LQSC RW PERF DIS

Default Value:	0b
Access:	R/W

Default: 0.
0: Performance mode is enabled.
when set, Rd to RW performance mode is disabled and all cycles proceed only after Parent recycles.

lbcf_csr_lsqc_rwperf_dis.

24 LSQC read rtrn local crdt pre-consume disable

Default Value:	0b
Access:	R/W

0 - Default, LSQD consumes the LNE local slicecredit when read return pending.
1 - LSQD consumes read rtrn credit in the clock it is ready to send read return data.
lbcf_csr_lsqd_rdtrn_precrdt_dis.

23 LSQC Mem Write sqcam HITM response disable

Default Value:	0b
Access:	R/W

0 - Default.
1 - This disables any Memory Write from cache with HitM tag response to respond for SQCAMs.
lbcf_csr_lsqc_sqcam_l3tagrsphitm_dis.

22 Non-IA coherent atomics enable

Default Value:	1b
Access:	R/W

0: Atomics in GTI.
1: Atomics in L3 (non-IA atomic) (default).
lbcf_csr_lsqc_glblatmcs_l3.
Value of this bit should be same as LNCF register bit 0xb008[0].
Value of this bit should be same as LBCF register bit 0xb11c[8].

L3SQCREG4 - L3 SQC register 4

	21	**Pipe line flush Coherent lines** Default Value: 0b Access: R/W 1: Treat pipeline flush as invalidating even coherent lines along with non coherent lines . 0: Flush invalidates non coherent lines only. lbcf_csr_lsqc_pipeflush_coh.
	20:6	**Reserved** Access: RO
	5	**Reserved2** Access: RO
	4	**Reserved** Access: RO
	3	**lslm flush denorm** Default Value: 0b Access: R/W lbcf_csr_lslm_flush_denorm_to_zero When this bit is enabled (1b), Floating Point SLM atomics output will be flushed to zero if it is a De-Norm.
	2	**lsqc disable sla coh** Default Value: 0b Access: R/W lbcf_lsqc_disable_sla_coh If this bit is set to 1b, it will disable Short loop atomics access for Coherent atomics.
	1	**lsqc disable sla** Default Value: 0b Access: R/W lbcf_lsqc_disable_sla If this bit is set to 1b, it will disable Short loop atomics access for Coherent and non-coherent atomics.
	0	**lsqd flush denorm** Default Value: 0b Access: R/W lbcf_csr_lsqd_flush_denorm_to_zero When this bit is enabled (1b), Floating Point atomics output will be flushed to zero if it is a De-Norm.

L3 SQC registers 1

L3SQCREG1 - L3 SQC registers 1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00810000	
Size (in bits):	32	
Address:	0B100h	
DWord	**Bit**	**Description**
0	31:24	**Reserved** Access: RO Reserved.
	23:19	**L3SQ General Priority Credit Initialization** Default Value: 10000b Access: R/W L3SQ General Priority Credit Initialization (SQGPCI): Number of general and high priority credits that SQ presents to L3 Arbiter blocks This inherently also determines the depth of the SQ; reduce the number of credits and SQ uses fewer slots. This field can be programmed only after a stalling flush (HSD:2133794/2133796/2134058) Any value not listed here is considered Reserved. Gen priority credits is always greater than high priority credits. Value # General Credits 00000b 0 00001b 2 00010b 4 00011b 6 00100b 8 00101b 10 00110b 12 00111b 14 01000b 16 01001b 18

L3SQCREG1 - L3 SQC registers 1

		01010b 20 01011b 22 01100b 24 01101b 26 01110b 28 01111b 30 10000b 32 (default) ... 10100b 40 Need to go up to 40 credits. lbcf_csr_lsqc_gen_credit_init[4:0].
	18:14	**L3SQ High Priority Credit Initialization** Default Value: 00100b Access: R/W L3SQ High Priority Credit Initialization (SQHPCI): Number of general and high priority credits that SQ presents to L3 Arbiter blocks. This inherently also determines the depth of the SQ; reduce the number of credits and SQ uses fewer slots. This field can be programmed only after a stalling flush (HSD:2133794/2133796/2134058) Any value not listed here is considered Reserved. gen priority credits is always greater than high priority credits. Value # High Pri Credits 00000b 0 00001b 2 00010b 4 00011b 6 00100b 8 (default) 00101b 10 00110b 12 00111b

L3SQCREG1 - L3 SQC registers 1

		14 01000b 16 01001b 18 01010b 20 01011b 22 01100b 24 01101b 26 01110b 28 01111b 30 10000b 32 ... 10100b 40 Can to go up to 40 credits for SKLT lbcf_csr_lsqc_hp_credit_init[4:0] + lbcf_csr_lsqc_gen_credit_init[4:0] should always be less than or equal to 40(SKLT). lbcf_csr_lsqc_hp_credit_init[4:0].
	13:10	**Reserved** Access: RO Reserved.
	9	**L3SQ Read Once Enable for Sampler Client** Access: R/W L3SQ Read Once Enable for Sampler Client (SQROE): Enables Read Once indications to L3 Cache from SQ. Once enabled, any reads from Sampler client (MT) are sent as Read Once. 0 = (default) Reads from Sampler clients issue Read to L3 Cache. 1 = Reads from Sampler clients issue Read Once to L3 Cache. lbcf_csr_sampler_readonce_en.
	8:6	**Reserved** Access: RO Reserved.

L3SQCREG1 - L3 SQC registers 1

	5:3	**L3SQ Outstanding L3 Fills** Access: R/W L3SQ Outstanding L3 Fills (SQOUTSL3F): Identifies the number of L3 Fills that can be outstanding before SQ throttles the fill requests to L3 Cache. This is not an exact limit, but instead it is used as a threshold to throttling. Once the fill count is greater than or equal to the threshold, then no fills are issued until the fill responses are received to bring the outstanding count back below the threshold. 000b = (default) No limit. 001b = 1 fill. 010b = 2 fills. 011b = 4 fills. 100b = 8 fills. 101b = 16 fills. 11Xb = Reserved. lbcf_csr_lsqc_outs_fill[2:0].
	2:0	**L3SQ Outstanding L3 Lookups** Access: R/W L3SQ Outstanding L3 Lookups (SQOUTSL3L): Identifies the number of L3 lookups that can be outstanding before SQ throttles the lookup requests to L3 Cache. This is not an exact limit, but instead it is used as a threshold to throttling. once the lookup count is greater than or equal to the threshold, then no lookups are issued until the lookup responses are received to bring the outstanding count back below the threshold. 000b = (default) No limit. 001b = 1 lookup. 010b = 2 lookups. 011b = 4 lookups. 100b = 8 lookups. 101b = 16 lookups. 11Xb = Reserved. lbcf_csr_lsqc_outs_lookup[2:0].

L3 SQC registers 2

L3SQCREG2 - L3 SQC registers 2		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00004567	
Size (in bits):	32	
Address:	0B104h	
DWord	**Bit**	**Description**
0	31:17	**Reserved** Access: RO Reserved.
	16	**L3SQ Priority Selection Disable** Access: R/W L3SQ Priority Selection Disable (SQPRIDIS): Enables the use of priority selection based on client ID decodes. If disabled, all cycles in SQ are treated as same priority. 0 = (default) Priority selection is enabled. 1 = Priority selection is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). lbcf_csr_priority_cnt_disable.
	15	**L3SQ Priority 3 Pool Count Disable** Access: R/W L3SQ Priority 3 Pool Count Disable (SQPRI3CNTDIS): When set, priority3 pool becomes unlimited. And priority3 pool count value should not be used in reset of the remaining counters. 0 = (default) Priority 3 pool count is enabled. 1 = Priority 3 pool count is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). lbcf_csr_priority3_cnt_disable.

L3SQCREG2 - L3 SQC registers 2

	14:12	**L3SQ Priority 3 Pool Counter** Default Value: 100b Access: R/W L3SQ Priority 3 Pool Counter (SQPRI3CNT): The count of cycles is selected from priority3 pool before switching to other priority pools. Count is used as the power of 2. 000b = 1 request. 001b = 2 requests. 010b = 4 requests. 011b = 8 requests. ... 111b = 128 requests. lbcf_csr_priority3_cnt[2:0].
	11	**L3SQ Priority 2 Pool Count Disable** Access: R/W L3SQ Priority 2 Pool Count Disable (SQPRI2CNTDIS): When set, priority2 pool becomes unlimited. And priority2 pool count value should not be used in reset of the remaining counters. 0 = (default) Priority 2 pool count is enabled. 1 = Priority 2 pool count is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). lbcf_csr_priority2_cnt_disable.
	10:8	**L3SQ Priority 2 Pool Counter** Default Value: 101b Access: R/W L3SQ Priority 2 Pool Counter (SQPRI2CNT): The count of cycles is selected from priority2 pool before switching to other priority pools. Count is used as the power of 2. 000b = 1 request. 001b = 2 requests. 010b = 4 requests. 011b = 8 requests. ... 111b = 128 requests. lbcf_csr_priority2_cnt[2:0].

L3SQCREG2 - L3 SQC registers 2

	7	**L3SQ Priority 1 Pool Count Disable** Access: R/W L3SQ Priority 1 Pool Count Disable (SQPRI1CNTDIS): When set, priority1 pool becomes unlimited. And priority1 pool count value should not be used in reset of the remaining counters. 0 = (default) Priority 1 pool count is enabled. 1 = Priority 1 pool count is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). lbcf_csr_priority1_cnt_disable.
	6:4	**L3SQ Priority 1 Pool Counter** Default Value: 110b Access: R/W L3SQ Priority 1 Pool Counter (SQPRI1CNT): The count of cycles is selected from priority1 pool before switching to other priority pools. Count is used as the power of 2. 000b = 1 request. 001b = 2 requests. 010b = 4 requests. 011b = 8 requests. ... 111b = 128 requests. lbcf_csr_priority1_cnt[2:0].
	3	**L3SQ Priority 0 Pool Count Disable** Access: R/W L3SQ Priority 0 Pool Count Disable (SQPRI0CNTDIS): When set, priority0 pool becomes unlimited. And priority0 pool count value should not be used in reset of the remaining counters. 0 = (default) Priority 0 pool count is enabled. 1 = Priority 0 pool count is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). lbcf_csr_priority0_cnt_disable.

L3SQCREG2 - L3 SQC registers 2

	2:0	**L3SQ Priority 0 Pool Counter** Default Value: 111b Access: R/W L3SQ Priority 0 Pool Counter (SQPRI0CNT): The count of cycles is selected from priority0 pool before switching to other priority pools. Count is used as the power of 2. 000b = 1 request. 001b = 2 requests. 010b = 4 requests. 011b = 8 requests. ... 111b = (default) 128 requests. lbcf_csr_priority0_cnt[2:0].

L3 SQC registers 3

L3SQCREG3 - L3 SQC registers 3		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00001ABF	
Size (in bits):	32	
Address:	0B108h	
DWord	**Bit**	**Description**
0	31:30	**Reserved** Access: RO Reserved.
	29:28	**SOLunit Priority Value** Access: R/W SOLunit Priority Value (SQSOLPRIVAL): Identifies the priority value for all cycles that are initiated by SOLunit. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0 (default). 01b = Priority 1. 10b = Priority 2. 11b = Priority 3. lbcf_csr_sol_priority[1:0].
	27:26	**GSunit Priority Value** Access: R/W GSunit Priority Value (SQGSPRIVAL): Identifies the priority value for all cycles that are initiated by GSunit. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0 (default). 01b = Priority 1. 10b = Priority 2. 11b = Priority 3. lbcf_csr_gs_priority[1:0].

L3SQCREG3 - L3 SQC registers 3

	25:24	**TEunit Priority Value** Access: R/W TEunit Priority Value (SQTEPRIVAL): Identifies the priority value for all cycles that are initiated by TEunit. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0 (default). 01b = Priority 1. 10b = Priority 2. 11b = Priority 3. lbcf_csr_te_priority[1:0].
	23:22	**CLunit Priority Value** Access: R/W CLunit Priority Value (SQCLPRIVAL): Identifies the priority value for all cycles that are initiated by CLunit. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0 (default). 01b = Priority 1. 10b = Priority 2. 11b = Priority 3. lbcf_csr_cl_priority[1:0].
	21:20	**TSunit Priority Value** Access: R/W TSunit Priority Value (SQTSPRIVAL): Identifies the priority value for all cycles that are initiated by TSunit. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0 (default). 01b = Priority 1. 10b = Priority 2. 11b = Priority 3. lbcf_csr_ts_priority[1:0].
	19:18	**SFunit Priority Value** Access: R/W SFunit Priority Value (SQSFPRIVAL): Identifies the priority value for all cycles that are initiated by SFunit. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0 (default). 01b = Priority 1. 10b = Priority 2. 11b = Priority 3. lbcf_csr_sf_priority[1:0].

L3SQCREG3 - L3 SQC registers 3

	17:16	**SVSM Priority Value** Access: R/W SVSM Priority Value (SQSVSMPRIVAL): Identifies the priority value for all cycles that are initiated by SVSM. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0 (default). 01b = Priority 1. 10b = Priority 2. 11b = Priority 3. lbcf_csr_svsm_priority[1:0].
	15:14	**SARB Priority Value** Access: R/W SARB Priority Value (SQSARBPRIVAL): Identifies the priority value for all cycles that are initiated by State Arbiter (SARB). Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0 (default). 01b = Priority 1. 10b = Priority 2. 11b = Priority 3. lbcf_csr_sarb_priority[1:0].
	13:12	**SBE Priority Value** Default Value: 01b Access: R/W SBE Priority Value (SQSBEPRIVAL): Identifies the priority value for all cycles that are initiated by SBE. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0. 01b = Priority 1 (default). 10b = Priority 2. 11b = Priority 3. lbcf_csr_sbe_priority[1:0].
	11:10	**IC$ Priority Value** Default Value: 10b Access: R/W IC$ Priority Value (SQICPRIVAL): Identifies the priority value for all cycles that are initiated by Instruction Cache (IC$). Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0. 01b = Priority 1. 10b = Priority 2 (default). 11b = Priority 3. lbcf_csr_ic_priority[1:0].

L3SQCREG3 - L3 SQC registers 3

	9:8	**TDL Priority Value** Default Value: 10b Access: R/W TDL Priority Value (SQTDLPRIVAL): Identifies the priority value for all cycles that are initiated by TDL. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0. 01b = Priority 1. 10b = Priority 2 (default). 11b = Priority 3. lbcf_csr_tdl_priority[1:0].
	7:6	**DCunit Priority Value** Default Value: 10b Access: R/W DCunit Priority Value (SQDCPRIVAL): Identifies the priority value for all cycles that are initiated by DC. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0. 01b = Priority 1. 10b = Priority 2 (default). 11b = Priority 3. lbcf_csr_dc_priority[1:0].
	5:4	**DAPR Priority Value** Default Value: 11b Access: R/W DAPR Priority Value (SQDAPRPRIVAL): Identifies the priority value for all cycles that are initiated by DAPR. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0. 01b = Priority 1. 10b = Priority 2. 11b = Priority 3 (default). lbcf_csr_dapr_priority[1:0].

L3SQCREG3 - L3 SQC registers 3

	3:2	**MTunit Priority Value** Default Value: 11b Access: R/W MTunit Priority Value (SQMTPRIVAL): Identifies the priority value for all cycles that are initiated by Sampler (MT). Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0. 01b = Priority 1. 10b = Priority 2. 11b = Priority 3 (default). lbcf_csr_mt_priority[1:0].
	1:0	**LSQCunit Priority Value** Default Value: 11b Access: R/W LSQCunit Priority Value (SQPRIVAL): Identifies the priority value for all cycles that are initiated by Super Queue (L3 Evictions). Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0. 01b = Priority 1. 10b = Priority 2. 11b = Priority 3 (default). lbcf_csr_lsqc_priority[1:0].

LBCF config save msg

LBCFCSR - LBCF config save msg		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B2FCh	
This register is not context saved and is written by PM unit.		
DWord	**Bit**	**Description**
0	31:10	**Reserved** Access: RO
	9:0	**Context save bit** Access: R/W Hardware Clear Bit[9]: Power Context Save Request. 0: Power context save is not being requested (default). 1: Power context save is being requested. Unit needs to self-clear this bit upon sampling. Bits[8:0]: QWord Credits for Power Context Save Request. Minimum Credits = 1: Unit may send 1 QWord pair (enough for first LRI at least). Maximum Credits = 511: Unit may send 511 QWord pairs. A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and consumes one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

LBS config bits

LBSREG - LBS config bits

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x46000000
Size (in bits):	32
Address:	0B124h

Config Bits for LBS unit

DWord	Bit	Description
0	31:27	**Retry timer for lookup into LSQC** Default Value: 01000b Access: R/W Time between receiving Reject Response from LSQC and doing a snoop lookup request again onto LSQCunit. 00000b: 0 clocks. 00001b: 1 clocks. 00010b: 2 clocks. ... 01000b: 8 clocks (default value). ... 11111b: 32 clocks. lbcf_retry_timer[4:0].
	26	**Recycle parent faster in R/W perf mode** Default Value: 1b Access: R/W Arc into recycle as soon as parent becomes eligible to be recycled. 0: Disabled (recycle possible only when parent is recycled). 1: Enabled (default). lbcf_csr_lsqc_rwperf_quickrec.
	25	**Perf mode for Writes to same address** Default Value: 1b Access: R/W Performance improvement for writes to same address in L3: 0 - Performance mode is not enabled. 1 - Performance mode is enabled (default). lbcf_csr_lsqc_erlyrec.
	24:0	**Reserved** Access: RO

LCPLL1_CTL

LCPLL1_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	46010h-46013h
Name:	LCPLL 1 Control
ShortName:	LCPLL1_CTL
Power:	PG0
Reset:	global

The register is used to enable DPLL0 for driving the display core clock (CDCLK), the core display 2X clock (CD2XCLK), and the DDI ports.
DPLL frequency and port mapping programming is done through the DPLL_CTRL* registers.
This register is not reset by the device 2 FLR.

Restriction
These fields must not be changed while any port or CDCLK is using DPLL0.

DWord	Bit	Description
0	31	**PLL Enable** This field enables or disables DPLL0. Value / Name: 0b Disable; 1b Enable Restriction: Configure DPLL0 frequency prior to enabling.
	30	**PLL Lock** Access: RO This read only bit indicates the status of the DPLL0 lock. Value / Name: 0b Not locked or not enabled; 1b Locked
	29:28	**Reserved**
	27:0	**Reserved** Format: MBZ

LCPLL2_CTL

LCPLL2_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	46014h-46017h
Name:	LCPLL 2 Control
ShortName:	LCPLL2_CTL
Power:	PG0
Reset:	soft

The register is used to enable DPLL1 for driving the DDI ports.
DPLL frequency, SSC, and port mapping programming is done through the DPLL_CTRL* and DPLL*_CFGCR* registers.

Restriction
These fields must not be changed while any port is using DPLL1.

DWord	Bit	Description
0	31	**PLL Enable** This bit enables or disables DPLL1. Value / Name: 0b Disable; 1b Enable Restriction: Configure DPLL1 frequency and SSC prior to enabling.
	30	**Reserved** Format: MBZ
	29:28	**Reserved**
	27:0	**Reserved** Format: MBZ

LINKM

LINKM	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	60040h-60043h
Name:	Transcoder A Link M Value 1
ShortName:	TRANS_LINKM1_A
Valid Projects:	
Power:	PG2
Reset:	soft
Address:	61040h-61043h
Name:	Transcoder B Link M Value 1
ShortName:	TRANS_LINKM1_B
Valid Projects:	
Power:	PG2
Reset:	soft
Address:	62040h-62043h
Name:	Transcoder C Link M Value 1
ShortName:	TRANS_LINKM1_C
Valid Projects:	
Power:	PG2
Reset:	soft
Address:	6F040h-6F043h
Name:	Transcoder EDP Link M Value 1
ShortName:	TRANS_LINKM1_EDP
Valid Projects:	
Power:	PG1
Reset:	soft

Description

There is one instance of this register for each transcoder A/B/C/EDP. This register is double buffered to update on the next MSA after LINKN is written.

DWord	Bit	Description	
0	31:24	**Reserved**	
		Format:	MBZ

LINKM		
	23:0	**Link M value** This field is the link M value for external transmission in the Main Stream Attributes.

LINKN

LINKN	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	60044h-60047h
Name:	Transcoder A Link N Value 1
ShortName:	TRANS_LINKN1_A
Valid Projects:	
Power:	PG2
Reset:	soft
Address:	61044h-61047h
Name:	Transcoder B Link N Value 1
ShortName:	TRANS_LINKN1_B
Valid Projects:	
Power:	PG2
Reset:	soft
Address:	62044h-62047h
Name:	Transcoder C Link N Value 1
ShortName:	TRANS_LINKN1_C
Valid Projects:	
Power:	PG2
Reset:	soft
Address:	6F044h-6F047h
Name:	Transcoder EDP Link N Value 1
ShortName:	TRANS_LINKN1_EDP
Valid Projects:	
Power:	PG1
Reset:	soft

Description
There is one instance of this register for each transcoder A/B/C/EDP. This register is double buffered to update on the next MSA after written. **Writes to this register arm M/N registers for this transcoder.**

DWord	Bit	Description	
0	31:24	**Reserved**	
		Format:	MBZ

LINKN		
	23:0	**Link N value** This field is the link N value for external transmission in the Main Stream Attributes and VB-ID.

LNCF config save msg

LNCFCSR - LNCF config save msg		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B0FCh	
This register is not context saved and is written by pm unit.		
DWord	**Bit**	**Description**
0	31:10	**Reserved** Access: RO
	9:0	**Context save bit** Access: R/W Hardware Clear Bit[9]. Power Context Save Request 0: Power context save is not being requested (default). 1: Power context save is being requested. Unit needs to self-clear this bit upon sampling. Bits[8:0]. QWord Credits for Power Context Save Request. Minimum Credits = 1: Unit may send 1 QWord pair (enough for first LRI at least). Maximum Credits = 511: Unit may send 511 QWord pairs. A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

LNCF Context Save Register

LNCF_CTX - LNCF Context Save Register		
Register Space:	MMIO: 0/2/0	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	0B0F8h	
This register is used to send messages to enable context saving. This register may not be written from CPU.		

DWord	Bit	Description
0	31:16	**Masks** Format: Mask[15:0] A 1 in a bit in this field allows the modification of the corresponding bit in bits 15:0.
	15:1	**Reserved** Format: MBZ
	0	**Context Save Start - Chunk1** Format: Enable When a 1 is written to this bit with the corresponding mask bit set, it will kick off a context save. Once the save is complete the bit will be cleared. LNCFunit on receiving this message sends the Chunk-1 of context image to CS.

LNCF MOCS Register 0

LNCFCMOCS0 - LNCF MOCS Register 0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00100000
Size (in bits):	32
Address:	0B020h

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 010000b Access: R/W [21:20] - L3 Cacheability Control (L3CC): Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls. 00: Use binding table index for direct EU accesses - for rest it is reserved. 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) [19:17] - Skip Caching Control (SCC) Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. If "0", then corresponding address bit value is don't care Bit[1]=1: address bit[9] needs to be '0' to cache in target Bit[2]=1: address bit[10] needs to be '0' to cache in target Bit[3]=1: address bit[11] needs to be '0' to cache in target [16] - Enable Skip Caching (ESC) Enable for the Skip cache mechanism Skip caching needs to be disabled in SKLT 0: Not enabled 1: Enabled for L3 LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO

LNCFCMOCS0 - LNCF MOCS Register 0

	5:0	**MOCS lower data** Default Value: 000000b Access: R/W [5:4] - L3 Cacheability Control (L3CC): Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls. 00: Use binding table index for direct EU accesses - for rest it is reserved. 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) [3:1] - Skip Caching Control (SCC) Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. If "0", then corresponding address bit value is don't care Bit[1]=1: address bit[9] needs to be '0' to cache in target Bit[2]=1: address bit[10] needs to be '0' to cache in target Bit[3]=1: address bit[11] needs to be '0' to cache in target [0] - Enable Skip Caching (ESC) Enable for the Skip cache mechanism Skip caching needs to be disabled in SKLT 0: Not enabled 1: Enabled for L3 LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 1

LNCFCMOCS1 - LNCF MOCS Register 1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00170013
Size (in bits):	32
Address:	0B024h

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 010111b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 010011b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 2

LNCFCMOCS2 - LNCF MOCS Register 2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0020001F
Size (in bits):	32
Address:	0B028h

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 100000b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 011111b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 3

LNCFCMOCS3 - LNCF MOCS Register 3

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00170013
Size (in bits):	32
Address:	0B02Ch

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 010111b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 010011b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 4

LNCFCMOCS4 - LNCF MOCS Register 4

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0030001F
Size (in bits):	32
Address:	0B030h

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 110000b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 011111b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 5

LNCFCMOCS5 - LNCF MOCS Register 5

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00170013
Size (in bits):	32
Address:	0B034h

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 010111b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 010011b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 6

LNCFCMOCS6 - LNCF MOCS Register 6

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000001F
Size (in bits):	32
Address:	0B038h

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 000000b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 011111b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 7

LNCFCMOCS7 - LNCF MOCS Register 7

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	0B03Ch

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 000000b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 000000b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 8

LNCFCMOCS8 - LNCF MOCS Register 8

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00100000
Size (in bits):	32
Address:	0B040h

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 010000b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 000000b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 9

LNCFCMOCS9 - LNCF MOCS Register 9

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00170013
Size (in bits):	32
Address:	0B044h

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 010111b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 010011b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 10

LNCFCMOCS10 - LNCF MOCS Register 10

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0020001F
Size (in bits):	32
Address:	0B048h

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 100000b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 011111b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 11

LNCFCMOCS11 - LNCF MOCS Register 11

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00170013
Size (in bits):	32
Address:	0B04Ch

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 010111b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 010011b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 12

LNCFCMOCS12 - LNCF MOCS Register 12

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0030001F
Size (in bits):	32
Address:	0B050h

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 110000b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 011111b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 13

LNCFCMOCS13 - LNCF MOCS Register 13

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00170013
Size (in bits):	32
Address:	0B054h

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 010111b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 010011b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 14

LNCFCMOCS14 - LNCF MOCS Register 14

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000001F
Size (in bits):	32
Address:	0B058h

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 000000b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 011111b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 15

LNCFCMOCS15 - LNCF MOCS Register 15

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	0B05Ch

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 000000b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 000000b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 16

LNCFCMOCS16 - LNCF MOCS Register 16

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00100000
Size (in bits):	32
Address:	0B060h

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 010000b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 000000b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 17

LNCFCMOCS17 - LNCF MOCS Register 17

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00170013
Size (in bits):	32
Address:	0B064h

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 010111b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 010011b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 18

LNCFCMOCS18 - LNCF MOCS Register 18

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0020001F
Size (in bits):	32
Address:	0B068h

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 100000b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 011111b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 19

LNCFCMOCS19 - LNCF MOCS Register 19

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00170013
Size (in bits):	32
Address:	0B06Ch

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 010111b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 010011b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 20

LNCFCMOCS20 - LNCF MOCS Register 20

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0030001F
Size (in bits):	32
Address:	0B070h

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 110000b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 011111b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 21

LNCFCMOCS21 - LNCF MOCS Register 21

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00170013
Size (in bits):	32
Address:	0B074h

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 010111b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 010011b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 22

LNCFCMOCS22 - LNCF MOCS Register 22

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000001F
Size (in bits):	32
Address:	0B078h

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 000000b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 011111b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 23

LNCFCMOCS23 - LNCF MOCS Register 23

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	0B07Ch

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 000000b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 000000b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 24

LNCFCMOCS24 - LNCF MOCS Register 24

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00100000
Size (in bits):	32
Address:	0B080h

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 010000b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 000000b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 25

LNCFCMOCS25 - LNCF MOCS Register 25

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00170013
Size (in bits):	32
Address:	0B084h

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 010111b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 010011b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 26

LNCFCMOCS26 - LNCF MOCS Register 26

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0020001F
Size (in bits):	32
Address:	0B088h

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 100000b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 011111b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 27

LNCFCMOCS27 - LNCF MOCS Register 27

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00170013
Size (in bits):	32
Address:	0B08Ch

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 010111b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 010011b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 28

LNCFCMOCS28 - LNCF MOCS Register 28

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0030001F
Size (in bits):	32
Address:	0B090h

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 110000b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 011111b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 29

LNCFCMOCS29 - LNCF MOCS Register 29

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00170013
Size (in bits):	32
Address:	0B094h

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 010111b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 010011b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 30

LNCFCMOCS30 - LNCF MOCS Register 30

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000001F
Size (in bits):	32
Address:	0B098h

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 000000b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 011111b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF MOCS Register 31

LNCFCMOCS31 - LNCF MOCS Register 31

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	0B09Ch

This register is for Mocs index

DWord	Bit	Description
0	31:22	**Reserved** Access: RO
	21:16	**MOCS upper data** Default Value: 000000b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.
	15:6	**Reserved** Access: RO
	5:0	**MOCS lower data** Default Value: 000000b Access: R/W Refer LNCF MOCS Register 0 for detailed description LNCF MOCS implementation does not support write to individual MOCS index. S/W needs to write both upper and lower index together. If S/W needs to write to a single index, it should read,merge and write it back.

LNCF Render config save msg

LNCFRCSR - LNCF Render config save msg		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B0F8h	
This register is not context saved and is written by CS unit		
DWord	**Bit**	**Description**
0	31:17	**Reserved** Access: RO
	16	**Render Context save Request Mask** Access: R/W Hardware Clear Bit[16] Render Context Save Request Mask 0 : LNCFRCSR.Bit[0] is masked (default) 1 : LNCFRCSR.Bit[0] is valid
	15:1	**Reserved** Access: RO
	0	**Render Context save Request** Access: R/W Hardware Clear Bit[0] Render Context Save Request 0 : Render context save is not being requested (default) 1 : Render context save is being requested Unit needs to self-clear this bit upon sampling.

Load Indirect Base Vertex

3DPRIM_BASE_VERTEX - Load Indirect Base Vertex	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02440h-02443h
Valid Projects:	

DWord	Bit	Description
0	31:0	**Base Vertex** Format: S31 This register is used to store the Base Vertex of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Instance Count

3DPRIM_INSTANCE_COUNT - Load Indirect Instance Count	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02438h-0243Bh
Valid Projects:	

DWord	Bit	Description
0	31:0	**Instance Count** This register is used to store the Instance Count of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Start Instance

3DPRIM_START_INSTANCE - Load Indirect Start Instance	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0243Ch-0243Fh
Valid Projects:	

DWord	Bit	Description
0	31:0	**Start Vertex** Format: U32 This register is used to store the Start Instance of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Start Vertex

3DPRIM_START_VERTEX - Load Indirect Start Vertex

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02430h-02433h

DWord	Bit	Description
0	31:0	**Start Vertex** Format: U32 This register is used to store the Start Vertex of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Vertex Count

3DPRIM_VERTEX_COUNT - Load Indirect Vertex Count	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02434h-02437h

DWord	Bit	Description
0	31:0	**Vertex Count** Format: U32 This register is used to store the Vertex Count of the 3D_PRIMITIVE command when Load Indirect Enable is set.

LPFC control register

LPFCCNTL - LPFC control register		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B01Ch	
LPFC control register.		
DWord	**Bit**	**Description**
0	31	**LPFC enable signal** Access: R/W LPPC event collection enable signal. Incf_lpfc_cnt_en.
	30	**LPFC Global enable signal** Access: R/W LPFCSL unit global enable signal. 0b - LPFCSL unit is disabled. 1b - LPFCSL unit is enabled. Incf_lpfc_gbl_en
	29:0	**Reserved** Access: RO Reserved.