Intel® UHD Graphics Open Source

Programmer's Reference Manual

For the 2021 11th Generation Intel Core™ Processors, Intel Xeon® Processors, and Intel 500 Series Chipsets based on the "Rocket Lake" Platform

Volume 2: Command Reference: Registers

July 2022, Revision 1.0

Notices and Disclaimers

Intel technologies may require enabled hardware, software or service activation.

No product or component can be absolutely secure.

Code names are used by Intel to identify products, technologies, or services that are in development and not publicly available. These are not "commercial" names and not intended to function as trademarks

Customer is responsible for safety of the overall system, including compliance with applicable safety-related requirements or standards.

No license (express or implied, by estoppel or otherwise) to any intellectual property rights is granted by this document, with the sole exceptions that a) you may publish an unmodified copy and b) code included in this document is licensed subject to Zero-Clause BSD open-source license (0BSD). You may create software implementations based on this document and in compliance with the foregoing that are intended to execute on the Intel product(s) referenced in this document. No rights are granted to create modifications or derivatives of this document.

The products described may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

You may not use or facilitate the use of this document in connection with any infringement or other legal analysis concerning Intel products described herein. You agree to grant Intel a non-exclusive, royalty-free license to any patent claim thereafter drafted which includes subject matter disclosed herein.

Intel disclaims all express and implied warranties, including without limitation, the implied warranties of merchantability, fitness for a particular purpose, and non-infringement, as well as any warranty arising from course of performance, course of dealing, or usage in trade.

Intel may make changes to specifications and product descriptions at any time, without notice. Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined". Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. The information here is subject to change without notice. Do not finalize a design with this information.

Table of Contents

ARB_CTL

ARB_CTL

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	45000h-45003h
Name:	Display Arbitration Control 1
ShortName:	ARB_CTL
Reset:	soft

DWord	Bit	Description
0	31	**FBC Memory Wake** Access: R/W Setting this bit allows FBC compressed write requests to wake memory. Value: 1b — Name: Wake On **[Default]** Value: 0b — Name: Wake Off
	30	**Reserved** Access: R/W
	29	**Reserved** Access: RO Format: MBZ
	28:26	**HP Queue Watermark** Access: R/W The value in this register indicates the number of entries the high priority queue should have before it can be read. The value is zero based. Program the values as N-1, where 3'b011 indicates 4 entries. Value: 011b — Name: 4 entries **[Default]** Value: [0,7] — Name:

ARB_CTL

	25:24	**LP Write Request Limit** Access: R/W The value in this register indicates the maximum number of back-to-back LP write requests that will be accepted from a single client before re-arbitrating. **Value** / **Name** 00b: 1 01b: 2 10b: 4 **[Default]** 11b: 8
	23:20	**TLB Request Limit** Access: R/W The value in this register indicates the maximum number of TLB requests that can be made in an arbitration loop. Zero is not a valid programming. **Value** / **Name** 0110b: 6 **[Default]** [1,15]
	19:16	**TLB Request InFlight Limit** Access: R/W The value in this register indicates the maximum number of TLB (or VTd) requests that can be in flight at any given time. Zero is not a valid programming. **Value** / **Name** 0110b: 6 **[Default]** [1,15]
	15	**FBC Watermark Disable** Access: R/W Setting this bit disables the FBC watermarks. **Value** / **Name** 0b: Enable 1b: Disable

ARB_CTL

	14:13	**Tiled Address Swizzling** Access: R/W DRAM configuration registers show if memory address swizzling is needed. **Value** / **Name** / **Description** 00b / No Display / No display request address swizzling 01b / Reserved / Address bit[6] swizzling for tiled surfaces is not used 10b / Reserved / 11b / Reserved /
	12:8	**HP Page Break Limit** Access: R/W The value in this register represents the maximum number of page breaks allowed in a HP request chain. Zero is not a valid programming. **Value** / **Name** 10000b / 16 **[Default]** [1,31] /
	7	**Reserved** Access: RO Format: MBZ
	6:0	**HP Data Request Limit** Access: R/W The value in this register represents the maximum number of cachelines allowed in a HP request chain. **Value** / **Name** 1010110b / 86 **[Default]** [1,127] / **Restriction** This value must always be programmed greater than 8.

ARB_CTL2

ARB_CTL2

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	45004h-45007h
Name:	Display Arbitration Control 2
ShortName:	ARB_CTL2
Reset:	soft

DWord	Bit	Description
0	31	**Reserved** Access: R/W
	30	**Reserved** Access: RO Format: MBZ
	29:28	**LP WD Write Request Limit** Access: R/W The value in this register indicates the maximum number of back-to-back LP write requests that will be accepted from WD before re-arbitrating. 00b: 1 01b: 2 10b: 4 **[Default]** 11b: 8
	27:26	**DSB LP Write Request Limit** Access: R/W The value in this register indicates the maximum number of back-to-back DSB LP write requests that will be accepted by a single client before re-arbitrating. 00b: 1 01b: 2 10b: 4 **[Default]** 11b: 8

ARB_CTL2

	25:23	**Reserved** Access: RO Format: MBZ
	22:20	**Reserved** Access: RO Format: MBZ
	19:18	**Par5 Request Limit** Access: R/W This field sets the maximum number of par5 requests before arbitration switches to another client. 00b: 1 01b: 2 10b: 4 **[Default]** 11b: 16
	17:16	**FBC Request Limit** Access: R/W This field sets the maximum number of FBC requests before arbitration switches to another client. 00b: 1 01b: 2 **[Default]** 10b: 4 11b: 8
	15:14	**Reserved** Access: RO Format: MBZ
	13	**Reserved** Access: R/W

ARB_CTL2

	12	**Arbiter Trickle Feed Allow On HP Request** Access: R/W If enabled, Arbiter will allow trickle feed request from all clients if any of the client sends a high priority request **Value** / **Name** 0b: Disable **[Default]** 1b: Enable
	11	**Reserved** Access: R/W
	10:9	**Inflight LP Read Request Limit** Access: R/W The value in this register represents the maximum number of LP read request transactions that can be inflight at any given time. **Value** / **Name** 00b: 1 LP 01b: 2 LP 10b: 3 LP 11b: 4 LP **[Default]**
	8:6	**Reserved** Access: RO Format: MBZ
	5:4	**Inflight HP Read Request Limit** Access: R/W The value in this register represents the maximum number of HP read request transactions that can be inflight at any given time. **Value** / **Name** 00b: 128 HP 01b: 64 HP 10b: 32 HP 11b: 16 HP

ARB_CTL2

	3	**Enable IPC** Access: R/W Enables the Isochronous Priority Control. If enabled, Display sends demoted requests once the transition watermark is reached. If transition watermark is not enabled, Display sends demoted requests when the display buffer is full. **Value** / **Name** 0b – Disable 1b – Enable **Programming Notes** This field is not connected in ARB_CTL2_ABOX1 andARB_CTL2_ABOX2. The "Enable IPC" field in ARB_CTL2 enables/disabled IPC in all ABOXs.
	2	**Reserved** Access: RO Format: MBZ
	1:0	**RTID FIFO Watermark** Access: R/W The value in this register represents the watermark value for the RTID FIFO. HP transactions will start only when the FIFO level is above or equal the watermark. **Value** / **Name** 00b – 8 RTIDs 01b – 16 RTIDs 10b – 32 RTIDs 11b – Reserved

AUD_CONFIG

AUD_CONFIG

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Address:	65000h-65003h
Name:	Audio Configuration Transcoder A
ShortName:	AUD_TCA_CONFIG
Reset:	soft

Address:	65100h-65103h
Name:	Audio Configuration Transcoder B
ShortName:	AUD_TCB_CONFIG
Reset:	soft

Address:	65200h-65203h
Name:	Audio Configuration Transcoder C
ShortName:	AUD_TCC_CONFIG
Reset:	soft

This register configures the audio output. There is one instance of this register per transcoder A/B/C. Each Transcoder is independent of the other.

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29	**N value Index** Access: R/W Value / Name / Description: 0b / HDMI **[Default]** / N value read on bits 27:20 and 15:4 reflects HDMI N value. Bits 27:20 and 15:4 are programmable to any N value. Default h7FA6 when bit 28 is not set. 1b / DisplayPort / N value read on bits 27:20 and 15:4 reflects DisplayPort N value. Set this bit to 1 before programming N value register. When this bit is set to 1, 27:20 and 15:4 will reflect the current N value. Default is h8000 when bit 28 is not set.

AUD_CONFIG

28 **N programming enable**

Access:	R/W

This bit enables programming of N values for non-CEA modes. Please note that the transcoder to which audio is attached must be disabled when changing this field.

27:20 **Upper N value**

Default Value:	00000111b
Access:	R/W

These are bits [19:12] of programmable N values for non-CEA modes. Bit 29 of this register must also be written in order to enable programming. Please note that the transcoder to which audio is attached must be disabled when changing this field. See bit 29 description for default values.

19:16 **Pixel Clock HDMI**

Access:	R/W

This is the target frequency of the CEA/HDMI video mode to which the audio stream is added. This value is used for generating N_CTS packets. This refers to only HDMI Pixel clock and does not refer to DisplayPort Link clock. DisplayPort Link clock does not require this programming. Note: The transcoder on which audio is attached must be disabled when changing this field.

Value	Name	Description
0b	**[Default]**	
0000b	25.2 / 1.001 MHz	25.2 / 1.001 MHz
0001b	25.2 MHz	25.2 MHz (Program this value for pixel clocks not listed in this field)
0010b	27 MHz	27 MHz
0011b	27 * 1.001 MHz	27 * 1.001 MHz
0100b	54 MHz	54 MHz
0101b	54 * 1.001 MHz	54 * 1.001 MHz
0110b	74.25 / 1.001 MHz	74.25 / 1.001 MHz
0111b	74.25 MHz	74.25 MHz
1000b	148.5 / 1.001 MHz	148.5 / 1.001 MHz
1001b	148.5 MHz	148.5 MHz
1010b	297 / 1.001 MHz	297 / 1.001 MHz
1011b	297 MHz	297 MHz

1100b	594 / 1.001 MHz	594 / 1.001 MHz
1101b	594 MHz	594 MHz
Others	Reserved	Reserved

15:4 Lower N value

Default Value:	111110100110b
Access:	R/W

These are bits [11:0] of programmable N values for non-CEA modes. Bit 29 of this register must also be written in order to enable programming. Please note that the transcoder to which audio is attached must be disabled when changing this field. See bit 29 description for default values

3 Reserved

Access:	R/W

2:0 Reserved

Access:	RO
Format:	MBZ

AUD_CONFIG_2

AUD_CONFIG_2	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	65004h-65007h
Name:	Audio Configuration Register 2 Transcoder A
ShortName:	AUD_TCA_CONFIG_2
Reset:	soft
Address:	65104h-65107h
Name:	Audio Configuration Register 2 Transcoder B
ShortName:	AUD_TCB_CONFIG_2
Reset:	soft
Address:	65204h-65207h
Name:	Audio Configuration Register 2 Transcoder C
ShortName:	AUD_TCC_CONFIG_2
Reset:	soft

This is a new register to add 297 and 584MHz frequencies support for HDMI TMDS clocks. These are programmed along with the other lower bits of the N and CTS values in the Audio Config register. There is one instance of this register per transcoder A/B/C. Each Transcoder is independent of the other.

DWord	Bit	Description
0	31	**Reserved** Access: R/W
	30:21	**Reserved** Access: RO Format: MBZ
	20:16	**DPSpecVersion** Default Value: 00010010b Access: R/W DP spec version number that goes in the header of the samples. Default 12h for DP MST. Currently DP Compliance is expecting this field to be 00010001 (DP1.1) as the Compliance spec has not been updated. SW must program this register to "00010001" to overcome this compliance failure. This programming can be updated after the Compliance Specification is updated.

AUD_CONFIG_2		
	15:12	**Reserved** Access: RO Format: MBZ
	11:8	**Upper bits for N value** Access: R/W These are bits are concatenated as the upper 4 bits to the N value in the AUD_CONFIG register. Please note that the transcoder to which audio is attached must be disabled when changing this field. See bit 29 description for default values
	7:4	**Reserved** Access: RO Format: MBZ
	3:0	**Upper bits for MCTS value** Access: R/W These are the upper 4bits concatenated to CTS or M generation for CTM modes.

AUD_DIP_ELD_CTRL_ST

AUD_DIP_ELD_CTRL_ST

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Address:	650B4h-650B7h
Name:	Audio Control State for DIP and ELD Transcoder A
ShortName:	AUD_TCA_DIP_ELD_CTRL_ST
Reset:	soft

Address:	651B4h-651B7h
Name:	Audio Control State for DIP and ELD Transcoder B
ShortName:	AUD_TCB_DIP_ELD_CTRL_ST
Reset:	soft

Address:	652B4h-652B7h
Name:	Audio Control State for DIP and ELD Transcoder C
ShortName:	AUD_TCC_DIP_ELD_CTRL_ST
Reset:	soft

There is one instance of this register per transcoder A/B/C.

DWord	Bit	Description
0	31:28	**DIP Port Select** Access: RO This read-only bit reflects which port is used to transmit the DIP data. This can only change when DIP is disabled. If one or more audio-related DIP packets is enabled and audio is enabled on a digital port, these bits will reflect the digital port to which audio is directed. For DP MST, this is the device select/pipe select.

Value	Name	Description
0000b	Reserved **[Default]**	Reserved
0001b	Digital Port B	Digital Port B
0010b	Digital Port C	Digital Port C
0011b	USBC1	USBC1
0100b	USBC2	USBC2
0101b	USBC3	USBC3
0110b	USBC4	USBC4
0111b	USBC5	USBC5
1000b	USBC6	USBC6

AUD_DIP_ELD_CTRL_ST

27:25 **Reserved**

Access:	RO
Format:	MBZ

24:21 **DIP type enable status**

Access:	RO

These bits reflect the DIP types enabled. It can be updated while the port is enabled. Within 2 vblank periods, the DIP is guaranteed to have been transmitted. Disabling a DIP type results in setting the contents of that DIP buffer to zero. A reserved setting reflects a disabled DIP.

Value	Name	Description
0000b	**[Default]**	
XXX0b	DIP Disable	Audio DIP disabled
XXX1b	DIP Enable	Audio DIP enabled
XX0Xb	ACP Disable	Generic 1 (ACP) DIP disabled
XX1Xb	ACP Enable	Generic 1 (ACP) DIP enabled
X0XXb	Generic 2 Disable	Generic 2 DIP disabled
X1XXb	Generic 2 Enable	Generic 2 DIP enabled, can be used by ISRC1 or ISRC2
1XXXb	Reserved	Reserved

20:18 **DIP buffer index**

Access:	R/W

This field is used during read of different DIPs, and during read or write of ELD data. These bits are used as an index to their respective DIP or ELD buffers. When the index is not valid, the contents of the DIP will return all 0s.

Value	Name	Description
000b	Audio **[Default]**	Audio DIP (31 bytes of address space, 31 bytes of data)
001b	Gen 1	Generic 1 (ACP) Data Island Packet (31 bytes of address space, 31 bytes of data)
010b	Gen 2	Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data)
011b	Gen 3	Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data)
Others	Reserved	Reserved

AUD_DIP_ELD_CTRL_ST

17:16 DIP transmission frequency

Access:	RO

These bits reflect the frequency of DIP transmission for the DIP buffer type designated in bits 20:18. When writing DIP data, this value is also latched when the first DW of the DIP is written. When read, this value reflects the DIP transmission frequency for the DIP buffer designated in bits 20:18.

Value	Name	Description
00b	Disable **[Default]**	Disabled
01b	Reserved	Reserved
10b	Send Once	Send Once
11b	Best Effort	Best effort (Send at least every other vsync)

15 Reserved

Access:	RO
Format:	MBZ

14:10 ELD buffer size

Default Value:	10101b
Access:	RO

This field reflects the size of the ELD buffer in DWORDs (84 Bytes of ELD)

9:5 ELD access address

Access:	R/W

Selects the DWORD address for access to the ELD buffer (84 bytes). The value wraps back to zero when incremented past the max addressing value 0x1F. This field change takes effect immediately after being written. The read value indicates the current access address.

4 ELD ACK

Access:	R/W

Acknowledgement from the audio driver that ELD read has been completed

3:0 DIP access address

Access:	R/W

Selects the DWORD address for access to the DIP buffers. The value wraps back to zero when it incremented past the max addressing value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.

AUD_EDID_DATA

AUD_EDID_DATA	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	65050h-65053h
Name:	Audio EDID Data Block Transcoder A
ShortName:	AUD_TCA_EDID_DATA
Reset:	soft
Address:	65150h-65153h
Name:	Audio EDID Data Block Transcoder B
ShortName:	AUD_TCB_EDID_DATA
Reset:	soft
Address:	65250h-65253h
Name:	Audio EDID Data Block Transcoder C
ShortName:	AUD_TCC_EDID_DATA
Reset:	soft

These registers contain the HDMI/DP data block from the EDID. The graphics driver reads the EDID and writes the structure to these registers. The vendor specific data block may be longer than 8 bytes, but the driver must not write more than 48 bytes to the buffer. The EDID format is Version 3 within the CEA-861B specification. The HDMI/DP Vendor Specific Data Block is described in version 1.1 of the HDMI specification. These values are returned from the device as the HDMI/DP Vendor Specific Data Block response to a Get HDMI/DP Widget command. Writing sequence:

- Video software sets ELD invalid, and sets the ELD access address to 0, or to the desired DWORD to be written.
- Video software writes ELD data 1 DWORD at a time. The ELD access address autoincrements with each DWORD write, wrapping around to address 0 when the max buffer address size of 0xF has been reached.
- Please note that software must write an entire DWORD at a time.
- Please note that the audio driver checks the valid bit with each byte read of the ELD. This means that the video driver can unilaterally write ELD irrespective of audio driver ELD read status.

Reading sequence:

- Video software sets the ELD access address to 0, or to the desired DWORD to be read.
- Video software reads ELD data 1 DWORD at a time. The ELD access address autoincrements with each DWORD read, wrapping around to address 0 when the max buffer address size of 0xF has been reached.

There is one instance of this register per transcoder A/B/C.

DWord	Bit	Description

AUD_EDID_DATA		
0	31:0	**EDID Data Block** Access: R/W Please note that the contents of this buffer are not cleared when ELD is disabled. The contents of this buffer are cleared during FLR.

AUD_INFOFR

AUD_INFOFR	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	65054h-65057h
Name:	Audio Widget Data Island Packet Transcoder A
ShortName:	AUD_TCA_INFOFR
Reset:	soft
Address:	65154h-65157h
Name:	Audio Widget Data Island Packet Transcoder B
ShortName:	AUD_TCB_INFOFR
Reset:	soft
Address:	65254h-65257h
Name:	Audio Widget Data Island Packet Transcoder C
ShortName:	AUD_TCC_INFOFR
Reset:	soft

When the IF type or dword index is not valid, the contents of the DIP will return all 0s.
These values are programmed by the audio driver in an HDMI/DP Widget Set command. They are returned one byte at a time from the device on the HD audio bus as the HDMI/DP DIP response to a Get HDMI/DP Widget command. To fetch a specific byte, the audio driver should send an HDMI/DP Widget HDMI/DP DIP Index Pointer Set command to set the index, then fetch the indexed byte using the HDMI/DP DIP get.

DWord	Bit	Description
0	31:0	**Data Island Packet Data** Access: RO This reflects the contents of the DIP indexed by the DIP access address. The contents of this buffer are cleared during function reset or HD audio link reset.

AUD_M_CTS_ENABLE

AUD_M_CTS_ENABLE

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Address:	65028h-6502Bh
Name:	Audio M and CTS Programming Enable Transcoder A
ShortName:	AUD_TCA_M_CTS_ENABLE
Reset:	soft

Address:	65128h-6512Bh
Name:	Audio M and CTS Programming Enable Transcoder B
ShortName:	AUD_TCB_M_CTS_ENABLE
Reset:	soft

Address:	65228h-6522Bh
Name:	Audio M and CTS Programming Enable Transcoder C
ShortName:	AUD_TCC_M_CTS_ENABLE
Reset:	soft

There is one instance of this register per transcoder A/B/C.

DWord	Bit	Description
0	31:22	**Reserved** Access: RO Format: MBZ
	21	**CTS M value Index** Access: R/W Value 0b: Name CTS **[Default]**: CTS value read on bits 19:0 reflects CTS value. Bit 19:0 is programmable to any CTS value. default is 0 Value 1b: Name M: M value read on bits 19:0 reflects DisplayPort M value. Set this bit to 1 before programming M value register. When this is set to 1 19:0 will reflect the current M value
	20	**Enable CTS or M prog** Access: R/W When set will enable CTS or M programming.

AUD_M_CTS_ENABLE		
	19:0	**CTS programming** Access: R/W These are bits [19:0] of programmable CTS values for non-CEA modes. Bit 21 of this register must also be written in order to enable programming. Please note that the transcoder to which audio is attached must be disabled when changing this field.

AUD_PIN_ELD_CP_VLD

AUD_PIN_ELD_CP_VLD

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	650C0h-650C3h
Name:	Audio Pin ELD and CP Ready Status
ShortName:	AUD_PIN_ELD_CP_VLD
Reset:	soft

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:12	**Reserved** Access: RO Format: MBZ
	11	**Audio InactiveC** Access: R/W Inactive: When this bit is set, a digital display sink device has been attached but not active for streaming audio. 0b – Disable – Device is active for streaming audio data 1b – Enable – Device is connected but not active
	10	**Audio Output EnableC** Access: R/W This bit directs audio to the device connected to this transcoder. When enabled along with Inactive set to 0 and audio data is available, the audio data will be combined with the video data and sent over this transcoder. The audio unit uses the status of this bit to indicate presence of the HDMI/DP output to the audio driver. 0b – Disable – No Audio output 1b – Valid – Audio is enabled

AUD_PIN_ELD_CP_VLD

	9	**CP ReadyC** Access: R/W This R/W bit reflects the state of CP request from the audio unit. When an audio CP request has been serviced, it must be reset to 1 by the video software to indicate that the CP request has been serviced. This is transcoder based. Software should add a delay of 1ms before updating the CP ready bit. This is needed to make sure that all the pending unsolicited responses are cleared (transmitted to HD audio) before CP ready unsolicited responses is generated. This is needed in case of DP MST is enabled and when many changes to PD, ELDV and CP ready bits are done during mode set. **Value** / **Name** / **Description** 0b / Pending or Not Ready / CP request pending or not ready to receive requests 1b / Ready / CP request ready
	8	**ELD validC** Access: R/W This R/W bit reflects the state of the ELD data written to the ELD RAM. After writing the ELD data, the video software must set this bit to 1 to indicate that the ELD data is valid. At audio codec initialization, or on a hotplug event, this bit is set to 0 by the video software. This bit is reflected in the audio pin complex widget as the ELD valid status bit. This is transcoder based. **Value** / **Name** / **Description** 0b / Invalid / ELD data invalid (default, when writing ELD data, set 0 by software) 1b / Valid / ELD data valid (Set by video software only)
	7	**Audio InactiveB** Access: R/W Inactive: When this bit is set, a digital display sink device has been attached but not active for streaming audio. **Value** / **Name** / **Description** 0b / Disable / Device is active for streaming audio data 1b / Enable / Device is connected but not active

AUD_PIN_ELD_CP_VLD

	6	**Audio Output EnableB** Access: R/W This bit directs audio to the device connected to this transcoder. When enabled along with Inactive set to 0 and audio data is available, the audio data will be combined with the video data and sent over this transcoder. The audio unit uses the status of this bit to indicate presence of the HDMI/DP output to the audio driver. This is transcoder based. **Value** / **Name** / **Description** 0b / Disable / No audio output 1b / Enable / Audio is enabled
	5	**CP ReadyB** Access: R/W See CP_ReadyC description. **Value** / **Name** / **Description** 0b / Not Ready / CP request pending or not ready to receive requests 1b / Ready / CP request ready
	4	**ELD validB** Access: R/W See ELD_validC descripion. **Value** / **Name** / **Description** 0b / Invalid / ELD data invalid (default, when writing ELD data, set 0 by software) 1b / Valid / ELD data valid (Set by video software only)
	3	**Audio InactiveA** Access: R/W Inactive: When this bit is set, a digital display sink device has been attached but not active for streaming audio. **Value** / **Name** / **Description** 0b / Disable / Device is active for streaming audio data 1b / Enable / Device is connected but not active

AUD_PIN_ELD_CP_VLD

	2	**Audio Output EnableA** Access: R/W This bit directs audio to the device connected to this transcoder. When enabled along with Inactive set to 0 and audio data is available, the audio data will be combined with the video data and sent over this transcoder. The audio unit uses the status of this bit to indicate presence of the HDMI/DP output to the audio driver. This is transcoder based. **Value** / **Name** / **Description** 0b / Disable / No audio output 1b / Enable / Audio is enabled
	1	**CP ReadyA** Access: R/W See CP_ReadyC description. **Value** / **Name** / **Description** 0b / Not Ready / CP request pending or not ready to receive requests 1b / Ready / CP request ready
	0	**ELD validA** Access: R/W See ELD_validC descripion. **Value** / **Name** / **Description** 0b / Invalid / ELD data invalid (default, when writing ELD data, set 0 by software) 1b / Valid / ELD data valid (Set by video software only)

AUD_PIN_PIPE_CONN_ENTRY_LNGTH

AUD_PIN_PIPE_CONN_ENTRY_LNGTH

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32

Address:	650A8h-650ABh
Name:	Audio Connection List Entry and Length Transcoder A
ShortName:	AUD_TCA_PIN_PIPE_CONN_ENTRY_LNGTH_RO
Reset:	soft

Address:	651A8h-651ABh
Name:	Audio Connection List Entry and Length Transcoder B
ShortName:	AUD_TCB_PIN_PIPE_CONN_ENTRY_LNGTH_RO
Reset:	soft

Address:	652A8h-652ABh
Name:	Audio Connection List Entry and Length Transcoder C
ShortName:	AUD_TCC_PIN_PIPE_CONN_ENTRY_LNGTH_RO
Reset:	soft

These values are returned from the device as the Connection List Length response to a Get Pin Widget command or Get Device Widget command if DP MST. There is one instance of this register per transcoder A/B/C.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:8	**Connection List Entry** Access: RO Connection to Convertor Widget Node 0x03
	7	**Long Form** Access: RO This bit indicates whether the items in the connection list are long form or short form. This bit is hardwired to 0 (items in connection list are short form)

<table>
<tr><th colspan="3">AUD_PIN_PIPE_CONN_ENTRY_LNGTH</th></tr>
<tr><td></td><td>6:0</td><td>Connection List Length

<table><tr><td>Default Value:</td><td>0000001b</td></tr><tr><td>Access:</td><td>RO</td></tr></table>This field indicates the number of items in the connection list. If this field is 2, there is only one hardwired input possible, which is read from the Connection List, and there is no Connection Select Control.</td></tr>
</table>

AUD_PIPE_CONN_SEL_CTRL

AUD_PIPE_CONN_SEL_CTRL	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	650ACh-650AFh
Name:	Audio Pipe Connection Select Control
ShortName:	AUD_PIN_PIPE_CONN_SEL_CTRL_RO
Reset:	soft

These values are returned from the device as the Connection List Length response to a Get Pin Widget command or Get Device Widget command for DP MST.

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23:16	**Connection select Control PipeC** Default Value: 0Fh Access: RO Connection Index Currently Set [Default 0x00], PipeC Widget is set to 0x02
	15:8	**Connection select Control PipeB** Default Value: 0Fh Access: RO Connection Index Currently Set [Default 0x00], PipeB Widget is set to 0x01
	7:0	**Connection select Control PipeA** Default Value: 0Fh Access: RO Connection Index Currently Set [Default 0x00], PipeA Widget is set to 0x00

BLC_PWM_CTL

BLC_PWM_CTL

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	48250h-48253h
Name:	Backlight PWM Control
ShortName:	BLC_PWM_CTL
Reset:	soft

This register controls the backlight PWM logic going to the display utility pin on the CPU.

DWord	Bit	Description
0	31	**PWM Enable** Access: R/W This bit enables the PWM logic. Value / Name / Description: 0b / Disable / PWM disabled 1b / Enable / PWM enabled **Restriction** The display utility pin must be configured correctly to output the PWM. Program the frequency and duty cycle before enabling PWM.
	30:29	**Pipe Select** Access: R/W This field selects which vertical blank will be used for backlight blinking. Value / Name / Description: 00b / Pipe A / Use Pipe A 01b / Pipe B / Use Pipe B 10b / Pipe C / Use Pipe C
	28	**Blinking Enable** Access: R/W This bit enables backlight blinking. When enabled, the backlight will be driven on at the programmed brightness during vertical blank and driven off during vertical active. Value / Name: 0b / Disable 1b / Enable

BLC_PWM_CTL

	27	**PWM Granularity** Access: R/W This field controls the granularity (minimum increment) of the PWM backlight control counter. **Value** / **Name** / **Description** 0b / 128 / PWM frequency adjustment on 128 clock increments 1b / 8 / PWM frequency adjustment on 8 clock increments
	26:0	**Reserved** Access: RO Format: MBZ

BW_BUDDY_CTL

BW_BUDDY_CTL

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	45130h-45133h
Name:	Bandwidth Buddy0 Control
ShortName:	BW_BUDDY0_CTL
Reset:	soft

DWord	Bit	Description
0	31	**BW Buddy Disable** Access: R/W This field indicates if the address buddy logic is disabled. Value: 0b — Name: Enabled **[Default]** Value: 1b — Name: Disabled
	30	**Reserved** Access: R/W
	29	**Reserved** Access: RO Format: MBZ
	28:23	**Plane Request Timer** Access: R/W This is the timer to pick when a tracker gets allocated by a regular HP plane Request and starts to wait for its buddy (based on the mask) to come in. Value: 010000b — Name: 16 **[Default]** Value: [1,63]
	22	**Reserved** Access: RO Format: MBZ

BW_BUDDY_CTL

	21:16	**TLB Request Timer** Access: R/W This is the timer to pick when a tracker gets allocated by a TLB Request and starts to wait for its buddy (based on the mask) to come in. **Value** / **Name** 0010000b: 8 **[Default]** [1,63]
	15	**Reserved** Access: R/W
	14:0	**Reserved** Access: RO Format: MBZ

BW_BUDDY_PAGE_MASK

BW_BUDDY_PAGE_MASK

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	45134h-45137h
Name:	Bandwidth Buddy0 Page Mask
ShortName:	BW_BUDDY0_PAGE_MASK
Reset:	soft

DWord	Bit	Description
0	31:28	**Reserved** Access: RO Format: MBZ
	27:0	**BW Buddy Page Mask** Default Value: 0000000h All address bits are not Masked Access: R/W When set, bits in this register will cause Address bits to be excluded from the buddy address comparison. Mask bit[0] is associated with address bit[9], mask bit[1] is associated with address bit[10] and so on. For example, if bit [0] of the mask register is set, then address bit[9] is not used in the buddy address comparison. The default is to compare all address bits. **Programming Notes** Optimal programming will depend on the memory configuration used. See **Arbiter** page for details.

Capabilities A

CAPID0_A_0_2_0_PCI - Capabilities A

Register Space:	PCI: 0/2/0
Size (in bits):	32
Address:	00044h

Populated by pulling relevant fuses.

DWord	Bit	Description
0	31:25	**Spare Fuses 1** Default Value: 00h Access: RO Variant _Custom_GTIReset: BUS Spare Fuse
	24	**Display FuSa disable** Default Value: 0b Access: RO Variant _Custom_GTIReset: BUS Fuse to disable FuSa
	23:4	**Spare Fuses 2** Default Value: 00000h Access: RO Variant _Custom_GTIReset: BUS Spare Fuses
	3	**VGT Enable Fuse** Default Value: 0b Access: RO Variant _Custom_GTIReset: BUS
	2	**Spare fuses 3** Access: RO Variant _Custom_GTIReset: BUS Spare fuse Value: 0b Name:

CAPID0_A_0_2_0_PCI - Capabilities A

	1	**SVM Disable Fuse** Default Value: 0b Access: RO Variant _Custom_GTIReset: BUS
	0	**Vtd Disable Fuse** Default Value: 0b Access: RO Variant _Custom_GTIReset: BUS

CDCLK_CTL

CDCLK_CTL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	46000h-46003h
Name:	CD Clock Control
ShortName:	CDCLK_CTL
Reset:	global

This register is not reset by the device 2 FLR.

Restriction
These fields should only be changed as part of the Display Sequences for Changing CD Clock Frequency.

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23:22	**CD2X Divider Select** Access: Double Buffered _Custom_Display_DoubleBufferUpdatePoint: Pipe off or start of vertical blank This field selects how the CDCLK PLL output is divided before driving the display CD2X clock. This field is double buffered to align with the pipe from CD2X Pipe Select. It will update at the start of vertical blank of the selected pipe, or immediately if the selected pipe is disabled or no pipe is selected. The divider change needs to happen within the vertical blank so the few cycles with clock stopped will not disrupt pixel traffic. Value / Name: 00b: Divide by 1 01b: Divide by 1.5 10b: Divide by 2 **[Default]** 11b: Divide by 4

CDCLK_CTL

		Restriction CD2X Divider Select must only be changed while no pipe is enabled, a single pipe is enabled, or multiple pipes are enabled all with the same vertical blank alignment by port sync, genlock, or pipe joining. CD2X Divider Select must not be changed while multiple pipes are enabled without vertical blank alignment.
	21:19	**CD2X Pipe Select** Access: R/W This field selects the pipe enable and vertical blank to be used for double buffering the CD2X Divider Select. To change CD2X Divider Select while a single pipe is enabled, set the select to that pipe. To change CD2X Divider Select while multiple pipes are enabled all with the same vertical blank alignment, set the select to one of those pipes. Value / Name / Description: 000b / Pipe A / 010b / Pipe B / 100b / Pipe C / 111b / None / Double buffer enable is tied to 1 so that writes to the CD2X Divider Select will take effect immediately.
	18	**Reserved** Access: R/W
	17	**Reserved** Access: R/W
	16	**SSA Precharge Enable** Access: R/W This field is unused. Value / Name: 0b / Disable
	15	**Reserved** Access: RO Format: MBZ
	14:11	**Reserved** Access: RO Format: MBZ

CDCLK_CTL

10:0 **CD Frequency Decimal**

Access:	R/W
Format:	U10.1

This field selects the decimal value of the frequency for CD clock, which is used to generate divided down clocks for some display engine timers. This value is represented in a 10.1 format with 10 integer bits and 1 fractional bit.
Many possible values are listed here, and not all valid values are included. To find which values are valid for a project, refer to the clocks page for that project.

Program this field to select the pre-defined value that matches the CD frequency chosen by the CDCLK PLL and CD2X Divider. If no value is defined, program this field with the CD frequency, rounded to the closest 0.5, then minus one.

Value	Name	Description
00 1010 0111 0b	168 MHz CD **[Default]**	This value is default, but not valid.
00101011000b	172.8 MHz CD	
00101100100b	179.2 MHz CD	
00101100110b	180 MHz CD	
00101111110b	192 MHz CD	
01001100100b	307.2 MHz CD	
01 0011 0111 0b	312 MHz CD	
01010000110b	324 MHz CD	
01010001011b	326.4MHz CD	
01110111110b	480MHz CD	
10 0010 0111 0b	552 MHz CD	
10 0010 1100 0b	556.8 MHz CD	
10 1000 0111 0b	648 MHz CD	
10 1000 1100 0b	652.8 MHz CD	

CGE_CTRL

CGE_CTRL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank
Address:	49080h-49083h
Name:	Pipe Color Gamut Enhancement Control
ShortName:	CGE_CTRL_A
Reset:	soft
Address:	49180h-49183h
Name:	Pipe Color Gamut Enhancement Control
ShortName:	CGE_CTRL_B
Reset:	soft
Address:	49280h-49283h
Name:	Pipe Color Gamut Enhancement Control
ShortName:	CGE_CTRL_C
Reset:	soft

DWord	Bit	Description
0	31	**CGE Enable** Access: Double Buffered This bit enables the Color Gamut Enhancement logic. 0b – Disable 1b – Enable
	30	**Allow Double Buffer Update Disable** Access: R/W This field controls whether double buffer updates are allowed to be disabled for the CGE registers that are double buffered. The DOUBLE_BUFFER_CTL register can be configured to globally disable double buffer updates for those resources that allow them to be disabled. 0b – Not Allowed 1b – Allowed **[Default]**

CGE_CTRL		
	29:0	**Reserved** Access: RO Format: MBZ

CGE_WEIGHT

CGE_WEIGHT	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	160
_Custom_Display_ DoubleBufferUpdate Point:	Start of vertical blank OR pipe disabled
Address:	49090h-490A3h
Name:	Pipe Color Gamut Enhancement Weights
ShortName:	CGE_WEIGHT_A
Reset:	soft
Address:	49190h-491A3h
Name:	Pipe Color Gamut Enhancement Weights
ShortName:	CGE_WEIGHT_B
Reset:	soft
Address:	49290h-492A3h
Name:	Pipe Color Gamut Enhancement Weights
ShortName:	CGE_WEIGHT_C
Reset:	soft

These are the weights contained in the lookup up table (LUT) used in pipe color gamut enhancement. LUT index 0 contains the weight for the least saturated colors, and LUT index 16 contains the weight for the most saturated colors. Weight values can range from 00000b (100% of the enhanced output color is from the pipe gamma and CSC output corrected color) to 100000b (100% of the enhanced output color is from the pipe gamma and CSC input color).

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29:24	**CGE Weight Index 3** Access: Double Buffered This is the weight value for this color gamut enhancement LUT index.
	23:22	**Reserved** Access: RO Format: MBZ

<table>
<tr><th colspan="3">CGE_WEIGHT</th></tr>
<tr><td></td><td>21:16</td><td>CGE Weight Index 2
<table><tr><td>Access:</td><td>Double Buffered</td></tr></table>This is the weight value for this color gamut enhancement LUT index.</td></tr>
<tr><td></td><td>15:14</td><td>Reserved
<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td></td><td>13:8</td><td>CGE Weight Index 1
<table><tr><td>Access:</td><td>Double Buffered</td></tr></table>This is the weight value for this color gamut enhancement LUT index.</td></tr>
<tr><td></td><td>7:6</td><td>Reserved
<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td></td><td>5:0</td><td>CGE Weight Index 0
<table><tr><td>Access:</td><td>Double Buffered</td></tr></table>This is the weight value for this color gamut enhancement LUT index.</td></tr>
<tr><td>1</td><td>31:30</td><td>Reserved
<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td></td><td>29:24</td><td>CGE Weight Index 7
<table><tr><td>Access:</td><td>Double Buffered</td></tr></table>This is the weight value for this color gamut enhancement LUT index.</td></tr>
<tr><td></td><td>23:22</td><td>Reserved
<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td></td><td>21:16</td><td>CGE Weight Index 6
<table><tr><td>Access:</td><td>Double Buffered</td></tr></table>This is the weight value for this color gamut enhancement LUT index.</td></tr>
<tr><td></td><td>15:14</td><td>Reserved
<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
</table>

CGE_WEIGHT		
	13:8	**CGE Weight Index 5** Access: Double Buffered This is the weight value for this color gamut enhancement LUT index.
	7:6	**Reserved** Access: RO Format: MBZ
	5:0	**CGE Weight Index 4** Access: Double Buffered This is the weight value for this color gamut enhancement LUT index.
2	31:30	**Reserved** Access: RO Format: MBZ
	29:24	**CGE Weight Index 11** Access: Double Buffered This is the weight value for this color gamut enhancement LUT index.
	23:22	**Reserved** Access: RO Format: MBZ
	21:16	**CGE Weight Index 10** Access: Double Buffered This is the weight value for this color gamut enhancement LUT index.
	15:14	**Reserved** Access: RO Format: MBZ
	13:8	**CGE Weight Index 9** Access: Double Buffered This is the weight value for this color gamut enhancement LUT index.
	7:6	**Reserved** Access: RO Format: MBZ

CGE_WEIGHT		
	5:0	**CGE Weight Index 8** Access: Double Buffered This is the weight value for this color gamut enhancement LUT index.
3	31:30	**Reserved** Access: RO Format: MBZ
	29:24	**CGE Weight Index 15** Access: Double Buffered This is the weight value for this color gamut enhancement LUT index.
	23:22	**Reserved** Access: RO Format: MBZ
	21:16	**CGE Weight Index 14** Access: Double Buffered This is the weight value for this color gamut enhancement LUT index.
	15:14	**Reserved** Access: RO Format: MBZ
	13:8	**CGE Weight Index 13** Access: Double Buffered This is the weight value for this color gamut enhancement LUT index.
	7:6	**Reserved** Access: RO Format: MBZ
	5:0	**CGE Weight Index 12** Access: Double Buffered This is the weight value for this color gamut enhancement LUT index.
4	31:6	**Reserved** Access: RO Format: MBZ

CGE_WEIGHT		
	5:0	**CGE Weight Index 16** Access: Double Buffered This is the weight value for this color gamut enhancement LUT index.

CSC_COEFF

CSC_COEFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	192
_Custom_Display_ DoubleBufferArmedBy:	Write to CSC_MODE
_Custom_Display_ DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	49010h-49027h
Name:	Pipe CSC Coefficients
ShortName:	CSC_COEFF_A
Reset:	soft
Address:	49110h-49127h
Name:	Pipe CSC Coefficients
ShortName:	CSC_COEFF_B
Reset:	soft
Address:	49210h-49227h
Name:	Pipe CSC Coefficients
ShortName:	CSC_COEFF_C
Reset:	soft

DWord	Bit	Description
0	31:16	**RY** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**GY** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
1	31:16	**BY** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**Reserved** Access: RO Format: MBZ

CSC_COEFF		
2	31:16	**RU** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**GU** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
3	31:16	**BU** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**Reserved** Access: RO Format: MBZ
4	31:16	**RV** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**GV** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
5	31:16	**BV** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**Reserved** Access: RO Format: MBZ

CSC_MODE

CSC_MODE	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_ DoubleBufferUpdatePoint:	Start of vertical blank OR pipe disabled
Address:	49028h-4902Bh
Name:	Pipe CSC Mode
ShortName:	CSC_MODE_A
Reset:	soft
Address:	49128h-4912Bh
Name:	Pipe CSC Mode
ShortName:	CSC_MODE_B
Reset:	soft
Address:	49228h-4922Bh
Name:	Pipe CSC Mode
ShortName:	CSC_MODE_C
Reset:	soft

Writes to this register arm CSC registers for this pipe.

DWord	Bit	Description
0	31	**Pipe CSC Enable** Access: Double Buffered This bit enables the pipe color space conversion.
	30	**Pipe Output CSC Enable** Access: Double Buffered This bit enables the pipe output color space conversion.
	29	**Allow Double Buffer Update Disable** Access: R/W This field controls whether double buffer updates are allowed to be disabled for the Color Space Conversion registers that are double buffered. The DOUBLE_BUFFER_CTL register can be configured to globally disable double buffer updates for those resources that allow them to be disabled. Value: 0b — Name: Not Allowed Value: 1b — Name: Allowed **[Default]**

CSC_MODE		
	28	**Reserved** Access: RO Format: MBZ
	27:0	**Reserved** Access: RO Format: MBZ

CSC_POSTOFF

CSC_POSTOFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	96
_Custom_Display_ DoubleBufferArmedBy:	Write to CSC_MODE
_Custom_Display_ DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	49040h-4904Bh
Name:	Pipe CSC Post-Offsets
ShortName:	CSC_POSTOFF_A
Reset:	soft
Address:	49140h-4914Bh
Name:	Pipe CSC Post-Offsets
ShortName:	CSC_POSTOFF_B
Reset:	soft
Address:	49240h-4924Bh
Name:	Pipe CSC Post-Offsets
ShortName:	CSC_POSTOFF_C
Reset:	soft

The post-offset is intended to add an offset from 0 on the Y or RGB channels and to convert UV channels from 2's complement to excess 0.5 as they exit pipe color space conversion (CSC).

DWord	Bit	Description
0	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PostCSC High Offset** Access: Double Buffered This value is used to give an offset to the high color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
1	31:13	**Reserved** Access: RO Format: MBZ

<table>
<tr><th colspan="3">CSC_POSTOFF</th></tr>
<tr><td></td><td>12:0</td><td>PostCSC Medium Offset

<table><tr><td>Access:</td><td>Double Buffered</td></tr></table>This value is used to give an offset to the medium color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).</td></tr>
<tr><td rowspan="2">2</td><td>31:13</td><td>Reserved

<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td>12:0</td><td>PostCSC Low Offset

<table><tr><td>Access:</td><td>Double Buffered</td></tr></table>This value is used to give an offset to the low color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).</td></tr>
</table>

CSC_PREOFF

CSC_PREOFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	96
_Custom_Display_ DoubleBufferArmedBy:	Write to CSC_MODE
_Custom_Display_ DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	49030h-4903Bh
Name:	Pipe CSC Pre-Offsets
ShortName:	CSC_PREOFF_A
Reset:	soft
Address:	49130h-4913Bh
Name:	Pipe CSC Pre-Offsets
ShortName:	CSC_PREOFF_B
Reset:	soft
Address:	49230h-4923Bh
Name:	Pipe CSC Pre-Offsets
ShortName:	CSC_PREOFF_C
Reset:	soft

The pre-offset is intended to remove an offset from 0 on the Y or RGB channels and to convert UV channels from excess 0.5 to 2's complement as they enter pipe color space conversion (CSC).

DWord	Bit	Description
0	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PreCSC High Offset** Access: Double Buffered This value is used to give an offset to the high color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
1	31:13	**Reserved** Access: RO Format: MBZ

<table>
<tr><th colspan="3">CSC_PREOFF</th></tr>
<tr><td></td><td>12:0</td><td>PreCSC Medium Offset

<table><tr><td>Access:</td><td>Double Buffered</td></tr></table>This value is used to give an offset to the medium color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).</td></tr>
<tr><td rowspan="2">2</td><td>31:13</td><td>Reserved

<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td>12:0</td><td>PreCSC Low Offset

<table><tr><td>Access:</td><td>Double Buffered</td></tr></table>This value is used to give an offset to the low color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).</td></tr>
</table>

CUR_BASE

CUR_BASE	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_ DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled
Address:	70084h-70087h
Name:	Cursor Base Address
ShortName:	CUR_BASE_A
Reset:	soft
Address:	71084h-71087h
Name:	Cursor Base Address
ShortName:	CUR_BASE_B
Reset:	soft
Address:	72084h-72087h
Name:	Cursor Base Address
ShortName:	CUR_BASE_C
Reset:	soft

Writes to this register arm cursor registers for this pipe.

DWord	Bit	Description
0	31:12	**Cursor Base 31 12** Access: Double Buffered Format: GraphicsAddress[31:12] This field specifies bits 31:12 of the graphics address of the base of the cursor for hi-res mode. When performing 180 degree rotation, this address does not need to change, hardware will internally offset to start from the last pixel of the last line of the cursor. **Workaround** To prevent false VT-d type 6 errors, use 64KB address alignment and allocate an extra 2 Page Table Entries (PTEs) beyond the end of the displayed surface. Only the PTEs will be used, not the pages themselves. **Restriction** The cursor surface address must be 4K byte aligned. The cursor must be in linear memory, it cannot be tiled.

CUR_BASE		
	11	**Reserved** Access: Double Buffered
	10:7	**Reserved** Access: RO Format: MBZ
	6:4	**Reserved** Access: Double Buffered
	3	**Reserved** Access: RO Format: MBZ
	2	**Reserved** Access: Double Buffered
	1:0	**Reserved** Access: RO Format: MBZ

CUR_COLOR_CTL

CUR_COLOR_CTL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_ DoubleBufferArmedBy:	Write to CUR_BASE or cursor not enabled
_Custom_Display_ DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	700C0h-700C3h
Name:	Cursor Color Control
ShortName:	CUR_COLOR_CTL_A
Reset:	soft
Address:	710C0h-710C3h
Name:	Cursor Color Control
ShortName:	CUR_COLOR_CTL_B
Reset:	soft
Address:	720C0h-720C3h
Name:	Cursor Color Control
ShortName:	CUR_COLOR_CTL_C
Reset:	soft

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15	**Tone Mapping Enable** Access: Double Buffered This field enables the tone mapping of cursor pixels using the programmed tone mapping factor. Value / Name: 1b: Enable 0b: Disable
	14:10	**Reserved** Access: RO Format: MBZ

CUR_COLOR_CTL		
	9:0	**Tone Mapping Factor** Access: Double Buffered This field specifies the tone mapping factor. Each color component gets corrected with this programmed 10 bit fractional value.

CUR_CSC_COEFF

CUR_CSC_COEFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	192
_Custom_Display_ DoubleBufferArmedBy:	Write to CUR_BASE
_Custom_Display_ DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	700D0h-700E7h
Name:	Cursor CSC Coefficients
ShortName:	CUR_CSC_COEFF_A
Reset:	soft
Address:	710D0h-710E7h
Name:	Cursor CSC Coefficients
ShortName:	CUR_CSC_COEFF_B
Reset:	soft
Address:	720D0h-720E7h
Name:	Cursor CSC Coefficients
ShortName:	CUR_CSC_COEFF_C
Reset:	soft

DWord	Bit	Description
0	31:16	**RY** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**GY** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
1	31:16	**BY** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**Reserved** Access: RO Format: MBZ

CUR_CSC_COEFF		
2	31:16	**RU** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**GU** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
3	31:16	**BU** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**Reserved** Access: RO Format: MBZ
4	31:16	**RV** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**GV** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
5	31:16	**BV** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**Reserved** Access: RO Format: MBZ

CUR_CTL

CUR_CTL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to CUR_BASE or cursor not enabled
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	70080h-70083h
Name:	Cursor Control
ShortName:	CUR_CTL_A
Reset:	soft
Address:	71080h-71083h
Name:	Cursor Control
ShortName:	CUR_CTL_B
Reset:	soft
Address:	72080h-72083h
Name:	Cursor Control
ShortName:	CUR_CTL_C
Reset:	soft
Address:	70880h-70883h
Name:	Selective Fetch Cursor Control
ShortName:	SEL_FETCH_CUR_CTL_A
Reset:	soft

The cursor is enabled by programming a valid cursor mode in the cursor mode select fields. The cursor is disabled by programming all 0s in the cursor mode select fields.

DWord	Bit	Description
0	31	**Reserved** Access: RO Format: MBZ
	30:28	**Pipe Slice Arbitration Slots** Access: Double Buffered This field specifies the number of slots allocated to cursor in pipe slice request arbitration. This field is ignored when the 'PIPE_SLICE_ARBITRATION_CTL->Use Programmed Slots' is not set. This field is zero based; a programmed value of 0 results in 1 slot allocation.

CUR_CTL

	27	**Reserved** Access: RO Format: MBZ
	26	**Gamma Enable** Access: Double Buffered This bit enables pipe gamma correction for the cursor pixel data. In VGA pop-up operation, the cursor data will always bypass gamma. This field is deprecated. Value / Name 0b: Disable 1b: Enable
	25	**Reserved** Access: RO Format: MBZ
	24	**Pipe CSC Enable** Access: Double Buffered This bit enables pipe color space conversion for the cursor pixel data. Use CSC_MODE.Pipe CSC Enable, GAMMA_MODE.*_GAMMA_ENABLE for enabling pipe color space conversion and gamma respectively across all pixels from all planes. Cursor CSC must be used for cursor specific color space conversion. This field is deprecated. Value / Name 0b: Disable 1b: Enable
	23	**Allow Double Buffer Update Disable** Access: R/W This field controls whether double buffer updates are allowed to be disabled for this cursor. The DOUBLE_BUFFER_CTL register can be configured to globally disable double buffer updates for resources that allow them to be disabled. Value / Name

		0b: Not Allowed 1b: Allowed
	22:19	**Reserved** Access: RO Format: MBZ
	18	**Pre CSC Gamma Enable** Access: Double Buffered This bit enables the cursor pre-CSC gamma for the cursor pixel data. This is generally used with HDR to de-gamma the sRGB cursor pixel data before the RGB2020 conversion. 0b: Disable 1b: Enable
	17	**Reserved** Access: RO Format: MBZ
	16	**CSC Enable** Access: Double Buffered This bit enables the cursor color space conversion for the cursor pixel data. Hardware uses the coefficients programmed in the CUR_CSC_COEFF registers to perform the color space conversion. 0b: Disable 1b: Enable
	15	**180 Rotation** Access: Double Buffered This mode causes the cursor image to be rotated 180 degrees. In addition to setting this bit, the cursor position must be adjusted to match the physical orientation of the display. 0b: No rotation 1b: 180 degree rotation **Restriction**

CUR_CTL

		Only 32 bits per pixel cursors can be rotated. This field must be zero when the cursor format is 2 bits per pixel.
	14:12	**Reserved** Access: RO Format: MBZ
	11:10	**Force Alpha Plane Select** Access: Double Buffered This field selects which planes the cursor alpha value will be forced for. It is used together with the Force Alpha Value field. **Value / Name / Description** 00b / Disable / Disable alpha forcing 01b / Pipe CSC Enabled / Enable alpha forcing where cursor overlaps a plane that has enabled pipe CSC 10b / Pipe CSC Disabled / Enable alpha forcing where cursor overlaps plane that has disabled pipe CSC 11b / Reserved / Reserved
	9:8	**Force Alpha Value** Access: Double Buffered This field controls the behavior of cursor when alpha blending onto certain plane pixels. It is used together with the Force Alpha Plane Select field. **Value / Name / Description** 00b / Disable / Cursor pixels alpha blend normally over any plane. 01b / 50 / Cursor pixels with alpha >= 50% are made fully opaque where they overlap the selected plane(s). Cursor pixels with alpha < 50% are made fully transparent where they overlap the selected plane(s). 10b / 75 / Cursor pixels with alpha >= 75% are made fully opaque where they overlap the selected plane(s). Cursor pixels with alpha < 75% are made fully transparent where they overlap the selected plane(s). 11b / 100 / Cursor pixels with alpha = 100% are made fully opaque where they overlap the selected plane(s). Cursor pixels with alpha < 100% are made fully transparent where they overlap the selected plane(s). **Restriction** Force Alpha is only for use with ARGB cursor formats.
	7:6	**Reserved**

CUR_CTL

Access:	RO
Format:	MBZ

5:0 Cursor Mode Select

Access:	Double Buffered

This field selects the cursor mode. Cursor is disabled when the selection is 000000b and enabled when the selection is any other value. The cursor vertical size can be overriden by the size reduction mode.
Color channels should be pre-multiplied with alpha by software.

Value	Name	Description
000000b	Disable	Cursor is disabled
000010b	128x128 32bpp AND/INV	128x128 32bpp AND/INVERT
000011b	256x256 32bpp AND/INV	256x256 32bpp AND/INVERT
000100b	64x64 2bpp 3-color	64x64 2bpp Indexed 3-color and transparency
000101b	64x64 2bpp 2-color	64x64 2bpp Indexed AND/XOR 2-color
000110b	64x64 2bpp 4-color	64x64 2bpp Indexed 4-color
000111b	64x64 32bpp AND/INV	64x64 32bpp AND/INVERT
100010b	128x128 32bpp ARGB	128x128 32bpp ARGB (8:8:8:8 MSB-A:R:G:B)
100011b	256x256 32bpp ARGB	256x256 32bpp ARGB (8:8:8:8 MSB-A:R:G:B)
100100b	64x64 32bpp AND/XOR	64x64 32bpp AND/XOR
100101b	128x128 32bpp AND/XOR	128x128 32bpp AND/XOR
100110b	256x256 32bpp AND/XOR	256x256 32bpp AND/XOR
100111b	64x64 32bpp ARGB	64x64 32bpp ARGB (8:8:8:8 MSB-A:R:G:B)
Others	Reserved	Reserved

Programming Notes

CUR_CTL		
		INVERT, XOR, and alpha blends may not look as expected when the plane underlying the cursor is YUV or extended range RGB. Out of range RGB values will be clamped prior to alpha blending, INVERT, or XOR with cursor. It is recommended to use Force Alpha when cursor is alpha blending onto a plane of a different color space or extended gamut.
		The AND/INVERT format uses the most significant byte (MSB) to control the color. If MSB is 0xFF: Cursor is opaque. Show cursor color from three least significant bytes. If MSB is 0x00: Cursor is transparent. Three least significant bytes must be zero. If MSB is not 0x00 or 0xFF: Cursor inverts the color of the surface underneath.
		The AND/XOR format uses the most significant byte (MSB) to control the color. If MSB is 0xFF: Cursor is opaque. Show cursor color from three least significant bytes. If MSB is 0x00: Cursor is transparent. Three least significant bytes must be zero. If MSB is not 0x00 or 0xFF: The three least significant bytes are XOR'd with the color of the surface underneath.

CUR_FBC_CTL

CUR_FBC_CTL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to CUR_BASE or cursor not enabled
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	700A0h-700A3h
Name:	Cursor FBC Control
ShortName:	CUR_FBC_CTL_A
Reset:	soft
Address:	710A0h-710A3h
Name:	Cursor FBC Control
ShortName:	CUR_FBC_CTL_B
Reset:	soft
Address:	720A0h-720A3h
Name:	Cursor FBC Control
ShortName:	CUR_FBC_CTL_C
Reset:	soft

DWord	Bit	Description
0	31	**Size Reduction Enable** Access: Double Buffered This enables cursor size reduction logic. The cursor engine will fetch and display the programmed reduced number of lines, then go transparent for the rest of the frame. Value / Name: 0b – Disable 1b – Enable **Restriction** Cursor size reduction is not allowed with 2bpp cursor formats or cursor 180-degree rotation. The reduced scan lines field must be programmed with a valid value when cursor size reduction is enabled.

<table>
<tr><th colspan="3">CUR_FBC_CTL</th></tr>
<tr><td></td><td>30:8</td><td>Reserved
<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td></td><td>7:0</td><td>Reduced Scan Lines
<table><tr><td>Access:</td><td>Double Buffered</td></tr></table>This specifies the number of scan lines of cursor data to fetch and display when cursor size reduction is enabled. The value programmed is the size minus one.<table><tr><th>Restriction</th></tr><tr><td>The minimum size is 8 lines, programmed as 07h.The maximum size can not be greater than the normal size when size reduction is not enabled.</td></tr></table></td></tr>
</table>

CUR_PAL

CUR_PAL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled
Address:	70090h-70093h
Name:	Cursor Palette
ShortName:	CUR_PAL_0_A
Reset:	soft
Address:	70094h-70097h
Name:	Cursor Palette
ShortName:	CUR_PAL_1_A
Reset:	soft
Address:	70098h-7009Bh
Name:	Cursor Palette
ShortName:	CUR_PAL_2_A
Reset:	soft
Address:	7009Ch-7009Fh
Name:	Cursor Palette
ShortName:	CUR_PAL_3_A
Reset:	soft
Address:	71090h-71093h
Name:	Cursor Palette
ShortName:	CUR_PAL_0_B
Reset:	soft
Address:	71094h-71097h
Name:	Cursor Palette
ShortName:	CUR_PAL_1_B
Reset:	soft
Address:	71098h-7109Bh
Name:	Cursor Palette
ShortName:	CUR_PAL_2_B
Reset:	soft
Address:	7109Ch-7109Fh
Name:	Cursor Palette

CUR_PAL

ShortName:	CUR_PAL_3_B
Reset:	soft

Address:	72090h-72093h
Name:	Cursor Palette
ShortName:	CUR_PAL_0_C
Reset:	soft

Address:	72094h-72097h
Name:	Cursor Palette
ShortName:	CUR_PAL_1_C
Reset:	soft

Address:	72098h-7209Bh
Name:	Cursor Palette
ShortName:	CUR_PAL_2_C
Reset:	soft

Address:	7209Ch-7209Fh
Name:	Cursor Palette
ShortName:	CUR_PAL_3_C
Reset:	soft

The cursor palette provides color information when using the indexed cursor modes. There are 4 instances of this register format per cursor. The table below describes how the cursor mode and index value will select between the cursor palette colors, AND/XOR, transparency, and destination invert.

Index Value	2 color mode	3 color mode	4 color mode
00	CUR_PAL 0	CUR_PAL 0	CUR_PAL 0
01	CUR_PAL 1	CUR_PAL 1	CUR_PAL 1
10	Transparent	Transparent	CUR_PAL 2
11	Invert Destination	CUR_PAL 3	CUR_PAL 3

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23:16	**Palette Red** Access: Double Buffered This field is the cursor palette red value

CUR_PAL		
	15:8	**Palette Green** Access: Double Buffered This field is the cursor palette green value.
	7:0	**Palette Blue** Access: Double Buffered This field is the cursor palette blue value.

CUR_POS

CUR_POS	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled
Address:	70088h-7008Bh
Name:	Cursor Position
ShortName:	CUR_POS_A
Reset:	soft
Address:	71088h-7108Bh
Name:	Cursor Position
ShortName:	CUR_POS_B
Reset:	soft
Address:	72088h-7208Bh
Name:	Cursor Position
ShortName:	CUR_POS_C
Reset:	soft

This register specifies the screen position of the cursor. The origin of the cursor position is always the upper left corner of the display pipe source image area. When performing 180 degree rotation, the cursor image is rotated by hardware, but the position is not, so it should be adjusted if it is desired to maintain the same apparent position on a physically rotated display.

Restriction
The cursor must have at least a single pixel positioned over the pipe source area. The cursor must not overlap both the left and right sides of the pipe source area.

DWord	Bit	Description
0	31	**Y Position Sign** Access: Double Buffered This specifies the sign of the vertical position of the cursor upper left corner.
	30:29	**Reserved** Access: RO Format: MBZ

CUR_POS		
	28:16	**Y Position Magnitude** Access: Double Buffered This specifies the magnitude of the vertical position of the cursor upper left corner in lines.
	15	**X Position Sign** Access: Double Buffered This specifies the sign of the horizontal position of the cursor upper left corner.
	14:13	**Reserved** Access: RO Format: MBZ
	12:0	**X Position Magnitude** Access: Double Buffered This specifies the magnitude of the horizontal position of the cursor upper left corner in pixels.

CUR_PRE_CSC_GAMC_DATA

CUR_PRE_CSC_GAMC_DATA	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	700B4h-700B7h
Name:	Cursor Pre CSC Gamma Data
ShortName:	CUR_PRE_CSC_GAMMA_DATA_A
Reset:	soft
Address:	710B4h-710B7h
Name:	Cursor Pre CSC Gamma Data
ShortName:	CUR_PRE_CSC_GAMMA_DATA_B
Reset:	soft
Address:	720B4h-720B7h
Name:	Cursor Pre CSC Gamma Data
ShortName:	CUR_PRE_CSC_GAMMA_DATA_C
Reset:	soft

CUR_PRE_CSC_GAMC_INDEX and CUR_PRE_CSC_GAMC_DATA registers are used to program the values that determine the characteristics of the gamma correction for the cursor pixel data before Color Space Conversion. Additional gamma correction can be done after the Color Space Conversion if desired.
The gamma correction curve is represented by specifying a set of gamma entry reference points spaced equally along the curve for values between -1 and 1. For extended values there are extended gamma entry reference points. All input values are clamped to the greater than -7.0 and less than 7.0 range before the gamma calculation.
For input values greater than or equal to 0 and less than 1.0, the input value is used to linearly interpolate between two adjacent points of the first 33 gamma entries to create the result value. The first 32 entries are stored as 16 bits per color in an unsigned 0.16 format with 0 integer and 16 fractional. The 33rd, 34th and 35th entries are stored as 19 bits per color in an unsigned 3.16 format with 3 integer and 16 fractional bits.
For input values greater than or equal to 1.0 and less than 3.0, the input value is used to linearly interpolate between the 33rd and 34th gamma entries to create the result value.
For input values greater than or equal to 3.0 and less than 7.0, the input value is used to linearly interpolate between the 34th and 35th gamma entries to create the result value.
For negative input values, gamma is mirrored along the X-axis, giving the same result as positive input values, except for a negative sign. When gamma input may be negative, the first gamma point should be programmed to a value of 0.0 in order to have a symmetric mirroring.
Pre-CSC Gamma correction gets enabled or disabled based on the "Pre CSC Enable" bit in the CUR_CTL register.

CUR_PRE_CSC_GAMC_DATA

Programming Notes
To program the gamma correction entries, calculate the desired gamma curve for inputs from 0 to 7.0. For inputs of 0 to 1.0, multiply the input value by 32 to find the gamma entry number, then store the desired gamma result in that entry. For inputs greater than 1.0 and less than or equal to 3.0, store the result for an input of 3.0 in the 34th gamma entry. For inputs greater than 3.0 and less than or equal to 7.0, store the result for an input of 7.0 in the 35th gamma entry.

Restriction
The gamma curve must be flat or increasing, never decreasing. The gamma correction registers should only be updated when the plane is off, otherwise screen artifacts may show temporarily.

DWord	Bit	Description
0	31:19	**Reserved** Access: RO Format: MBZ
	18:0	**Gamma Value** Default Value: 0000000000000000000b Access: R/W Format: U3.16

CUR_PRE_CSC_GAMC_INDEX

CUR_PRE_CSC_GAMC_INDEX

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	700B0h-700B3h
Name:	Cursor Pre CSC Gamma Index
ShortName:	CUR_PRE_CSC_GAMMA_INDEX_A
Reset:	soft
Address:	710B0h-710B3h
Name:	Cursor Pre CSC Gamma Index
ShortName:	CUR_PRE_CSC_GAMMA_INDEX_B
Reset:	soft
Address:	720B0h-720B3h
Name:	Cursor Pre CSC Gamma Index
ShortName:	CUR_PRE_CSC_GAMMA_INDEX_C
Reset:	soft

DWord	Bit	Description
0	31:11	**Reserved** Access: RO Format: MBZ
	10	**Index Auto Increment** Access: R/W This field enables the index auto increment. Value / Name / Description 0b / No Increment / Do not automatically increment the index value. 1b / Auto Increment **[Default]** / Increment the index value with each read or write to the data register.
	9:6	**Reserved** Access: RO Format: MBZ

<table>
<tr><th colspan="3">CUR_PRE_CSC_GAMC_INDEX</th></tr>
<tr><td></td><td>5:0</td><td>Index Value

<table><tr><td>Access:</td><td>Write/Read Status</td></tr></table>This index controls access to the array of pipe pre color space conversion gamma values. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set.
When automatically incrementing, the index will roll over to 0 after writing or reading the entire allowed range.
While in auto increment mode, after performing reads or writes to only part of the range, the auto increment bit must be cleared before resetting the index value.<table><tr><th>Value</th><th>Name</th></tr><tr><td>[0,34]</td><td></td></tr></table></td></tr>
</table>

CUR_SURFLIVE

CUR_SURFLIVE	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	700ACh-700AFh
Name:	Cursor Live Base Address
ShortName:	CUR_SURFLIVE_A
Reset:	soft
Address:	710ACh-710AFh
Name:	Cursor Live Base Address
ShortName:	CUR_SURFLIVE_B
Reset:	soft
Address:	720ACh-720AFh
Name:	Cursor Live Base Address
ShortName:	CUR_SURFLIVE_C
Reset:	soft
There is one instance of this register for each pipe.	

DWord	Bit	Description
0	31:12	**Live Surface Base Address** Access: RO This gives the live value of the surface base address as being currently used for the cursor.
	11:0	**Reserved** Access: RO Format: MBZ

DE_FUSA_IOSF_PARITY_CNTRL

DE_FUSA_IOSF_PARITY_CNTRL - DE_FUSA_IOSF_PARITY_CNTRL

Register Space: MMIO: 0/2/0
Size (in bits): 32
SOC_Consumer: BIOS

Address: 100140h

This register controls the parity generation, checking, and error insertion logic in the DE IOSF endpoints: PSF 0 and PSF DIP

DWord	Bit	Description
0	31:29	**Reserved** Access: RO Format: MBZ
	28	**Reserved** Access: RO Format: MBZ
	27:22	**Reserved** Access: RO Format: MBZ
	21:20	**Reserved** Access: RO Format: MBZ
	19:14	**Reserved** Access: RO Format: MBZ
	13	**PSF 0 Cmd Parity Gen Dis** Default Value: 0h Access: R/W _Custom_GTIReset: BUS When 1 command parity generation is disabled

DE_FUSA_IOSF_PARITY_CNTRL - DE_FUSA_IOSF_PARITY_CNTRL

	12	**PSF 0 Data Parity Gen Dis** Default Value: 0h Access: R/W _Custom_GTIReset: BUS When 1 data parity generation is disabled
	11:10	**Reserved** Access: RO Format: MBZ
	9	**PSF 0 Cmd Parity Chk En** Default Value: 0h Access: R/W _Custom_GTIReset: BUS When 1 checking of command parity is enabled
	8	**PSF 0 Data Parity Chk En** Default Value: 0h Access: R/W _Custom_GTIReset: BUS When 1 checking of data parity is enabled
	7	**Reserved** Access: RO Format: MBZ
	6	**PSF 0 Cmd Parity Err Inj** Default Value: 0h Access: R/W _Custom_GTIReset: BUS 0: No error injection 1: Invert mcparity Once set the next command mcparity is corrupted and then the bit is cleared by HW.

DE_FUSA_IOSF_PARITY_CNTRL - DE_FUSA_IOSF_PARITY_CNTRL

	5:4	**PSF 0 Data Parity Error Inj** Default Value: 0h Access: R/W _Custom_GTIReset: BUS 00: No error injected 01:Invert mdparity[0] 10:Invert mdparity[1] 11: Invert mdparity[1:0] Once set the next command with data is corrupted and then the bit is cleared by HW. Note: mdparity[1] is only present for IOSF data widths of 512
	3:1	**Reserved** Access: RO Format: MBZ
	0	**DE_FUSA_IOSF_PARITY_CNTRL_LOCK** Default Value: 000b _Custom_GTIReset: BUS Writing 1 to this bit will lock the register from further updates

DE_PIPE_INTERRUPT

DE_PIPE_INTERRUPT	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	44400h-4440Fh
Name:	Display Engine Pipe A Interrupts
ShortName:	DE_PIPE_INTERRUPT_A
Reset:	soft
Address:	44410h-4441Fh
Name:	Display Engine Pipe B Interrupts
ShortName:	DE_PIPE_INTERRUPT_B
Reset:	soft
Address:	44420h-4442Fh
Name:	Display Engine Pipe C Interrupts
ShortName:	DE_PIPE_INTERRUPT_C
Reset:	soft

This table indicates which events are mapped to each bit of the Display Engine Pipe Interrupt registers. The IER enabled Display Engine Pipe Interrupt IIR (sticky) bits are ORed together to generate the DE_Pipe Interrupts Pending bit in the next level up interrupt registers. There is one full set of Display Engine Pipe interrupts per display pipe. The STEREO3D_EVENT_MASK selects between left eye and right eye reporting of vertical blank, vertical sync, and scanline events in stereo 3D modes.

0x44400 = ISR A, 0x44410 = ISR B, 0x44420 = ISR C, 0x44430 = ISR D
0x44404 = IMR A, 0x44414 = IMR B, 0x44424 = IMR C, 0x44434 = IMR D
0x44408 = IIR A, 0x44418 = IIR B, 0x44428 = IIR C, 0x44438 = IIR D
0x4440C = IER A, 0x4441C = IER B, 0x4442C = IER C, 0x4443C = IER D

DWord	Bit	Description
0	31	**Underrun** **Description** The ISR is an active high pulse when there is an underrun on the transcoder attached to this pipe.
	30	**VRR Double Buffer Update** The ISR is an active high pulse on the eDP/DP Variable Refresh Rate double buffer update event on this pipe.
	29	**Reserved**
	28	**Reserved**

DE_PIPE_INTERRUPT

27	**Reserved** Access: RO Format: MBZ
26	**PIPEDMC_Interrupt** The ISR is an active high pulse when the PIPE DMC has an interrupt.
25	**PIPEDMC_gtt_fault_status** The ISR is an active high pulse when the PIPE DMC gtt fault occurs.
24	**Unused_Int_24** These interrupts are currently unused.
23	**LACE Fast Access Interrupt** The ISR is an active high level indicating an interrupt is set in DPLC_FA_STATUS.
22:21	**Reserved** Access: RO Format: MBZ
20	**Plane5_GTT_Fault_Status** Description The ISR is an active high pulse when a GTT fault is detected for plane 5 on this pipe.
19	**Vblank unmodified** The ISR is an active high level for the duration of the vertical blank of the transcoder attached to this pipe, the unmodified vertical blank, as opposed to the modified vertical blank that the pipe units use. The transcoder vertical blank always begins at the end of transcoder vertical active (unmodified). When the transcoder vertical blank start is programmed later than transcoder vertical active, the pipe vertical blank will start later than the transcoder vertical blank (modified).
18:17	**Reserved** Access: RO Format: MBZ
16	**Plane5_Flip_Done** The ISR is an active high pulse when the flip is done for plane 5 on this pipe.
15	**DSB_2_Interrupt** The ISR is an active high pulse when there is interrupt from DSB 2. SW must read the DSB interrupt registers to check what is caused interrupt in DSB.

DE_PIPE_INTERRUPT		
	14	**DSB_1_Interrupt** The ISR is an active high pulse when there is interrupt from DSB 1. SW must read the DSB interrupt registers to check what is caused interrupt in DSB..
	13	**DSB_0_Interrupt** The ISR is an active high pulse when there is interrupt from DSB 0. SW must read the DSB interrupt registers to check what is caused interrupt in DSB..
	12	**DPST_Histogram_event** The ISR is an active high pulse on the DPST Histogram event on this pipe.
	11	**Cursor_GTT_Fault_Status** **Description** The ISR is an active high pulse when a GTT fault is detected for the cursor on this pipe.
	10	**Plane4_GTT_Fault_Status** **Description** The ISR is an active high pulse when a GTT fault is detected for plane 4 on this pipe.
	9	**Plane3_GTT_Fault_Status** **Description** The ISR is an active high pulse when a GTT fault is detected for plane 3 on this pipe.
	8	**Plane2_GTT_Fault_Status** **Description** The ISR is an active high pulse when a GTT fault is detected for plane 2 on this pipe.
	7	**Plane1_GTT_Fault_Status** **Description** The ISR is an active high pulse when a GTT fault is detected for plane 1 on this pipe.
	6	**Plane4_Flip_Done** The ISR is an active high pulse when the flip is done for plane 4 on this pipe.
	5	**Plane3_Flip_Done** The ISR is an active high pulse when the flip is done for plane 3 on this pipe.
	4	**Plane2_Flip_Done** The ISR is an active high pulse when the flip is done for plane 2 on this pipe.

DE_PIPE_INTERRUPT		
	3	**Plane1_Flip_Done** The ISR is an active high pulse when the flip is done for plane 1 on this pipe.
	2	**Scan_Line_Event** The ISR is an active high pulse on the scan line event of the transcoder attached to this pipe.
	1	**Vsync** The ISR is an active high level for the duration of the vertical sync of the transcoder attached to this pipe.
	0	**Vblank** **Description** The ISR is an active high level for the duration of the vertical blank of the transcoder attached to this pipe. This represents the vertical blank observed by units within the pipe and used for updating double-buffered registers in the pipe. The transcoder vertical blank always begins at the end of transcoder vertical active (unmodified). When the transcoder vertical blank start is programmed later than transcoder vertical active, the pipe vertical blank will start later than the transcoder vertical blank (modified).

DE_POWER1

DE_POWER1	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	42400h-42403h
Name:	Display Engine Power 1
ShortName:	DE_POWER1
Reset:	global

DWord	Bit	Description
0	31	**Power Well 3 State** Access: RO This field indicates the status of display power well 3. Value / Name: 0b – Off 1b – On
	30	**Display Pipes Enabled** Access: RO This field indicates if any display pipes are enabled. Value / Name / Description: 0b – Disabled – All display pipes disabled 1b – Enabled – One or more display pipes enabled
	29	**Reserved** Access: RO Format: MBZ
	28	**Power Well 1 State** Access: RO This field indicates the status of display power well 1. Value / Name: 0b – Off 1b – On

DE_POWER1

	27:26	**SRD Status** Access: RO This field indicates the live status of the SRD link on transcoder A. Value / Name / Description: 00b / Full Off / Link is fully off. DDI lanes are disabled, and most memory reads are disabled. 01b / Full On / Link is fully on. Normal operation. 11b / Reserved / Reserved
	25	**KVM Session Status** Access: RO This field indicates the status of KVM session. Value / Name / Description: 0b / Disabled / KVM session disabled 1b / Enabled / KVM session enabled
	24:20	**Transmit Lanes Enabled** Access: RO The total number of DDI lanes enabled.
	19:14	**Reserved** Access: RO Format: MBZ
	13:10	**Enabled Pipe Scalers** Access: RO Indicates total usage of the Scaler EBBs.
	9:8	**Enabled DEPLLs** Access: RO The total number of display CCU PLLs enabled.
	7	**Reserved** Access: RO Format: MBZ
	6:4	**Reserved** Access: RO Format: MBZ

DE_POWER1		
	3	**Enabled CDPLLs** Access: RO Indicates if CD PLL is enabled.
	2:0	**Enabled MGPLLs** Access: RO The total number of type-C PLLs enabled by display.

DE_RR_DEST

DE_RR_DEST	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	44058h-4405Bh
Name:	Render Response Destination
ShortName:	DE_RR_DEST
Reset:	soft

This register selects the destination of certain render responses that may go to CS, BCS, or both. In order for a response to be sent to a particular destination, the event most occur, the event must be unmasked, and that destination must be selected.

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: MBZ
	7:6	**Reserved** Access: RO Format: MBZ
	5:4	**Pipe C Vertical Blank Destination** Access: R/W This field selects the destination for the render response sent on pipe C start of vertical blank. Value: 00b — Name: CS Value: 01b — Name: BCS Value: 10b,11b — Name: Both CS and BCS
	3:2	**Pipe B Vertical Blank Destination** Access: R/W This field selects the destination for the render response sent on pipe B start of vertical blank. Value: 00b — Name: CS Value: 01b — Name: BCS Value: 10b,11b — Name: Both CS and BCS

DE_RR_DEST

	1:0	**Pipe A Vertical Blank Destination** Access: R/W This field selects the destination for the render response sent on pipe A start of vertical blank.

Value	Name
00b	CS
01b	BCS
10b,11b	Both CS and BCS

Device 0 Capabilities A

CAPID0_A_0_0_0_PCI - Device 0 Capabilities A

Register Space:	PCI: 0/0/0
Source:	BSpec
Size (in bits):	32
Address:	000E4h

DWord	Bit	Description
0	31	**Display HD Audio Disable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	30	**PEG12 Disable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	29	**PEG11 Disable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	28	**PEG10 Disable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	27	**PCI Express Link Width Upconfig Disable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project

CAPID0_A_0_0_0_PCI - Device 0 Capabilities A

	26	**DMI Width** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	25	**ECC Disable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	24	**Force DRAM ECC Enabled** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	23	**VTd Disable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS 0: Enable VTd 1: Disable VTd
	22	**DMI Gen 2 Disable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	21	**PEG Gen 2 Disable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project

CAPID0_A_0_0_0_PCI - Device 0 Capabilities A

	20:19	**DDR Size** Default Value: 00b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	18	**Bclk overclocking disable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	17	**Disable 1N Mode** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	16	**Full ULT Fuse Read Disable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	15	**Camarillo Device Disable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS 0: DPTF (Camarillo) associated memory spaces are accessible. 1: DPTF (Camarillo) associated memory and IO spaces are disabled. DEVEN_0_0_0_PCI field for DPTF cannot be set.
	14	**2 DIMMS per Channel Disable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project

CAPID0_A_0_0_0_PCI - Device 0 Capabilities A

	13	**X2APIC Enabled** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	12	**Performance Dual Channel Disable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	11	**Internal Graphics Disable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS 0b: There is a graphics engine within this CPU. Internal Graphics Device (Device 2) is enabled, and all of its memory and I/O spaces are accessible. Configuration cycles to Device 2 will be completed within the CPU. All non-SMM memory and IO accesses to VGA will be handled based on Memory and IO enables of Device 2 and IO registers within Device 2 and VGA Enable of the PCI to PCI bridge control (If PCI Express GFX attach is supported). A selected amount of Graphics Memory space is pre-allocated from the main memory based on Graphics Mode Select (GMS in the GGC Register). Graphics Memory is pre-allocated above TSEG Memory. 1b: There is no graphics engine within this CPU. Internal Graphics Device (Device 2) and all of its memory and I/O functions are disabled. Configuration cycle targeted to Device 2 will be passed on. All non-SMM memory and IO accesses to VGA will be handled based on VGA Enable of the PCI to PCI bridge control. Device 2 is disabled and hidden.
	10	**Reserved**
	9:8	**Capability Device ID** Default Value: 00b Access: R/W _Custom_GTIReset: BUS
	7:4	**Compatibility Rev ID** Default Value: 0000b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project

CAPID0_A_0_0_0_PCI - Device 0 Capabilities A

	3	**DDR Overclocking** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	2	**IA Overclocking Enabled by DSKU** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	1	**DDR Write VRef Enable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	0	**DDR3L Enable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project

Device 0 Capabilities B

CAPID0_B_0_0_0_PCI - Device 0 Capabilities B

Register Space:	PCI: 0/0/0
Source:	BSpec
Size (in bits):	32
Address:	000E8h

DWord	Bit	Description
0	31	**Reserved_31** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	30	**IA Overclocking DSKU Control Disable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	29	**IA Overclocking Enable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	28	**SMT Capability** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	27:25	**Cache Size Capability** Default Value: 000b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project

CAPID0_B_0_0_0_PCI - Device 0 Capabilities B

	24	**SVMDIS** Access: R/W _Custom_GTIReset: BUS Value: 0b — Name: SVM mode enabled **[Default]** Value: 1b — Name: SVM mode disabled
	23:21	**DDR3 Maximum Frequency Capability with 100 Memory** Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	20	**Gen3 Disable Fuse for PCIe PEG Controllers** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	19	**Package Type** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	18	**Additive Graphics Enabled** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	17	**Additive Graphics Capable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project

CAPID0_B_0_0_0_PCI - Device 0 Capabilities B

	16	**Primary PEG Port x16 Disable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	15:12	**Reserved_15_12** Default Value: 0000b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	11	**Reserved**
	10:8	**Reserved_10_8** Default Value: 000b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	7	**Reserved**
	6	**DEVICE10_DIS** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	5	**DEVICE11F1_DIS** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	4	**DEVICE11F0_DIS** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project

CAPID0_B_0_0_0_PCI - Device 0 Capabilities B

	3	**Reserved_3** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	2	**DDR4 DSKU Enable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	1	**Dual PEG Force x1 when VGA Enabled** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project
	0	**Single PEG Force x1 when VGA Enabled** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Unused - Bit field not relevant for the current project

DFSM

DFSM

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	51000h-51003h
Name:	Display Fuse
ShortName:	DFSM
Reset:	global

This register contains fuse and strap settings for display. This register is not reset by FLR.

DWord	Bit	Description
0	31	**Reserved** Access: R/W
	30	**Display PipeA Disable** Access: R/W This bit indicates whether the display pipe A (first pipe) capability is disabled. 0b – Enable – Pipe A Capability Enabled 1b – Disable – Pipe A Capability Disabled
	29	**Reserved** Access: R/W
	28	**Display PipeC Disable** Access: R/W This bit indicates whether the display pipe C (third pipe) capability is disabled. 0b – Enable – Pipe C Capability Enabled 1b – Disable – Pipe C Capability Disabled
	27	**Display PM Disable** Access: R/W This bit indicates whether the display power management FBC and DPST capabilities are disabled. 0b – Enable – PM Capability Enabled 1b – Disable – PM Capability Disabled

DFSM

26 Display eDP Disable

Access:	R/W

Description
This fuse indicates that all combo PHY ports are disabled by the SoC and cannot be used.

Value	Name	Description
0b	Enable	eDP Capability Enabled
1b	Disable	eDP Capability Disabled

25 Reserved

Access:	R/W

24 Reserved

Access:	R/W

23 Reserved

Access:	R/W

22 Display PipeD Disable

Access:	R/W

Description
This bit indicates whether the display pipe D (fourth pipe) capability is disabled.
This fuse is treated as a SPARE. There is no Pipe D.

Value	Name
0b	Enable
1b	Disable

21 Display PipeB Disable

Access:	R/W

This bit indicates whether the display pipe B (second pipe) capability is disabled.

Value	Name
0b	Pipe B Capability Enabled
1b	Pipe B Capability Disabled

DFSM

20 — Display WD Disable

Access:	R/W

This bit indicates whether the display WD capability is disabled.

Value	Name	Description
0b	Enable	WD Capability Enabled
1b	Disable	WD Capability Disabled

19 — Reserved

Access:	R/W

18 — Reserved

Access:	R/W

17 — Reserved

Access:	R/W

16 — Isolated Decode Disable

Access:	R/W

This field indicates whether the Isolated Decode feature is disabled.

Value	Name
0b	Isolated Decode Capability Enabled
1b	Isolated Decode Capability Disabled

15:8 — Audio Codec ID

Access:	R/W

This field indicates the lower 8 bits of the audio codec device ID. See the root node F00 verb for the device IDs on each project.

Value	Name	Description
0Bh	Audio Codec ID 280Bh **[Default]**	Default value is N/A. Fuse download will override with correct value for this project.

7 — Display DSC Disable

Access:	R/W

This field indicates whether the DSC (port Display Stream Compression) feature is disabled.

Value	Name
0b	DSC Capability Enabled
1b	DSC Capability Disabled

	6	**Display RSB Enable** Access: R/W This bit indicates whether the remote screen blanking feature is enabled in the display engine. Value / Name / Description 0b / Disable / RSB Capability Disabled 1b / Enable / RSB Capability Enabled
	5	**Reserved** Access: R/W
	4	**Reserved** Access: R/W
	3	**Reserved** Access: R/W
	2	**Reserved** Access: R/W
	1	**Reserved** Access: R/W
	0	**Display Audio Codec Disable** Access: R/W This bit indicates whether the display audio codec capability is disabled. Value / Name / Description 0b / Enable / Audio Codec Capability Enabled 1b / Disable / Audio Codec Capability Disabled

DISPLAY_INT_CTL

DISPLAY_INT_CTL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	44200h-44203h
Name:	Display Interrupt Control
ShortName:	DISPLAY_INT_CTL
Reset:	soft

This register has the primary enable for display interrupts and gives an overview of what interrupts are pending.
An interrupt pending bit will read 1b while one or more interrupts of that category are set (IIR) and enabled (IER).
All Pending Interrupts are ORed together to generate the combined interrupt.
The combined interrupt is ANDed with the Display Interrupt enable to create the display enabled interrupt.
The display enabled interrupt goes to graphics interrupt processing.

DWord	Bit	Description
0	31	**Display Interrupt Enable** Access: R/W This is the ultimate control for display interrupts. This must be enabled for any of these interrupts to propagate to graphics interrupt processing. 0b: Disable 1b: Enable
	30:25	**Reserved** Access: RO Format: MBZ
	24	**Audio Codec Interrupts Pending** Access: RO This field indicates if audio codec interrupts are pending.
	23	**DE PCH Interrupts Pending** Access: RO This field indicates if South (PCH) display interrupts are pending. The South Display interrupt is configured through the SDE interrupt registers.
	22	**DE Misc Interrupts Pending** Access: RO This field indicates if DE Misc interrupts are pending.

DISPLAY_INT_CTL		
	21	**DE HPD Interrupts Pending** Access: RO This field indicates if North DE HPD interrupts are pending.
	20	**DE Port Interrupts Pending** Access: RO This field indicates if Port interrupts are pending.
	19	**Reserved** Access: RO Format: MBZ
	18	**DE Pipe C Interrupts Pending** Access: RO This field indicates if Pipe C interrupts are pending.
	17	**DE Pipe B Interrupts Pending** Access: RO This field indicates if Pipe B interrupts are pending.
	16	**DE Pipe A Interrupts Pending** Access: RO This field indicates if Pipe A interrupts are pending.
	15:0	**Reserved** Access: RO Format: MBZ

DKLP_ACU_ACU_DWORD21

DKLP_ACU_ACU_DWORD21		
Register Space: MMIO: 0/2/0 Size (in bits): 32		
Display Controller is using this register for compliance in DP Mode.		
DWord	**Bit**	**Description**
0	31:26	**Reserved** Access: R/W
	25:18	**Modifications** Access: R/W
	17	**Set Modifications** Access: R/W
	16:13	**Preset** Access: R/W
	12:9	**Pattern** Access: R/W PRBS and Square wave pattern selection Note that only square wave patterns are to be selected from this field.

Value	Name
0000b	PRBS31 **[Default]**
0001b	PRBS15
0010b	PRBS9
0011b	PRBS7
0100b	SQ2 pattern
0101b	SQ4 pattern
0110b	SQ32 pattern
0111b	SQ128 pattern
1111b	SLOS1

DKLP_ACU_ACU_DWORD21

	8:6	**Adapter** Access: R/W Lane selection **Value** / **Name** 000b: lane0 **[Default]** 001b: lane1 111b: All lanes
	5:0	**Port** Access: R/W Reserved

DKLP_ACU_ACU_DWORD22

DKLP_ACU_ACU_DWORD22		
Register Space: MMIO: 0/2/0 Size (in bits): 32		
USB4 Port Ops cmd metadata		
DWord	**Bit**	**Description**
0	31:24	**port_ops_cmd_metadata3** Default Value: 00h port_ops_cmd_metadata3_defaultreset Access: R/W cmd metadata byte 3
	23:16	**port_ops_cmd_metadata2** Default Value: 00h port_ops_cmd_metadata2_defaultreset Access: R/W cmd metadata byte 2
	15:8	**port_ops_cmd_metadata1** Default Value: 00h port_ops_cmd_metadata1_defaultreset Access: R/W cmd metadata byte 1
	7:0	**port_ops_cmd_metadata0** Default Value: 00h port_ops_cmd_metadata0_defaultreset Access: R/W cmd metadata byte 0

DKLP_CMN_DIG_CMN_DIG_DWORD8

DKLP_CMN_DIG_CMN_DIG_DWORD8		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
MISC_SUS0		
DWord	**Bit**	**Description**
0	31	**os_cfg_dig_superset_gaon** Default Value: 0b os_cfg_dig_superset_gaon_defaultreset Access: R/W Power well:SUS
	30	**os_cri_imblbiasen** Default Value: 1b os_cri_imblbiasen_defaultreset Access: R/W CMN_DIG::cmn_dig_dwo d6::os_c i_im l biasen
	29	**os_cfg_dis_firstcomp_mask_for_pok** Default Value: 0b os_cfg_dis_firstcomp_mask_for_pok_defaultreset Access: R/W CMN_DIG::cmn_dig_dwo d6::os_cfg_dis_fi stcom _mask_fo _ ok
	28:26	**os_cfg_imb750select** Default Value: 010b cfg_os_cfg_imb750select_defaultreset Access: R/W Power well:SUS
	25:24	**os_cfg_imbcompsel_2** Default Value: 00b cfg_os_cfg_imbcompsel_2_defaultreset Access: R/W CMN_DIG::cmn_dig_dwo d6::os_cfg_imbcompsel_2
	23	**os_cfg_imbcompsel** Default Value: 1b cfg_os_cfg_imbcompsel_defaultreset Access: R/W Power well:SUS

DKLP_CMN_DIG_CMN_DIG_DWORD8

	22	**os_cfg_ircomp_ovrd_value** Default Value: 0b cfg_os_cfg_ircomp_ovrd_value_defaultreset Access: R/W Power well:SUS
	21	**os_cfg_ircomp_ovrd_en** Default Value: 0b cfg_os_cfg_ircomp_ovrd_en_defaultreset Access: R/W Power well:SUS
	20	**os_cfg_invert_ptrim_ircomp_h** Default Value: 0b cfg_os_cfg_invert_ptrim_ircomp_h_defaultreset Access: R/W Power well:SUS
	19	**os_cfg_invert_ntrim_ircomp_h** Default Value: 0b cfg_os_cfg_invert_ntrim_ircomp_h_defaultreset Access: R/W Power well:SUS
	18	**os_cfg_invert_ptrim_h** Default Value: 0b cfg_os_cfg_invert_ptrim_h_defaultreset Access: R/W Power Well:SUS
	17	**os_cfg_invert_ntrim_h** Default Value: 0b cfg_os_cfg_invert_ntrim_h_defaultreset Access: R/W Power well:SUS
	16	**os_cfg_invert_ircomp_h** Default Value: 0b os_cfg_invert_ircomp_h_defaultreset Access: R/W Power well:SUS

DKLP_CMN_DIG_CMN_DIG_DWORD8

	15:14	**os_susclk_dynclkgate_mode_1_0** Default Value: 00b cfg_os_susclk_dynclkgate_mode_1_0_defaultreset Access: R/W Dynamic Susclk Gating Model Select 00: Susclk gating and CLKREQ Forced High. In this mode the susclk will not be gated under any circumstances and the CLKREQ sent to the SOC will be statically forced high. (default) 01: Susclk gating disabled, CLKREQ enabled. In this mode the susclk will not be gated under any circumstances. The CLKREQ sent to the SOC will toggle ased on whether the susclk is needed by the MPHY 10: Susclk gating enabled, CLKREQ disabled (Forced High). In this mode the susclk will be gated during PS3-PS7 when no functions are requesting the susclk. The CLRKEQ sent to the SOC will be statically forced high. 11: Susclk gating and CLKREQ enabled (POR Mode). In this mode the susclk will be gated during PS3-PS7 when no functions are requesting the susclk. The CLKREQ sent to the SOC will toggle based on whether the susclk is needed by the MPHY.
	13	**os_cfg_calclk_srcsel** Default Value: 0b cfg_os_cfg_calclk_srcsel_defaultreset Access: R/W oa_ck_ xcalclk (Hardcoded to zero always)
	12	**os_cfg_tr2pwr_gating_ctrl** Default Value: 0b cfg_os_cfg_tr2pwr_gating_ctrl_defaultreset Access: R/W Dynamic TR2 Power Gating Control Enable[ ] When asserted the dynamic power gating is enabled in the common logic. Default it is disable dynamic power gating. IOM could override these registers.
	11	**os_cfg_cl2pwr_gating_ctrl** Default Value: 0b cfg_os_cfg_cl2pwr_gating_ctrl_defaultreset Access: R/W Dynamic CL2 Power Gating Control Enable When asserted the dynamic power gating is enabled in the common logic. Default it is disable dynamic power gating. IOM could override these registers.
	10	**os_cfg_gaonpwr_gating_ctrl** Default Value: 0b cfg_os_cfg_gaonpwr_gating_ctrl_defaultreset Access: R/W Dynamic gated AON Power Gating Control Enable When asserted the dynamic power gating is enabled in the common logic. Default it is disable dynamic power gating. IOM could override these registers.

DKLP_CMN_DIG_CMN_DIG_DWORD8

	9	**os_cfg_cl2pwr_pll1en_gating_ctrl** Default Value: 1b cfg_os_cfg_cl2pwr_pll1en_gating_ctrl_defaultreset Access: R/W When enabled CL2 pwr will not turn off if pll1 is enabled. When disabled CL2 will ignore pll1 enable.
	8	**cfg_calclkgate_dis** Default Value: 0b cfg_cfg_calclkgate_dis_defaultreset Access: R/W 0 - enable cal clock gating 1 - disable cal clock gating
	7	**os_cfg_trpwr_gating_ctrl** Default Value: 0b cfg_os_cfg_trpwr_gating_ctrl_defaultreset Access: R/W Dynamic TR Power Gating Control Enable When asserted the dynamic power gating is enabled in the common logic. Default it is disable dynamic power gating. IOM could override these registers.
	6	**os_cfg_cl1pwr_gating_ctrl** Default Value: 0b cfg_os_cfg_cl1pwr_gating_ctrl_defaultreset Access: R/W Dynamic CL1 Power Gating Control Enable When asserted the dynamic power gating is enabled in the common logic. Default it is disable dynamic power gating. IOM could override these registers.
	5	**os_cfg_dgpwr_gating_ctrl** Default Value: 0b cfg_os_cfg_dgpwr_gating_ctrl_defaultreset Access: R/W Dynamic DG Power Gating Control Enable When asserted the dynamic power gating is enabled in the common logic. Default it is disable dynamic power gating. IOM could override these registers.
	4:0	**os_cfg_susclk_delay_5_1** Default Value: 10h cfg_os_cfg_susclk_delay_5_1_defaultreset Access: R/W Susclk Gating Cycle Delay Time When dynamic susclk gating is enabled. When all susclk requests are deasserted, this is the number of susclk cycles that the susclk will remain active before gating.

DKLP_PCS_PCS_DWORD5

DKLP_PCS_PCS_DWORD5	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	168C04h-168C07h
Name:	DKLP_PCS_PCS_DWORD5
ShortName:	DKLP_PCS_PCS_DWORD5
Reset:	global

DWord	Bit	Description
0	31:28	**cri_rxpwrfsm_rxsqshunt_timer** Default Value: 1h cri_rxpwrfsm_rxsqshunt_timer_defaultreset Access: R/W Number of sus clocks fo rx shunt pulse width. Default is 1 sus clock (40 ns)
	27:24	**cri_rxpwrfsm_timer_rx_sqen_lo** Default Value: 1h cri_rxpwrfsm_timer_rx_sqen_lo_defaultreset Access: R/W Number of sus clocks for squelch turn-on when already in PS0, PS1, or PS6. Goal is to have at least 100ns of delay
	23:16	**cri_rxpwrfsm_timer_rx_sqen_hi** Default Value: 00h cri_rxpwrfsm_timer_rx_sqen_hi_defaultreset Access: R/W Number of sus clocks for powering up squelch fsm when coming from reset or PS3 - PS5 power state. Goal is to have at least 650ns of delay
	15	**cri_disable_ps1_sus_hndshk** Default Value: 0b cri_disable_ps1_sus_hndshk_defaultreset Access: R/W When set, disables the susclk handshake for Power Down transitions into and out of PS1.
	14	**cri_disable_tx_ps1_fastmode** Default Value: 0b cri_disable_tx_ps1_fastmode_defaultreset Access: R/W When this register is 0, the PCS will allow TxPower State transitions to flow on AMI without waiting for the Rx as long as the RxPower State is already at the same value. This would result in a latency speedup if the Rx is in PS1 (RxStandby) and a Power Down request is made for PS1.

DKLP_PCS_PCS_DWORD5

	13	**cri_disable_ps3_ps0_usb3_tx_only_init** Default Value: 0b cri_disable_ps3_ps0_usb3_tx_only_init_defaultreset Access: R/W Setting this register will require both Tx and Rx subsystems to be ready prior to the PhyStatus return. The default behavior is that PhyStatus will be returned based only on Tx. This register is only applicable for USB3. For all other PhyModes, both Tx and Rx responses are needed to acknowledge this state transition. 0: PS3->PS0 INIT_DONE PhyStatus acknowledgement based on TX_READY 1: PS3->PS0 INIT_DONE PhyStatus acknowledgement based on TX_READY and RX_READY
	12	**cri_disable_ps0_ps1_usb3_fastmode** Default Value: 0b cri_disable_ps0_ps1_usb3_fastmode_defaultreset Access: R/W Setting this register disables the shortened handshake time between PCLK and SUSCLK for USB3 PS1 entries. 0: Use shortened handshake 1: Use full handshake
	11	**reg_core_softreset_en** Default Value: 0b reg_core_softreset_en_defaultreset Access: R/W Enable soft reset for PCLK domain
	10	**reg_core_softreset** Default Value: 1b reg_core_softreset_defaultreset Access: R/W Set low to reset PCLK domain, set high to leave reset
	9	**cri_disable_ps1_ps0_usb3_tx_only** Default Value: 0b cri_disable_ps1_ps0_usb3_tx_only_defaultreset Access: R/W Setting this register will require both Tx and Rx sub systems to be ready prior to the PhyStatus return. The default behavior is that PhyStatus will be returned based only on Tx. This register is only applicable for USB3. For all other PhyModes, both Tx and Rx responses are needed to acknowledge this state transition. 0: PS1->PS0 PhyStatus acknowledgement based on TX_READY 1: PS1-]PS0 PhyStatus acknowledgement based on TX_READY and RX_READY

DKLP_PCS_PCS_DWORD5

	8	**cri_disable_ps2_ps0_usb3_tx_only** Default Value: 1b cri_disable_ps2_ps0_usb3_tx_only_defaultreset Access: R/W Setting this register will require both Tx and Rx sub systems to be ready prior to the PhyStatus return. The default behavior is that PhyStatus will be returned based only on Tx. This register is only applicable for USB3. For all other PhyModes, both Tx and Rx responses are needed to acknowledge this state transition. 0: PS2->PS0 PhyStatus acknowledgement based on TX_READY 1: PS2->PS0 PhyStatus acknowledgement based on TX_READY and RX_READY
	7	**cri_disable_pcie3_int_eqtrain** Default Value: 0b cri_disable_pcie3_int_eqtrain_defaultreset Access: R/W Setting this register will prevent the PHY from autonomously generating an RxEqTrain operation when entering PCIe Gen3.
	6	**cri_disable_ps3_ps0_usb3_tx_only** Default Value: 0b cri_disable_ps3_ps0_usb3_tx_only_defaultreset Access: R/W Setting this register will require both a TX_READY and a RX_READY before setting PhyStatus for a PS3->PS0 transition in USB3 mode.
	5	**cri_rxeb_eiosenable** Default Value: 0b cri_rxeb_eiosenable_defaultreset Access: R/W When 1 enables EIOS based Rx power down (Set to 0 to disable Auto RX off feature)
	4	**cri_rxdigfiltsq_enable** Default Value: 1b cri_rxdigfiltsq_enable_defaultreset Access: R/W When 1 enables unsquelch based Rx power up in P0 or P0s
	3	**cri_disable_sq_eqtrain** Default Value: 0b cri_disable_sq_eqtrain_defaultreset Access: R/W Disables waiting for unsquelch from the Rx before starting an internal RxEqTrain for a PCIe Gen3 speed change. Only applicable if cri_disable_pcie3_int_eqtrain is 1'b0. 0: Wait for unsquelch before starting an RxEqTrain 1: Do not wait for unsquelch before starting RxEqTrain

DKLP_PCS_PCS_DWORD5		
	2	**cri_always_do_int_rxeqtrain** Default Value: 0b cri_always_do_int_rxeqtrain_defaultreset Access: R/W When set, always performs an internal RxEqTrain on speed change to PCIe3, regardless of the PIPE RxEqTrain input. If an external request is active, this will always result in back-to-back RxEqTrain operations. 0: Cancel internal request if an external request is outstanding 1: Always do internal EqTrain, even if an external request is active
	1:0	**cri_sqdig_int_time** Default Value: 01b cri_sqdig_int_time_defaultreset Access: R/W Sets the value of on/off times for sqreset going to the digital squelch. 00=1.0susclk on 0.5 off, 01=1.5on 0.5off 10=2.0on 0.5off, 11=2.5on 0.5off

DKLP_TX2_PMD_LANE_MISC_LANE_TX_CNTRL

DKLP_TX2_PMD_LANE_MISC_LANE_TX_CNTRL		
Register Space: MMIO: 0/2/0 Size (in bits): 32		
TX2_PMD_LANE_MISC_LANEx::TX_CTRL		
DWord	**Bit**	**Description**
0	31:24	**Reserved** Access: RO Format: MBZ
	23:16	**dig_tx_tx_mode_sel_tx1** Access: R/W This mode sel will fix divider in TX 8'h08 : piso_clk = pll_no_div; 8'h14 : piso_clk = pll_div2; 8'h12 : piso_clk = pll_div4; 8'hA1 : piso_clk = pll_div8; 8'hC0 : piso_clk = pll_div16;
	15	**force_val_dig_tx_reset_act_low** Access: R/W
	14	**force_dig_tx_reset_act_low** Access: R/W
	13	**ecsr_dig_tx_tx_iddq_mode_tx1** Default Value: 1 Access: R/W Needs to be programmed to '0' for USB/TBT modes. This is the config directly connected to the 'iddq_mode_tx2' logic which should be '0' while working in USB and TBT as per ckt requirement. This is one of the control to indicate 'tx' will be in HighZ or not. '0' value indicates its NOT in HighZ, and for USB/TBT that's the expectations from Tx2. Value 1(def): for Dp/HDMI, so until ami setup is done post lane reset deassertion, this will be 1 after that it becomes 0; Value 0(to be programmed through NVM): For USB/TBT, so its value will be '0' throughout.
	12	**tx_cntrl_12_reserved** Access: R/W

DKLP_TX2_PMD_LANE_MISC_LANE_TX_CNTRL		
	11	**tx_cntrl_11_reserved** Access: R/W
	10	**tx_cntrl_10_reserved** Access: R/W
	9	**tx_cntrl_9_reserved** Access: R/W
	8:0	**reserved_0_8** Access: R/W

DPCLKA_CFGCR0

DPCLKA_CFGCR0	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	164280h-164283h
Name:	DPCLKA_CFGCR0
ShortName:	DPCLKA_CFGCR0
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31	**Reserved** Access: RO Format: MBZ
	30	**Reserved** Access: R/W
	29	**Reserved** Access: RO Format: MBZ
	28:27	**DDID Clock Select** Access: R/W This field selects which DPLL will drive the DDI clock. Value / Name: 00b: DPLL0 01b: DPLL1 10b: DPLL4
	26:21	**Reserved** Access: RO Format: MBZ
	20	**Reserved** Access: R/W

DPCLKA_CFGCR0

	19	**Reserved** Access: R/W
	18	**Reserved** Access: R/W
	17	**Reserved** Access: R/W
	16	**Reserved** Access: R/W
	15	**Reserved** Access: R/W
	14	**Reserved** Access: RO Format: MBZ
	13	**DDID Clock Off** Access: R/W This field gates off the DDI clock going to the display engine. It is automatically gated when the PLL is not locked. 0b: On 1b: Off **[Default]**
	12	**DDIC Clock Off** Access: R/W This field gates off the DDI clock going to the display engine. It is automatically gated when the PLL is not locked. 0b: On 1b: Off **[Default]**

DPCLKA_CFGCR0

	11	**DDIB Clock Off** Access: R/W This field gates off the DDI clock going to the display engine. It is automatically gated when the PLL is not locked. **Value** / **Name** 0b: On 1b: Off **[Default]**
	10	**DDIA Clock Off** Access: R/W This field gates off the DDI clock going to the display engine. It is automatically gated when the PLL is not locked. **Value** / **Name** 0b: On 1b: Off **[Default]**
	9:6	**Reserved** Access: RO Format: MBZ
	5:4	**DDIC Clock Select** Access: R/W This field selects which DPLL will drive the DDI clock. **Value** / **Name** 00b: DPLL0 01b: DPLL1 10b: DPLL4
	3:2	**DDIB Clock Select** Access: R/W This field selects which DPLL will drive the DDI clock. **Value** / **Name** 00b: DPLL0 01b: DPLL1 10b: DPLL4

DPCLKA_CFGCR0

	1:0	**DDIA Clock Select** Access: R/W This field selects which DPLL will drive the DDI clock. **Value** / **Name** 00b – DPLL0 01b – DPLL1 10b – DPLL4

DPST_BIN

DPST_BIN	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank
Address:	490C4h-490C7h
Name:	Pipe DPST Bin Data
ShortName:	DPST_BIN_A
Reset:	soft
Address:	491C4h-491C7h
Name:	Pipe DPST Bin Data
ShortName:	DPST_BIN_B
Reset:	soft
Address:	492C4h-492C7h
Name:	Pipe DPST Bin Data
ShortName:	DPST_BIN_C
Reset:	soft

Access to this address is steered to the correct register by programming the Bin Register Function Select and the Bin Register Index.Updates take place at the start of vertical blank.

DWord	Bit	Description

0	31	**Busy Bit**
		Access: Double Buffered
		If (DPST_CTL:Bin Register Function Select = Threshold Count) {
		This is a read only bit. If set, the engine is busy and the rest of the register is undefined. If clear, the register contains valid data.
		}
		Else (Image Enhancement) {
		This bit is reserved.
		}

	30:24	**Reserved** Access: RO Format: MBZ

DPST_BIN		

	23:0	**Data**
		
		Access: Double Buffered
		If (DPST_CTL : Bin Register Function Select = Threshold Count) {
		Bits 23:0 are read only bits when the Restore DPST bit (DPST_CTL) is cleared and read/write when the Restore DPST bit is set.
		They indicate the total number of pixels in this bin. The bin value is updated when guardband interrupt delay is met, and is not valid until after a histogram event has occurred. The bin value will stop incrementing once the maximum has been reached.
		}
		Else (Image Enhancement) {
		Bits 23:10 are reserved and should be written as zeroes. Bits 9:0 are R/W double-buffered and program the correction value for this bin. Writes to this register are double buffered on the next vblank. The value written here is the 10bit corrected channel value for the lowest point of the bin.
		}

DPST_CTL

DPST_CTL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	490C0h-490C3h
Name:	Pipe DPST Control
ShortName:	DPST_CTL_A
Reset:	soft
Address:	491C0h-491C3h
Name:	Pipe DPST Control
ShortName:	DPST_CTL_B
Reset:	soft
Address:	492C0h-492C3h
Name:	Pipe DPST Control
ShortName:	DPST_CTL_C
Reset:	soft

DWord	Bit	Description
0	31	**IE Histogram Enable** Access: R/W This bit enables the Image Enhancement histogram logic to collect data. The collected data will be valid after a histogram event has occurred. Value / Name: 0b: Disable 1b: Enable **Programming Notes** If histogram is enabled while no planes are enabled on the pipe, it may get an incorrect pixel count for a frame.
	30:29	**Reserved** Access: RO Format: MBZ
	28	**Reserved** Access: RO Format: MBZ

DPST_CTL

	27	**IE Modification Table Enable** Access: R/W This bit enables the Image Enhancement modification table. When enabled, modifications begin after the next vertical blank. Value / Name 0b: Disable 1b: Enable
	26:25	**Reserved** Access: RO Format: MBZ
	24	**Histogram Mode Select** Access: R/W Value / Name / Description 0b: YUV: YUV Luma Mode 1b: HSV: HSV Intensity Mode
	23:16	**Reserved** Access: RO Format: MBZ
	15	**IE Table Value Format** Access: R/W This field indicates what format is used for the image enhancement table values in multiplicative mode. The other modes use a 0.10 (0 integer and 10 fractional bits) format. Value / Name / Description 0b: 1.9: 1 integer and 9 fractional bits 1b: 2.8: 2 integer and 8 fractional bits

DPST_CTL

14:13 Enhancement mode

Access:	R/W

Value	Name	Description
00b	Direct	Direct look up mode
01b	Additive	Additive mode
10b	Multiplicative	Multiplicative mode
11b	Reserved	Reserved

12 Reserved

Access:	RO
Format:	MBZ

11 Bin Register Function Select

Access:	R/W

This field indicates what data is being written to or read from the bin data register.

Value	Name	Description
0b	TC	Threshold Count. A read from the bin data register returns that bin's threshold value from the most recent vblank load event (guardband threshold trip). Valid range for the Bin Index is 0 to 31.
1b	IE	Image Enhancement Value. Valid range for the Bin Index is 0 to 32

10:7 Reserved

Access:	RO
Format:	MBZ

6:0 Bin Register Index

Access:	R/W

This field indicates the bin number whose data can be accessed through the bin data register. This value is automatically incremented by a read or a write to the bin data register if the busy bit is not set.

DPST_GUARD

DPST_GUARD	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank
Address:	490C8h-490CBh
Name:	Pipe DPST Threshold Guardband
ShortName:	DPST_GUARD_A
Reset:	soft
Address:	491C8h-491CBh
Name:	Pipe DPST Threshold Guardband
ShortName:	DPST_GUARD_B
Reset:	soft
Address:	492C8h-492CBh
Name:	Pipe DPST Threshold Guardband
ShortName:	DPST_GUARD_C
Reset:	soft

Updates take place at the start of vertical blank.

DWord	Bit	Description
0	31	**Histogram Interrupt enable** Access: Double Buffered Value / Name / Description: 0b / Disable / Disabled 1b / Enable / This generates a histogram interrupt once a Histogram event occurs.
	30	**Histogram Event status** Access: R/WC When a Histogram event has occurred, this will get set by the hardware. For any more Histogram events to occur, clear this bit by writing a '1'. Value / Name / Description: 0b / Not Occurred / Histogram event has not occurred 1b / Occurred / Histogram event has occurred

<table>
<tr><th colspan="3">DPST_GUARD</th></tr>
<tr><td></td><td>29:22</td><td>Guardband Interrupt Delay

<table><tr><td>Access:</td><td>Double Buffered</td></tr></table>An interrupt is always generated after this many consecutive frames of the guardband threshold being surpassed. This value is double buffered on start of vblank.<table><tr><th>Restriction</th></tr><tr><td>A value of 0 is invalid.</td></tr></table></td></tr>
<tr><td></td><td>21:0</td><td>Threshold Guardband

<table><tr><td>Access:</td><td>Double Buffered</td></tr></table>This value is used to determine the guardband for the threshold interrupt generation. This single value is used for all the segments. This value is double buffered on start of vblank. This value is shifted left 2 bits (multiplied by 4) for use with the 24 bit bin values.</td></tr>
</table>

DSSM

DSSM	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	51004h-51007h
Name:	Display Strap State
ShortName:	DSSM
Reset:	global

This register contains fuse and strap settings for display. This register is not reset by FLR.

DWord	Bit	Description
0	31:29	**Reference Frequency** Access: RO This field indicates the reference clock frequency. Software should use this value when programming the display clocks. Value / Name: 000b: 24 MHz 001b: 19.2 MHz 010b: 38.4 MHz
	28	**Spare 28** Access: R/W
	27	**Spare 27** Access: R/W
	26	**Spare 26** Access: R/W
	25	**Spare 25** Access: R/W
	24	**Spare 24** Access: R/W
	23	**Spare 23** Access: R/W

DSSM		
	22	**Spare 22** Access: R/W
	21	**Spare 21** Access: R/W
	20	**Spare 20** Access: R/W
	19	**Spare 19** Access: R/W
	18	**Spare 18** Access: R/W
	17	**Spare 17** Access: R/W
	16	**Spare 16** Access: R/W
	15	**Spare 15** Access: R/W
	14	**Spare 14** Access: R/W
	13	**Spare 13** Access: R/W
	12	**Spare 12** Access: R/W
	11	**Spare 11** Access: R/W
	10	**Spare 10** Access: R/W

DSSM

	9	**Spare 9** Access: R/W
	8	**Spare 8** Access: R/W
	7	**Spare 7** Access: R/W
	6	**DE 8k Dis** Access: R/W DE_8K_DIS 8k capability fuse. This bit indicates whether hardware supports screens with widths greater than 5120 pixels. For tiled or joined displays, this is the total width after combining the widths of both pipes. Software must not enable these resolutions when the fuse is configured to disable 8k.

Value	Name	Description
0b	Enable	8k Capability Enabled
1b	Disable	8k Capability Disabled

	5	**Audio IO Flop Bypass** Access: R/W This field specifies whether the audio IO flop should be bypassed for dies with a long path to IO.

Value	Name
0b	Don't Bypass
1b	Bypass

	4	**Audio IO Select** Access: R/W This field specifies which audio IO location to use. It has to match where the PCH audio is connecting to the die.

Value	Name
0b	South
1b	North

DSSM

	3	**WD Video Fault Continue** Access: R/W This field specifies whether WD video should continue data writes after a fault or stop the writes. Value / Name 0b: Stop Writes 1b: Continue Writes
	2	**Reserved** Access: R/W
	1	**Part Is SOC** Access: R/W
	0	**DisplayPort A Present** Access: R/W This bit specifies whether the port was present during initialization. This strap state can also be read in the DDI_BUF_CTL_A 0x64000 register bit 0. Value / Name / Description 0b: Not Present: Port not present 1b: Present: Port present

FUSE_STATUS

FUSE_STATUS

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	42000h-42003h
Name:	Fuse Status
ShortName:	FUSE_STATUS
Reset:	global

This register is on the ungated clock and the chip reset, not the FLR.

DWord	Bit	Description
0	31	**Fuse Download Status** Access: RO This field indicates the status of fuse and strap download to the Display Engine. After fuse and strap download, fuses will be distributed within the Display Engine. Value: 0b – Not Done; 1b – Done
	30:28	**Reserved** Access: RO Format: MBZ
	27	**Fuse PG0 Distribution Status** Access: RO This field indicates the status of fuse distribution to power well #0. Value: 0b – Not Done; 1b – Done
	26	**Fuse PG1 Distribution Status** Access: RO This field indicates the status of fuse distribution to power well #1. Value: 0b – Not Done; 1b – Done

FUSE_STATUS

	25	**Reserved** Access: RO Format: MBZ
	24	**Fuse PG3 Distribution Status** Access: RO This field indicates the status of fuse distribution to power well #3. 0b – Not Done 1b – Done
	23	**Fuse PG4 Distribution Status** Access: RO This field indicates the status of fuse distribution to power well #4. 0b – Not Done 1b – Done
	22:16	**Reserved** Access: RO Format: MBZ
	15:0	**Reserved** Access: RO Format: MBZ

HDPORT_STATE

HDPORT_STATE - HDPORT_STATE

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32

Address:	45050h-45053h
Name:	HD PORT STATE
ShortName:	HDPORT_STATE
Reset:	soft

Description

This register reflects global status of the HDPORT (AKA HTI). HDPORT/HTI can take away display PLL and PHY resources on some projects. Refer to the sequence to initialize display to find on which projects that HDPORT/HTI will impact display.
The list of PLLs and PHYs in this register is a superset of resources that HDPORT/HTI can make use of, so it does not necessarily reflect all the resources supported by display engine.

Mapping to display resource names
DDI0 = PHY A, connected to DDI A
DDI1 = PHY B, connected to DDI B
DDI2 = PHY C, connected to DDI TC1
DDI3 = PHY D, connected to DDI TC2
DDI4 = Unused
DPLL0 = DPLL0
DPLL1 = DPLL1
DPLL2 = DPLL4
DPLL3 = Unused

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15	**DPLL3_USED** Access: RO Indicates if display PLL3 is being used by HTI. 0b – Not used 1b – Used

HDPORT_STATE - HDPORT_STATE

	14	**DPLL2_USED** Access: RO Indicates if display PLL2 is being used by HTI. 0b: Not used 1b: Used
	13	**DPLL1_USED** Access: RO Indicates if display PLL1 is being used by HTI. 0b: Not used 1b: Used
	12	**DPLL0_USED** Access: RO Indicates if display PLL0 is being used by HTI. 0b: Not used 1b: Used
	11	**Spare_11** Access: RO
	10	**Spare_10** Access: RO
	9	**Spare_9** Access: RO
	8	**HDMI_DP3** Access: RO Indicates if PHY D is being used by HTI in HDMI mode. 0b: DP 1b: HDMI

HDPORT_STATE - HDPORT_STATE

	7	**DDI3_USED** Access: RO Indicates if PHY D is being used by HTI. Value: 0b – Not used; 1b – Used
	6	**HDMI_DP2** Access: RO Indicates if PHY C is being used by HTI in HDMI mode. Value: 0b – DP; 1b – HDMI
	5	**DDI2_USED** Access: RO Indicates if PHY C is being used by HTI. Value: 0b – Not used; 1b – Used
	4	**HDMI_DP1** Access: RO Indicates if PHY B is being used by HTI in HDMI mode. Value: 0b – DP; 1b – HDMI
	3	**DDI1_USED** Access: RO Indicates if PHY B is being used by HTI. Value: 0b – Not used; 1b – Used

HDPORT_STATE - HDPORT_STATE

	2	**HDMI_DP0** Access: RO Indicates if PHY A is being used by HTI in HDMI mode. Value / Name: 0b – DP 1b – HDMI
	1	**DDI0_USED** Access: RO Indicates if PHY A is being used by HTI. Value / Name: 0b – Not used 1b – Used
	0	**HDPORT_En** Access: RO Indicates if HD PORT is enabled.

MBUS_ABOX_CTL

MBUS_ABOX_CTL

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	45038h-4503Bh
Name:	MBus ABox Control
ShortName:	MBUS_ABOX_CTL
Reset:	soft

DWord	Bit	Description
0	31	**Status** Access: RO This field indicates if the box is enabled. 0b – Disabled 1b – Enabled
	30:27	**Ring Stop Address** Access: RO This field indicates the address of the box in the ring.
	26:22	**B2B Transactions Max** Access: R/W This fields indicates the number of back-to-back transactions that can be added to either to top or bottom of the ring when 'Regulate Transactions' bit is 1b. 10 – **[Default]** [1-31]
	21:20	**BW Credits** Default Value: 1h Access: R/W BW credits are used by the Arbiter to initiate write cycles when performing VRH read-modified-writes to the display buffer.

MBUS_ABOX_CTL

	19:16	**B Credits** Default Value: 1h Access: R/W B credits are used by the Arbiter to initiate read cycles when performing VRH read-modified-writes to the display buffer.
	15:14	**Reserved** Access: RO Format: MBZ
	13	**Regulate B2B Transactions** Access: R/W This field controls the regulation of back-to-back transactions from this ring stop. 0b – Disable 1b – Enable **[Default]**
	12:8	**BT Credits Pool2** Default Value: 10h Access: R/W BT credits are used by the Arbiter to request trackers from the Display Buffer.
	7:5	**B2B Transactions Delay** Access: R/W This field indicates the number of wait cycles after the maximum back-to-back transactions is sent. [0-7] 2 – **[Default]**
	4:0	**BT Credits Pool1** Default Value: 10h Access: R/W BT credits are used by the Arbiter to request trackers from the Display Buffer.

MBUS_DBOX_CTL

MBUS_DBOX_CTL

Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank OR pipe disabled

Address:	7003Ch-7003Fh
Name:	Pipe MBus DBox Control
ShortName:	PIPE_MBUS_DBOX_CTL_A
Reset:	soft

Address:	7103Ch-7103Fh
Name:	Pipe MBus DBox Control
ShortName:	PIPE_MBUS_DBOX_CTL_B
Reset:	soft

Address:	7203Ch-7203Fh
Name:	Pipe MBus DBox Control
ShortName:	PIPE_MBUS_DBOX_CTL_C
Reset:	soft

DWord	Bit	Description
0	31	**Status** Access: RO This field indicates if the box is enabled. 0b: Disabled 1b: Enabled
	30:27	**Ring Stop Address** Access: RO This field indicates the address of the box in the ring.
	26:25	**Reserved** Access: RO Format: MBZ

MBUS_DBOX_CTL

	24:20	**B2B Transactions Max** Access: Double Buffered This fields indicates the number of back-to-back transactions that can be added to either to top or bottom of the ring when 'Regulate Transactions' bit is 1b. Value / Name 16 / **[Default]** [1-31] /
	19:17	**B2B Transactions Delay** Access: Double Buffered This field indicates the number of wait cycles after the maximum back-to-back transactions is sent. Value / Name [0-7] / 1 / **[Default]**
	16	**Regulate B2B Transactions** Access: Double Buffered This field controls the regulation of back-to-back transactions from this ring stop. Value / Name 0b / Disable 1b / Enable **[Default]**
	15:14	**BW Credits** Access: Double Buffered BW credits are used by the display pipe to write color clear data to DBUF. Value / Name 1h / **[Default]** Programming Notes See the Mbus narrative page for programming instructions and optimal values.
	13	**Reserved** Access: RO Format: MBZ

MBUS_DBOX_CTL

	12:8	**B Credits** Access: Double Buffered B credits are used by the display pipe to request data from display buffer. **Value** / **Name**: 0Ch / **[Default]** **Programming Notes**: See the Mbus narrative page for programming instructions and optimal values.
	7:5	**Reserved** Access: RO Format: MBZ
	4	**Reserved** Access: RO Format: MBZ
	3:0	**A Credits** Access: Double Buffered A credits are used by the display pipe to make data/TLB/VTd/MCS requests to Arbiter. **Value** / **Name**: 2h / 2 credits **[Default]**

OUTPUT_CSC_COEFF

OUTPUT_CSC_COEFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	192
_Custom_Display _DoubleBufferArmedBy:	Write to CSC_MODE
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank after armed

Address:	49050h-49067h
Name:	Pipe Output CSC Coefficients
ShortName:	OUTPUT_CSC_COEFF_A
Reset:	soft

Address:	49150h-49167h
Name:	Pipe Output CSC Coefficients
ShortName:	OUTPUT_CSC_COEFF_B
Reset:	soft

Address:	49250h-49267h
Name:	Pipe Output CSC Coefficients
ShortName:	OUTPUT_CSC_COEFF_C
Reset:	soft

DWord	Bit	Description
0	31:16	**RY** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**GY** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
1	31:16	**BY** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**Reserved** Access: RO Format: MBZ

OUTPUT_CSC_COEFF		
2	31:16	**RU** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**GU** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
3	31:16	**BU** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**Reserved** Access: RO Format: MBZ
4	31:16	**RV** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**GV** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
5	31:16	**BV** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**Reserved** Access: RO Format: MBZ

OUTPUT_CSC_POSTOFF

OUTPUT_CSC_POSTOFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	96
_Custom_Display _DoubleBufferArmedBy:	Write to CSC_MODE
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	49074h-4907Fh
Name:	Pipe Output CSC Post-Offsets
ShortName:	OUTPUT_CSC_POSTOFF_A
Reset:	soft
Address:	49174h-4917Fh
Name:	Pipe Output CSC Post-Offsets
ShortName:	OUTPUT_CSC_POSTOFF_B
Reset:	soft
Address:	49274h-4927Fh
Name:	Pipe Output CSC Post-Offsets
ShortName:	OUTPUT_CSC_POSTOFF_C
Reset:	soft

The post-offset is intended to add an offset from 0 on the Y or RGB channels and to convert UV channels from 2's complement to excess 0.5 as they exit pipe output color space conversion (CSC).

DWord	Bit	Description
0	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PostCSC High Offset** Access: Double Buffered This value is used to give an offset to the high color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
1	31:13	**Reserved** Access: RO Format: MBZ

<table>
<tr><th colspan="3">OUTPUT_CSC_POSTOFF</th></tr>
<tr><td></td><td>12:0</td><td>PostCSC Medium Offset

<table><tr><td>Access:</td><td>Double Buffered</td></tr></table>This value is used to give an offset to the medium color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).</td></tr>
<tr><td rowspan="2">2</td><td>31:13</td><td>Reserved

<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td>12:0</td><td>PostCSC Low Offset

<table><tr><td>Access:</td><td>Double Buffered</td></tr></table>This value is used to give an offset to the low color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).</td></tr>
</table>

OUTPUT_CSC_PREOFF

OUTPUT_CSC_PREOFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	96
_Custom_Display _DoubleBufferArmedBy:	Write to CSC_MODE
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	49068h-49073h
Name:	Pipe Output CSC Pre-Offsets
ShortName:	OUTPUT_CSC_PREOFF_A
Reset:	soft
Address:	49168h-49173h
Name:	Pipe Output CSC Pre-Offsets
ShortName:	OUTPUT_CSC_PREOFF_B
Reset:	soft
Address:	49268h-49273h
Name:	Pipe Output CSC Pre-Offsets
ShortName:	OUTPUT_CSC_PREOFF_C
Reset:	soft

The pre-offset is intended to remove an offset from 0 on the Y or RGB channels and to convert UV channels from excess 0.5 to 2's complement as they enter pipe output color space conversion (CSC).

DWord	Bit	Description
0	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PreCSC High Offset** Access: Double Buffered This value is used to give an offset to the high color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
1	31:13	**Reserved** Access: RO Format: MBZ

OUTPUT_CSC_PREOFF		
	12:0	**PreCSC Medium Offset** Access: Double Buffered This value is used to give an offset to the medium color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
2	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PreCSC Low Offset** Access: Double Buffered This value is used to give an offset to the low color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).

PHY_MISC

PHY_MISC	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	64C00h-64C03h
Name:	PHY_MISC_A
ShortName:	PHY_MISC_A
Reset:	global
Address:	64C04h-64C07h
Name:	PHY_MISC_B
ShortName:	PHY_MISC_B
Reset:	global
Address:	64C08h-64C0Bh
Name:	PHY_MISC_C
ShortName:	PHY_MISC_C
Reset:	global

This register is on the ungated clock and the chip reset, not the FLR.

DWord	Bit	Description
0	31:28	**DE to IO Misc** Default Value: 0010b Access: R/W
	27:24	**IO to DE Misc** Access: RO
	23	**DE to IO Comp Pwr Down** Access: R/W Description: This register field need only be programmed for port A and B.
	22	**Spare 22** Access: R/W
	21	**Spare 21** Access: R/W

PHY_MISC		
	20	**Spare 20** Access: R/W
	19:12	**Reserved** Access: RO Format: MBZ
	11:4	**Reserved** Access: RO Format: MBZ
	3:0	**Reserved** Access: RO Format: MBZ

PIPE_ARB_CTL

PIPE_ARB_CTL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank OR pipe disabled
Address:	70028h-7002Bh
Name:	Pipe Arbiter Control
ShortName:	PIPE_ARB_CTL_A
Reset:	soft
Address:	71028h-7102Bh
Name:	Pipe Arbiter Control
ShortName:	PIPE_ARB_CTL_B
Reset:	soft
Address:	72028h-7202Bh
Name:	Pipe Arbiter Control
ShortName:	PIPE_ARB_CTL_C
Reset:	soft

There is one instance of this register per pipe.

DWord	Bit	Description
0	31	**Reserved** Access: RO Format: MBZ
	30:21	**Reserved** Access: RO Format: MBZ
	20	**Disable Weighted Arbitration** Access: Double Buffered This field disables the weighted pipe slice arbitration. 0b: Enable **[Default]** 1b: Disable

PIPE_ARB_CTL

	19	**Reserved** Access: Double Buffered
	18:16	**Additional Slots** Access: Double Buffered These additional Slots gets added to each arbitration cycle during which the clients gets serviced in a round robin manner. A programmed value of 1b results in 1 additional slot.
	15:14	**Reserved** Access: RO Format: MBZ
	13	**Use Programmed Slots** Access: Double Buffered When this field is set, HW uses the Slots programmed in the PLANE_CTL register instead of the HW defaults.
	12	**Disable Block Valid Check** Access: Double Buffered The field disables the block valid check done at pipe arbiter. Value: 0b – Enable Value: 1b – Disable
	11:10	**DSB Arbitration Interval** Access: Double Buffered This field defines the DSB requests service interval in the pipe arbitration. Value: 00b – 16 clocks Value: 01b – 32 clocks Value: 10b – 64 clocks **[Default]** Value: 11b – 128 clocks

PIPE_ARB_CTL

	9:8	**Request Vs Data Arbitration** Access: Double Buffered This field selects the arbitration weightage for the Streamer and the DDB requests. **Value** / **Name** / **Description** 00b / / Allow 1 Streamer requests every 2 DDB requests. 01b / / Allow 1 Streamer requests every 4 DDB requests. 10b / **[Default]** / Allow 1 Streamer requests every 8 DDB requests. 11b / / Allow 1 Streamer requests every 16 DDB requests.
	7:6	**Reserved** Access: RO Format: MBZ
	5:0	**Frame Start Drain Delay** Access: Double Buffered This field contains the time, in microseconds, the pipe waits before draining the data from the Display Buffer. **Value** / **Name** [0-31] / 15 / **[Default]**

PIPE_BOTTOM_COLOR

PIPE_BOTTOM_COLOR	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank OR pipe disabled
Address:	70034h-70037h
Name:	Pipe Bottom Color
ShortName:	PIPE_BOTTOM_COLOR_A
Reset:	soft
Address:	71034h-71037h
Name:	Pipe Bottom Color
ShortName:	PIPE_BOTTOM_COLOR_B
Reset:	soft
Address:	72034h-72037h
Name:	Pipe Bottom Color
ShortName:	PIPE_BOTTOM_COLOR_C
Reset:	soft

This register sets the color that appears underneath the bottom most plane in the pipe blender Z-order.The value for each color channel is represented in an unsigned 0.10 format with 0 integer and 10 fractional bits.

DWord	Bit	Description
0	31	**Pipe Gamma Enable** Access: Double Buffered This bit enables pipe gamma correction for the bottom color. This field is deprecated. Value: 0b — Disable; 1b — Enable

PIPE_BOTTOM_COLOR

30 Pipe CSC Enable

Access:	Double Buffered

This bit enables pipe color space conversion for the bottom color.
This field is deprecated.

Value	Name
0b	Disable
1b	Enable

29:20 V R Bottom Color

Access:	Double Buffered
Format:	U0.10

This field sets the bottom color for the V or Red channel.

19:10 Y G Bottom Color

Access:	Double Buffered
Format:	U0.10

This field sets the bottom color for the Y or Green channel.

9:0 U B Bottom Color

Access:	Double Buffered
Format:	U0.10

This field sets the bottom color for the U or Blue channel.

PIPE_DMCSCANLINECOMP

PIPE_DMCSCANLINECOMP

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	7000Ch-7000Fh
Name:	Pipe Scan Line Compare for DMC
ShortName:	PIPE_DMCSCANLINECOMP_A
Reset:	soft
Address:	7100Ch-7100Fh
Name:	Pipe Scan Line Compare for DMC
ShortName:	PIPE_DMCSCANLINECOMP_B
Reset:	soft
Address:	7200Ch-7200Fh
Name:	Pipe Scan Line Compare for DMC
ShortName:	PIPE_DMCSCANLINECOMP_C
Reset:	soft

DWord	Bit	Description
0	31	**Enable Compare** Access: R/W This field enables the scan line compare for DMC event generation. When this register is written with this bit set to 1b, the display engine will, trigger a scan line event after reaching the programmed scan line number. It will do the same on every frame. Value / Name: 0b – Do nothing 1b – Enable compare Restriction: Do not enable this register if the event is not needed in the DMC.
	30:20	**Reserved** Access: RO Format: MBZ
	19:0	**Scan Line Value** Access: R/W This field specifies the ending scan line number of the scan line window.

PIPE_FLIPCNT

PIPE_FLIPCNT	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	70044h-70047h
Name:	Pipe Flip Count
ShortName:	PIPE_FLIPCNT_A
Reset:	soft
Address:	71044h-71047h
Name:	Pipe Flip Count
ShortName:	PIPE_FLIPCNT_B
Reset:	soft
Address:	72044h-72047h
Name:	Pipe Flip Count
ShortName:	PIPE_FLIPCNT_C
Reset:	soft

DWord	Bit	Description
0	31:0	**Pipe Flip Counter** Access: R/W This field provides read back of the display pipe flip counter. The counter increments on the start of each flip to the selected plane of this pipe. The start of flip is when the plane surface address is updated, not when the flip completes. The flip can be through command streamer asynchronous and synchronous flips or MMIO writes to the plane 1 surface address. It rolls over back to 0 after (2^32)-1 flips. Pipe flip counter is restricted to one plane at a time. The plane select is programmed in PIPE_MISC2->Flip Timestamp Plane Select.

PIPE_FLIPDONETMSTMP

PIPE_FLIPDONETMSTMP	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	70054h-70057h
Name:	Pipe Flip Done Time Stamp
ShortName:	PIPE_FLIPDONETMSTMP_A
Reset:	soft
Address:	71054h-71057h
Name:	Pipe Flip Done Time Stamp
ShortName:	PIPE_FLIPDONETMSTMP_B
Reset:	soft
Address:	72054h-72057h
Name:	Pipe Flip Done Time Stamp
ShortName:	PIPE_FLIPDONETMSTMP_C
Reset:	soft

DWord	Bit	Description
0	31:0	**Pipe Flip Done Time Stamp** Access: R/W This field provides read back of the display pipe flip done time stamp. The time stamp value is sampled when hardware latches on to the new surface and the flip done gets sent. The flip can be through command streamer asynchronous and synchronous flips or MMIO writes to the plane. The TIMESTAMP_CTR register has the current time stamp value. Flip time stamp sampling is restricted to one plane at a time. The plane select is programmed in PIPE_MISC2->Flip Timestamp Plane Select.

PIPE_FLIPTMSTMP

PIPE_FLIPTMSTMP	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	7004Ch-7004Fh
Name:	Pipe Flip Time Stamp
ShortName:	PIPE_FLIPTMSTMP_A
Reset:	soft
Address:	7104Ch-7104Fh
Name:	Pipe Flip Time Stamp
ShortName:	PIPE_FLIPTMSTMP_B
Reset:	soft
Address:	7204Ch-7204Fh
Name:	Pipe Flip Time Stamp
ShortName:	PIPE_FLIPTMSTMP_C
Reset:	soft

DWord	Bit	Description
0	31:0	**Pipe Flip Time Stamp** Access: R/W This field provides read back of the display pipe flip time stamp. The time stamp value is sampled on the start of each flip. The start of flip is when the plane surface address is updated, not when the flip completes. The flip can be through command streamer asynchronous and synchronous flips or MMIO writes. The TIMESTAMP_CTR register has the current time stamp value. Writes to this register will overwrite and update the time stamp value. Flip time stamp sampling is restricted to one plane at a time. The plane select is programmed in PIPE_MISC2->Flip Timestamp Plane Select.

PIPE_FRMCNT

PIPE_FRMCNT		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	70040h-70043h	
Name:	Pipe Frame Count	
ShortName:	PIPE_FRMCNT_A	
Reset:	soft	
Address:	71040h-71043h	
Name:	Pipe Frame Count	
ShortName:	PIPE_FRMCNT_B	
Reset:	soft	
Address:	72040h-72043h	
Name:	Pipe Frame Count	
ShortName:	PIPE_FRMCNT_C	
Reset:	soft	

DWord	Bit	Description
0	31:0	**Pipe Frame Counter** Access: R/W Provides read back of the display pipe frame counter. This counter increments on every start of vertical blank and rolls over back to 0 after (2^32)-1 frames.

PIPE_FRMTMSTMP

PIPE_FRMTMSTMP	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	70048h-7004Bh
Name:	Pipe Frame Time Stamp
ShortName:	PIPE_FRMTMSTMP_A
Reset:	soft
Address:	71048h-7104Bh
Name:	Pipe Frame Time Stamp
ShortName:	PIPE_FRMTMSTMP_B
Reset:	soft
Address:	72048h-7204Bh
Name:	Pipe Frame Time Stamp
ShortName:	PIPE_FRMTMSTMP_C
Reset:	soft

DWord	Bit	Description
0	31:0	**Pipe Frame Time Stamp** Access: R/W This field provides read back of the display pipe frame time stamp. The time stamp value is sampled at every start of vertical blank. The TIMESTAMP_CTR register has the current time stamp value. Writes to this register will overwrite and update the time stamp value.

PIPE_ISOCREQ

PIPE_ISOCREQ - PIPE_ISOCREQ

Register Space:	MMIO: 0/2/0
Size (in bits):	64

Address:	70010h-70017h
Name:	Pipe Isoch Request
ShortName:	PIPE_ISOCREQ_A
Reset:	soft

Address:	71010h-71017h
Name:	Pipe Isoch Request
ShortName:	PIPE_ISOCREQ_B
Reset:	soft

Address:	72010h-72017h
Name:	Pipe Isoch Request
ShortName:	PIPE_ISOCREQ_C
Reset:	soft

When enabled, the write to DWord 1 (higher address DWord) of this register triggers an IsocReq to be sent with the last written values from both DWords.

DWord	Bit	Description
0	31:16	**LTR** Access: R/W This field specifies the latency tolerance (LTR) for this pipe in microseconds.
	15:0	**Bandwidth** Access: R/W This field specifies the bandwidth requirement for this pipe in multiples of 100 MB/s.
1	31	**Enable** Access: R/W This field enables IsocReq to be sent when DWord 1 of this register is written. Value: 1b — Name: Enable Value: 0b — Name: Disable
	30:8	**Reserved** Access: RO Format: MBZ

PIPE_ISOCREQ - PIPE_ISOCREQ		
	7:0	**Delay** Access: R/W This field specifies the downwards transition delay for this pipe in milliseconds.

PIPE_ISOCREQ_OFFSET

PIPE_ISOCREQ_OFFSET - PIPE_ISOCREQ_OFFSET	
Register Space:	MMIO: 0/2/0
Size (in bits):	64
Address:	70018h-7001Fh
Name:	Pipe Isoch Offset addition
ShortName:	PIPE_ISOCREQ_OFFSET_A
Reset:	soft
Address:	71018h-7101Fh
Name:	Pipe Isoch Offset addition
ShortName:	PIPE_ISOCREQ_OFFSET_B
Reset:	soft
Address:	72018h-7201Fh
Name:	Pipe Isoch Offset addition
ShortName:	PIPE_ISOCREQ_OFFSET_C
Reset:	soft

The values programmed in this register will added as offsets to the LTR, BW and Delay. SW must ensure to clear these registers if no offset is desired to be added.
For example, if LTR offset is programmed to 0x0100 in this register, then this value is added to the LTR value programmed in PIPE_ISOCREQ.

DWord	Bit	Description
0	31:16	**LTR offset** Access: R/W This field specifies the latency tolerance (LTR) offset to be added to LTR value in PIPE_ISOCREQ for this pipe in microseconds.
	15:0	**Bandwidth offset** Access: R/W This field specifies the bandwidth requirement offset to be added to BW value in the PIPE_ISOCREQ register
1	31:8	**Reserved** Access: RO Format: MBZ

PIPE_ISOCREQ_OFFSET - PIPE_ISOCREQ_OFFSET		
	7:0	**Delay Offset** Access: R/W This field specifies the offset to be added to the downwards transition delay programmed in the PIPE_ISOCREQ.

PIPE_MISC

PIPE_MISC	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank OR pipe disabled
Address:	70030h-70033h
Name:	Pipe Miscellaneous
ShortName:	PIPE_MISC_A
Reset:	soft
Address:	71030h-71033h
Name:	Pipe Miscellaneous
ShortName:	PIPE_MISC_B
Reset:	soft
Address:	72030h-72033h
Name:	Pipe Miscellaneous
ShortName:	PIPE_MISC_C
Reset:	soft

DWord	Bit	Description
0	31:30	**Stereo Mask Pipe Int** Access: Double Buffered This field controls which pipe vertical timing (vertical blank, scan line, and vertical sync) events will be reported in interrupts during stereo 3D mode. Value / Name / Description: 00b / Mask None / No masking. Report both the left and right eye vertical events. 01b / Mask Left / Mask the left eye vertical events. Only report right eye events. 10b / Mask Right / Mask the right eye vertical events. Only report left eye events. 11b / Reserved / Reserved

PIPE_MISC

		Restriction This field must be programmed prior to enabling stereo 3D mode and must not be changed while stereo 3D is enabled. In the stacked frame mode, the vertical sync is not generated in the gap between left and right eye images, and the scan line count increments across the entire tall frame, so masking may cause unexpected behavior for those events.
	29:28	**Stereo Mask Pipe Render** Access: Double Buffered This field controls which pipe vertical timing (vertical blank, scan line, and vertical sync) events will be reported in render responses during stereo 3D mode. **Value** / **Name** / **Description** 00b / Mask None / No masking. Report both the left and right eye vertical events. 01b / Mask Left / Mask the left eye vertical events. Only report right eye events. 10b / Mask Right / Mask the right eye vertical events. Only report left eye events. 11b / Reserved / Reserved **Restriction** This field must be programmed prior to enabling stereo 3D mode and must not be changed while stereo 3D is enabled. In the stacked frame mode, the vertical sync is not generated in the gap between left and right eye images, and the scan line count increments across the entire tall frame, so masking may cause unexpected behavior for those events.
	27	**YUV420 Enable** Access: Double Buffered This field enables YUV420 output from this pipe. This is only for use with HDMI and DP. **Value** / **Name** 0b / Disable 1b / Enable **Restriction** This field must be programmed prior to enabling the transcoder attached to this pipe.

PIPE_MISC

26 YUV420 Mode

Access:	Double Buffered

This field specifies the mode in which YUV420 pixels are generated by this pipe.

Value	Name	Description
0b	Bypass	Bypass mode defeatured. Only full blend mode supported.
1b	Full blend	

25 Pipe Gamma Input Clamp Disable

Access:	Double Buffered

This field controls the pipe post csc gamma input clamp operation. When this bit is set to 0b the negative pixel values get clamped to zero at the gamma input.

Value	Name
0b	Enable **[Default]**
1b	Disable

24 Allow Double Buffer Update Disable

Access:	R/W

This field controls whether double buffer updates are allowed to be disabled for the double buffered pipe registers listed below. The DOUBLE_BUFFER_CTL register can be configured to globally disable double buffer updates for those resources that allow them to be disabled.

Value	Name
0b	Not Allowed
1b	Allowed **[Default]**

23 HDR Mode

Access:	Double Buffered

This field enables the HDR mode, allowing for higher precision output from the HDR supporting planes and bypassing the SDR planes in blending.

In addition to setting bit 8 of this register (Pixel Rounding), this bit must be set to 1b to passthrough the frame buffer pixels unmodified across the pipe.

Value	Name
0b	Disable
1b	Enable

PIPE_MISC

	22	**Change Mask for LDPST** Access: Double Buffered This field controls the change tracking for the LACE. Change tracking can be used by PSR/SRD and WD Value: 0b — Name: Not Masked Value: 1b — Name: Masked
	21	**Change Mask for Register Write** Access: Double Buffered This field controls change tracking for the pipe register write. Change tracking can be used by PSR/SRD and WD. Value: 0b — Name: Not Masked Value: 1b — Name: Masked
	20	**Change Mask for Vblank Vsync Int** Access: Double Buffered This field controls change tracking for the vblank or vsync interrupt enable. Change tracking can be used by PSR/SRD and WD. Value: 0b — Name: Not Masked Value: 1b — Name: Masked
	19	**Reserved** Access: Double Buffered
	18	**Reserved** Access: Double Buffered
	17	**Reserved** Access: Double Buffered
	16	**Reserved** Access: Double Buffered

PIPE_MISC

15:14 Rotation Info

Access:	Double Buffered

This field indicates to internal KVMR screen capture that the display has been rotated through software or hardware rotation. Select the closest value if the rotation is not an exact multiple of 90 degrees. Hardware rotation of the display output is controlled through the plane control registers, not through this field.

Value	Name	Description
00b	None	No rotation on this pipe
01b	90	90 degree rotation on this pipe
10b	180	180 degree rotation on this pipe
11b	270	270 degree rotation on this pipe

Restriction
This field must be programmed in order for internal KVMR screen capture to work correctly when display is rotated by software or hardware.

13 Reserved

Access:	RO
Format:	MBZ

12 OLED Compensation

Access:	Double Buffered

This field enables the OLED compensation on the pipe. When this bit is set, plane 5 is used as the OLED compensation plane with up to 10 bits per channel precision. OLED compensation must be used only when the pipe is configured to output RGB format.

The OLED compensation plane size must be same as the pipe active size.

Value	Name
0b	Disable
1b	Enable

11 Pipe output color space select

Access:	Double Buffered

This field indicates the output color space. This field affects the values of the pipe border and some capture functions. This field does not affect the planes, pipe CSC, or ports.

Value	Name
0b	RGB

PIPE_MISC

		1b: YUV

Restriction
This field must be set to match the color space that will be output from the pipe CSC or output from the planes if they pipe CSC is bypassed.

10 — xvYCC Color Range Limit

Access:	Double Buffered

This field limits the color range of the pipe output to 1 to 254 for 8-bit components, 4 to 1019 for 10bit components, and 16 to 4079 for 12-bit components. Values outside of the range will be clamped to fit within the range.

Value	Name	Description
0b	Full	Do not limit the range
1b	Limit	Limit range

9 — Pixel Extension

Access:	Double Buffered

This field controls how the pixel extension is handled in the pipe.
In scenarios where the frame buffers bpc is larger or equal to the port output bpc, this bit may be programmed to 'Zero Extend'.

Value	Name
0b	MSB Extend **[Default]**
1b	Zero Extend

8 — Pixel Rounding

Access:	Double Buffered

This field controls the pixel rounding at the end of the pipe.
This bit must be set to 1b to passthrough the frame buffer pixels unmodified across the pipe.

Value	Name
0b	Round Up **[Default]**
1b	Truncate

7:5 — Dithering BPC

Access:	Double Buffered

This field selects the number of bits per color to be used in dithering.

Value	Name	Description
000b	8 bpc	8 bits per color
001b	10 bpc	10 bits per color
010b	6 bpc	6 bits per color

PIPE_MISC

Others	Reserved	Reserved

Programming Notes
When dithering is enabled, the value selected here should match the bits per color selected in the Transcoder DDI Function Control register attached to this pipe.

4 **Dithering enable**

Access:	Double Buffered

This field enables dithering.

Value	Name
0b	Disable
1b	Enable

3:2 **Dithering type**

Access:	Double Buffered

This field selects the dithering type.

Value	Name	Description
00b	Spatial	Spatial
01b	ST1	Spatio-Temporal 1
10b	ST2	Spatio-Temporal 2
11b	Temporal	Temporal

1 **Reserved**

Access:	RO
Format:	MBZ

0 **Reserved**

Access:	Double Buffered

PIPE_MISC2

PIPE_MISC2	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank OR pipe disabled
Address:	7002Ch-7002Fh
Name:	Pipe Miscellaneous 2
ShortName:	PIPE_MISC2_A
Reset:	soft
Address:	7102Ch-7102Fh
Name:	Pipe Miscellaneous 2
ShortName:	PIPE_MISC2_B
Reset:	soft
Address:	7202Ch-7202Fh
Name:	Pipe Miscellaneous 2
ShortName:	PIPE_MISC2_C
Reset:	soft

There is one instance of this register per pipe.

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23:20	**TLB Throttle** Default Value: 8 Access: Double Buffered This field specifies how often the TLB requests are sent. If the programmed value is x, TLBs requests are sent once in x clocks if there are competing data requests.
	19:16	**Reserved** Access: RO Format: MBZ

PIPE_MISC2

	15:12	**IPC Demote Req Chunk Size** Default Value: 8 Access: Double Buffered This field limits the request burst sizes while in IPC demote. A value of 0 disables the inflight limit.
	11	**Reserved** Access: RO Format: MBZ
	10:9	**Reserved** Access: RO Format: MBZ
	8	**ASFU Flip exception** Access: Double Buffered Value / Name / Description: 1b / mask / Add exception for Flip for global register update event and Pipe register update event. 0b / No mask / Do not add exception for Flip for global register update event and Pipe register update event.
	7	**Reserved** Access: RO Format: MBZ
	6:4	**Scanline Plane Select** Access: Double Buffered This field specifies the plane for which scanline compare fetch line is captured. A programmed value of 0b selects plane 1. Value / Name: [0h-6h] /
	3	**Reserved** Access: RO Format: MBZ

<table>
<tr><th colspan="3">PIPE_MISC2</th></tr>
<tr><td></td><td>2:0</td><td>Flip Info Plane Select

<table><tr><td>Access:</td><td>Double Buffered</td></tr></table>This field specifies the plane for which flip information is captured. A programmed value of 0b selects plane 1.<table><tr><th>Value</th><th>Name</th></tr><tr><td>[0h-6h]</td><td></td></tr></table></td></tr>
</table>

PIPE_SCANLINE

PIPE_SCANLINE

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	70000h-70003h
Name:	Pipe Scan Line
ShortName:	PIPE_SCANLINE_A
Reset:	soft
Address:	71000h-71003h
Name:	Pipe Scan Line
ShortName:	PIPE_SCANLINE_B
Reset:	soft
Address:	72000h-72003h
Name:	Pipe Scan Line
ShortName:	PIPE_SCANLINE_C
Reset:	soft

This register enables the read back of the pipe vertical line counter. The value increments at the leading edge of HSYNC. The value resets to line zero at the first active line of the display. In interlaced display timings, the scan line counter provides the current line in the field. One field can have a total number of lines that is one greater than the other field.

DWord	Bit	Description
0	31	**Current Field** Access: RO This is an indication of the current display field. Value / Name / Description: 0b / Odd / First field (odd field) 1b / Even / Second field (even field)
	30:20	**Reserved** Access: RO Format: MBZ

<table>
<tr><th colspan="3">PIPE_SCANLINE</th></tr>
<tr><td></td><td>19:0</td><td>Line Counter for Display

<table><tr><td>Access:</td><td>RO</td></tr></table>This is an indication of the current display scan line.
<table><tr><th>Programming Notes</th></tr><tr><td>The line count value is from the display output timing generator, representing the scan line currently being output to a receiver. Due to buffering within the display engine, the line being fetched (read) from the frame buffer is not directly linked to the line being output. It is possible for the fetched line to be hundreds of lines ahead of the timing generator output line.</td></tr></table></td></tr>
</table>

PIPE_SCANLINECOMP

PIPE_SCANLINECOMP	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	70004h-70007h
Name:	Pipe Scan Line Compare
ShortName:	PIPE_SCANLINECOMP_A
Reset:	soft
Address:	71004h-71007h
Name:	Pipe Scan Line Compare
ShortName:	PIPE_SCANLINECOMP_B
Reset:	soft
Address:	72004h-72007h
Name:	Pipe Scan Line Compare
ShortName:	PIPE_SCANLINECOMP_C
Reset:	soft

This register is used to initiate a display scan line compare. This MMIO driven scan line compare cannot be used at the same time as the command streamer driven scan line compare on the same pipe. When this register is written with the Initiate Compare bit set to 1b, the Display Engine (DE) will start comparing the display pipe or plane (selectable) current scan line value (current scan line) with the start scan line value (current scan line >= start scan line) and the end scan line value (current scan line <= end scan line) to decide if the pipe scan line is inside or outside the scan line window of interest. DE will wait until the current scan line is either outside (Inclusive mode) or inside (Exclusive mode) the scan line window, then trigger a scan line event and stop any further comparing. The scan line event can cause display to send a scan line compare response to the command streamer, (used for releasing a MI_WAIT_FOR_EVENT on scan line window), if unmasked in the DERRMR mask register 0x44050. The scan line event can also cause display to generate a scan line compare interrupt, if the interrupt registers are configured for that. The value programmed should be the desired value - 1, so for scan line 0, the value programmed is vertical total, and for scan line 1, the value programmed is 0. The programmable range can include the vertical blank. In interlaced display timings, the current scan line is the current line of the current interlaced field. Either MMIO or a MI_LOAD_REGISTER_IMM command can be used to unmask the scan line render response 0x44050. That can be done anytime before programming this register. There is one instance of this register per pipe.

Restriction
A new scan line compare must not be started until after the previous compare has finished. The end scan line value must be greater than or equal to the start scan line value. When using LRI care must be taken to follow all the programming rules for LRI targeting the display engine.

DWord	Bit	Description

PIPE_SCANLINECOMP

0	31	**Initiate Compare** Access: R/W This field initiates the scan line compare. When this register is written with this bit set to 1b, the display engine will do one complete comparison cycle, trigger a scan line event, then stop comparing. **Value** / **Name** 0b – Do nothing 1b – Initiate compare **Restriction** Do not write this register again until after any previous scan line compare has completed.
	30	**Inclusive Exclusive Select** Access: R/W This field selects whether the scan line compare is done in inclusive mode, where display triggers the scan line event when outside the scan line window, or inclusive mode, where display triggers when inside the window. **Value** / **Name** / **Description** 0b – Exclusive – Exclusive mode: trigger scan line event when inside the scan line window 1b – Inclusive – Inclusive mode: trigger scan line event when outside the scan line window
	29	**Counter Select** Access: R/W This field selects whether the scan line compare is done using the pipe timing generator scanline counter or a plane scanline counter. The pipe timing generator counts the scanlines being output from display. The plane counts the scan lines being fetched from the frame buffer. **Value** / **Name** / **Description** 0b – Timing generator – Use the scanline count from the pipe timing generator 1b – Plane – Use the scanline count from plane selected in PIPE_MISC2. **Programming Notes** Due to buffering within the display engine, the line being fetched from the frame buffer is not directly linked to the line being output. It is possible for the fetched line to be hundreds of lines ahead of the timing generator output line. The plane scan line count more closely represents what data is currently being fetched by the plane.

PIPE_SCANLINECOMP

	28:16	**Start Scan Line** Access: R/W This field specifies the starting scan line number of the scan line window.
	15	**Render Response Destination** Access: R/W This bit indicates what destination to send the scan line event render response to. Value / Name / Description 0b / CS / Send scan line event response to CS 1b / BCS / Send scan line event response to BCS
	14:13	**Reserved** Access: RO Format: MBZ
	12:0	**End Scan Line** Access: R/W This field specifies the ending scan line number of the scan line window.

PIPE_SEAM_EXCESS

PIPE_SEAM_EXCESS - PIPE_SEAM_EXCESS	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank OR pipe disabled
Address:	60020h-60023h
Name:	Pipe Seam Excess
ShortName:	PIPE_SEAM_EXCESS_A
Reset:	soft
Address:	61020h-61023h
Name:	Pipe Seam Excess
ShortName:	PIPE_SEAM_EXCESS_B
Reset:	soft
Address:	62020h-62023h
Name:	Pipe Seam Excess
ShortName:	PIPE_SEAM_EXCESS_C
Reset:	soft

This register defines the number of excess pixels within the Pipe window (on the right or left) that the Scaler will need to remove from the post scaled image.
When an image is split across two Pipes, scaled, and then joined at the Port, the Scalers within each Pipe will operate on a split image that contains overlap pixels around where the final seam will be to facilitate a seamless join at the Port. For example, if the left portion of an image is being scaled in Pipe A and the right portion of the image is being scaled in Pipe B, then there will be an excess number of pixels (i.e. overlap pixels) on the right side of the Pipe A image and an excess number of pixels on the left side of the Pipe B image. The overlap pixels of the window within each of the Pipes need to be dropped by the Scaler before they are delivered to the Port.
Notes:

1. Dropping of the overlap/excess pixels is done at the very end of the Pipe within the Scaler regardless of whether a Scaler is bound to the Pipe, or not.
2. The values programmed within this register are one-based (i.e. a programming of 1 equals 1 pixel of excess)
3. The values programmed within this register will be added to the Horizontal Active programming of the TRANS_HTOTAL register of the port bound to this pipe. I.e. the pipe will see a Horizontal size equal to Horizontal Active + Left Excess Amount + Right Excess Amount

PIPE_SEAM_EXCESS - PIPE_SEAM_EXCESS

Restriction:

1. The number of excess pixels cannot exceed the size of the horizontal blank, otherwise there will not be enough time to throw them away before starting the next line and the image will be corrupted
2. Pillarbox boarders must be even
3. The source size on each pipe, including pre-scale excess, must be a multiple of 2. When the Pipe output format is YUV 420 with full blend, the source size is required to be a multiple of 4.

DWord	Bit	Description
0	31:29	**Reserved** Access: RO Format: MBZ
	28:16	**Right Excess Amount** Access: Double Buffered This field defines the number of excess pixels to drop, if any, on the right side of the Pipe window
	15:13	**Reserved** Access: RO Format: MBZ
	12:0	**Left Excess Amount** Access: Double Buffered This field defines the number of excess pixels to drop, if any, on the left side of the Pipe window

PIPE_SRCSZ

PIPE_SRCSZ	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank
Address:	6001Ch-6001Fh
Name:	Pipe Source Image Size
ShortName:	PIPE_SRCSZ_A
Reset:	soft
Address:	6101Ch-6101Fh
Name:	Pipe Source Image Size
ShortName:	PIPE_SRCSZ_B
Reset:	soft
Address:	6201Ch-6201Fh
Name:	Pipe Source Image Size
ShortName:	PIPE_SRCSZ_C
Reset:	soft

There is one instance of this register for each pipe.

Programming Notes

In VGA display mode, this register is ignored and the VGA size from the VGA registers is used instead.

Restriction

Refer to the Resolution Support section for maximum size restrictions.

DWord	Bit	Description
0	31:29	**Reserved** Access: RO Format: MBZ
	28:16	**Horizontal Source Size** Access: Double Buffered This field specifies Horizontal Source Size. This determines the horizontal size of the image created by the display planes. This field is programmed to the number of pixels desired minus one.

<table>
<tr><th colspan="3">PIPE_SRCSZ</th></tr>
<tr><td></td><td></td><td>Restriction
• This register must always be programmed to the same value as the Horizontal Active, except when panel fitting is enabled, or DSC pixel replication is enabled.
  • Refer to PS_CTRL for size restrictions when panel fitting is enabled.
• Horizontal source size must always be even. The programmed value must be odd.</td></tr>
<tr><td></td><td>15:13</td><td>Reserved
<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td></td><td>12:0</td><td>Vertical Source Size
<table><tr><td>Access:</td><td>Double Buffered</td></tr></table>This field specifies Vertical Source Size. This determines the vertical size of the image created by the display planes. This field is programmed to the number of lines desired minus one.
Restriction
This register must always be programmed to the same value as the Vertical Active, except when panel fitting is enabled. Refer to PS_CTRL for size restrictions when panel fitting is enabled.</td></tr>
</table>

PIPE_STATUS

PIPE_STATUS	
Register Space:	MMIO: 0/2/0
Access:	R/WC
Size (in bits):	32
CrashLogSaved:	true
CrashLogPriority:	1
CrashLogVisibility:	public
ExternalLongName:	DE Pipe Status
ExternalDescription:	Display engine pipe status
Address:	70058h-7005Bh
Name:	Pipe Status
ShortName:	PIPE_STATUS_A
Reset:	soft
Address:	71058h-7105Bh
Name:	Pipe Status
ShortName:	PIPE_STATUS_B
Reset:	soft
Address:	72058h-7205Bh
Name:	Pipe Status
ShortName:	PIPE_STATUS_C
Reset:	soft

DWord	Bit	Description
0	31	**Underrun** Access: R/WC This field indicates that there is an underrun on the transcoder attached to this pipe.
	30	**Vblank** Access: R/WC The field is set at the start of the vertical blank of the transcoder attached to this pipe.
	29	**Frame start** Access: R/WC The field is set at the frame start of the transcoder attached to this pipe.
	28	**Not Used 28** Access: R/WC

PIPE_STATUS		
	27	**Not Used 27** Access: R/WC
	26	**Not Used 26** Access: R/WC
	25	**Not Used 25** Access: R/WC
	24	**Not Used 24** Access: R/WC
	23	**Not Used 23** Access: R/WC
	22	**Not Used 22** Access: R/WC
	21	**Not Used 21** Access: R/WC
	20	**Not Used 20** Access: R/WC
	19	**Not Used 19** Access: R/WC
	18	**Not Used 18** Access: R/WC
	17	**Not Used 17** Access: R/WC
	16	**Not Used 16** Access: R/WC
	15	**Not Used 15** Access: R/WC

PIPE_STATUS		
	14	**Not Used 14** Access: R/WC
	13	**Not Used 13** Access: R/WC
	12	**Not Used 12** Access: R/WC
	11	**Not Used 11** Access: R/WC
	10	**Not Used 10** Access: R/WC
	9	**Not Used 9** Access: R/WC
	8	**Not Used 8** Access: R/WC
	7	**Not Used 7** Access: R/WC
	6	**BW Credits Pending At VBlank** Access: R/WC A '1' indicates that the there are some pending MBUS BW-Credits at the start of VBlank. Sticky bit cleared by a write of '1'
	5	**B Credits Pending At VBlank** Access: R/WC A '1' indicates that the there are some pending MBUS B-Credits at the start of VBlank. Sticky bit cleared by a write of '1'
	4	**A Credits Pending At VBlank** Access: R/WC A '1' indicates that the there are some pending MBUS A-Credits at the start of VBlank. Sticky bit cleared by a write of '1'

PIPE_STATUS		
	3	**Not Used 3** Access: R/WC
	2	**Not used 2** Access: R/WC
	1	**Valid Block At FrameStart** Access: R/WC A '1' indicates that a valid block is still present in Display Buffer at frame start. Sticky bit cleared by a write of '1'.
	0	**Valid Block Overwritten** Access: R/WC A '1' indicates that a valid block in Display Buffer was overwritten. Sticky bit cleared by a write of '1'.

PIPEDMC_CONTROL

PIPEDMC_CONTROL - PIPEDMC_CONTROL	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	45250h-45253h
Name:	Pipe DMC Control
ShortName:	PIPEDMC_CONTROL_A
Reset:	soft
Address:	45254h-45257h
Name:	Pipe DMC Control
ShortName:	PIPEDMC_CONTROL_B
Reset:	soft
Address:	45258h-4525Bh
Name:	Pipe DMC Control
ShortName:	PIPEDMC_CONTROL_C
Reset:	soft

This Register is to add pipe DMC enable. To use pipeDMC driver must enable pipeDMC first.

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**pipedmc_enable** Access: R/W Setting this bit enables the pipeDMC.

PLANE_AUX_DIST

PLANE_AUX_DIST	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	704C0h-704C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_4_A
Reset:	soft
Address:	705C0h-705C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_5_A
Reset:	soft
Address:	714C0h-714C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_4_B
Reset:	soft
Address:	715C0h-715C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_5_B
Reset:	soft
Address:	724C0h-724C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_4_C
Reset:	soft
Address:	725C0h-725C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_5_C
Reset:	soft
Address:	701C0h-701C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_1_A
Reset:	soft

PLANE_AUX_DIST

Address:	702C0h-702C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_2_A
Reset:	soft
Address:	703C0h-703C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_3_A
Reset:	soft
Address:	711C0h-711C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_1_B
Reset:	soft
Address:	712C0h-712C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_2_B
Reset:	soft
Address:	713C0h-713C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_3_B
Reset:	soft
Address:	721C0h-721C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_1_C
Reset:	soft
Address:	722C0h-722C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_2_C
Reset:	soft
Address:	723C0h-723C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_3_C
Reset:	soft

This register is used to specify the distance from the main surface base address and the stride of the auxiliary surface. Unlike the surface base address, this register value cannot be updated through flips.

DWord	Bit	Description
0	31:12	**Auxiliary Surface Distance**

PLANE_AUX_DIST

		Access: Double Buffered When using a compressed surface, this field represents the distance of the control surface in 4K pages, where a value of [31:12] = 1 represents one 4K page.
	11:10	**Reserved** Access: RO Format: MBZ
	9:0	**Auxiliary Surface Stride** Access: Double Buffered **Description** This field is unused. Leave at default value.

PLANE_BUF_CFG

PLANE_BUF_CFG	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank, plane not enabled, or pipe not enabled
Address:	7017Ch-7017Fh
Name:	Cursor Buffer Config
ShortName:	CUR_BUF_CFG_A
Reset:	soft
Address:	7117Ch-7117Fh
Name:	Cursor Buffer Config
ShortName:	CUR_BUF_CFG_B
Reset:	soft
Address:	7217Ch-7217Fh
Name:	Cursor Buffer Config
ShortName:	CUR_BUF_CFG_C
Reset:	soft
Address:	7057Ch-7057Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_4_A
Reset:	soft
Address:	7067Ch-7067Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_5_A
Reset:	soft
Address:	7157Ch-7157Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_4_B
Reset:	soft
Address:	7167Ch-7167Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_5_B
Reset:	soft

PLANE_BUF_CFG	
Address:	7257Ch-7257Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_4_C
Reset:	soft
Address:	7267Ch-7267Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_5_C
Reset:	soft
Address:	7027Ch-7027Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_1_A
Reset:	soft
Address:	7037Ch-7037Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_2_A
Reset:	soft
Address:	7047Ch-7047Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_3_A
Reset:	soft
Address:	7127Ch-7127Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_1_B
Reset:	soft
Address:	7137Ch-7137Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_2_B
Reset:	soft
Address:	7147Ch-7147Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_3_B
Reset:	soft
Address:	7227Ch-7227Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_1_C
Reset:	soft

PLANE_BUF_CFG

Address:	7237Ch-7237Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_2_C
Reset:	soft

Address:	7247Ch-7247Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_3_C
Reset:	soft

DWord	Bit	Description
0	31:28	**Reserved** Access: RO Format: MBZ
	27	**Reserved** Access: RO Format: MBZ
	26:16	**Buffer End** Default Value: 000h Access: Double Buffered This field contains the buffer end position for this plane.
	15:12	**Reserved** Access: RO Format: MBZ
	11	**Reserved** Access: RO Format: MBZ
	10:0	**Buffer Start** Default Value: 000h Access: Double Buffered This field contains the buffer start position for this plane.

PLANE_CC_VAL

PLANE_CC_VAL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	64
_Custom_Display _DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	704B4h-704BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_4_A
Reset:	soft
Address:	705B4h-705BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_5_A
Reset:	soft
Address:	714B4h-714BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_4_B
Reset:	soft
Address:	715B4h-715BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_5_B
Reset:	soft
Address:	724B4h-724BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_4_C
Reset:	soft
Address:	725B4h-725BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_5_C
Reset:	soft
Address:	701B4h-701BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_1_A
Reset:	soft

PLANE_CC_VAL	
Address:	702B4h-702BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_2_A
Reset:	soft
Address:	703B4h-703BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_3_A
Reset:	soft
Address:	711B4h-711BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_1_B
Reset:	soft
Address:	712B4h-712BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_2_B
Reset:	soft
Address:	713B4h-713BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_3_B
Reset:	soft
Address:	721B4h-721BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_1_C
Reset:	soft
Address:	722B4h-722BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_2_C
Reset:	soft
Address:	723B4h-723BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_3_C
Reset:	soft
This register programs the clear color value to be used with render decompression. The value is used only when render decompression and clear color are both enabled in the plane control register. The register value can be updated when flipping to a new surface with new clear color value. It does not need to be updated if the new surface has the same clear color value as the previous surface.	

DWord	Bit	Description
0	31:0	**Clear Color Value DW0** Access: Double Buffered This field gives the 32 bit value of the clear color.
1	31:0	**Clear Color Value DW1** Access: Double Buffered This field gives the upper 32 bit value of the clear color. This field is used only with 64 bits formats, ignored otherwise.

PLANE_COLOR_CTL

PLANE_COLOR_CTL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	704CCh-704CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_4_A
Reset:	soft
Address:	705CCh-705CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_5_A
Reset:	soft
Address:	714CCh-714CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_4_B
Reset:	soft
Address:	715CCh-715CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_5_B
Reset:	soft
Address:	724CCh-724CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_4_C
Reset:	soft
Address:	725CCh-725CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_5_C
Reset:	soft
Address:	701CCh-701CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_1_A
Reset:	soft

PLANE_COLOR_CTL

Address:	702CCh-702CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_2_A
Reset:	soft

Address:	703CCh-703CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_3_A
Reset:	soft

Address:	711CCh-711CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_1_B
Reset:	soft

Address:	712CCh-712CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_2_B
Reset:	soft

Address:	713CCh-713CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_3_B
Reset:	soft

Address:	721CCh-721CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_1_C
Reset:	soft

Address:	722CCh-722CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_2_C
Reset:	soft

Address:	723CCh-723CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_3_C
Reset:	soft

DWord	Bit	Description
0	31	**Reserved** Access: RO Format: MBZ

PLANE_COLOR_CTL

30 Pipe Gamma Enable

Access:	Double Buffered

This bit enables pipe gamma correction for the plane pixel data.
This field is deprecated. Use 'GAMMA_MODE.Post CSC Gamma Enable' for enabling pipe gamma across all pixels from all planes.

Value	Name
0b	Disable
1b	Enable

29 Remove YUV Offset

Access:	Double Buffered

This field controls whether the plane removes or preserves the 1/2 offset on U and V components when the source pixel format is YUV and the plane YUV to RGB CSC is disabled. This bit has no effect on RGB source pixel formats

Value	Name	Description
0b	Remove	Remove 1/2 offset on UV components
1b	Preserve	Preserve 1/2 offset on UV components

28 YUV Range Correction Disable

Access:	Double Buffered

Setting this bit disables the YUV range correction logic inside the plane. The range correction logic is used to expand the compressed range YUV to full range YUV. The Y channel is expanded from the 8 bit +16 to +235 range to full range. The U and V channels are expanded from the 8 bit -112 to +112 range to full range. Extended range values will be preserved after the expansion. This bit has no effect on RGB source pixel formats since they automatically bypass range correction.

Value	Name
0b	Enable
1b	Disable

27:24 Reserved

Access:	RO
Format:	MBZ

23 Pipe CSC Enable

Access:	Double Buffered

PLANE_COLOR_CTL

		This bit enables pipe color space conversion and the pipe pre color space conversion gamma for the plane pixel data. This is separate from the color conversion logic within the plane. This field is deprecated. Use 'CSC_MODE.Pipe CSC Enable', 'GAMMA_MODE.Pre CSC Gamma Enable' for enabling pipe color space conversion and gamma respectively across all pixels from all planes. Plane CSC must be used for plane specific color space conversion. Value: 0b – Disable; 1b – Enable
	22	**Reserved** Access: Double Buffered
	21	**Plane CSC Enable** Access: Double Buffered This field enables the plane color space conversion. This field applies only to planes 1 through 3. Value: 0b – Disable; 1b – Enable
	20	**Plane Input CSC Enable** Access: Double Buffered This field enables the plane input color space conversion. This field applies only to planes 1 through 3. Value: 0b – Disable; 1b – Enable
	19:17	**Plane CSC Mode** Access: Double Buffered Description: This field specifies the mode of plane color space conversion operation. This is used only for planes 4 through 5. For planes 1 through 3, CSC is programmed in PLANE_CSC_* registers.

PLANE_COLOR_CTL

Value	Name	Description
000b	Bypass	Pixel data bypasses the plane color space conversion
001b	YUV601 to RGB601	YUV BT.601 to RGB BT.601 conversion.
010b	YUV709 to RGB709	YUV BT.709 to RGB BT.709 conversion.
011b	YUV2020 to RGB2020	YUV BT.2020 to RGB BT.2020 conversion.
100b	RGB709 to RGB2020	RGB BT.709 to RGB BT.2020 conversion.

16 **Reserved**

Access:	RO
Format:	MBZ

15 **Plane Post CSC Gamma Multi Segment Enable**

Access:	Double Buffered

This bit enables plane post CSC gamma multi segment processing. It is only used for HDR tone Mapping. It is only valid if Plane Gamma (bit[13]) is enabled.

Value	Name
1b	Enable
0b	Disable **[Default]**

14 **Plane Pre CSC Gamma Enable**

Access:	Double Buffered

This bit controls plane internal pre-CSC gamma correction.

Value	Name
1b	Enable
0b	Disable

13 **Plane Gamma Disable**

Access:	Double Buffered

This bit controls plane internal post-CSC gamma correction.

Value	Name
1b	Disable
0b	Enable

12 **Plane Gamma Mode**

Access:	Double Buffered

This field specifies the plane gamma mode of operation. This field is ignored if plane gamma is disabled.

PLANE_COLOR_CTL

Value	Name	Description
0b	Direct **[Default]**	Direct mode is used for regular plane gamma programming. Lookup is based on incoming pixel individual r, g, b values. The output is a computed by lookup of two nearest points and interpolation.
1b	Multiply	Multiple mode is used when plane gamma is used for HDR tone mapping. Lookup is based on a pseudo luminance of the incoming pixel calculated using Lin = 0.25*Red input + 0.625*Green input + 0.125*Blue input. An adjustment factor 'F' is computed by lookup of two nearest points and interpolation. Output is computed by multiplying each color channel with the adjustment factor F.

11

Plane Gamma Multiplier Precision

Access:	Double Buffered

This field specifies the plane gamma entry format in the multiplier mode. This field is ignored in the direct lookup mode. The gamma entries can be programmed in either unsigned 0.24 format or unsigned 8.16 format.

Value	Name
0b	U0.24 **[Default]**
1b	U8.16

10:6

Reserved

Access:	RO
Format:	MBZ

5:4

Alpha Mode

Access:	Double Buffered

This field controls how the plane will use per pixel alpha data from frame buffer. Constant plane alpha is defined in PLANE_KEYMSK and PLANE_KEYMAX registers.
RGB 64-bit - only alpha in 0-1 range supported with 8 bit granularity. RGB 64-bit UINT - only 8 upper bits of alpha used. RGB 2:10:10:10 - 2 bit alpha expanded out to 8 bit to give full range of opacity. XR_BIAS 10:10:10 - 2 bit alpha expanded out to 8 bit to give full range of opacity.

		Value / **Name** / **Description** 00b / Disable / Alpha channel ignored. 10b / Enable with SW pre-multiply / Alpha channel used. Color channels should be pre-multiplied with alpha by software. 11b / Enable with HW pre-multiply / Alpha channel used. Color channels will be pre-multiplied with alpha by hardware. **Restriction** Per pixel alpha is supported only with RGB pixel formats. FBC is not compatible with per pixel alpha.
	3:0	**Reserved** Access: RO Format: MBZ

PLANE_CSC_COEFF

PLANE_CSC_COEFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	192
_Custom_Display _DoubleBufferArmedBy:	Write to PLANE_SURF
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	70210h-70227h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_1_A
Reset:	soft
Address:	70310h-70327h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_2_A
Reset:	soft
Address:	70410h-70427h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_3_A
Reset:	soft
Address:	71210h-71227h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_1_B
Reset:	soft
Address:	71310h-71327h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_2_B
Reset:	soft
Address:	71410h-71427h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_3_B
Reset:	soft
Address:	72210h-72227h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_1_C
Reset:	soft

PLANE_CSC_COEFF

Address:	72310h-72327h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_2_C
Reset:	soft

Address:	72410h-72427h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_3_C
Reset:	soft

Programming Notes

Refer to Color Space Conversion page for programming details and examples.

DWord	Bit	Description
0	31:16	**RY** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**GY** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
1	31:16	**BY** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**Reserved** Access: RO Format: MBZ
2	31:16	**RU** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**GU** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**

<table>
<tr><th colspan="3">PLANE_CSC_COEFF</th></tr>
<tr><td>3</td><td>31:16</td><td>BU
<table><tr><td>Access:</td><td>Double Buffered</td></tr><tr><td>Format:</td><td>CSC COEFFICIENT FORMAT</td></tr></table></td></tr>
<tr><td></td><td>15:0</td><td>Reserved
<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td>4</td><td>31:16</td><td>RV
<table><tr><td>Access:</td><td>Double Buffered</td></tr><tr><td>Format:</td><td>CSC COEFFICIENT FORMAT</td></tr></table></td></tr>
<tr><td></td><td>15:0</td><td>GV
<table><tr><td>Access:</td><td>Double Buffered</td></tr><tr><td>Format:</td><td>CSC COEFFICIENT FORMAT</td></tr></table></td></tr>
<tr><td>5</td><td>31:16</td><td>BV
<table><tr><td>Access:</td><td>Double Buffered</td></tr><tr><td>Format:</td><td>CSC COEFFICIENT FORMAT</td></tr></table></td></tr>
<tr><td></td><td>15:0</td><td>Reserved
<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
</table>

PLANE_CSC_POSTOFF

PLANE_CSC_POSTOFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	96
_Custom_Display _DoubleBufferArmedBy:	Write to PLANE_SURF
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	70234h-7023Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_1_A
Reset:	soft
Address:	70334h-7033Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_2_A
Reset:	soft
Address:	70434h-7043Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_3_A
Reset:	soft
Address:	71234h-7123Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_1_B
Reset:	soft
Address:	71334h-7133Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_2_B
Reset:	soft
Address:	71434h-7143Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_3_B
Reset:	soft
Address:	72234h-7223Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_1_C
Reset:	soft

PLANE_CSC_POSTOFF

Address:	72334h-7233Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_2_C
Reset:	soft

Address:	72434h-7243Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_3_C
Reset:	soft

The post-offset is intended to add an offset from 0 on the Y or RGB channels and to convert UV channels from 2's complement to excess 0.5 as they exit plane color space conversion (CSC).

DWord	Bit	Description
0	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PostCSC High Offset** Access: Double Buffered This value is used to give an offset to the high color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
1	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PostCSC Medium Offset** Access: Double Buffered This value is used to give an offset to the medium color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
2	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PostCSC Low Offset** Access: Double Buffered This value is used to give an offset to the low color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).

PLANE_CSC_PREOFF

PLANE_CSC_PREOFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	96
_Custom_Display _DoubleBufferArmedBy:	Write to PLANE_SURF
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	70228h-70233h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_1_A
Reset:	soft
Address:	70328h-70333h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_2_A
Reset:	soft
Address:	70428h-70433h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_3_A
Reset:	soft
Address:	71228h-71233h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_1_B
Reset:	soft
Address:	71328h-71333h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_2_B
Reset:	soft
Address:	71428h-71433h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_3_B
Reset:	soft
Address:	72228h-72233h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_1_C
Reset:	soft

PLANE_CSC_PREOFF

Address:	72328h-72333h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_2_C
Reset:	soft

Address:	72428h-72433h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_3_C
Reset:	soft

The pre-offset is intended to remove an offset from 0 on the Y or RGB channels and to convert UV channels from excess 0.5 to 2's complement as they enter plane color space conversion (CSC).
RGB modes:Red is in the High channel, Green in Medium, and Blue in Low.
YUV modes:V is in the High channel, Y in Medium, and U in Low.

DWord	Bit	Description
0	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PreCSC High Offset** Access: Double Buffered This value is used to give an offset to the high color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
1	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PreCSC Medium Offset** Access: Double Buffered This value is used to give an offset to the medium color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
2	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PreCSC Low Offset** Access: Double Buffered This value is used to give an offset to the low color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).

PLANE_CTL

PLANE_CTL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	70480h-70483h
Name:	Plane Control
ShortName:	PLANE_CTL_4_A
Reset:	soft
Address:	70580h-70583h
Name:	Plane Control
ShortName:	PLANE_CTL_5_A
Reset:	soft
Address:	71480h-71483h
Name:	Plane Control
ShortName:	PLANE_CTL_4_B
Reset:	soft
Address:	71580h-71583h
Name:	Plane Control
ShortName:	PLANE_CTL_5_B
Reset:	soft
Address:	72480h-72483h
Name:	Plane Control
ShortName:	PLANE_CTL_4_C
Reset:	soft
Address:	72580h-72583h
Name:	Plane Control
ShortName:	PLANE_CTL_5_C
Reset:	soft
Address:	70180h-70183h
Name:	Plane Control
ShortName:	PLANE_CTL_1_A
Reset:	soft

PLANE_CTL

Address:	70280h-70283h
Name:	Plane Control
ShortName:	PLANE_CTL_2_A
Reset:	soft

Address:	70380h-70383h
Name:	Plane Control
ShortName:	PLANE_CTL_3_A
Reset:	soft

Address:	71180h-71183h
Name:	Plane Control
ShortName:	PLANE_CTL_1_B
Reset:	soft

Address:	71280h-71283h
Name:	Plane Control
ShortName:	PLANE_CTL_2_B
Reset:	soft

Address:	71380h-71383h
Name:	Plane Control
ShortName:	PLANE_CTL_3_B
Reset:	soft

Address:	72180h-72183h
Name:	Plane Control
ShortName:	PLANE_CTL_1_C
Reset:	soft

Address:	72280h-72283h
Name:	Plane Control
ShortName:	PLANE_CTL_2_C
Reset:	soft

Address:	72380h-72383h
Name:	Plane Control
ShortName:	PLANE_CTL_3_C
Reset:	soft

The pipe scaler can be attached to a plane to scale the plane output before blending.

Restriction
Refer to 'Plane Capability and Interoperability' page for plane capabilities and restrictions.

DWord	Bit	Description

PLANE_CTL

0:31 — Plane Enable

Access:	Double Buffered

When this bit is set, the plane will generate pixels for display. When cleared to zero, plane memory fetches cease, and plane output is transparent.

Value	Name
0b	Disable
1b	Enable

30:28 — Pipe Slice Arbitration Slots

Access:	Double Buffered

This field specifies the number of slots allocated to this plane in pipe slice request arbitration. This field is ignored when the 'PIPE_SLICE_ARBITRATION_CTL->Use Programmed Slots' is not set. This field is zero based; a programmed value of 0 results in 1 slot allocation.

27:23 — Source Pixel Format

Access:	Double Buffered

This field selects the source pixel format for the plane. Before entering the blender, each source format is converted to the pipe pixel format. The 8-bpp indexed format will always use the pipe palette.
In planar YUV formats Y samples appear first in memory followed by interleaved UV samples.
YUV 4:2:2 byte order is programmed separately. YUV 4:2:0 and YUV 4:4:4 byte order is not programmable.
RGB color order is programmed separately for some formats.
Refer to Universal Plane, Plane Pixel Formats section for color channel bit mappings.

YUV 4:2:0 P010, P012 and P016 formats share the same 16 bpc memory layout but use 10, 12 and 16 bits per channel respectively. The color values are stored in the most significant bits.

64-bit formats supported only on the HDR planes.
P01x output is only allowed from HDR planes.

Value	Name	Description
00000b	YUV 422 Packed 8 bpc	YUV 4:2:2 packed, 8 bpc
00010b	YUV 420 Planar 8 bpc	YUV 4:2:0 Planar, 8 bpc - NV12
00100b	RGB 2101010	RGB 2:10:10:10, 32 bit.
00110b	YUV 420 Planar 10 bpc	YUV 4:2:0 Planar, 10 bpc - P010
01000b	RGB 8888	RGB 8:8:8:8, 32 bit

01010b	YUV 420 Planar 12 bpc	YUV 4:2:0 Planar 12 bpc - P012
01100b	RGB 16161616 Float	RGB 16:16:16:16 Floating Point, 64 bit (FP16)
01110b	YUV 420 Planar 16 bpc	YUV 4:2:0 Planar, 16 bpc - P016
10000b	YUV 444 Packed 8 bpc	YUV 4:4:4 packed (MSB-X:Y:U:V), 8bpc
10100b	RGB 2101010 XR_BIAS	RGB 2:10:10:10 Extended Range Bias (MSB-X:B:G:R), 32 bit
11000b	Indexed 8 bit	Indexed 8-bit
11100b	RGB 565	RGB 5:6:5 (MSB-R:G:B), 16 bit
00001b	YUV 422 Packed 10 bpc	YUV 4:2:2 packed, 10 bpc - Y210
00011b	YUV 422 Packed 12 bpc	YUV 4:2:2 packed, 12 bpc - Y212
00101b	YUV 422 Packed 16 bpc	YUV 4:2:2 packed, 16 bpc - Y216
00111b	YUV 444 Packed 10 bpc	YUV 4:4:4 packed (MSB-X:V:Y:U), 10 bpc - Y410
01001b	YUV 444 Packed 12 bpc	YUV 4:4:4 packed (MSB-X:V:Y:U), 12 bpc - Y412
01011b	YUV 444 Packed 16 bpc	YUV 4:4:4 packed (MSB-X:V:Y:U), 16 bpc - Y416

Restriction
Plane scaling is not compatible with the Indexed 8-bit, XR_BIAS source pixel formats.

22:21

Key Enable

Access:	Double Buffered

This field enables color keying. The key color, range, channel enables, and mask are programmed in PLANE_KEYVAL, PLANE_KEYMSK, and PLANE_KEYMAX.

Value	Name	Description
00b	Disable	Disable keying for this plane.
01b	Source Key Enable	This plane's pixels will be checked for a key match. The blend between this plane and the plane below will treat the key matched pixels as transparent.

10b	Destination Key Enable	This plane's pixels will be checked for a key match. The blend between this plane and the plane above will treat the pixels above as opaque only where this plane is key matched, and the plane above is opaque. When plane gamma is enabled, the gamma processing may shift the pixel color values sent to blender and may cause it to not match the key color as desired. The recommendation is to use the pipe gamma when destination keying is enabled.
11b	Source Key Window Enable	This plane's pixels will be checked for a key match. The blend between this plane and the plane below will treat the key matched pixels as transparent only where the plane below is opaque.

Restriction
Plane color keying is not compatible with the Indexed 8-bit pixel format. Destination key/Source Key Window should be enabled only on one set (a pair) of planes, per pipe, at a time. Source key and Source Key Window must not be enabled on the bottom most active plane. Destination key must not be enabled on the topmost active plane.

20 **RGB Color Order**

Access:	Double Buffered

This field is used to select the color order when using RGB data formats, except RGB 32-bit XR_BIAS 10:10:10 and 16-bit BGRX 5:6:5. For other formats, this field is ignored.

Value	Name	Description
0b	BGRX	BGRX (MSB-X:R:G:B)
1b	RGBX	RGBX (MSB-X:B:G:R)

19 **Planar YUV420 component**

Access:	Double Buffered

This field selects the planar YUV420 component for the plane when NV12/P0xx source pixel formats is used. This field must be set to '0b' for other (YUV non-planar/RGB) surface formats.

Value	Name	Description
0b	UV	Planes 1 to 3 can be configured as UV plane. Planes 4 and 5 must not be configured as a UV plane.
1b	Y	Planes 4 and 5 can be configured as Y plane. Planes 1 to 3 must not be configured as a Y plane.

PLANE_CTL

18	**Reserved** Access: RO Format: MBZ
17:16	**YUV 422 Byte Order** Access: Double Buffered This field is used to select the byte order for YUV 4:2:2 8bpc data formats. For other formats, this field is ignored. **Value / Name / Description** 00b / YUYV / YUYV (MSB-V:Y2:U:Y1) 01b / UYVY / UYVY (MSB-Y2:V:Y1:U) 10b / YVYU / YVYU (MSB-U:Y2:V:Y1) 11b / VYUY / VYUY (MSB-Y2:U:Y1:V)
15	**Render Decomp** Access: Double Buffered This bit enables the Display decompression of Render compressed surfaces. **Value / Name** 0b / Disable 1b / Enable **Restriction** Color Clear is supported. Only the Left-right cache-line pair decompression is supported. The compressed surface should be Y (Legacy) or Y F Tiled. Decompression is not supported with 90/270 degree rotation. Decompression is supported with RGB8888, RGB1010102 and FP16 formats. Decompression is supported on all planes and pipes.
14	**Reserved** Access: RO Format: MBZ
13	**Clear Color Disable** Access: Double Buffered This field disables the render decompression clear color mode. It is ignored when the Render Decomp field is disabled. The color value must be programmed in PLANE_CC_VAL before flipping to the surface that uses clear color value.

PLANE_CTL

Value	Name
1b	Disable
0b	Enable **[Default]**

12:10 **Tiled Surface**

Access:	Double Buffered

This field indicates that the surface data is in tiled memory. This bit may be updated through MMIO writes or through a command streamer initiated synchronous flip.

Value	Name
000b	Linear memory
001b	Tile X memory
100b	Tile Y (Legacy) memory

Restriction
Interlaced mode is not supported with Y Tiling. Tile Ys is not supported.

9 **Async Address Update Enable**

Access:	R/W

This bit will enable asynchronous updates of the plane surface address when written by MMIO (MMIO asynchronous flips). The surface address will change as soon as possible. This bit is not double buffered, and the changes will apply immediately. When performing an asynchronous update, only the plane surface can be updated. Changes to stride, pixel, format, compression, FBC, etc. are not allowed.

Value	Name	Description
0b	Sync	Surface Address MMIO writes will update synchronous to start of vertical blank
1b	Async	Surface Address MMIO writes will update asynchronous to start of vertical blank

Restriction
No command streamer (ring) flips to this plane are allowed when this bit is enabled. Command streamer flips will set a similar bit in the flip message that it sends to display.
Asynchronous S3D flips are not allowed.
Each async surface address write must be followed by a wait for flip done indication before writing the surface address register again.

PLANE_CTL

	8	**Horizontal Flip** Access: Double Buffered This field controls the horizontal flipping of the plane. When horizontal flipping is enabled with rotation, the horizontal flip operation is logically performed first followed by rotation. For further information refer to "Universal Plane" section. **Value** / **Name** 0b: Disable **[Default]** 1b: Enable **Restriction** Horizontal flip is not supported with linear surface formats.
	7:6	**Stereo Surface Vblank Mask** Access: Double Buffered This field controls which vertical blank (left eye, right eye, or both) will be used for the plane surface address double-buffering during stereo 3D mode. This field is ignored when not in stereo 3D mode. **Value** / **Name** / **Description** 00b: Mask None: Both the left and right eye vertical blanks will be used. 01b: Mask Left: Mask the left eye vertical blank. Only the right eye vertical blank will be used. 10b: Mask Right: Mask the right eye vertical blank. Only the left eye vertical blank will be used.
	5	**Reserved** Access: Double Buffered
	4	**Media Decomp** Access: Double Buffered This bit enables the Display decompression of Media compressed surfaces. 'Media Decomp' and 'Render Decomp' are mutually exclusive and must not enabled at the same time for a given plane. Media decompression is supported with NV12, P0xx, YUV422, YUV444, RGB8888, RGB1010102 and FP16 formats. **Value** / **Name** 0b: Disable 1b: Enable

PLANE_CTL

3 — Allow Double Buffer Update Disable

Access:	R/W

This field controls whether double buffer updates are allowed to be disabled for this plane. The DOUBLE_BUFFER_CTL register can be configured to globally disable double buffer updates for resources that allow them to be disabled. This field applies only to the plane registers that supports double buffering. Scaler registers used for plane scaling purposes are not included in this.

Value	Name
0b	Not Allowed
1b	Allowed **[Default]**

2 — Reserved

Access:	RO
Format:	MBZ

1:0 — Plane Rotation

Access:	Double Buffered

This field controls hardware rotation of the plane.

Value	Name
00b	No rotation
01b	90 degree rotation
10b	180 degree rotation
11b	270 degree rotation

Programming Notes
Hardware does not change the plane position when rotation is enabled. Software may need to adjust the plane position to match the physical orientation of the display.

Restriction
90/270 degree rotation requires the surface to be Y Tiled. Interlaced mode is not supported with 90/270 degree rotation. Render-Display decompression is not supported with 90/270 degree rotation.
90/270 rotation is supported with plane width (pre-rotation) up to 4096 pixels.

PLANE_CUS_CTL

PLANE_CUS_CTL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	701C8h-701CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_1_A
Reset:	soft
Address:	702C8h-702CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_2_A
Reset:	soft
Address:	703C8h-703CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_3_A
Reset:	soft
Address:	711C8h-711CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_1_B
Reset:	soft
Address:	712C8h-712CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_2_B
Reset:	soft
Address:	713C8h-713CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_3_B
Reset:	soft
Address:	721C8h-721CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_1_C
Reset:	soft

PLANE_CUS_CTL

Address:	722C8h-722CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_2_C
Reset:	soft

Address:	723C8h-723CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_3_C
Reset:	soft

Description

This register programs the chroma upsampler for processing pixel streams from hybrid planar YUV 420 (NV12, P0xx) surfaces.
This dedicated chroma upsampling capability is available only in Planes 1 through 3.
The following table shows phase programming for frequently used YUV420 to YUV444 chroma upsampling scenarios where the chroma is being filtered to the top left of the pixel.

YUV 420Chroma Siting	Horz Phase	Vert Phase	Programmed Horz Initial Phase	Programmed Horz Initial Phase Sign	Programmed Vert Initial Phase	Programmed Vert Initial Phase Sign
Top Left	0	0	0	0	0	0
Top	-0.25	0	0.25	1	0	0
Left (MPEG-2)	0	-0.25	0	0	0.25	1
Center (MPEG-1)	-0.25	-0.25	0.25	1	0.25	1

Restriction : When the Chroma upsampler is enabled, then:

1. The maximum horizontal plane size allowed is 4096 pixels
2. The minimum horizontal plane size allowed is 8 pixels
3. The minimum vertical plane size allowed is 4 lines
4. The horizontal and vertical plane size should be even

DWord	Bit	Description
0	31	**Chroma Upsampler Enable** Access: Double Buffered This field enables the plane chroma upsampler for handling hybrid planar YUV 420 (NV12, P0xx) formats. 0b – Disable 1b – Enable

PLANE_CUS_CTL

	30	**Y Binding** Access: Double Buffered This field defines the Y plane from where the chroma upsampler will receive the Y pixels stream when processing hybrid planar YUV 420 (NV12, P0xx) formats. Value: 0b — Name: Plane 4 Value: 1b — Name: Plane 5
	29:24	**Reserved** Access: RO Format: MBZ
	23	**Reserved** Access: Double Buffered
	22	**Reserved** Access: RO Format: MBZ
	21:20	**Reserved** Access: Double Buffered
	19	**Horz Initial Phase Sign** Access: Double Buffered This field defines the direction of the horizontal initial phase adjustment on the UV stream during upsampling. A positive initial phase will have an effect of shifting the UV pixels to the right with respect to the Y pixels whereas a negative initial phase will have an effect of shifting left. The sign bit must be zero if the initial phase is zero. Value: 0b — Name: Positive Initial Phase Value: 1b — Name: Negative Initial Phase
	18	**Reserved** Access: RO Format: MBZ

PLANE_CUS_CTL

	17:16	**Horz Initial Phase** Access: Double Buffered This field defines the horizontal initial phase adjustment required on the UV stream during upsampling. This field should be programmed based on the YUV 420 chroma siting. **Value** / **Name** 00b: 0 01b: 0.25 10b: 0.5 11b: Reserved
	15	**Vert Initial Phase Sign** Access: Double Buffered This field defines the direction of the vertical initial phase adjustment on the UV stream during upsampling. A positive initial phase will have an effect of shifting the UV pixels down with respect to the Y pixels whereas a negative initial phase will have an effect of shifting up. The sign bit must be zero if the initial phase is zero. **Value** / **Name** 0b: Positive Initial Phase 1b: Negative Initial Phase
	14	**Reserved** Access: RO Format: MBZ
	13:12	**Vert Initial Phase** Access: Double Buffered This field defines the vertical initial phase adjustment required on the UV stream during upsampling. This field should be programmed based on the YUV 420 chroma siting. **Value** / **Name** 00b: 0 01b: 0.25 10b: 0.5 11b: Reserved
	11	**Reserved** Access: Double Buffered

PLANE_CUS_CTL		
	10:9	**Power Up Delay** Access: Double Buffered This field indicates the wait (in CD clocks) between powering up the line buffer arrays.
	8	**Reserved** Access: Double Buffered
	7:6	**Reserved** Access: RO Format: MBZ
	5	**ECC Single Error** Access: R/WC This field indicates that a single bit error encountered at the ECC logic. Hardware will correct the single bit errors. Hardware will set the bit; SW can clear with a write of 1.
	4	**ECC Double Error** Access: R/WC This field indicates that a double bit error encountered at the ECC logic. Hardware will not correct the double bit errors. Hardware will set the bit; SW can clear with a write of 1.
	3:1	**Reserved** Access: RO Format: MBZ
	0	**Power Up In Progress** Access: RO This field is set when the chroma upsampler line buffers are being powered up. Chroma upsampler cannot handle pixel traffic when this bit is set.

PLANE_INPUT_CSC_COEFF

PLANE_INPUT_CSC_COEFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	192
_Custom_Display _DoubleBufferArmedBy:	Write to PLANE_SURF
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	701E0h-701F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_1_A
Reset:	soft
Address:	702E0h-702F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_2_A
Reset:	soft
Address:	703E0h-703F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_3_A
Reset:	soft
Address:	711E0h-711F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_1_B
Reset:	soft
Address:	712E0h-712F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_2_B
Reset:	soft
Address:	713E0h-713F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_3_B
Reset:	soft
Address:	721E0h-721F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_1_C
Reset:	soft

PLANE_INPUT_CSC_COEFF

Address:	722E0h-722F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_2_C
Reset:	soft

Address:	723E0h-723F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_3_C
Reset:	soft

DWord	Bit	Description
0	31:16	**RY** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**GY** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
1	31:16	**BY** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**Reserved** Access: RO Format: MBZ
2	31:16	**RU** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**GU** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
3	31:16	**BU** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**

PLANE_INPUT_CSC_COEFF		
	15:0	**Reserved** Access: RO Format: MBZ
4	31:16	**RV** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**GV** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
5	31:16	**BV** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**Reserved** Access: RO Format: MBZ

PLANE_INPUT_CSC_POSTOFF

PLANE_INPUT_CSC_POSTOFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	96
_Custom_Display _DoubleBufferArmedBy:	Write to PLANE_SURF
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	70204h-7020Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_1_A
Reset:	soft
Address:	70304h-7030Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_2_A
Reset:	soft
Address:	70404h-7040Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_3_A
Reset:	soft
Address:	71204h-7120Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_1_B
Reset:	soft
Address:	71304h-7130Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_2_B
Reset:	soft
Address:	71404h-7140Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_3_B
Reset:	soft
Address:	72204h-7220Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_1_C
Reset:	soft

PLANE_INPUT_CSC_POSTOFF

Address:	72304h-7230Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_2_C
Reset:	soft

Address:	72404h-7240Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_3_C
Reset:	soft

The post-offset is intended to add an offset from 0 on the Y or RGB channels and to convert UV channels from 2's complement to excess 0.5 as they exit plane input color space conversion (CSC).

DWord	Bit	Description
0	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PostCSC High Offset** Access: Double Buffered This value is used to give an offset to the high color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
1	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PostCSC Medium Offset** Access: Double Buffered This value is used to give an offset to the medium color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
2	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PostCSC Low Offset** Access: Double Buffered This value is used to give an offset to the low color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).

PLANE_INPUT_CSC_PREOFF

PLANE_INPUT_CSC_PREOFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	96
_Custom_Display _DoubleBufferArmedBy:	Write to PLANE_SURF
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	701F8h-70203h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_1_A
Reset:	soft
Address:	702F8h-70303h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_2_A
Reset:	soft
Address:	703F8h-70403h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_3_A
Reset:	soft
Address:	711F8h-71203h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_1_B
Reset:	soft
Address:	712F8h-71303h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_2_B
Reset:	soft
Address:	713F8h-71403h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_3_B
Reset:	soft
Address:	721F8h-72203h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_1_C
Reset:	soft

PLANE_INPUT_CSC_PREOFF

Address:	722F8h-72303h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_2_C
Reset:	soft

Address:	723F8h-72403h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_3_C
Reset:	soft

The pre-offset is intended to remove an offset from 0 on the Y or RGB channels and to convert UV channels from excess 0.5 to 2's complement as they enter plane input color space conversion (CSC).

DWord	Bit	Description
0	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PreCSC High Offset** Access: Double Buffered This value is used to give an offset to the high color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
1	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PreCSC Medium Offset** Access: Double Buffered This value is used to give an offset to the medium color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
2	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PreCSC Low Offset** Access: Double Buffered This value is used to give an offset to the low color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).

PLANE_KEYMAX

PLANE_KEYMAX	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank, pipe not enabled, or plane not enabled
Address:	704A0h-704A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_4_A
Reset:	soft
Address:	705A0h-705A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_5_A
Reset:	soft
Address:	714A0h-714A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_4_B
Reset:	soft
Address:	715A0h-715A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_5_B
Reset:	soft
Address:	724A0h-724A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_4_C
Reset:	soft
Address:	725A0h-725A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_5_C
Reset:	soft
Address:	701A0h-701A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_1_A
Reset:	soft

PLANE_KEYMAX	
Address:	702A0h-702A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_2_A
Reset:	soft
Address:	703A0h-703A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_3_A
Reset:	soft
Address:	711A0h-711A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_1_B
Reset:	soft
Address:	712A0h-712A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_2_B
Reset:	soft
Address:	713A0h-713A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_3_B
Reset:	soft
Address:	721A0h-721A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_1_C
Reset:	soft
Address:	722A0h-722A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_2_C
Reset:	soft
Address:	723A0h-723A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_3_C
Reset:	soft

When plane source is YUV, this register specifies the maximum YUV key value to be used together with the minimum YUV key value and the channel enables to determine if the plane matches the key. When plane source is RGB, this register is not used.

DWord	Bit	Description

PLANE_KEYMAX		
0	31:24	**Plane Alpha Value** Access: Double Buffered Specifies the plane alpha value when plane alpha is enabled in PLANE_KEYMSK register.
	23:16	**V Key Max Value** Access: Double Buffered Specifies the maximum key value for the V channel.
	15:8	**Y Key Max Value** Access: Double Buffered Specifies the maximum key value for the Y channel.
	7:0	**U Key Max Value** Access: Double Buffered Specifies the maximum key value for the U channel.

PLANE_KEYMSK

PLANE_KEYMSK	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank, pipe not enabled, or plane not enabled
Address:	70498h-7049Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_4_A
Reset:	soft
Address:	70598h-7059Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_5_A
Reset:	soft
Address:	71498h-7149Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_4_B
Reset:	soft
Address:	71598h-7159Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_5_B
Reset:	soft
Address:	72498h-7249Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_4_C
Reset:	soft
Address:	72598h-7259Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_5_C
Reset:	soft
Address:	70198h-7019Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_1_A
Reset:	soft

PLANE_KEYMSK		
Address:	70298h-7029Bh	
Name:	Plane Key Mask	
ShortName:	PLANE_KEYMSK_2_A	
Reset:	soft	
Address:	70398h-7039Bh	
Name:	Plane Key Mask	
ShortName:	PLANE_KEYMSK_3_A	
Reset:	soft	
Address:	71198h-7119Bh	
Name:	Plane Key Mask	
ShortName:	PLANE_KEYMSK_1_B	
Reset:	soft	
Address:	71298h-7129Bh	
Name:	Plane Key Mask	
ShortName:	PLANE_KEYMSK_2_B	
Reset:	soft	
Address:	71398h-7139Bh	
Name:	Plane Key Mask	
ShortName:	PLANE_KEYMSK_3_B	
Reset:	soft	
Address:	72198h-7219Bh	
Name:	Plane Key Mask	
ShortName:	PLANE_KEYMSK_1_C	
Reset:	soft	
Address:	72298h-7229Bh	
Name:	Plane Key Mask	
ShortName:	PLANE_KEYMSK_2_C	
Reset:	soft	
Address:	72398h-7239Bh	
Name:	Plane Key Mask	
ShortName:	PLANE_KEYMSK_3_C	
Reset:	soft	
DWord	**Bit**	**Description**

PLANE_KEYMSK

0	31	**Plane Alpha Enable** Access: Double Buffered Enables the plane alpha. Color channels will be pre-multiplied by hardware with the plane alpha value from PLANE_KEYMAX register. Per-pixel alpha is defined in the PLANE_COLOR_CTL register. Value: 0b — Disable Value: 1b — Enable
	30:27	**Reserved** Access: RO Format: MBZ
	26	**V or R Key Channel Enable** Access: Double Buffered Enables the V/Red channel for key comparison. A disabled channel will be ignored when determining a key match. Value: 0b — Disable Value: 1b — Enable
	25	**Y or G Key Channel Enable** Access: Double Buffered Enables the Y/Green channel for key comparison. A disabled channel will be ignored when determining a key match. Value: 0b — Disable Value: 1b — Enable
	24	**U or B Key Channel Enable** Access: Double Buffered Enables the U/Blue channel for key comparison. A disabled channel will be ignored when determining a key match. Value: 0b — Disable Value: 1b — Enable

PLANE_KEYMSK		
	23:16	**R Key Mask Value** Access: Double Buffered Specifies the key mask for the Red channel. A zero bit in the mask indicates that the corresponding bit will be ignored when determining a key match.
	15:8	**G Key Mask Value** Access: Double Buffered Specifies the key mask for the Green channel. A zero bit in the mask indicates that the corresponding bit will be ignored when determining a key match.
	7:0	**B Key Mask Value** Access: Double Buffered Specifies the key mask for the Blue channel. A zero bit in the mask indicates that the corresponding bit will be ignored when determining a key match.

PLANE_KEYVAL

PLANE_KEYVAL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank, pipe not enabled, or plane not enabled
Address:	70494h-70497h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_4_A
Reset:	soft
Address:	70594h-70597h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_5_A
Reset:	soft
Address:	71494h-71497h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_4_B
Reset:	soft
Address:	71594h-71597h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_5_B
Reset:	soft
Address:	72494h-72497h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_4_C
Reset:	soft
Address:	72594h-72597h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_5_C
Reset:	soft
Address:	70194h-70197h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_1_A
Reset:	soft

PLANE_KEYVAL	
Address:	70294h-70297h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_2_A
Reset:	soft
Address:	70394h-70397h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_3_A
Reset:	soft
Address:	71194h-71197h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_1_B
Reset:	soft
Address:	71294h-71297h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_2_B
Reset:	soft
Address:	71394h-71397h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_3_B
Reset:	soft
Address:	72194h-72197h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_1_C
Reset:	soft
Address:	72294h-72297h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_2_C
Reset:	soft
Address:	72394h-72397h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_3_C
Reset:	soft

PLANE_KEYVAL

When plane source is YUV, this register specifies the minimum YUV key value to be used together with the maximum YUV key value and the channel enables to determine if the plane matches the key. When plane source is RGB, this register specifies the RGB key value to be used together with the channel masks to determine if the plane matches the key. RGB key matches can only occur for positive pixel values in the 0 to 1 range. Extended range pixel values will not match. MSB bits are used for comparison.

Restriction: Keying is not supported in HDR mode.

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23:16	**V Min or R Key Value** Access: Double Buffered Specifies the minimum key value for the V channel or the compare value for Red channel.
	15:8	**Y Min or G Key Value** Access: Double Buffered Specifies the minimum key value for the Y channel or the compare value for Green channel.
	7:0	**U Min or B Key Value** Access: Double Buffered Specifies the minimum key value for the U channel or the compare value for Blue channel.

PLANE_LEFT_SURF

PLANE_LEFT_SURF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display _DoubleBufferUpdatePoint:	Start of left or right eye vertical blank (selectable), pipe not enabled. or plane not enabled; after armed
Address:	704B0h-704B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_4_A
Reset:	soft
Address:	705B0h-705B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_5_A
Reset:	soft
Address:	714B0h-714B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_4_B
Reset:	soft
Address:	715B0h-715B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_5_B
Reset:	soft
Address:	724B0h-724B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_4_C
Reset:	soft
Address:	725B0h-725B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_5_C
Reset:	soft
Address:	701B0h-701B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_1_A
Reset:	soft

PLANE_LEFT_SURF

Address:	702B0h-702B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_2_A
Reset:	soft
Address:	703B0h-703B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_3_A
Reset:	soft
Address:	711B0h-711B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_1_B
Reset:	soft
Address:	712B0h-712B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_2_B
Reset:	soft
Address:	713B0h-713B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_3_B
Reset:	soft
Address:	721B0h-721B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_1_C
Reset:	soft
Address:	722B0h-722B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_2_C
Reset:	soft
Address:	723B0h-723B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_3_C
Reset:	soft

Restriction
This register must be programmed with a valid address prior to enabling stereo 3D on this pipe.

DWord	Bit	Description

<table>
<tr><th colspan="3">PLANE_LEFT_SURF</th></tr>
<tr><td rowspan="2">0</td><td>31:12</td><td>Left Surface Base Address

<table><tr><td>Access:</td><td>Double Buffered</td></tr><tr><td>Format:</td><td>GraphicsAddress[31:12]</td></tr></table>This address specifies the stereo 3D left eye surface base address bits 31:12.
<table><tr><th>Restriction</th></tr><tr><td>This surface must have the same stride, tiling, and panning offset parameters as the right eye surface and meet all the same restrictions.</td></tr></table></td></tr>
<tr><td>11:0</td><td>Reserved

<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
</table>

PLANE_OFFSET

PLANE_OFFSET	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank, pipe not enabled, or plane not enabled
Address:	704A4h-704A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_4_A
Reset:	soft
Address:	705A4h-705A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_5_A
Reset:	soft
Address:	714A4h-714A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_4_B
Reset:	soft
Address:	715A4h-715A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_5_B
Reset:	soft
Address:	724A4h-724A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_4_C
Reset:	soft
Address:	725A4h-725A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_5_C
Reset:	soft
Address:	701A4h-701A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_1_A
Reset:	soft

PLANE_OFFSET	
Address:	702A4h-702A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_2_A
Reset:	soft
Address:	703A4h-703A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_3_A
Reset:	soft
Address:	711A4h-711A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_1_B
Reset:	soft
Address:	712A4h-712A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_2_B
Reset:	soft
Address:	713A4h-713A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_3_B
Reset:	soft
Address:	721A4h-721A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_1_C
Reset:	soft
Address:	722A4h-722A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_2_C
Reset:	soft
Address:	723A4h-723A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_3_C
Reset:	soft
Address:	7089Ch-7089Fh
Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_1_A
Reset:	soft

PLANE_OFFSET

Address:	708BCh-708BFh
Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_2_A
Reset:	soft

Address:	708DCh-708DFh
Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_3_A
Reset:	soft

Address:	708FCh-708FFh
Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_4_A
Reset:	soft

Address:	7092Ch-7092Fh
Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_5_A
Reset:	soft

This register specifies the panning for the plane surface. The start position is specified in this register as a (x, y) offset from the beginning of the surface. When performing 180 rotation, hardware will internally add the plane size to the offsets so the plane will start displaying from the bottom right corner of the image.

Restriction

Plane Size + Plane Offset should not exceed the surface <stride/width> (in pixels)
X and Y offset restrictions are specified in the following table. For formats not specified in the table, both odd and even offsets are supported.

PixelFormat	Rotate	Start X Position	Start Y Position
YUV 420 Planar - NV12	All	Even	Even
YUV 420 Planar - P01x	All	Even	Even
YUV 422	All	Even	Even

DWord	Bit	Description
0	31:29	**Reserved** Access: RO Format: MBZ
	28:16	**Start Y Position** Access: Double Buffered The Start Y Position or the Y Offset is the vertical offset in lines of the beginning of the active display plane relative to the display surface.

PLANE_OFFSET		
	15:13	**Reserved** Access: RO Format: MBZ
	12:0	**Start X Position** Access: Double Buffered The Start X Position or the X Offset is the horizontal offset in pixels of the beginning of the active display plane relative to the display surface.

PLANE_PIXEL_NORMALIZE

PLANE_PIXEL_NORMALIZE	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to PLANE_SURF
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	701A8h-701ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_1_A
Reset:	soft
Address:	702A8h-702ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_2_A
Reset:	soft
Address:	703A8h-703ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_3_A
Reset:	soft
Address:	711A8h-711ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_1_B
Reset:	soft
Address:	712A8h-712ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_2_B
Reset:	soft
Address:	713A8h-713ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_3_B
Reset:	soft
Address:	721A8h-721ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_1_C
Reset:	soft

PLANE_PIXEL_NORMALIZE

Address:	722A8h-722ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_2_C
Reset:	soft

Address:	723A8h-723ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_3_C
Reset:	soft

DWord	Bit	Description
0	31	**Enable** Access: Double Buffered This field enables the normalization of FP16 pixels with the specified normalization factor.
	30:16	**Reserved** Access: RO Format: MBZ
	15:0	**Normalization Factor** Access: Double Buffered **Description** This field specifies the normalization factor in the FP16 format. This programmed value is multiplied with the input pixel value and normalized to range -4.0 to 4.0, exclusive. Out of bound values get clamped to be within the range from -4.0 to 4.0, exclusive. The programmed half float value must be a positive and not de-normalized, zero or NAN.

PLANE_POS

PLANE_POS	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	7048Ch-7048Fh
Name:	Plane Position
ShortName:	PLANE_POS_4_A
Reset:	soft
Address:	7058Ch-7058Fh
Name:	Plane Position
ShortName:	PLANE_POS_5_A
Reset:	soft
Address:	7148Ch-7148Fh
Name:	Plane Position
ShortName:	PLANE_POS_4_B
Reset:	soft
Address:	7158Ch-7158Fh
Name:	Plane Position
ShortName:	PLANE_POS_5_B
Reset:	soft
Address:	7248Ch-7248Fh
Name:	Plane Position
ShortName:	PLANE_POS_4_C
Reset:	soft
Address:	7258Ch-7258Fh
Name:	Plane Position
ShortName:	PLANE_POS_5_C
Reset:	soft
Address:	7018Ch-7018Fh
Name:	Plane Position
ShortName:	PLANE_POS_1_A
Reset:	soft

PLANE_POS	
Address:	7028Ch-7028Fh
Name:	Plane Position
ShortName:	PLANE_POS_2_A
Reset:	soft
Address:	7038Ch-7038Fh
Name:	Plane Position
ShortName:	PLANE_POS_3_A
Reset:	soft
Address:	7118Ch-7118Fh
Name:	Plane Position
ShortName:	PLANE_POS_1_B
Reset:	soft
Address:	7128Ch-7128Fh
Name:	Plane Position
ShortName:	PLANE_POS_2_B
Reset:	soft
Address:	7138Ch-7138Fh
Name:	Plane Position
ShortName:	PLANE_POS_3_B
Reset:	soft
Address:	7218Ch-7218Fh
Name:	Plane Position
ShortName:	PLANE_POS_1_C
Reset:	soft
Address:	7228Ch-7228Fh
Name:	Plane Position
ShortName:	PLANE_POS_2_C
Reset:	soft
Address:	7238Ch-7238Fh
Name:	Plane Position
ShortName:	PLANE_POS_3_C
Reset:	soft
Address:	70894h-70897h
Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_1_A
Reset:	soft

PLANE_POS

Address:	708B4h-708B7h
Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_2_A
Reset:	soft

Address:	708D4h-708D7h
Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_3_A
Reset:	soft

Address:	708F4h-708F7h
Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_4_A
Reset:	soft

Address:	70924h-70927h
Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_5_A
Reset:	soft

This register specifies the screen position of the plane. The origin of the plane position is always the upper left corner of the display pipe source image area. When plane scaling is not enabled on this plane, this is the position of the plane when blended with other planes on this pipe. When plane scaling is enabled on this plane, the scaler window position is the position of the plane when blended with other planes on this pipe. When performing rotation, the plane image is rotated by hardware, but the position is not, so it must be adjusted if it is desired to maintain the same apparent position on a physically rotated display.

Restriction

When plane scaling is not enabled on this plane, the plane must be completely contained within the pipe source area. Pipe source size >= plane position + plane size. When plane scaling is enabled on this plane, the X and Y positions must be programmed to 0.

DWord	Bit	Description
0	31:29	**Reserved** Access: RO Format: MBZ
	28:16	**Y Position** Access: Double Buffered This specifies the vertical position of the plane upper left corner in lines.
	15:13	**Reserved** Access: RO Format: MBZ

PLANE_POS		
	12:0	**X Position** Access: Double Buffered This specifies the horizontal position of the plane upper left corner in pixels.

PLANE_POST_CSC_GAMC_DATA

PLANE_POST_CSC_GAMC_DATA	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	704DCh-704DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_4_A
Reset:	soft
Address:	705DCh-705DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_5_A
Reset:	soft
Address:	714DCh-714DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_4_B
Reset:	soft
Address:	715DCh-715DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_5_B
Reset:	soft
Address:	724DCh-724DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_4_C
Reset:	soft
Address:	725DCh-725DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_5_C
Reset:	soft

PLANE_POST_CSC_GAMC_DATA

PLANE_POST_CSC_GAMC_INDEX and PLANE_POST_CSC_GAMC_DATA registers are used to program the values that determine the characteristics of the gamma correction for the plane pixel data after plane Color Space Conversion.
The gamma correction curve is represented by specifying a set of gamma entry reference points spaced equally along the curve for values between -1 and 1. For extended values there are extended gamma entry reference points. All input values are clamped to the greater than -7.0 and less than 7.0 range before the gamma calculation.
For input values greater than or equal to 0 and less than 1.0, the input value is used to linearly interpolate between two adjacent points of the first 33 gamma entries to create the result value. The first 32 entries are stored as 16 bits per color in an unsigned 0.16 format with 0 integer and16 fractional. The 33rd, 34th and 35th entries are stored as19 bits per color in an unsigned 3.16 format with 3 integer and16 fractional bits.
For input values greater than or equal to 1.0 and less than 3.0, the input value is used to linearly interpolate between the 33rd and 34th gamma entries to create the result value.
For input values greater than or equal to 3.0 and less than 7.0, the input value is used to linearly interpolate between the 34th and 35th gamma entries to create the result value.
For negative input values, gamma is mirrored along the X-axis, giving the same result as positive input values, except for a negative sign. When gamma input may be negative, the first gamma point should be programmed to a value of 0.0 in order to have a symmetric mirroring.
Plane Post-CSC Gamma correction gets enabled or disabled based on the 'Plane Gamma Disable' bit in the 'PLANE_COLOR_CTL' register. The same set of values is used for gamma correction of the red, blue and green channels.

Programming Notes

To program the gamma correction entries, calculate the desired gamma curve for inputs from 0 to 7.0. For inputs of 0 to 1.0, multiply the input value by 32 to find the gamma entry number, then store the desired gamma result in that entry. For inputs greater than 1.0 and less than or equal to 3.0, store the result for an input of 3.0 in the 34th gamma entry. For inputs greater than 3.0 and less than or equal to 7.0, store the result for an input of 7.0 in the 35th gamma entry.

Restriction

The gamma curve must be flat or increasing, never decreasing in Direct mode. The gamma correction registers should only be updated when the plane is off, otherwise screen artifacts may show temporarily.

DWord	Bit	Description
0	31:19	**Reserved** Access: RO Format: MBZ
	18:0	**Gamma Value** Default Value: 00000000000000000b Access: Double Buffered Format: U3.16

PLANE_POST_CSC_GAMC_DATA_ENH

PLANE_POST_CSC_GAMC_DATA_ENH	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	701DCh-701DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_1_A
Reset:	soft
Address:	702DCh-702DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_2_A
Reset:	soft
Address:	703DCh-703DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_3_A
Reset:	soft
Address:	711DCh-711DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_1_B
Reset:	soft
Address:	712DCh-712DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_2_B
Reset:	soft
Address:	713DCh-713DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_3_B
Reset:	soft
Address:	721DCh-721DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_1_C
Reset:	soft

PLANE_POST_CSC_GAMC_DATA_ENH

Address:	722DCh-722DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_2_C
Reset:	soft

Address:	723DCh-723DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_3_C
Reset:	soft

PLANE_POST_CSC_GAMC_INDEX and PLANE_POST_CSC_GAMC_DATA registers are used to program the values that determine the characteristics of the gamma correction for the plane pixel data before Color Space Conversion. Additional gamma correction can be done after the Color Space Conversion, if needed.
The gamma correction curve is represented by specifying a set of gamma entry reference points spaced equally along the curve for values between -1 and 1. For extended values there are extended gamma entry reference points. All input values are clamped to the greater than -7.0 and less than 7.0 range before the gamma calculation.
For input values greater than or equal to 0 and less than 1.0, the input value is used to linearly interpolate between two adjacent points of the first 33 gamma entries to create the result value. The first 32 entries are stored as 24 bits per color in an unsigned 0.24 format with 0 integer and 24 fractional. The 33rd, 34th and 35th entries are stored as27 bits per color in an unsigned 3.24 format with 3 integer and 24 fractional bits.
For input values greater than or equal to 1.0 and less than 3.0, the input value is used to linearly interpolate between the 33rd and 34th gamma entries to create the result value.
For input values greater than or equal to 3.0 and less than 7.0, the input value is used to linearly interpolate between the 34th and 35th gamma entries to create the result value.
For negative input values, gamma is mirrored along the X-axis, giving the same result as positive input values, except for a negative sign. When gamma input may be negative, the first gamma point should be programmed to a value of 0.0 in order to have a symmetric mirroring.
Pre-CSC Gamma correction gets enabled or disabled based on the "Pipe CSC Enable" bit in the plane control register. The same set of values is used for gamma correction of the red, blue and green channels.
See Pipe Gamma for an example gamma curve diagram.
To program the gamma correction entries, calculate the desired gamma curve for inputs from 0 to 7.0. For inputs of 0 to 1.0, multiply the input value by 32 to find the gamma entry number, then store the desired gamma result in that entry. For inputs greater than 1.0 and less than or equal to 3.0, store the result for an input of 3.0 in the 34th gamma entry. For inputs greater than 3.0 and less than or equal to 7.0, store the result for an input of 7.0 in the 35th gamma entry.
For HDR tone mapping usages, only the first 33 entries gets used. The entries are used either in an unsigned 0.24 format or unsigned 8.16 format based on PLANE_COLOR_CTL->Plane Gamma Multiplier Precision programming.

Restriction
The gamma curve must be flat or increasing, never decreasing when used in the direct lookup mode. The gamma correction registers should only be updated when the plane is off, otherwise screen artifacts may show temporarily.

DWord	Bit	Description

PLANE_POST_CSC_GAMC_DATA_ENH		
0	31:27	**Reserved** Access: RO Format: MBZ
	26:0	**Gamma Value** Default Value: 00000000000000000000000000b Access: R/W Format: U3.24

PLANE_POST_CSC_GAMC_INDEX

PLANE_POST_CSC_GAMC_INDEX	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	704D8h-704DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_4_A
Reset:	soft
Address:	705D8h-705DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_5_A
Reset:	soft
Address:	714D8h-714DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_4_B
Reset:	soft
Address:	715D8h-715DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_5_B
Reset:	soft
Address:	724D8h-724DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_4_C
Reset:	soft
Address:	725D8h-725DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_5_C
Reset:	soft

DWord	Bit	Description

PLANE_POST_CSC_GAMC_INDEX

0 — 31:11 — Reserved

Access:	RO
Format:	MBZ

0 — 10 — Index Auto Increment

Access:	Double Buffered

This field enables the index auto increment.

Value	Name	Description
0b	No Increment	Do not automatically increment the index value.
1b	Auto Increment **[Default]**	Increment the index value with each read or write to the data register.

0 — 9:6 — Reserved

Access:	RO
Format:	MBZ

0 — 5:0 — Index Value

Access:	Write/Read Status

This index controls access to the array of plane pre color space conversion gamma values.
This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set.
When automatically incrementing, the index will roll over to 0 after writing or reading the entire allowed range.
While in auto increment mode, after performing reads or writes to only part of the range, the auto increment bit must be cleared before resetting the index value.

Value	Name
[0,34]	

PLANE_POST_CSC_GAMC_INDEX_ENH

PLANE_POST_CSC_GAMC_INDEX_ENH	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	701D8h-701DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_1_A
Reset:	soft
Address:	702D8h-702DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_2_A
Reset:	soft
Address:	703D8h-703DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_3_A
Reset:	soft
Address:	711D8h-711DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_1_B
Reset:	soft
Address:	712D8h-712DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_2_B
Reset:	soft
Address:	713D8h-713DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_3_B
Reset:	soft
Address:	721D8h-721DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_1_C
Reset:	soft

PLANE_POST_CSC_GAMC_INDEX_ENH

Address:	722D8h-722DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_2_C
Reset:	soft

Address:	723D8h-723DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_3_C
Reset:	soft

DWord	Bit	Description
0	31:11	**Reserved** Access: RO Format: MBZ
	10	**Index Auto Increment** Access: R/W This field enables the index auto increment. 0b – No Increment – Do not automatically increment the index value. 1b – Auto Increment **[Default]** – Increment the index value with each read or write to the data register.
	9:6	**Reserved** Access: RO Format: MBZ
	5:0	**Index Value** Access: Write/Read Status This index controls access to the array of plane pre color space conversion gamma values. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set. When automatically incrementing, the current automatically calculated index value can be read here, and the index will roll over to 0 after reaching the end of the allowed range. While in auto increment mode, after performing reads or writes to only part of the range, the auto increment bit must be cleared before resetting the index value. [0,34]

PLANE_POST_CSC_GAMC_SEG0_DATA_ENH

PLANE_POST_CSC_GAMC_SEG0_DATA_ENH	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	70164h-70167h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_1_A
Reset:	soft
Address:	70264h-70267h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_2_A
Reset:	soft
Address:	70364h-70367h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_3_A
Reset:	soft
Address:	71164h-71167h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_1_B
Reset:	soft
Address:	71264h-71267h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_2_B
Reset:	soft
Address:	71364h-71367h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_3_B
Reset:	soft
Address:	72164h-72167h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_1_C
Reset:	soft

PLANE_POST_CSC_GAMC_SEG0_DATA_ENH

Address:	72264h-72267h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_2_C
Reset:	soft

Address:	72364h-72367h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_3_C
Reset:	soft

PLANE_POST_CSC_GAMC_SEG0_INDEX and PLANE_POST_CSC_GAMC_SEG0_DATA registers are used to program the segment 0 values of the HDR tone mapping curve.
The entries are stored as 24 bits per color in an unsigned 0.24 format with 0 integer and 24 fractional.

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23:0	**Gamma Value** Default Value: 000000000000000000000000b Access: R/W Format: U0.24

PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH

PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	70160h-70163h
Name:	Plane Post CSC Gamma Segment0 Index
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_1_A
Reset:	soft
Address:	70260h-70263h
Name:	Plane Post CSC Gamma Segment0 Index
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_2_A
Reset:	soft
Address:	70360h-70363h
Name:	Plane Post CSC Gamma Segment0 Index
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_3_A
Reset:	soft
Address:	71160h-71163h
Name:	Plane Post CSC Gamma Segment0 Index
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_1_B
Reset:	soft
Address:	71260h-71263h
Name:	Plane Post CSC Gamma Segment0 Index
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_2_B
Reset:	soft
Address:	71360h-71363h
Name:	Plane Post CSC Gamma Segment0 Index
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_3_B
Reset:	soft
Address:	72160h-72163h
Name:	Plane Post CSC Gamma Segment0 Index
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_1_C
Reset:	soft

PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH

Address:	72260h-72263h
Name:	Plane Post CSC Gamma Segment0 Index
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_2_C
Reset:	soft

Address:	72360h-72363h
Name:	Plane Post CSC Gamma Segment0 Index
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_3_C
Reset:	soft

DWord	Bit	Description
0	31:11	**Reserved** Access: RO Format: MBZ
	10	**Index Auto Increment** Access: R/W This field enables the index auto increment. 0b – No Increment – Do not automatically increment the index value. 1b – Auto Increment **[Default]** – Increment the index value with each read or write to the data register.
	9:4	**Reserved** Access: RO Format: MBZ
	3:0	**Index Value** Access: Write/Read Status This index controls access to the segment 0of plane postcolor space conversion gamma values. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set. When automatically incrementing, the current automatically calculated index value can be read here, and the index will roll over to 0 after reaching the end of the allowed range. While in auto increment mode, after performing reads or writes to only part of the range, the auto increment bit must be cleared before resetting the index value. [0,8]

PLANE_PRE_CSC_GAMC_DATA

PLANE_PRE_CSC_GAMC_DATA	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	704D4h-704D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_4_A
Reset:	soft
Address:	705D4h-705D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_5_A
Reset:	soft
Address:	714D4h-714D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_4_B
Reset:	soft
Address:	715D4h-715D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_5_B
Reset:	soft
Address:	724D4h-724D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_4_C
Reset:	soft
Address:	725D4h-725D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_5_C
Reset:	soft

PLANE_PRE_CSC_GAMC_DATA

PLANE_PRE_CSC_GAMC_INDEX and PLANE_PRE_CSC_GAMC_DATA registers are used to program the values that determine the characteristics of the gamma correction for the plane pixel data before Color Space Conversion. Additional gamma correction can be done after the Color Space Conversion, if needed.
The gamma correction curve is represented by specifying a set of gamma entry reference points spaced equally along the curve for values between -1 and 1. For extended values there are extended gamma entry reference points. All input values are clamped to the greater than -7.0 and less than 7.0 range before the gamma calculation.
For input values greater than or equal to 0 and less than 1.0, the input value is used to linearly interpolate between two adjacent points of the first 33 gamma entries to create the result value. The first 32 entries are stored as16 bits per color in an unsigned 0.16 format with 0 integer and 16 fractional. The 33rd, 34th and 35th entries are stored as 19 bits per color in an unsigned 3.16 format with 3 integer and 16 fractional bits.
For input values greater than or equal to 1.0 and less than 3.0, the input value is used to linearly interpolate between the 33rd and 34th gamma entries to create the result value.
For input values greater than or equal to 3.0 and less than 7.0, the input value is used to linearly interpolate between the 34th and 35th gamma entries to create the result value.
For negative input values, gamma is mirrored along the X-axis, giving the same result as positive input values, except for a negative sign. When gamma input may be negative, the first gamma point should be programmed to a value of 0.0 in order to have a symmetric mirroring.
Plane Pre-CSC Gamma correction gets enabled or disabled based on the 'Plane Pre CSC Gamma Enable' bit in the 'PLANE_COLOR_CTL' register. The same set of values is used for gamma correction of the red, blue and green channels.

Programming Notes

To program the gamma correction entries, calculate the desired gamma curve for inputs from 0 to 7.0. For inputs of 0 to 1.0, multiply the input value by 32 to find the gamma entry number, then store the desired gamma result in that entry. For inputs greater than 1.0 and less than or equal to 3.0, store the result for an input of 3.0 in the 34th gamma entry. For inputs greater than 3.0 and less than or equal to 7.0, store the result for an input of 7.0 in the 35th gamma entry.

Restriction

The gamma curve must be flat or increasing, never decreasing. The gamma correction registers should only be updated when the plane is off, otherwise screen artifacts may show temporarily.

DWord	Bit	Description
0	31:19	**Reserved** Access: RO Format: MBZ
	18:0	**Gamma Value** Default Value: 0000000000000000000b Access: Double Buffered Format: U3.16

PLANE_PRE_CSC_GAMC_DATA_ENH

PLANE_PRE_CSC_GAMC_DATA_ENH	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
Address:	701D4h-701D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_1_A
Reset:	soft
Address:	702D4h-702D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_2_A
Reset:	soft
Address:	703D4h-703D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_3_A
Reset:	soft
Address:	711D4h-711D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_1_B
Reset:	soft
Address:	712D4h-712D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_2_B
Reset:	soft
Address:	713D4h-713D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_3_B
Reset:	soft
Address:	721D4h-721D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_1_C
Reset:	soft
Address:	722D4h-722D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_2_C

PLANE_PRE_CSC_GAMC_DATA_ENH

Reset:	soft

Address:	723D4h-723D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_3_C
Reset:	soft

PLANE_PRE_CSC_GAMC_INDEX and PLANE_PRE_CSC_GAMC_DATA registers are used to program the values that determine the characteristics of the gamma correction for the plane pixel data before Color Space Conversion. Additional gamma correction can be done after the Color Space Conversion, if needed.
The gamma correction curve is represented by specifying a set of gamma entry reference points spaced equally along the curve for values between -1 and 1. For extended values there are extended gamma entry reference points. All input values are clamped to the greater than -7.0 and less than 7.0 range before the gamma calculation.
For input values greater than or equal to 0 and less than 1.0, the input value is used to linearly interpolate between two adjacent points of the first 129 gamma entries to create the result value. The first 128 entries are stored as 24 bits per color in an unsigned 0.24 format with 0 integer and 24 fractional. The 129th, 130th and 131th entries are stored as 27 bits per color in an unsigned 3.24 format with 3 integer and 24 fractional bits.
For input values greater than or equal to 1.0 and less than 3.0, the input value is used to linearly interpolate between the 129th and 130th gamma entries to create the result value.
For input values greater than or equal to 3.0 and less than 7.0, the input value is used to linearly interpolate between the 130th and 131st gamma entries to create the result value.
For negative input values, gamma is mirrored along the X-axis, giving the same result as positive input values, except for a negative sign. When gamma input may be negative, the first gamma point should be programmed to a value of 0.0 in order to have a symmetric mirroring.
Pre-CSC Gamma correction gets enabled or disabled based on the "Plane Pre CSC Gamma Enable" bit in the plane color control register. The same set of values is used for gamma correction of the red, blue and green channels.
See Pipe Gamma for an example gamma curve diagram.

Programming Notes

To program the gamma correction entries, calculate the desired gamma curve for inputs from 0 to 7.0. For inputs of 0 to 1.0, multiply the input value by 128 to find the gamma entry number, then store the desired gamma result in that entry. For inputs greater than 1.0 and less than or equal to 3.0, store the result for an input of 3.0 in the 129th gamma entry. For inputs greater than 3.0 and less than or equal to 7.0, store the result for an input of 7.0 in the 130th gamma entry.

Restriction

The gamma curve must be flat or increasing, never decreasing. The gamma correction registers should only be updated when the plane is off, otherwise screen artifacts may show temporarily.

DWord	Bit	Description
0	31:27	**Reserved** Access: RO Format: MBZ

PLANE_PRE_CSC_GAMC_DATA_ENH		
	26:0	**Gamma Value** Default Value: 00000000000000000000000000b Access: Double Buffered Format: U3.24

PLANE_PRE_CSC_GAMC_INDEX

PLANE_PRE_CSC_GAMC_INDEX	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed

Address:	704D0h-704D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_4_A
Reset:	soft

Address:	705D0h-705D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_5_A
Reset:	soft

Address:	714D0h-714D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_4_B
Reset:	soft

Address:	715D0h-715D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_5_B
Reset:	soft

Address:	724D0h-724D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_4_C
Reset:	soft

Address:	725D0h-725D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_5_C
Reset:	soft

DWord	Bit	Description
0	31:11	**Reserved** Access: RO Format: MBZ

PLANE_PRE_CSC_GAMC_INDEX

	10	**Index Auto Increment** Access: Double Buffered This field enables the index auto increment. **Value** / **Name** / **Description** 0b / No Increment / Do not automatically increment the index value. 1b / Auto Increment **[Default]** / Increment the index value with each read or write to the data register.
	9:6	**Reserved** Access: RO Format: MBZ
	5:0	**Index Value** Access: Write/Read Status This index controls access to the array of plane pre color space conversion gamma values. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set. When automatically incrementing, the index will roll over to 0 after writing or reading the entire allowed range. While in auto increment mode, after performing reads or writes to only part of the range, the auto increment bit must be cleared before resetting the index value. **Value** / **Name** [0,34] /

PLANE_PRE_CSC_GAMC_INDEX_ENH

PLANE_PRE_CSC_GAMC_INDEX_ENH	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
Address:	701D0h-701D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_1_A
Reset:	soft
Address:	702D0h-702D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_2_A
Reset:	soft
Address:	703D0h-703D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_3_A
Reset:	soft
Address:	711D0h-711D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_1_B
Reset:	soft
Address:	712D0h-712D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_2_B
Reset:	soft
Address:	713D0h-713D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_3_B
Reset:	soft
Address:	721D0h-721D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_1_C
Reset:	soft

PLANE_PRE_CSC_GAMC_INDEX_ENH

Address:	722D0h-722D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_2_C
Reset:	soft

Address:	723D0h-723D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_3_C
Reset:	soft

<table>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td rowspan="4">0</td><td>31:11</td><td>Reserved
<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td>10</td><td>Index Auto Increment
<table><tr><td>Access:</td><td>Double Buffered</td></tr></table>This field enables the index auto increment.
<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0b</td><td>No Increment</td><td>Do not automatically increment the index value.</td></tr><tr><td>1b</td><td>Auto Increment
[Default]</td><td>Increment the index value with each read or write to the data register.</td></tr></table></td></tr>
<tr><td>9:8</td><td>Reserved
<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td>7:0</td><td>Index Value
<table><tr><td>Access:</td><td>Write/Read Status</td></tr></table>This index controls access to the array of plane pre color space conversion gamma values.
This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set.
When automatically incrementing, the index will roll over to 0 after writing or reading the entire allowed range.
While in auto increment mode, after performing reads or writes to only part of the range, the auto increment bit must be cleared before resetting the index value.
<table><tr><th>Value</th><th>Name</th></tr><tr><td>[0,130]</td><td></td></tr></table></td></tr>
</table>

PLANE_SIZE

PLANE_SIZE	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	70490h-70493h
Name:	Plane Size
ShortName:	PLANE_SIZE_4_A
Reset:	soft
Address:	70590h-70593h
Name:	Plane Size
ShortName:	PLANE_SIZE_5_A
Reset:	soft
Address:	71490h-71493h
Name:	Plane Size
ShortName:	PLANE_SIZE_4_B
Reset:	soft
Address:	71590h-71593h
Name:	Plane Size
ShortName:	PLANE_SIZE_5_B
Reset:	soft
Address:	72490h-72493h
Name:	Plane Size
ShortName:	PLANE_SIZE_4_C
Reset:	soft
Address:	72590h-72593h
Name:	Plane Size
ShortName:	PLANE_SIZE_5_C
Reset:	soft
Address:	70190h-70193h
Name:	Plane Size
ShortName:	PLANE_SIZE_1_A
Reset:	soft

PLANE_SIZE	
Address:	70290h-70293h
Name:	Plane Size
ShortName:	PLANE_SIZE_2_A
Reset:	soft
Address:	70390h-70393h
Name:	Plane Size
ShortName:	PLANE_SIZE_3_A
Reset:	soft
Address:	71190h-71193h
Name:	Plane Size
ShortName:	PLANE_SIZE_1_B
Reset:	soft
Address:	71290h-71293h
Name:	Plane Size
ShortName:	PLANE_SIZE_2_B
Reset:	soft
Address:	71390h-71393h
Name:	Plane Size
ShortName:	PLANE_SIZE_3_B
Reset:	soft
Address:	72190h-72193h
Name:	Plane Size
ShortName:	PLANE_SIZE_1_C
Reset:	soft
Address:	72290h-72293h
Name:	Plane Size
ShortName:	PLANE_SIZE_2_C
Reset:	soft
Address:	72390h-72393h
Name:	Plane Size
ShortName:	PLANE_SIZE_3_C
Reset:	soft
Address:	70898h-7089Bh
Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_1_A
Reset:	soft

PLANE_SIZE

Address:	708B8h-708BBh
Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_2_A
Reset:	soft

Address:	708D8h-708DBh
Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_3_A
Reset:	soft

Address:	708F8h-708FBh
Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_4_A
Reset:	soft

Address:	70928h-7092Bh
Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_5_A
Reset:	soft

This register specifies the plane source size, the size of the image fetched from the frame buffer. When plane scaling is not enabled on this plane, this is the size of the plane when blended with other planes on this pipe. When plane scaling is enabled on this plane, the scaler window size is the size of the plane when blended with other planes on this pipe.

Restriction

When plane scaling is not enabled on this plane, the plane must be completely contained within the pipe source area. Pipe source size >= plane position + plane size.
Refer to the Resolution Support section for maximum size restrictions.

Height and Width even size restrictions are specified in the following table. For formats not specified in the table, both odd and even sizes are supported.

Pixel Format	Rotate	Width	Height
YUV 420 Planar - NV12	All	Even	Even
YUV 420 Planar - P01x	All	Even	Even
YUV 422	All	Even	Even
RGB565	90, 270	Even	Even

If Plane Scaling or using the Chroma Up-Sampler (CUS) for this plane, please refer to PS_CTRL or PLANE_CUS_CTL respectively, for further size restrictions.

DWord	Bit	Description
0	31:29	**Reserved** Access: RO Format: MBZ

PLANE_SIZE

	28:16	**Height** Access: Double Buffered This specifies the height of the plane in lines. The value in the register is the height minus one. **Restriction** The height must be at least one line when non-interlaced, two lines when interlaced.
	15:13	**Reserved** Access: RO Format: MBZ
	12:0	**Width** Access: Double Buffered This specifies the width of the plane in pixels. The value in the register is the width minus one. **Restriction** The width must be even (programmed value odd) when YUV 4:2:2 or YUV 4:2:0 source pixel format is used. For YUV4:2:0 (NV12), the UV plane must be greater than or equal to 8 and the Y plane must be greater than or equal to 16. The width must be greater than or equal to 4 for 32bpp, YUV212, and YUV216 formats, greater than or equal to 8 for 16bpp formats, and greater than or equal to 16 for 8bpp formats. The width must be greater than or equal to 2 for 64bpp formats. The width must be greater than or equal to 8 for P010, P012 and P016 formats. The width should be less than or equal to the stride in pixels. For planar YUV 420 formats, refer to chroma upsampler size restrictions in PLANE_CUS_CTL register.

Tiling format	Bytes per pixel	Max Width supported in pixels
Linear, X Tiling	1,2,4,8	5120
Y Tiling	1,2,4,8	5120

PLANE_STRIDE

PLANE_STRIDE	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	70488h-7048Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_4_A
Reset:	soft
Address:	70588h-7058Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_5_A
Reset:	soft
Address:	71488h-7148Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_4_B
Reset:	soft
Address:	71588h-7158Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_5_B
Reset:	soft
Address:	72488h-7248Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_4_C
Reset:	soft
Address:	72588h-7258Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_5_C
Reset:	soft
Address:	70188h-7018Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_1_A
Reset:	soft

PLANE_STRIDE

Address:	70288h-7028Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_2_A
Reset:	soft
Address:	70388h-7038Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_3_A
Reset:	soft
Address:	71188h-7118Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_1_B
Reset:	soft
Address:	71288h-7128Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_2_B
Reset:	soft
Address:	71388h-7138Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_3_B
Reset:	soft
Address:	72188h-7218Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_1_C
Reset:	soft
Address:	72288h-7228Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_2_C
Reset:	soft
Address:	72388h-7238Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_3_C
Reset:	soft

This register may be updated through MMIO writes or through command streamer initiated synchronous flips.

DWord	Bit	Description
0	31:18	**Reserved**

PLANE_STRIDE

		Access: RO Format: MBZ
	17:12	**Reserved** Access: RO Format: MBZ
	11	**Reserved** Access: RO Format: MBZ
	10:0	**Stride** Access: Double Buffered This field specifies the stride for the plane. The field is used to determine the line-to-line increment for the plane. For Linear memory, this field specifies the stride in chunks of 64 bytes (1 cache line). If the programmed value is 100, the actual stride = 100 * 64 = 6400 bytes. For X-Tiled & Y-Tiled memory, this field specifies the stride in number of tiles. For Tile X, if the programmed value is 10, the actual stride = 10 * 512 (X tile width) = 5120 bytes. For Tile Y, if the programmed value is 10, the actual stride = 10 * 128 (Y tile width) = 1280 bytes.

Tile Format	Width in bytes
Tile X	512
Tile Y (legacy)	128

PLANE_STRIDE

Restriction : For YUV planar (NV12 or P0xx) plane pixel formats, the stride calculated in bytes should be equal for the Y and UV surfaces.
The stride in bytes must not exceed the of the size of 8K pixels.

Tile Format	Pixel Format	Maximum Stride in tiles
Linear	64 bpp pixel format	1024
	32 bpp pixel format	512
	16 bpp pixel format	256
	8 bpp pixel format	128
X Tiling	64 bpp pixel format	128
	32 bpp pixel format	64
	16 bpp pixel format	32
	8 bpp pixel format	16
Y Tiling (Legacy)	64 bpp pixel format	512
	32 bpp pixel format	256
	16 bpp pixel format	128
	8 bpp pixel format	64

PLANE_SURF

PLANE_SURF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferUpdatePoint:	Start of left or right eye vertical blank (selectable), pipe not enabled, or plane not enabled
Address:	7049Ch-7049Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_4_A
Reset:	soft
Address:	7059Ch-7059Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_5_A
Reset:	soft
Address:	7149Ch-7149Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_4_B
Reset:	soft
Address:	7159Ch-7159Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_5_B
Reset:	soft
Address:	7249Ch-7249Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_4_C
Reset:	soft
Address:	7259Ch-7259Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_5_C
Reset:	soft
Address:	7019Ch-7019Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_1_A
Reset:	soft

PLANE_SURF	
Address:	7029Ch-7029Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_2_A
Reset:	soft
Address:	7039Ch-7039Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_3_A
Reset:	soft
Address:	7119Ch-7119Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_1_B
Reset:	soft
Address:	7129Ch-7129Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_2_B
Reset:	soft
Address:	7139Ch-7139Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_3_B
Reset:	soft
Address:	7219Ch-7219Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_1_C
Reset:	soft
Address:	7229Ch-7229Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_2_C
Reset:	soft
Address:	7239Ch-7239Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_3_C
Reset:	soft

PLANE_SURF

Writes to this register arm primary registers for this pipe. A write to this register is considered a flip and can cause a flip done interrupt if the interrupt registers are configured for that. The values in this register may be updated through MMIO writes or through command streamer initiated flips. Synchronous updates (synchronous command streamer flips or synchronous MMIO writes) will update the plane surface values at the start of the next vertical blank. Asynchronous updates (asynchronous command streamer flips or asynchronous MMIO writes) will update the plane surface values at the next TLB request or at the start of the next vertical blank. Stereo 3D synchronous updates (stereo 3D command streamer flips or synchronous MMIO writes while stereo 3D is enabled) will update at the start of either the left or right eye vertical blank, selectable by the plane control register stereo surface vblank mask.

Double buffering control does not apply to PLANE_SURF updates that occur when the plane is disabled. An interrupt event is generated immediately when the PLANE_SURF is written. If the interrupt is unmasked, the interrupt is logged in the IIR.

Asynchronous flip completion time depends greatly on how much data has been prefetched for power savings, and can take up to 1 full frame to complete. For faster flip completion, disable FBC and render compression and allocate a small amount of data buffer for the plane.

DWord	Bit	Description
0	31:12	**Surface Base Address** Access: Double Buffered Format: GraphicsAddress[31:12]
	11	**Reserved** Access: Double Buffered
	10:7	**Reserved** Access: RO Format: MBZ
	6:4	**Reserved** Access: Double Buffered
	3	**Ring Flip Source** Access: Double Buffered This bit indicates if the source of the last ring flip was CS or BCS. This will determine where the flip done response is sent. 0b: CS 1b: BCS
	2	**Reserved** Access: Double Buffered

PLANE_SURF		
	1:0	**Reserved** Access: RO Format: MBZ

PLANE_SURFLIVE

PLANE_SURFLIVE	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	704ACh-704AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_4_A
Reset:	soft
Address:	704BCh-704BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_4_A
Reset:	soft
Address:	705ACh-705AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_5_A
Reset:	soft
Address:	705BCh-705BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_5_A
Reset:	soft
Address:	714ACh-714AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_4_B
Reset:	soft
Address:	714BCh-714BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_4_B
Reset:	soft
Address:	715ACh-715AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_5_B
Reset:	soft
Address:	715BCh-715BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_5_B
Reset:	soft

PLANE_SURFLIVE	
Address:	724ACh-724AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_4_C
Reset:	soft
Address:	724BCh-724BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_4_C
Reset:	soft
Address:	725ACh-725AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_5_C
Reset:	soft
Address:	725BCh-725BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_5_C
Reset:	soft
Address:	701ACh-701AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_1_A
Reset:	soft
Address:	701BCh-701BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_1_A
Reset:	soft
Address:	702ACh-702AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_2_A
Reset:	soft
Address:	702BCh-702BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_2_A
Reset:	soft
Address:	703ACh-703AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_3_A
Reset:	soft

PLANE_SURFLIVE	
Address:	703BCh-703BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_3_A
Reset:	soft
Address:	711ACh-711AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_1_B
Reset:	soft
Address:	711BCh-711BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_1_B
Reset:	soft
Address:	712ACh-712AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_2_B
Reset:	soft
Address:	712BCh-712BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_2_B
Reset:	soft
Address:	713ACh-713AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_3_B
Reset:	soft
Address:	713BCh-713BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_3_B
Reset:	soft
Address:	721ACh-721AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_1_C
Reset:	soft
Address:	721BCh-721BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_1_C
Reset:	soft

PLANE_SURFLIVE

Address:	722ACh-722AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_2_C
Reset:	soft

Address:	722BCh-722BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_2_C
Reset:	soft

Address:	723ACh-723AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_3_C
Reset:	soft

Address:	723BCh-723BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_3_C
Reset:	soft

There is one instance of this register for each plane.

DWord	Bit	Description
0	31:12	**Live Surface Base Address** Access: RO This gives the live value of the surface base address as being currently used for the plane.
	11	**Reserved** Access: RO Format: MBZ
	10:9	**Reserved**
	8:0	**Reserved** Access: RO Format: MBZ

PLANE_WM

PLANE_WM	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to PLANE_SURF/CUR_BASE or plane/cursor not enabled
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank, plane not enabled, or pipe not enabled
Address:	70140h-70143h
Name:	Cursor Watermarks
ShortName:	CUR_WM_0_A
Reset:	soft
Address:	70144h-70147h
Name:	Cursor Watermarks
ShortName:	CUR_WM_1_A
Reset:	soft
Address:	70148h-7014Bh
Name:	Cursor Watermarks
ShortName:	CUR_WM_2_A
Reset:	soft
Address:	7014Ch-7014Fh
Name:	Cursor Watermarks
ShortName:	CUR_WM_3_A
Reset:	soft
Address:	70150h-70153h
Name:	Cursor Watermarks
ShortName:	CUR_WM_4_A
Reset:	soft
Address:	70154h-70157h
Name:	Cursor Watermarks
ShortName:	CUR_WM_5_A
Reset:	soft
Address:	70158h-7015Bh
Name:	Cursor Watermarks
ShortName:	CUR_WM_6_A
Reset:	soft

PLANE_WM	
Address:	7015Ch-7015Fh
Name:	Cursor Watermarks
ShortName:	CUR_WM_7_A
Reset:	soft
Address:	70168h-7016Bh
Name:	Cursor Transition Watermark
ShortName:	CUR_WM_TRANS_A
Reset:	soft
Address:	71140h-71143h
Name:	Cursor Watermarks
ShortName:	CUR_WM_0_B
Reset:	soft
Address:	71144h-71147h
Name:	Cursor Watermarks
ShortName:	CUR_WM_1_B
Reset:	soft
Address:	71148h-7114Bh
Name:	Cursor Watermarks
ShortName:	CUR_WM_2_B
Reset:	soft
Address:	7114Ch-7114Fh
Name:	Cursor Watermarks
ShortName:	CUR_WM_3_B
Reset:	soft
Address:	71150h-71153h
Name:	Cursor Watermarks
ShortName:	CUR_WM_4_B
Reset:	soft
Address:	71154h-71157h
Name:	Cursor Watermarks
ShortName:	CUR_WM_5_B
Reset:	soft
Address:	71158h-7115Bh
Name:	Cursor Watermarks
ShortName:	CUR_WM_6_B
Reset:	soft

PLANE_WM	
Address:	7115Ch-7115Fh
Name:	Cursor Watermarks
ShortName:	CUR_WM_7_B
Reset:	soft
Address:	71168h-7116Bh
Name:	Cursor Transition Watermark
ShortName:	CUR_WM_TRANS_B
Reset:	soft
Address:	72140h-72143h
Name:	Cursor Watermarks
ShortName:	CUR_WM_0_C
Reset:	soft
Address:	72144h-72147h
Name:	Cursor Watermarks
ShortName:	CUR_WM_1_C
Reset:	soft
Address:	72148h-7214Bh
Name:	Cursor Watermarks
ShortName:	CUR_WM_2_C
Reset:	soft
Address:	7214Ch-7214Fh
Name:	Cursor Watermarks
ShortName:	CUR_WM_3_C
Reset:	soft
Address:	72150h-72153h
Name:	Cursor Watermarks
ShortName:	CUR_WM_4_C
Reset:	soft
Address:	72154h-72157h
Name:	Cursor Watermarks
ShortName:	CUR_WM_5_C
Reset:	soft
Address:	72158h-7215Bh
Name:	Cursor Watermarks
ShortName:	CUR_WM_6_C
Reset:	soft

PLANE_WM	
Address:	7215Ch-7215Fh
Name:	Cursor Watermarks
ShortName:	CUR_WM_7_C
Reset:	soft
Address:	72168h-7216Bh
Name:	Cursor Transition Watermark
ShortName:	CUR_WM_TRANS_C
Reset:	soft
Address:	70540h-70543h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_4_A
Reset:	soft
Address:	70544h-70547h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_4_A
Reset:	soft
Address:	70548h-7054Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_4_A
Reset:	soft
Address:	7054Ch-7054Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_4_A
Reset:	soft
Address:	70550h-70553h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_4_A
Reset:	soft
Address:	70554h-70557h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_4_A
Reset:	soft
Address:	70558h-7055Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_4_A
Reset:	soft

PLANE_WM	
Address:	7055Ch-7055Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_4_A
Reset:	soft
Address:	70568h-7056Bh
Name:	Plane Transition Watermark
ShortName:	PLANE_WM_TRANS_4_A
Reset:	soft
Address:	70640h-70643h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_5_A
Reset:	soft
Address:	70644h-70647h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_5_A
Reset:	soft
Address:	70648h-7064Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_5_A
Reset:	soft
Address:	7064Ch-7064Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_5_A
Reset:	soft
Address:	70650h-70653h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_5_A
Reset:	soft
Address:	70654h-70657h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_5_A
Reset:	soft
Address:	70658h-7065Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_5_A
Reset:	soft

PLANE_WM	
Address:	7065Ch-7065Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_5_A
Reset:	soft
Address:	70668h-7066Bh
Name:	Plane Transition Watermark
ShortName:	PLANE_WM_TRANS_5_A
Reset:	soft
Address:	71540h-71543h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_4_B
Reset:	soft
Address:	71544h-71547h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_4_B
Reset:	soft
Address:	71548h-7154Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_4_B
Reset:	soft
Address:	7154Ch-7154Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_4_B
Reset:	soft
Address:	71550h-71553h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_4_B
Reset:	soft
Address:	71554h-71557h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_4_B
Reset:	soft
Address:	71558h-7155Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_4_B
Reset:	soft

PLANE_WM	
Address:	7155Ch-7155Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_4_B
Reset:	soft
Address:	71568h-7156Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_4_B
Reset:	soft
Address:	71640h-71643h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_5_B
Reset:	soft
Address:	71644h-71647h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_5_B
Reset:	soft
Address:	71648h-7164Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_5_B
Reset:	soft
Address:	7164Ch-7164Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_5_B
Reset:	soft
Address:	71650h-71653h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_5_B
Reset:	soft
Address:	71654h-71657h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_5_B
Reset:	soft
Address:	71658h-7165Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_5_B
Reset:	soft

PLANE_WM	
Address:	7165Ch-7165Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_5_B
Reset:	soft
Address:	71668h-7166Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_5_B
Reset:	soft
Address:	72540h-72543h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_4_C
Reset:	soft
Address:	72544h-72547h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_4_C
Reset:	soft
Address:	72548h-7254Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_4_C
Reset:	soft
Address:	7254Ch-7254Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_4_C
Reset:	soft
Address:	72550h-72553h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_4_C
Reset:	soft
Address:	72554h-72557h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_4_C
Reset:	soft
Address:	72558h-7255Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_4_C
Reset:	soft

PLANE_WM	
Address:	7255Ch-7255Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_4_C
Reset:	soft
Address:	72568h-7256Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_4_C
Reset:	soft
Address:	72640h-72643h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_5_C
Reset:	soft
Address:	72644h-72647h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_5_C
Reset:	soft
Address:	72648h-7264Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_5_C
Reset:	soft
Address:	7264Ch-7264Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_5_C
Reset:	soft
Address:	72650h-72653h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_5_C
Reset:	soft
Address:	72654h-72657h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_5_C
Reset:	soft
Address:	72658h-7265Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_5_C
Reset:	soft

PLANE_WM	
Address:	7265Ch-7265Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_5_C
Reset:	soft
Address:	72668h-7266Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_5_C
Reset:	soft
Address:	70240h-70243h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_1_A
Reset:	soft
Address:	70244h-70247h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_1_A
Reset:	soft
Address:	70248h-7024Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_1_A
Reset:	soft
Address:	7024Ch-7024Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_1_A
Reset:	soft
Address:	70250h-70253h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_1_A
Reset:	soft
Address:	70254h-70257h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_1_A
Reset:	soft
Address:	70258h-7025Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_1_A
Reset:	soft

PLANE_WM	
Address:	7025Ch-7025Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_1_A
Reset:	soft
Address:	70268h-7026Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_1_A
Reset:	soft
Address:	70340h-70343h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_2_A
Reset:	soft
Address:	70344h-70347h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_2_A
Reset:	soft
Address:	70348h-7034Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_2_A
Reset:	soft
Address:	7034Ch-7034Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_2_A
Reset:	soft
Address:	70350h-70353h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_2_A
Reset:	soft
Address:	70354h-70357h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_2_A
Reset:	soft
Address:	70358h-7035Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_2_A
Reset:	soft

PLANE_WM	
Address:	7035Ch-7035Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_2_A
Reset:	soft
Address:	70368h-7036Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_2_A
Reset:	soft
Address:	70440h-70443h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_3_A
Reset:	soft
Address:	70444h-70447h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_3_A
Reset:	soft
Address:	70448h-7044Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_3_A
Reset:	soft
Address:	7044Ch-7044Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_3_A
Reset:	soft
Address:	70450h-70453h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_3_A
Reset:	soft
Address:	70454h-70457h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_3_A
Reset:	soft
Address:	70458h-7045Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_3_A
Reset:	soft

PLANE_WM	
Address:	7045Ch-7045Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_3_A
Reset:	soft
Address:	70468h-7046Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_3_A
Reset:	soft
Address:	71240h-71243h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_1_B
Reset:	soft
Address:	71244h-71247h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_1_B
Reset:	soft
Address:	71248h-7124Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_1_B
Reset:	soft
Address:	7124Ch-7124Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_1_B
Reset:	soft
Address:	71250h-71253h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_1_B
Reset:	soft
Address:	71254h-71257h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_1_B
Reset:	soft
Address:	71258h-7125Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_1_B
Reset:	soft

PLANE_WM	
Address:	7125Ch-7125Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_1_B
Reset:	soft
Address:	71268h-7126Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_1_B
Reset:	soft
Address:	71340h-71343h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_2_B
Reset:	soft
Address:	71344h-71347h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_2_B
Reset:	soft
Address:	71348h-7134Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_2_B
Reset:	soft
Address:	7134Ch-7134Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_2_B
Reset:	soft
Address:	71350h-71353h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_2_B
Reset:	soft
Address:	71354h-71357h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_2_B
Reset:	soft
Address:	71358h-7135Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_2_B
Reset:	soft

PLANE_WM	
Address:	7135Ch-7135Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_2_B
Reset:	soft
Address:	71368h-7136Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_2_B
Reset:	soft
Address:	71440h-71443h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_3_B
Reset:	soft
Address:	71444h-71447h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_3_B
Reset:	soft
Address:	71448h-7144Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_3_B
Reset:	soft
Address:	7144Ch-7144Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_3_B
Reset:	soft
Address:	71450h-71453h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_3_B
Reset:	soft
Address:	71454h-71457h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_3_B
Reset:	soft
Address:	71458h-7145Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_3_B
Reset:	soft

PLANE_WM	
Address:	7145Ch-7145Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_3_B
Reset:	soft
Address:	71468h-7146Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_3_B
Reset:	soft
Address:	72240h-72243h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_1_C
Reset:	soft
Address:	72244h-72247h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_1_C
Reset:	soft
Address:	72248h-7224Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_1_C
Reset:	soft
Address:	7224Ch-7224Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_1_C
Reset:	soft
Address:	72250h-72253h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_1_C
Reset:	soft
Address:	72254h-72257h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_1_C
Reset:	soft
Address:	72258h-7225Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_1_C
Reset:	soft

PLANE_WM	
Address:	7225Ch-7225Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_1_C
Reset:	soft
Address:	72268h-7226Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_1_C
Reset:	soft
Address:	72340h-72343h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_2_C
Reset:	soft
Address:	72344h-72347h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_2_C
Reset:	soft
Address:	72348h-7234Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_2_C
Reset:	soft
Address:	7234Ch-7234Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_2_C
Reset:	soft
Address:	72350h-72353h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_2_C
Reset:	soft
Address:	72354h-72357h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_2_C
Reset:	soft
Address:	72358h-7235Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_2_C
Reset:	soft

PLANE_WM	
Address:	7235Ch-7235Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_2_C
Reset:	soft
Address:	72368h-7236Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_2_C
Reset:	soft
Address:	72440h-72443h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_3_C
Reset:	soft
Address:	72444h-72447h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_3_C
Reset:	soft
Address:	72448h-7244Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_3_C
Reset:	soft
Address:	7244Ch-7244Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_3_C
Reset:	soft
Address:	72450h-72453h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_3_C
Reset:	soft
Address:	72454h-72457h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_3_C
Reset:	soft
Address:	72458h-7245Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_3_C
Reset:	soft

PLANE_WM

Address:	7245Ch-7245Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_3_C
Reset:	soft

Address:	72468h-7246Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_3_C
Reset:	soft

Programming Notes

There are eight regular watermarks and a transition watermark per plane/cursor. For YUV planar source formats, only the Y surface watermark value should be programmed. Watermark programming instructions are documented separately.

Restriction

For minimum watermark requirements refer to Display Watermark Programming section.

DWord	Bit	Description
0	31	**Enable** Access: Double Buffered This field enables this watermark. All the watermarks at this level for all enabled planes must be enabled before the level will be used. Value / Name: 1b: Enable 0b: Disable
	30	**Reserved** Access: Double Buffered
	29:27	**Reserved** Access: RO Format: MBZ
	26:19	**Reserved** Access: RO Format: MBZ

<table>
<tr><th colspan="3">PLANE_WM</th></tr>
<tr><td></td><td>18:14</td><td>Lines

<table><tr><td>Default Value:</td><td>01h</td></tr><tr><td>Access:</td><td>Double Buffered</td></tr></table>This field contains the watermark value in lines. Hardware ignores the lines for the transition watermark.</td></tr>
<tr><td></td><td>13:12</td><td>Reserved

<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td></td><td>11</td><td>Reserved

<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td></td><td>10:0</td><td>Blocks

<table><tr><td>Default Value:</td><td>007h</td></tr><tr><td>Access:</td><td>Double Buffered</td></tr></table>This field contains the watermark value in blocks of 8 cachelines.</td></tr>
</table>

PS_ADAPTIVE_CTRL

PS_ADAPTIVE_CTRL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to PS_WIN_SZ
_Custom_Display _DoubleBufferUpdatePoint:	Start of horizontal blank after armed
Address:	681A8h-681ABh
Name:	PS Adaptive Control Set 0 1
ShortName:	PS_ADAPTIVE_CTRL_SET_0_1_A
Reset:	soft
Address:	681ACh-681AFh
Name:	PS Adaptive Control Set 1 1
ShortName:	PS_ADAPTIVE_CTRL_SET_1_1_A
Reset:	soft
Address:	682A8h-682ABh
Name:	PS Adaptive Control Set 0 1
ShortName:	PS_ADAPTIVE_CTRL_SET_0_2_A
Reset:	soft
Address:	682ACh-682AFh
Name:	PS Adaptive Control Set 1 1
ShortName:	PS_ADAPTIVE_CTRL_SET_1_2_A
Reset:	soft
Address:	689A8h-689ABh
Name:	PS Adaptive Control Set 0 1
ShortName:	PS_ADAPTIVE_CTRL_SET_0_1_B
Reset:	soft
Address:	689ACh-689AFh
Name:	PS Adaptive Control Set 1 1
ShortName:	PS_ADAPTIVE_CTRL_SET_1_1_B
Reset:	soft

PS_ADAPTIVE_CTRL

Address:	68AA8h-68AABh
Name:	PS Adaptive Control Set 0 1
ShortName:	PS_ADAPTIVE_CTRL_SET_0_2_B
Reset:	soft

Address:	68AACh-68AAFh
Name:	PS Adaptive Control Set 1 1
ShortName:	PS_ADAPTIVE_CTRL_SET_1_2_B
Reset:	soft

Address:	691A8h-691ABh
Name:	PS Adaptive Control Set 0 1
ShortName:	PS_ADAPTIVE_CTRL_SET_0_1_C
Reset:	soft

Address:	691ACh-691AFh
Name:	PS Adaptive Control Set 1 1
ShortName:	PS_ADAPTIVE_CTRL_SET_1_1_C
Reset:	soft

Address:	692A8h-692ABh
Name:	PS Adaptive Control Set 0 1
ShortName:	PS_ADAPTIVE_CTRL_SET_0_2_C
Reset:	soft

Address:	692ACh-692AFh
Name:	PS Adaptive Control Set 1 1
ShortName:	PS_ADAPTIVE_CTRL_SET_1_2_C
Reset:	soft

Programming Notes

Recommended threshold programming:
Threshold 1: 1Eh
Threshold 2: 2Dh
Threshold 3: 3Ch

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ

PS_ADAPTIVE_CTRL		
	23:16	**Threshold 3** Access: Double Buffered This field specifies the third threshold value used in adaptive filtering.
	15:8	**Threshold 2** Access: Double Buffered This field specifies the second threshold value used in adaptive filtering.
	7:0	**Threshold 1** Access: Double Buffered This field specifies the first threshold value used in adaptive filtering.

PS_COEF_DATA

PS_COEF_DATA	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to PS_WIN_SZ
_Custom_Display _DoubleBufferUpdatePoint:	Start of horizontal blank after armed
Address:	6819Ch-6819Fh
Name:	PS Coeffecient Set 0 Data 1
ShortName:	PS_COEF_SET_0_DATA_1_A
Reset:	soft
Address:	681A4h-681A7h
Name:	PS Coeffecient Set 1 Data 1
ShortName:	PS_COEF_SET_1_DATA_1_A
Reset:	soft
Address:	6829Ch-6829Fh
Name:	PS Coeffecient Set 0 Data 1
ShortName:	PS_COEF_SET_0_DATA_2_A
Reset:	soft
Address:	682A4h-682A7h
Name:	PS Coeffecient Set 1 Data 1
ShortName:	PS_COEF_SET_1_DATA_2_A
Reset:	soft
Address:	6899Ch-6899Fh
Name:	PS Coeffecient Set 0 Data 1
ShortName:	PS_COEF_SET_0_DATA_1_B
Reset:	soft
Address:	689A4h-689A7h
Name:	PS Coeffecient Set 1 Data 1
ShortName:	PS_COEF_SET_1_DATA_1_B
Reset:	soft
Address:	68A9Ch-68A9Fh
Name:	PS Coeffecient Set 0 Data 1
ShortName:	PS_COEF_SET_0_DATA_2_B
Reset:	soft

PS_COEF_DATA

Address:	68AA4h-68AA7h
Name:	PS Coeffecient Set 1 Data 1
ShortName:	PS_COEF_SET_1_DATA_2_B
Reset:	soft

Address:	6919Ch-6919Fh
Name:	PS Coeffecient Set 0 Data 1
ShortName:	PS_COEF_SET_0_DATA_1_C
Reset:	soft

Address:	691A4h-691A7h
Name:	PS Coeffecient Set 1 Data 1
ShortName:	PS_COEF_SET_1_DATA_1_C
Reset:	soft

Address:	6929Ch-6929Fh
Name:	PS Coeffecient Set 0 Data 1
ShortName:	PS_COEF_SET_0_DATA_2_C
Reset:	soft

Address:	692A4h-692A7h
Name:	PS Coeffecient Set 1 Data 1
ShortName:	PS_COEF_SET_1_DATA_2_C
Reset:	soft

These are the coefficient values for scaler.
The scaler coefficient Index indicates the coefficients array location to be accessed through this register.
The contents of the coefficient array is uninitialized until Software loads the array (i.e. the array is not resetable). Use of the coefficient array or reading from the coefficient array before Software has initialized it will result in non-deterministic behavior or read back data.

Restriction
This register must be written only as a full 32 bit dword. Byte or word writes are not supported.

DWord	Bit	Description
0	31:16	**Coefficient2** Access: Double Buffered Format: SCALER_COEFFICIENT_FORMAT Specifies the value for the second coefficient stored in this dword.
	15:0	**Coefficient1** Access: Double Buffered Format: SCALER_COEFFICIENT_FORMAT Specifies the value for the first coefficient stored in this dword.

PS_COEF_INDEX

PS_COEF_INDEX	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	68198h-6819Bh
Name:	PS Coeffecient Set 0 Index 1
ShortName:	PS_COEF_SET_0_INDEX_1_A
Reset:	soft
Address:	681A0h-681A3h
Name:	PS Coeffecient Set 1 Index 1
ShortName:	PS_COEF_SET_1_INDEX_1_A
Reset:	soft
Address:	68298h-6829Bh
Name:	PS Coeffecient Set 0 Index 1
ShortName:	PS_COEF_SET_0_INDEX_2_A
Reset:	soft
Address:	682A0h-682A3h
Name:	PS Coeffecient Set 1 Index 1
ShortName:	PS_COEF_SET_1_INDEX_2_A
Reset:	soft
Address:	68998h-6899Bh
Name:	PS Coeffecient Set 0 Index 1
ShortName:	PS_COEF_SET_0_INDEX_1_B
Reset:	soft
Address:	689A0h-689A3h
Name:	PS Coeffecient Set 1 Index 1
ShortName:	PS_COEF_SET_1_INDEX_1_B
Reset:	soft
Address:	68A98h-68A9Bh
Name:	PS Coeffecient Set 0 Index 1
ShortName:	PS_COEF_SET_0_INDEX_2_B
Reset:	soft

PS_COEF_INDEX

Address:	68AA0h-68AA3h
Name:	PS Coeffecient Set 1 Index 1
ShortName:	PS_COEF_SET_1_INDEX_2_B
Reset:	soft

Address:	69198h-6919Bh
Name:	PS Coeffecient Set 0 Index 1
ShortName:	PS_COEF_SET_0_INDEX_1_C
Reset:	soft

Address:	691A0h-691A3h
Name:	PS Coeffecient Set 1 Index 1
ShortName:	PS_COEF_SET_1_INDEX_1_C
Reset:	soft

Address:	69298h-6929Bh
Name:	PS Coeffecient Set 0 Index 1
ShortName:	PS_COEF_SET_0_INDEX_2_C
Reset:	soft

Address:	692A0h-692A3h
Name:	PS Coeffecient Set 1 Index 1
ShortName:	PS_COEF_SET_1_INDEX_2_C
Reset:	soft

DWord	Bit	Description
0	31:11	**Reserved** Access: RO Format: MBZ
	10	**Index Auto Increment** Access: R/W This field enables the index auto increment. 0b – No Increment – Do not automatically increment the index value. 1b – Auto Increment **[Default]** – Increment the index value with each read or write to the data register.
	9:6	**Reserved** Access: RO Format: MBZ

PS_COEF_INDEX		
	5:0	**Index Value** Access: R/W This index controls access to the array of scaler coefficient values. Value: [0,59] Name:

PS_CTRL

PS_CTRL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to PS_WIN_SZ
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	68180h-68183h
Name:	PS Control 1
ShortName:	PS_CTRL_1_A
Reset:	soft
Address:	68280h-68283h
Name:	PS Control 1
ShortName:	PS_CTRL_2_A
Reset:	soft
Address:	68980h-68983h
Name:	PS Control 1
ShortName:	PS_CTRL_1_B
Reset:	soft
Address:	68A80h-68A83h
Name:	PS Control 1
ShortName:	PS_CTRL_2_B
Reset:	soft
Address:	69180h-69183h
Name:	PS Control 1
ShortName:	PS_CTRL_1_C
Reset:	soft
Address:	69280h-69283h
Name:	PS Control 1
ShortName:	PS_CTRL_2_C
Reset:	soft
Description	

PS_CTRL

The pipe scalers are used to scale the output of a display pipe or of a display plane. All pipes have two scalers each.
The scaler preserves 8 bits of alpha and 10 bits of each color channel for plane scaling and 12 bits of each color channel for pipe scaling.
The scalers can be assigned to any plane (except cursor) output or the output of the display pipe (after blending and color correction, before dithering and color clamping).
Downscale usages have scale factor restrictions:

- All scaler modes support a downscale factor of less than 3.0 in each direction.
- When configured for Pipe YUV 420 encoding for port output, limit downscaling to less than 1.5 (source/destination) in the horizontal direction and 1.0 in the vertical direction

Beyond the restrictions of the Scaler output fitting within the destination window size, there are effectively no upscale restrictions except for the following:
(Scale Factor) * 2^{15} >= 1.0
Where the Scale Factor = (Source Size) / (Destination Size)

The scalers support horizontal source sizes up to 5120 and vertical source sizes up to 4096.

Programming Notes

The scalers must not be enabled when the horizontal source sizes are greater than 5120 and the vertical sizes greater than 4320.

Driver is responsible for making sure all the plane, pipe, and scaler size registers are programmed appropriately and gets applied atomically to the same frame since hardware does not ensure an atomic update of plane, scaler, and pipe source size registers.

When scaling a pipe, the scaler window size and position must fit within the pipe active size. If there is a seam present (i.e. PIPE_SEAM_EXCESS is non-zero), then the pipe's horizontal active size that the scaler sees is the horizontal active size defined within the TRANS_HTOTAL register plus the amount(s) specified within the PIPE_SEAM_EXCESS.
Pipe Horizontal Active = Horizontal Active + Left Excess Amount + Right Excess Amount

Refer to 'YUV 420 Support' page for scaler restrictions with YUV 420 pipe output.

Restriction

Down scaling (scaler input size is larger than scaler window size) can reduce the maximum supported pixel rate for a pipe as well as increase the watermark and data buffer requirements. Refer to the Display Resolution Support page and Watermark Calculations page for detailed calculations.

Scaler 1 and 2 must not be both scaling the same plane output.
When scaling a pipe, the scaler window size and position must fit within the pipe active size.
When scaling a plane, the plane position must be programmed to 0 and the scaler window size and position must fit within the pipe source size.
When scaling is enabled, the scaler input width should be a minimum of 8 pixels and the height should be minimum of 8 scanlines.
When the plane scaling is used with YUV 420 planar formats, the height should be a minimum of 16 scanlines.
When using down scaling (scaler input size is larger than scaler output size) the maximum supported pixel rate will be reduced by the down scale amount.

<table>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td>0</td><td>31</td><td>Enable Scaler

<table><tr><td>Access:</td><td>Double Buffered</td></tr></table>This field enables the scaler.
<table><tr><th>Value</th><th>Name</th></tr><tr><td>0b</td><td>Disable</td></tr><tr><td>1b</td><td>Enable</td></tr></table></td></tr>
<tr><td></td><td>30</td><td>Reserved

<table><tr><td>Access:</td><td>Double Buffered</td></tr></table></td></tr>
<tr><td></td><td>29</td><td>Reserved

<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td></td><td>28</td><td>Adaptive Filtering

<table><tr><td>Access:</td><td>Double Buffered</td></tr></table>This field enables the scaler adaptive vertical and horizontal filtering. When adaptive filtering is enabled, the adaptive threshold values must be programmed in the PS_ADAPTIVE_CTRL register and the Filter Set Select bits should be programmed.
<table><tr><th>Value</th><th>Name</th></tr><tr><td>0h</td><td>Disable</td></tr><tr><td>1h</td><td>Enable</td></tr></table></td></tr>
<tr><td></td><td>27:25</td><td>Scaler Binding

<table><tr><td>Access:</td><td>Double Buffered</td></tr></table>This field selects the where the scaling operation is done. When scaling a pipe, the pipe source size specifies the input size to the scaler. When scaling a plane, the PLANE_SIZE specifies the input size to the scaler. Any border around a scaled plane window will become transparent at the plane blender.
<table><tr><th>Value</th><th>Name</th></tr><tr><td>000b</td><td>Pipe Scaler</td></tr><tr><td>001b</td><td>Plane 1 Scaler</td></tr><tr><td>010b</td><td>Plane 2 Scaler</td></tr><tr><td>011b</td><td>Plane 3 Scaler</td></tr><tr><td>100b</td><td>Plane 4 Scaler</td></tr><tr><td>101b</td><td>Plane 5 Scaler</td></tr></table></td></tr>
</table>

PS_CTRL

		Programming Notes When plane scaling is enabled on planes 1 through 3, make sure that the *PLANE_CUS_CTL.Plane Scaling Enabled* (bit 30) is programmed correctly. **Restriction** The scaler input size should be at least 8 scanlines. Plane/Pipe scaling is not compatible with interlaced fetch mode. Plane up and down scaling is not compatible with keying. Keying can be enabled with 1:1 plane scaling. Plane scaling is not compatible with the Indexed 8-bit, XR_BIAS, or any pixel values less than 0 or greater than 1.
	24:23	**FILTER SELECT** Access: Double Buffered This field selects filter coefficients. The medium coefficients will provide an unfiltered image when the scale factor is 1:1. In the programmed mode, the filter coefficients must be programmed using the PS_COEF_INDEX and PS_COEF_DATA registers and the Filter Set Select bits should be programmed. **Value** / **Name** 00b: Medium 01b: Programmed 10b: Edge Enhance 11b: Bilinear
	22	**ADAPTIVE FILTER SELECT** Access: Double Buffered This field selects the filter coefficients used for adaptive filtering. The field is ignored when adaptive filtering is not enabled. **Value** / **Name** 0b: Medium 1b: Edge Enhance
	21	**Pipe Scaler Location** Access: Double Buffered This field selects where the pipe scaling is done in the pipe. **Value** / **Name** / **Description** 0b: After Output CSC: This is a non-linear tap point 1b: After CSC: This is a linear tap point

PS_CTRL

		Restriction The HDR Mode cannot be enabled for the Pipe(PIPE_MISC[23] = 0), when the Scaler is bound to the linear tap point
	20	**Reserved** Access: Double Buffered
	19	**Reserved** Access: Double Buffered
	18	**Reserved** Access: RO Format: MBZ
	17	**Reserved** Access: Double Buffered
	16	**Reserved** Access: RO Format: MBZ
	15	**Reserved** Access: Double Buffered
	14	**Reserved** Access: RO Format: MBZ
	13:12	**Reserved** Access: Double Buffered
	11:10	**Reserved** Access: RO Format: MBZ
	9	**Allow Double Buffer Update Disable** Access: R/W This field controls whether double buffer updates are allowed to be disabled for this scaler. The DOUBLE_BUFFER_CTL register can be configured to globally disable double

buffer updates for resources that allow them to be disabled.

Value	Name
0b	Not Allowed
1b	Allowed **[Default]**

8 Reserved

Access:	Double Buffered

7:5 Reserved

Access:	RO
Format:	MBZ

4 Y Vert Filter Set Sel

Access:	Double Buffered

This field selects the programmed coefficient set and/or the adaptive threshold set used by the Y component vertical filter when filtering YUV planar formats. This field is ignored with other formats.

Value	Name
0b	Set 0 **[Default]**
1b	Set 1

3 Y Horz Filter Set Sel

Access:	Double Buffered

This field selects the programmed coefficient set and/or the adaptive threshold set used by the Y component horizontal filter when filtering YUV hybrid planar formats. This field is ignored with other formats.

Value	Name
0b	Set 0 **[Default]**
1b	Set 1

2 UV Vert Filter Set Sel

Access:	Double Buffered

This field selects the programmed coefficient set and/or the adaptive threshold set used by the UV component vertical filter when filtering YUV hybrid planar formats. With other formats, this field selects the coefficient set and/or the adaptive threshold set used by the vertical filter.

Value	Name
0b	Set 0 **[Default]**
1b	Set 1

PS_CTRL

	1	**UV Horz Filter Set Sel** Access: Double Buffered This field selects the programmed coefficient set and/or the adaptive threshold set used by the UV component horizontal filter when filtering YUV hybrid planar formats. With other formats, this field selects the coefficient set and/or the adaptive threshold set used by the horizontal filter. **Value** / **Name** 0b: Set 0 **[Default]** 1b: Set 1
	0	**Reserved** Access: RO Format: MBZ

PS_ECC_STAT

PS_ECC_STAT	
Register Space:	MMIO: 0/2/0
Access:	R/WC
Size (in bits):	32
Address:	681D0h-681D3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_1_A
Reset:	soft
Address:	682D0h-682D3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_2_A
Reset:	soft
Address:	689D0h-689D3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_1_B
Reset:	soft
Address:	68AD0h-68AD3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_2_B
Reset:	soft
Address:	691D0h-691D3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_1_C
Reset:	soft
Address:	692D0h-692D3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_2_C
Reset:	soft

Each of these fields is a sticky bit that gives the ECC error status for a particular memory bank. A '1' in a bit indicates that ECC detected an error. A write of '1' to a bit will clear the bit. Single errors are corrected by ECC. Double errors are not correctable.

DWord	Bit	Description
0	31:17	**Reserved** Access: RO Format: MBZ

PS_ECC_STAT		
	16	**Double Error Detected** Access: R/WC
	15:1	**Reserved** Access: RO Format: MBZ
	0	**Single Error Detected** Access: R/WC

PS_HPHASE

PS_HPHASE	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to PS_WIN_SZ
_Custom_Display _DoubleBufferUpdatePoint:	Start of horizontal blank after armed
Address:	68194h-68197h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_1_A
Reset:	soft
Address:	68294h-68297h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_2_A
Reset:	soft
Address:	68994h-68997h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_1_B
Reset:	soft
Address:	68A94h-68A97h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_2_B
Reset:	soft
Address:	69194h-69197h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_1_C
Reset:	soft
Address:	69294h-69297h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_2_C
Reset:	soft

PS_HPHASE

Description
This register programs the scaler horizontal filtering initial phase. The initial phase within the -0.5 to 1.5 range is supported. Refer to PS_VPHASE for programming details.
The programming of this register is ignored by the pipe scaler when the pipe is in the Full Blend YUV420 mode. The scaler hardware is responsible for calculating and applying the appropriate horizontal phase when encoding the YUV420 format.

DWord	Bit	Description
0	31:30	**Y Initial HPhase Int** Access: Double Buffered This field specifies the integer part of the Y horizontal filtering initial phase when the scaler is operating on YUV420 hybrid planar formats. This field is ignored for non-YUV420 pixel formats.
	29:17	**Y Initial HPhase Frac** Access: Double Buffered This field specifies the most significant 13 bits of the fractional part of the Y horizontal filtering initial phase when the scaler is operating onYUV420 hybrid planar formats. This field should be programmed with the fractional portion of the initial phase multiplied by 2^13. This field is ignored for non-YUV420 pixel formats.
	16	**Y Initial HPhase Trip** Access: Double Buffered This field specifies whether the initial trip, that may occur while applying the initial phase, is used in Y horizontal filtering. This field is ignored for non-YUV420 pixel formats. Value: 1b — Name: Enable Value: 0b — Name: Disable
	15:14	**UV or RGB Initial HPhase Int** Access: Double Buffered This field specifies the integer part of the UV or RGB horizontal filtering initial phase.

<table>
<tr><th colspan="3">PS_HPHASE</th></tr>
<tr><td></td><td>13:1</td><td>UV or RGB Initial HPhase Frac

<table><tr><td>Access:</td><td>Double Buffered</td></tr></table>This field specifies the most significant 13 bits of the fractional part of the UV or RGB horizontal filtering initial phase.
This field should be programmed with the fractional portion of the initial phase multiplied by 2^13.</td></tr>
<tr><td></td><td>0</td><td>UV or RGB Initial HPhase Trip

<table><tr><td>Access:</td><td>Double Buffered</td></tr></table>This field specifies whether the initial trip, that may occur while applying the initial phase, is used in UV or RGB horizontal filtering.<table><tr><th>Value</th><th>Name</th></tr><tr><td>1b</td><td>Enable</td></tr><tr><td>0b</td><td>Disable</td></tr></table></td></tr>
</table>

PS_HSCALE

PS_HSCALE		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	68190h-68193h	
Name:	PS Horizontal Scale 1	
ShortName:	PS_HSCALE_1_A	
Reset:	soft	
Address:	68290h-68293h	
Name:	PS Horizontal Scale 1	
ShortName:	PS_HSCALE_2_A	
Reset:	soft	
Address:	68990h-68993h	
Name:	PS Horizontal Scale 1	
ShortName:	PS_HSCALE_1_B	
Reset:	soft	
Address:	68A90h-68A93h	
Name:	PS Horizontal Scale 1	
ShortName:	PS_HSCALE_2_B	
Reset:	soft	
Address:	69190h-69193h	
Name:	PS Horizontal Scale 1	
ShortName:	PS_HSCALE_1_C	
Reset:	soft	
Address:	69290h-69293h	
Name:	PS Horizontal Scale 1	
ShortName:	PS_HSCALE_2_C	
Reset:	soft	

DWord	Bit	Description
0	31:18	**Reserved** Access: RO Format: MBZ

PS_HSCALE		
	17:15	**HScale Int** Access: RO This field gives the integer part of the horizontal scaling factor divided by the oversampling rate. HSCALE_INT = int(src width/dest width)
	14:0	**HScale Frac** Access: RO This field gives the fractional part of the horizontal scaling factor divided by the oversampling rate. HSCALE_FRAC = int((((src width/dest width)-HSCALE_INT) * 2^^15) + 0.5)

PS_PROG_HSCALE

PS_PROG_HSCALE	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to PS_WIN_SZ
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	68168h-6816Bh
Name:	PS Programmed Horizontal Scale 1
ShortName:	PS_PROG_HSCALE_1_A
Reset:	soft
Address:	68268h-6826Bh
Name:	PS Programmed Horizontal Scale 1
ShortName:	PS_PROG_HSCALE_2_A
Reset:	soft
Address:	68968h-6896Bh
Name:	PS Programmed Horizontal Scale 1
ShortName:	PS_PROG_HSCALE_1_B
Reset:	soft
Address:	68A68h-68A6Bh
Name:	PS Programmed Horizontal Scale 1
ShortName:	PS_PROG_HSCALE_2_B
Reset:	soft
Address:	69168h-6916Bh
Name:	PS Programmed Horizontal Scale 1
ShortName:	PS_PROG_HSCALE_1_C
Reset:	soft
Address:	69268h-6926Bh
Name:	PS Programmed Horizontal Scale 1
ShortName:	PS_PROG_HSCALE_2_C
Reset:	soft

This register is used to specify the horizontal scale factor when Programmable Scale Factor is enabled.

DWord	Bit	Description
0	31:18	**Reserved** Access: RO

PS_PROG_HSCALE			
		Format:	MBZ
	17:15	**HScale Int** Access: Double Buffered This field gives the integer part of the horizontal scaling factor divided by the oversampling rate. HSCALE_INT = int(src width/dest width)	
	14:0	**HScale Frac** Access: Double Buffered This field gives the fractional part of the horizontal scaling factor divided by the oversampling rate. HSCALE_FRAC = int(((src width/dest width)-HSCALE_INT)*2^^15)	

PS_PROG_VSCALE

PS_PROG_VSCALE	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to PS_WIN_SZ
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	68164h-68167h
Name:	PS Programmed Vertical Scale 1
ShortName:	PS_PROG_VSCALE_1_A
Reset:	soft
Address:	68264h-68267h
Name:	PS Programmed Vertical Scale 1
ShortName:	PS_PROG_VSCALE_2_A
Reset:	soft
Address:	68964h-68967h
Name:	PS Programmed Vertical Scale 1
ShortName:	PS_PROG_VSCALE_1_B
Reset:	soft
Address:	68A64h-68A67h
Name:	PS Programmed Vertical Scale 1
ShortName:	PS_PROG_VSCALE_2_B
Reset:	soft
Address:	69164h-69167h
Name:	PS Programmed Vertical Scale 1
ShortName:	PS_PROG_VSCALE_1_C
Reset:	soft
Address:	69264h-69267h
Name:	PS Programmed Vertical Scale 1
ShortName:	PS_PROG_VSCALE_2_C
Reset:	soft

This register is used to specify the vertical scale factor when Programmable Scale Factor is enabled.

DWord	Bit	Description
0	31:18	**Reserved** Access: RO

PS_PROG_VSCALE			
		Format:	MBZ
	17:15	**VScale Int** Access: Double Buffered This field gives the integer part of the vertical scale factor. VSCALE_INT = int(src height/(interlace x dest height)) Interlace = 1/2 in interlace modes, 1 in progressive modes.	
	14:0	**VScale Frac** Access: Double Buffered This field gives the fractional part of the vertical scale factor. VSCALE_FRAC = int((src height/(interlace x dest height)-VSCALE_INT)*2^^15) Interlace = 1/2 in interlace modes, 1 in progressive modes.	

PS_PWR_GATE

PS_PWR_GATE	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to PS_WIN_SZ
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	68160h-68163h
Name:	Power Gate Control 1
ShortName:	PS_PWR_GATE_1_A
Reset:	soft
Address:	68260h-68263h
Name:	Power Gate Control 1
ShortName:	PS_PWR_GATE_2_A
Reset:	soft
Address:	68960h-68963h
Name:	Power Gate Control 1
ShortName:	PS_PWR_GATE_1_B
Reset:	soft
Address:	68A60h-68A63h
Name:	Power Gate Control 1
ShortName:	PS_PWR_GATE_2_B
Reset:	soft
Address:	69160h-69163h
Name:	Power Gate Control 1
ShortName:	PS_PWR_GATE_1_C
Reset:	soft
Address:	69260h-69263h
Name:	Power Gate Control 1
ShortName:	PS_PWR_GATE_2_C
Reset:	soft

DWord	Bit	Description
0	31	**Reserved** Access: Double Buffered

PS_PWR_GATE

	30	**Reserved** Access: RO Format: MBZ
	29:6	**Reserved** Access: RO Format: MBZ
	5	**Dynamic Pwr Gate Disable** Access: Double Buffered Disables the dynamic power gate of unused EBB's when processing low resolution source images. 0b: Do Not Disable **[Default]** 1b: Disable
	4:3	**Reserved** Access: Double Buffered
	2	**Reserved** Access: RO Format: MBZ
	1:0	**Reserved** Access: Double Buffered

PS_VPHASE

PS_VPHASE	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to PS_WIN_SZ
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	68188h-6818Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_1_A
Reset:	soft
Address:	68288h-6828Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_2_A
Reset:	soft
Address:	68988h-6898Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_1_B
Reset:	soft
Address:	68A88h-68A8Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_2_B
Reset:	soft
Address:	69188h-6918Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_1_C
Reset:	soft
Address:	69288h-6928Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_2_C
Reset:	soft

PS_VPHASE

Description

This register programs the scaler vertical filtering initial phase. The programming of this register is ignored in the pipe scaler PF/ID fetch mode, and the pipe scaler is responsible for applying the appropriate vertical phase to the proper frame when interlacing.
The initial phase within the -0.5 to 1.5 range is supported.
Programming +ve initial phase:

- Initial Phase Trip = 1b
- Initial Phase Int = Desired Initial Phase Int
- Initial Phase Frac = Desired Initial Phase Frac

Programming -ve initial phase:

- Initial Phase Trip = 0b
- Initial Phase Int = 00b
- Initial Phase Frac = 1 - Desired Initial Phase Frac

For example, -0.25 initial phase should be programmed as

- Initial Phase Trip = 0b
- Initial Phase Int = 00b
- Initial Phase Frac = 1 - 0.25 = 0.75

The following table shows phase programming for frequently used YUV420 to YUV444 chroma upsampling scenarios (chroma being filtered to the center of the pixel).

YUV 420 Chroma Siting	H Phase	V Phase	Programmed H Initial Phase	Programmed H Initial Trip	Programmed V Initial Phase	Programmed V Initial Trip
Top Left	0.25	0.25	0.25	1	0.25	1
Bottom Right (MPEG-1)	-0.25	-0.25	0.75	0	0.75	0
Bottom Center (MPEG-2)	0	-0.25	0	0	0.75	0

The programming of this register is ignored by a pipe scaler when the pipe is in the Full Blend YUV420 mode. The scaler hardware is responsible for calculating and applying the appropriate vertical phase when encoding the YUV420 format.

DWord	Bit	Description
0	31:30	**Y Initial VPhase Int** Access: Double Buffered This field specifies the integer part of the Y vertical filtering initial phase when the scaler is operating on YUV420 hybrid planar formats. This field is ignored for non-YUV420 pixel formats.

PS_VPHASE

	29:17	**Y Initial VPhase Frac** Access: Double Buffered This field specifies the most significant 13 bits of the fractional part of the Y vertical filtering initial phase when the scaler is operating on YUV420 hybrid planar formats. This field should be programmed with the fractional portion of the initial phase multiplied by 2^13. This field is ignored for non-YUV420 pixel formats.
	16	**Y Initial VPhase Trip** Access: Double Buffered This field specifies whether the initial trip, that may occur while applying the initial phase, is used in Y vertical filtering. This field is ignored for non-YUV420 pixel formats. **Value** / **Name** 1b: Used 0b: Not Used
	15:14	**UV or RGB Initial VPhase Int** Access: Double Buffered This field specifies the integer part of the UV or RGB vertical filtering initial phase.
	13:1	**UV or RGB Initial VPhase Frac** Access: Double Buffered This field specifies the most significant 13 bits of the fractional part of the UV or RGB vertical filtering initial phase. This field should be programmed with the fractional portion of the initial phase multiplied by 2^13.
	0	**UV or RGB Initial VPhase Trip** Access: Double Buffered This field specifies whether the initial trip, that may occur while applying the initial phase, is used in UV or RGB vertical filtering. **Value** / **Name** 1b: Used 0b: Not Used

PS_VSCALE

PS_VSCALE	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	68184h-68187h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_1_A
Reset:	soft
Address:	68284h-68287h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_2_A
Reset:	soft
Address:	68984h-68987h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_1_B
Reset:	soft
Address:	68A84h-68A87h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_2_B
Reset:	soft
Address:	69184h-69187h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_1_C
Reset:	soft
Address:	69284h-69287h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_2_C
Reset:	soft

DWord	Bit	Description	
0	31:18	**Reserved**	
		Access:	RO
		Format:	MBZ

PS_VSCALE		
	17:15	**VScale Int** Access: RO This field gives the integer part of the vertical scale factor. VSCALE_INT = int(src height/(interlace x dest height)) Interlace = 1/2 in interlace modes, 1 in progressive modes.
	14:0	**VScale Frac** Access: RO This field gives the fractional part of the vertical scale factor. VSCALE_FRAC = int(((src height/(interlace x dest height)-VSCALE_INT) * 2^^15) + 0.5) Interlace = 1/2 in interlace modes, 1 in progressive modes.

PS_WIN_POS

PS_WIN_POS	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to PS_WIN_SZ
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	68170h-68173h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_1_A
Reset:	soft
Address:	68270h-68273h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_2_A
Reset:	soft
Address:	68970h-68973h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_1_B
Reset:	soft
Address:	68A70h-68A73h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_2_B
Reset:	soft
Address:	69170h-69173h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_1_C
Reset:	soft
Address:	69270h-69273h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_2_C
Reset:	soft
Coordinates are determined with a value of (0,0) being the upper left corner of the display device (rotation does not affect this).	

PS_WIN_POS

Restriction
When scaling a pipe, the scaled output must fit inside the pipe active area, so Pipe active size >= PS window position + PS window size. When scaling a plane, the scaled output must fit inside the pipe source area, so Pipe source size >= PS window position + PS window size.

DWord	Bit	Description
0	31:29	**Reserved** Access: RO Format: MBZ
	28:16	**XPOS** Access: Double Buffered This field specifies the horizontal coordinate in pixels of the upper left most pixel of the scaled output window. Restriction: This field must be even when the scaler is delivering a YUV420 format to the ports (i.e. encoding YUV420, or chroma down-sampling).
	15:13	**Reserved** Access: RO Format: MBZ
	12:0	**YPOS** Access: Double Buffered This field specifies the vertical coordinate in lines of the upper left most pixel of the scaled output window. **Restriction** Bit 0 must be zero for interlaced modes. This field must be even when the scaler is delivering a YUV420 format to the ports (i.e. encoding YUV420, or chroma down-sampling).

PS_WIN_SZ

PS_WIN_SZ	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank
Address:	68174h-68177h
Name:	PS Window Size 1
ShortName:	PS_WIN_SZ_1_A
Reset:	soft
Address:	68274h-68277h
Name:	PS Window Size 1
ShortName:	PS_WIN_SZ_2_A
Reset:	soft
Address:	68974h-68977h
Name:	PS Window Size 1
ShortName:	PS_WIN_SZ_1_B
Reset:	soft
Address:	68A74h-68A77h
Name:	PS Window Size 1
ShortName:	PS_WIN_SZ_2_B
Reset:	soft
Address:	69174h-69177h
Name:	PS Window Size 1
ShortName:	PS_WIN_SZ_1_C
Reset:	soft
Address:	69274h-69277h
Name:	PS Window Size 1
ShortName:	PS_WIN_SZ_2_C
Reset:	soft
This register specifies the size in pixels of the scaled output window. A programmed value of (100, 100) will result in scaled output window of size 100x100 pixels. **Writes to this register arm PS registers on this pipe.** After arming, any write to other PS registers will disarm all PS registers. Subsequent write to this register will arm them again.	

PS_WIN_SZ

Restriction
When scaling a pipe, the scaled output must fit inside the pipe active area, so Pipe active size >= PS window position + PS window size. When scaling a plane, the scaled output must fit inside the pipe source area, so Pipe source size >= PS window position + PS window size.

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29:16	**XSIZE** Access: Double Buffered This field specifies the horizontal size in pixels of the scaled output window. Restriction: When the pipe scalar is configured to output YUV 420, the X size must be even.
	15:13	**Reserved** Access: RO Format: MBZ
	12:0	**YSIZE** Access: Double Buffered This field specifies the vertical size in scan lines of the scaled output window. Restriction: Bit 0 must be zero for interlaced modes. **Restriction** When the pipe scalar is configured to output YUV 420, the Y size must be even.

PSR_EVENT

PSR_EVENT	
Register Space:	MMIO: 0/2/0
Access:	R/WC
Size (in bits):	32
Address:	60848h-6084Bh
Name:	Transcoder PSR Event
ShortName:	PSR_EVENT_A
Reset:	soft
Address:	61848h-6184Bh
Name:	Transcoder PSR Event
ShortName:	PSR_EVENT_B
Reset:	soft
Address:	62848h-6284Bh
Name:	Transcoder PSR Event
ShortName:	PSR_EVENT_C
Reset:	soft
Address:	63848h-6384Bh
Name:	Transcoder PSR Event
ShortName:	PSR_EVENT_D
Reset:	soft

This register captures the event that caused an exit from PSR or PSR2. The exit events will be set by hardware. Software will need to clear these events.

DWord	Bit	Description
0	31:18	**Reserved** Access: RO Format: MBZ
	17	**PSR2 watch dog timer expire** Access: R/WC This is a sticky bit which is set when the PSR2 watch dog timer expires, causing PSR exit. Clear by writing with a 1. Value / Name: 0b – Condition Not Detected 1b – Condition Detected

PSR_EVENT

	16	**PSR2 Disable** Access: R/WC This is a sticky bit which is set when the PSR2 is disabled, causing PSR exit. Clear by writing with a 1. **Value** / **Name** 0b: Condition Not Detected 1b: Condition Detected
	15	**Selective Update Dirty FIFO Underrun** Access: R/WC This is a sticky bit which is set when the selective update dirty/clean FIFO Underruns, causing PSR exit. Clear by writing with a 1. **Value** / **Name** 0b: Condition Not Detected 1b: Condition Detected
	14	**Selective Update CRC FIFO Underrun** Access: R/WC This is a sticky bit which is set when the selective update CRC FIFO Underruns, causing PSR exit. Clear by writing with a 1. **Value** / **Name** 0b: Condition Not Detected 1b: Condition Detected
	13	**Reserved** Access: RO Format: MBZ
	12	**Graphics Reset** Access: R/WC This is a sticky bit which is set when a graphics reset causes PSR exit. Clear by writing with a 1. **Value** / **Name** 0b: Condition Not Detected 1b: Condition Detected

PSR_EVENT

11	**PCH Interrupt** Access: R/WC This is a sticky bit which is set when a PCH Interrupt causes PSR exit. Clear by writing with a 1. Value: 0b — Name: Condition Not Detected Value: 1b — Name: Condition Detected
10	**Memory Up** Access: R/WC This is a sticky bit which is set when a PCU memup up event causes PSR exit. Clear by writing with a 1. Value: 0b — Name: Condition Not Detected Value: 1b — Name: Condition Detected
9	**Front Buffer Modify** Access: R/WC This is a sticky bit which is set when a front buffer modify causes PSR exit. Clear by writing with a 1. Value: 0b — Name: Condition Not Detected Value: 1b — Name: Condition Detected
8	**Watch dog timer expire** Access: R/WC This is a sticky bit which is set when the PSR watch dog timer expires, causing PSR exit. Clear by writing with a 1. Value: 0b — Name: Condition Not Detected Value: 1b — Name: Condition Detected
7	**Reserved** Access: RO Format: MBZ

PSR_EVENT

	6	**Pipe Registers Update** Access: R/WC This is a sticky bit which is set when a display pipe register update causes PSR exit. Clear by writing with a 1.
	5	**Reserved** Access: RO Format: MBZ
	4	**Reserved** Access: R/WC
	3	**KVMR session enable** Access: R/WC This is a sticky bit which is set when a KVMR session is enabled, causing PSR exit. Clear by writing with a 1. Value: 0b – Condition Not Detected Value: 1b – Condition Detected
	2	**VBI enable** Access: R/WC This is a sticky bit which is set when vblank or vsync interrupt is enabled, causing PSR exit. Clear by writing with a 1. Value: 0b – Condition Not Detected Value: 1b – Condition Detected
	1	**LPSP mode exit** Access: R/WC This is a sticky bit which is set when LPSP mode is exited, causing PSR exit. This bit is reserved for DDIs. Clear by writing with a '1'. Value: 0b – Condition not detected Value: 1b – Condition detected

PSR_EVENT		
	0	**SRD disable** Access: R/WC This is a sticky bit which is set when SRD enable is cleared, causing PSR exit. Clear by writing with a 1. Value / Name 0b: Condition Not Detected 1b: Condition Detected

PSR2_CTL

PSR2_CTL

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60900h-60903h
Name:	PSR2 Control
ShortName:	PSR2_CTL_A
Reset:	soft

Programming Notes

To use FBC modification tracking for idleness calculations when FBC is disabled, program FBC_CTL CPU Fence Enable, FBC_CONTROL_SA_REGISTER, FBC_CPU_FENCE_OFFSET_REGISTER, FBC_RT_BASE_ADDR_REGISTER, and BLITTER_TRACKING_REGISTER as they are programmed when FBC is enabled.

Restriction

PSR needs to be enabled only when at least one plane is enabled.

PSR2 is limited to 30bpp 10:10:10, even when using the manual tracking mode.

Only the PSR2 Enable can be changed while PSR2 is enabled. The other fields must not be changed while PSR2 is enabled. Selective Update Tracking Enable must be set before or along with PSR2 enable

PSR2 is supported for pipe active sizes up to 5120 pixels wide and 3200 lines tall.

DWord	Bit	Description
0	31	**PSR2 Enable** Access: R/W This bit enables Revision 2.0 of the Panel Self Refresh function. Updates will take place at the start of the next vertical blank. The port will send PSR2 VDMs while enabled.

Value	Name
0b	Disable
1b	Enable

Programming Notes

Clear the register field SRD_CTL [TP2 TP3 Select] before enabling this bit.
Do not set the register field SRD_CTL [TP2 TP3 Select] while PSR2 is enabled.

Restriction

PSR2 must not be enabled when the PSR Setup time from DPCD 00071h is greater than the time for vertical blank minus one line.

PSR2 must not be enabled together with Interlacing, Black Frame Insertion (BFI), Compression Mode, or S3D.

Disable FBC when PSR2 is enabled.

PSR2_CTL

30 Reserved

Access:	RO
Format:	MBZ

29 Context restore to PSR2 Deep Sleep State

Access:	R/W

This field restores PSR2 into Deep Sleep State

Value	Name
0b	Disable
1b	Enable

Restriction
This bit should only be used with context save restore.

28 Block count number

Access:	R/W

This field selects block count number before SU turn on sequence

Value	Name
0b	2 blocks OR 8 lines
1b	3 blocks OR 12 lines

27 Aux Frame Sync Enable

Access:	R/W

This field selects whether the frame sync will be sent on Aux channel.

Value	Name
1b	Enable
0b	Disable

Restriction
Must be programmed to match the panel's requirements.

26 Y-coordinate valid

Access:	R/W

This field selects whether PSR2 Y-coordinate valid behaves as per eDP 1.4a

Value	Name
0b	Include Y-coordinate valid eDP1.4a
1b	Do not include Y-coordinate valid eDP 1.4

PSR2_CTL

	25	**Y-coordinate enable** Access: R/W This field selects whether PSR2 VSC packet will include vertical line count. Value: 0b — Do not include count Value: 1b — Include count
	24:20	**Max SU Disable Time** Default Value: 00000b Disabled Access: R/W This field is the maximum time to spend in PSR2 Selective update without fetching a full frame. It is programmed in increments of sixty frames. Programming all 1s gives 31x60 frames time. Restriction: Programming all 0s disable the forced fetch of a full frame in SU.
	19	**Reserved** Access: R/W
	18	**PSR2 RAM power state** Access: RO
	17:16	**Reserved** Access: R/W
	15:13	**IO buffer Wake** Access: R/W This field selects the number of lines before the Selective Update Region to wake the IO Buffers. Value: 000b — 5 lines Value: 001b — 6 lines Value: 010b — 7 lines **[Default]** Value: 011b — 8 lines Value: 100b — 9 lines Value: 101b — 10 lines Value: 110b — 11 lines Value: 111b — 12 lines

PSR2_CTL

		Restriction To program line 9 to 12, block count number bit [28] must be set.
	12:10	**Fast Wake** Access: R/W This field selects the number of lines before the Selective Update Region to send the Fast Wake. **Value** / **Name** 000b: 5 lines 001b: 6 lines 010b: 7 lines **[Default]** 011b: 8 lines 100b: 9 lines 101b: 10 lines 110b: 11 lines 111b: 12 lines **Restriction** To program line 9 to 12, block count number bit [28] must be set.
	9:8	**TP2 Time** Access: R/W This field selects the TP2 time when training the link on exit from PSR2 DeepSleep (waking). **Value** / **Name** 00b: 500us 01b: 100us 10b: 2.5ms 11b: 50us
	7:4	**Frames Before SU Entry** Default Value: 0001b 1 Frames Before SU Entry Access: R/W This field is the number of frames it takes to enter into Selective Update when PSR2 is enabled. Note: HW takes a minimum of 2frames, so'0' and '1' are are not valid entries for this field.

PSR2_CTL

	3:0	**Idle Frames** Access: R/W This field is the number of idle frames required before entering PSR2 Deep Sleep. Write to this field doesn't cause a PSR2 exit and frame update. **Value** / **Name** 0000b: Deep Sleep Disabled 0001b: 1 idle frame **[Default]**

PWR_WELL_CTL

PWR_WELL_CTL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	45400h-45403h
Name:	Power Well Control 1
ShortName:	PWR_WELL_CTL1
Reset:	soft
CrashLogSaved:	true
CrashLogPriority:	2
CrashLogVisibility:	public
ExternalLongName:	DE Power Well Control 1
ExternalDescription:	Display engine power well control
Address:	45404h-45407h
Name:	Power Well Control 2
ShortName:	PWR_WELL_CTL2
Reset:	soft

This register is used for display power control. There are multiple instances of this register format to allow software components to have parallel control of the display power.
PWR_WELL_CTL1 is generally used for BIOS to control power.
PWR_WELL_CTL2 is generally used for driver to control power.
The power enable requests from all sources are logically ORd together to enable the power, so the power will only disable after all sources have requested the power to disable.
When a power well is disabled (powered down), access to any registers in the power well will complete but write data will be dropped and read data will be all zeroes.
The display connections diagram indicates which functional blocks are contained in each power well. The display MMIO register specification has a field for each register to indicate which power well it is in.

Restriction
The power request field must not be changed for a resource while a power enable/disable for that resource is currently in progress, as indicated by power well state for that resource.
Power wells must be enabled and disabled following the display initialization and mode set sequences.

DWord	Bit	Description
0	31:22	**Reserved** Access: RO Format: MBZ

PWR_WELL_CTL

	21:8	**Reserved** Access: RO Format: MBZ
	7	**Power Well 4 Request** Access: R/W This field requests power well to enable or disable. 0b: Disable 1b: Enable
	6	**Power Well 4 State** Access: RO This field indicates the status of power well. 0b: Disabled 1b: Enabled
	5	**Power Well 3 Request** Access: R/W This field requests power well to enable or disable. 0b: Disable 1b: Enable
	4	**Power Well 3 State** Access: RO This field indicates the status of power well. 0b: Disabled 1b: Enabled
	3:2	**Reserved** Access: RO Format: MBZ
	1	**Power Well 1 Request** Access: R/W

PWR_WELL_CTL

		This field requests power well to enable or disable. **Value** / **Name** 0b – Disable 1b – Enable
	0	**Power Well 1 State** Access: RO This field indicates the status of power well. **Value** / **Name** 0b – Disabled 1b – Enabled

SEL_FETCH_PLANE_CTL

SEL_FETCH_PLANE_CTL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display _DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display _DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	70890h-70893h
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_1_A
Reset:	soft
Address:	708B0h-708B3h
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_2_A
Reset:	soft
Address:	708D0h-708D3h
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_3_A
Reset:	soft
Address:	708F0h-708F3h
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_4_A
Reset:	soft
Address:	70920h-70923h
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_5_A
Reset:	soft

Restriction
Refer to 'Plane Capability and Interoperability' page for plane capabilities and restrictions.

DWord	Bit	Description
0	31	**Selective Fetch Plane Enable** Access: Double Buffered When this bit is set, Plane is enabled for selective fetch update.

<table>
<tr><th colspan="3">SEL_FETCH_PLANE_CTL</th></tr>
<tr><td></td><td></td><td>
<table>
<tr><th>Value</th><th>Name</th></tr>
<tr><td>0b</td><td>Disable</td></tr>
<tr><td>1b</td><td>Enable</td></tr>
</table>
</td></tr>
<tr><td></td><td>30:0</td><td>Spares

<table>
<tr><td>Access:</td><td>Double Buffered</td></tr>
</table>
</td></tr>
</table>

TRANS_CLK_SEL

TRANS_CLK_SEL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	46140h-46143h
Name:	Transcoder A Clock Select
ShortName:	TRANS_CLK_SEL_A
Reset:	soft
Address:	46144h-46147h
Name:	Transcoder B Clock Select
ShortName:	TRANS_CLK_SEL_B
Reset:	soft
Address:	46148h-4614Bh
Name:	Transcoder C Clock Select
ShortName:	TRANS_CLK_SEL_C
Reset:	soft

This register maps the port clock to the transcoder.

DWord	Bit	Description
0	31:28	**Trans Clock Select** Access: R/W Select which DDI clock to use for this transcoder. **Value** / **Name** 0000b – None - Clock Disabled 0001b – DDI A 0010b – DDI B 0011b – DDI C 0100b – DDI USBC1 0101b – DDI USBC2 0110b – DDI USBC3 0111b – DDI USBC4 1000b – DDI USBC5 1001b – DDI USBC6 **Restriction** This must not be changed while the transcoder is enabled.

TRANS_CLK_SEL		
	27:0	**Reserved** Access: RO Format: MBZ

TRANS_DDI_FUNC_CTL2

TRANS_DDI_FUNC_CTL2

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6B404h-6B407h
Name:	Transcoder DSI 0 DDI Function Control2
ShortName:	TRANS_DDI_FUNC_CTL2_DSI0
Reset:	soft
Address:	6BC04h-6BC07h
Name:	Transcoder DSI 1 DDI Function Control2
ShortName:	TRANS_DDI_FUNC_CTL2_DSI1
Reset:	soft
Address:	60404h-60407h
Name:	Transcoder DDI Function Control2
ShortName:	TRANS_DDI_FUNC_CTL2_A
Reset:	soft
Address:	61404h-61407h
Name:	Transcoder DDI Function Control2
ShortName:	TRANS_DDI_FUNC_CTL2_B
Reset:	soft
Address:	62404h-62407h
Name:	Transcoder DDI Function Control2
ShortName:	TRANS_DDI_FUNC_CTL2_C
Reset:	soft
Address:	63404h-63407h
Name:	Transcoder DDI Function Control2
ShortName:	TRANS_DDI_FUNC_CTL2_D
Reset:	soft

DWord	Bit	Description
0	31	**Genlock Enable** Access: R/W 1b: Enable 0b: Disable

TRANS_DDI_FUNC_CTL2

30:29 Genlock Mode

Access:	R/W

Value	Name	Description
10b	Primary	Primary transcoder outputs frame sync for other transcoders to secondary to.
00b	Local Secondary	Local secondary transcoder secondaries to frame sync from a primary transcoder in the same device. The primary transcoder is selected by Port Sync Mode Primary Select.
01b	Remote Secondary	Remote secondary transcoder secondaries to frame sync from a primary transcoder in a different device.
11b	Reserved	

28 Reserved

Access:	RO
Format:	MBZ

27:9 Reserved

Access:	RO
Format:	MBZ

8 Double Buffer Vactive

Access:	R/W

Value	Name
0b	Normal Vactive
1b	Double Buffer Vactive

7:6 Audio Mute Override

Access:	R/W

This field overrides audio mutesignal in VBID.

Value	Name	Description
00b,01b	Do not override	
10b	Override and reset	Override audio mute bit to '0'.
11b	Override and set	Override audio mute bit to '1'.

TRANS_DDI_FUNC_CTL2

	5	**Dual Pipe Sync Enable** Access: R/W This bit informs the DSI transcoder that while it is synchronized with another DSI transcoder, it will also be driven by a separate Pipe Value / Name / Description 0b / Disabled / Both transcoders are being driven by a single Pipe (Dual Link - Single Pipe) 1b / Enabled / Each transcoder is being driven by a separate Pipe (Dual Link - Dual Pipe)
	4	**Port Sync Mode Enable** Access: R/W This field enables the DisplayPort port sync mode on this transcoder. This mode forces two or more transcoders to be in sync; with one transcoder primary and one or more transcoder secondaries. The primary is unaware that it is operating in this mode. Only the secondary is aware that it is operating in this mode. Port sync mode is only enabled in the secondary transcoder. For DSI, this bit enables DSI Transcoder 1 to be a secondary to DSI Transcoder 0. DSI Transcoder 0 is unaware that it is the primary of DSI Transcoder 1 Value / Name 0b / Disable 1b / Enable Restriction Follow the instructions for enabling and disabling Sync Mode in the Display Mode Set Sequence - Sequence for DisplayPort. Port Sync Mode Primary Select must be programmed with a valid value when Port sync Mode is enabled. The secondary and primary transcoders and associated ports must have identical parameters and properties; same color format, link width (number of lanes enabled), resolution, refresh rate, PLL configuration, dot clock, TU size, M and N programming, etc. Spread spectrum clocking cannot be used when the ports use separate PLLs. Port Sync Mode can be enabled with DisplayPort SST and with DisplayPort MST.
	3	**Reserved** Access: RO Format: MBZ

TRANS_DDI_FUNC_CTL2

	2:0	**Port Sync Mode Primary Select** Access: R/W **Description** This field indicates which transcoder will be the primary to this transcoder when in port sync mode. This field is ignored by the DSI transcoders since only DSI 0 can be the primary. This field is also used for genlock for the local secondary transcoder to select a primary transcoder. In a primary genlock system this field needs to be programmed only for secondary transcoders. In a primary genlock system this field needs to be programmed to default 0 for primary transcoder. In a secondary genlock system this field is not programmed for any transcoder. Keep it at default=0 for all transcoders. **Value** / **Name** 001b – Transcoder A 010b – Transcoder B 011b – Transcoder C **Restriction** A port cannot be secondary to itself. The DSI transcoders cannot be secondary to a non-DSI transcoder - field ignored by the DSI transcoder.

TRANS_WD_FUNC_CTL

TRANS_WD_FUNC_CTL		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	6E400h-6E403h	
Name:	Transcoder WD0 Function Control	
ShortName:	TRANS_WD_FUNC_CTL_0	
Reset:	soft	
Address:	6EC00h-6EC03h	
Name:	Transcoder WD1 Function Control	
ShortName:	TRANS_WD_FUNC_CTL_1	
Reset:	soft	

DWord	Bit	Description
0	31	**WD Function Enable** Access: R/W This bit enables the WD function. 0b: Disable 1b: Enable
	30	**Triggered Capture Mode Enable** Access: R/W This field enables the triggered capture mode where a frame is only captured after the Start Trigger Frame bit is written with 1, and hardware will ignore the transcoder frame time. This must be set before or when WD Function Enable is set. When triggered capture mode is disabled hardware will periodically capture frames following the transcoder frame time. 0b: Disable 1b: Enable
	29	**Start Trigger Frame** Access: R/W Set Write a 1 to this field to start a software triggered frame capture when Triggered Capture Mode Enable is 1. Hardware will clear the field when the frame starts.

TRANS_WD_FUNC_CTL

28	**Stop Trigger Frame** Access: R/W Set Write a 1 to this field to stop a software triggered frame capture when Triggered Capture Mode Enable is 1. Hardware will clear the field when the frame stops. This is only intended for use in case of an error where capture is never completing and software times out. It must not be set at the same time as Start Trigger Frame. After a stop trigger, VDenc will be out of sync with WD and also need to be stopped. WD and VDenc then need to start from the same frame number.
27	**Reserved** Access: R/W
26	**Chroma Filtering Enable** Access: R/W This field selects how U and V are downsampled from YUV 444 to 422. This field only applies to the YUV 422 formats.

Value	Name	Description
0	Drop	Drop U2 and V2
1	Filter **[Default]**	Use a 15-34-15 three tap filter

25:23	**Reserved** Access: RO Format: MBZ
22:20	**WD Color Mode** Access: R/W This field selects the capture color format.

Value	Name	Description
000b	YUV 4:4:4	YUV 32-bit 4:4:4 packed (8:8:8:8 MSB-Y:U:X:V)
001b	YUV 4:2:2	YUV 16-bit 4:2:2 packed (8:8:8:8 MSB- Y1:U:Y2:V) Chroma downsampling is programmable according to the Chroma Filtering field.
010b	XYUV 4:4:4	YUV 32-bit 4:4:4 packed (8:8:8:8 MSB-X:Y:U:V)
011b	RGBX	RGBX 32-bit (8:8:8:8 MSB-X:B:G:R)
100b	Y410	YUV 444 10bpc (MSB-X:V:Y:U)
101b	YUY2 8b	8 bit YUV 422 (MSB-V:Y2:U:Y1) Chroma downsampling is programmable according to the Chroma Filtering field.

110b	RGB10	RGB1010102 (MSB-X:B:G:R)

Restriction
This field must not be changed while the function is enabled.

19:18 Control Pointers

Access:	R/W

This field controls which pointers are sent and followed. If the head pointer is ignored, then the transcoder captures frames without any pointer comparison to stall the capture.

Value	Name	Description
00b	Enable Tail and Head	Send tail pointer to GT. Follow head pointer from GT.
01b	Enable Tail, Disable Head	Send tail pointer to GT. Ignore head pointer from GT. Non-cacheable.
11b	Disable Tail and Head	Do not send tail pointer to GT. Ignore head pointer from GT. Non-cacheable.

17:16 VDenc Session Select

Access:	R/W

This field selects the encode session. Each enabled WD transcoder must select a unique session. It is not valid to have multiple WD transcoders select the same session.

Value	Name
00b	0
01b	1
10b	2
11b	3

15 Reserved

Access:	RO
Format:	MBZ

14:12 WD Input Select

Access:	R/W

These bits determine the input to WD.

Value	Name
000b	Pipe A
101b	Pipe B
110b	Pipe C
Others	Reserved

TRANS_WD_FUNC_CTL		
		Restriction This field must not be changed while the function is enabled. It is not valid to have the same pipes driving multiple enabled transcoders.
	11:4	**Reserved** Access: R/W
	3:0	**Frame Number** Access: R/W SW provided frame number. This is sent in the tail pointer message to media, to be used for synchronizing the encode with the display frame.

UTIL_PIN_CTL

UTIL_PIN_CTL

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	48400h-48403h
Name:	Utility Pin Control
ShortName:	UTIL_PIN_CTL
Reset:	soft

This register controls the display utility pin. The maximum switching frequency is 100 KHz.

DWord	Bit	Description
0	31	**Util Pin Enable** Access: R/W This bit enables the utility pin. 0b: Disable 1b: Enable
	30:29	**Pipe Select** Access: R/W This bit selects which pipe will be used when the utility pin is outputting timing related signals. 00b: Pipe A 01b: Pipe B 10b: Pipe C 11b: Reserved **Restriction** The field should only be changed when the utility pin is disabled or not configured to use any timing signals.
	28	**Reserved** Access: RO Format: MBZ
	27:24	**Util Pin Mode** Access: R/W This bit configures the utility pin mode of operation for output.

UTIL_PIN_CTL

Value	Name	Description
0000b	Data	Output the Util_Pin_Output_Data value.
0001b	PWM	Output from the backlight PWM circuit.
0100b	Vblank	Output the vertical blank. [] This is the pipe delayed vblank.
0101b	Vsync	Output the vertical sync.
0110b	framestart	Output the framestart
1000b	Right/Left Eye Level	Output the stereo 3D right/left eye level signal. Asserted for the left eye and de-asserted for the right eye.
Others	Reserved	Reserved

Restriction
The field should only be changed when the utility pin is disabled.

23 **Util Pin Output Data**

Access:	R/W

This bit selects what the value to drive as an output when in the data mode.

Value	Name
0b	0
1b	1

22 **Util Pin Output Polarity**

Access:	R/W

This bit inverts the polarity of the pin output.

Value	Name
0b	Not inverted
1b	Inverted

21:20 **Reserved**

Access:	RO
Format:	MBZ

19 **Util Pin Direction**

Access:	R/W

This bit selects whether the pin is used as an output or an input.

Value	Name
0b	Output
1b	Input

UTIL_PIN_CTL		
		Restriction The field should only be changed when the utility pin is disabled.
	18:17	**Reserved** Access: RO Format: MBZ
	16	**Util Pin Input Data** Access: RO This bit gives the value received on the pin. This is only valid when the utility pin is enabled and the direction is input.
	15:0	**Reserved** Access: RO Format: MBZ

WM_LINETIME

WM_LINETIME		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	45270h-45273h	
Name:	Pipe Watermark Line Time	
ShortName:	WM_LINETIME_A	
Reset:	soft	
Address:	45274h-45277h	
Name:	Pipe Watermark Line Time	
ShortName:	WM_LINETIME_B	
Reset:	soft	
Address:	45278h-4527Bh	
Name:	Pipe Watermark Line Time	
ShortName:	WM_LINETIME_C	
Reset:	soft	

DWord	Bit	Description
0	31:9	**Reserved** Access: RO Format: MBZ
	8:0	**Line Time** Access: R/W This field specifies the line time for the current screen resolution in units of 0.125us. **Programming Notes** Line time in microseconds = Pipe horizontal total number of pixels / pixel rate in MHz. Multiply by 8 to get units of 0.125us and round to nearest integer. Program the smallest line time when using multiple refresh rates. **Restriction** The line time value must be programmed before enabling any display low power watermark. Maximum supported line time is 63.875us (111111111b).