Intel® OpenSource HD Graphics PRM

Volume 3 Part 3: PCH Display Registers [DevIBX]

For the all new 2010 Intel Core Processor Family Programmer's Reference Manual (PRM)

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1. PCH Display Registers [DevIBX]

1.1 Introduction and Register Summary

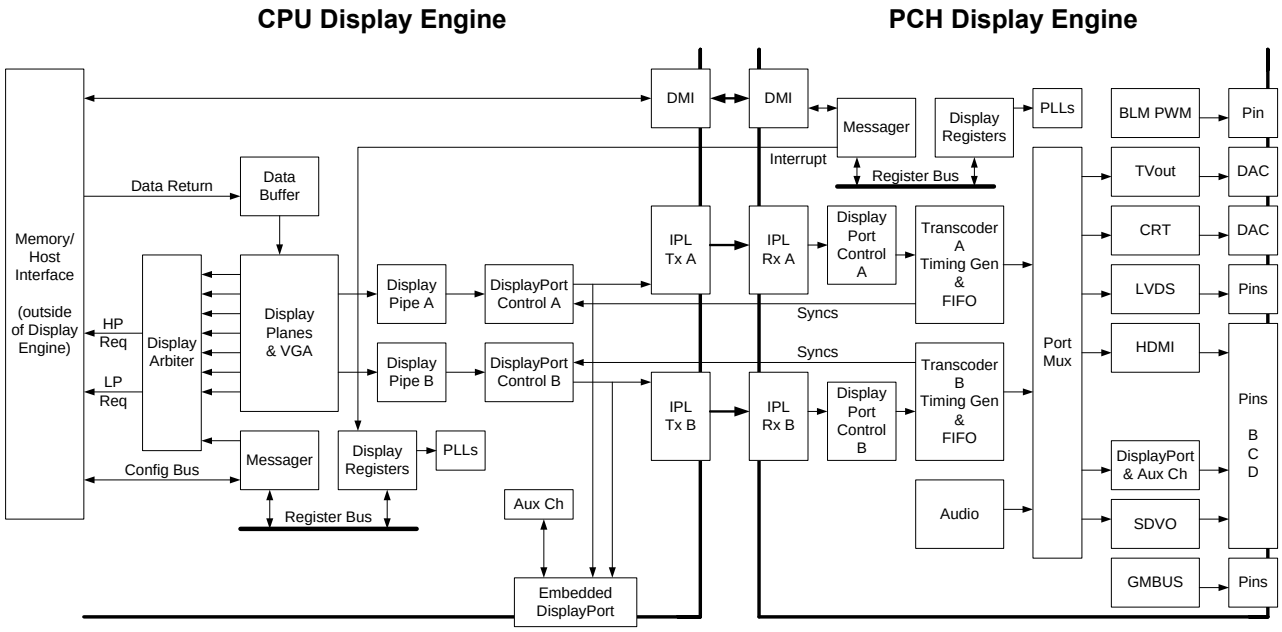
This chapter contains the register descriptions for the display portion of a family of integrated graphics devices. These registers do vary by devices within the family of devices so special attention needs to be paid to which devices use which registers and register fields.

Different devices within the family may add, modify, or delete registers or register fields relative to another device in the same family based on the supported functions of that device. Additional information on the use and programming of these registers can be found in the display chapter.

The following table contains the sections break down where the register information is contained within this chapter:

Address Range	Description
C0000h-CFFFFh	Shared Functions
D0000h-DFFFFh	Messages
E0000h–EFFFFh	Transcoder and Port Controls
F0000h–FBFFFh	Transcoder and FDI Rx Controls
FC000h–FFFFFh	AFE Registers

1.1.1 Display Diagram



The display engine plane and pipe functions are in the CPU and most of the port functions are in the PCH.

FDI transfers pixel data from the CPU Display Engine (Tx - transmit side) to the PCH Display Engine (Rx - receive side). Sync signals control the pixel flow over FDI.

A pipe in the CPU Display Engine connects to a transcoder in the PCH Display Engine through the FDI interface.

The CPU Display Engine is also called the "North Display".

The PCH Display Engine is also called the "South Display".

1.1.2 Terminol ogy

Description	Software Use	Should be implemented as
Read/Write	This bit can be read or written.	
Reserved:	Don't assume a value for these bits. Writes have no effect.	Writes are ignored. Reads return zero.
Reserved: write as zero, must be zero, or MBZ	Software must always write a zero to these bits. This allows new features to be added using these bits that will be disabled when using old software and as the default case.	Writes are ignored. Reads return zero. Maybe be connected as Read/Write in future projects.
Reserved: software must preserve contents	Software must write the original value back to this bit. This allows new features to be added using these bits.	Read only Read/Write.
Read Only	This bit is read only. The read value is determined by hardware. Writes to this bit have no effect.	According to each specific bit. The bit value is determined by hardware and not affected by register writes to the actual bit.
Read/Clear	This bit can be read and writes to it with a one cause the bit to clear.	Hardware events cause the bit to be set and the bit will be cleared on a write operation where the corresponding bit has a one for a value.
Double Buffered	Write when desired. Read gives the unbuffered value (written value) unless specified otherwise. Written values will update to take effect after a certain point. Some have a specific arming sequence where a write to another register is required before the update can take place. This is used to ensure atomic updates of several registers.	Two stages of registers used. First stage is written into and used for readback (unless specified otherwise). First stage value is transferred into second stage at the update point. Second stage value is used to control hardware. Arm/disarm flag needed for specific arming sequences.

1.1.3 Display Mode Set Sequence

See the CPU Display Registers Bspec.

1.1.4 Simultaneous Display Capabilities on a Single Display Pipe/Transcoder

Embe	dded DP (on CPU)	Inte-grated LVDS	DP CRT	
Embedded DP (CPU)		No (6)	No (6)	No (6)
Integrated LVDS			No (2, 7)	No (3, 7)
DP			No(3, 5, 7)	No (4, 7)
CRT				

Shading: Rose = Does not work, Yellow = Some cases work, Green = works

2) No internal LVDS, HDMI. DP optionally has SSC.

6) Digital ports are multiplexed on the same pins, only works if ports are different.

7) Embedded DP is on the CPU; can not share the link.

8) Dithering, range correction, and gamma are done in the CPU; the display with lower bpp can truncate or the display with higher bpp can lose bits. One of the displays dictates range and gamma.

9) No DisplayPort allowed with other port on the same pipe/transcoder.

10) No HDMI allowed with another HDMI on the same transcoder.

2. South Shared Functions (C0000h–CFFFFh)

2.1 Interrupt Control Registers

2.1.1 South Display Engine Interrupt Registers Bit Definition

South Display Engine Interrupt Control Registers Bit Definition			
Project:	All	Project:	**All**
South Display Engine (SDE) interrupt bits come from events within the south display engine. The SDEIIR is ORed together to generate the South/PCH Display Interrupt Event which will appear in the Display Engine Interrupt Control Registers. Only the rising edge of the PCH Display interrupt will cause the North Display IIR (DEIIR) PCH Display Interrupt event bit to be set, so all PCH Display Interrupts, including back to back interrupts, must be cleared in the SDEIIR before a new PCH Display Interrupt can cause the DEIIR to be set. The South Display Engine Interrupt Control Registers all share the same bit definitions from this table.			
Bit Description		Bit	Description
31:28	**Reserved** Project: All Format:		
27	**audio_Power_State_change_Port_D** Project: All Format: This is an active high pulse when there is a power state change for audio for port D.		
26	**audio_Power_State_change_Port_C** Project: All Format: This is an active high pulse when there is a power state change for audio for port C.		
25	**audio_Power_State_change_Port_B** Project: All Format: This is an active high pulse when there is a power state change for audio for port B.		
24	**Gmbus** Project: All Format: This is an active high pulse when any of the events unmasked events in GMBUS4 Interrupt Mask register occur.		
23	**Reserved** Project: All Format:		
22	**Reserved**		
21	**audio_Transcoder_B** Project: All Format: This is an active high level caused when audio protection is turned on for transcoder B.		

South Display Engine Interrupt Control Registers Bit Definition		
20	**audio_Transcoder_A** Project: All Format: This is an active high level caused when audio protection is turned on for transcoder A.	
19	**Poison** Project: All Format: This is an active high pulse on receiving the poison message.	
18	**Reserved** Project: All Format:	
17	**FDI_RXB(combined)** Project: All Format: This is an active high level while any of the FDI_RXB_IIR bits are set	
16	**FDI_RXA(combined)** Project: All Format: This is an active high level while any of the FDI_RXA_IIR bits are set	
15	**AUX_Channel_D** Project: All Format: This is an active high pulse on the AUX D done event	
14	**AUX_Channel_C** Project: All Format: This is an active high pulse on the AUX C done event	
13	**AUX_Channel_B** Project: All Format: This is an active high pulse on the AUX B done event	
12	**Reserved** Project: All Format:	
11	**CRT_Hotplug** Project: All Format: The ISR is an active high level representing the ORed together blue and green channel detection status as of the last detection cycle. The unmasked IIR is set on the rising or falling edges of the blue or green channel detection status in the Analog display port Register.	
10	**DP/HDMI/DVI_D_Hotplug** Project: All Format: The ISR is an active high level representing the Digital Port D hotplug line when the Digital Port D hotplug detect input is enabled. The unmasked IIR is set on either a short or long pulse detection status in the Digital Port Hot Plug Control Register.	
9	**DP/HDMI/DVI_C_Hotplug** Project: All Format: The ISR is an active high level representing the Digital Port C hotplug line when the Digital Port C hotplug detect input is enabled. The unmasked IIR is set on either a short or long pulse detection status in the Digital Port Hot Plug Control Register.	
8	**DP/HDMI/DVI_B_Hotplug** Project: All Format: The ISR is an active high level representing the Digital Port B hotplug line when the Digital Port B hotplug detect input is enabled. The unmasked IIR is set on either a short or long pulse detection status in the Digital Port Hot Plug Control Register.	
7	**Reserved** Project: All Format:	
6	**SDVO_B_hotplug** Project: All Format: The ISR is an active high level representing the de-glitched SDVO B hotplug line when the SDVO B hotplug interrupt detect is enabled. The unmasked IIR is set on the rising edge of the ISR.	

South Display Engine Interrupt Control Registers Bit Definition		
5	**Transcoder_B_CRC_done** Project: All Format: This is an active high pulse on the Transcoder B CRC done.	
4	**Transcoder_B_CRC_error** Project: All Format: This is an active high pulse on the Transcoder B CRC error.	
3	**Transcoder_B_FIFO_underrun** Project: All Format: **This is an active high level for the duration of the Transcoder B FIFO underrun**	
2	**Transcoder_A_CRC_done** **Project: A II Format:** **This is an active high pulse on the Transcoder A CRC done.**	
1	**Transcoder_A_CRC_error** **Project: A II Format:** **This is an active high pulse on the Transcoder A CRC error.**	
0	**Transcoder_A_FIFO_underrun** **Project: A II Format:** **This is an active high level for the duration of the Transcoder A FIFO underrun**	

2.1.1.1 SDEISR — South Display Engine Interrupt Status Register

SDEISR — South Display Engine Interrupt Status Register	
Register Type:	MMIO
Address Offset:	C4000h
Project:	All
Default Value:	00000000h
Access:	Read Only
Size (in bits):	32

The ISR register contains the non-persistent value of all interrupt status bits. The IMR register selects which of these interrupt conditions are reported in the persistent IIR (i.e., set bits must be cleared by software). Bits in the IER are used to selectively enable IIR bits to cause CPU interrupts.

Bit De	scription
31:0	**South_Display_Engine_Interrupt_Status_Bits** Project: All Format: South Display Engine Interrupt Control Registers Bit Definition See description above This field contains the non-persistent values of all interrupt status bits.

Value Na	me	Description	Project
0b	Condition Doesn't Exist	Interrupt Condition currently does not exist	All
1b	Condition Exists	Interrupt Condition currently exists	All

Programming Notes

Some inputs to this register are short pulses; therefore software should not expect to use this register to sample these conditions.

2.1.1.2 DEIMR — South Display Engine Interrupt Mask Register

SDEIMR — South Display Engine Interrupt Mask Register	
Register Type:	MMIO
Address Offset:	C4004h
Project:	All
Default Value:	FFFEDFFFh
Access:	R/W
Size (in bits):	32

The IMR register is used by software to control which Interrupt Status Register bits are “masked” or “unmasked”. “Unmasked” bits will be reported in the IIR, possibly triggering a CPU interrupt, and will persist in the IIR until cleared by software. “Masked” bits will not be reported in the IIR and therefore cannot generate CPU interrupts.

Bit De	scription
31:0	**South_Display_Engine_Interrupt_Mask_Bits** Project: All Format: South Display Engine Interrupt Control Registers Bit Definition See description above This field contains a bit mask which selects which interrupt bits from the ISR are reported in the IIR.

Value Na	me	Description	Project
0b	Not Masked	Will be reported in the IIR	All
1b	Masked	Will not be reported in the IIR	All

2.1.1.3 SDEIIR — South Display Engine Interrupt Identity Register

SDEIIR — South Display Engine Interrupt Identity Register	
Register Type:	MMIO
Address Offset:	C4008h
Project:	All
Default Value:	00000000h
Access:	R/W Clear
Size (in bits):	32

The IIR register contains the interrupt bits that are “unmasked” by the IMR and thus can generate CPU interrupts (if enabled via the IER). When a CPU interrupt is generated, this should be the first register to be interrogated to determine the source of the interrupt. **Writing a ‘1’ into the appropriate bit position within this register clears interrupts.**

Bit De	scription
31:0	**South_Display_Engine_Interrupt_Identity_Bits** Project: All Format: South Display Engine Interrupt Control Registers Bit Definition See description above This field holds the persistent values of the interrupt bits from the ISR which are “unmasked” by the IMR. If enabled by the IER, bits set in this register will generate a CPU interrupt. Bits set in this register will remain set (persist) until the interrupt condition is “cleared” via software by writing a ‘1’ to the appropriate bit(s).

Value	Name	Description	Project
0b	Condition Not Detected	Interrupt Condition Not Detected	All
1b	Condition Detected	Interrupt Condition Detected (may or may not have actually generated a CPU interrupt)	All

2.1.1.4 SDEIER — South Display Engine Interrupt Enable Register

SDEIER — South Display Engine Interrupt Enable Register			
Register Type:	MMIO		
Address Offset:	C400Ch		
Project:	All		
Default Value:	00000000h		
Access:	R/W		
Size (in bits):	32		
The IER register contains an interrupt enable bit for each interrupt bit in the IIR register. A disabled interrupt will still appear in the Interrupt Identity Register to allow polling of interrupt sources.			
Bit De	**scription**		
31:0	**South_Display_Engine_Interrupt_Enable_Bits** Project: All Format: South Display Engine Interrupt Control Registers Bit Definition See description above The bits in this register enable a CPU interrupt to be generated whenever the corresponding bit in the Interrupt Identity Register becomes set.		
	Value Na	**me**	**Description** **Project**
	0b	Disable	Disable All
	1b	Enable	Enable All

2.1.1.5 Digital Port Hot Plug Control Register

Digital Port Hot Plug Control Register	
Register Type:	MMIO
Address Offset:	C4030h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

Bit De	scription
31:21	**Reserved** Project: All Format:
20	**Digital_Port_D_Hot_Plug_Detect_Input_Enable** Project: All Default Value: 0b Controls the state of the HPD buffer for the digital port. The buffer state is independent of whether the port is enabled or not. **Value Na me** / **Description** / **Project** 0b Disable / Buffer disabled / All 1b Enable / Buffer enabled. Hot plugs bit reflect the electrical state of the HPD pin / All
19:18	**Digital_Port_D_Hot_Plug_Short_Pulse_Duration** Project: All Default Value: 0b These bits define the duration of the pulse defined as a short pulse. **Value Na me** / **Description** / **Project** 00b 2ms / 2mS / All 01b 4.5ms / 4.5mS / All 10b 6ms / 6mS / All 11b 100ms / 100mS / All

Digital Port Hot Plug Control Register

17:16 — Digital_Port_D_Hot_Plug_Interrupt_Detect_Status

Project: All

Default Value: 0b

This reflects hot plug detect status on the digital port. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. When either a long or short pulse is detected, one of these bits will set. These bits are ORed together to go to the main ISR hotplug register bit.

Value	Name	Description	Project
00b	No Detect	Digital port hot plug event not detected	All
X1b	Short Detect	Digital port short pulse hot plug event detected	All
1Xb	Long Detect	Digital port long pulse hot plug event detected	All

15:13 — Reserved Project: All Format:

12 — Digital_Port_C_Hot_Plug_Detect_Input_Enable

Project: All

Default Value: 0b

Controls the state of the HPD buffer for the digital port. The buffer state is independent of whether the port is enabled or not.

Value	Name	Description	Project
0b	Disable	Buffer disabled	All
1b	Enable	Buffer enabled. Hot plugs bit reflect the electrical state of the HPD pin	All

11:10 — Digital_Port_C_Hot_Plug_Short_Pulse_Duration

Project: All

Default Value: 0b

These bits define the duration of the pulse defined as a short pulse.

Value	Name	Description	Project
00b	2ms	2mS	All
01b	4.5ms	4.5mS	All
10b	6ms	6mS	All
11b	100ms	100mS	All

Digital Port Hot Plug Control Register

9:8 Digital_Port_C_Hot_Plug_Interrupt_Detect_Status

Project: All

Default Value: 0b

This reflects hot plug detect status on the digital port. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. When either a long or short pulse is detected, one of these bits will set. These bits are ORed together to go to the main ISR hotplug register bit.

Value	Name	Description	Project
00b	No Detect	Digital port hot plug event not detected	All
X1b	Short Detect	Digital port short pulse hot plug event detected	All
1Xb	Long Detect	Digital port long pulse hot plug event detected	All

7:5 Reserved Project: All Format:

4 Digital_Port_B_Hot_Plug_Detect_Input_Enable

Project: All

Default Value: 0b

Controls the state of the HPD buffer for the digital port. The buffer state is independent of whether the port is enabled or not.

Value	Name	Description	Project
0b	Disable	Buffer disabled	All
1b	Enable	Buffer enabled. Hot plugs bit reflect the electrical state of the HPD pin	All

3:2 Digital_Port_B_Hot_Plug_Short_Pulse_Duration

These bits define the duration of the pulse defined as a short pulse.

00 = 2mS **(Default)**

01 = 4.5mS

10 = 6mS

11 = 100mS

1:0 Digital_Port_B_Hot_Plug_Interrupt_Detect_Status

Project: All

Default Value: 0b

This reflects hot plug detect status on the digital port. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. When either a long or short pulse is detected, one of these bits will set. These bits are ORed together to go to the main ISR hotplug register bit.

Value	Name	Description	Project
00b	No Detect	Digital port hot plug event not detected	All
X1b	Short Detect	Digital port short pulse hot plug event detected	All
1Xb	Long Detect	Digital port long pulse hot plug event detected	All

2.2 GMBUS and I/O Control Registers (C5000h–C5FFFh)

2.2.1 GPIO Pin Usage (By Functions)

GPIO pins allow the support of simple query and control functions such as DDC and I^2C interface protocols. GPIO pins exist in pairs (for the most part) and provide a mechanism to control external devices through a register programming interface. GPIO pins can be set to a level or the value of the pin can be read. This allows for a "bit banging" version of an I2C interface to be implemented. An additional function of using the GMBUS engine to run the I2C protocols is also allowed. Refer to the *CSpec* for GPIO signal descriptions. Refer to the *Philips I2C-BUS SPECIFICATION version 2.1* for a description of the I2C bus and protocol.

The number and names of the GPIO pins vary from device type to device type. Some of the GPIO pins will be muxed with other functions and are only available when the other function is not being used. The following subsections describe the GPIO pin to register mapping for the various devices. OEMs have the ability to remap these functions onto other pins as long as the hardware limitations are observed.

2.2.2 GPIO Pin Usage (By Device)

Port Pin	Use (Name)	GMBUS Use	sDVO Use	Internal Pullup	I^2C Device	Description
7	Reserved	No	No	No		
	Reserved					
6	Reserved	No	No	No		
	Reserved					
5	HDMI/DPD CTLDATA	Yes	No	No – weak pulldown on reset	Yes	DDC for HDMI connection via the integrated HDMI display port D
	HDMI/DPD CTLCLK			No	Yes	
4	SDVO/HDMIB CTLDATA	Yes	Yes	No – weak pulldown on reset	Yes	Used for programming SDVO/HDMI device via GMBUS protocol. The SDVO device provides extension of this to the EEROM, DDC.
	SDVO/HDMIB CTLCLK			No	Yes	
3	HDMI/DPC CTLDATA	Yes	No	No – weak pulldown on reset	Yes	DDC for HDMI connection via the integrated HDMI display port C.

Port Pin	Use (Name)	GMBUS Use	sDVO Use	Internal Pullup	I^2C De	vice	Description
	HDMI/DPC CTLCLK			No	Yes		
2	LVDS DDC Data (DDCLDATA)	Yes	No	No	Yes	All	DDC for Digital Display connection via the integrated LVDS
	LVDS DDC Clock (DDCLCLK)				Yes		
1	I2C Data (LCLKCTRLB)	Yes	No	No	Yes	All	For control of SSC clock generator devices on motherboard. Support can be optionally i2c or control level.
	I2C Clock (LCLKCTRLA)				Yes		
0	DAC DDC Data (DDCADATA)	Yes	No	No	Yes	All	DDC for Analog monitor (VGA) connection. This cannot be shared with other DDC or I2C pairs due to legacy monitor issues.
	DAC DDC Clock (DDCACLK)				Yes		

2.2.2.1 GPIO Control Registers

The number of registers and their usage may change with each product.

GPIO Control Register Format	
Project:	All
Bit De	**scription**
31:13	**Reserved** Project: All Format: MBZ
12	**GPIO_Data_In** Project: All Access: Read Only This is the value that is sampled on the GPIO_Data pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset.
11	**GPIO_Data_Value** Project: All Access: R/W Default Value: 1b This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if **GPIO DATA MASK** is also asserted. The value will appear on the pin if this data value is actually written to this register and the **GPIO Data DIRECTION VALUE** contains a value that will configure the pin as an output. **Default = 1.** The GPIO default clock data value is programmed to '1' in hardware. The hardware drives a default of '1' since the I2C interface defaults to a '1'. (this mimics the I2C external pull-ups on the bus)
10	**GPIO_Data_Mask** Project: All Access: Write Only Default Value: 0b This is a mask bit to determine whether the **GPIO DATA VALUE** bit should be written into the register. This value is not stored and when read returns 0. **Value Na me** / **Description** / **Project** 0b — No Write — Do NOT write GPIO Data Value bit — All 1b — Write — Write GPIO Data Value bit. — All
9	**GPIO_Data_Direction_Value** Project: All Access: R/W Default Value: 0b This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if **GPIO Data DIRECTION MASK** is also asserted. The value that will appear on the pin is defined by what is in the register for the **GPIO DATA VALUE** bit. **Value Na me** / **Description** / **Project** 0b — Input — Pin is configured as an input — All 1b — Output — Pin is configured as an output — All

GPIO Control Register Format

8 — **GPIO_Data_Direction_Mask**

Project: All

Access: Write Only

Default Value: 0b

This is a mask bit to determine whether the **GPIO DIRECTION VALUE** bit should be written into the register. This value is not stored and when read always returns 0.

Value Name	Description	Project
0b No Write	Do NOT write GPIO Data Direction Value bit	All
1b Write	Write GPIO Data Direction Value bit	All

7:5 — **Reserved** Project: All Format: MBZ

4 — **GPIO_Clock_Data_In** Project: All Access: Read Only

This is the value that is sampled on the GPIO Clock pin as an input.

This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset.

3 — **GPIO_Clock_Data_Value** Project: All Access: R/W

Default Value: 1b

This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if **GPIO Clock DATA MASK** is also asserted. The value will appear on the pin if this data value is actually written to this register and the **GPIO Clock DIRECTION VALUE** contains a value that will configure the pin as an output.

Default = 1. The GPIO default clock data value is programmed to '1' in hardware. The hardware drives a default of '1' since the I2C interface defaults to a '1'. (this mimics the I2C external pull-ups on the bus)

2 — **GPIO_Clock_Data_Mask**

Project: All

Access: Write Only

Default Value: 0b

This is a mask bit to determine whether the **GPIO Clock DATA VALUE** bit should be written into the register. This value is not stored and when read always returns 0.

Value Name	Description	Project
0b No Write	Do NOT write GPIO Clock Data Value bit	All
1b Write	Write GPIO Clock Data Value bit	All

GPIO Control Register Format

1	**GPIO_Clock _Direction_Value** Project: All Access: R/W Default Value: 0b This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if **GPIO Clock DIRECTION MASK** is also asserted. The value that will appear on the pin is defined by what is in the register for the **GPIO Clock DATA VALUE** bit.

Value	Name	Description	Project
0b	Input	Pin is configured as an input and the output driver is set to tri-state	All
1b	Output	Pin is configured as an output	All

0	**GPIO_Clock_Direction_Mask** Project: All Access: Write Only Default Value: 0b This is a mask bit to determine whether the **GPIO Clock DIRECTION VALUE** bit should be written into the register. This value is not stored and when read returns 0.

Value	Name	Description	Project
0b	No Update	Do NOT update the GPIO Clock Direction Value bit on a write	All
1b	Update	Update the GPIO Clock Direction Value bit. on a write operation to this register	All

GPIO Control Registers

Register Type: MMIO
Address Offset: C5010h
Project: All
Default Value: 000U1000b
Access: R/W
Size (in bits): 6x32

These registers define the control of sets of the “general purpose” I/O pins. Each register controls a pair of pins that can be used for general purpose control, but most are designated for specific functions according to the requirements of the device and the system that the device is in. Each pin of the two pin pair is designated as a clock or data for descriptive purposes. See the table at the beginning of this section to determine for each product which pins/registers are supported and their intended functions. **Board design variations are possible and would affect the usage of these pins.**

The registers that control digital display (HDMI, displayport) pins should only be utilized if the related Digital Port detected bit in the related control register is set to 1.

DWord	Bit	Description				
0	31:0	GPIOCTL_0	Project:	All	Format:	GPIO Control Register Format
1	31:0	GPIOCTL_1	Project:	All	Format:	GPIO Control Register Format
2	31:0	GPIOCTL_2	Project:	All	Format:	GPIO Control Register Format
3	31:0	GPIOCTL_3	Project:	All	Format:	GPIO Control Register Format
4	31:0	GPIOCTL_4	Project:	All	Format:	GPIO Control Register Format
5	31:0	GPIOCTL_5	Project:	All	Format:	GPIO Control Register Format
6	31:0	GPIOCTL_6	Project:	All	Format:	GPIO Control Register Format
7	31:0	GPIOCTL_7	Project:	All	Format:	GPIO Control Register Format

2.2.3 GMBUS Controller Programming Interface

The GMBUS (Graphic Management Bus) can be used to indirectly access/control devices connected to a GMBUS bus as an alternate to bit-wise programming via software.

The GMBUS interface is I^2C compatible. The basic features are listed as follow:

1. Works as the master of a single master bus.
2. The bus clock frequency is selectable by software to be 50KHz, 100KHz, 400KHz , and 1MHz
3. The GMBUS controller can be attached to the selected GPIO pin pairs.
4. 7 or 10-Bit Slave Address and 8- or 16-bit index.
5. Hardware byte counter to track the data transmissions/reception
6. Timing source from core display clock.
7. There is a double buffered data register and a 9 bit counter to support 0 byte to 256 byte transfers.
8. The slave device can cause a stall by pulling down the clock line (Slave Stall), or delay the slave acknowledge response.
9. The master controller detects and reports time out conditions for a stall from a slave device or delayed or missing slave acknowledge.
10. Interrupt may optionally be generated.
11. There is no support for ring buffer based operation of GMBUS. The GMBUS is controlled by a set of memory mapped IO registers. Status is reported through the GMBUS status register.

The byte counter register is a read/write register, and in receiving mode, is used to track the data bytes received. There is a status register to indicate the error condition, data buffer busy, time out, and data complete acknowledgement.

2.2.3.1 GMBUS0—GMBUS Clock/Port Select

GMBUS0—GMBUS Clock/Port Select

Register Type: MMIO
Address Offset: C5100h
Project: All
Default Value: 00000000h
Access: R/W
Size (in bits): 32

The GMBUS0 register will set the clock rate of the serial bus and the device the controller is connected to. The clock rate options are 50 KHz, 100 KHz, 400 KHz, and 1MHz. This register should be set before the first data valid bit is set, because it will be read only at the very first data valid bit, and not read during the period of the transmission until stop is issued and next first data valid bit is set.

Bit De	scription
31:11	**Reserved** Project: All Format:
10:8	**GMBUS_Rate_Select** Project: All Default Value: 0b These two bits select the rate that the GMBUS will run at. It also defines the AC timing parameters used. It should only be changed when between transfers when the GMBUS is idle. **Value Na me** / **Description** / **Project** 000b 100KHz / 100 KHz / All 001b 50KHz / 50 KHz / All 010b 400KHz / 400 KHz / All 011b 1MHz / Reserved / All 1XXb RESERVED / Reserved / All
7	**Hold_Time_extension** Project: All Default Value: 0b This bit selects the hold time on the data line driven from the GMBUS. **Value Na me** / **Description** / **Project** 0b 0ns / Hold time of 0ns / All 1b 300ns / Hold time of 300ns / All
6:3	**Reserved** Project: All Format:

GMBUS0—GMBUS Clock/Port Select	
2:0	**Pin_Pair_Select** Project: All Default Value: 0b This field selects a GMBUS pin pair for use in the GMBUS communication. Use the table above to determine which pin pairs are available for a particular device and the intended function of that pin pair. Note that it is not a straight forward mapping of port numbers to pair select numbers.

Value	Name	Description	Project
000b	None	None (disabled)	All
001b	LCTRCLK	LCTRCLKA, LCTRLCLKB SSC Clock Device	All
010b	Analog Mon	Dedicated Analog Monitor DDC Pins (DDC1DATA, DDC1CLK)	All
011b	LVDS	Integrated Digital Panel DDC Pins, LVDS	All
100b	Port C	Reserved	All
101b	Port B	Reserved	All
110b	Port D	Reserved	All
111b	Reserved	Reserved	All

2.2.3.2 GMBUS1—GMBUS Command/Status

GMBUS1—GMBUS Command/Status	
Register Type:	MMIO
Address Offset:	C5104h
Project:	All
Default Value:	00000000h
Access:	R/W Protect
Size (in bits):	32

This register lets the software indicate to the GMBUS controller the slave device address, register index, and indicate when the data write is complete.
When the SW_CLR_INT bit is asserted, all writes to the GMBUS2, GMBUS3, and GMBUS4 registers are discarded. The GMBUS1 register writes to any other bit except the SW_CLR_INT are also lost. Reads to these registers always work normally regardless of the state of the SW_CLR_INT bit.

GMBUS1—GMBUS Command/Status

Bit De	scription
31	**Software_Clear_Interrupt(SW_CLR_INT)** Project: All Access: R/W Default Value: 0b This bit must be clear for normal operation. Setting the bit then clearing it acts as local reset to the GMBUS controller. This bit is commonly used by software to clear a BUS_ERROR when a slave device delivers a NACK. **Value Na me** / **Description** / **Project** 0b — Clear HW_RDY — If this bit is written as a zero when its current state is a one, will clear the **HW_RDY** bit and allows register writes to be accepted to the GMBUS registers (Write Protect Off). This bit is cleared to zero when an event causes the HW_RDY bit transition to occur. — All 1b — Assert HW_RDY — Asserted by software after servicing the GMBUS interrupt. Setting this bit causes the INT status bit to be cleared. Setting (1) this bit also asserts the **HW_RDY** bit (until this bit is written with a 0). When this bit is set, no writes to GMBUS registers will cause the contents to change with the exception of this bit which can be written. — All
30	**Software_Ready(SW_RDY)** Project: All Default Value: 0b Data handshake bit used in conjunction with **HW_RDY** bit. **Value Na me** / **Description** / **Project** 0b — De-Assert — De-asserted via the assertion event for **HW_RDY** bit — All 1b — SW Assert — When asserted by software, results in de-assertion of **HW_RDY** bit — All
29	**Enable_Timeout(ENT)** Project: All Default Value: 0b Enables timeout for slave response. When this bit is enabled and the slave device response has exceeded the timeout period, the GMBUS Slave Stall Timeout Error interrupt bit is set. **Value Na me** / **Description** / **Project** 0b — Disable — Disable timeout counter — All 1b — Enable — Enable timeout counter — All
28	**Reserved**

GMBUS1—GMBUS Command/Status

27:25 Bus_Cycle_Select

Project: All

Default Value: 0b

GMBUS cycle will always consist of a START followed by Slave Address, followed by an optional read or write data phase. A read cycle with an index will consist of a START followed by a Slave Address a WRITE indication and the INDEX and then a RESTART with a Slave Address and an optional read data phase. The GMBUS cycle will terminate either with a STOP or by entering a wait state. The WAIT state is exited by generating a STOP or by starting another GMBUS cycle.

This can only cause a STOP to be generated if a GMBUS cycle is generated, the GMBUS is currently in a data phase, or it is in a WAIT phase:

Note that the three bits can be decoded as follows:

27 = STOP generated

26 = INDEX used

25 = Cycle ends in a WAIT

Value	Name	Description	Project
000b	No cycle	No GMBUS cycle is generated	All
001b	No Index, No Stop, Wait	GMBUS cycle is generated without an INDEX, with no STOP, and ends with a WAIT	All
010b	Reserved	Reserved	All
011b	Index, No Stop, Wait	GMBUS cycle is generated with an INDEX, with no STOP, and ends with a WAIT	All
100b	Gen Stop	Generates a STOP if currently in a WAIT or after the completion of the current byte if active	All
101b	No Index, Stop	GMBUS cycle is generated without an INDEX and with a STOP	All
110b	Reserved	Reserved	All
111b	Index, Stop	GMBUS cycle is generated with an INDEX and with a STOP	All

24:16 Total_Byte_Count Project: All Format:

(9-bits) This determines the total number of bytes to be transferred during the DATA phase of a GMBUS cycle. The DATA phase can be prematurely terminated by generating a STOP while in the DATA phase (see Bus Cycle Select). Do not change the value of this field during GMBUS cycles transactions.

15:8 8-bit_GMBUS_Slave_Register_Index(INDEX) Project: All Format:

This field specifies the 8-bits of index to be used for the generated bus write transaction or the index used for the WRITE portion of the WRITE/READ pair. It only has an effect if the enable Index bit is set. Do not change this field during a GMBUS transaction.

GMBUS1—GMBUS Command/Status	
7:0	**GMBUS_Slave_Address_And_Direction** Project: All Bits 7:1 = **7-bit GMBUS Slave Address (SADDR):** When a GMBUS cycle is to be generated using the Bus Cycle Select field, this field specifies the value of the slave address that is to be sent out. For use with 10-bit slave address devices, set this value to 11110XXb (where the last two bits (xx) are the two MSBs of the 10-bit address) and the slave direction bit to a write. This is followed by the first data byte being the 8 LSBs of the 10-bit slave address. Bit 0 = **Slave Direction Bit:** When a GMBUS cycle is to be generated based on the Bus Cycle Select, this bit determines if the operation will be a read or a write. A read operation with the index enabled will perform a write with just the index followed by a re-start and a read. A 1 indicates that a Read from the slave device operation is to be performed. A 0 indicates that a Write to the slave device operation is to be performed.

Value Na	me	Description	Project
00000001b	General	General Call Address	All
00000000b	Start	Start Bye	All
0000001Xb	CBUS	CBUS Address	All
11110XXXb	10-bit	10-Bit addressing	All
Others	Reserved	Reserved	All

2.2.3.3 GMBUS2—GMBUS Status Register

GMBUS2—GMBUS Status Register	
Register Type:	MMIO
Address Offset:	C5108h
Project:	All
Default Value:	00000800h
Access:	R/W Protect
Size (in bits):	32

Bit De	scription
31:16	**Reserved** Project: All Format:

GMBUS2—GMBUS Status Register

15 — INUSE

Project: All

Default Value: 0b

Software wishing to arbitrate for the GMBUS resource can poll this bit until it reads a zero and will then own usage of the GMBUS controller. This bit has no effect on the hardware, and is only used as semaphore among various independent software threads that don't know how to synchronize their use of this resource that may need to use the GMBUS logic. Writing a one to this bit is software's indication that the software use of this resource is now terminated and it is available for other clients.

Value	Name	Description	Project
0b	GMBUS is Acquired	Read operation that contains a zero in this bit position indicates that the GMBUS engine is now acquired and the subsequent reads of this register will now have this bit set. Writing a 0 to this bit has no effect.	All
1b	GMBUS in Use	Read operation that contains a one for this bit indicates that the GMBUS is currently allocated to someone else and "In use". Once set, a write of a 1 to this bit indicates that the software has relinquished the GMBUS resource and will reset the value of this bit to a 0.	All

14 — Hardware_Wait_Phase(HW_WAIT_PHASE)

Project: All

Access: Read Only

Default Value: 0b

Once in a WAIT_PHASE, the software can now choose to generate a STOP cycle or a repeated start (RESTART) cycle followed by another GMBUS transaction on the GMBUS.

Value	Name	Description	Project
0b	No Wait	The GMBUS engine is not in a wait phase.	All
1b	Wait	Set when GMBUS engine is in wait phase. Wait phase is entered at the end of the current transaction when that transaction is selected not to terminate with a STOP.	All

13 — Slave_Stall_Timeout_Error

Project: All

Access: Read Only

Default Value: 0b

This bit indicates that a slave stall timeout has occurred. It is tied to the Enable Timeout (ENT) bit.

Value	Name	Description	Project
0b	No Slave Timeout	No slave timeout has occurred	All
1b	Slave Timeout	A slave acknowledge timeout has occurred	All

GMBUS2—GMBUS Status Register

12 **GMBUS_Interrupt_Status**

Project: All

Access: Read Only

Default Value: 0b

This bit indicates that an event that causes a GMBUS interrupt has occurred.

Value	Name	Description	Project
0b	No Interrupt	The conditions that could cause a GMBUS interrupt have not occurred or this bit has been cleared by software assertion of the **SW_CLR_INT** bit.	All
1b	Interrupt	GMBUS interrupt event occurred. This interrupt must have been one of the types enabled in the GMBUS4 register	All

11 **Hardware_Ready(HW_RDY)**

Project: All

Access: Read Only

Default Value: 1b See Description Below

This provides a method of detecting when the current software client routine can proceed with the next step in a sequence of GMBUS operations. This data handshake bit is used in conjunction with the **SW_RDY** bit. When this bit is asserted by the GMBUS controller, it results in the de-assertion of the **SW_RDY** bit.

This bit resumes to normal operation when the **SW_CLR_INT** bit is written to a 0.

Value	Name	Description	Project
0b		Condition required for assertion has not occurred or when this bit is a one and: - **SW_RDY** bit has been asserted - During a GMBUS read transaction, after the each read of the data register - During a GMBUS write transaction, after each write of the data register - **SW_CLR_INT** bit has been cleared	All
1b		This bit is asserted under the following conditions: - After a reset or when the transaction is aborted by the setting of the **SW_CLR_INT** bit - When an active GMBUS cycle has terminated with a STOP - When during a GMBUS write transaction, the data register needs and can accept another four bytes of data - During a GMBUS read transaction, this bit is asserted when the data register has four bytes of new data or the read transaction DATA phase is complete and the data register contains the last few bytes of the read data	All

GMBUS2—GMBUS Status Register

10 — NAK_Indicator

Project: All

Access: Read Only

Default Value: 0b

Value	Name	Description	Project
0b	No bus error	No bus error has been detected or **SW_CLR_INT** has been written as a zero since the last bus error	All
1b	No Ack	Set by hardware if any expected device acknowledge is not received from the slave within the timeout	All

9 — GMBUS_Active(GA)

Project: All

Access: Read Only

Default Value: 0b

This is a status bit that indicates whether the GMBUS controller is in an IDLE state or not.

Value	Name	Description	Project
0b	Idle	The GMBUS controller is currently IDLE	All
1b	Active	This indicates that the bus is in START, ADDRESS, INDEX, DATA, WAIT, or STOP Phase. Set when GMBUS hardware is not IDLE.	All

8:0 — Current_Byte_Count

Project: All

Access: Read Only

Can be used to determine the number of bytes currently transmitted/received by the GMBUS controller hardware. Set to zero at the start of a GMBUS transaction data transfer and incremented after the completion of each byte of the data phase. Note that because reads have internal storage, the byte count on a read operation may be ahead of the data that has been accepted from the data register.

2.2.3.4 GMBUS3—GMBUS Data Buffer

GMBUS3—GMBUS Data Buffer				
Register Type:	MMIO			
Address Offset:	C510Ch			
Project:	All			
Default Value:	00000000h			
Access:	R/W Protect			
Size (in bits):	32			
Double Buffer Update Point:	Start of next Vblank			
Double Buffer Armed By:	HW_RDY			
This is data read/write register. This register is double buffered. Bit 0 is the first bit sent or read, bit 7 is the 8th bit sent or read, all the way through bit 31 being the 32nd bit sent or read. For GMBUS write operations with a non-zero byte count, this register should be written with the data before the GMBUS cycle is initiated. For byte counts that are greater than four bytes, this register will be written with subsequent data only after the HW_RDY status bit is set indicating that the register is now ready for additional data. For GMBUS read operations, software should wait until the HW_RDY bit indicates that the register contains the next set of valid read data before reading this register.				
Bit De	**scription**			
31:24	**Data Byte 3**	Project:	All	Format:
23:16	**Data Byte 2**	Project:	All	Format:
15:8	**Data Byte 1**	Project:	All	Format:
7:0	**Data Byte 0**	Project:	All	Format:

2.2.3.5 GMBUS4—GMBUS Interrupt Mask

GMBUS4—GMBUS Interrupt Mask			
Register Type:	MMIO		
Address Offset:	C5110h		
Project:	All		
Default Value:	00000000h		
Access:	R/W		
Size (in bits):	32		
Bit De	**scription**		
31:5	**Reserved** Project: All Format:		
4:0	**Interrupt_Mask** Project: All Default Value: 0b This field specifies which GMBUS interrupts events may contribute to the setting of GMBUS interrupt status bit in second level interrupt status register.		

Value Na	me	Description	Project
0XXXXb	GMBUS Slave stall TO Disable	Disable GMBUS Slave stall timeout interrupt	All
1XXXXb	GMBUS Slave stall TO Enable	Enable GMBUS Slave stall timeout interrupt	All
X0XXXb	GMBUS NAK Disable	Disable GMBUS NAK interrupt	All
X1XXXb	GMBUS NAK Enable	Enable GMBUS NAK interrupt	All
XX0XXb	GMBUS Idle Disable	Disable GMBUS Idle interrupt	All
XX1XXb	GMBUS Idle Enable	Enable GMBUS Idle interrupt	All
XXX0Xb	HW Wait Disable	Disable Hardware wait (GMBUS cycle without a stop has completed) Interrupt	All
XXX1Xb	HW Wait Enable	Enable Hardware wait (GMBUS cycle without a stop has completed) Interrupt	All
XXXX0b	HW Ready Disable	Disable Hardware ready (Data has been transferred) interrupt	All
XXXX1b	HW Ready Enable	Enable Hardware ready (Data has been transferred) interrupt	

2.2.3.6 GMBUS5—2 Byte Index Register

GMBUS5—2 Byte Index Register	
Register Type:	MMIO
Address Offset:	C5120h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32
This register provides a method for the software indicate to the GMBUS controller the 2 byte device index.	
Bit De	**scription**
31	**2_Byte_Index_Enable** Project: All Format: When this bit is asserted (1), then bits 15:0 are used as the index. Bits 15:8 are used in the first byte which is the most significant index bits. The slave index in the GMBUS1<15:8> are ignored. Bits 7:0 are used in the second byte which is the least significant index bits.
30:16	**Reserved** Project: All Format:
15:0	**2_Byte_Slave_Index** Project: All Format: This is the 2 byte index used in all GMBUS accesses when bit 31 is asserted (1).

2.3 Display Clock Control Registers (C6000h–C6FFFH)

LVDS

Pixel Data Rate	Dot Clock	Dual Channel?	External Clock	Data Clock Rate	Multiplier
25-112MHz 25-1	**12MHz**	**NO 25-1**	**12MHz**	**175-784MHz**	**1x**
80-224MHz 80-2	**24MHz**	**YES**	**80-224MHz**	**280-784MHz**	**1x**

Display Modes	Display Clock Frequency Range (MHz)
CRT DAC	25-350
LVDS (Single Channel)	25-112
LVDS (Dual Channel)	80-224

The PLL frequency selection must be done such that the internal VCO frequency is within its limits. The PLL Frequency is based on the selected register and the following formula.

Reference Frequency: 120MHz for CRT and LVDS. 100MHz for the FDI.

DotClk_Frequency = (ReferenceFrequency * (5* (M1+2)+(M2+2)) / (N+2))/ (P1* P2)

Item Un	its	Range	Notes
Dot Clock	Frequency	20-350	MHz (Combining ALL modes)
VCO	Frequency	1760-3510	MHz
N – Counter	Value	3-8	
M – Counter	Value	79-127	M=5*(M1+2)+(M2+2)
M1 and M2		M1 > M2	
M1	Value	12-22	
M2	Value	5-9	
P-Div	Value	5-80	Reserved
P-Div	Value	28-112	Combined P1 and P2 for LVDS mode
P1-Div	Value	1-8	All modes

2.3.1.1 DPLLA_CTRL—DPLL A Control Register

DPLLA_CTRL—DPLL A Control Register	
Register Type:	MMIO
Address Offset:	C6014h
Project:	All
Default Value:	04800080h
Access:	R/W Protect
Size (in bits):	32
Double Buffer Update Point:	Transcoder A vertical blank, except as stated

De	scription
31	**DPLL_VCO_Enable** Project: All Access: R/W Default Value: 0b This bit will enable or disable the PLL VCO. Disabling the PLL will cause the display clock to stop. **Value Name** / **Description** / **Project** 0b Disable — DPLL is disabled in its lowest power state — All 1b Enable — DPLL is enabled and operational — All
30	**Reserved**
29:28	**Reserved** Project: All Format: MBZ
27:26	**DPLLA_Mode_Select** Project: All Default Value: 01b DPLLA in DAC /Integrated TV mode Configure the DPLLA for various supported Display Modes **Value Name** / **Description** / **Project** 00b Reserved — Reserved — All 01b Non-LVDS — DPLLA in DAC /Integrated TV mode (default) — All 10b LVDS — DPLLA in LVDS mode — All 11b Reserved — Reserved — All

DPLLA_CTRL—DPLL A Control Register

25:24 FPA0/FPA1 _P2_Clock_Divide_LVDS_Mode

Project: All

Exists If: DPLLA_CTRL: DPLLA_Mode_Select = 10b

Default Value: 00b

Value Name		Description	Project
00b	Div 14	Divide by 14. This is used in Single-Channel LVDS	All
01b	Div 7	Divide by 7. This is used in Dual-Channel LVDS	All
Others	Reserved	Reserved	All

25:24 FPA0/FPA1 _P2_Clock_Divide_NonLVDS_Mode

Project: All

Exists If: DPLLA_CTRL: DPLLA_Mode_Select != 10b

Default Value: 00b

Value Name		Description	Project
00b	Div 10	Divide by 10. This is used when Dot Clock =< 270MHz DVI, DP, or DAC modes	All
Others	Reserved	Reserved	All

23:16 FPA0_P1_Post_Divisor

Project: All

Default Value: 80h Divide by eight

Writes to this byte finalize the write of m, n and p values into the PLL when the PLL is disabled. Writing to FPA1 when FPA0 is in use (or vice versa) is also allowed. **Writes to this register take effect immediately.**

Value Name		Description	Project
00000001b	1	Divide by one	All
00000010b	2	Divide by two	All
00000100b	3	Divide by three	All
00001000b	4	Divide by four	All
00010000b	5	Divide by five	All
00100000b	6	Divide by six	All
01000000b	7	Divide by seven	All
10000000b	8	Divide by eight (default)	All
Others	Illegal	Values are illegal and should not be used	All

DPLLA_CTRL—DPLL A Control Register

15:13 **PLL_Reference_Input_Select(NOT_DOUBLE_BUFFERED)**

Project: All

Default Value: 000b

The PLL reference should be selected based on the display device that is being driven. The standard reference clock is used for CRT modes using the LCD panels for the integrated LVDS.

Value Na	me	Description	Project
000b	DREFCLK	DREFCLK (default is 120 MHz) for DAC/DVI/DP/TV	All
001b	Super SSC	120MHz super-spread clock	All
010b	Reserved	Reserved	All
011b	SSC	Spread spectrum input clock (120MHz default) for LVDS/DP	All
101b	Reserved	Reserved	All
others	Not Allowed	**Not allowed**	All

12 **Reserved** Project: All Format:

11:9 **Reserved**

8 **Reserved** Project: All Format: MBZ

7:0 **FPA1_P1_Post_Divisor**

Project: All

Default Value: 80h Divide by eight

Writes to this byte finalize the write of m, n and p values into the PLL when the PLL is disabled. Writing to FPA1 when FPA0 is in use (or vice versa) is also allowed. Writes to this register take effect immediately.

Value Na	me	Description	Project
00000001b	1	Divide by one	All
00000010b	2	Divide by two	All
00000100b	3	Divide by three	All
00001000b	4	Divide by four	All
00010000b	5	Divide by five	All
00100000b	6	Divide by six	All
01000000b	7	Divide by seven	All
10000000b	8	Divide by eight (Default)	All
Others	Illegal	Values are illegal and should not be used	All

2.3.1.2 DPLLB_CTRL—DPLL B Control Registers

DPLLB_CTRL—DPLL B Control Registers	
Register Type:	MMIO
Address Offset:	C6018h
Project:	All
Security:	None
Default Value:	04800080h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Transcoder B vertical blank, except as stated

Bit De	scription
31	**DPLLB_VCO_Enable** Project: All Default Value: 0b See DPLLA description. **Value Na me** / **Description** / **Project** 0b Disable — DPLL is disabled in it's lowest power state — All 1b Enable — DPLL is enabled and operational — All
30	**Reserved**
29:28	**Reserved** Project: All Format: MBZ
27:26	**DPLLB_Mode_Select** Project: All Default Value: 01b DPLLB in DAC/Integrated TV mode See DPLLA description **Value Na me** / **Description** / **Project** 00b Reserved — Reserved — All 01b Non-LVDS — DPLLB in DAC/DP/Integrated TV mode (default) — All 10b LVDS — DPLLB in LVDS mode — All 11b Reserved — Reserved — All

25:24

FPB0/FPB1 _P2_Clock_Divide_LVDS_Mode

Project: All

Exists If: DPLLB_CTRL: DPLLB_Mode_Select = 10b

Default Value: 00b

Value Name		Description	Project
00b	Div 14	Divide by 14. This is used in Single-Channel LVDS	All
01b	Div 7	Divide by 7. This is used in Dual-Channel LVDS	All
Others	Reserved	Reserved	All

25:24

FPB0/FPB1 _P2_Clock_Divide_NonLVDS_Mode

Project: All

Exists If: DPLLB_CTRL: DPLLB_Mode_Select != 01b

Default Value: 00b

Value	Name	Description	Project
01b	Div 10	Divide by 10. Default setting for sDVO and displayport. Also used for DAC and &BI&HDMI modes with Dot Clock <= 225MHz.	All
Others	Div 5	Divide by 5. This is used in DAC and &BI&HDMI modes with Dot Clock > 225MHz.	All
00b	Reserved	Reserved	All

23:16

FPB0_P1_Post_Divisor

Project: All

Default Value: 80h Divide by eight

See DPLLA description.

Value Name		Description	Project
00000001b	1	Divide by one	All
00000010b	2	Divide by two	All
00000100b	3	Divide by three	All
00001000b	4	Divide by four	All
00010000b	5	Divide by five	All
00100000b	6	Divide by six	All
01000000b	7	Divide by seven	All
10000000b	8	Divide by eight (Default)	All
Others	Illegal	Values are illegal and should not be used	All

DPLLB_CTRL—DPLL B Control Registers

15:13 PLL_Reference_Input_Select(NOT_DOUBLE_BUFFERED)

Project: All

Default Value: 000b

See DPLLA description.

Value	Name	Description	Project
000b	DREFCLK	DREFCLK (default is 120 MHz) for DAC/DVI/DP/TV	All
001b	Super SSC	120MHz super-spread clock	All
010b	Reserved	Reserved	All
011b	SSC	Spread spectrum input clock (120MHz default) for LVDS/DP	All
101b	Reserved	Reserved	All
others	Not Allowed	**Not allowed**	All

12 Reserved Project: All Format:

11:9 Reserved

8 Reserved Project: All Format: MBZ

7:0 FPB1_P1_Post_Divisor

Project: All

Default Value: 80h Divide by eight

See DPLLA description.

Value	Name	Description	Project
00000001b	1	Divide by one	All
00000010b	2	Divide by two	All
00000100b	3	Divide by three	All
00001000b	4	Divide by four	All
00010000b	5	Divide by five	All
00100000b	6	Divide by six	All
01000000b	7	Divide by seven	All
10000000b	8	Divide by eight (default)	All
Others	Illegal	Values are illegal and should not be used	All

2.3.1.3 FPA0—DPLL A Divisor Register 0

FPA0—DPLL A Divisor Register 0					
Register Type:	MMIO				
Address Offset:	C6040h				
Project:	All				
Default Value:	00030D07h				
Access:	R/W				
Size (in bits):	32				
Double Buffer Update Point:	Transcoder A vertical blank				

Bit De	scription
31:28	**Reserved** Project: All Format: MBZ
27	**Frequency_doubler_clock_enable** Project: All Default Value: 0b This bit enables/disables the frequency doubler clock. When the VCO clock to the doubler is disabled, the circuit does not dissipate power and its output clock is not available

Value Na	me	Description	Project
0h	Disable	Disables clock of frequency doubler	All
1h	Enable	Enables clock of frequency doubler	All

26:25	**Reserved** Project: All Format: MBZ

FPA0—DPLL A Divisor Register 0

24:22 CB_Tuning

Project: All

Default Value: 000b

These bits are used for CB tuning the Display PLL Analog core on PCH. These bits are required to improve the jitter performance and VCO headroom of the Display PLL across Process, Voltage and Temperature variations.

Display Mode	VCO Frequency	If M/N Ratio is less than	Bits <24:22>
DAC	2520.00	21.00	011
LVDS 1ch	2520.00	21.00	011
LVDS 2ch	2500.00	25.00	011

Value Name		Description	Project
000b	Off	CB Tune Off (Functional)	All
001b	Reserved	Reserved	All
010b	Reserved	Reserved	All
011b	100%	CB Tune 100% On (Functional)	All

21:16 FPA0_N-Divisor Project: All Format:

N-Divisor value calculated for the desired output frequency. The register value is programmed two less than the actual divisor.

15:14 Reserved Project: All Format: MBZ

13:8 FPA0_M1-Divisor Project: All Format:

M-Divisor value calculated for the desired output frequency. The register value is programmed to two less than the actual divisor.

7:6 Reserved Project: All Format: MBZ

5:0 FPA0_M2-Divisor Project: All Format:

M-Divisor value calculated for the desired output frequency. The register value is programmed two less than the actual divisor.

2.3.1.4 FPA1— DPLL A Divisor Register 1

FPA1—DPLL A Divisor Register 1

Register Type: MMIO
Address Offset: C6044h
Project: All
Default Value: 00030D07h
Access: R/W
Size (in bits): 32
Double Buffer Update Point: Transcoder A vertical blank

Bit De	scription
31:25	**Reserved** Project: All Format: MBZ
24:22	**CB_Tuning** Project: All Default Value: 000b See FPA0 CB_Tuning description **Value Na me** / **Description** / **Project** 000b Off / CB Tune Off (Functional) / All 001b Reserved / Reserved / All 010b Reserved / Reserved / All 011b 100% / CB Tune 100% On (Functional) / All
21:16	**FPA1_N-Divisor** Project: All Format: N-Divisor value calculated for the desired output frequency. The register value is programmed two less than the actual divisor.
15:14	**Reserved** Project: All Format: MBZ
13:8	**FPA1_M1-Divisor** Project: All Format: M-Divisor value calculated for the desired output frequency. The register value is programmed to two less than the actual divisor.
7:6	**Reserved** Project: All Format: MBZ
5:0	**FPA1_M2-Divisor** Project: All Format: M-Divisor value calculated for the desired output frequency. The register value is programmed two less than the actual divisor.

2.3.1.5 FPB0— DPLL B Divisor Register 0

FPB0—DPLL B Divisor Register 0

Register Type:	MMIO
Address Offset:	C6048h
Project:	All
Default Value:	00030D07h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Transcoder B vertical blank

Bit De	scription
31:28	**Reserved** Project: All Format: MBZ
27	**Frequency_doubler_clock_enable** Project: All Default Value: 0b This bit enables/disables the frequency doubler clock. When the VCO clock to the doubler is disabled, the circuit does not dissipate power and its output clock is not available **Value Na me** / **Description** / **Project** 0b Disable / Disables clock of frequency doubler / All 1b Enable / Enables clock of frequency doubler / All
26:25	**Reserved** Project: All Format: MBZ
24:22	**CB_Tuning** Project: All Default Value: 000b See FPA0 CB_Tuning description **Value Na me** / **Description** / **Project** 000b Off / CB Tune Off (Functional) / All 001b Reserved / Reserved / All 010b Reserved / Reserved / All 011b 100% / CB Tune 100% On (Functional) / All
21:16	**FPB0_N-Divisor** Project: All Format: See FPA description.
15:14	**Reserved** Project: All Format: MBZ
13:8	**FPB0_M1-Divisor** Project: All Format: See FPA description.
7:6	**Reserved** Project: All Format: MBZ
5:0	**FPB0_M2-Divisor** Project: All Format: See FPA description.

2.3.1.6 FPB1—DPLL B Divisor Register 1

FPB1—DPLL B Divisor Register 1	
Register Type:	MMIO
Address Offset:	C604Ch
Project:	All
Default Value:	00030D07h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Transcoder B vertical blank

Bit De	scription
31:25	**Reserved** Project: All Format: MBZ
24:22	**CB_Tuning** Project: All Default Value: 000b See FPA0 CB_Tuning description **Value Name** / **Description** / **Project** 000b Off — CB Tune Off (Functional) — All 001b Reserved — Reserved — All 010b Reserved — Reserved — All 011b 100% — CB Tune 100% On (Functional) — All
21:16	**FPB1_N-Divisor** Project: All Format: See FPA description.
15:14	**Reserved** Project: All Format: MBZ
13:8	**FPB1_M1-Divisor** Project: All Format: See FPA description.
7:6	**Reserved** Project: All Format: MBZ
5:0	**FPB1_M2-Divisor** Project: All Format: See FPA description.

2.3.1.7 DREF_CONTROL – Display Reference Clock Control Register

DREF_CONTROL – Display Reference Clock Control Register

Register Type: MMIO
Address Offset: C6200h
Project: All
Default Value: 00000000h
Access: R/W
Size (in bits): 32

Bit De	scription
31:15	**Reserved** Project: All Format: MBZ
14:13	**120MHz_CPU_source_output_enable** Project: All Default Value: 00b

Value	Name	Description	Project
00b	Disabled	Source output to CPU disabled	All
01b	Reserved	Rerserved	All
10b	Downspread	-0.5% SSC downspread source output to CPU enabled. Both the 120MHz SSC source and the SSC1 modulator must be enabled prior to enabling this output	All
11b	Non-spread	Non-spread source output to CPU enabled. The 120MHz non-SSC source must be enabled prior to enabling this output	All

Bit De	scription
12:11	**120MHz_SSC_source_enable** Project: All Default Value: 00b This bit enables the 120MHz SSC source used as a reference for CPU

Value	Name	Description	Project
00b	Disabled	Source disabled	All
01b	Reserved	Reserved for CK505 buffered source enabled	All
10b	Enabled	Integrated source enabled	All
11b	Reserved	Reserved	All

DREF_CONTROL – Display Reference Clock Control Register

10:9 **120MHz_non-spread_source_enable**

Project: All

Default Value: 00b

This field enables the 120MHz non-SSC source for display

Value	Name	Description	Project
00b	Disabled	Source disabled	All
01b	CK505	CK505 buffered source enabled. This setting enables the 96MHz	All
10b	Integrated	Integrated source enabled	All
11b	Reserved	Reserved	All

8:7 **120MHz_super-spread_source_enable**

Project: All

Default Value: 00b

This field enables the 120MHz super-SSC source for display

Value	Name	Description	Project
00b	Disabled	Source disabled	All
01b	Reserved	Reserved	All
10b	Enabled	Integrated source enabled	All
11b	Reserved	Reserved	All

6:2 **120MHz_SSC4(variable%)source_programming**

Project: All

Default Value: 00000b

This is the reference clock used for super-spread on LVDS. Please note that this reference is shared with SATA. If it is used for SATA it must not be used for LVDS

Value	Name	Description	Project
0XXXXb	Downspread	Center vs downspread: this bit sets center vs downspread on the SSC4 modulator used for superspread.	All
1XXXXb	Centerspread	Center vs downspread: this bit sets center vs downspread on the SSC4 modulator used for superspread.	All
X0001b	0%	0% SSC	All
X0010b	0.5%	0.5% SSC (center or downspread)	All
X0011b	1%	1.0% (center spread only)	All
X0100b	1.5%	1.5% (center spread only)	All
X0101b	2%	2% (center spread only)	All
X0110b	2.5%	2.5% (center spread only)	All
Others	Not Allowed	Not Allowed	All

DREF_CONTROL – Display Reference Clock Control Register

1	**120MHz_SSC1(-0.5%)modulation_enable** Project: All Default Value: 0b PLL's using this clock as an input must be enabled not more than yyuS after this bit is enabled to ensure a stable input. **Value Name** **Description** **Project** 0b Disabled SSC1 disabled All 1b Enabled SSC1 enabled All
0	**120MHz_SSC4_modulation_enable** Project: All Default Value: 0b This bit enables the variable % modulator used for the 120MHz SSC source used for LVDS. It must be set xxuS after the 120MHz SSC output is enabled. PLL's using this clock as an input must be enabled not more than yyuS after this bit is enabled to ensure a stable input. **Value Name** **Description** **Project** 0b Disabled SSC4 disabled All 1b Enabled SSC4 enabled All

2.3.1.8 RAWCLK_FREQ—Rawclk frequency

RAWCLK_FREQ—Rawclk frequency	
Register Type:	MMIO
Address Offset:	C6204h
	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

Bit De	scription
31:14	**Reserved** Project: All Format:
13:12	**FDL_TP1_Timer** Project: All This field selects the minimum time TP1 is to be sent during training of the FDL interface. **Value Na me** / **Description** / **Project** 00b 0.5us / 0.5us / All 01b 1us / 1.0us / All 10b 2us / 2.0us / All 11b 4us / 4.0us / All
11:10	**FDL_TP2_Timer** Project: All This field selects the minimum time TP2 is to be sent during training of the FDL interface. **Value Na me** / **Description** / **Project** 00b 1.5us / 1.5us / All 01b 3us / 3.0us / All 10b 6us / 6.0us / All 11b 12us / 12.0us / All
9:0	**Rawclk frequency** Project: All Format: Program this field with rawclk frequency. This is used to generate a divided down clock for miscellaneous timers in display.

2.4 Panel Power Sequencing Registers

2.4.1.1 PP_STAT US—Panel Power Status Register

PP_STATUS—Panel Power Status Register				
Register Type:	MMIO			
Address Offset:	C7200h			
Project:	All			
Default Value:	08000000h			
Access:	Read Only			
Size (in bits):	32			
Bit De	**scription**			
31	**Panel_Power_On_Status** Project: All Default Value: 0b If the LVDS port is selected as the target for the panel control, Software is responsible for enabling the LCD display by writing a “1” to the port enable bit only after all transcoder timing and DPLL registers are properly programmed and the PLL has locked to the reference signal. This bit is cleared (set to “0”) only after the panel power down sequencing is completed.			
	Value	**Name**	**Description**	**Project**
	0b	Off	Indicates that the panel power down sequencing has completed. A power cycle delay may be currently active. It is safe and allowed to program timing, port, and DPLL registers. If this bit is not a zero, it activates the register write protect and writes to those registers will be ignored unless the write protect key value is set in the panel sequencing control register.	All
	1b	On	In conjunction with bits Power Sequence Progress field and Power Cycle Delay Active, this bit set to a one indicates that the panel is currently powered up or is currently in the power down sequence and it is unsafe to change the timing, port, and DPLL registers for the pipe or transcoder that is assigned to the panel output.	All

PP_STATUS—Panel Power Status Register

30 — Require_Asset_Status

Project: All

Default Value: 0b

This bit indicates the status of programming of the display PLL and the selected port. A power on cycle will not be allowed unless this status indicates that the required assets are programmed and ready for use.

The following conditions determine that the assets are ready:

1) Display pipe or transcoder PLL enabled and frequency locked.

2) Display pipe or transcoder enabled.

3) Port attached to the panel is enabled.

Value	Name	Description	Project
0b	Not Ready	All required assets are not properly programmed	All
1b	Ready	All required assets are ready for the driving of a panel	All

29:28 — Power_Sequence_Progress

Project: All

Default Value: 0b

Value	Name	Description	Project
00b	None	Indicates that the panel is not in a power sequence	All
01b	Power Up	Indicates that the panel is in a power up sequence (may include power cycle delay)	All
10b	Power Down	Indicates that the panel is in a power down sequence	All
11b	Reserved	Reserved	All

27 — Power_Cycle_Delay_Active

Project: All

Default Value: 1b A power cycle delay (T4) is currently active

Power cycle delays occur after a panel power down sequence or after a hardware reset. On reset, a power cycle delay will occur using the default value for the timing.

Value	Name	Description	Project
0b	Not Active	A power cycle delay is not currently active	All
1b	Active	A power cycle delay (T4) is currently active	All

26:4 — Reserved Project: All Format:

3:0 — Reserved

2.4.1.2 PP_CONT ROL—Panel Power Control Register

PP_CONTROL—Panel Power Control Register	
Register Type:	MMIO
Address Offset:	C7204h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

Bit De	scription
31:16	**Reserved**
15:3	**Reserved** Project: All Format:
2	**Backlight_Enable** Project: All Default Value: 0b Software must enable this bit after training the link, and disable it when disabling the panel power state target. **Value Na me** / **Description** / **Project** 0b Disable / Backlight disabled / All 1b Enable / Backlight enabled / All
1	**Power_Down_on_Reset** Project: All Default Value: 0b Enabling this bit causes the panel to power down on reset warning. When system reset is initiated, the panel power down sequence begins automatically. If the panel is not on during a reset event, this bit is ignored. **Value Na me** / **Description** / **Project** 0b Do not Run / Do not run panel power down sequence when reset is detected / All 1b Run / Run panel power down sequence when system is reset / All

PP_CONTROL—Panel Power Control Register	
0	**Power_State_Target** Project: All Default Value: 0b Writing this bit can occur any time, it will only be used at the completion of any current power cycle.

Value	Name	Description	Project
0b	Off	The panel power state target is off, if the panel is either on or in a power on sequence, a power off sequence is started as soon as the panel reaches the power on state. This may include a power cycle delay. If the panel is currently off, there is no change of the power state or sequencing done.	All
1b	On	The panel power state target is on, if the panel is in either the off state or a power off sequence, if all pre-conditions are met, a power on sequence is started as soon as the panel reaches the power off state. This may include a power cycle delay. If the panel is currently off, there is no change of the power state or sequencing done. While the panel is on or in a power on sequence, the register write lock will be enabled.	All

2.4.1.3 PP_ON_DELAYS—Panel Power on Sequencing Delays

PP_ON_DELAYS—Panel Power on Sequencing Delays	
Register Type:	MMIO
Address Offset:	C7208h
Project:	All
Default Value:	00000000h
Access:	R/W Protect
Size (in bits):	32
Write Protect by Panel Power Sequencer	

Bit	Description
29	**Reserved** Project: All Format:
28:16	**Power_up_delay** Project: All Format: Programmable value of panel power sequencing delay during panel power up. This provides the time delay for the T1+T2 time sequence. The time unit used is the 100us timer.
15:13	**Reserved** Project: All Format:
12:0	**Power_on_to_Backlight_enable_delay** Project: All Format: Programmable value of panel power sequencing delay during panel power up. This provides the time delay for the T5 time sequence. The time unit used is the 100us timer.

2.4.1.4 PP_OFF_DELAYS—Panel Power off Sequencing Delays

PP_OFF_DELAYS—Panel Power off Sequencing Delays	
Register Type:	MMIO
Address Offset:	C720Ch
Project:	All
Default Value:	00000000h
Access:	R/W Protect
Size (in bits):	32
Write Protect by Panel Power Sequencer	
Bit De	**scription**
31:29	**Reserved** Project: All Format:
28:16	**Power_Down_delay** Project: All Format: Programmable value of panel power sequencing delay during power up. This provides the time delay for the T3 time sequence. The time unit used is the 100us timer.
15:13	**Reserved** Project: All Format:
12:0	**Power_Backlight_off_to_power_down_delay** Project: All Format: U32 Programmable value of panel power sequencing delay during power down. This provides the time delay for the Tx time sequence. The time unit used is the 100us timer.

2.4.1.5 PP_DIVISOR—Panel Power Cycle Delay and Reference Divisor

PP_DIVISOR—Panel Power Cycle Delay and Reference Divisor			
Register Type:	MMIO		
Address Offset:	C7210h		
Project:	All		
Default Value:	00186904h		
Access:	R/W Protect		
Size (in bits):	32		
Write Protect by Panel Power Sequencer This register selects the reference divisor and controls how long the panel must remain in a power off condition once powered down. This has a default value that allows a timer to initiate directly after device reset. If the panel limits how fast we may sequence from up to down to up again. Typically this is 0.5-1.5 seconds, but limited to 400ms in the SPWG specification. This register forces the panel to stay off for a programmed duration. Special care is needed around reset and D3 cold situations to conform to power cycle delay specifications.			
Bit De	**scription**		
31:8	**Reference_divider** Project: All Default Value: 001869h 125MHz raw clock. This field provides the value of the divider used for the creation of the panel timer reference clock. The output of the divider is used as the fastest of the three time bases (100us) for all other timers. The other time bases are divided from this frequency. The value of zero should not be used. When it is desired to divide by N, the actual value to be programmed is (N/2)-1. The value should be (100 * Ref clock frequency in MHz / 2) - 1. The default value is for the 125MHz raw clock. **Example:** **Reference Clock Frequency** **Value of Field** 233MHz 2D81h 200MHz 270Fh 125MHz 1869h		
7:5	**Reserved** Project: All		Format:

PP_DIVISOR—Panel Power Cycle Delay and Reference Divisor	
4:0	**Power_Cycle_Delay** Project: All Format: Programmable value of time panel must remain in a powered down state after powering down. For devices coming out of reset, the default values will define how much time must pass before a power on sequence can be started. This field uses the 0.1 S time base unit from the divider. If the panel power on sequence is attempted during this delay, the power on sequence will commence once the power cycle delay is complete. Writing a value of 0 selects no delay or is used to abort the delay if it is active. During the initial power up reset, a D3 cold power cycle, or a user instigated system reset, the timer will be set to the default value and the count down will begin after the de-assertion of reset. Writing this field to a zero while the count is active will abort this portion of the sequence. This corresponds to the T4 of the SPWG specification. Note: Even if the panel is not enabled, the T4 count happens after reset. This register needs to be programmed to a "+1" value. For instance for meeting the SPWG specification of 400mS, program 5 to achieve at least 400mS delay prior to powerup.

2.5 Backlight Control Registers

2.5.1.1 Backlight PWM PCH Control Register

Backlight PWM PCH Control Register			
Register Type: MMIO **Address Offset:** C8250h **Project:** All **Default Value:** 00000000h **Access:** R/W **Size (in bits):** 32			
Bit De	**scription**		
31	**PWM_PCH_Enable** Project: All Default Value: 0b This bit enables the PWM counter logic in the PCH.		
	Value Na **me**	**Description**	**Project**
	0b Disable	PCH PWM disabled (drives 0 always)	All
	1b Enable	PCH PWM enabled	All
30	**Reserved**		

Backlight PWM PCH Control Register	
29	**Backlight_Polarity** Project: All Default Value: 0b This field controls the polarity of the PWM signal. **Value Name** **Description** **Project** 0b High Active High All 1b Low Active Low All
28:0	**Reserved** Project: All Format:

2.5.1.2 Backlight PWM PCH Control Register

Backlight PWM PCH Control Register	
Register Type:	MMIO
Address Offset:	C8254h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

Bit De	scription
31:16	**Backlight_Modulation_Frequency** Project: All Format: This field determines the number of time base events in total for a complete cycle of modulated backlight control. This field is normally set once during initialization based on the frequency of the clock that is being used and the desired PWM frequency. This value represents the period of the PWM stream in PCH display raw clocks multiplied by 128.
15:0	**Reserved** Project: All

3. South Transcoder and Port Controls (E0000h–EFFFFh)

3.1 Transcoder A Timing

3.1.1.1 TRANS_HTOTAL_A—Transco der A Horizontal Total Register

TRANS_HTOTAL_A—Transcoder A Horizontal Total Register	
Register Type:	MMIO
Address Offset:	E0000h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

Bit De	scription
31:29	**Reserved** Project: All Format: MBZ
28:16	**Transcoder_A_Horizontal_Total_Display_Clocks** Project: All Default Value: 0b This 13-bit field provides Horizontal Total up to 8192 pixels encompassing the Horizontal Active Display period, front/back border and retrace period. This field is programmed to the number of clocks desired minus one. This number of clocks needs to be a multiple of two when driving the LVDS port in two channel mode. This value should always be equal or greater to the sum of the horizontal active and the horizontal blank, and border region sizes.
15:12	**Reserved** Project: All Format: MBZ
11:0	**Transcoder_A_Horizontal_Active_Display_Pixels** Project: All Default Value: 0b This 12-bit field provides Horizontal Active Display resolutions up to 4096 pixels. Note that the first horizontal active display pixel is considered pixel number 0. The value programmed should be the (active pixels/line – 1). The number of active pixels will be limited to multiples of two pixels when driving the LVDS port in two channel mode. The minimum horizontal active display size allowed will be 64 pixels.

3.1.1.2 TRANS_HBLANK_A—Transco der A Horizontal Blank Register

TRANS_HBLANK_A—Transcoder A Horizontal Blank Register	
Register Type:	MMIO
Address Offset:	E0004h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

Bit De	scription
31:29	**Reserved** Project: All Format: MBZ
28:16	**Transcoder_A_Horizontal_Blank_End** Project: All Default Value: 0b This 13-bit field specifies the position of Horizontal Blank End expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HBLANK End pixel position, where the first active pixel is considered position 0; the second active pixel is considered position 1, etc. Horizontal blank ending at the same point as the horizontal total indicates that there is no left hand border area. HBLANK size has a minimum value of 32 clocks. The number of clocks within blank needs to be a multiple of two when driving the LVDS port in two channel mode. The value loaded in the register would be equal to RightBorder+Active+HBlank-1. If this transcoder is connected to the TVout port the border must be zero. In that case this register is programmed to the same value as the HTOTAL register.
15:13	**Reserved** Project: All Format: MBZ
12:0	**Transcoder_A_Horizontal_Blank_Start** Project: All Default Value: 0b This 13-bit field specifies the Horizontal Blank Start position expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HBLANK Start pixel position, where the first active pixel is considered position 0; the second active pixel is considered position 1, etc. The number of clocks for both left and right borders need to be a multiple of two when driving the LVDS port in two channel mode. Horizontal blank should only start after the end of the horizontal active region. The value loaded in the register would be equal to RightBorder+Active-1. If this transcoder is connected to the TVout port the border must be zero. In that case this register is programmed to the same value as the HACTIVE register.

3.1.1.3 TRANS_HSYNC_A— Transcoder A Horizontal Sync Register

TRANS_HSYNC_A—Transcoder A Horizontal Sync Register	
Register Type:	MMIO
Address Offset:	E0008h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

Bit De	scription
31:29	**Reserved** Project: All Format: MBZ
28:16	**Transcoder_A_Horizontal_Sync_End** Project: All Default Value: 0b This 13-bit field specifies the horizontal Sync End position expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HSYNC End pixel position, where the first active pixel is considered position 0; the second active pixel is considered position 1, etc. The number of clocks in the sync period needs to be a multiple of two when driving the LVDS port in two channel mode. This value should be greater than the horizontal sync start position and would be loaded with the Active+RightBorder+FrontPorch+Sync-1.
15:13	**Reserved** Project: All Format: MBZ
12:0	**Transcoder_A_Horizontal_Sync_Start** Project: All Default Value: 0b This 13-bit field specifies the horizontal Sync Start position expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HSYNC Start pixel position, where the first active pixel is considered position 0; the second active pixel is considered position 1, etc. Note that when HSYNC Start is programmed equal to HBLANK Start, both HSYNC and HBLANK will be asserted on the same pixel clock. It should never be programmed to less than HBLANK start. The number of cycles from the beginning of the line needs to be a multiple of two when driving the LVDS port in two channel mode. This register should not be less than the horizontal active end. This register should be loaded with the Active+RightBorder+FrontPorch-1.

3.1.1.4 TRANS_VTOTAL_A—Transco der A Vertical Total Register

TRANS_VTOTAL_A—Transcoder A Vertical Total Register	
Register Type:	MMIO
Address Offset:	E000Ch
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

Bit De	scription
31:29	**Reserved** Project: All Format: MBZ
28:16	**Transcoder_A_Vertical_Total_Display_Clocks** Project: All Default Value: 0b This 13 bit field provides Vertical Total up to 8192 lines encompassing the Vertical Active Display Lines, top/bottom border and retrace period. The value programmed should be the number of lines required minus one. Vertical total needs to be large enough to be greater than the sum of the vertical active, vertical border, and the vertical blank regions. The vertical counter is incremented on the leading edge of the horizontal sync. For interlaced display modes, this indicates the total number of lines in both fields. In interlaced modes, hardware automatically divides this number by 2 to get the number of lines in each field.
15:12	**Reserved** Project: All Format: MBZ
11:0	**Transcoder_A_Vertical_Active_Display_Pixels** Project: All Default Value: 0b This 12-bit field provides vertical active display resolutions up to 4096 lines. It should be programmed with the desired number of lines minus one. When using the internal panel fitting logic, the minimum vertical active area must be seven lines. For interlaced display modes, this indicates the total number of lines in both fields. In interlaced modes, hardware automatically divides this number by 2 to get the number of lines in each field.

3.1.1.5 TRANS_VBLANK_A—Transco der A Vertical Blank Register

TRANS_VBLANK_A—Transcoder A Vertical Blank Register	
Register Type:	MMIO
Address Offset:	E0010h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

Bit De	scription
31:29	**Reserved** Project: All Format: MBZ
28:16	**Transcoder_A_Vertical_Blank_End** Project: All Default Value: 0b This 13-bit field specifies the Vertical Blank End position expressed in terms of the absolute Line number relative to the vertical active display start. The value programmed should be the VBLANK End line position, where the first active line is considered line 0, the second active line is considered line 1, etc. The end of vertical blank should be after the start of vertical blank and before or equal to the vertical total. This register should be loaded with the Vactive+BottomBorder+VBlank-1. For interlaced display modes, hardware automatically divides this number by 2 to get the vertical blank end in each field. It does not count the two half lines that get added when operating in modes with half lines. If this transcoder is connected to the TVout port the border must be zero. In that case this register is programmed to the same value as the VTOTAL register.
15:13	**Reserved** Project: All Format: MBZ
12:0	**Transcoder_A_Vertical_Blank_Start** Project: All Default Value: 0b This 13-bit field specifies the Vertical Blank Start expressed in terms of the absolute line number relative to the vertical active display start. The value programmed should be the VBLANK Start line position, where the first active line is considered line 0, the second active line is considered line 1, etc. Minimum vertical blank size is required to be at least three lines. Blank should start after the end of active. This register is loaded with the Vactive+BottomBorder-1. For interlaced display modes, hardware automatically divides this number by 2 to get the vertical blank start in each field. It does not count the two half lines that get added when operating in modes with half lines. If this transcoder is connected to the TVout port the border must be zero. In that case this register is programmed to the same value as the VACTIVE register.

3.1.1.6 TRANS_VSYNC_ A—Transcoder A Vertical Sync Register

TRANS_VSYNC_A—Transcoder A Vertical Sync Register	
Register Type:	MMIO
Address Offset:	E0014h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

Bit De	scription
31:29	**Reserved** Project: All Format: MBZ
28:16	**Transcoder_A_Vertical_Sync_End** Project: All Default Value: 0b This 13-bit field specifies the Vertical Sync End position expressed in terms of the absolute Line number relative to the vertical active display start. The value programmed should be the VSYNC End line position, where the first active line is considered line 0, the second active line is considered line 1, etc. This register should be loaded with Vactive+BottomBorder+FrontPorch+Sync-1. For interlaced display modes, hardware automatically divides this number by 2 to get the vertical sync end in each field. It does not count the two half lines that get added when operating in modes with half lines.
15:13	**Reserved** Project: All Format: MBZ
12:0	**Transcoder_A_Vertical_Sync_Start** Project: All Default Value: 0b This 13-bit field specifies the Vertical Sync Start position expressed in terms of the absolute line number relative to the vertical active display start. The value programmed should be the VSYNC Start line position, where the first active line is considered line 0, the second active line is considered line 1, etc. This register would be loaded with Vactive+BottomBorder+FrontPorch-1. For interlaced display modes, hardware automatically divides this number by 2 to get the vertical sync start in each field. It does not count the two half lines that get added when operating in modes with half lines.

3.1.1.7 TRANS_BCLRPAT_A— Transcoder A Border Color Pattern Register

TRANS_BCLRPAT_A— Transcoder A Border Color Pattern Register					
Register Type: MMIO **Address Offset:** E0020h **Project:** All **Default Value:** 00000000h **Access:** R/W **Size (in bits):** 32					
This register value determines what color should be sent to the display in the border region, the space between the end of active and the beginning of blank and the end of blank and the beginning of active. The border is programmed with 8 bits per color, which will be padded or dropped as needed if the transcoder is other than 8 bits per color.					
Bit De	**scription**				
31:24	**Reserved**	Project:	All	Format:	
23:16	**Border_Red_Channel_Value**	Project:	All	Format:	
15:8	**Border_Green_Channel_Value**	Project:	All	Format:	
7:0	**Border_Blue_Channel_Value**	Project:	All	Format:	

3.1.1.8 TRANS_VSYNCSHIF T_A— Transcoder A Vertical Sync Shift Register

TRANS_VSYNCSHIFT_A— Transcoder A Vertical Sync Shift Register	
Register Type:	MMIO
Address Offset:	E0028h
Project:	All
Default Value:	00000000h
Access:	R/W Project
Size (in bits):	32
Write Protect by Panel Power Sequencer when panel is connected to transcoder A.	

Bit De	scription
31:13	**Reserved** Project: All Format: MBZ
120	**Transcoder_A_Second_Field_Vertical_Sync_Shift** Project: All This value specifies the vertical sync alignment for the start of the interlaced second field expressed in terms of the absolute pixel number relative to the horizontal active display start. This value will only be used if the transcoder is in an interlaced mode. Typically, the interlaced second field vertical sync should start one pixel after the point halfway between successive horizontal syncs, so the value of this register should be programmed to: (horizontal sync start - floor[horizontal total / 2]). (For calculation, use the actual horizontal sync start and horizontal total values and not the minus one values programmed into the registers) This vertical sync shift only occurs during the interlaced second field. In all other cases the vertical sync start position is aligned with horizontal sync start.

3.2 Transcoder A M/N Values

Calculation of TU, Data M, and Data N is as follows:
For modes that divide into the link frequency evenly,
Active/TU = Payload/Capacity = Data M/N = dot clock * bytes per pixel / ls_clk * number of lanes
Default value to program TU size is "111111" for TU size of 64

Calculation of Link M and Link N is as follows:
Link M/N = dot clock / ls_clk

When switching between two refresh rates, both the M1/N1 data and link values and the M2/N2 link values must be programmed. For dynamic refresh rate control, M1/N1 values are used for higher power, and M2/N2 values are used for lower power. Selection of M1/N1 or M2/N2 is indicated via MSA from the CPU display.

3.2.1.1 TransADataM1— Transcoder A Data M value 1

TransADataM1— Transcoder A Data M value 1	
Register Type:	MMIO
Address Offset:	E0030h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of Vblank
Double Buffer Armed By:	Writing the TransADPLinkN1

Bit De	scription
31	**Reserved** Project: All Format: MBZ
30:25	**TU1_Size** Project: All This field is the size of the transfer unit for DP, minus one.
24	**Reserved** Project: All Format: MBZ
23:0	**Transcoder_A_Data_M1_value** Project: All This field is the M1 value for internal use of the DDA.

3.2.1.2 TransADataN1— Transcoder A Data N value 1

TransADataN1— Transcoder A Data N value 1	
Register Type:	MMIO
Address Offset:	E0034h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of Vblank
Double Buffer Armed By:	Writing the TransADPLinkN1

Bit De	scription
31:24	**Reserved** Project: All Format: MBZ
23:0	**Transcoder_A_Data_N1_value** Project: All This field is the N1 value for internal use of the DDA.

3.2.1.3 TransADataM2— Transcoder A Data M value 2

TransADataM2— Transcoder A Data M value 2	
Register Type:	MMIO
Address Offset:	E0038h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of Vblank
Double Buffer Armed By:	Writing the TransADPLinkN2

Bit De	scription
31	**Reserved** Project: All Format: MBZ
30:25	**TU2_Size** Project: All This field is the size of the transfer unit for DP, minus one.
24	**Reserved** Project: All Format: MBZ
23:0	**Transcoder_A_Data_M2_value** Project: All This field is the M2 value for internal use of the DDA.

3.2.1.4 TransADataN2— Transcoder A Data N value 2

TransADataN2— Transcoder A Data N value 2	
Register Type:	MMIO
Address Offset:	E003Ch
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of Vblank
Double Buffer Armed By:	Writing the TransADPLinkN2

Bit De	scription
31:24	**Reserved** Project: All Format: MBZ
23:0	**Transcoder_A_Data_N2_value** Project: All This field is the N2 value for internal use of the DDA.

3.2.1.5 TransADPLinkM1— Transcoder A Link M value 1

TransADPLinkM1— Transcoder A Link M value 1	
Register Type:	MMIO
Address Offset:	E0040h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of Vblank
Double Buffer Armed By:	Writing the TransADPLinkN1

Bit De	scription
31:24	**Reserved** Project: All Format: MBZ
23:0	**Transcoder_A_Link_M1_value** Project: All This field is the M1 value for external transmission in the Main Stream Attributes.

3.2.1.6 TransADPLinkN1— Transcoder A Link N value 1

TransADPLinkN1— Transcoder A Link N value 1	
Register Type:	MMIO
Address Offset:	E0044h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of Vblank
Double Buffer Armed By:	Writing the TransADPLinkN1

Bit De	scription
31:24	**Reserved** Project: All Format: MBZ
23:0	**Transcoder_A_Link_N1_value** Project: All This field is the N1 value for external transmission in the Main Stream Attributes and VB-ID.

3.2.1.7 TransADPLinkM2— Transcoder A Link M value 2

TransADPLinkM2— Transcoder A Link M value 2	
Register Type:	MMIO
Address Offset:	E0048
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of Vblank
Double Buffer Armed By:	Writing the TransADPLinkN2

Bit De	scription
31:24	**Reserved** Project: All Format: MBZ
23:0	**Transcoder_A_Link_M2_value** Project: All This field is the M2 value for external transmission in the Main Stream Attributes.

3.2.1.8 TransADPLinkN2— Transcoder A Link N value 2

TransADPLinkN2— Transcoder A Link N value 2	
Register Type:	MMIO
Address Offset:	E004Ch
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of Vblank
Double Buffer Armed By:	Writing the TransADPLinkN2

Bit De	scription
31:24	**Reserved** Project: All Format: MBZ
23:0	**Transcoder_A_Link_N2_value** Project: All This field is the N2 value for external transmission in the Main Stream Attributes and VB-ID.

3.3 Transcoder A Video DIP

3.3.1.1 VIDEO_DI P_CTL_A—Video DIP Control for Transcoder A

VIDEO_DIP_CTL_A—Video DIP Control for Transcoder A	
Register Type:	MMIO
Address Offset:	E0200h
Project:	All
Default Value:	20000000h
Access:	R/W
Size (in bits):	32
Please note that writes to this register take effect immediately. Therefore, it is critical for software to follow the write and read sequences as described in the bit 31 text.	

VIDEO_DIP_CTL_A—Video DIP Control for Transcoder A

Bit De	scription
31	**Enable_Graphics_Data_Island_Packet** Project: All Default Value: 0b Data Island Packet (DIP) is a mechanism that allows up to 36 bytes to be sent over digital port during VBLANK. This includes header, payload, checksum and ECC information. Each type of DIP can be sent once per vsync, once every other vsync, or once. This data can be transmitted on either transcoder, through any digital port (digital port B, C or D), but not two simultaneously on one transcoder. Please note that the audio subsystem is also capable of sending Data Island Packets. These packets are programmed by the audio driver and can be read by in MMIO space via the audio control state register, address E20B4h. Write sequence: 1) Wait for 1 VSync to ensure completion of any pending DIP transmissions. 2) Disable the DIP type (bits 24:21) and set the DIP buffer index (bits 20:19) for the DIP being written. 3) Set the DIP access address (bits 3:0) to 0, or to the desired DWORD to be written. 4) Write DIP data 1 DWORD at a time. The IF access address autoincrements with each DWORD write, wrapping around to address 0 when the max buffer address size of 0xF has been reached. Please note that software must write an entire DWORD at a time. 5) Enable the DIP type and transmission frequency. Reading sequence: 1) Set the DIP buffer index (bits 20:19) for the DIP being read. 2) Set the DIP access address to 0, or to the desired DWORD to be read. Read DIP data 1 DWORD at a time. The DIP access address autoincrements with each DWORD read, wrapping around to address 0 when the max buffer address size of 0xF has been reached. **Value Na me** — **Description** — **Project** 0b — Disable — Video DIP is disabled — All 1b — Enable — Video DIP is enabled — All **Programming Notes** + Partial DIPs are never sent out while the port is enabled. Disabling the DIP at the same time it is being transferred will result in the DIP being completed before the function is disabled. + Shutting off the port on which DIP is being transmitted will result in partial transfer of DIP data. There is no need to switch off the DIP enable bit if the port transmitting DIP is disabled. + When disabling both the DIP port and DIP transmission, first disable the port and then disable DIP. + Enabling a DIP function at the same time that the DIP would have been sent out (had it already been enabled) will result in the DIP being sent on the following frame. + Enabling should only be done after the buffer contents have been written.

VIDEO_DIP_CTL_A—Video DIP Control for Transcoder A

30:29 **Port_Select**

Project: All

Default Value: 01b Digital Port B

This selects which port is to transmit the data island. This field must not be changed while data island transmission is enabled.

Value Name		Description	Project
00b	Reserved	Reserved	All
01b	Digital Port B	Digital Port B (Default)	All
10b	Digital Port C	Digital Port C	All
11b	Digital Port D	Digital Port D	All

28:26 **Reserved** Project: All Format:

25 **GCP_DIP_enable**

Project: All

Default Value: 0b

This bit enables the output of the General Control Packet. GCP is different from other DIPs in that much of the payload is automatically reflected in the packet, and therefore a DIP buffer for GCP is not needed. Please refer to the GCP payload register for payload details. Writes to this bit take effect immediately.

This bit shoud not be enabled for 8bpc mode if at least one of the other HDMI ports is enabled in 12bpc mode.

Value Name		Description	Project
0b	Disable	GCP DIP disabled	All
1b	Enable	GCP DIP enabled	All

24:21 **Data_Island_Packet_type_enable**

Project: All

Default Value: 0001b Enable AVI DIP

These bits enable the output of a given data island packet (DIP) type. It can be updated while the port is enabled and is immediately updated (not double-buffered). Within 2 vblank periods, the DIP is guaranteed to have been transmitted.

Value Name		Description	Project
XXX1b	Enable AVI	Enable AVI DIP **(Default = enabled)**	All
XX1Xb	Enable Vendor	Enable Vendor-specific DIP **(Default = disabled)**	All
X1XXb	Enable Gamut	Enable Gamut Metadata Packet **(Default = disabled)**	All
1XXXb	Enable Source	Enable Source Product Description DIP **(Default = disabled)**	All

VIDEO_DIP_CTL_A—Video DIP Control for Transcoder A

20:19 DIP_buffer_index

Project: All

Default Value: 00b

This field is used during programming of different DIPs. These bits are used as an index to their respective DIP buffers. The transmission frequency must also be written when programming the buffer.

Value Na	me	Description	Project
00b	AVI	AVI DIP (31 bytes of space available)	All
01b	Vendor-specific	Vendor-specific DIP	All
10b	Gamut Metadata	Gamut Metadata Packet	All
11b	Source Product	Source Product Description DIP	All

18 Reserved Project: All Format:

17:16 Video_DIP_transmission_frequency

Project: All

Default Value: 00b

These bits dictate the frequency of Video DIP transmission for the DIP buffer index designated in bits 20:19. When writing Video DIP data, this value is also latched when the first DW of the Video DIP is written.

When read, this value reflects the Video DIP transmission frequency for the Video DIP buffer designated in bits 20:19.

Value Na	me	Description	Project
00b	Send Once	Send Once	All
01b	Every VSync	Send Every VSync (Default for AVI)	All
10b	Every Other Vsync	Send at least every other VSync	All
11b	Reserved	Reserved	All

15:12 Reserved Project: All Format: MBZ

11:8 Video_DIP_buffer_size

Project: All

Access: Read Only

Default Value: 0000b

This reflects the buffer size in dwords available for the type of Video DIP being indexed by bits 20:19 of this register, including the header. It is hardwired to the maximum size of a Video DIP, 36 bytes. Please note that this count includes ECC bytes, which are not writable by software. These bits are immediately valid after write of the DIP index.

7:4 Reserved Project: All Format: MBZ

VIDEO_DIP_CTL_A—Video DIP Control for Transcoder A	
3:0	**Video_DIP_RAM_access_address** Project: All Selects the DWORD address for access to the Video DIP buffers. This value is automatically incremented after each read or write of the Video DIP Data Register. The value wraps back to zero when it autoincrements past the max address value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.

3.3.1.2 VIDEO_DI P_DATA_A–Video Data Island Packet Data for Transcoder A

VIDEO_DIP_DATA_A–Video Data Island Packet Data for Transcoder A	
Register Type:	MMIO
Address Offset:	E0208h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32
Bit De	**scription**
31:0	**Video_DIP_DATA** Project: All When read, this returns the current value at the location specified in the Video DIP buffer index select and Video DIP RAM access address fields. The index used to address the RAM is incremented after each read or write of this register. DIP data can be read at any time. Data should be loaded into the RAM before enabling the transmission through the DIP type enable bit. Accesses to this register are on a per-DWORD basis.

Construction of DIP write:

MSB LSB

DW0	ECC for header (read only, calculated by HW)	Header byte 2	Header byte 1	Header byte 0
DW1	Data byte 3	Data byte 2	Data byte 1: start of payload	Data byte 0: Checksum for payload
…				
DW8 (read only, calculated by HW)	ECC		ECC for data bytes 7-13	ECC for data bytes 0-6

3.3.1.3 VIDEO_DIP_GDCP_PAYLOAD_A–Video Data Island Payload for Transcoder A

VIDEO_DIP_GDCP_PAYLOAD_A–Video Data Island Payload for Transcoder A	
Register Type:	MMIO
Address Offset:	E0210h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

Bit De	scription
31:3	**Reserved** Project: All Format: MBZ
2	**Reserved_for_GCP_color_indication** Project: All Default Value: 0b This bit must be set when in deep color mode. It may optionally be set for 24-bit mode. It must be set if the sink attached to Transcoder A can receive GCP data. **Value Name / Description / Project** 0b – Don't Indicate – Don't indicate color depth. CD and PP bits in GCP set to zero – All 1b – Indicate – Indicate color depth using CD bits in GCP. It will be set depending on programmed pixel depth in port control register – All

VIDEO_DIP_GDCP_PAYLOAD_A–Video Data Island Payload for Transcoder A

1 — **GCP_default_phase_enable**

Project: All

Default Value: 0b

Indicates the video timings meet alignment requirements such that the following conditions are met:

1) Htotal is an even number

2) Hactive is an even number

3) Hsync is an even number

4) Front and back porches for Hsync are even numbers

5) Vsync always starts on an even-numbered pixel within a line in interlaced modes (starting counting with 0)

Value	Name	Description	Project
0b	Clear	Default phase bit in GCP is cleared	All
1b	Require Met	Default phase bit in GCP is set. All requirements must be met before setting this bit	All

0 — **GCP_AV_mute**

Project: All

Default Value: 0b

Set AV mute bit in GCP

Value	Name	Description	Project
0b	Clear	AV mute bit in GCP is cleared. When this bit transitions to 0, the AV mute clear flag is sent in the next GCP packet	All
1b	Set	AV mute bit in GCP is set. When this bit transitions to 1, the AV mute set flag is sent in the next GCP packet	All

3.4 Transcoder B Timing

3.4.1.1 TRANS_HTOTAL_B—Transco der B Horizontal Total Register

TRANS_HTOTAL_B—Transcoder B Horizontal Total Register	
Register Type:	MMIO
Address Offset:	E1000h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

Bit De	scription
31:29	**Reserved** Project: All Format: MBZ
28:16	**Transcoder_B_Horizontal_Total_Display_Clocks** Project: All See Transcoder A description.
15:12	**Reserved** Project: All Format: MBZ
11:0	**Transcoder_B_Horizontal_Active_Display_Pixels** Project: All See Transcoder A description.

3.4.1.2 TRANS_HBLANK_B—Transco der B Horizontal Blank Register

TRANS_HBLANK_B—Transcoder B Horizontal Blank Register	
Register Type:	MMIO
Address Offset:	E1004h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

Bit De	scription
31:29	**Reserved** Project: All Format: MBZ
28:16	**Transcoder_B_Horizontal_Blank_End** Project: All See Transcoder A description.
15:13	**Reserved** Project: All Format: MBZ
12:0	**Transcoder_B_Horizontal_Blank_Start** Project: All See Transcoder A description.

3.4.1.3 TRANS_HSYNC_B— Transcoder B Horizontal Sync Register

TRANS_HSYNC_B—Transcoder B Horizontal Sync Register	
Register Type:	MMIO
Address Offset:	E1008h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

Bit De	scription
31:29	**Reserved** Project: All Format: MBZ
28:16	**Transcoder_B_Horizontal_Sync_End** Project: All See Transcoder A description.
15:13	**Reserved** Project: All Format: MBZ
12:0	**Transcoder_B_Horizontal_Sync_Start** Project: All See Transcoder A description.

3.4.1.4 TRANS_VTOTAL_B—Transco der B Vertical Total Register

TRANS_VTOTAL_B—Transcoder B Vertical Total Register					
Register Type:	MMIO				
Address Offset:	E100Ch				
Project:	All				
Default Value:	00000000h				
Access:	R/W				
Size (in bits):	32				
Bit De	**scription**				
31:29	**Reserved**	Project:	All	Format:	MBZ
28:16	**Transcoder_B_Vertical_Total_Display_Lines**			Project:	All
	See Transcoder A description.				
15:12	**Reserved**	Project:	All	Format:	MBZ
11:0	**Transcoder_B_Vertical_Active_Display_Lines**			Project:	All
	See Transcoder A description.				

3.4.1.5 TRANS_VBLANK_B—Transco der B Vertical Blank Register

TRANS_VBLANK_B—Transcoder B Vertical Blank Register					
Register Type:	MMIO				
Address Offset:	E1010h				
Project:	All				
Default Value:	00000000h				
Access:	R/W				
Size (in bits):	32				
Bit De	**scription**				
31:29	**Reserved**	Project:	All	Format:	MBZ
28:16	**Transcoder_B_Vertical_Blank_End**			Project:	All
	See Transcoder A description.				
15:13	**Reserved**	Project:	All	Format:	MBZ
12:0	**Transcoder_B_Vertical_Blank_Start**			Project:	All
	See Transcoder A description.				

3.4.1.6 TRANS_VSYNC_ B—Transcoder B Vertical Sync Register

TRANS_VSYNC_B—Transcoder B Vertical Sync Register						
Register Type:	MMIO					
Address Offset:	E1014h					
Project:	All					
Default Value:	00000000h					
Access:	R/W					
Size (in bits):	32					
Bit De	**scription**					
31:29	**Reserved**	Project:	All	Format:	MBZ	
28:16	**Transcoder_B_Vertical_Sync_End** See Transcoder A description.				Project:	All
15:13	**Reserved**	Project:	All	Format:	MBZ	
12:0	**Transcoder_B_Vertical_Sync_Start** See Transcoder A description.				Project:	All

3.4.1.7 TRANS_BCLRPAT_B— Transcoder B Border Color Pattern Register

TRANS_BCLRPAT_B— Transcoder B Border Color Pattern Register						
Register Type:	MMIO					
Address Offset:	E1020h					
Project:	All					
Default Value:	00000000h					
Access:	R/W					
Size (in bits):	32					
See Transcoder A description.						
Bit De	**scription**					
31:24	**Reserved**	Project:	All	Format:		
23:16	**Border_Red_Channel_Value**				Project:	All
15:8	**Border_Green_Channel_Value**				Project:	All
7:0	**Border_Blue_Channel_Value**				Project:	All

3.4.1.8 TRANS_VSYNCSHIF T_B— Transcoder B Vertical Sync Shift Register

TRANS_VSYNCSHIFT_B— Transcoder B Vertical Sync Shift Register					
Register Type:	MMIO				
Address Offset:	E1028h				
Project:	All				
Default Value:	00000000h				
Access:	R/W				
Size (in bits):	32				
Bit De	**scription**				
31:13	**Reserved**	Project:	All	Format:	MBZ
12:0	**Transcoder_B_Second_Field_Vertical_Sync_Shift** See Transcoder A description.			Project:	All

3.5 Transcoder B M/N Values

3.5.1.1 TransBDataM1— Transcoder B Data M value 1

TransBDataM1— Transcoder B Data M value 1					
Register Type:	MMIO				
Address Offset:	E1030h				
Project:	All				
Default Value:	00000000h				
Access:	R/W				
Size (in bits):	32				
Double Buffer Update Point:	Start of Vblank				
Double Buffer Armed By:	Writing the TransBDPLinkN1				
See Transcoder A description					
Bit De	**scription**				
31	**Reserved**	Project:	All	Format:	MBZ
30:25	**TU1_Size** See Transcoder A description.			Project:	All
24	**Reserved**	Project:	All	Format:	MBZ
23:0	**Transcoder_B_Data_M1_value** See Transcoder A description.			Project:	All

3.5.1.2 TransBDataN1— Transcoder B Data N value 1

TransBDataN1— Transcoder B Data N value 1					
Register Type:	MMIO				
Address Offset:	E1034h				
Project:	All				
Default Value:	00000000h				
Access:	R/W				
Size (in bits):	32				
Double Buffer Update Point:	Start of Vblank				
Double Buffer Armed By:	Writing the TransBDPLinkN1				
See Transcoder A description					
Bit De	**scription**				
31:24	**Reserved** Project: All			Format:	MBZ
23:0	**Transcoder_B_Data_N1_value** Project: All See Transcoder A description.				

3.5.1.3 TransBDataM2— Transcoder B Data M value 2

TransBDataM2— Transcoder B Data M value 2					
Register Type:	MMIO				
Address Offset:	E1038h				
Project:	All				
Default Value:	00000000h				
Access:	R/W				
Size (in bits):	32				
Double Buffer Update Point:	Start of Vblank				
Double Buffer Armed By:	Writing the TransBDPLinkN2				
See Transcoder A description					
Bit De	**scription**				
31	**Reserved** Project: All			Format:	MBZ
30:25	**TU2_Size** Project: All See Transcoder A description.				
24	**Reserved** Project: All			Format:	MBZ
23:0	**Transcoder_B_Data_M2_value** Project: All See Transcoder A description.				

3.5.1.4 TransBDataN2— Transcoder B Data N value 2

TransBDataN2— Transcoder B Data N value 2			
Register Type:	MMIO		
Address Offset:	E103Ch		
Project:	All		
Default Value:	00000000h		
Access:	R/W		
Size (in bits):	32		
Double Buffer Update Point:	Start of Vblank		
Double Buffer Armed By:	Writing the TransBDPLinkN2		
See Transcoder A description			
Bit De	**scription**		
31:24	**Reserved** Project: All	Format: MBZ	
23:0	**Transcoder_B_Data_N2_value** Project: All See Transcoder A description.		

3.5.1.5 TransBDPLinkM1— Transcoder B Link M value 1

TransBDPLinkM1— Transcoder B Link M value 1			
Register Type:	MMIO		
Address Offset:	E1040h		
Project:	All		
Default Value:	00000000h		
Access:	R/W		
Size (in bits):	32		
Double Buffer Update Point:	Start of Vblank		
Double Buffer Armed By:	Writing the TransBDPLinkN1		
See Transcoder A description			
Bit De	**scription**		
31:24	**Reserved** Project: All	Format: MBZ	
23:0	**Transcoder_B_Link_M1_value** Project: All See Transcoder A description.		

3.5.1.6 TransBDPLinkN1— Transcoder B Link N value 1

TransBDPLinkN1— Transcoder B Link N value 1			
Register Type:	MMIO		
Address Offset:	E1044h		
Project:	All		
Default Value:	00000000h		
Access:	R/W		
Size (in bits):	32		
Double Buffer Update Point:	Start of Vblank		
Double Buffer Armed By:	Writing the TransBDPLinkN1		
See Transcoder A description			
Bit De	**scription**		
31:24	**Reserved** Project: All	Format: MBZ	
23:0	**Transcoder_B_Link_N1_value** Project: All See Transcoder A description.		

3.5.1.7 TransBDPLinkM2— Transcoder B Link M value 2

TransBDPLinkM2— Transcoder B Link M value 2			
Register Type:	MMIO		
Address Offset:	E1048h		
Project:	All		
Default Value:	00000000h		
Access:	R/W		
Size (in bits):	32		
Double Buffer Update Point:	Start of Vblank		
Double Buffer Armed By:	Writing the TransBDPLinkN2		
See Transcoder A description			
Bit De	**scription**		
31:24	**Reserved** Project: All	Format: MBZ	
23:0	**Transcoder_B_Link_M2_value** Project: All See Transcoder A description.		

3.5.1.8 TransBDPLinkN2— Transcoder B Link N value 2

TransBDPLinkN2— Transcoder B Link N value 2	
Register Type:	MMIO
Address Offset:	E104Ch
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Star of Vblank
Double Buffer Armed By:	Writing the TransBDPLinkN2
See Transcoder A description	

Bit De	scription
31:24	**Reserved** Project: All Format: MBZ
23:0	**Transcoder_B_Link_N2_value** Project: All See Transcoder A description.

3.6 Transcoder B Video DIP

3.6.1.1 VIDEO_DI P_CTL_B—Video DIP Control for Transcoder B

VIDEO_DIP_CTL_B—Video DIP Control for Transcoder B	
Register Type:	MMIO
Address Offset:	E1200h
Project:	All
Default Value:	20000000h
Access:	R/W
Size (in bits):	32
See Transcoder A description.	

Bit De	scription
31	**Enable_Graphics_Data_Island_Packet** Project: All See Transcoder A description.
30:29	**Port_Select** Project: All See Transcoder A description.
28:26	**Reserved** Project: All Format:
25	**GCP_DIP_enable** Project: All See Transcoder A description. This bit shoud not be enabled for 8bpc mode if at least one of the other HDMI ports is enabled in 12bpc mode.
24:21	**Data_Island_Packet_type_enable** Project: All See Transcoder A description.
20:19	**DIP_buffer_index** Project: All See Transcoder A description.
18	**Reserved** Project: All Format:
17:16	**Video_DIP_transmission_frequency** Project: All See Transcoder A description.
15:12	**Reserved** Project: All Format: MBZ
11:8	**Video_DIP_buffer_size** Project: All Access: Read Only Default Value: 0b See Transcoder A description.
7:4	**Reserved** Project: All Format: MBZ
3:0	**Video_DIP_RAM_access_address** Project: All See Transcoder A description.

3.6.1.2 VIDEO_DIP_DATA_B–Video Data Island Packet Data for Transcoder B

VIDEO_DIP_DATA_B–Video Data Island Packet Data for Transcoder B	
Register Type:	MMIO
Address Offset:	E1208h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

Bit De	scription
31:0	**Video_DIP_DATA** Project: All Format: See Transcoder A description.

3.6.1.3 VIDEO_DIP_GDCP_PAYLOAD_B–Video Data Island Payload for Transcoder B

VIDEO_DIP_GDCP_PAYLOAD_B–Video Data Island Payload for Transcoder B	
Register Type:	MMIO
Address Offset:	E1210h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

Bit De	scription
31:3	**Reserved** Project: All Format: MBZ
2	**Reserved_for_GCP_color_indication** Project: All See Transcoder A description.
1	**GCP_default_phase_enable** Project: All See Transcoder A description.
0	**GCP_AV_mute** Project: All See Transcoder A description.

3.7 CRT DAC

3.7.1.1 ADP—Analog Display Port Control Register (CRT DAC)

ADP—Analog Display Port Control Register (CRT DAC)	
Register Type:	MMIO
Address Offset:	E1100h
Project:	All
Default Value:	00040000h
Access:	R/W
Size (in bits):	32

Bit De	scription
31	**Analog_Display-Port_Enable** Project: All Default Value: 0b This bit enables or disables the analog port CRT DAC and syncs outputs.

Value Na	me	Description	Project
0b	Disable	Disable the analog port DAC and disable output of syncs	All
1b	Enable	Enable the analog port DAC and enable output of syncs	All

Bit De	scription
30	**Transcoder_Select** Project: All Default Value: 0b Determines which transcoder will feed this DAC port.

Value Na	me	Description	Project
0b	Transcoder A	Transcoder A	All
1b	Transcoder B	Transcoder B	All

Bit De	scription
29:26	**Reserved** Project: All Format:

ADP—Analog Display Port Control Register (CRT DAC)

25:24

CRT_Hot_Plug_Detection_Channel_Status

Project: All

Access: Read Only

Default Value: 00b

These bits are set when a CRT hot plug or unplug event has been detected and indicate which color channels were attached. Write a one to these bits to clear the status. The rising or falling edges of these bits are ORed together to go to the main ISR CRT hot plug register bit.

Value Na	me	Description	Project
00b	None	No channels attached	All
01b	Blue	Blue channel only is attached	All
10b	Green	Green channel only is attached	All
11b	Both	Both blue and green channel attached	All

23

CRT_Hot_Plug_Detection_Enable

Project: All

Default Value: 0b

Hot plug detection is used to set status bits or an interrupt on the connection or disconnection of a CRT to the analog display port.

Value Na	me	Description	Project
0b	Disable	CRT hot plug detection is disabled	All
1b	Enable	CRT hot plug detection is enabled	All

22

CRT_Hot_Plug_Circuit_Activation_Period

Project: All

Default Value: 0b

This bit sets the activation period for the CRT hot plug circuit.

Value Na	me	Description	Project
0b	64 cdclk	64 cdclk periods	All
1b	128 cdclk	128 cdclk periods	All

21

CRT_Hot_Plug_Detect_Warmup_Time

Project: All

Default Value: 0b

This bit sets the warmup time for the CRT hot plug circuit.

Value Na	me	Description	Project
0b	2M pcdclks	2M pcdclks warmup (approximately 5ms)	All
1b	4M pcdclks	4M pcdclks warmup (approximately 10ms)	All

ADP—Analog Display Port Control Register (CRT DAC)

20 — CRT_Hot_Plug_Detect_Sampling_Period

Project: All

Default Value: 0b

This bit determines the length of time between sampling periods when the transcoder is disabled.

Value Na	me	Description	Project
0b	1G pcdclks	1G pcdclks (approximately 2 seconds)	All
1b	2G pcdclks	2G pcdclks (approximately 4 seconds)	All

19:18 — CRT_Hot_Plug_Voltage_Compare_Value

Project: All

Default Value: 01b 50

Compare value for Vref to determine whether the analog port is connected to a CRT.

Value Na	me	Description	Project
00b	40	40	All
01b	50	50 (Default)	All
10b	60	60	All
11b	70	70 (bit 17 must be = 1)	All

17 — CRT_Hot_Plug_Reference_Voltage

Project: All

Default Value: 0b

Value Na	me	Description	Project
0b	325mv	325mv	All
1b	475mv	475mv (bits 19:18 must be = 11)	All

16 — Force_CRT_Hot_Plug_Detect_Trigger

Project: All

Default Value: 0b

Triggers a CRT hotplug/unplug detection cycle independent of the hot plug detection enable bit. This bit is automatically cleared after the detection is completed. The result of this trigger is reflected in the CRT Hot Plug Detection Status. Software must reset status after a force CRT detect trigger.

Value Na	me	Description	Project
0b	No Trigger	No Trigger	All
1b	Force Trigger	Force Trigger	All

15:5 — Reserved Project: All Format:

ADP—Analog Display Port Control Register (CRT DAC)

4 — **VSYNC_Polarity_Control**

Project: All

Default Value: 0b

The output VSYNC polarity is controlled by this bit. This is used to implement display modes that require inverted polarity syncs and to set the disabled state of the VSYNC signal.

Value Na	me	Description	Project
0b	Low	Active Low	All
1b	High	Active High	All

3 — **HSYNC_Polarity_Control**

Project: All

Default Value: 0b

The output HSYNC polarity is controlled by this bit. This is used to implement display modes that require inverted polarity syncs and to set the disabled state of the HSYNC signal.

Value Na	me	Description	Project
0b	Low	Active Low	All
1b	High	Active High	All

2:0 — **Reserved** Project: All Format:

3.8 HDMI port C

3.8.1.1 HDMIC—Digital Display Port C Register

HDMIC—Digital Display Port C Register	
Register Type:	MMIO
Address Offset:	E1150h
Project:	All
Default Value:	00000018h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Depends on bit

Bit De	scription
31	**HDMIC_Enable(Digital_Display_Port_C_Enable)** Project: All Default Value: 0b Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written. Both this bit and bit 6 of this register must be enabled to send audio over this port in HDMI mode. This port must not be enabled simultaneously with DisplayPort C. [DevIBX] When disabling the port, software must temporarily enable the port with transcoder select (bit #30) cleared to '0' after disabling the port. This is workaround for hardware issue where the transcoder select set to '1' will prevent DPC from being enabled on transcoder A. [DevIBX] Software must write this bit twice when enabling the port (setting to '1') as a workaround for hardware issue that may result in first write getting masked. [DevIBX] Toggle this bit off then on at the end of mode set sequence when enabling HDMI 12-bit per color with pixel repeat.

Value Na me	Description	Project
0b	Disable	Disable and tristates the Digital Display Port C interface for HDMI or DVI modes.	All
1b	Enable	Enable. This bit enables the Digital Display Port C interface for HDMI or DVI modes.	All

HDMIC—Digital Display Port C Register

30 — Transcoder_Select

Project: All

Default Value: 0b

See HDMIB Description.

[DevIBX] Writing to this bit only takes effect when port is enabled. Due to hardware issue it is required that this bit be cleared when port is disabled. To clear this bit software must temporarily enable this port on transcoder A.

Value Name	Description	Project
0b	Transcoder A	All
1b	Transcoder B	All

29 — Reserved Project: All Format: MBZ

28:26 — Color_Format

Project: All

Default Value: 0b

See HDMIB Description.

Value Name	Description	Project
000b	8 bits per color	All
011b	12 bits per color	All
others	Reserved	All

25:19 — Reserved Project: All Format:

18 — Clock_Output_Inversion

Project: All

Security: Test

Default Value: 0b

See HDMIB Description.

Value Name	Description	Project
0b	Clock output is NOT inverted	All
1b	Clock output is inverted	All

17:16 — Reserved Project: All Format:

HDMIC—Digital Display Port C Register

15 — **Port_Lane_Reversal**

Project: All

Default Value: 0b

See HDMIB Description.

Value Name	Description	Project
0b	Not reversed	All
1b	Reversed	All

14:10 — **Reserved** Project: All Format: MBZ

9 — **Null_packets_enabled_during_Vsync**

Project: All

Default Value: 0b

See HDMIB Description.

Value Name	Description	Project
0b	Disable null infoframe packets when Vsync=1 on this port.	All
1b	Enable null infoframe packets when Vsync=1 on this port.	All

8:7 — **Reserved** Project: All Format: MBZ

6 — **Audio_Output_Enable**

Project: All

Default Value: 0b

See HDMIB Description.

Value Name	Description	Project
0b	No audio output on this port	All
1b	Enable audio on this port	All

5 — **Reserved**

4:3 — **Sync_Polarity**

Project: All

Default Value: 11b VS and HS are active high

See HDMIB Description.

Value Name	Description	Project
00b	VS and HS are active low (inverted)	All
01b	VS is active low (inverted), HS is active high	All
10b	VS is active high, HS is active low (inverted)	All
11b	VS and HS are active high (Default)	All

HDMIC—Digital Display Port C Register

2	**Digital_Port_C_Detected** Project: All Access: Read Only Default Value: 0b Read-only bit indicating whether a digital port C was detected during initialization. It signifies the level of the GMBUS port 3 (port C) data line at boot. This bit is valid regardless of whether the port is enabled.

Value	Name	Description	Project
0b	Not Detected	Digital Port C not detected during initialization	All
1b	Detected	Digital Port C detected during initialization	All

1:0	**Reserved** Project: All Format: MBZ

3.9 HDMI port D

3.9.1 HDMID—Digital Display Port D Register

HDMID—Digital Display Port D Register	
Register Type:	MMIO
Address Offset:	E1160h
Project:	All
Default Value:	00000018h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Depends on bit

Bit De	scription
31	**HDMID_Enable(Digital_Display_Port_D_Enable)** Project: All Default Value: 0b Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written. Both this bit and bit 6 of this register must be enabled to send audio over this port in HDMI mode. This port must not be enabled simultaneously with DisplayPort D. [DevIBX] When disabling the port, software must temporarily enable the port with transcoder select (bit #30) cleared to '0' after disabling the port. This is workaround for hardware issue where the transcoder select set to '1' will prevent DPD from being enabled on transcoder A. [DevIBX] Software must write this bit twice when enabling the port (setting to '1') as a workaround for hardware issue that may result in first write getting masked. [DevIBX] Toggle this bit off then on at the end of mode set sequence when enabling HDMI 12-bit per color with pixel repeat.

Value	Name	Description	Project
0b	Disable	Disable and tristates the Digital Display Port D interface for HDMI or DVI modes.	All
1b	Enable	Enable. This bit enables the Digital Display Port D interface for HDMI or DVI modes.	All

HDMID—Digital Display Port D Register

30 — Transcoder_Select

Project: All

Default Value: 0b

See HDMIC Description.

[DevIBX] Writing to this bit only takes effect when port is enabled. Due to hardware issue it is required that this bit be cleared when port is disabled. To clear this bit software must temporarily enable this port on transcoder A.

Value Name	Description	Project
0b	Transcoder A	All
1b	Transcoder B	All

29 — Reserved Project: All Format: MBZ

28:26 — Color_Format

Project: All

Default Value: 0b

See HDMIC Description.

Value Name	Description	Project
000b	8 bits per color	All
011b	12 bits per color	All
others	Reserved	All

25:19 — Reserved Project: All Format:

18 — Clock_Output_Inversion

Project: All

Security: Test

Default Value: 0b

See HDMIC Description.

Value Name	Description	Project
0b	Clock output is NOT inverted	All
1b	Clock output is inverted	All

17:16 — Reserved Project: All Format:

HDMID—Digital Display Port D Register

15 — Port_Lane_Reversal

Project: All

Default Value: 0b

See HDMIC Description.

Value Name	Description	Project
0b	Not reversed	All
1b	Reversed	All

14:10 — Reserved Project: All Format: MBZ

9 — Null_packets_enabled_during_Vsync

Project: All

Default Value: 0b

See HDMIC Description.

Value Name	Description	Project
0b	Disable	Disable null infoframe packets when Vsync=1 on this port.	All
1b	Enable	Enable null infoframe packets when Vsync=1 on this port.	All

8:7 — Reserved Project: All Format: MBZ

6 — Audio_Output_Enable

Project: All

Default Value: 0b

See HDMIC Description.

Value Name	Description	Project
0b	Disable	No audio output on this port	All
1b	Enable	Enable audio on this port	All

5 Reserved

4:3 — Sync_Polarity

Project: All

Default Value: 11b VS and HS are active high

See HDMIC Description.

Value Name	Description	Project
00b	VS-HS Low	VS and HS are active low (inverted)	All
01b	VS Low, HS High	VS is active low (inverted), HS is active high	All
10b	Vs High, HS Low	VS is active high, HS is active low (inverted)	All
11b	High	VS and HS are active high (Default)	All

HDMID—Digital Display Port D Register

2 — **Digital_Port_D_Detected**

Project: All

Access: Read Only

Default Value: 0b

Read-only bit indicating whether a digital port D was detected during initialization. It signifies the level of the GMBUS port 5 (port D) data line at boot. This bit is valid regardless of whether the port is enabled.

Value Name		Description	Project
0b	Not Detected	Digital Port D not detected during initialization	All
1b	Detected	Digital Port D detected during initialization	All

1:0 — **Reserved** Project: All Format: MBZ

3.10 LVDS

3.10.1.1 LVDS—LVDS Port Control Register

LVDS—LVDS Port Control Register

Register Type: MMIO
Address Offset: E1180h
Project: All
Default Value: 40000000h
Access: R/W Protect
Size (in bits): 32

Write Protect by Panel Power Sequencer

Bit	Description
31	**LVDS_Port_Enable** Project: All Default Value: 0b When disabled the LVDS port is inactive and in it's low power state. Enabling the LVDS port changes the way that the PLL for this transcoder is programmed. This bit must be set before the display PLL is enabled and the port is power sequenced on using the panel power sequencing logic.
30	**LVDS_Port_Transcoder_Select** Project: All Default Value: 1b Transcoder B
29:25	**Reserved** Project: All Format:

Value	Name	Description	Project
0b	Disable	The port is disabled and all LVDS pairs are powered down.	All
1b	Enable	The port is enabled (port must be enabled before powering up a connected panel)	All

Value	Name	Description	Project
0b	Transcoder A	The port gets data from Transcoder A	All
1b	Transcoder B	The port gets data from Transcoder B	All

LVDS—LVDS Port Control Register

24 **Data_Format_Select**

Project: All

Default Value: 0b

Combined with the other control bits it selects the LVDS data format. Other control bits in this register determine if two channel is enabled and 18 or 24 bit color is enabled.

Value Name	Description	Project
0b	1x18.0, 2x18.0, 1x24.0 or 2x24.0	1x18.0, 2x18.0, 1x24.0 or 2x24.0	All
1b	1x24.1 or 2x24.1	1x24.1 or 2x24.1	All

23 **LE_Control_Enable**

Project: All

Default Value: 0b

This bit is used when the second channel control signal field indicates that we are using the LE instead of HS and the two channel mode is enabled. In single channel mode, this bit has no effect.

Value Name	Description	Project
0b	Send 0	Send 0 on second channel HS (B2<2>)	All
1b	Send 1	Send 1 on second channel HS	All

22 **LF_Control_Enable**

Project: All

Default Value: 0b

This bit is used when the second channel control signal field indicates that we are using the LF instead of VS and two channel mode is enabled. In single channel mode, this bit has no effect.

Value Name	Description	Project
0b	Send 0	Send 0 on second channel VS (B2<3>)	All
1b	Send 1	Send 1 on second channel VS	All

21 **VSYNC_Polarity**

Project: All

Default Value: 0b

This controls the polarity of the VSYNC indicator that is sent over the LVDS connection. Panels may require one or the other polarity or work with either polarity.

Value Name	Description	Project
0b	No Invert	No inversion (1=active)	All
1b	Invert	Invert the sense (0=active)	All

LVDS—LVDS Port Control Register

20

HSYNC_Polarity(LP_Invert)

Project: All

Default Value: 0b

This controls the polarity of the HSYNC indicator that is sent over the LVDS connection. Panels may require one or the other polarity or work with either polarity.

Value Name		Description	Project
0b	No Invert	No inversion (1=active)	All
1b	Invert	Invert the sense (0=active)	All

19

DE_Invert

Project: All

Default Value: 0b

This controls the polarity of the DE indicator that is sent over the LVDS connection.

Value Name		Description	Project
0b	No Invert	No inversion of DE (1=active)	All
1b	Invert	Invert the sense of DE (0=active)	All

18:17

Second_Channel_Control_Signals

Project: All

Default Value: 00b

This bit only applies to the two channel modes of operation it has no effect in single channel modes.

Value Name		Description	Project
00b		Send DE, HS, VS on second channel if enabled	All
01b	Reserved	Reserved	All
10b		Do not send DE, HS, VS on second channel use zero instead	All
11b		Use DE=0, HS=LE, VS=LF on second channel	All

16

Channel_Reserved_Bits

Project: All

Default Value: 0b

Value Name		Description	Project
0b	Send 0	Send 0 for the channel reserved bits	All
1b	Send Duplicate	Send duplicate data bit for reserved bits	All

LVDS—LVDS Port Control Register

15 — **LVDS_Border_Enable**

Project: All

Default Value: 0b

This selects whether the border data should be included in the active display data sent to the panel.

Value	Name	Description	Project
0b	Disable	Border to the LVDS transmitter is disabled. DE (Display Enable) is used	All
1b	Enable	Border to the LVDS transmitter is enabled. Blank# is used as DE for the panel	All

14:11 — **Reserved** Project: All Format:

10 — **Buffer_Power_Down_State**

Project: All

Default Value: 0b

This bit selects the state of the LVDS buffers during a powered down state caused by the power sequence logic power down. This selection will be made based on the connected panel requirements.

Value	Name	Description	Project
0b	Zero	Zero Volts (Driven on both lines of the pairs)	All
1b	Tri-State	Tri-State (High impedance state)	All

9:8 — **ClkA,A0,A1,A2_Control**

Project: All

Default Value: 00b

This field controls the A0-A2 data pairs and CLKA. It sets the highest level of activity that is allowed on these lines when the panel is powered on. Power sequencing for LVDS connected panels overrides the control. When the power sequencer is in the power down mode all signals are in the power down state.

Value	Name	Description	Project
00b	Power Down	Power Down all A channel signals including A3 (0V)	All
01b	Power Up Data 0	Power up – A0, A1, A2 Data bits forced to 0,Timing active, Clock Active	All
10b	Reserved	Reserved	All
11b	Power Up All Active	Power up – Data lines and clock active	All

LVDS—LVDS Port Control Register

7:6

Eight_bit_color_channel_A3,(B3)_Control

Project: All

Default Value: 00b

This field can control both the A3 and B3 data pairs. Enabling those pairs indicates the selection of 8-bit per color channel mode. It sets the highest level of activity that is allowed on these lines when the panel is powered on. The A3 pair will only be powered up if both this field and the A0, A1, A2, CLKA field indicates that the pair should be powered up and will only be active if both indicate that it should be active. The B3 pair will only be powered up if both this field and the B0, B1, B2, (B3) field indicates that the pair should be powered up and will only be active if both indicate that it should be active. Power sequencing for LVDS connected panels overrides the control. When the power sequencer is in the power down mode all signals are in the power down state.

Value	Name	Description	Project
00b	Power Down	Power Down all signals A3, B3 (common mode)	All
01b	Power Up Data 0	Power up – A3, (B3) Data (pixel data not control) lines forced to 0 output	All
10b	Reserved	Reserved	All
11b	Power Up Data Active	Power up – A3, (B3) Data lines active	All

5:4

Two_channel_mode_ClkB_Control

Project: All

Default Value: 00b

When in two channel mode, this field controls the CLKB pair. It sets the highest level of activity that is allowed on these lines when the panel is powered on. The CLKB pair should only be powered up if the B0, B1, B2, (B3) field indicates that the second channel should be powered up and will only be active if both indicate that it should be active. Power sequencing for LVDS connected panels overrides the control.

Value	Name	Description	Project
00b	Power Down	Power Down CLKB (common mode)	All
01b	Power Up CLKB 0	Power up – CLKB Forced to 0	All
10b	Reserved	Reserved	All
11b	Power Up CLKB Active	Power up – Clock B active	All

LVDS—LVDS Port Control Register

3:2

Two_channel_mode_B0,B1,B2_Control

Project: All

Default Value: 00b

This field controls both the set B0-B2 data pairs. It sets the highest level of activity that is allowed on these lines when the panel is powered on. Power sequencing for LVDS connected panels overrides the control. During single channel operation (1x18.0), these bits need to be both zero. Two channel operation is selected by setting them to ones. Note that the second clock can be optionally enabled or disabled by the two channel mode ClkB control field.

Value	Name	Description	Project
00b	Power Down	Power Down all signals including B3 and CLKB	All
01b	Power Up Data 0	Power up – B0, B1, B2, Data lines forced to 0, timing is active	All
10b	Reserves	Reserved	All
11b	Power Up Data Active	Power up – Data lines active (color and timing)	All

1

LVDS_detected

Project: All

Access: Read Only

Default Value: 0b

Read-only bit indicating whether LVDS was detected during initialization. It signifies the level of the GMBUS port 2 (LVDS) data line at boot. This bit is valid regardless of whether the port is enabled.

Value	Name	Description	Project
0b	Not Detected	LVDS not detected during initialization	All
1b	Detected	LVDS detected during initialization	All

0

Reserved Project: All Format:

4. South FDI Rx and Transcoder Control (F0000h–FBFFFh)

4.1.1 Display Transcoder A Control

4.1.1.1 TRANSACONF—Transcode r A Configuration Register

TRANSACONF—Transcoder A Configuration Register	
Register Type:	MMIO
Address Offset:	F0008h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank OR transcoder disabled

Bit De	scription
31	**Transcoder_A_Enable** Project: All Setting this bit to the value of one, turns on transcoder A. This must be done before FDI A is enabled. Changing it to a zero should only be done when FDI A has been disabled. Turning the transcoder enable bit off disables the timing generator in this transcoder. FDI disable occurs after the next VBLANK event after the FDI is disabled. Synchronization pulses to the display are not maintained if the timing generator is disabled. Transcoder timing registers must contain valid values before this bit is enabled. **Value Na me** / **Description** / **Project** 0b Disable / Disabled / All 1b Enable / Enabled / All
30	**Transcoder_State** Project: All This **read only** bit indicates the actual state of the transcoder. Since there can be some delay between disabling the transcoder and the transcoder actually shutting off, this bit indicates the true current state. **Value Na me** / **Description** / **Project** 0b Disable / Disabled / All 1b Enable / Enabled / All
29	**Reserved** Project: All Format:
28:27	**Reserved**

TRANSACONF—Transcoder A Configuration Register

26	**Reserved** Project: All Format:
25	**Reserved**
24	**Reserved** Project: All Format:
23:21	**Interlaced_Mode** Project: All Default Value: 000b These bits are used to indicate what interlaced mode is being set in the pipe, and must be set by software during transcoder setup (mode set). They are updated immediately if the transcoder is off, or in the vertical blank after programming if transcoder is enabled. The default behavior is to have Interlaced/Progressive selection driven by PIPEACONF and transmitted over FDI VB-ID.
20:8	**Reserved** Project: All Format:
4:2	**Reserved** Project: All Format:
1	**Reserved**
0	**Reserved** Project: All Format: MBZ

Value Name	Description	Project
000b Progressive	Progressive display	All
010b Reserved	Reserved	All
011b Interlace	Interlaced display, programmable Vsync for CRT, DP	All
Others Reserved	Reserved	All

4.1.2 Display Transcoder B Control

4.1.2.1 TRANSBCONF—Transcode r B Configuration Register

TRANSBCONF—Transcoder B Configuration Register	
Register Type:	MMIO
Address Offset:	F1008h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank OR transcoder disabled

Bit De	scription
31	**Transcoder_B_Enable** Project: All Format: See Transcoder A description
30	**Transcoder_State** Project: All Format: See Transcoder A description
29	**Reserved** Project: All Format:
28:27	**Frame_Start_Delay** Project: All Format: See Transcoder A description
26	**Reserved** Project: All Format:
25	**Reserved** Project: All
24	**Reserved** Project: All Format:
23:21	**Reserved** Project: All
20:8	**Reserved** Project: All Format:
7:5	**Display_Port_Bits_Per_Color** Project: All Format: See Transcoder A description
4:2	**Reserved** Project: All Format:
1	**Reserved** Project: All
0	**Reserved** Project: All Format: MBZ

4.1.3 FDI A Receiver Control

4.1.3.1 FDI_RXA_CTL- FDI A Rx Control Register

FDI_RXA_CTL- FDI A Rx Control Register	
Register Type:	MMIO
Address Offset:	F000Ch
Project:	All
Default Value:	00000040h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Depends on bit

Bit De	scription
31	**FDI_Rx_A_Enable** Project: All Default Value: 0b Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written. Please note that link A is hardwired to transcoder A. **Value Na / me / Description / Project** 0b / Disable / Disables and tristates the FDI Rx A interface / All 1b / Enable / Enable. This bit enables the FDI Rx A interface. / All
30	**Reserved** Project: All Format: MBZ
29:28	**Link_training_pattern_enable** Project: All Default Value: 0b **Value Na / me / Description / Project** 00b / Pattern 1 / Pattern 1 enabled: Repetition of D10.2 characters. / All 01b / Pattern 2 / Pattern 2 enabled: Repetition of K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2. / All 10b / Idle / Idle Pattern enabled: Transmit single-context scheduling followed by VB-ID with NoVideoStream_flag set to 1, five times / All 11b / Normal / Link not in training: Send normal pixels / All
27:22	**Reserved** Project: All Format:

FDI_RXA_CTL- FDI A Rx Control Register

21:19 Port_Width_Selection

Project: All

Default Value: 0b

Value Name		Description	Project
000b	x1 Mode	x1 Mode	All
001b	x2 Mode	x2 Mode	All
010b	x3 Mode	x3 Mode	All
011b	x4 Mode	x4 Mode	All
111b	x8 Mode	x8 Mode	All
Others	Reserved	Reserved	All

18:16 Bits_Per_Color

Project: All

Default Value: 0b

This field selects the number of bits per color sent over the link. Color format takes place on the Vblank after being written. Color format change can be done independent of a pixel clock change in the link.

Value Name		Description	Project
000b	8 bpc	8 bits per color	All
001b	10 bpc	10 bits per color	All
010b	6 bpc	6 bits per color	All
011b	12 bpc	12 bits per color	All
1XXb	Reserved	Reserved	All

15 Link_reversal_strap_override

Project: All

Default Value: 0b

Link is reversed if DMI is reversed. This bit overrides the status of DMI reversal to the reverse of what is strapped. It must be set before the link is enabled in order to take effect. Writing to this bit when the link is enabled has no effect. Both link A and link B must be off in order for this bit to take effect.

Value Name		Description	Project
0b	Not Overwritten	Link reversal strap not overwritten	All
1b	Overwritten	Link reversal strap overwritten.	All

FDI_RXA_CTL- FDI A Rx Control Register

14	**DMI_Link_reversal_status** Project: All Access: Read Only Default Value: 0b This bit reflects the DMI link reversal strap. **Value Name** / **Description** / **Project** 0b Not Reversed — Link not reversed — All 1b Reversed — Link reversed. — All
13	**FDI_PLL_enable** Project: All Format: Enable This bit enables the FDI PLL. Software must enable this bit 10uS prior to enabling the link. This bit can be set in either FDI RXA or FDI RXB Control registers.
12:9	**Reserved** Project: All
8	**Reserved**
7	**Reserved** Project: All
6	**Reserved** Project: All
5	**Reserved**
4	**Rawclk_to_PCDCLK_selection** Project: All Default Value: 0b This bit switches PCH display clocking from the raw oscillator clock to PCDCLK (or vice versa). It must be programmed as part of enabling and disabling the link. If FDI PLL is disabled, this register will be disregarded and Rawclk will be used. Please see the mode set / boot flow for more detail. This bit can be set in either FDI RXA or FDI RXB Control registers. **Value Name** / **Description** / **Project** 0b Rawclk — Rawclk used — All 1b PCDCLK — PCDCLK used — All
3:0	**Reserved** Project: All Format: MBZ

4.1.3.2 FDI_RXA_MISC— FDI A Rx Miscellaneous

FDI_RXA_MISC— FDI A Rx Miscellaneous	
Register Type:	MMIO
Address Offset:	F0010h
Project:	All
Default Value:	00000080h
Access:	R/W
Size (in bits):	32

Bit De	scription
31:13	**Reserved** Project: All Format: MBZ
12:0	**FDI_Delay** Project: All Default Value: 80h Default 80h. This field specifies latency as relative delay w.r.t. the dot clock required for active data over the FDI interface to reach the timing generator FIFO in the transcoder. Specific calculations (if required) to be provided later.

4.1.3.3 FDI_RXA_ISR — FDI A Rx Interrupt Status Register

FDI_RXA_ISR — FDI A Rx Interrupt Status Register	
Register Type:	MMIO
Address Offset:	F0014h
Project:	All
Default Value:	00000000h
Access:	Read Only
Size (in bits):	32

The ISR register contains the non-persistent value of FDI Receiver A interrupt status bits. FDI_RXA_IMR selects which of these interrupt conditions are reported on the combined FDI_RXA interrupt in the SDEISR.

Bit De	scription
31:11	**Reserved** Project: All Format:
10	**FDI_RX_Inter-lane_Alignment** Project: All This bit indicates all the lanes are properly inter-lane aligned

Value Na	me	Description	Project
0b	Not Aligned	Inter-lane symbols are not aligned	All
1b	Aligned	Inter-lane symbols are properly aligned	All

FDI_RXA_ISR — FDI A Rx Interrupt Status Register

9 — FDI_RX_Symbol_Lock

Project: All

This bit indicates receiver logic consecutively received training pattern 2 successfully on all the enabled lanes

Value	Name	Description	Project
0b	Not Locked	Symbol is not locked	All
1b	Locked	Symbol lock is achieved	All

8 — FDI_RX_Bit_Lock

Project: All

This bit indicates receiver logic consecutively received D10.2 pattern in training pattern 1 successfully on all the enabled lanes.

Value	Name	Description	Project
0b	Not Locked	Bit is not locked	All
1b	Locked	Bit lock is achieved	All

7 — FDI_RX_Training_Pattern_2_Fail

Project: All

This bit indicates that the training pattern 2 has failed

Value	Name	Description	Project
0b	No Error	Pattern 2 training did not report an error	All
1b	Failed	Pattern 2 has failed	All

6 — Reserved Project: All Format:

5 — FDI_RX_AFE_BIT_Unlocked

Project: All

This bit indicates DRC circuit detects that the recovered clock has drifted from the received data

Value	Name	Description	Project
0b	No Drift	Recovered clock does not drift from the received data	All
1b	Drift	Recovered clock has drifted from the received data	All

4 — FDI_RX_Symbol_Error_Rate_above_10^-9

Project: All

This bit indicates the received symbol error rate is more than 10^-9.

Value	Name	Description	Project
0b	Less than	The received symbol error rate is not greater than 10^-9	All
1b	Greater than	The received symbol error rate is greater than 10^-9	All

FDI_RXA_ISR — FDI A Rx Interrupt Status Register

3	**Reserved**
2	**FDI_RX_Pixel_FIFO_Overflow** Project: All This bit indicates weather the Pixel FIFO overflowed or not. **Value Name** / **Description** / **Project** 0b — No Overflow — Pixel FIFO did not overflow — All 1b — Overflow — Pixel FIFO overflowed — All
1	**FDI_RX_Cross_Clock_FIFO_Overflow** Project: All This bit indicates weather the Cross Clock symbol clock to display clock FIFO overflowed or not. **Value Name** / **Description** / **Project** 0b — No Overflow — Cross Clock FIFO did not overflow — All 1b — Overflow — Cross Clock FIFO overflowed — All
0	**FDI_RX_Symbol_Queue_overflow** Project: All This bit indicates weather the symbol queue overflowed or not. **Value Name** / **Description** / **Project** 0b — No Overflow — Symbol Queue did not overflow — All 1b — Overflow — Symbol Queue overflowed — All

4.1.3.4 FDI_RXA_IMR — FDI A Rx Interrupt Mask Register

FDI_RXA_IMR — FDI A Rx Interrupt Mask Register			
Register Type:	MMIO		
Address Offset:	F0018h		
Project:	All		
Default Value:	000007FFh		
Access:	R/W		
Size (in bits):	32		
The IMR register is used by software to control which FDI_RXA_ISR bits are “masked” or “unmasked”. “Unmasked” bits will be reported on the combined FDI_RXA interrupt in the SDEISR. "Masked” bits will not be reported.			
Bit De	**scription**		
31:11	**Reserved** Project: All Format: MBZ		
10:0	**Interrupt_Mask_Bits** Project: All Format: Interrupt Control Registers This field contains a bit mask which selects which interrupt bits from the FDI_RXA_ISR are reported on the combined FDI_RXA interrupt in the SDEISR.		
	Value Na	**me**	**Description** / **Project**
	0b	Not Masked	Not Masked – will be reported on the combined FDI_RXA interrupt in the main SDEISR / All
	1b	Masked	Masked – will not be reported / All

4.1.4 FDI B Receiver Control

4.1.4.1 FDI_RXB_ISR — FDI B Rx Interrupt Status Register

FDI_RXB_ISR — FDI B Rx Interrupt Status Register

Register Type: MMIO
Address Offset: F1014h
Project: All
Default Value: 00000000h
Access: Read Only
Size (in bits): 32

See FDI_RXA description.

Bit De	scription
31:11	**Reserved** Project: All Format:
10	**FDI_RX_Inter-lane_Alignment** Project: All See FDI_RXA description **Value Na me** / **Description** / **Project** 0b Not Aligned — Inter-lane symbols are not aligned — All 1b Aligned — Inter-lane symbols are properly aligned — All
9	**FDI_RX_Symbol_Lock** Project: All See FDI_RXA description **Value Na me** / **Description** / **Project** 0b Not Locked — Symbol is not locked — All 1b Locked — Symbol lock is achieved — All
8	**FDI_RX_Bit_Lock** Project: All See FDI_RXA description. **Value Na me** / **Description** / **Project** 0b Not Locked — Bit is not locked — All 1b Locked — Bit lock is achieved — All

FDI_RXB_ISR — FDI B Rx Interrupt Status Register

7 — FDI_RX_Training_Pattern_2_Fail

Project: All

See FDI_RXA description

Value	Name	Description	Project
0b	No Error	Pattern 2 training did not report an error	All
1b	Failed	Pattern 2 has failed	All

6 — Reserved Project: All Format:

5 — FDI_RX_AFE_BIT_Unlocked

Project: All

See FDI_RXA description

Value	Name	Description	Project
0b	No Drift	Recovered clock does not drift from the received data	All
1b	Drift	Recovered clock has drifted from the received data	All

4 — FDI_RX_Symbol_Error_Rate_above_10^-9

Project: All

See FDI_RXA description.

Value	Name	Description	Project
0b	Less than	The received symbol error rate is not greater than 10^-9	All
1b	Greater than	The received symbol error rate is greater than 10^-9	All

3 — Reserved

2 — FDI_RX_Pixel_FIFO_Overflow

Project: All

See FDI_RXA description.

Value	Name	Description	Project
0b	No Overflow	Pixel FIFO did not overflow	All
1b	Overflow	Pixel FIFO overflowed	All

1 — FDI_RX_Cross_Clock_FIFO_Overflow

Project: All

See FDI_RXA description

Value	Name	Description	Project
0b	No Overflow	Cross Clock FIFO did not overflow	All
1b	Overflow	Cross Clock FIFO overflowed	All

FDI_RXB_ISR — FDI B Rx Interrupt Status Register	
0	**FDI_RX_Symbol_Queue_overflow** Project: All See FDI_RXA description. **Value Name / Description / Project** 0b — No Overflow — Symbol Queue did not overflow — All 1b — Overflow — Symbol Queue overflowed — All

4.1.4.2 FDI_RXB_IMR — FDI B Rx Interrupt Mask Register

FDI_RXB_IMR — FDI B Rx Interrupt Mask Register	
Register Type:	MMIO
Address Offset:	F1018h
Project:	All
Default Value:	000007FFh
Access:	R/W
Size (in bits):	32
See FDI_RXA description.	
Bit Description	
31:11	**Reserved** Project: All Format: MBZ
10:0	**Interrupt_Mask_Bits** Project: All Format: Interrupt Control Registers See FDI_RXA description. **Value Name / Description / Project** 0b — Not Masked — Not Masked – will be reported on the combined FDI_RXB interrupt in the SDEISR. — All 1b — Masked — Masked – will not be reported — All

4.1.4.3 FDI_RXB_CTL- FDI B Rx Control Register

FDI_RXB_CTL- FDI B Rx Control Register	
Register Type:	MMIO
Address Offset:	F100Ch
Project:	All
Default Value:	00000040h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Depends on bit

Bit De	scription
31	**FDI_Rx_B_Enable** Project: All Default Value: 0b See FDI_RXA description. **Value Na / me / Description / Project** 0b / Disable / Disables and tristates the FDI Rx A interface / All 1b / Enable / Enable. This bit enables the FDI Rx A interface. / All
30	**Reserved** Project: All Format: MBZ
29:28	**Link_training_pattern_enable** Project: All Default Value: 0b See FDI_RXA description. **Value Na / me / Description / Project** 00b / Pattern 1 / Pattern 1 enabled: Repetition of D10.2 characters. / All 01b / Pattern 2 / Pattern 2 enabled: Repetition of K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2. / All 10b / Idle / Idle Pattern enabled: Transmit single-context scheduling followed by VB-ID with NoVideoStream_flag set to 1, five times / All 11b / Normal / Link not in training: Send normal pixels / All
27:22	**Reserved** Project: All Format:

FDI_RXB_CTL- FDI B Rx Control Register

21:19 Port_Width_Selection

Project: All
Default Value: 0b
See FDI_RXA description.

Value Name	Description	Project
000b	x1 Mode	All
001b	x2 Mode	All
010b	x3 Mode	All
011b	x4 Mode	All
111b	x8 Mode	All
others	Reserved	All

18:16 Bits_Per_Color

Project: All
Default Value: 0b
See FDI_RXA description.

Value Name	Description	Project
000b	8 bits per color	All
001b	10 bits per color	All
010b	6 bits per color	All
011b	12 bits per color	All
1XXb	Reserved	All

15 Reserved Project: All Format: MBZ

14 DMI_Link_reversal_status

Project: All
Access: Read Only
Default Value: 0b
See FDI_RXA description.

Value Name	Description	Project
0b	Not Reversed	Link not reversed	All
1b	Reversed	Link reversed.	All

13 FDI_PLL_enable Project: All Format: Enable
See FDI_RXA description.

12:9 Reserved Project: All Format:

8 Reserved

7 Reserved Project: All

FDI_RXB_CTL- FDI B Rx Control Register	
6	**Reserved** Project: All
5	**Reserved**
4	**Rawclk_to_PCDCLK_selection** Project: All Default Value: 0b See FDI_RXA description. **Value Name** / **Description** / **Project**: 0b Rawclk — Rawclk used — All 1b PCDCLK — PCDCLK used — All
3:0	**Reserved** Project: All Format: MBZ

4.1.4.4 FDI_RXB_MISC— FDI B Rx Miscellaneous

FDI_RXB_MISC— FDI B Rx Miscellaneous	
Register Type:	MMIO
Address Offset:	F1010h
Project:	All
Default Value:	00000080h
Access:	R/W
Size (in bits):	32
Bit De	**scription**
31:13	**Reserved** Project: All Format: MBZ
12:0	**FDI_Delay** Project: All Default Value: 80h See FDI_RXA description.

4.2 HD Audio Registers (E2000h–E2FFFh)

These registers are memory mapped and accessible through normal 32 bit, 16 bit, or 8 bit accesses.

4.2.1 Audio Configuration

The video driver configures the audio operation through the following procedure.

1. Read the Capabilities Written bit in the Audio Configuration register at address offset 0xE2000. If this bit is a 1, the video driver does not need to write the audio configuration. If this bit is a 0, continue this procedure to write the audio configuration.
2. Read the EDID and directly write the EDID data into the audio EDID register region at address offset 0xE2080
3. Parse the EDID information to determine the monitor's audio capabilities. Then configure the hardware for those capabilities by setting the capability registers.
   - Write the audio capabilities to the Audio PCM Sizes and Rates register at address offset 0xE2044
   - Write the compressed audio supported formats to the Audio Stream Formats register at address offset 0xE2048
   - Set the presence detect bit to 1 in the Audio Pin Sense register at address offset 0xE2074
4. Set the Capabilities Written bit in the Audio Configuration register to 1. This indicates that the hardware can begin processing audio data using the current settings.

4.2.2 AUD_CONFIG_A—Audio Configuration – Transcoder A

AUD_CONFIG_A—Audio Configuration – Transcoder A				
Register Type:	MMIO			
Address Offset:	E2000h			
Project:	All			
Default Value:	00000000h			
Access:	R/W			
Size (in bits):	32			
This register configures the audio output.				
Bit De	**scription**			
31:30	**Reserved**	Project:	All	Format:

AUD_CONFIG_A—Audio Configuration – Transcoder A

29 **N_value_Index**

Project: All

Default Value: 0b

Value Na	me	Description	Project
0b	HDMI	N value read on bits 27:20 and 15:4 reflects HDMI N value. Bits 27:20 and 15:4 are is programmable to any N value - default h7FA6.	All
1b	DP	N value read on bits 27:20 and 15:4 reflects DP N value. Set this bit to 1 before programming N value register. When this is set to 1, 27:20 and 15:4 will reflect the current N value – default h8000.	All

28 **N_programming_enable** Project: All Security: Test

This bit enables programming of N values for non-CEA modes. Please note that the Transcoder to which audio is attached must be disabled when changing this field.

27:20 **Upper_N_value** Project: All Security: Test

These are bits [19:12] of programmable N values for non-CEA modes. Bit 25 of this register must also be written in order to enable programming. Please note that the Transcoder to which audio is attached must be disabled when changing this field.

This register can also be used to program N value for DP for a specific Port. Default value on this register when bit 29 is set to 1 is h7FA6

19:16 **Pixel_Clock(HDMI)**

Project: All

Default Value: 0b

This is the target frequency of the CEA/HDMI video mdoe to which the audio stream is added. This value is used for generating N_CTS packets.

This refers to only HDMI Pixel clock and does not refer to DP Link clock. DP Link clock does not require this programming.

Note: The Transcoder on which audio is attached must be disabled when changing this field.

Value Na	me	Description	Project
0000b	25.2 / 1.001 MHz	25.2 / 1.001 MHz	All
0001b	25.2 MHz	25.2 MHz Program this value for pixel clocks not listed in this field	All
0010b	27 MHz	27 MHz	All
0011b	27 * 1.001 MHz	27 * 1.001 MHz	All
0100b	54 MHz	54 MHz	All
0101b	54 * 1.001 MHz	54 * 1.001 MHz	All
0110b	74.25 / 1.001 MHz	74.25 / 1.001 MHz	All
0111b	74.25 MHz	74.25 MHz	All
1000b	148.5 / 1.001 MHz	148.5 / 1.001 MHz	All
1001b	148.5 MHz	148.5 MHz	All
Others	Reserved	Reserved	All

AUD_CONFIG_A—Audio Configuration – Transcoder A	
15:4	**Lower_N_value** Project: All Security: Test These are bits [11:0] of programmable N values for non-CEA modes. Bit 25 of this register must also be written in order to enable programming. Please note that the Transcoder to which audio is attached must be disabled when changing this field. **This register can also be used to program N value for DP for a specific Port. Default value on this register when bit 29 is set to 1 is h7FA6**
3	**Disable_NCTS** Project: All Set this bit to disable N & CTS or M generation for CTM modes. This is to enable prediction of CRC in CTM modes.
2:0	**Reserved** Project: All Format:

4.2.3 AUD_CONFIG_B—Audio Configuration – Transcoder B

AUD_CONFIG_B—Audio Configuration – Transcoder B

Register Type: MMIO
Address Offset: E2100h
Project: All
Default Value: 00000000h
Access: R/W
Size (in bits): 32

This register configures the audio output.

Bit De	scription
31:30	**Reserved** Project: All Format:
29	**N_value_Index** Project: All Default Value: 0b

Value Na	me	Description	Project
0b	HDMI	N value read on bits 27:20 and 15:4 reflects HDMI N value. Bits 27:20 and 15:4 are is programmable to any N value - default h7FA6.	All
1b	DP	N value read on bits 27:20 and 15:4 reflects DP N value. Set this bit to 1 before programming N value register. When this is set to 1, 27:20 and 15:4 will reflect the current N value – default h8000.	All

28	**N_programming_enable** Project: All Security: Test See Transcoder A description.
27:20	**Upper_N_value** Project: All Security: Test See Transcoder A description

AUD_CONFIG_B—Audio Configuration – Transcoder B

19:16

Pixel_Clock(HDMI)

Project: All

Default Value: 0b

See Transcoder A description.

Value Na	me	Description	Project
0000b	25.2 / 1.001 MHz	25.2 / 1.001 MHz	All
0001b	25.2 MHz	25.2 MHz Program this value for pixel clocks not listed in this field	All
0010b	27 MHz	27 MHz	All
0011b	27 * 1.001 MHz	27 * 1.001 MHz	All
0100b	54 MHz	54 MHz	All
0101b	54 * 1.001 MHz	54 * 1.001 MHz	All
0110b	74.25 / 1.001 MHz	74.25 / 1.001 MHz	All
0111b	74.25 MHz	74.25 MHz	All
1000b	148.5 / 1.001 MHz	148.5 / 1.001 MHz	All
1001b	148.5 MHz	148.5 MHz	All
others	Reserved	Reserved	All

15:4

Lower_N_value Project: All Security: Test

See Transcoder A description

3

Disable_NCTS Project: All

See Transcoder A description

2:0

Reserved Project: All Format:

4.2.4 AUD_MISC_CTRL_A—Audio MISC Control for Transcoder A

AUD_MISC_CTRL_A—Audio MISC Control for Transcoder A	
Register Type:	MMIO
Address Offset:	E2010h
Project:	All
Default Value:	00000040h
Access:	Read Only
Size (in bits):	32

Bit De	scription
31:8	**Reserved** Project: All Format: MBZ
8	**Sample_present_Disable** Project: All Security: Debug This bit is used to Disable sample present for HDMI or DP (Chicken Bit)
7:4	**Output_Delay** Project: All Default Value: 0100b The number of samples between when the sample is received from the HD Audio link and when it appears as an analog signal at the pin.
3	**Reserved** Project: All Format: MBZ
2	**Sample_Fabrication_EN_bit** Project: All Access: R/W Default Value: 0b This bit indicates whether internal fabrication of audio samples is enabled during a link underrun.

Value Na	me	Description	Project
0b	Disable	Audio fabrication disabled	All
1b	Enable	Audio fabrication enabled	All

AUD_MISC_CTRL_A—Audio MISC Control for Transcoder A	
1	**Pro_Allowed** Project: All Access: R/W Default Value: 0b By default, the audio device is configured to consumer mode and does not allow the mode to be changed to professional mode by an HD Audio verb. When Pro is allowed by setting this configuration bit, the HD Audio codec allows a verb to set the device into professional mode. Note: Setting this configuration bit does not change the default Pro bit value to be 1. Pro must be set to 1 through the normal process, using a verb.

Value Name	Description	Project
0b	Consumer	Consumer use only	All
1b	Professional	Professional use allowed	All

0	**Reserved** Project: All Format: MBZ

4.2.5 AUD_MISC_CTRL_B—Audio MISC Control for Transcoder B

AUD_MISC_CTRL_B—Audio MISC Control for Transcoder B	
Register Type:	MMIO
Address Offset:	E2110h
Project:	All
Default Value:	00000040h
Access:	Read Only
Size (in bits):	32

Bit Description	
31:8	**Reserved** Project: All Format: MBZ
8	**Sample_present_Disable** Project: All Security: Debug See Transcoder A description
7:4	**Output_Delay** Project: All Default Value: 0100b See Transcoder A description.
3	**Reserved** Project: All Format: MBZ

AUD_MISC_CTRL_B—Audio MISC Control for Transcoder B

2 — **Sample_Fabrication_EN_bit**

Project: All
Access: R/W
Default Value: 0b
See Transcoder A description.

Value Na	me	Description	Project
0b	Disable	Audio fabrication disabled	All
1b	Enable	Audio fabrication enabled	All

1 — **Pro_Allowed**

Project: All
Access: R/W
Default Value: 0b
See Transcoder A description.

Value Na	me	Description	Project
0b	Consumer	Consumer use only	All
1b	Professional	Professional use allowed	All

0 — **Reserved** Project: All Format: MBZ

4.2.6 AUD_VID_DID—Audio Vendor ID / Device ID

AUD_VID_DID—Audio Vendor ID / Device ID	
Register Type:	MMIO
Address Offset:	E2020h
Project:	All
Default Value:	80862804h
Access:	Read Only
Size (in bits):	32
These values are returned from the device as the Vendor ID/ Device ID response to a Get Root Node command.	
Bit De	**scription**
31:16	**Vendor_ID** Project: All Format: U16 Used to identify the codec within the PnP system. This field is hardwired within the device. Value = 0x8086
15:0	**Device_ID** Project: All Format: U16 Constant used to identify the codec within the PnP system. This field is set by the device hardware. Value = 0x2804 [Ibexpeak]

4.2.7 AUD_RID—Audio Revision ID

AUD_RID—Audio Revision ID	
Register Type:	MMIO
Address Offset:	E2024h
Project:	All
Default Value:	00100000h
Access:	Read Only
Size (in bits):	32
These values are returned from the device as the Revision ID response to a Get Root Node command.	
Bit De	**scription**
31:24	**Reserved** Project: All Format:
23:20	**Major_Revision** Project: All Default Value: 0001b The major revision number (left of the decimal) of the HD Audio Spec to which the codec is fully compliant. This field is hardwired within the device. Value = 0x1

AUD_RID—Audio Revision ID	
19:16	**Minor_Revision** Project: All The minor revision number (rights of the decimal) or “dot number” of the HD Audio Spec to which the codec is fully compliant. This field is hardwired within the device. Value = 0x0
15:8	**Revision_ID** Project: All The vendor’s revision number for this given Device ID. This field is hardwired within the device. Value = 0x0
7:0	**Stepping_ID** Project: All An optional vendor stepping number within the given Revision ID. This field is hardwired within the device. Value = 0x0

4.2.8 AUD_ PWRST—Audio Power State (Function Group, Convertor, Pin Widget)

Audio Power State Format				
Project:	All			
Bit De	**scription**			
1:0	**Power_State** Project: All Default Value: 11b D3			
	Value Na	**me**	**Description**	**Project**
	00b	D0	D0	All
	01b,10b	Unsupported	Unsupported	All
	11b	D3	D3	All

AUD_PWRST—Audio Power State (Function Group, Convertor, Pin Widget)					
Register Type:	MMIO				
Address Offset:	E204Ch				
Project:	All				
Default Value:	00FFFFFFh				
Access:	Read Only				
Size (in bits):	32				
These values are returned from the device as the Power State response to a Get Audio Function Group command.					
Bit De	**scription**				
31:24	**Reserved**	Project:	All	Format:	
23:22	**Function_Group_Device_Power_State_Current** Current power state	Project:	All	Format:	Audio Power State Format
21:20	**Function_Group_Device_Power_State_Set** Power state that was set	Project:	All	Format:	Audio Power State Format
19:18	**ConvertorB_Widget_Power_State_Current** Current power state	Project:	All	Format:	Audio Power State Format
17:16	**ConvertorB_Widget_Power_State_Requested** Power state that was requested by audio software	Project:	All	Format:	Audio Power State Format

AUD_PWRST—Audio Power State (Function Group, Convertor, Pin Widget)						
15:14	**ConvertorA_Widget_Power_State_Current** Current power state	Project:	All	Format:	Audio Power State Format	
13:12	**ConvertorA_Widget_Power_State_Requsted** Power state that was requested by audio software	Project:	All	Format:	Audio Power State Format	
11:10	**PinD_Widget_Power_State_Current** Current power state	Project:	All	Format:	Audio Power State Format	
9:8	**PinD_Widget_Power_State_Set** Power state that was set	Project:	All	Format:	Audio Power State Format	
7:6	**PinC_Widget_Power_State_Current** Current power state	Project:	All	Format:	Audio Power State Format	
5:4	**PinC_Widget_Power_State_Set** Power state that was set	Project:	All	Format:	Audio Power State Format	
3:2	**PinB_Widget_Power_State_Current** Current power state	Project:	All	Format:	Audio Power State	
1:0	**PinB_Widget_Power_State_Set** Power state that was set	Project:	All	Format:	Audio Power State Format	

4.2.9 AUD_PORT_EN_HD_CFG — Audio Port Enable HDAudio Config

AUD_PORT_EN_HD_CFG — Audio Port Enable HDAudio Config

Register Type: MMIO
Address Offset: E207Ch
Project: All
Security: Debug
Default Value: 00077003h
Access: Read Only
Size (in bits): 32

These values are returned from the device as the Digital Converter response to a Get Audio Output Converter Widget command.

Bit De	scription
31:19	**Reserved** Project: All Format:
18	**Port_D_Amp_Mute_Status** Project: All Default Value: 1b Amp muted This read-only bit reflects the mute status of the amplifier

Value Na	me	Description	Project
0b	Amp not muted	Amp not muted	All
1b	Amp muted	Amp muted	All

Bit De	scription
17	**Port_C_Amp_Mute_Status** Project: All Default Value: 1b Amp muted This read-only bit reflects the mute status of the amplifier

Value Na	me	Description	Project
0b	Amp not muted	Amp not muted	All
1b	Amp muted	Amp muted	All

Bit De	scription
16	**Port_B_Amp_Mute_Status** Project: All Default Value: 1b Amp muted This read-only bit reflects the mute status of the amplifier

Value Na	me	Description	Project
0b	Amp not muted	Amp not muted	All
1b	Amp muted	Amp muted	All

Bit De	scription
15	**Reserved** Project: All Format:

AUD_PORT_EN_HD_CFG — Audio Port Enable HDAudio Config

14 **Port_D_Out_Enable**

Project: All

Default Value: 1b Audio is Enabled

This bit reflects the state of the output path of the Pin Widget.

Value Na	me	Description	Project
0b	Disable	Audio is Disabled	All
1b	Enable	Audio is Enabled	All

13 **Port_C_Out_Enable**

Project: All

Default Value: 1b Audio is Enabled

This bit reflects the state of the output path of the Pin Widget.

Value Na	me	Description	Project
0b	Disable	Audio is Disabled	All
1b	Enable	Audio is Enabled	All

12 **Port_B_Out_Enable**

Project: All

Default Value: 1b Audio is Enabled

This bit reflects the state of the output path of the Pin Widget.

Value Na	me	Description	Project
0b	Disable	Audio is Disabled	All
1b	Enable	Audio is Enabled	All

11:8 **ConvertorB_Stream_ID** Project: All Format:

Represents the link stream used by the converter for data input or output. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default = 0 (stream 0)

7:4 **ConvertorA_Stream_ID** Project: All Format:

Represents the link stream used by the converter for data input or output. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default = 0 (stream 0)

3:2 **Reserved** Project: All Format:

AUD_PORT_EN_HD_CFG — Audio Port Enable HDAudio Config	
1	**Convertor_B_Digen** Project: All Default Value: 1b Digital Transmission Enabled Enables digital transmission through this node. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command.

Value Name	Description	Project
0b	Block	Digital data is blocked from passing through the node, regardless of the state	All
1b	Pass	Digital data can pass through the node (Default)	All

0	**Convertor_A_Digen** Project: All Default Value: 1b Digital Transmission Enabled Enables digital transmission through this node. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command.

Value Name	Description	Project
0b	Block	Digital data is blocked from passing through the node, regardless of the state	All
1b	Pass	Digital data can pass through the node (Default)	All

4.2.10 AUD_ OUT_DIG_CNVT_A—Audio Digital Converter – Conv A

AUD_OUT_DIG_CNVT_A—Audio Digital Converter – Conv A	
Register Type:	MMIO
Address Offset:	E2080h
Project:	All
Security:	Debug
Default Value:	00000001h
Access:	Read Only
Size (in bits):	32

These values are returned from the device as the Digital Converter response to a Get Audio Output Converter Widget command.

Bit	Description
31:24	**Reserved** Project: All Format:
23:20	**Stream_ID** Project: All Format: Represents the link stream used by the converter for data input or output. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default = 0 (stream 0)

AUD_OUT_DIG_CNVT_A—Audio Digital Converter – Conv A

19:16	**Lowest_Channel_Number** Project: All Format: Represents the lowest channel used by the converter. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default = 0
15	**Reserved** Project: All Format:
14:8	**Category_Code** Project: All Format: S/PDIF IEC Category Code. This value is set in the Digital Converter 1 through the Set Audio Output Converter Widget command. Default = 0
7	**Level** Project: All Format: S/PDIF IEC Generation Level. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0
6	**PRO** Project: All Default Value: 0b This bit indicates professional or consumer use of channel. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. **This value can only be set to 1 if the Pro Allowed bit is set in the audio configuration register.**

Value Na	me	Description	Project
0b	Consumer	Consumer use	All
1b	Professional	Professional use	All

5	**Non-Audio** Project: All Default Value: 0b Data is non PCM format. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command.

Value Na	me	Description	Project
0b	PCM	Data is PCM	All
1b	Non PCM	Data is non PCM format	All

4	**Copy** Project: All Default Value: 0b Copyright asserted. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command.

Value Na	me	Description	Project
0b	Not Asserted	Copyright is not asserted	All
1b	Asserted	Copyright is asserted	All

AUD_OUT_DIG_CNVT_A—Audio Digital Converter – Conv A	
3	**PRE** Project: All Default Value: 0b Filter preemphasis. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. **Value Name / Description / Project** 0b – Disabled – Preemphasis is disabled – All 1b – Enabled – Filter preemphasis is enabled – All
2	**VCFG** Project: All Format: Validity Configuration. Determines S/PDIF transmitter behavior when data is not being transmitted. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0
1	**V** Project: All Format: Affects the validity flag transmitted in each subframe, and enables the S/PDIF transmitter to maintain connection during error or mute conditions. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0
0	**Reserved** Project: All Format: MBZ

4.2.11 AUD_ OUT_DIG_CNVT_B—Audio Digital Converter – Conv

AUD_OUT_DIG_CNVT_B—Audio Digital Converter – Conv B	
Register Type: MMIO **Address Offset:** E2180h **Project:** All **Security:** Debug **Default Value:** 00000001h **Access:** Read Only **Size (in bits):** 32	
These values are returned from the device as the Digital Converter response to a Get Audio Output Converter Widget command.	
Bit De	**scription**
31:24	**Reserved** Project: All Format:
23:20	**Stream_ID** Project: All Format: See Conv A description.
19:16	**Lowest_Channel_Number** Project: All Format: See Conv A description
15	**Reserved** Project: All Format:
14:8	**Category_Code** Project: All Format: See Conv A description
7	**Level** Project: All Format: See Conv A description

AUD_OUT_DIG_CNVT_B—Audio Digital Converter – Conv B

6 — PRO

Project: All
Default Value: 0b
See Conv A description

Value Na	me	Description	Project
0b	Consumer	Consumer use	All
1b	Professional	Professional use	All

5 — Non-Audio

Project: All
Default Value: 0b
See Conv A description.

Value Na	me	Description	Project
0b	PCM	Data is PCM	All
1b	Non PCM	Data is non PCM format	All

4 — Copy

Project: All
Default Value: 0b
See Conv A description

Value Na	me	Description	Project
0b	Not Asserted	Copyright is not asserted	All
1b	Asserted	Copyright is asserted	All

3 — PRE

Project: All
Default Value: 0b
See Conv A description

Value Na	me	Description	Project
0b	Disabled	Preemphasis is disabled	All
1b	Enabled	Filter preemphasis is enabled	All

2 — VCFG Project: All Format:
See Conv A description

1 — V Project: All Format:
See Conv A description

0 — Reserved Project: All Format: MBZ

4.2.12 AUD_OUT_CH_STR—Audio Channel ID and Stream ID

AUD_OUT_CH_STR—Audio Channel ID and Stream ID	
Register Type:	MMIO
Address Offset:	E2088h
Project:	All
Security:	Debug
Default Value:	00000000h
Access:	Read Only
Size (in bits):	32

These values are returned from the device as the Channel ID and Stream ID response to a Get Audio Output Converter Widget command.

Bit De	scription
31:24	**Reserved** Project: All Format:
23:20	**Converter_Channel_MAP_PORTD** Project: All The number in this field reflects the HD audio channel to which the Digital Display Audio channel in bits 19:16 is mapped. This field is read only
19:16	**Digital_Display_Audio_Index_PORTD** Project: All This field is the Digital Display Audio channel number. When these bits are written, the audio channel number assigned to the Digital Display Audio channel number are reflected in bits 20:23 of this register.
15:12	**Converter_Channel_MAP_PORTC** Project: All The number in this field reflects the HD audio channel to which the Digital Display Audio channel in bits 11:8 is mapped. This field is read only
11:8	**HDMI_Index_PORTC** Project: All This field is the Digital Display Audio channel number. When these bits are written, the audio channel number assigned to the Digital Display Audio channel number are reflected in bits 12:15 of this register.
7:4	**Converter_Channel_MAP_PORTB** Project: All The number in this field reflects the HD audio channel to which the Digital Display Audio channel in bits 3:0 is mapped. This field is read only
3:0	**HDMI_Index_PORTB** Project: All This field is the Digital Display Audio channel number. When these bits are written, the audio channel number assigned to the Digital Display Audio channel number are reflected in bits 4:7 of this register.

4.2.13 AUD_OUT_STR_DESC_A—Audio Stream Descriptor Format – Conv A

AUD_OUT_STR_DESC_A—Audio Stream Descriptor Format – Conv A			
Register Type:	MMIO		
Address Offset:	E2084h		
Project:	All		
Security:	Debug		
Default Value:	00000032h		
Access:	Read Only		
Size (in bits):	32		
These values are returned from the device as the Stream Descriptor Format response to a Get Audio Output Converter Widget command.			
Bit De	**scription**		
31:29	**Reserved**	Project: All	Format:
28:27	**HBR_enable** This reflects the current HBR settings.	Project: All	Format:
26:21	**Reserved**	Project: All	Format:
20:16	**Convertor_Channel_Count** This reflects the Convertor Channel Count programmed through HDAudio.	Project: All	Format:
15	**Reserved**	Project: All	Format:
14	**Sample_Base_Rate** Project: All Default Value: 0b 48 kHz Sampling base rate of audio stream. This bit is hardwired to 0.		

Value Na	me	Description	Project
0b	48 kHz	48 kHz	All
1b	44.1 kHz	44.1 kHz	All

AUD_OUT_STR_DESC_A—Audio Stream Descriptor Format – Conv A

13:11 **Sample_Base_Rate_Mult**

Project: All

Default Value: 000b 48 kHz

Audio stream sample base rate multiple. This field is hardwired to 000.

Value Na	me	Description	Project
000b	x1	x1 (48 kHz/44.1 kHz or less)	All
001b	x2	x2 (96 kHz, 88.2 kHz, 32 kHz)	All
010b	x3	x3 (144 kHz)	All
011b	x4	x4 (192 kHz, 176.4 kHz)	All
1XXb	Reserved	Reserved	All

10:8 **Sample_Base_Rate_Divisor**

Project: All

Default Value: 000b 48 kHz

Audio stream sample base rate divisor. This field is hardwired to 000.

Value Na	me	Description	Project
000b	Div 1	Divide by 1 (48 kHz, 44.1 kHz)	All
001b	Div 2	Divide by 2 (24 kHz, 22.05 kHz)	All
010b	Div 3	Divide by 3 (16 kHz, 32 kHz)	All
011b	Div 4	Divide by 4 (11.025 kHz)	All
100b	Div 5	Divide by 5 (9.6 kHz)	All
101b	Div 6	Divide by 6 (8 kHz)	All
110b	Div 7	Divide by 7	All
111b	Div 8	Divide by 8 (6 kHz)	All

7 **Reserved** Project: All Format: MBZ

AUD_OUT_STR_DESC_A—Audio Stream Descriptor Format – Conv A	
6:4	**Bits_per_Sample** Project: All Default Value: 011b 32 bits

Value Na	me	Description	Project
000b	8 bit	The data will be packed in memory in 8 bit containers on 16 bit boundaries	All
001b	16 bits	The data will be packed in memory in 16 bit containers on 16 bit boundaries	All
100b	20 bits	The data will be packed in memory in 20 bit containers on 32 bit boundaries	All
010b	24 bits	The data will be packed in memory in 32 bit containers on 32 bit boundaries	All
011b	32 bits	The data will be packed in memory in 32 bit containers on 32 bit boundaries	All
Others	Reserved	Reserved	All

3:0	**Number_of_Channels_in_a_Stream** Project: All Default Value: 0010b 3 channels in each frame Format: U4+1 Binary value plus 1. 0000 = 1, 1111= 16 Number of channels in each frame of the stream. This field is hardwired to 0010.

4.2.14 AUD_OUT_STR_DESC_B—Audio Stream Descriptor Format – Conv B

AUD_OUT_STR_DESC_B—Audio Stream Descriptor Format – Conv B	
Register Type:	MMIO
Address Offset:	E2184h
Project:	All
Security:	Debug
Default Value:	00000032h
Access:	Read Only
Size (in bits):	32
See Conv A description.	

Bit De	scription
31:29	**Reserved** Project: All Format:
28:27	**HBR_enable** Project: All Format: See Conv A description.

AUD_OUT_STR_DESC_B—Audio Stream Descriptor Format – Conv B

26:21	**Reserved** Project: All Format:
20:16	**Convertor_Channel_Count** Project: All Format: See Conv A description.
15	**Reserved** Project: All Format:
14	**Sample_Base_Rate** Project: All Default Value: 0b 48 kHz See Conv A description.

Value Na	me	Description	Project
0b	48 kHz	48 kHz	All
1b	44.1 kHz	44.1 kHz	All

13:11 **Sample_Base_Rate_Mult**
Project: All
Default Value: 000b 48 kHz
See Conv A description.

Value Na	me	Description	Project
000b	x1	x1 (48 kHz/44.1 kHz or less)	All
001b	x2	x2 (96 kHz, 88.2 kHz, 32 kHz)	All
010b	x3	x3 (144 kHz)	All
011b	x4	x4 (192 kHz, 176.4 kHz)	All
1XXb	Reserved	Reserved	All

10:8 **Sample_Base_Rate_Divisor**
Project: All
Default Value: 000b 48 kHz
See Conv A description.

Value Na	me	Description	Project
000b	Div 1	Divide by 1 (48 kHz, 44.1 kHz)	All
001b	Div 2	Divide by 2 (24 kHz, 22.05 kHz)	All
010b	Div 3	Divide by 3 (16 kHz, 32 kHz)	All
011b	Div 4	Divide by 4 (11.025 kHz)	All
100b	Div 5	Divide by 5 (9.6 kHz)	All
101b	Div 6	Divide by 6 (8 kHz)	All
110b	Div 7	Divide by 7	All
111b	Div 8	Divide by 8 (6 kHz)	All

AUD_OUT_STR_DESC_B—Audio Stream Descriptor Format – Conv B	
7	**Reserved** Project: All Format: MBZ
6:4	**Bits_per_Sample** Project: All Default Value: 011b 32 bits

Value Name		Description	Project
000b	8 bit	The data will be packed in memory in 8 bit containers on 16 bit boundaries	All
001b	16 bits	The data will be packed in memory in 16 bit containers on 16 bit boundaries	All
100b	20 bits	The data will be packed in memory in 20 bit containers on 32 bit boundaries	All
010b	24 bits	The data will be packed in memory in 24 bit containers on 32 bit boundaries	All
011b	32 bits	The data will be packed in memory in 32 bit containers on 32 bit boundaries	All
others	Res.	Reserved	All

3:0	**Number_of_Channels_in_a_Stream** Project: All Default Value: 0010b 3 channels in each frame Format: U4+1 Binary value plus 1. 0000 = 1, 1111= 16 See Conv A description.

4.2.14.1 AUD_PINW_CONNL NG_LIST—Audio Connection List

AUD_PINW_CONNLNG_LIST—Audio Connection List	
Register Type:	MMIO
Address Offset:	E20A8h
Project:	All
Default Value:	00000302h
Access:	Read Only
Size (in bits):	32
These values are returned from the device as the Connection List Length response to a Get Pin Widget command.	
Bit De	**scription**
31:16	**Reserved** Project: All Format:

AUD_PINW_CONNLNG_LIST—Audio Connection List	
15:8	**Connection_List_Entry** Project: All Default Value: 03h Connection to Convertor Widget Node 0x03
7	**Long_Form** Project: All Default Value: 0b This bit indicates whether the items in the connection list are ‘long form’ or ‘short form’. This bit is hardwired to 0 (items in connection list are short form)
6:0	**Connection_List_Length** Project: All Default Value: 02h This field indicates the number of items in the connection list. If this field is 2, there is only one hardwired input possible, which is read from the Connection List, and there is no Connection Select Control.

4.2.15 AUD_ PINW_CONNLNG_SEL—Audio Connection Select

AUD_PINW_CONNLNG_SEL—Audio Connection Select	
Register Type:	MMIO
Address Offset:	E20ACh
Project:	All
Default Value:	00000000h
Access:	Read Only
Size (in bits):	32
These values are returned from the device as the Connection List Length response to a Get Pin Widget command.	
Bit De	**scription**
31:24	**Reserved** Project: All Format:
23:16	**Connection_select_Control_D** Project: All Format: Connection Index Currently Set [Default 0x00], Port D Widget is set to 0x00
15:8	**Connection_select_Control_C** Project: All Format: Connection Index Currently Set [Default 0x00], Port C Widget is set to 0x00
7:0	**Connection_select_Control_B** Project: All Format: Connection Index Currently Set [Default 0x00], Port B Widget is set to 0x00

4.2.16 AUD_CNTL_ST_A—Audio Control State Register – Transcoder A

AUD_CNTL_ST_A—Audio Control State Register – Transcoder A					
Register Type:	MMIO				
Address Offset:	E20B4h				
Project:	All				
Default Value:	00005400h				
Access:	R/W				
Size (in bits):	32				
Bit De	**scription**				
31	**Reserved** Project: All Format: MBZ				
30:29	**DIP_Port_Select** Project: All Access: Read Only Default Value: 00b This read-only bit reflects which port is used to transmit the DIP data. This can only change when DIP is disabled. If one or more audio-related DIP packets is enabled and audio is enabled on a digital port, these bits will reflect the digital port to which audio is directed.				
	Value Na	**me**	**Description**		**Project**
	00b	Reserved	Reserved		All
	01b	Digital Port B	Digital Port B		All
	10b	Digital Port C	Digital Port C		All
	11b	Digital Port D	Digital Port D		All
28:25	**Reserved** Project: All Format: MBZ				

AUD_CNTL_ST_A—Audio Control State Register – Transcoder A

24:21

DIP_type_enable_status

Project: All

Access: Read Only

Default Value: 0000b

These bits reflect the DIP types enabled. It can be updated while the port is enabled. Within 2 vblank periods, the DIP is guaranteed to have been transmitted. Disabling a DIP type results in setting the contents of that DIP buffer to zero. A reserved setting reflects a disabled DIP.

Value Na	me	Description	Project
XXX0b	Disable	Audio DIP disabled	All
XXX1b	Enable	Audio DIP enabled	All
XX0Xb	Disable	Generic 1 (ACP) DIP disabled	All
XX1Xb	Enable	Generic 1 (ACP) DIP enabled	All
X0XXb	Disable	Generic 2 DIP disabled	All
X1XXb	Enable	Generic 2 DIP enabled, can be used by ISRC1 or ISRC2	All
1XXXb	Reserved	Reserved	All

20:18

DIP_buffer_index

Project: All

Default Value: 0000b

This field is used during read of different DIPs, and during read or write of ELD data. These bits are used as an index to their respective DIP or ELD buffers. When the index is not valid, the contents of the DIP will return all 0's.

Value Na	me	Description	Project
000b	Audio	Audio DIP (31 bytes of address space, 31 bytes of data)	All
001b	Gen 1	Generic 1 (ACP) Data Island Packet (31 bytes of address space, 31 bytes of data)	All
010b	Gen 2	Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data)	All
011b	Gen 3	Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data)	All
1XXb	Reserved	Reserved	All

AUD_CNTL_ST_A—Audio Control State Register – Transcoder A

17:16 DIP_transmission_frequency

Project: All

Access: Read Only

Default Value: 00b

These bits reflect the frequency of DIP transmission for the DIP buffer type designated in bits 20:18. When writing DIP data, this value is also latched when the first DW of the DIP is written.

When read, this value reflects the DIP transmission frequency for the DIP buffer designated in bits 20:18.

Value Na	me	Description	Project
00b	Disable	Disabled	All
01b	Reserved	Reserved	All
10b	Send Once	Send Once	All
11b	Best Effort	Best effort (Send at least every other vsync)	All

15 Reserved Project: All Format: MBZ

14:10 ELD_buffer_size Project: All Access: Read Only

10101 = This field reflects the size of the ELD buffer in DWORDs (84 Bytes of ELD)

9:5 ELD_access_address Project: All

Selects the DWORD address for access to the ELD buffer (84 bytes). The value wraps back to zero when incremented past the max addressing value 0x1F. This field change takes effect immediately after being written. The read value indicates the current access address.

4 ELD_ACK Project: All

Acknowledgement from the audio driver that ELD read has been completed

3:0 DIP_RAM_access_address Project: All

Selects the DWORD address for access to the DIP buffers. The value wraps back to zero when it incremented past the max addressing value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.

4.2.17 AUD_CNTL_ST_B—Audio Control State Register – Transcoder B

AUD_CNTL_ST_B—Audio Control State Register – Transcoder B

Register Type: MMIO
Address Offset: E21B4h
Project: All
Default Value: 00005400h
Access: R/W
Size (in bits): 32

Bit De	scription
31	**Reserved** Project: All Format: MBZ
30:29	**DIP_Port_Select** Project: All Access: Read Only Default Value: 00b See Transcoder A description.
28:25	**Reserved** Project: All Format: MBZ
24:21	**DIP_type_enable_status** Project: All Access: Read Only Default Value: 0000b See Transcoder A description.

Value Na	me	Description	Project
00b	Reserved	Reserved	All
01b	Digital Port B	Digital Port B	All
10b	Digital Port C	Digital Port C	All
11b	Digital Port D	Digital Port D	All

Value Na	me	Description	Project
XXX0b	Disable	Audio DIP disabled (Default)	All
XXX1b	Enable	Audio DIP enabled	All
XX0Xb	Disable	Generic 1 (ACP) DIP disabled	All
XX1Xb	Enable	Generic 1 (ACP) DIP enabled	All
X0XXb	Disable	Generic 2 DIP disabled	All
X1XXb	Enable	Generic 2 DIP enabled, can be used by ISRC1 or ISRC2	All
1XXXb	Reserved	Reserved	All

AUD_CNTL_ST_B—Audio Control State Register – Transcoder B

20:18 DIP_buffer_index

Project: All

Default Value: 000b

See Transcoder A description.

Value Na	me	Description	Project
000b	Audio	Audio DIP (31 bytes of address space, 31 bytes of data)	All
001b	Gen 1	Generic 1 (ACP) Data Island Packet (31 bytes of address space, 11 bytes of data)	All
010b	Gen 2	Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data)	All
011b	Gen 3	Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data)	All
1XXb	Reserved	Reserved	All

17:16 DIP_transmission_frequency

Project: All

Access: Read Only

Default Value: 00b

See Transcoder A description

Value Na	me	Description	Project
00b	Disable	Disabled	All
01b	Reserved	Reserved	All
10b	Send Once	Send Once	All
11b	Best Effort	Best effort (Send at least every other vsync)	All

15 Reserved Project: All Format: MBZ

14:10 ELD_buffer_size Project: All Access: Read Only

10101 = This field reflects the size of the ELD buffer in DWORDs (84 Bytes of ELD)

9:5 ELD_access_address Project: All

See Transcoder A description.

4 ELD_ACK Project: All

See Transcoder A description.

3:0 DIP_RAM_access_address Project: All

See Transcoder A description.

4.2.18 AUD_CNTL_ST2— Audio Control State 2

AUD_CNTL_ST2— Audio Control State 2

Register Type: MMIO
Address Offset: E20C0h
Project: All
Default Value: 00000000h
Access: R/W
Size (in bits): 32

This register is used for handshaking between the audio and video drivers for interrupt management. For each port, ELD readiness is sent by the display software to the audio software via an unsolicited response when the ELD or CP ready bit is set. Display software sets these bits as part of enabling the respective audio-enabled digital display port.

Bit De	scription
31:10	**Reserved** Project: All Format:
9	**CP_ReadyD** Project: All Default Value: 0b This **R/W** bit reflects the state of CP request from the audio unit. When an audio CP request has been serviced, it must be reset to 1 by the video software to indicate that the CP request has been serviced.
8	**ELD_validD** Project: All Default Value: 0b This **R/W** bit reflects the state of the ELD data written to the ELD RAM. After writing the ELD data, the video software must set this bit to 1 to indicate that the ELD data is valid. At audio codec initialization, or on a hotplug event, this bit is set to 0 by the video software. This bit is reflected in the audio pin complex widget as the ELD valid status bit.
7:6	**Reserved** Project: All Format:

Value Na me	Description	Project
0b	Pending or Not Ready	CP request pending or not ready to receive requests	All
1b	Ready	CP request ready	All

Value Na me	Description	Project
0b	Invalid	ELD data invalid (default, when writing ELD data, set 0 by software)	All
1b	Valid	ELD data valid (Set by video software only)	All

AUD_CNTL_ST2— Audio Control State 2

5 — **CP_ReadyC**

Project: All

Default Value: 0b

See CP_ReadyD description.

Value	Name	Description	Project
0b	Not Ready	CP request pending or not ready to receive requests	All
1b	Ready	CP request ready	All

4 — **ELD_validC**

Project: All

Default Value: 0b

See ELD_validD descripion.

Value	Name	Description	Project
0b	Invalid	ELD data invalid (default, when writing ELD data, set 0 by software)	All
1b	Valid	ELD data valid (Set by video software only)	All

3:2 — **Reserved** Project: All Format:

1 — **CP_ReadyB**

Project: All

Default Value: 0b

See CP_ReadyD description.

Value	Name	Description	Project
0b	Not Ready	CP request pending or not ready to receive requests	All
1b	Ready	CP request ready	All

0 — **ELD_validB**

Project: All

Default Value: 0b

See ELD_validD descripion.

Value	Name	Description	Project
0b	Invalid	ELD data invalid (default, when writing ELD data, set 0 by software)	All
1b	Valid	ELD data valid (Set by video software only)	All

4.2.19 AUD_HDMIW_STATUS—Audio HDMI Status

AUD_HDMIW_STATUS—Audio HDMI Status	
Register Type:	MMIO
Address Offset:	E20D4h
Project:	All
Security:	Debug
Default Value:	00000000h
Access:	R/W Clear
Size (in bits):	32

Bit De	scription
31	**Conv_B_CDCLK/DOTCLK_FIFO_Underrun** Project: All This bit indicates an underrun in the FIFO inside the clock crossing logic between CDCLK and DOTCLK. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.
30	**Conv_B_CDCLK/DOTCLK_FIFO_Overrun** Project: All This bit indicates an overrun in the FIFO inside the clock crossing logic between CDCLK and DOTCLK. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.
29	**Conv_A_CDCLK/DOTCLK_FIFO_Underrun** Project: All This bit indicates an underrun in the FIFO inside the clock crossing logic between CDCLK and DOTCLK. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.
28	**Conv_A_CDCLK/DOTCLK_FIFO_Overrun** Project: All This bit indicates an overrun in the FIFO inside the clock crossing logic between CDCLK and DOTCLK. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.
27:26	**Reserved** Project: All Format:
25	**BCLK/CDCLK_FIFO_Overrun** Project: All This bit indicates an overrun in the FIFO inside the clock crossing logic between BCLK and CDCLK. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.
24	**Function_Reset** Project: All Security: Debug This bit indicates that an audio function reset occurred through the reset signal on the HD audio bus. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.
23:0	**Reserved** Project: All Format:

4.2.20 AUD_HDMIW_HDMIEDID_A—HDMI Data EDID Block – Transcoder A

AUD_HDMIW_HDMIEDID_A—HDMI Data EDID Block – Transcoder A	
Register Type:	MMIO
Address Offset:	E2050h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

These registers contain the HDMI data block from the EDID. The graphics driver reads the EDID and writes the structure to these registers. The vendor specific data block may be longer than 8 bytes, but the driver must not write more than 48 bytes to the buffer. The EDID format is Version 3 within the CEA-861B specification. The HDMI Vendor Specific Data Block is described in version 1.1 of the HDMI specification. These values are returned from the device as the HDMI Vendor Specific Data Block response to a Get HDMI Widget command.

Writing sequence:

- Video software sets ELD invalid, and sets the ELD access address to 0, or to the desired DWORD to be written.
- Video software writes ELD data 1 DWORD at a time. The ELD access address autoincrements with each DWORD write, wrapping around to address 0 when the max buffer address size of 0xF has been reached. Please note that software must write an entire DWORD at a time.
- Please note that the audio driver checks the valid bit with each byte read of the ELD. This means that the video driver can unilaterally write ELD irrespective of audio driver ELD read status.

Reading sequence:

- Video software sets the ELD access address to 0, or to the desired DWORD to be read.
- Video software reads ELD data 1 DWORD at a time. The ELD access address autoincrements with each DWORD read, wrapping around to address 0 when the max buffer address size of 0xF has been reached.

Bit De	scription
31:0	**EDID_HDMI_Data_Block** Project: All Format: Please note that the contents of this buffer are not cleared when ELD is disabled. The contents of this buffer are cleared during gfx reset

4.2.21 AUD_HDMIW_HDMIEDID_B—HDMI Data EDID Block – Transcoder B

AUD_HDMIW_HDMIEDID_B—HDMI Data EDID Block – Transcoder B					
Register Type: MMIO **Address Offset:** E2150h **Project:** All **Default Value:** 00000000h **Access:** R/W **Size (in bits):** 32					
See Transcoder A description.					
Bit De	**scription**				
31:0	**EDID_HDMI_Data_Block** See Transcoder A description	Project:	All	Format:	

4.2.22 AUD_ HDMIW_INFOFR_A—Audio Widget Data Island Packet – Transcoder A

AUD_HDMIW_INFOFR_A—Audio Widget Data Island Packet – Transcoder A	
Register Type:	MMIO
Address Offset:	E2054h
Project:	All
Default Value:	00000000h
Access:	Read Only
Size (in bits):	32

When the IF type or dword index is not valid, the contents of the DIP will return all 0's.
These values are programmed by the audio driver in an HDMI Widget Set command. They are returned one byte at a time from the device on the HD audio bus as the HDMI DIP response to a Get HDMI Widget command. To fetch a specific byte, the audio driver should send an HDMI Widget HDMI DIP Index Pointer Set command to set the index, then fetch the indexed byte using the HDMI DIP get.
Video driver read sequence (for debug only):
Video software sets DIP type to the appropriate DIP, and sets the DIP access address to the desired DWORD.
Video software reads DIP data 1 DWORD at a time. The DIP access address auto increments with each DWORD write, wrapping around to address 0 when the max buffer address size of 0xF has been reached.

Bit De	scription
31:0	**Data_Island_Packet_Data** Project: All Format: This reflects the contents of the DIP indexed by the DIP access address. The contents of this buffer are cleared during function reset or HD audio link reset.

4.2.23 AUD_ HDMIW_INFOFR_B—Audio Widget Data Island Packet – Transcoder B

AUD_HDMIW_INFOFR_B—Audio Widget Data Island Packet – Transcoder B	
Register Type:	MMIO
Address Offset:	E2154h
Project:	All
Default Value:	00000000h
Access:	Read Only
Size (in bits):	32

See Transcoder A description.

Bit De	scription
31:0	**Data_Island_Packet_Data** Project: All Format: See Transcoder A description.

4.3 DPB Control and Aux Channel

4.3.1 DPB—DisplayPort B Control Register

DPB—DisplayPort B Control Register	
Register Type:	MMIO
Address Offset:	E4100h
Project:	All
Default Value:	00000018h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Depends on bit

Please note that DisplayPort B uses the same lanes as HDMIB. Therefore +B/HDMIB and DisplayPort B cannot be enabled simultaneously.

Bit De	scription
31	**DisplayPort_B_Enable** Project: All Default Value: 0b Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written. [DevIBX] When disabling the port, software must temporarily enable the port with transcoder select (bit #30) cleared to '0' after disabling the port. This is workaround for hardware issue where the transcoder select set to '1' will prevent HDMIB from being enabled on transcoder A.

Value Na	me	Description	Project
0b	Disable	Disable and tristates the Display Port B interface	All
1b	Enable	Enable. This bit enables the Display Port B interface	All

DPB—DisplayPort B Control Register

30

Transcoder_Select

Project: All

Default Value: 0b

This bit determines from which display transcoder the source data will originate. Transcoder selection takes place on the Vblank after being written

[DevIBX] Writing to this bit only takes effect when port is enabled. Due to hardware issue it is required that this bit be cleared when port is disabled. To clear this bit software must temporarily enable this port on transcoder A.

Value Na	me	Description	Project
0b	Transcoder A	Transcoder A	All
1b	Transcoder B	Transcoder B	All

29:28

Link_training_pattern_enable

Project: All

Default Value: 0b

These bits are used for link initialization as defined in the DisplayPort specification. Please note that the link must first be configured prior to sending training patterns.

When enabling the port, it must be turned on with pattern 1 enabled. When retraining a link, the port must be disabled, then re-enabled with pattern 1 enabled.

Value Na	me	Description	Project
00b	Pattern 1	Pattern 1 enabled: Repetition of D10.2 characters	All
01b	Pattern 2	Pattern 2 enabled: Repetition of K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2.	All
10b	Idle	Idle Pattern enabled: Transmit BS followed by VB-ID with NoVideoStream_flag set to 1, five times	All
11b	Normal	Link not in training: Send normal pixels	All

DPB—DisplayPort B Control Register

27:25 **Voltage_swing_level_set**

Project: All

Default Value: 0b

These bits are used for setting the voltage swing for pattern 1, defined as Vdiff_pp in the DisplayPort specification. They mirror registers in the PCI express configuration.

Value Name	Description	Project
000b	0.4V	0.4 V	All
001b	0.6V	0.6 V	All
010b	0.8V	0.8 V	All
011b	1.2V	1.2 V	All
1XXb	Reserved	Reserved	All

24:22 **Pre-emphasis_level_set**

Project: All

Default Value: 0b

These bits are used for setting link pre-emphasis for pattern 2, as defined in the DisplayPort specification. They mirror registers in the PCI express configuration.

Value Name	Description	Project
000b	None	**No pre-emphasis**	All
001b	3.5dB	3.5dB pre-emphasis (1.5x)	All
010b	6 dB	6dB pre-emphasis (2x)	All
011b	9.5 dB	9.5dB pre-emphasis (3x)	All
1XXb	Reserved	Reserved	All

21:19 **Port_Width_Selection**

Project: All

Default Value: 0b

This bit selects the number of lanes to be enabled on the DisplayPort link. Port width change must be done as a part of mode set. **Locked once port is enabled. Updates when the port is disabled then re-enabled**

Value Name	Description	Project
000b	x1	x1 Mode	All
001b	x2	x2 Mode	All
011b	x4	x4 Mode	All
Others	Reserved	Reserved	All

DPB—DisplayPort B Control Register

18 — Enhanced_Framing_Enable

Project: All

Default Value: 0b

This bit selects enhanced framing. **Locked once port is enabled. Updates when the port is disabled then re-enabled**

Value Na	me	Description	Project
0b	Disable	Enhanced framing disabled	All
1b	Enable	Enhanced framing enabled	All

17:16 — Reserved Project: All Format: MBZ

15 — Port_reversal

Project: All

Default Value: 0b

Enables lane reversal within the port: lane 0 mapped to lane 3, lane 1 mapped to lane 2, etc. Port reversal is not controlled by a strap. **Locked once port is enabled. Updates when the port is disabled then re-enabled**

Value Na	me	Description	Project
0b	Not Reversed	Port not reversed	All
1b	Reversed	Port reversed	All

14:8 — Reserved Project: All Format: MBZ

7 — Scrambling Disable

Project: All

Security: Debug

Default Value: 0b

This bit disables scrambling for DisplayPort

Value Na	me	Description	Project
0b	Enable	Scrambling enabled	All
1b	Disable	Scrambling disabled	All

6 — Audio_Output_Enable

Project: All

Default Value: 0b

This bit enables audio on this output port. It may be enabled or disabled only when the link training is complete and set to “Normal.”

Value Na	me	Description	Project
0b	Disable	Audio output disabled	All
1b	Enable	Audio output enabled	All

DPB—DisplayPort B Control Register

5 Reserved

4:3 **Sync_Polarity**

Project: All

Default Value: 11b VS and HS are active high

Indicates the polarity of Hsync and Vsync to be transmitted in MSA

Value Name	Description	Project
00b	Low	VS and HS are active low (inverted)	All
11b	VS Low, HS High	VS is active low (inverted), HS is active high	All
11b	VS High, HS Low	VS is active high, HS is active low (inverted)	All
11b	High	VS and HS are active high	All

2 **Digital_Display_B_Detected**

Project: All

Access: Read Only

Default Value: 0b

Read-only bit indicating whether a digital display was detected during initialization. It signifies the level of the GMBUS port 4 (port B) data line at boot.

Value Name	Description	Project
0b	Not Detected	Digital display not detected during initialization	All
1b	Detected	Digital display detected during initialization	All

1:0 **Reserved** Project: All Format: MBZ

4.3.2 DPB_AUX_CH_ CTL—Display Port B AUX Channel Control

DPB_AUX_CH_CTL—Display Port B AUX Channel Control

Register Type: MMIO
Address Offset: E4110h
Project: All
Default Value: 00050000h
Access: R/W
Size (in bits): 32

Bit De	scription
31	**Send/Busy** Project: All Default Value: 0b Setting this bit to a one initiates the transaction, when read this bit will be a 1 until the transmission completes. The transaction is completed when the response is received or when a timeout occurs. Do not write a 1 again until transaction completes. Writes of 0 will be ignored. **Programming Notes** Do not change any fields while Busy bit 31 is asserted.
30	**Done** Project: All Access: R/W Clear A sticky bit that indicates the transaction has completed. SW must write a 1 to this bit to clear the event.
29	**Interrupt_on_Done** Project: All Format: Enable an interrupt in the hotplug status register when the transaction completes or times out.
28	**Time_out_error** Project: All Access: R/W Clear A sticky bit that indicates the transaction has timed out. SW must write a 1 to this bit to clear the event.
27:26	**Time_out_timer_value** Project: All Default Value: 0b The time count depends on the 2X bit clock divider (bits 10:0) being programmed for 2MHz.

Value Na	me	Description	Project
00b	400us	400us	All
01b	600us	600us	All
10b	800us	800us	All
11b	1600us	1600us	All

25	**Receive_error** Project: All Access: R/W Clear A sticky bit that indicates that the data received was corrupted, not in multiples of a full byte, or more than 20 bytes. SW must write a 1 to this bit to clear the event.

DPB_AUX_CH_CTL—Display Port B AUX Channel Control

24:20	**Message_Size** Project: All Format: This field is used to indicate the total number bytes to transmit (including the header). It also indicates the number of bytes received in a transaction (including the header). This field is valid only when the done bit is set, and if timeout or receive error has not occurred. Sync/Stop are not part of the message or the message size. Reads of this field will give the response message size. The read value will not be valid while Busy bit 31 is asserted. Message sizes of 0 or >20 are not allowed.
19:16	**Precharge_Time** Project: All Format: Default Value: 0101b 10us Used to determine the precharge time for the Aux Channel drivers. The value is the number of microseconds times 2 (assuming 2X bit clock divider programmed for 2MHz). Default is 5 decimal which gives 10us of precharge. Example: For 10us precharge, program 5 (10us/2us).
15	Reserved
14	**Invert_Manchester** Project: All Security: Test Default Value: 0b

Value Name		Description	Project
0b	Normal	Manchester code rising edge mid-clk signifies zero	All
1b	Invert	Manchester code rising edge mid-clk signifies one	All

13	**Sync_Only_Clock_Recovery** Project: All Security: Test Default Value: 0b

Value Name		Description	Project
0b	Sync and Data	Recover clock during sync pattern and data phase	All
1b	Sync Only	Only recover clock during sync pattern	All

DPB_AUX_CH_CTL—Display Port B AUX Channel Control

12 **Disable_De-glitch**

Project: All
Security: Test
Default Value: 0b

Value Name		Description	Project
0b	Enable	Enable serial input de-glitch logic	All
1b	Disable	Disable serial input de-glitch logic	All

11 **Double_precharge**

Project: All
Security: Test
Default Value: 0b

Value Name		Description	Project
0b	Programmed	Precharge time is as programmed	All
1b	Doubled	Precharge time is doubled	All

10:0 **2X_Bit_Clock_divider** Project: All Format: 2*U11

Used to determine the 2X bit clock the Aux Channel logic runs on.

This value divides the input clock frequency down to 2X bit clock rate. The 2X bit clock rate is ideally 2MHz (0.5us). The input clock is the 125mhz rawclk.

Example:

For 300MHz input clock and desired 2MHz 2X bit clock, program 150 (300MHz/2MHz).

4.3.3 DPB_AUX_CH_DATA—Display Port B AUX Data Registers

DP Aux Ch Data Format	
Project:	All
Bit De	**scription**
31:0	**AUX_CH_DATA** Project: All A DWord of the message. Writes give the data to transmit during the transaction. The MSbyte is transmitted first. Reads will give the response data after transaction complete.

DPB_AUX_CH_DATA—Display Port B AUX Data Registers	
Register Type:	MMIO
Address Offset:	E4114h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	5x32

The read value will not be valid while Busy bit 31 is asserted.

DWord	Bit	Description
0	31:0	**AUX_CH_DATA1** Project: All Format: DP Aux Ch Data Format
1	31:0	**AUX_CH_DATA2** Project: All Format: DP Aux Ch Data Format
2	31:0	**AUX_CH_DATA3** Project: All Format: DP Aux Ch Data Format
3	31:0	**AUX_CH_DATA4** Project: All Format: DP Aux Ch Data Format
4	31:0	**AUX_CH_DATA5** Project: All Format: DP Aux Ch Data Format

]

4.4 DPC Control and Aux Channel

4.4.1 DPC—Display Port C Control Register

DPC—Display Port C Control Register

Register Type:	MMIO
Address Offset:	E4200h
Project:	All
Default Value:	00000018h
Access:	R/W Protect
Size (in bits):	32
Double Buffer Update Point:	Depends on bit

Port enable and transcoder select are write protected by Panel Power Sequencer when panel is connected to this port. Please note that DisplayPort C uses the same lanes as HDMI. Therefore HDMIC and DisplayPort C cannot be enabled simultaneously.

Bit De	scription
31	**DisplayPort_C_Enable** Project: All Default Value: 0b See DPB description. [DevIBX] When disabling the port, software must temporarily enable the port with transcoder select (bit #30) cleared to '0' after disabling the port. This is workaround for hardware issue where the transcoder select set to '1' will prevent HDMIC from being enabled on transcoder A.

Value Na	me	Description	Project
0b	Disable	Disable and tristates the Display Port C interface	All
1b	Enable	Enable. This bit enables the Display Port C interface	All

30	**Transcoder_Select** Project: All Default Value: 0b See DPB description. [DevIBX] Writing to this bit only takes effect when port is enabled. Due to hardware issue it is required that this bit be cleared when port is disabled. To clear this bit software must temporarily enable this port on transcoder A.

Value Na	me	Description	Project
0b	Transcoder A	Transcoder A	All
1b	Transcoder B	Transcoder B	All

DPC—Display Port C Control Register

29:28 **Link_training_pattern_enable**

Project: All

Default Value: 0b

These bits are used for link initialization as defined in the DisplayPort specification. Please note that the link must first be configured prior to sending training patterns.

When enabling the port, it must be turned on with pattern 1 enabled. When retraining a link, the port must be disabled, then re-enabled with pattern 1 enabled.

Value Name		Description	Project
00b	Pattern 1	Pattern 1 enabled: Repetition of D10.2 characters	All
01b	Pattern 2	Pattern 2 enabled: Repetition of K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2.	All
10b	Idle	Idle Pattern enabled: Transmit BS followed by VB-ID with NoVideoStream_flag set to 1, five times	All
11b	Normal	Link not in training: Send normal pixels	All

27:25 **Voltage_swing_level_set**

Project: All

Default Value: 0b

See DPB description.

Value Name		Description	Project
000b	0.4V	0.4 V	All
001b	0.6V	0.6 V	All
010b	0.8V	0.8 V	All
011b	1.2V	1.2 V	All
1XXb	Reserved	Reserved	All

24:22 **Pre-emphasis_level_set**

Project: All

Default Value: 0b

See DPB description.

Value Name		Description	Project
000b	None	**No pre-emphasis**	All
001b	3.5dB	3.5dB pre-emphasis (1.5x)	All
010b	6 dB	6dB pre-emphasis (2x)	All
011b	9.5 dB	9.5dB pre-emphasis (3x)	All
1XXb	Reserved	Reserved	All

DPC—Display Port C Control Register

21:19 Port_Width_Selection

Project: All
Default Value: 0b
See DPB description.

Value Name		Description	Project
000b	x1	x1 Mode	All
001b	x2	x2 Mode	All
011b	x4	x4 Mode	All
others	Reserved	Reserved	All

18 Enhanced_Framing_Enable

Project: All
Default Value: 0b
See DPB description.

Value Name		Description	Project
0b	Disable	Enhanced framing disabled	All
1b	Enable	Enhanced framing enabled	All

17:16 Reserved Project: All Format: MBZ

15 Port_reversal

Project: All
Default Value: 0b
See DPB description.

Value Name		Description	Project
0b	Not Reversed	Port not reversed	All
1b	Reversed	Port reversed	All

14:8 Reserved Project: All Format: MBZ

7 Scrambling_Disable

Project: All
Security: Debug
Default Value: 0b
See DPB description.

Value Name		Description	Project
0b	Enable	Scrambling enabled	All
1b	Disable	Scrambling disabled	All

DPC—Display Port C Control Register

6 — Audio_Output_Enable

Project: All

Default Value: 0b

This bit enables audio on this output port. It may be enabled or disabled only when the link training is complete and set to “Normal.”

Value Name	Description	Project
0b Disable	Audio output disabled	All
1b Enable	Audio output enabled	All

5 — Reserved

4:3 — Sync_Polarity

Project: All

Default Value: 11b VS and HS are active high

See DPB description.

Value Name	Description	Project
00b Low	VS and HS are active low (inverted)	All
11b VS Low, HS High	VS is active low (inverted), HS is active high	All
11b VS High, HS Low	VS is active high, HS is active low (inverted)	All
11b High	VS and HS are active high	All

2 — Digital_Display_C_Detected

Project: All

Access: Read Only

Default Value: 0b

Read-only bit indicating whether a digital display was detected during initialization. It signifies the level of the GMBUS port 3 (port C) data line at boot.

Value Name	Description	Project
0b Not Detected	Digital display not detected during initialization	All
1b Detected	Digital display detected during initialization	All

1:0 — Reserved Project: All Format: MBZ

4.4.2 DPC_AUX_CH_ CTL—Display Port C AUX Channel Control

DPC_AUX_CH_CTL—Display Port C AUX Channel Control

Register Type: MMIO
Address Offset: E4210h
Project: All
Default Value: 00050000h
Access: R/W
Size (in bits): 32

Bit De	scription
31	**Send/Busy** Project: All Default Value: 0b See DPB description. **Programming Notes** Do not change any fields while Busy bit 31 is asserted.
30	**Done** Project: All Access: R/W Clear See DPB description.
29	**Interrupt_on_Done** Project: All Format: See DPB description.
28	**Time_out_error** Project: All Access: R/W Clear See DPB description.
27:26	**Time_out_timer_value** Project: All Default Value: 0b See DPB description.
25	**Receive_error** Project: All Access: R/W Clear See DPB description.
24:20	**Message_Size** Project: All Format: See DPB description.

Value Na	me	Description	Project
00b	400us	400us	All
01b	600us	600us	All
10b	800us	800us	All
11b	1600us	1600us	All

DPC_AUX_CH_CTL—Display Port C AUX Channel Control

19:16 Precharge_Time Project: All Format:
Default Value: 0101b 5 decimal which gives 10us of precharge
See DPB description.

15 Reserved

14 Invert_Manchester
Project: All
Security: Test
Default Value: 0b

Value Name	Description	Project
0b Zero	Manchester code rising edge mid-clk signifies zero	All
1b One	Manchester code rising edge mid-clk signifies one	All

13 Sync_Only_Clock_Recovery
Project: All
Security: Test
Default Value: 0b

Value Name	Description	Project
0b Sync and Data	Recover clock during sync pattern and data phase	All
1b Sync Only	Only recover clock during sync pattern	All

12 Disable_De-glitch
Project: All
Security: Test
Default Value: 0b

Value Name	Description	Project
0b Enable	Enable serial input de-glitch logic	All
1b Disable	Disable serial input de-glitch logic	All

11 Double_precharge
Project: All
Security: Test
Default Value: 0b

Value Name	Description	Project
0b Programmed	Precharge time is as programmed	All
1b Doubled	Precharge time is doubled	All

10:0 2X_Bit_Clock_divider Project: All Format: 2*U11
See DPB description.

4.4.3 DPC_AUX_CH_DATA—Display Port C AUX Data Registers

DPC_AUX_CH_DATA—Display Port C AUX Data Registers						
Register Type: MMIO **Address Offset:** E4214h **Project:** All **Default Value:** 00000000h; **Access:** R/W **Size (in bits):** 5x32						
The read value will not be valid while Busy bit 31 is asserted.						
DWord Bit		**Description**				
0	31:0	**AUX_CH_DATA1**	Project:	All	Format:	DP Aux Ch Data Format
1	31:0	**AUX_CH_DATA2**	Project:	All	Format:	DP Aux Ch Data Format
2	31:0	**AUX_CH_DATA3**	Project:	All	Format:	DP Aux Ch Data Format
3	31:0	**AUX_CH_DATA4**	Project:	All	Format:	DP Aux Ch Data Format
4	31:0	**AUX_CH_DATA5**	Project:	All	Format:	DP Aux Ch Data Format

4.5 DPD Control and Aux Channel

4.5.1 DPD—DisplayPort D Control Register

DPD—DisplayPort D Control Register	
Register Type:	MMIO
Address Offset:	E4300h
Project:	All
Default Value:	00000018h
Access:	R/W Protect
Size (in bits):	32
Double Buffer Update Point:	Depends on bit

Port enable and transcoder select are write protected by Panel Power Sequencer when panel is connected to this port. Please note that DisplayPort D uses the same lanes as HDMID. Therefore HDMID and DisplayPort D cannot be enabled simultaneously.

Bit De	scription
31	**DisplayPort_D_Enable** Project: All Default Value: 0b See DPB description. [DevIBX] When disabling the port, software must temporarily enable the port with transcoder select (bit #30) cleared to '0' after disabling the port. This is workaround for hardware issue where the transcoder select set to '1' will prevent HDMID from being enabled on transcoder A.

Value Na	me	Description	Project
0b	Disable	Disable and tristates the Display Port D interface	All
1b	Enable	Enable. This bit enables the Display Port D interface	All

DPD—DisplayPort D Control Register

30

Transcoder_Select

Project: All

Default Value: 0b

See DPB description.

[DevIBX] Writing to this bit only takes effect when port is enabled. Due to hardware issue it is required that this bit be cleared when port is disabled. To clear this bit software must temporarily enable this port on transcoder A.

Value Na	me	Description	Project
0b	Transcoder A	Transcoder A	All
1b	Transcoder B	Transcoder B	All

29:28

Link_training_pattern_enable

Project: All

Default Value: 0b

These bits are used for link initialization as defined in the DisplayPort specification. Please note that the link must first be configured prior to sending training patterns.

When enabling the port, it must be turned on with pattern 1 enabled. When retraining a link, the port must be disabled, then re-enabled with pattern 1 enabled.

Value Na	me	Description	Project
00b	Pattern 1	Pattern 1 enabled: Repetition of D10.2 characters	All
01b	Pattern 2	Pattern 2 enabled: Repetition of K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2.	All
10b	Idle	Idle Pattern enabled: Transmit BS followed by VB-ID with NoVideoStream_flag set to 1, five times	All
11b	Normal	Link not in training: Send normal pixels	All

27:25

Voltage_swing_level_set

Project: All

Default Value: 0b

See DPB description.

Value Na	me	Description	Project
000b	0.4V	0.4 V	All
001b	0.6V	0.6 V	All
010b	0.8V	0.8 V	All
011b	1.2V	1.2 V	All
1XXb	Reserved	Reserved	All

DPD—DisplayPort D Control Register

24:22 Pre-emphasis_level_set

Project: All

Default Value: 0b

See DPB description.

Value Name	Description	Project
000b	None **No pre-emphasis**	All
001b	3.5dB 3.5dB pre-emphasis (1.5x)	All
010b	6 dB 6dB pre-emphasis (2x)	All
011b	9.5 dB 9.5dB pre-emphasis (3x)	All
1XXb	Reserved Reserved	All

21:19 Port_Width_Selection

Project: All

Default Value: 0b

See DPB description.

Value Name	Description	Project
000b	x1 x1 Mode	All
001b	x2 x2 Mode	All
011b	x4 x4 Mode	All
others	Reserved Reserved	All

18 Enhanced_Framing_Enable

Project: All

Default Value: 0b

See DPB description.

Value Name	Description	Project
0b	Disable Enhanced framing disabled	All
1b	Enable Enhanced framing enabled	All

17:16 Reserved Project: All Format: MBZ

15 Port_reversal

Project: All

Default Value: 0b

See DPB description.

Value Name	Description	Project
0b	Not Reversed Port not reversed	All
1b	Reversed Port reversed	All

DPD—DisplayPort D Control Register

14:8	**Reserved** Project: All Format: MBZ
7	**Scrambling_Disable** Project: All Security: Debug Default Value: 0b See DPB description.

Value Name	Description	Project
0b Enable	Scrambling enabled	All
1b Disable	Scrambling disabled	All

6	**Audio_Output_Enable** Project: All Default Value: 0b This bit enables audio on this output port. It may be enabled or disabled only when the link training is complete and set to “Normal.”

Value Name	Description	Project
0b Disable	Audio output disabled	All
1b Enable	Audio output enabled	All

5	Reserved
4:3	**Sync_Polarity** Project: All Default Value: 11b VS and HS are active high See DPB description.

Value Name	Description	Project
00b Low	VS and HS are active low (inverted)	All
11b VS Low, HS High	VS is active low (inverted), HS is active high	All
11b VS High, HS Low	VS is active high, HS is active low (inverted)	All
11b High	VS and HS are active high	All

DPD—DisplayPort D Control Register

2 — **Digital_Display_D_Detected**

Project: All

Access: Read Only

Default Value: 0b

Read-only bit indicating whether a digital display was detected during initialization. It signifies the level of the GMBUS port 5 (port D) data line at boot.

Value Name	Description	Project
0b	Not Detected	Digital display not detected during initialization	All
1b	Detected	Digital display detected during initialization	All

1:0 — **Reserved** Project: All Format: MBZ

4.5.2 DPD_AUX_CH_ CTL—Display Port D AUX Channel Control

DPD_AUX_CH_CTL—Display Port D AUX Channel Control

Register Type: MMIO
Address Offset: E4310h
Project: All
Default Value: 00050000h
Access: R/W
Size (in bits): 32

Bit De	scription
31	**Send/Busy** Project: All Default Value: 0b See DPB description. **Programming Notes** Do not change any fields while Busy bit 31 is asserted.
30	**Done** Project: All Access: R/W Clear See DPB description.
29	**Interrupt_on_Done** Project: All Format: See DPB description.
28	**Time_out_error** Project: All Access: R/W Clear See DPB description.
27:26	**Time_out_timer_value** Project: All Default Value: 0b See DPB description.
25	**Receive_error** Project: All Access: R/W Clear See DPB description.
24:20	**Message_Size** Project: All Format: See DPB description.

Value Name	Description	Project
00b	400us	All
01b	600us	All
10b	800us	All
11b	1600us	All

DPD_AUX_CH_CTL—Display Port D AUX Channel Control

19:16 **Precharge_Time** Project: All Format:
Default Value: 0101b 5 decimal which gives 10us of precharge
See DPB description.

15 Reserved

14 **Invert_Manchester**
Project: All
Security: Test
Default Value: 0b

Value Name	Description	Project
0b Zero	Manchester code rising edge mid-clk signifies zero	All
1b One	Manchester code rising edge mid-clk signifies one	All

13 **Sync_Only_Clock_Recovery**
Project: All
Security: Test
Default Value: 0b

Value Name	Description	Project
0b Sync and Data	Recover clock during sync pattern and data phase	All
1b Sync Only	Only recover clock during sync pattern	All

12 **Disable_De-glitch**
Project: All
Security: Test
Default Value: 0b

Value Name	Description	Project
0b Enable	Enable serial input de-glitch logic	All
1b Disable	Disable serial input de-glitch logic	All

11 **Double_precharge**
Project: All
Security: Test
Default Value: 0b

Value Name	Description	Project
0b Programmed	Precharge time is as programmed	All
1b Doubled	Precharge time is doubled	All

10:0 **2X_Bit_Clock_divider** Project: All Format: 2*U11
See DPB description.

4.5.3 DPD_AUX_CH_DATA—Display Port D AUX Data Registers

DPD_AUX_CH_DATA—Display Port D AUX Data Registers						
Register Type: MMIO **Address Offset:** E4314h **Project:** All **Default Value:** 00000000h; **Access:** R/W **Size (in bits):** 5x32						
The read value will not be valid while Busy bit 31 is asserted.						
DWord Bit		**Description**				
0	31:0	**AUX_CH_DATA1**	Project:	All	Format:	DP Aux Ch Data Format
1	31:0	**AUX_CH_DATA2**	Project:	All	Format:	DP Aux Ch Data Format
2	31:0	**AUX_CH_DATA3**	Project:	All	Format:	DP Aux Ch Data Format
3	31:0	**AUX_CH_DATA4**	Project:	All	Format:	DP Aux Ch Data Format
4	31:0	**AUX_CH_DATA5**	Project:	All	Format:	DP Aux Ch Data Format

4.6 DP_BUFTRANS—DisplayPort Buffer Translation

DisplayPort Buffer Translation Format						
Project: All **Default Value:** 00000000h						
Bit De	**scription**					
31:28	**Reserved**	Project:	All	Format:	MBZ	
27:19	**OE** These bits select the OE vswing level	Project:	All	Range:	0..511	
18:17	**Reserved**	Project:	All	Format:	MBZ	
16:12	**Pre_Emphasis** These bits select the pre-emphasis level	Project:	All	Range:	0..31	
11:10	**Reserved**	Project:	All	Format:	MBZ	
9:6	**P_current_drive** These bits select the P current drive value	Project:	All	Range:	0..15	
5:4	**Reserved**	Project:	All	Format:	MBZ	
3:0	**N_current_drive** These bits select the N current drive value	Project:	All	Range:	0..15	

The register defaults for B0 silicon was provided by EV team (2/09). These MUST be programmed by software before enabling DisplayPort the first time. They only need to be programmed once after power on.

10/6/09: L3 0dB setting has been revised to pass compliance testing

DP mode		Offset	Value
L1	0dB	0xE4F00	**0x0100030C**
L1	3.5dB	0xE4F04	**0x00B8230C**
L1	6dB	0xE4F08	**0x06F8930C**
L1	9.5dB	0xE4F0C	**0x09F8E38E**
L2	0dB	0xE4F10	**0x00B8030C**
L2	3.5dB	0xE4F14	**0x0B78830C**
L2	6dB	0xE4F18	**0x0FF8D3CF**
L3	0dB	0xE4F1C	**0x01E8030C**
L3	3.5dB	0xE4F20	**0x0FF863CF**
L4	0 dB	0xE4F24	**0x0FF803CF**

Vswing	0dB pre-emphasis	3.5dB pre-emphasis	6dB pre-emphasis	9.5dB pre-emphasis
400mV	E4F00	E4F04	E4F08	E4F0C
600mV	E4F10	E4F14	E4F18	Not supported
800mV	E4F1C	E4F20	Not supported	Not supported
1200mV	E4F24	Not supported	Not supported	Not supported

DP_BUFTRANS—DisplayPort Buffer Translation

Register Type: MMIO
Address Offset: E4F00h
Project: DevIBX-B+
Default Value: 0100038Eh; 00B8338Eh; 0178838Eh; 09F8E38Eh; 00B8038Eh; 0978838Eh; 09F8B38E; 0178038Eh; 09F8638Eh; 09F8038Eh
Access: Write Only
Size (in bits): 10x32

These registers define current drive, pre-emphasis and voltage swing buffer programming required for the different voltage swing and pre-emphasis settings in the DisplayPort Control.

DWord	Bit	Description
0	31:0	**Voltage_swing_400mV_and_Pre-emphasis_0.0dB** Project: All Format: DisplayPort Buffer Translation Format See Description Above
1	31:0	**Voltage_swing_400mV_and_Pre-emphasis_3.5dB** Project: All Format: DisplayPort Buffer Translation Format See Description Above
2	31:0	**Voltage_swing_400mV_and_Pre-emphasis_6.0dB** Project: All Format: DisplayPort Buffer Translation Format See Description Above
3	31:0	**Voltage_swing_400mV_and_Pre-emphasis_9.5dB** Project: All Format: DisplayPort Buffer Translation Format See Description Above
4	31:0	**Voltage_swing_600mV_and_Pre-emphasis_0.0dB** Project: All Format: DisplayPort Buffer Translation Format See Description Above
5	31:0	**Voltage_swing_600mV_and_Pre-emphasis_3.5dB** Project: All Format: DisplayPort Buffer Translation Format See Description Above
6	31:0	**Voltage_swing_600mV_and_Pre-emphasis_6.0dB** Project: All Format: DisplayPort Buffer Translation Format See Description Above
7	31:0	**Voltage_swing_800mV_and_Pre-emphasis_0.0dB** Project: All Format: DisplayPort Buffer Translation Format See Description Above
8	31:0	**Voltage_swing_800mV_and_Pre-emphasis_3.5dB** Project: All Format: DisplayPort Buffer Translation Format See Description Above
9	31:0	**Voltage_swing_1200mV_and_Pre-emphasis_0.0dB** Project: All Format: DisplayPort Buffer Translation Format See Description Above

5. South AFE Registers (FC000h–FFFFFh)

This topic is documented separately