Intel Open Source Graphics Programmer's Reference Manual (PRM) for the 2013 Intel® Core™ Processor Family, including Intel HD Graphics, Intel Iris™ Graphics and Intel Iris Pro Graphics

Volume 11b: Display Watermark Guide (Haswell)

12/18/2013

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Display Watermark Programming

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Watermark Overview

The display watermarks are used to control the display engine memory request behavior.

The default settings of the watermark configuration registers will allow the display engine to operate; however, they are not optimized for power or memory bandwidth efficiency. The watermark values must be properly calculated and programmed in order to achieve optimum power and performance. Incorrectly programmed watermark values can result in screen corruption.

The watermarks should be calculated and programmed when any of the watermark calculation inputs change. This includes planes enabling or disabling, plane source format or size changing, etc.

Besides programming the watermark registers, there are other display configuration requirements and registers that must be programmed in order for the display to operate in a low power mode, and there are memory controller configuration requirements which are not documented here.

Watermark Calculations

The display watermarks are calculated using information from the display and memory configurations.

The calculation must be done for every enabled display plane and watermark level. The calculated values are then compared against the maximum allowed values to decide how to program the display watermark configuration registers.

There are two methods for calculating watermarks. Use the following table to select the method.

Plane Type	Watermark Level	Watermark Method
Primary	WM_PIPE	Method 1
	WM_LP*	The lesser of Method 1 and Method 2
Sprite	WM_PIPE	The lesser of Method 1 and Method 2
	WM_LP*	The lesser of Method 1 and Method 2
Cursor	WM_PIPE	Method 2
	WM_LP*	Method 2

Note: See the Memory Values section to find the memory value used in the watermark methods.

Note: Pixel rate may have to be adjusted, see the Pixel Rate Adjustments section.

The ceiling function rounds any non-integer value up to the next greater integer.

Example: ceiling[0.3]=1, ceiling[2.1]=3, ceiling[4.8]=5

The floor function rounds any non-integer value down to the integer.

Example: floor[0.3]=0.0, floor[2.1]=2.0, floor[4.8]=4.0

Watermark Method 1

Watermark intermediate value = pixel rate MHz * plane source bytes per pixel * memory value microseconds

Watermark final value = ceiling[(watermark intermediate value / 64) + 2]

Example:

4 bytes per pixel plane source, pixel rate 108 MHz, and memory value of 7.5:

Watermark intermediate value = 108 MHz * 4 Bpp * 7.5 = 3240

Watermark final value = ceiling[(3240 / 64) + 2] = 53

Note: Pixel rate may have to be adjusted, see the Pixel Rate Adjustments section.

Watermark Method 2

Line time in microseconds = Pipe horizontal total number of pixels / pixel rate MHz

Watermark intermediate value = [floor(memory value microseconds / line time microseconds) + 1] * plane source width pixels * plane source bytes per pixel

Watermark final value = ceiling[(watermark intermediate value / 64) + 2]

Example:

4 bytes per pixel plane source, 640 pixel plane source width, 12.5 us line time, and memory value of 1.7:

Watermark intermediate value = [floor(1.7 / 12.5) + 1] * 640 * 4 = 2560

Watermark final value = ceiling[(2560 / 64) + 2] = 42

Example:

4 bytes per pixel plane source, 640 pixel plane source width, 12.5 us line time, and memory value of 22.0:

Watermark intermediate value = [floor(22.0 / 12.5 us) + 1] * 640 * 4 Bpp = 5120

Watermark final value = ceiling[(5120 / 64) + 2] = 82

Note: Pixel rate may have to be adjusted, see the Pixel Rate Adjustments section.

Watermark for Frame Buffer Compression

The Frame Buffer Compression (FBC) watermark only needs to be programmed if FBC is enabled.

The FBC watermark is disabled by setting MMIO register ARB_CT 0x45000 bit 15 = 1b.

FBC watermark value = ceiling [((primary plane watermark value * 64) / (horizontal source size * bytes per pixel)) + 2]

Example:

4 bytes per pixel plane source, 800 pixel plane source width, and primary plane watermark value of 124:

FBC watermark = ceiling [((124 * 64) / (800 * 4 Bpp)) + 2] = 5

Watermark Maximum Value

The maximum watermark values for each watermark depend on the display configuration and the data buffer partitioning selection in WM_MISC 0x45260 bit 0.

The maximums control which watermark levels can be programmed in the watermark registers and which watermark registers can be enabled.

Pipe Watermark Maximums

These are the maximum values for the WM_PIPE watermarks.

Watermark	Maximum
Primary	127
Sprite	127
Cursor	63

If any of the WM_PIPE maximum watermark values are exceeded, the display configuration cannot be supported.

Low Power Watermark Maximums

These are the maximum values for the WM_LP* watermarks.

Table: Single Display Pipe Enabled

Watermark	Configuration	Maximum
Primary	Sprite disabled	768
	Sprite enabled, Data buffer partitioning = 0	384
	Sprite enabled, Data buffer partitioning = 1	128
Sprite	Data buffer partitioning = 0	384
	Data buffer partitioning = 1	640
Cursor	Any	255
FBC	Any	15 lines

Table: Multiple Display Pipes Enabled

Watermark	Configuration	Maximum
Primary	Sprite disabled	256
	Sprite enabled	128
Sprite	Any	128
Cursor	Any	64
FBC	Any	15 lines

If the maximum watermark level is exceeded due to the data buffer partitioning selection, it is preferred to change the data buffer partitioning selection instead of disabling a watermark level.

If the FBC maximum watermark value is exceeded, it is preferred to disable FBC watermarks (set ARB_CTRL 0x45000 bit 15 = 1) instead of disabling a watermark level.

See the Watermark Calculations section for the formulas used to calculate watermark values.

Watermark Mappings

There are five sets of memory values, level 0, level 1, level 2, level 3, and level 4. Level 0 is used in both high and low power modes. Levels 1 through 4 map roughly to increasingly deeper package C states.

There are four sets of watermark registers, WM_PIPE, WM_LP1, WM_LP2, and WM_LP3.

The mapping of the memory values to watermark registers and decision on which watermark registers can be enabled is based on whether the watermark calculations for a given level exceed the maximum watermark value. The watermark calculations for a memory level are considered to exceed the maximum if any plane (primary, sprite, or cursor) watermark value calculated with that memory level value is greater than the maximum watermark for that plane, after any adjustment to data buffer partitioning.

There are two mappings of the five memory values to the four sets of watermark registers.

WM_PIPE memory value selection = Level 0

WM_LP_1 memory value selection = Level 1

WM_LP_2 memory value selection = Level 2 if watermark calculation for memory value level 4 exceeds maximum, else level 3

WM_LP_3 memory value selection = Level 3 If watermark calculation for memory value level 4 exceeds maximum, else level 4

The WM_LP* watermark configuration registers Latency field (bits 30:24) is programmed to **twice** the selected memory level.

On Haswell A step the WM_LP* watermark configuration registers Latency field (bits 30:24) is programmed to **match** the selected memory level.

A watermark register should only be enabled if the watermark calculations for that register do not exceed the maximum and the lower level watermark registers are enabled.

WM_PIPE enable if watermark calculation for WM_PIPE does not exceed maximum

WM_LP_1 enable if watermark calculation for WM_LP_1 does not exceed maximum and WM_PIPE is enabled

WM_LP_2 enable if watermark calculation for WM_LP_2 does not exceed maximum and WM_LP_1 is enabled

WM_LP_3 enable if watermark calculation for WM_LP_3 does not exceed maximum and WM_LP_2 is enabled

The WM_LP* watermark configuration registers Enabled field (bit 31) is programmed to 1b if enabled, 0b if disabled.

If WM_PIPE is disabled, then the display mode is not supported.

The following examples represent Haswell B step or later.

Table: Example: Level 4 fits maximum

Watermark Register	Enable Field	Latency Field
WM_LP_1	1	2
WM_LP_2	1	6
WM_LP_3	1	8

Table: Example: Level 4 exceeds maximum

Watermark Register	Enable Field	Latency Field
WM_LP_1	1	2
WM_LP_2	1	4
WM_LP_3	1	6

Table: Example: Level 3 exceeds maximum

Watermark Register	Enable Field	Latency Field
WM_LP_1	1	2
WM_LP_2	1	4
WM_LP_3	0 (disabled)	N/A

Pixel Rate Adjustments

The pixel rate is a key input to the watermark calculations. The base pixel rate for watermark calculations comes from the pixel rate for the selected display resolution. That value is then adjusted depending on the display configuration as explained below.

Multiple Refresh Rates

When multiple refresh rates are programmed for a single display pipe, use the fastest pixel rate for the watermark calculation base pixel rate.

The WM_LINETIME register Line Time field (bits 8:0) is programmed using the smallest line time when using multiple refresh rates.

Interlacing

When the display pipe configuration is set to the Progressive Fetch - Interlace Display (PF-ID) mode, the watermark calculation pixel rate must be doubled.

The WM_LINETIME register Line Time field (bits 8:0) is not adjusted for Interlacing.

Panel Fitter Down Scaling

When a panel fitter is enabled and down scaling (panel fitter window size is less than pipe source size for either the horizontal or vertical dimension), the watermark calculation pixel rate must be increased by the down scale amount.

Both the panel fitter vertical and horizontal down scale amounts must be multiplied together to give the total down scale amount. If any down scale amount is less than 1, replace it with 1 (see second example).

Horizontal down scale amount = Pipe horizontal source size / Panel fitter horizontal window size

Vertical down scale amount = Pipe vertical source size / Panel fitter vertical window size

Total down scale amount = Horizontal down scale amount (if less than 1, use 1 instead) * Vertical down scale amount (if less than 1, use 1 instead)

Example:

Down scale in both vertical and horizontal with a 1920x1080 source size and 1700x964 window size

Horizontal down scale amount = 1920 / 1700 = 1.13

Vertical down scale amount = 1080 / 964 = 1.12

Total down scale amount = 1.13 * 1.12 = 1.27

Pixel rate must be multiplied by 1.27 to compensate for down scale

Example:

Down scale in only horizontal with a 1920x1080 source size and 1700x1120 window size

Horizontal down scale amount = 1920 / 1700 = 1.13

Vertical down scale amount = 1080 / 1120 = 0.96 **(less than 1 so use 1 instead in the next calculation)**

Total down scale amount = 1.13 * 1 = 1.13

Pixel rate must be multiplied by 1.13 to compensate for down scale

When both panel fitter down scaling and progressive fetch - interlace (PF-ID) display is enabled, the pixel rate increases will multiply together. For example PF-ID with total downscale 1.10 requires pixel rate to be multiplied by 2.20.

The WM_LINETIME register Line Time field (bits 8:0) is not adjusted for panel fitter down scaling.

IPS

The WM_LINETIME register IPS Line Time field (bits 24:0) is programmed specifically for IPS, using core display clock as the frequency.

Multiple Pipes

When multiple display pipes are enabled, calculate the watermark separately for every enabled plane and level. Program WM_PIPE separately for each enabled pipe. Consolidate the level 1 to level 4 plane results by choosing the maximum value from all pipes, then follow the Watermark Mappings section to find the mapping and which watermarks can be enabled.

The maximum watermark values are changed when multiple pipes are enabled. See the watermark maximum value tables.

Example: Primary planes enabled on three pipes and the low power watermark maximum is 256

Calculated pipe A primary plane Level 1 watermark value = 20

Calculated pipe B primary plane Level 1 watermark value = 22 (greatest)

Calculated pipe C primary plane Level 1 watermark value = 18

Consolidated primary plane Level 1 watermark value = 22

...same sort of consolidation repeated across all levels...

Consolidated primary plane Level 2 watermark value = 60

Consolidated primary plane Level 3 watermark value = 108

Consolidated primary plane Level 4 watermark value = 300 (exceeds the maximum, so level 4 will not be used)

Result:

WM_LP_1 enabled, latency 2, and primary watermark 20.

WM_LP_2 enabled, latency 4, and primary watermark 60.

WM_LP_3 enabled, latency 6, and primary watermark 108.

Memory Values

The values for a given memory configuration are found in the MCHBAR PCU 0:0:0 0x5D10 SSKPD register which can also be accessed through GTTMMADR 0x145D10.

There are two separate fields for WM0, the level 0 watermark. If New WM0 (bits 63:56) is non-zero, use that field for watermark calculations, otherwise use Old WM0 (bits 3:0) for watermark calculations.

Table: SSKPD Register Definition

Symbol	Name	MSb:LSb	Description
New WM0	**New** Level 0	63:56	**New WM0 field** Number of microseconds for level 0 (0.1us granularity). 00h=0us 01h=0.1us ... FFh=25.5us
Reserved	Reserved	55:41	Reserved
WM4	Level 4	40:32	Number of microseconds for level 4 (0.5us granularity). 000h=0us 001h=0.5us ... 1FFh=255.5us
Reserved	Reserved	31:29	Reserved
WM3	Level 3	28:20	Number of microseconds for level 3 (0.5us granularity). 000h=0us 001h=0.5us ... 1FFh=255.5us
WM2	Level 2	19:12	Number of microseconds for level 2 (0.5us granularity). 00h=0us 01h=0.5us ... FFh=127.5us

Symbol	Name	MSb:LSb	Description
WM1	Level 1	11:4	Number of microseconds for level 1 (0.5us granularity). 00h=0us 01h=0.5us ... FFh=127.5us
Old WM0	**Old** Level 0	3:0	**Old WM0 field** Number of microseconds for level 0 (0.1us granularity). 0h=0us 1h=0.1us ... Fh=1.5us

Display Low Power Configuration Requirements

Besides programming the watermark registers, there are other configuration requirements and registers that must be programmed in order for the display to operate in a low power mode

The following requirements represent the static values required for lower power modes and the listing order does not indicating a programming sequence. See the display programming document for programming sequence information.

Besides the display configuration requirements there are memory controller configuration requirements which are not documented here. Those should be programmed by the BIOS Memory Reference Code (MRC).

Display Configuration Register Requirements for Display Low Power Level 1

Pipe watermark values programmed per watermark calculation:

WM_PIPE_A 0x45100 Pipe Primary Watermark, Pipe Sprite Watermark, Pipe Cursor Watermark = Calculated values for primary plane, sprite plane, and cursor plane

WM_PIPE_B 0x45104 Pipe Primary Watermark, Pipe Sprite Watermark, Pipe Cursor Watermark = Calculated values for primary plane, sprite plane, and cursor plane

WM_PIPE_C 0x45200 Pipe Primary Watermark, Pipe Sprite Watermark, Pipe Cursor Watermark = Calculated values for primary plane, sprite plane, and cursor plane

Watermark line time values programmed per screen resolution:

WM_LINETIME_A 0x45270 bits [8:0] = Pipe A line time in multiples of 0.125 microseconds

WM_LINETIME_B 0x45274 bits [8:0] = Pipe B line time in multiples of 0.125 microseconds

WM_LINETIME_C 0x45278 bits [8:0] = Pipe C line time in multiples of 0.125 microseconds

Low Power 1 watermark enabled:

WM_LP1 0x45108 bit 31 = 1

Low Power 1 watermark memory configuration value comes from SSKPD:

WM_LP1 0x45108 bits [30:24] = Value matching the selected level from SSKPD

Low Power 1 watermark calculated values programmed:

WM_LP1 0x45108 bits [23:0] = Calculated values for primary plane, FBC, and cursor plane

WM_LP1_SPR 0x45120 bits [9:0] = Calculated values for sprite plane

VGA plane disabled:

VGA_CONTROL 0x41000 bit 31 = 1

IPS watermark line time value programmed per screen resolution (If IPS is enabled):

WM_LINETIME_A 0x45270 bits [8:0] = Pipe A IPS line time in multiples of 0.125 microseconds

Display Configuration Register Requirements for Display Low Power Level 2

Low Power Level 2 has all of the above requirements for Low Power Level 1, plus the additional requirements below.

Low Power 2 watermark enabled:

WM_LP2 0x4510C bit 31 = 1

Low Power 2 watermark memory configuration value comes from SSKPD:

WM_LP2 0x4510C bits [30:24] = Value for the selected level from SSKPD

Low Power 2 watermark calculated values programmed:

WM_LP2 0x4510C bits [23:0] = Calculated values for primary plane, FBC, and cursor plane

WM_LP2_SPR 0x45124 bits [9:0] = Calculated values for sprite plane

Display Configuration Register Requirements for Display Low Power Level 3

Low Power Level 3 has all of the above requirements for Low Power Level 2, plus the additional requirements below.

Low Power 3 watermark enabled:

WM_LP3 0x45110 bit 31 = 1

Low Power 3 watermark memory configuration value comes from SSKPD:

WM_LP3 0x45110 bits [30:24] = Value for the selected level from SSKPD

Low Power 3 watermark calculated values programmed:

WM_LP3 0x45110 bits [23:0] = Calculated values for primary plane, FBC, and cursor plane

WM_LP3_SPR 0x45128 bits [9:0] = Calculated values for sprite plane