

# Intel® Open Source HD Graphics Programmers' Reference Manual (PRM)

## **Volume 2a: Command Reference: Instructions (Command Opcodes)**

For the 2014-2015 Intel Atom™ Processors, Celeron™ Processors and Pentium™ Processors based on the "Cherry Trail/Braswell" Platform  
(Cherryview/Braswell graphics)

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## 3DPRIMITIVE

<b>3DPRIMITIVE</b>		
Project:	CHV, BSW	
Source:	RenderCS	
Length Bias:	2	
<p>The 3DPRIMITIVE command is used to submit 3D primitives to be processed by the 3D pipeline. Typically the processing results in rendering pixel data into the render targets, but this is not required.</p> <p>The parameters passed in this command are forwarded to the Vertex Fetch function. The Vertex Fetch function will use this information to generate vertex data structures and store them in the URB. These vertices are then passed down the 3D pipeline.</p>		
Programming Notes		
<p>If the threads spawned by this command are required to observe memory writes performed by threads spawned from a previous command, software must precede this command with a command that performs a (preferably pipelined) memory flush (e.g., 3D_PIPECONTROL).</p>		
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 3h GFXPIPE
	Format: OpCode	
	28:27	<b>Command SubType</b>
		Default Value: 3h GFXPIPE_3D
	Format: OpCode	
	26:24	<b>3D Command Opcode</b>
		Default Value: 3h 3DPRIMITIVE
	Format: OpCode	
	23:16	<b>3D Command Sub Opcode</b>
Default Value: 0h 3DPRIMITIVE		
Format: OpCode		
15	<b>Reserved</b>	
14:13	<b>Reserved</b>	
	Format: MBZ	
12	<b>Reserved</b>	
11	<b>Reserved</b>	
10	<b>Indirect Parameter Enable</b>	
	Format: Enable	
<p>If set, the values in DW 2-5 are ignored and replaced by the current values of the corresponding 3DPRIM_xxx MMIO registers:</p> <ul style="list-style-type: none"> <li>3DPRIM_VERTEX_COUNT (instead of DW2: VertexCountPerInstance)</li> </ul>		

<b>3DPRIMITIVE</b>							
	<ul style="list-style-type: none"> <li>• 3DPRIM_START_VERTEX (instead of DW3: StartVertexLocation)</li> <li>• 3DPRIM_INSTANCE_COUNT (instead of DW4: InstanceCount)</li> <li>• 3DPRIM_START_INSTANCE (instead of DW5: StartInstanceLocation)</li> <li>• 3DPRIM_BASE_VERTEX (instead of DW6: BaseVertexLocation)</li> </ul> <p>Indirect Parameter Enable and End Offset Enable shall not be ENABLED at the same time, or behavior is UNDEFINED.</p>						
	<p><b>9 UAV Coherency Required</b></p> <table border="1"> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>SW will be required to set this bit if there is the possibility of sharing a UAV from a previous 3DPRIMITVE command. If set, this command may cause a flush due to UAV coherency requirements. If none of the shaders have UAV access enabled, then this bit is ignored.</p>	Format:	U1				
Format:	U1						
	<p><b>8 Predicate Enable</b></p> <table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>If set, this command is executed (or not) depending on the current value of the MI Predicate internal state bit. This command is ignored only if PredicateEnable is set and the Predicate state bit is 0.</p>	Format:	Enable				
Format:	Enable						
	<p><b>7:0 DWord Length</b></p> <table border="1"> <tr> <td>Default Value:</td> <td>5h Excludes DWord (0,1)</td> </tr> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>=n Total Length - 2</td> </tr> </table>	Default Value:	5h Excludes DWord (0,1)	Project:	CHV, BSW	Format:	=n Total Length - 2
Default Value:	5h Excludes DWord (0,1)						
Project:	CHV, BSW						
Format:	=n Total Length - 2						
1	<p><b>31:10 Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p><b>9 End Offset Enable</b></p> <table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>If set, the Vertex Count Per Instance field is IGNORED, and the VB0ENDOFFSET register is used to indirectly specify the vertex count by defining the amount of valid data in VB0. The following restrictions apply:</p> <ul style="list-style-type: none"> <li>• VB0 must be enabled for use</li> <li>• VertexAccessType = SEQUENTIAL</li> <li>• Start Vertex Location = 0</li> <li>• Start Instance Location = 0</li> <li>• Base Vertex Location = 0</li> </ul> <p>Vertices are output until EndOffset is reached or exceeded in VB0. If EndOffset is reached or exceeded within the data associated with a vertex, that vertex is considered incomplete and will not be output. Partial objects will be discarded (as is normally done).</p>	Format:	MBZ	Format:	Enable		
Format:	MBZ						
Format:	Enable						

<b>3DPRIMITIVE</b>										
	<p>If clear, End Offset is ignored. Indirect Parameter Enable and End Offset Enable must not be ENABLED at the same time, or behavior is UNDEFINED.</p>									
8	<p><b>Vertex Access Type</b> This field specifies how data held in vertex buffers marked as VERTEXDATA is accessed by Vertex Fetch.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>SEQUENTIAL</td> <td>VERTEXDATA buffers are accessed sequentially Requiref if End Offset Enable is ENABLED.</td> </tr> <tr> <td>1h</td> <td>RANDOM</td> <td>VERTEXDATA buffers are accessed randomly via an index obtained from the Index Buffer.</td> </tr> </tbody> </table>	Value	Name	Description	0h	SEQUENTIAL	VERTEXDATA buffers are accessed sequentially Requiref if End Offset Enable is ENABLED.	1h	RANDOM	VERTEXDATA buffers are accessed randomly via an index obtained from the Index Buffer.
Value	Name	Description								
0h	SEQUENTIAL	VERTEXDATA buffers are accessed sequentially Requiref if End Offset Enable is ENABLED.								
1h	RANDOM	VERTEXDATA buffers are accessed randomly via an index obtained from the Index Buffer.								
7:6	<b>Reserved</b>									
5:0	<p><b>Primitive Topology Type</b></p> <table border="1"> <tr> <td>Format:</td> <td>3D_Prim_Topo_Type [CHV, BSW] See table below for encoding, see 3D Overview for diagrams and general comments</td> </tr> </table> <p style="text-align: center;"><b>Description</b></p> <p>This field specifies the topology type of 3D primitive generated by this command. Note that a single primitive topology (list/strip/fan/etc.) can contain a number of basic objects (lines, triangles, etc.).</p> <p>This field is ignored. The topology type is specified via the 3DSTATE_VF_TOPOLOGY command.</p>	Format:	3D_Prim_Topo_Type [CHV, BSW] See table below for encoding, see 3D Overview for diagrams and general comments							
Format:	3D_Prim_Topo_Type [CHV, BSW] See table below for encoding, see 3D Overview for diagrams and general comments									
2	<p>31:0 <b>Vertex Count Per Instance</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32 Count of vertices</td> </tr> </table> <p>This field specifies how many vertices are to be generated for each instance of the primitive topology. If End Offset Enable is clear: Format = U32 count of vertices Range = [0, 2<sup>32</sup>-1] (upper limit probably constrained by VB size) Ignored if End Offset Enable or Indirect Parameter Enable is ENABLED.</p> <p style="text-align: center;"><b>Programming Notes</b></p> <ul style="list-style-type: none"> <li>This per-instance value should specify a valid number of vertices for the primitive topology type. E.g., for 3DPRIM_TRILIST_ADJ, this field should specify a multiple of 6 vertices. However, in cases where too few or too many vertices are provided, the unused vertices will be silently discarded by the pipeline.</li> <li>A 0 value in this field effectively makes the command a 'no-operation'.</li> </ul>	Format:	U32 Count of vertices							
Format:	U32 Count of vertices									
3	<p>31:0 <b>Start Vertex Location</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32 structure index</td> </tr> </table> <p>This field specifies the "starting vertex" for each instance. This allows skipping over part of the vertices in a buffer if, for example, a previous 3DPRIMITIVE command had already drawn the primitives associated with the earlier entries. For SEQUENTIAL access, this field specifies, for each instance, a starting structure index into the vertex buffers For RANDOM access, this field specifies, for each instance, a starting index into the Index Buffer.</p>	Format:	U32 structure index							
Format:	U32 structure index									

		<b>3DPRIMITIVE</b>	
		<b>Programming Notes</b>	
		<ul style="list-style-type: none"> <li>• Access of any data outside of the valid extent of a vertex or index buffer will return the value 0 (i.e., appears as if the data stored at the invalid location was 0).</li> <li>• Must be set to 0 if End Offset Enable is ENABLED.</li> <li>• Ignored if Indirect Parameter Enable is ENABLED</li> </ul>	
4	31:0	<b>Instance Count</b>	
		Format:	U32 Count of instances
		<p>This field specifies the number of instances by which the primitive topology is to be regenerated. A value of 0 indicates "no instances" (no-op operation). A value of 1 effectively specifies "non-instanced" operation, though vertex buffers will still be used to provide instance data, if so programmed. Ignored if Indirect Parameter Enable is ENABLED.</p>	
		<b>Value</b>	<b>Name</b>
		[0, FFFFFFFFh]	
5	31:0	<b>Start Instance Location</b>	
		Format:	U32 structure index
		<b>Description</b>	
		<p>This field specifies the "starting instance" for the command as an initial structure index into Vertex Buffers for vertex elements with InstancingEnable set.</p> <p>Subsequent instances will access sequential instance data structures, as controlled by the Instance Data Step Rate.</p>	
		<b>Programming Notes</b>	
		<ul style="list-style-type: none"> <li>• Access of any data outside of the valid extent of a vertex or index buffer will return the value 0 (i.e., appears as if the data stored at the invalid location was 0).</li> <li>• Must be set to 0 if End Offset Enable is ENABLED.</li> <li>• Ignored if Indirect Parameter Enable is ENABLED.</li> </ul>	
6	31:0	<b>Base Vertex Location</b>	
		Format:	S31 index structure bias
		<p>This field specifies a signed bias to be added to values read from the index buffer. This allows the same index buffer values to access different vertex data for different commands. This field applies only to RANDOM access mode. This field is ignored for SEQUENTIAL access mode, where there Start Vertex Location can be used to specify different regions in the vertex buffers.</p>	
		<b>Programming Notes</b>	
		<ul style="list-style-type: none"> <li>• Access of any data outside of the valid extent of a vertex or index buffer will return the value 0 (i.e., appears as if the data stored at the invalid location was 0).</li> <li>• Must be set to 0 if End Offset Enable is ENABLED.</li> <li>• Ignored if Indirect Parameter Enable is ENABLED.</li> </ul>	

## 3DSTATE\_AA\_LINE\_PARAMETERS

3DSTATE_AA_LINE_PARAMETERS			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
<p>The 3DSTATE_AA_LINE_PARAMS command is used to specify the slope and bias terms used in the improved alpha coverage computation (specifically for DX WHQL compliance). Note that in these devices the coverage values passed to PS threads are full U0.8 values.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
Default Value:		1h 3DSTATE_NONPIPELINED	
Format:		OpCode	
23:16	<b>3D Command Sub Opcode</b>		
	Default Value:	0Ah 3DSTATE_AA_LINE_PARAMS	
	Format:	OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>Dword Length</b>		
	Default Value:	1h Excludes Dword (0,1)	
	Project:	All	
	Format:	=n Total Length - 2	
1	31:24	<b>AA Point Coverage Bias</b>	
		Project:	CHV, BSW
		Format:	U0.8
	<p>This field specifies the bias term to be used in the aa coverage computation for edges 0 and 3.</p>		
23:16	<b>AA Coverage Bias</b>		
	Project:	All	
	Format:	U0.8	

<b>3DSTATE_AA_LINE_PARAMETERS</b>					
	<p>This field specifies the bias term to be used in the aa coverage computation for edges 0 and 3.</p>				
15:8	<p><b>AA Point Coverage Slope</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U0.8</td> </tr> </table> <p>This field specifies the slope term to be used in the aa coverage computation for edges 0 and 3.If this field is zero, the Windower will revert to legacy aa line coverage computation (though still output expanded U0.8 coverage values).</p>	Project:	CHV, BSW	Format:	U0.8
	Project:	CHV, BSW			
Format:	U0.8				
7:0	<p><b>AA Coverage Slope</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.8</td> </tr> </table> <p>This field specifies the slope term to be used in the aa coverage computation for edges 0 and 3.If this field is zero, the Windower will revert to legacy aa line coverage computation (though still output expanded U0.8 coverage values).</p>	Project:	All	Format:	U0.8
	Project:	All			
Format:	U0.8				
2	<p>31:24 <b>AA Point Coverage EndCap Bias</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U0.8</td> </tr> </table> <p>This field specifies the bias term to be used in the aa coverage computation for edges 1 and 2.</p>	Project:	CHV, BSW	Format:	U0.8
	Project:	CHV, BSW			
	Format:	U0.8			
	<p>23:16 <b>AA Coverage EndCap Bias</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.8</td> </tr> </table> <p>This field specifies the bias term to be used in the aa coverage computation for edges 1 and 2.</p>	Project:	All	Format:	U0.8
Project:	All				
Format:	U0.8				
<p>15:8 <b>AA Point Coverage EndCap Slope</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U0.8</td> </tr> </table> <p>This field specifies the slope term to be used in the aa coverage computation for edges 1 and 2.</p>	Project:	CHV, BSW	Format:	U0.8	
Project:	CHV, BSW				
Format:	U0.8				
<p>7:0 <b>AA Coverage EndCap Slope</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.8</td> </tr> </table> <p>This field specifies the slope term to be used in the aa coverage computation for edges 1 and 2.</p>	Project:	All	Format:	U0.8	
Project:	All				
Format:	U0.8				

## 3DSTATE\_BINDING\_TABLE\_EDIT\_DS

3DSTATE_BINDING_TABLE_EDIT_DS			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
This command edits the binding table for DS.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		46h 3DSTATE_BINDING_TABLE_EDIT_DS	
Format:		OpCode	
15:9	<b>Reserved</b>		
	Format:	MBZ	
8:0	<b>DWord Length</b>		
	Format:	=n	
	<b>Value</b>	<b>Name</b>	
	0h	DWORD_COUNT_n <b>[Default]</b>	
	0h - 100h	Range	
1	31:16	<b>Binding Table Block Clear</b>	
		Format:	U16
	Each bit in this field corresponds to a 16 entry block of the binding table. Bit 0 of this field corresponds to entries 0-15, bit 1 to 16-31, and so on. When a bit is set it clears the corresponding bind table entries to 0. (effectively disabling them). The clear is applied before the individual binding table entries contained in this message are applied. When this bit is clear then the corresponding 16 entry block is not cleared.		
15:2	<b>Reserved</b>		
	Format:	MBZ	

<b>3DSTATE_BINDING_TABLE_EDIT_DS</b>																	
	1:0	<b>Binding Table Edit Target</b> Specifies which core should respond to this <b>3DSTATE_BINDING_TABLE_EDIT_DS</b> command:															
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td>11b</td> <td>All Cores</td> <td>All cores should respond to this command</td> </tr> <tr> <td>10b</td> <td>Core 1</td> <td>Only Core1 should respond to this command</td> </tr> <tr> <td>01b</td> <td>Core 0</td> <td>Only Core0 should respond to this command</td> </tr> <tr> <td>00b</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table>	Value	Name	Description	11b	All Cores	All cores should respond to this command	10b	Core 1	Only Core1 should respond to this command	01b	Core 0	Only Core0 should respond to this command	00b	Reserved	Reserved
		Value	Name	Description													
		11b	All Cores	All cores should respond to this command													
		10b	Core 1	Only Core1 should respond to this command													
01b	Core 0	Only Core0 should respond to this command															
00b	Reserved	Reserved															
2..n	31:0	<b>Entry [n]</b> Format:            BINDING_TABLE_EDIT_ENTRY [CHV, BSW]															



## 3DSTATE\_BINDING\_TABLE\_EDIT\_GS

3DSTATE_BINDING_TABLE_EDIT_GS			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
This command edits the binding table for GS.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		44h 3DSTATE_BINDING_TABLE_EDIT_GS	
Format:		OpCode	
15:9	<b>Reserved</b>		
	Format:	MBZ	
8:0	<b>DWord Length</b>		
	Format:	=n	
	<b>Value</b>	<b>Name</b>	
	0h	DWORD_COUNT_n <b>[Default]</b>	
	0h - 100h	Range	
1	31:16	<b>Binding Table Block Clear</b>	
		Format:	U16
	<p>Each bit in this field corresponds to a 16 entry block of the binding table. Bit 0 of this field corresponds to entries 0-15, bit 1 to 16-31, and so on. When a bit is set it clears the corresponding bind table entries to 0. (effectively disabling them). The clear is applied before the individual binding table entries contained in this message are applied. When this bit is clear then the corresponding 16 entry block is not cleared.</p>		
15:2	<b>Reserved</b>		
Format:	MBZ		

<b>3DSTATE_BINDING_TABLE_EDIT_GS</b>																	
	1:0	<b>Binding Table Edit Target</b> Specifies which core should respond to this <b>3DSTATE_BINDING_TABLE_EDIT_GS</b> command:															
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td>11b</td> <td>All Cores</td> <td>All cores should respond to this command</td> </tr> <tr> <td>10b</td> <td>Core 1</td> <td>Only Core1 should respond to this command</td> </tr> <tr> <td>01b</td> <td>Core 0</td> <td>Only Core0 should respond to this command</td> </tr> <tr> <td>00b</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table>	Value	Name	Description	11b	All Cores	All cores should respond to this command	10b	Core 1	Only Core1 should respond to this command	01b	Core 0	Only Core0 should respond to this command	00b	Reserved	Reserved
		Value	Name	Description													
		11b	All Cores	All cores should respond to this command													
		10b	Core 1	Only Core1 should respond to this command													
01b	Core 0	Only Core0 should respond to this command															
00b	Reserved	Reserved															
2..n	31:0	<b>Entry [n]</b> Format:            BINDING_TABLE_EDIT_ENTRY [CHV, BSW]															

## 3DSTATE\_BINDING\_TABLE\_EDIT\_HS

3DSTATE_BINDING_TABLE_EDIT_HS			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
This command edits the binding table for HS.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		45h 3DSTATE_BINDING_TABLE_EDIT_HS	
Format:		OpCode	
15:9	<b>Reserved</b>		
	Format:	MBZ	
8:0	<b>DWord Length</b>		
	Format:	=n	
	<b>Value</b>	<b>Name</b>	
	0h	DWORD_COUNT_n <b>[Default]</b>	
	0h - 100h	Range	
1	31:16	<b>Binding Table Block Clear</b>	
		Format:	U16
	<p>Each bit in this field corresponds to a 16 entry block of the binding table. Bit 0 of this field corresponds to entries 0-15, bit 1 to 16-31, and so on. When a bit is set it clears the corresponding bind table entries to 0. (effectively disabling them). The clear is applied before the individual binding table entries contained in this message are applied. When this bit is clear then the corresponding 16 entry block is not cleared.</p>		
15:2	<b>Reserved</b>		
	Format:	MBZ	

<b>3DSTATE_BINDING_TABLE_EDIT_HS</b>																	
	1:0	<b>Binding Table Edit Target</b> Specifies which core should respond to this <b>3DSTATE_BINDING_TABLE_EDIT_HS</b> command:															
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td>11b</td> <td>All Cores</td> <td>All cores should respond to this command</td> </tr> <tr> <td>10b</td> <td>Core 1</td> <td>Only Core1 should respond to this command</td> </tr> <tr> <td>01b</td> <td>Core 0</td> <td>Only Core0 should respond to this command</td> </tr> <tr> <td>00b</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table>	Value	Name	Description	11b	All Cores	All cores should respond to this command	10b	Core 1	Only Core1 should respond to this command	01b	Core 0	Only Core0 should respond to this command	00b	Reserved	Reserved
		Value	Name	Description													
		11b	All Cores	All cores should respond to this command													
		10b	Core 1	Only Core1 should respond to this command													
01b	Core 0	Only Core0 should respond to this command															
00b	Reserved	Reserved															
2..n	31:0	<b>Entry [n]</b> Format:            BINDING_TABLE_EDIT_ENTRY [CHV, BSW]															

## 3DSTATE\_BINDING\_TABLE\_EDIT\_PS

3DSTATE_BINDING_TABLE_EDIT_PS			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
This command edits the binding table for PS.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		47h 3DSTATE_BINDING_TABLE_EDIT_PS	
Format:		OpCode	
15:9	<b>Reserved</b>		
	Format:	MBZ	
8:0	<b>DWord Length</b>		
	Format:	=n	
	<b>Value</b>	<b>Name</b>	
	0h	DWORD_COUNT_n <b>[Default]</b>	
	0h - 100h	Range	
1	31:16	<b>Binding Table Block Clear</b>	
		Format:	U16
	<p>Each bit in this field corresponds to a 16 entry block of the binding table. Bit 0 of this field corresponds to entries 0-15, bit 1 to 16-31, and so on. When a bit is set it clears the corresponding bind table entries to 0. (effectively disabling them). The clear is applied before the individual binding table entries contained in this message are applied. When this bit is clear then the corresponding 16 entry block is not cleared.</p>		
15:2	<b>Reserved</b>		
	Format:	MBZ	

<b>3DSTATE_BINDING_TABLE_EDIT_PS</b>																	
	1:0	<b>Binding Table Edit Target</b> Specifies which core should respond to this <b>3DSTATE_BINDING_TABLE_EDIT_PS</b> command:															
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td>11b</td> <td>All Cores</td> <td>All cores should respond to this command</td> </tr> <tr> <td>10b</td> <td>Core 1</td> <td>Only Core1 should respond to this command</td> </tr> <tr> <td>01b</td> <td>Core 0</td> <td>Only Core0 should respond to this command</td> </tr> <tr> <td>00b</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table>	Value	Name	Description	11b	All Cores	All cores should respond to this command	10b	Core 1	Only Core1 should respond to this command	01b	Core 0	Only Core0 should respond to this command	00b	Reserved	Reserved
		Value	Name	Description													
		11b	All Cores	All cores should respond to this command													
		10b	Core 1	Only Core1 should respond to this command													
01b	Core 0	Only Core0 should respond to this command															
00b	Reserved	Reserved															
2..n	31:0	<b>Entry [n]</b> Format:            BINDING_TABLE_EDIT_ENTRY [CHV, BSW]															

## 3DSTATE\_BINDING\_TABLE\_EDIT\_VS

3DSTATE_BINDING_TABLE_EDIT_VS			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
This command edits the binding table for VS. The 3DSTATE_BINDING_TABLE_EDIT_VS is a variable length command.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		43h 3DSTATE_BINDING_TABLE_EDIT_VS	
Format:		OpCode	
15:9	<b>Reserved</b>		
	Format:	MBZ	
8:0	<b>DWord Length</b>		
	Format:	=n	
	<b>Value</b>	<b>Name</b>	
	0h	DWORD_COUNT_n [Default]	
	0h - 100h	Range	
1	31:16	<b>Binding Table Block Clear</b>	
		Format:	U16
	Each bit in this field corresponds to a 16 entry block of the binding table. Bit 0 of this field corresponds to entries 0-15, bit 1 to 16-31, and so on. When a bit is set it clears the corresponding bind table entries to 0. (affectively disabling them). The clear is applied before the individual binding table entries contained in this message are applied. When this bit is clear then the corresponding 16 entry block is not cleared.		
15:2	<b>Reserved</b>		
Format:		MBZ	

<b>3DSTATE_BINDING_TABLE_EDIT_VS</b>																	
	1:0	<b>Binding Table Edit Target</b> Specifies which core should respond to this <b>3DSTATE_BINDING_TABLE_EDIT_VS</b> command:															
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td>11b</td> <td>All Cores</td> <td>All cores should respond to this command</td> </tr> <tr> <td>10b</td> <td>Core 1</td> <td>Only Core1 should respond to this command</td> </tr> <tr> <td>01b</td> <td>Core 0</td> <td>Only Core0 should respond to this command</td> </tr> <tr> <td>00b</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table>	Value	Name	Description	11b	All Cores	All cores should respond to this command	10b	Core 1	Only Core1 should respond to this command	01b	Core 0	Only Core0 should respond to this command	00b	Reserved	Reserved
		Value	Name	Description													
		11b	All Cores	All cores should respond to this command													
		10b	Core 1	Only Core1 should respond to this command													
01b	Core 0	Only Core0 should respond to this command															
00b	Reserved	Reserved															
2..n	31:0	<b>Entry [n]</b> Format:            BINDING_TABLE_EDIT_ENTRY [CHV, BSW]															



## 3DSTATE\_BINDING\_TABLE\_POINTERS\_DS

3DSTATE_BINDING_TABLE_POINTERS_DS			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
The 3DSTATE_BINDING_TABLE_POINTERS_DS command is used to define the location of fixed functions' BINDING_TABLE_STATE. Only some of the fixed functions utilize binding tables.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		28h 3DSTATE_BINDING_TABLE_POINTERS_DS	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	0h DWORD_COUNT_n	
	Project:	All	
	Format:	=n	
1	31:16	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	15:5	<b>Pointer to DS Binding Table</b>	
		Project:	CHV, BSW
		Format:	SurfaceStateOffset[15:5]BINDING_TABLE_STATE*256 When HW binding table is disabled
		Format:	SurfaceStateOffset[16:6]BINDING_TABLE_STATE*256 When HW-generated binding table is enabled

<b>3DSTATE_BINDING_TABLE_POINTERS_DS</b>						
		Specifies an aligned address offset of the function's BINDING_TABLE_STATE. The offset's base and alignment differ depending on whether HW Binding Table is enabled: If HW Binding Table is disabled, the offset is relative to <b>Surface State Base Address</b> and the alignment is <b>32B</b> . If HW Binding Table is enabled the offset is relative to the <b>Binding Table Pool Base Address</b> and the alignment is <b>64B</b> .				
	4:0	<b>Reserved</b>				
		<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ
Project:	All					
Format:	MBZ					

## 3DSTATE\_BINDING\_TABLE\_POINTERS\_GS

3DSTATE_BINDING_TABLE_POINTERS_GS			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
The 3DSTATE_BINDING_TABLE_POINTERS_GS command is used to define the location of fixed functions' BINDING_TABLE_STATE. Only some of the fixed functions utilize binding tables.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		29h 3DSTATE_BINDING_TABLE_POINTERS_GS	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	0h DWORD_COUNT_n	
	Project:	All	
	Format:	=n	
1	31:16	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	15:5	<b>Pointer to GS Binding Table</b>	
		Project:	CHV, BSW
		Format:	SurfaceStateOffset[15:5]BINDING_TABLE_STATE*256 When HW binding table is disabled
		Format:	SurfaceStateOffset[16:6]BINDING_TABLE_STATE*256 When HW-generated binding table is enabled

### 3DSTATE\_BINDING\_TABLE\_POINTERS\_GS

		Specifies an aligned address offset of the function's BINDING_TABLE_STATE. The offset's base and alignment differ depending on whether HW Binding Table is enabled: If HW Binding Table is disabled, the offset is relative to <b>Surface State Base Address</b> and the alignment is <b>32B</b> . If HW Binding Table is enabled the offset is relative to the <b>Binding Table Pool Base Address</b> and the alignment is <b>64B</b> .	
	4:0	<b>Reserved</b>	
		Project:	All
		Format:	MBZ

## 3DSTATE\_BINDING\_TABLE\_POINTERS\_HS

3DSTATE_BINDING_TABLE_POINTERS_HS			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
The 3DSTATE_BINDING_TABLE_POINTERS_HS command is used to define the location of fixed functions' BINDING_TABLE_STATE. Only some of the fixed functions utilize binding tables.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		27h 3DSTATE_BINDING_TABLE_POINTERS_HS	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	0h DWORD_COUNT_n	
	Project:	All	
	Format:	=n	
1	31:16	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	15:5	<b>Pointer to HS Binding Table</b>	
		Project:	CHV, BSW
		Format:	SurfaceStateOffset[15:5]BINDING_TABLE_STATE*256 When HW binding table is disabled
	Format:	SurfaceStateOffset[16:6]BINDING_TABLE_STATE*256 When HW-generated binding table is enabled	

### 3DSTATE\_BINDING\_TABLE\_POINTERS\_HS

		Specifies an aligned address offset of the function's BINDING_TABLE_STATE. The offset's base and alignment differ depending on whether HW Binding Table is enabled: If HW Binding Table is disabled, the offset is relative to <b>Surface State Base Address</b> and the alignment is <b>32B</b> . If HW Binding Table is enabled the offset is relative to the <b>Binding Table Pool Base Address</b> and the alignment is <b>64B</b> .	
	4:0	<b>Reserved</b>	
		Project:	All
		Format:	MBZ

## 3DSTATE\_BINDING\_TABLE\_POINTERS\_PS

3DSTATE_BINDING_TABLE_POINTERS_PS			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
The 3DSTATE_BINDING_TABLE_POINTERS_PS command is used to define the location of fixed functions' BINDING_TABLE_STATE. Only some of the fixed functions utilize binding tables.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		2Ah 3DSTATE_BINDING_TABLE_POINTERS_PS	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	0h DWORD_COUNT_n	
	Project:	All	
	Format:	=n	
1	31:16	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	15:5	<b>Pointer to PS Binding Table</b>	
		Project:	CHV, BSW
		Format:	SurfaceStateOffset[15:5]BINDING_TABLE_STATE*256 When HW binding table is disabled
		Format:	SurfaceStateOffset[16:6]BINDING_TABLE_STATE*256 When HW-generated binding table is enabled

<b>3DSTATE_BINDING_TABLE_POINTERS_PS</b>						
		Specifies an aligned address offset of the function's BINDING_TABLE_STATE. The offset's base and alignment differ depending on whether HW Binding Table is enabled: If HW Binding Table is disabled, the offset is relative to <b>Surface State Base Address</b> and the alignment is <b>32B</b> . If HW Binding Table is enabled the offset is relative to the <b>Binding Table Pool Base Address</b> and the alignment is <b>64B</b> .				
	4:0	<b>Reserved</b>				
		<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ
Project:	All					
Format:	MBZ					



## 3DSTATE\_BINDING\_TABLE\_POINTERS\_VS

3DSTATE_BINDING_TABLE_POINTERS_VS			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
The 3DSTATE_BINDING_TABLE_POINTERS_VS command is used to define the location of fixed functions' BINDING_TABLE_STATE. Only some of the fixed functions utilize binding tables.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		26h 3DSTATE_BINDING_TABLE_POINTERS_VS	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	0h DWORD_COUNT_n	
	Project:	All	
	Format:	=n	
1	31:16	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	15:5	<b>Pointer to VS Binding Table</b>	
		Project:	CHV, BSW
Format:		SurfaceStateOffset[15:5]BINDING_TABLE_STATE*256 When HW binding table is disabled	
	Format:	SurfaceStateOffset[16:6]BINDING_TABLE_STATE*256 When HW-generated binding table is enabled	

### 3DSTATE\_BINDING\_TABLE\_POINTERS\_VS

		Specifies an aligned address offset of the function's BINDING_TABLE_STATE. The offset's base and alignment differ depending on whether HW Binding Table is enabled: If HW Binding Table is disabled, the offset is relative to <b>Surface State Base Address</b> and the alignment is <b>32B</b> . If HW Binding Table is enabled the offset is relative to the <b>Binding Table Pool Base Address</b> and the alignment is <b>64B</b> .	
	4:0	<b>Reserved</b>	
		Project:	All
		Format:	MBZ

## 3DSTATE\_BINDING\_TABLE\_POOL\_ALLOC

3DSTATE_BINDING_TABLE_POOL_ALLOC			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
This command sets up the binding table pool for HW generated binding tables.			
<b>Programming Notes</b>			
When RS is enabled due to a MI_RS_CONTROL or MI_BATCH_BUFFER_START with RS enable bit set, driver must reprogram the 3DSTATE_BINDING_TABLE_POOL_ALLOC to ensure the resource streamer and render engine are in sync with the programming with the command. Otherwise there could be cases where RS sees that the Binding Table Pool is disabled while the render pipeline sees the binding table is enabled in the case the 3DSTATE_BINDING_TABLE_POOL_ALLOC was enabled while RS was off.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	1h 3DSTATE_NONPIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		19h 3DSTATE_BINDING_TABLE_POOL_ALLOC	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>	Project:	All
		Format:	=n
	<b>Value</b>	<b>Name</b>	<b>Project</b>
	2h	DWORD_COUNT_n [Default]	CHV, BSW
1..2 <b>Project:</b> CHV,	63:12	<b>Binding Table Pool Base Address</b>	
	Project:	CHV, BSW	

<b>3DSTATE_BINDING_TABLE_POOL_ALLOC</b>																					
BSW		<table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[63:12]BindingTablePool</td> </tr> </table> <p>This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space.</p>	Format:	GraphicsAddress[63:12]BindingTablePool																	
	Format:	GraphicsAddress[63:12]BindingTablePool																			
	11	<p><b>Binding Table Pool Enable</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>When this bit is set it enables HW generation of binding tables. When this bit is cleared it disables HW generation of binding tables.</p>	Project:	CHV, BSW	Format:	U1															
	Project:	CHV, BSW																			
	Format:	U1																			
10	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table>	Project:	CHV, BSW																		
Project:	CHV, BSW																				
9:7	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table>	Project:	CHV, BSW																		
Project:	CHV, BSW																				
6:0	<p><b>Surface Object Control State</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MEMORY_OBJECT_CONTROL_STATE</td> </tr> </table> <p>Specifies the memory object control state for this surface.</p> <table border="1" style="background-color: #e6f2ff;"> <tr> <th colspan="3" style="text-align: center;">Programming Notes</th> </tr> <tr> <td colspan="3">Bit 2 is not programmable and is always zero.</td> </tr> </table>	Project:	CHV, BSW	Format:	MEMORY_OBJECT_CONTROL_STATE	Programming Notes			Bit 2 is not programmable and is always zero.												
Project:	CHV, BSW																				
Format:	MEMORY_OBJECT_CONTROL_STATE																				
Programming Notes																					
Bit 2 is not programmable and is always zero.																					
3 Project: CHV, BSW	31:12	<p><b>Binding Table Pool Buffer Size</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U20</td> </tr> </table> <p>This field specifies the size of the buffer in 4K pages. Any access which straddle or go past the end of the buffer will return 0.</p> <table border="1" style="background-color: #e6f2ff;"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[0,1048575]</td> <td></td> <td></td> </tr> <tr> <td>0</td> <td>No Valid Data</td> <td>There is no valid data in the buffer</td> </tr> </tbody> </table> <table border="1" style="background-color: #e6f2ff;"> <tr> <th colspan="3" style="text-align: center;">Restriction</th> </tr> <tr> <td colspan="3">Programming size of zero is illegal in the case that the pool is enabled.</td> </tr> </table>	Project:	CHV, BSW	Format:	U20	Value	Name	Description	[0,1048575]			0	No Valid Data	There is no valid data in the buffer	Restriction			Programming size of zero is illegal in the case that the pool is enabled.		
	Project:	CHV, BSW																			
	Format:	U20																			
	Value	Name	Description																		
	[0,1048575]																				
0	No Valid Data	There is no valid data in the buffer																			
Restriction																					
Programming size of zero is illegal in the case that the pool is enabled.																					
11	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ																
Project:	CHV, BSW																				
Format:	MBZ																				
10:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ																
Project:	CHV, BSW																				
Format:	MBZ																				

## 3DSTATE\_BLEND\_STATE\_POINTERS

<b>3DSTATE_BLEND_STATE_POINTERS</b>			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
The 3DSTATE_BLEND_STATE_POINTERS command is used to set up the pointers to the color calculator state.			
<b>Programming Notes</b>			
When the BLEND_STATE pointer changes but not the CC_STATE pointer, driver needs to force a CC_STATE pointer change to improve blend performance in pixel backend.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
Default Value:		0h 3DSTATE_PIPELINED	
Format:		OpCode	
23:16	<b>3D Command Sub Opcode</b>		
	Default Value:	24h 3DSTATE_BLEND_STATE_POINTERS	
	Format:	OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	0h DWORD_COUNT_n	
	Project:	All	
	Format:	=n	
1	31:6	<b>Blend State Pointer</b>	
		Project:	All
	Format:	DynamicStateOffset[31:6]BLEND_STATE*8	
Specifies the 64-byte aligned offset of the BLEND_STATE. This offset is relative to the <b>Dynamic State Base Address</b> .			
	5:1	<b>Reserved</b>	

<b>3DSTATE_BLEND_STATE_POINTERS</b>		
		Project: All
		Format: MBZ
	0	<b>Blend State Pointer Valid</b>
		Project: CHV, BSW
		Format: Enable
		This bit, if set, indicates that the BLEND_STATE pointer has changed and new state needs to be fetched.

## 3DSTATE\_CC\_STATE\_POINTERS

DWord		Bit	Description
<b>3DSTATE_CC_STATE_POINTERS</b>			
Project:		CHV, BSW	
Source:		RenderCS	
Length Bias:		2	
The 3DSTATE_CC_STATE_POINTERS command is used to set up the pointers to the color calculator state.			
<b>Programming Notes</b>			
When the CC_STATE pointer changes but not the BLEND_STATE pointer, driver needs to force a BLEND_STATE pointer change in order to improve blend performance in the pixel backend.			
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
		Default Value:	0Eh 3DSTATE_CC_STATE_POINTERS
		Format:	OpCode
	15:8	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	7:0	<b>DWord Length</b>	
		Default Value:	0h DWORD_COUNT_n
		Project:	All
		Format:	=n
1	31:6	<b>Color Calc State Pointer</b>	
		Project:	All
		Format:	DynamicStateOffset[31:6]COLOR_CALC_STATE
		Specifies the 64-byte aligned offset of the COLOR_CALC_STATE. This offset is relative to the <b>Dynamic State Base Address</b> .	
	5:1	<b>Reserved</b>	

<b>3DSTATE_CC_STATE_POINTERS</b>					
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ
Project:	All				
Format:	MBZ				
0	<p><b>Color Calc State Pointer Valid</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>If set, the hardware will fetch the CC state. This bit is context saved and restored so the CC state is considered undefined once this bit is cleared due to the possibility of the CC state changing between context switches.</p>	Project:	CHV, BSW	Format:	Enable
Project:	CHV, BSW				
Format:	Enable				



## 3DSTATE\_CHROMA\_KEY

3DSTATE_CHROMA_KEY					
Project:	CHV, BSW				
Source:	RenderCS				
Length Bias:	2				
<p>The 3DSTATE_CHROMA_KEY instruction is used to program texture color/chroma-key key values. A table containing four set of values is supported. The ChromaKey Index sampler state variable is used to select which table entry is associated with the map. Texture chromakey functions are enabled and controlled via use of the ChromaKey Enable texture sampler state variable. Texture Color Key (keying on a paletted texture index) is not supported.</p>					
DWord	Bit	Description			
0	31:29	<b>Command Type</b>			
		Default Value: 3h GFXPIPE Format: Opcode			
	28:27	<b>Command SubType</b>			
		Default Value: 3h GFXPIPE_3D Format: Opcode			
	26:24	<b>3D Command Opcode</b>			
		Default Value: 1h 3DSTATE_NONPIPELINED Format: Opcode			
	23:16	<b>3D Command Sub Opcode</b>			
Default Value: 04h 3DSTATE_CHROMA_KEY Format: Opcode					
15:8	<b>Reserved</b>				
	Project: All Format: MBZ				
7:0	<b>DWord Length</b>				
	Default Value: 2h Excludes DWord (0,1) Format: =n				
	Total Length - 2				
1	31:30	<b>ChromaKey Table Index</b>			
		Project: All Format: U2 index			
	Selects which entry in the ChromaKey table is to be loaded				
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>[0,3]</td> <td></td> </tr> </tbody> </table>	Value	Name	[0,3]
Value	Name				
[0,3]					

		<b>3DSTATE_CHROMA_KEY</b>			
	29:0	<b>Reserved</b>			
		Project:	All		
		Format:	MBZ		
2	31:0	<b>ChromaKey Low Value</b> This field specifies the "low" (minimum) value of the chroma key range. Texel samples are considered "matching the key" if each component of the texel falls within the (inclusive) chroma range. See ChromaKey High Value for further format, programming info.			
3	31:0	<b>ChromaKey High Value</b> This field specifies the "high" (maximum) value of the chroma key range. Texel samples are considered "matching the key" if each component of the texel falls within the (inclusive) chroma range.			
		<b>Programming Notes</b>			
		ChromaKey values are specified using 8-bit channels. When using surface formats with less than 8 bits per channel, the device will expand channels by replicating the required number of MSBs into the LSBs of each channel. Software must account for this conversion when it programs Chromakey Low/High Values (e.g., by performing the same replication).			
		For channels that do not exist in the actual surface (e.g., Alpha channel for non-ARGB maps), software must explicitly program full range high/low values (High=FFh, Low=0h for formats using unsigned chroma key values, High=7Fh, Low=FFh for formats using sign magnitude chroma key values) in order to effectively remove the comparison of that field from the ChromaKey function.			
		For channels in SNORM format in the surface format, the value in the high/low value for that channel is interpreted in sign magnitude format. Negative zero value is not supported (use positive zero instead). For channels with mixed UNORM/SNORM formats (i.e. R5G5_SNORM_B6_UNORM), the ChromaKey is programmed as if all channels are SNORM.			
		YUV ChromaKey will use an interpolated chrominance value from the map for comparison to the chroma key values for those texels without chrominance due to downsampling. The chrominance value used is the average of values to the left and right of the texel in question.			
		It is UNDEFINED to program any component of the ChromaKey High Value to be less than the corresponding component of ChromaKey Low Value.			
		Format = interpreted according to associated texel format "class":			
		Only the surface formats listed as supported for chroma key in the surface formats table can be used with this feature. Use of any other surface format with chroma key enabled is UNDEFINED.			
		<b>Surface Format</b>	<b>31:24</b>	<b>23:15</b>	<b>16:8</b> <b>7:0</b>
		ARGB and BC (DXT) formats	A	R	G   B
		YCrCb formats	A	Cr	Y   Cb

## 3DSTATE\_CLEAR\_PARAMS

3DSTATE_CLEAR_PARAMS		
Project:	CHV, BSW	
Source:	RenderCS	
Length Bias:	2	
Description		Project
This command defines the depth clear value delivered as a pipelined state command. However, the state change pipelining isn't completely transparent (see restriction below).		
HW will internally manage the draining pipe and flushing of the caches when this command is issued. The PIPE_CONTROL restrictions are removed.		CHV, BSW
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 3h GFXPIPE Format: OpCode
	28:27	<b>Command SubType</b>
		Default Value: 3h GFXPIPE_3D Format: OpCode
	26:24	<b>3D Command Opcode</b>
		Default Value: 0h 3DSTATE_PIPELINED Format: OpCode
	23:16	<b>3D Command Sub Opcode</b>
Default Value: 04h 3DSTATE_CLEAR_PARAMS Format: OpCode		
15:8	<b>Reserved</b>	
	Format: MBZ	
7:0	<b>Dword Length</b>	
	Default Value: 1h Excludes Dword (0,1) Format: =n Total Length - 2	
1	31:0	<b>Depth Clear Value</b>
		Project: CHV, BSW Format: IEEE_Float
	This field defines the clear value that will be applied to the depth buffer if the Depth Buffer Clear field is enabled. It is valid only if Depth Buffer Clear Value Valid is set.	
	<p style="text-align: center;"><b>Programming Notes</b></p> The clear value must be between the min and max depth values (inclusive) defined in the CC_VIEWPORT. If the depth buffer format is D32_FLOAT, then values must be limited to the	

<b>3DSTATE_CLEAR_PARAMS</b>		
		range of +0.0f and 1.0f inclusive; values outside this range are reserved.
2	31:1	<b>Reserved</b> Format: <span style="float: right;">MBZ</span>
	0	<b>Depth Clear Value Valid</b> Format: <span style="float: right;">Boolean</span> This field enables the <b>Depth Clear Value</b> . If clear, the depth clear value is obtained from interpolated depth of an arbitrary pixel of the primitive rendered with <b>Depth Buffer Clear</b> set in WM_STATE or 3DSTATE_WM. If set, the depth clear value is obtained from the <b>Depth Clear Value</b> field of this command.

## 3DSTATE\_CLIP

3DSTATE_CLIP			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		12h 3DSTATE_CLIP	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>	Default Value:	02h Excludes DWord (0,1)
		Project:	All
		Format:	=n
		Total Length - 2	
1	31:21	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	20	<b>Force User Clip Distance Cull Test Enable Bitmask</b>	
		Project:	All
Format:		Enable	
This field provides a work around override for the computation of SOL_INT::Render_Enable			
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0h	Normal	Clip_INT::User Clip Distance Cull Test Enable Bitmask normally

<b>3DSTATE_CLIP</b>			
	1h	Force	Forces Clip_INT::User Clip Distance Cull Test Enable Bitmask to use the value in 3DSTATE_CLIP:: User Clip Distance Cull Test Enable Bitmask
19	<b>Vertex Sub Pixel Precision Select</b>		
	Project:		All
	Format:		U1
	Selects the number of fractional bits maintained in the vertex data		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
			<b>Project</b>
	0h	8 Bit	8 sub pixel precision bits maintained
	1h	4 Bit	4 sub pixel precision bits maintained
			All
			All
18	<b>Early Cull Enable</b>		
	Project:		All
	Format:		Enable
	This field is used to enable/disable the EarlyCull function.		
17	<b>Force User Clip Distance Clip Test Enable Bitmask</b>		
	Project:		All
	Format:		Enable
	This field provides a work around override for the computation of SOL_INT::Render_Enable.		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
			<b>Project</b>
	0b	Normal	Clip_INT:: User Clip Distance Clip Test Enable Bitmask normally
	1b	Force	Forces Clip_INT:: User Clip Distance Clip Test Enable Bitmask to use the value in 3DSTATE_CLIP::User Clip Distance Clip Test Enable Bitmask
			All
			All
16	<b>Force Clip Mode</b>		
	Format:		Enable
	This field provides a work around override for the computation of SOL_INT::Render_Enable.		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
			<b>Project</b>
	0b	Normal	Clip_INT::Clip Mode is computed normally.
	1b	Force	Forces Clip_INT::Clip Mode to use the value in 3DSTATE_CLIP::User Clip Mode.
			All
			All
15:11	<b>Reserved</b>		
	Project:		All
	Format:		MBZ
10	<b>Clipper Statistics Enable</b>		
	Project:		All
	Format:		Enable
	This bit controls whether Clip-unit-specific statistics register(s) can be incremented.		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
			<b>Project</b>

<b>3DSTATE_CLIP</b>														
		0h	Disable	CL_INVOCATIONS_COUNT cannot increment	All									
		1h	Enable	CL_INVOCATIONS_COUNT can increment	All									
	9:8	<b>Reserved</b>												
		Project:												
		Format:		MBZ										
	7:0	<b>User Clip Distance Cull Test Enable Bitmask</b>												
		Project:		All										
		Format:		Enable[8]										
	<p>This 8 bit mask field selects which of the 8 user clip distances against which trivial reject / trivial accept determination needs to be made (does not cause a must clip).DX10 allows simultaneous use of ClipDistance and Cull Distance test of up to 8 distances.</p>													
	2	31	<b>Clip Enable</b>											
		Project:		All										
		Format:		Enable										
<p>Specifies whether the Clip function is enabled or disabled (pass-through).</p>														
30		<b>API Mode</b>												
		Project:		All										
<p>Controls the definition of the NEAR clipping plane</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 50%;">Description</th> <th style="width: 20%;">Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>OGL</td> <td>NEAR VP boundary == 0.0 (NDC)</td> <td>All</td> </tr> </tbody> </table>						Value	Name	Description	Project	0h	OGL	NEAR VP boundary == 0.0 (NDC)	All	
Value		Name	Description	Project										
0h		OGL	NEAR VP boundary == 0.0 (NDC)	All										
29		<b>Reserved</b>												
	Project:		All											
	Format:		MBZ											
28	<b>Viewport XY Clip Test Enable</b>													
	Project:		All											
	Format:		Enable											
<p>This field is used to control whether the Viewport X, Y extents are considered in VertexClipTest. See Tristrip Clipping subsection.</p>														
27	<b>Reserved</b>													
	Project:		All											
	Format:		MBZ											
26	<b>Guardband Clip Test Enable</b>													
	Project:		All											
	Format:		Enable											
<p>This field is used to control whether the Guardband X, Y extents are considered in VertexClipTest</p>														

<b>3DSTATE_CLIP</b>			
		for non-point objects. If the Guardband ClipTest is DISABLED but the Viewport XY ClipTest is ENABLED, ClipDetermination operates as if the Guardband were coincident with the Viewport. If both the Guardband and Viewport XY ClipTest are DISABLED, all vertices are considered "visible" with respect to the XY directions.	
25:24	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
23:16	<b>User Clip Distance Clip Test Enable Bitmask</b>		
	Project:	All	
	Format:	Enable[8]	
	This 8 bit mask field selects which of the 8 user clip distances against which trivial reject / trivial accept / must clip determination needs to be made. DX10 allows simultaneous use of ClipDistance and Cull Distance test of up to 8 distances.		
15:13	<b>Clip Mode</b>		
	Project:	All	
	This field specifies a general mode of the CLIP unit, when the CLIP unit is ENABLED.		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0h	NORMAL	TrivialAccept objects are passed down the pipeline, MustClip objects Clipped in the Fixed Function Clipper HW, TrivialReject and BAD objects are discarded
	1h	Reserved	
	2h	Reserved	
	3h	REJECT_ALL	All objects are discarded
	4h	ACCEPT_ALL	All objects (except BAD objects) are trivially accepted. This effectively disables the clip-test/clip-determination function. Note that the CLIP unit will still filter out adjacency information, which may be required since the SF unit does not accept primitives with adjacency.
	5h-7h	Reserved	
			All
12:10	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
9	<b>Perspective Divide Disable</b>		
	Project:	All	
	Format:	Disable	
	This field disables the Perspective Divide function performed on homogeneous position read from the URB. This feature can be used by software to submit pre-transformed "screen-space" geometry for rasterization. This likely requires the W component of positions to contain "rhw"		



### 3DSTATE\_CLIP

	<p>(aka 1/w) in order to support perspective-correct interpolation of vertex attributes. Likewise, the X, Y, Z components will likely be required to be X/W, Y/W, Z/W. Note that the device does not support clipping when perspective divide is disabled. Software must specify CLIPMODE_ACCEPT_ALL whenever it disables perspective divide. This implies that software must ensure that object positions are completely contained within the "guardband" screen-space limits imposed by the SF unit (e.g., by clipping in CPU SW before submitting the objects).</p>																				
8	<p><b>Non-Perspective Barycentric Enable</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field enables computation of non-perspective barycentric parameters in the clipper, which are sent to SF unit in the must clip case. This field must be enabled if any non-perspective barycentric parameters are enabled in the Windower.</p>		Project:	All	Format:	Enable															
Project:	All																				
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7:6	<p><b>Reserved</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>		Project:	All	Format:	MBZ															
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5:4	<p><b>Triangle Strip/List Provoking Vertex Select</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U2</td> </tr> </table> <p>enumerated type</p> <p>This field selects which vertex of a triangle (in a triangle strip or list primitive) is considered the "provoking vertex".</p> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr style="background-color: #e1eef6;"> <th style="width: 33%;">Value</th> <th style="width: 33%;">Name</th> <th style="width: 33%;">Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>0</td> <td>All</td> </tr> <tr> <td>1h</td> <td>1</td> <td>All</td> </tr> <tr> <td>2h</td> <td>2</td> <td>All</td> </tr> <tr> <td>3h</td> <td>Reserved</td> <td>All</td> </tr> </tbody> </table>		Project:	All	Format:	U2	Value	Name	Project	0h	0	All	1h	1	All	2h	2	All	3h	Reserved	All
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Value	Name	Project																			
0h	0	All																			
1h	1	All																			
2h	2	All																			
3h	Reserved	All																			
3:2	<p><b>Line Strip/List Provoking Vertex Select</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U2</td> </tr> </table> <p>enumerated type</p> <p>This field selects which vertex of a line (in a line strip or list primitive) is considered the "provoking vertex".</p> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr style="background-color: #e1eef6;"> <th style="width: 33%;">Value</th> <th style="width: 33%;">Name</th> <th style="width: 33%;">Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>0</td> <td>All</td> </tr> </tbody> </table>		Project:	All	Format:	U2	Value	Name	Project	0h	0	All									
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2h	Reserved	All																			
3h	Reserved	All																			
	1:0	<p><b>Triangle Fan Provoking Vertex Select</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U2</td> </tr> </table> <p>enumerated type</p> <p>This field selects which vertex of a triangle (in a triangle fan primitive) is considered the "provoking vertex".</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>0</td> <td>All</td> </tr> <tr> <td>1h</td> <td>1</td> <td>All</td> </tr> <tr> <td>2h</td> <td>2</td> <td>All</td> </tr> <tr> <td>3h</td> <td>Reserved</td> <td>All</td> </tr> </tbody> </table>	Project:	All	Format:	U2	Value	Name	Project	0h	0	All	1h	1	All	2h	2	All	3h	Reserved	All
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Value	Name	Project																			
0h	0	All																			
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2h	2	All																			
3h	Reserved	All																			
3	31:28	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ															
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	27:17	<p><b>Minimum Point Width</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U8.3 pixels</td> </tr> </table> <p>This value is used to clamp read-back PointWidth values.</p>	Project:	All	Format:	U8.3 pixels															
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	16:6	<p><b>Maximum Point Width</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U8.3 pixels</td> </tr> </table> <p>This value is used to clamp read-back PointWidth values.</p>	Project:	All	Format:	U8.3 pixels															
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	5	<p><b>Force Zero RTA Index Enable</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>If set, the Clip unit will ignore the read-back RTAIndex and operate as if the value 0 was read-back. If clear, the read-back value is used.</p>	Project:	All	Format:	Enable															
Project:	All																				
Format:	Enable																				
	4	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ															
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<b>3DSTATE_CLIP</b>					
3:0	<p><b>Maximum VP Index</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U4-1 index value (# of viewports)</td> </tr> </table> <p>This field specifies the maximum valid VPIndex value, corresponding to the number of active viewports. If the source of the VPIndex exceeds this maximum value, a VPIndex value of 0 is passed down the pipeline. Note that this clamping does not affect a VPIndex value stored in the URB.</p>	Project:	All	Format:	U4-1 index value (# of viewports)
Project:	All				
Format:	U4-1 index value (# of viewports)				

## 3DSTATE\_CONSTANT\_DS

3DSTATE_CONSTANT_DS			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
<p>This command sets pointers to the push constants for the DS unit. The constant data pointed to by this command is loaded into the DS unit's push constant buffer (PCB).</p>			
<b>Programming Notes</b>		<b>Project</b>	
[CHV, BSW] A 3DSTATE_GATHER_DS command must be dispatched along with any 3DSTATE_CONSTANT_DS command when Gather Pool is enabled within a batch buffer.		CHV, BSW	
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
		Default Value:	1Ah 3DSTATE_CONSTANT_DS
		Format:	OpCode
15	<b>Reserved</b>		
	Project:	CHV, BSW	
	Format:	MBZ	
14:8	<b>Constant Buffer Object Control State</b>		
	Project:	CHV, BSW	
	Format:	MEMORY_OBJECT_CONTROL_STATE	
	Specifies the memory object control state for all constant buffers defined in this command.		
	<b>Programming Notes</b>		
	Constant Buffer Object Control State must be always programmed to zero.		
7:0	<b>DWord Length</b>		
	Project:	All	

<b>3DSTATE_CONSTANT_DS</b>														
		<table border="1"> <tr> <td>Format:</td> <td colspan="2">=n Total Length - 2</td> </tr> <tr> <td></td> <td></td> <td></td> </tr> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Project</th> </tr> <tr> <td>9h</td> <td>Excludes DWord (0,1) <b>[Default]</b></td> <td>CHV, BSW</td> </tr> </table>	Format:	=n Total Length - 2					Value	Name	Project	9h	Excludes DWord (0,1) <b>[Default]</b>	CHV, BSW
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9h	Excludes DWord (0,1) <b>[Default]</b>	CHV, BSW												
1..10 <b>Project:</b> CHV, BSW	319:0	<p><b>Constant Body</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>3DSTATE_CONSTANT(Body)</td> </tr> </table> <p>Following table is the shared portion of the 3DSTATE_CONSTANT command for VS, HS, DS, and GS</p>	Project:	CHV, BSW	Format:	3DSTATE_CONSTANT(Body)								
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## 3DSTATE\_CONSTANT\_GS

3DSTATE_CONSTANT_GS			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
This command sets pointers to the push constants for the GS unit. The constant data pointed to by this command will be loaded into the GS unit's push constant buffer (PCB).			
Programming Notes		Project	
[CHV, BSW]: A 3DSTATE_GATHER_GS command must be dispatched along with any 3DSTATE_CONSTANT_GS command when the Gather Pool is enabled within a batch buffer.		CHV, BSW	
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
		Default Value:	16h 3DSTATE_CONSTANT_GS
		Format:	OpCode
15	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
14:8	<b>Constant Buffer Object Control State</b>		
	Project:	CHV, BSW	
	Format:	MEMORY_OBJECT_CONTROL_STATE	
	Specifies the memory object control state for all constant buffers defined in this command.		
	Programming Notes	Project	
Constant Buffer Object Control State must be always programmed to zero.		CHV, BSW	
7:0	<b>DWord Length</b>		
	Project:	All	

<b>3DSTATE_CONSTANT_GS</b>														
		<table border="1"> <tr> <td>Format:</td> <td colspan="2">=n Total Length - 2</td> </tr> <tr> <td></td> <td></td> <td></td> </tr> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Project</th> </tr> <tr> <td>9h</td> <td>Excludes DWord (0,1) <b>[Default]</b></td> <td>CHV, BSW</td> </tr> </table>	Format:	=n Total Length - 2					Value	Name	Project	9h	Excludes DWord (0,1) <b>[Default]</b>	CHV, BSW
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Value	Name	Project												
9h	Excludes DWord (0,1) <b>[Default]</b>	CHV, BSW												
1..10 <b>Project:</b> CHV, BSW	319:0	<p><b>Constant Body</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>3DSTATE_CONSTANT(Body)</td> </tr> </table> <p>Following table is the shared portion of the 3DSTATE_CONSTANT command for VS, HS, DS, and GS</p>	Project:	CHV, BSW	Format:	3DSTATE_CONSTANT(Body)								
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## 3DSTATE\_CONSTANT\_HS

3DSTATE_CONSTANT_HS			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
<p>This command sets pointers to the push constants for the HS unit. The constant data pointed to by this command is loaded into the HS unit's push constant buffer (PCB).</p>			
Programming Notes		Project	
A 3DSTATE_GATHER_HS command must be dispatched along with any 3DSTATE_CONSTANT_HS command when Gather Pool is enabled within a batch buffer.		CHV, BSW	
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
		Default Value:	19h 3DSTATE_CONSTANT_HS
		Format:	OpCode
15	<b>Reserved</b>		
	Project:	CHV, BSW	
	Format:	MBZ	
14:8	<b>Constant Buffer Object Control State</b>		
	Project:	CHV, BSW	
	Format:	MEMORY_OBJECT_CONTROL_STATE	
	Specifies the memory object control state for all constant buffers defined in this command.		
	Programming Notes		Project
	Constant Buffer Object Control State must be always programmed to zero.		CHV, BSW
7:0	<b>DWord Length</b>		
	Project:	All	



<b>3DSTATE_CONSTANT_HS</b>								
		<table border="1"> <tr> <td>Format:</td> <td>=n Total Length - 2</td> </tr> </table>	Format:	=n Total Length - 2				
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Value	Name	Project						
9h	Excludes DWord (0,1) <b>[Default]</b>	CHV, BSW						
1..10 <b>Project:</b> CHV, BSW	319:0	<p><b>Constant Body</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>3DSTATE_CONSTANT(Body)</td> </tr> </table> <p>Following table is the shared portion of the 3DSTATE_CONSTANT command for VS, HS, DS, and GS</p>	Project:	CHV, BSW	Format:	3DSTATE_CONSTANT(Body)		
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Format:	3DSTATE_CONSTANT(Body)							

## 3DSTATE\_CONSTANT\_PS

3DSTATE_CONSTANT_PS			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
This command sets pointers to the push constants for the PS unit. The constant data pointed to by this command is loaded into the PS unit's push constant buffer (PCB).			
Programming Notes		Project	
[CHV, BSW]: A 3DSTATE_GATHER_PS command must be dispatched along with any 3DSTATE_CONSTANT_PS command when the Gather Pool is enabled within a batch buffer.		CHV, BSW	
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
		Default Value:	17h 3DSTATE_CONSTANT_PS
		Format:	OpCode
	15	<b>Reserved</b>	
		Project:	CHV, BSW
Format:		MBZ	
14:8	<b>Constant Buffer Object Control State</b>		
	Project:	CHV, BSW	
	Format:	MEMORY_OBJECT_CONTROL_STATE	
	Specifies the memory object control state for all constant buffers defined in this command.		
	Programming Notes		Project
	Constant Buffer Object Control State must be always programmed to zero.		CHV, BSW
7:0	<b>Dword Length</b>		
	Project:	All	

<b>3DSTATE_CONSTANT_PS</b>														
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## 3DSTATE\_CONSTANT\_VS

3DSTATE_CONSTANT_VS			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
This command sets pointers to the push constants for VS unit. The constant data pointed to by this command is loaded into the VS unit's push constant buffer (PCB).			
Programming Notes		Project	
[CHV, BSW] A 3DSTATE_GATHER_VS command must be dispatched along with any 3DSTATE_CONSTANT_VS command when Gather Pool is enabled within a batch buffer.		CHV, BSW	
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
		Default Value:	15h 3DSTATE_CONSTANT_VS
		Format:	OpCode
15	<b>Reserved</b>		
	Project:	CHV, BSW	
	Format:	MBZ	
14:8	<b>Constant Buffer Object Control State</b>		
	Project:	CHV, BSW	
	Format:	MEMORY_OBJECT_CONTROL_STATE	
	Specifies the memory object control state for all constant buffers defined in this command.		
	Programming Notes	Project	
Constant Buffer Object Control State must be always programmed to zero.		CHV, BSW	
7:0	<b>DWord Length</b>		
	Project:	All	

<b>3DSTATE_CONSTANT_VS</b>														
		<table border="1"> <tr> <td>Format:</td> <td colspan="2">=n Total Length - 2</td> </tr> <tr> <td></td> <td></td> <td></td> </tr> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Project</th> </tr> <tr> <td>9h</td> <td>Excludes DWord (0,1) <b>[Default]</b></td> <td>CHV, BSW</td> </tr> </table>	Format:	=n Total Length - 2					Value	Name	Project	9h	Excludes DWord (0,1) <b>[Default]</b>	CHV, BSW
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Value	Name	Project												
9h	Excludes DWord (0,1) <b>[Default]</b>	CHV, BSW												
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Format:	3DSTATE_CONSTANT(Body)													

## 3DSTATE\_DEPTH\_BUFFER

3DSTATE_DEPTH_BUFFER																				
Project:	CHV, BSW																			
Source:	RenderCS																			
Length Bias:	2																			
<p>The depth buffer surface state is delivered as a pipelined state packet. However, the state change pipelining isn't completely transparent (see restriction below).</p> <p>WM HW will internally manage the draining pipe and flushing of the caches when this commands is issued. The PIPE_CONTROL restrictions are removed.</p>																				
DWord	Bit	Description																		
0	31:2	<b>Command Type</b>																		
	9	Default Value: 3h GFXPIPE																		
		Format: OpCode																		
	28:2	<b>Command SubType</b>																		
	7	Default Value: 3h GFXPIPE_3D																		
		Format: OpCode																		
	26:2	<b>3D Command Opcode</b>																		
4	Default Value: 0h 3DSTATE_PIPELINED																			
	Format: OpCode																			
23:1	<b>3D Command Sub Opcode</b>																			
6	Default Value: 5h 3DSTATE_DEPTH_BUFFER																			
	Format: OpCode																			
15:8	<b>Reserved</b>																			
	Format: MBZ																			
7:0	<b>DWord Length</b>																			
	Default Value: 6h Excludes Dword (0,1)																			
	Format: =n																			
	Excludes DWord(0,1)																			
1	31:2	<b>Surface Type</b>																		
	9	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>SURFTYPE_1D</td> <td>Defines a 1-dimensional map or array of maps</td> </tr> <tr> <td>1h</td> <td>SURFTYPE_2D</td> <td>Defines a 2-dimensional map or array of maps</td> </tr> <tr> <td>2h</td> <td>SURFTYPE_3D</td> <td>Defines a 3-dimensional (volumetric) map</td> </tr> <tr> <td>3h</td> <td>SURFTYPE_CUBE</td> <td>Defines a cube map</td> </tr> <tr> <td>4h-6h</td> <td>Reserved</td> <td></td> </tr> </tbody> </table>	Value	Name	Description	0h	SURFTYPE_1D	Defines a 1-dimensional map or array of maps	1h	SURFTYPE_2D	Defines a 2-dimensional map or array of maps	2h	SURFTYPE_3D	Defines a 3-dimensional (volumetric) map	3h	SURFTYPE_CUBE	Defines a cube map	4h-6h	Reserved	
	Value	Name	Description																	
	0h	SURFTYPE_1D	Defines a 1-dimensional map or array of maps																	
	1h	SURFTYPE_2D	Defines a 2-dimensional map or array of maps																	
	2h	SURFTYPE_3D	Defines a 3-dimensional (volumetric) map																	
3h	SURFTYPE_CUBE	Defines a cube map																		
4h-6h	Reserved																			

<b>3DSTATE_DEPTH_BUFFER</b>		
7h	SURFTYPE_NULL	Defines a null surface
<b>Programming Notes</b>		
The Surface Type of the depth buffer must be the same as the Surface Type of the render target(s) (defined in SURFACE_STATE), unless either the depth buffer or render targets are SURFTYPE_NULL.		
28	<b>Depth Write Enable</b>	
	Format:	Enable
This field enables depth writes to the depth buffer surface. Both this field and the Depth Buffer Write Enable field in DEPTH_STENCIL_STATE must be enabled in order for depth writes to occur.		
27	<b>Stencil Write Enable</b>	
	Format:	Enable
This field enables stencil writes to the depth buffer or stencil buffer surface, depending on where stencil is located. Both this field and the Stencil Buffer Write Enable field in DEPTH_STENCIL_STATE must be enabled in order for stencil writes to occur.		
26:2	<b>Reserved</b>	
3	Format:	MBZ
22	<b>Hierarchical Depth Buffer Enable</b>	
	Format:	Enable
If enabled, indicates that a hierarchical depth buffer is defined.		
<b>Programming Notes</b>		
If this field is enabled, the Software Tiled Rendering Mode must be NORMAL. This field must be disabled if Early Depth Test Enable is disabled OR if depth buffer surface type is NULL.		
21	<b>Reserved</b>	
	Format:	MBZ
20:1	<b>Surface Format</b>	
8	Specifies the format of the depth buffer. See Stencil Test Enable field in DEPTH_STENCIL_STATE field for restrictions on the use of some of these formats.	
	<b>Value</b>	<b>Name</b>
	0h	Reserved
	1h	D32_FLOAT
	2h	Reserved
	3h	D24_UNORM_X8_UINT
	4h	Reserved
	5h	D16_UNORM
	6h-7h	Reserved

<b>3DSTATE_DEPTH_BUFFER</b>																								
	17:0	<p><b>Surface Pitch</b></p> <table border="1"> <tr> <td>Format:</td> <td>U18-1 Pitch in (Bytes-1)</td> </tr> </table> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[7Fh,3FFFFh]</td> <td></td> <td>corresponding to [128B, 256KB] also restricted to a multiple of 128B</td> </tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>The pitch specified must be a multiple of the tile pitch, in the range [128B, 128KB].</p>	Format:	U18-1 Pitch in (Bytes-1)	Value	Name	Description	[7Fh,3FFFFh]		corresponding to [128B, 256KB] also restricted to a multiple of 128B														
	Format:	U18-1 Pitch in (Bytes-1)																						
	Value	Name	Description																					
	[7Fh,3FFFFh]		corresponding to [128B, 256KB] also restricted to a multiple of 128B																					
2..3 <b>Project:</b> CHV, BSW	63:0	<p><b>Surface Base Address</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[63:0]DepthBuffer</td> </tr> </table> <p>This field specifies address of the buffer in mapped Graphics Memory. Graphics Address [63:48] are ignored by the HW and assumed to be in correct canonical form [63:48] = [47].</p> <p style="text-align: center;"><b>Programming Notes</b></p> <p>The Depth Buffer can only be mapped to Main Memory (uncached).</p> <p>If the buffer is linear, the surface must be 64-byte aligned.</p>	Project:	CHV, BSW	Format:	GraphicsAddress[63:0]DepthBuffer																		
Project:	CHV, BSW																							
Format:	GraphicsAddress[63:0]DepthBuffer																							
4	31:1	<p><b>Height</b></p> <table border="1"> <tr> <td>Format:</td> <td>U14-1</td> </tr> </table> <p>This field specifies the height of the surface. If the surface is MIP-mapped, this field contains the height of the base MIP level.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Exists If</th> </tr> </thead> <tbody> <tr> <td>[0,0]</td> <td>Legal Range</td> <td>Must be zero</td> <td>(Structure[RENDER_SURFACE_STATE][Surface Type] == 'SURFTYPE_1D')</td> </tr> <tr> <td>[0,16383]</td> <td>Legal Range</td> <td>Height of surface - 1 (y/v dimension)</td> <td>(Structure[RENDER_SURFACE_STATE][Surface Type] == 'SURFTYPE_2D')</td> </tr> <tr> <td>[0,2047]</td> <td>Legal Range</td> <td>Height of surface - 1 (y/v dimension)</td> <td>(Structure[RENDER_SURFACE_STATE][Surface Type] == 'SURFTYPE_3D')</td> </tr> <tr> <td>[0,16383]</td> <td>Legal Range</td> <td>y/v dimension</td> <td>(Structure[RENDER_SURFACE_STATE][Surface Type] == 'SURFTYPE_CUBE')</td> </tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>The Height of the depth buffer must be the same as the Height of the render target(s) (defined in SURFACE_STATE), unless Surface Type is SURFTYPE_1D or SURFTYPE_2D with Depth = 0 (non-array) and LOD = 0 (non-mip mapped).</p>	Format:	U14-1	Value	Name	Description	Exists If	[0,0]	Legal Range	Must be zero	(Structure[RENDER_SURFACE_STATE][Surface Type] == 'SURFTYPE_1D')	[0,16383]	Legal Range	Height of surface - 1 (y/v dimension)	(Structure[RENDER_SURFACE_STATE][Surface Type] == 'SURFTYPE_2D')	[0,2047]	Legal Range	Height of surface - 1 (y/v dimension)	(Structure[RENDER_SURFACE_STATE][Surface Type] == 'SURFTYPE_3D')	[0,16383]	Legal Range	y/v dimension	(Structure[RENDER_SURFACE_STATE][Surface Type] == 'SURFTYPE_CUBE')
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8	17:4	<p><b>Width</b></p> <table border="1"> <tr> <td>Format:</td> <td>U14-1</td> </tr> </table>	Format:	U14-1																				
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		<b>3DSTATE_DEPTH_BUFFER</b>																							
		<p>This field specifies the width of the surface. If the surface is MIP-mapped, this field specifies the width of the base MIP level. The width is specified in units of pixels.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Exists If</th> </tr> </thead> <tbody> <tr> <td>[0,16383]</td> <td>Legal Range</td> <td>Width of surface - 1 (x/u dimension)</td> <td>(Structure[RENDER_SURFACE_STATE][Surface Type]='SURFTYPE_1D')</td> </tr> <tr> <td>[0,16383]</td> <td>Legal Range</td> <td>Width of surface - 1 (x/u dimension)</td> <td>(Structure[RENDER_SURFACE_STATE][Surface Type]='SURFTYPE_2D')</td> </tr> <tr> <td>[0,2047]</td> <td>Legal Range</td> <td>Width of surface - 1 (x/u dimension)</td> <td>(Structure[RENDER_SURFACE_STATE][Surface Type]='SURFTYPE_3D')</td> </tr> <tr> <td>[0,16383]</td> <td>Legal Range</td> <td>Width of surface - 1 (x/u dimension)</td> <td>(Structure[RENDER_SURFACE_STATE][Surface Type]='SURFTYPE_CUBE')</td> </tr> </tbody> </table>				Value	Name	Description	Exists If	[0,16383]	Legal Range	Width of surface - 1 (x/u dimension)	(Structure[RENDER_SURFACE_STATE][Surface Type]='SURFTYPE_1D')	[0,16383]	Legal Range	Width of surface - 1 (x/u dimension)	(Structure[RENDER_SURFACE_STATE][Surface Type]='SURFTYPE_2D')	[0,2047]	Legal Range	Width of surface - 1 (x/u dimension)	(Structure[RENDER_SURFACE_STATE][Surface Type]='SURFTYPE_3D')	[0,16383]	Legal Range	Width of surface - 1 (x/u dimension)	(Structure[RENDER_SURFACE_STATE][Surface Type]='SURFTYPE_CUBE')
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		<b>Programming Notes</b>																							
		<p>The Width specified by this field must be less than or equal to the surface pitch (specified in bytes via the Surface Pitch field). For cube maps, Width must be set equal to Height. The Width of the depth buffer must be the same as the Width of the render target(s) (defined in SURFACE_STATE), unless Surface Type is SURFTYPE_1D or SURFTYPE_2D with Depth = 0 (non-array) and LOD = 0 (non-mip mapped).</p>																							
	3:0	<b>LOD</b>																							
		Format:	U4 for LOD units																						
		<b>Value</b>	<b>Name</b>																						
		[0,14]																							
		<b>Programming Notes</b>																							
		<p>The LOD of the depth buffer must be the same as the LOD of the render target(s) (defined in SURFACE_STATE)</p>																							
5	31:2 1	<b>Depth</b>																							
		Format:	U11-1																						
		<p>This field specifies the total number of levels for a volume texture or the number of array elements allowed to be accessed starting at the Minimum Array Element for arrayed surfaces. If the volume texture is MIP-mapped, this field specifies the depth of the base MIP level.</p>																							
		<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Exists If</b>																				
		[0,2047]	Legal Range	Number of array elements - 1	(Structure[RENDER_SURFACE_STATE][Surface Type]='SURFTYPE_1D')																				
		[0,2047]	Legal Range	Number of array elements - 1	(Structure[RENDER_SURFACE_STATE][Surface Type]='SURFTYPE_2D')																				
		[0,2047]	Legal Range	Depth of surface - 1 (r/z dimension)	(Structure[RENDER_SURFACE_STATE][Surface Type]='SURFTYPE_3D')																				
		[0,0]	Legal Range	Must be zero	(Structure[RENDER_SURFACE_STATE][Surface Type]='SURFTYPE_CUBE')																				

<b>3DSTATE_DEPTH_BUFFER</b>																	
<b>Programming Notes</b>																	
The Depth of the depth buffer must be the same as the Depth of the render target(s) (defined in SURFACE_STATE).																	
20:1 0	<b>Minimum Array Element</b>																
	Format: U11																
	<p><b>For 1D and 2D Surfaces:</b> This field indicates the minimum array element that can be accessed as part of this surface. The delivered array index is added to this field before being used to address the surface.</p> <p><b>For 3D Surfaces</b> This field indicates the minimum 'R' coordinate on the LOD currently being rendered to. This field is added to the delivered array index before it is used to address the surface.</p> <p><b>For Other Surfaces</b> This field is ignored</p>																
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[0,2047]	SURFTYPE_3D	(Structure[RENDER_SURFACE_STATE][Surface Type]== 'SURFTYPE_3D')															
9:7	<b>Reserved</b>																
	Format: MBZ																
6:0	<b>Depth Buffer Object Control State</b>																
	Format: MEMORY_OBJECT_CONTROL_STATE Specifies the memory object control state for the depth buffer.																
6	31:2 6	<b>Reserved</b>															
		Project: CHV, BSW															
	Format: MBZ																
25:0	<b>Reserved</b>																
	Format: MBZ																
7	31:2 1	<b>Render Target View Extent</b>															
		Format: U11-1															
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[0,2047]	Legal	To indication	(Structure[RENDER_SURFACE_STATE][Surface														
<p><b>For 1D and 2D Surfaces:</b> This field must be set to the same value as the</p>																	

<b>3DSTATE_DEPTH_BUFFER</b>				
<p>Depth field.</p> <p><b>For 3D Surfaces:</b> This field indicates the extent of the accessible 'R' coordinate s minus 1 on the LOD currently being rendered to.</p> <p><b>For Other Surfaces</b> This field is ignored.</p>		Range	extent of [1,2048] Type]='SURFTYPE_3D')	
	[0,0]	Legal Range	Must be zero (Structure[RENDER_SURFACE_STATE][Surface Type]='SURFTYPE_CUBE')	
	20:1	<b>Reserved</b>		
	5			
	14:0	<b>Surface QPitch</b>		
		Format:	QPitch[16:2]	
		<b>Description</b>		
		This field specifies the distance in rows between array slices. It is used only in the following cases: <ul style="list-style-type: none"> <li>• <b>Surface Array</b> is enabled <i>OR</i></li> <li>• <b>Number of Multisamples</b> is not NUMSAMPLES_1 and <b>Multisampled Surface Storage Format</b> set to MSFMT_MSS <i>OR</i></li> <li>• <b>Surface Type</b> is SURFTYPE_CUBE</li> </ul>		
		Other surface types: field is ignored		
		<b>Value</b>	<b>Name</b>	<b>Description</b>
	[4h, 1FFFCh]		in multiples of 4 (low 2 bits missing)	
	<b>Programming Notes</b>			
	Software must ensure that this field is set to a value sufficiently large that array slices in the surface do not overlap. Refer to the <i>Memory Data Formats</i> section for information on how surfaces are stored.			

## 3DSTATE\_DRAWING\_RECTANGLE

3DSTATE_DRAWING_RECTANGLE				
Project:	CHV, BSW			
Source:	RenderCS			
Length Bias:	2			
The 3DSTATE_DRAWING_RECTANGLE command is used to set the 3D drawing rectangle and related state.				
DWord	Bit	Description		
0	31:29	<b>Command Type</b>		
		Default Value:	3h GFXPIPE	
		Format:	OpCode	
	28:27	<b>Command SubType</b>		
		Default Value:	3h GFXPIPE_3D	
		Format:	OpCode	
	26:24	<b>3D Command Opcode</b>		
		Default Value:	1h 3DSTATE_NONPIPELINED	
		Format:	OpCode	
	23:16	<b>3D Command Sub Opcode</b>		
Default Value:		00h 3DSTATE_DRAWING_RECTANGLE		
Format:		OpCode		
15:14	<b>Core Mode Select</b>			
	Project:	CHV, BSW		
	Format:	U2		
	Specifies which core this command will be considered valid and update based on the state in this command.			
	<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>
	0h	Legacy	Both cores are enabled and will update the state.	All
	1h	Core 0 Enabled	State will be updated in Core 0 only	All
	2h	Core 1 Enabled	State will be updated in Core 1 only	All
	3h	Reserved		All
	13:8	<b>Reserved</b>		
Format:		MBZ		
7:0		<b>DWord Length</b>		
	Default Value:	2h Excludes DWord (0,1)		
	Project:	All		
	Format:	=n Total Length - 2		
1	31:16	<b>Clipped Drawing Rectangle Y Min</b>		

### 3DSTATE\_DRAWING\_RECTANGLE

		Project:	All	
		Format:	U16 in Pixels from Color Buffer origin (upper left corner)	
		Specifies Ymin value of (inclusive) intersection of Drawing rectangle with the Color (Destination) Buffer, used for clipping. Pixels with Y coordinates less than Ymin will be clipped out.		
		<b>Value</b>	<b>Name</b>	
		[0,16383]	Device ignores bits 31:30	
		<b>Programming Notes</b>		
		This value can be larger than Clipped Drawing Rectangle Y Max. If Ymin>Ymax, the clipped drawing rectangle is null, all polygons are discarded. If Ymin==Ymax, the clipped drawing rectangle is 1 pixel wide in the Y direction.		
	15:0	<b>Clipped Drawing Rectangle X Min</b>		
		Project:	All	
		Format:	U16 in Pixels from Color Buffer origin (upper left corner)	
		Specifies Xmin value of (inclusive) intersection of Drawing rectangle with the Color (Destination) Buffer, used for clipping. Pixels with X coordinates less than Xmin will be clipped out.		
		<b>Value</b>	<b>Name</b>	
		[0,16383]	Device ignores bits 15:14	
		<b>Programming Notes</b>		
		This value can be larger than Clipped Drawing Rectangle X Max. If Xmin>Xmax, the clipped drawing rectangle is null, all polygons are discarded. If Xmin==Xmax, the clipped drawing rectangle is 1 pixel wide in the X direction.		
2	31:16	<b>Clipped Drawing Rectangle Y Max</b>		
		Project:	All	
		Format:	U16 in Pixels from Color Buffer origin (upper left corner)	
		Specifies Ymax value of (inclusive) intersection of Drawing rectangle with the Color (Destination) Buffer, used for clipping. Pixels with coordinates greater than Ymax will be clipped out.		
		<b>Value</b>	<b>Name</b>	
		[0,16383]	Device ignores bits 31:30	
		<b>Programming Notes</b>		
		This value can be less than Clipped Drawing Rectangle Y Min. If Ymax<Ymin, the clipped drawing rectangle is null, all polygons are discarded. If Ymin==Ymax, the clipped drawing rectangle is 1 pixel wide in the Y direction.		
	15:0	<b>Clipped Drawing Rectangle X Max</b>		
		Project:	All	
		Format:	U16 in Pixels from Color Buffer origin (upper left corner)	
		Specifies Xmax value of (inclusive) intersection of Drawing rectangle with the Color (Destination) Buffer, used for clipping. Pixels with coordinates greater than Xmax will be clipped out.		

<b>3DSTATE_DRAWING_RECTANGLE</b>												
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3	31:16	<p><b>Drawing Rectangle Origin Y</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 20%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>S15 in Pixels from Color Buffer origin (upper left corner).</td> </tr> </table> <table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 80%;">Description</th> <th style="width: 20%;">Project</th> </tr> </thead> <tbody> <tr> <td>Range: [-16384,16383] (Bit 31 should be a sign extension)</td> <td>CHV, BSW</td> </tr> <tr> <td>Specifies Y origin of Drawing Rectangle (in whole pixels) relative to origin of the Color Buffer, used to map incoming (Draw Rectangle-relative) vertex positions to the Color Buffer space.</td> <td></td> </tr> </tbody> </table>	Project:	All	Format:	S15 in Pixels from Color Buffer origin (upper left corner).	Description	Project	Range: [-16384,16383] (Bit 31 should be a sign extension)	CHV, BSW	Specifies Y origin of Drawing Rectangle (in whole pixels) relative to origin of the Color Buffer, used to map incoming (Draw Rectangle-relative) vertex positions to the Color Buffer space.	
	Project:	All										
Format:	S15 in Pixels from Color Buffer origin (upper left corner).											
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	15:0	<p><b>Drawing Rectangle Origin X</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 20%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>S15 in Pixels from Color Buffer origin (upper left corner).</td> </tr> </table> <table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 80%;">Description</th> <th style="width: 20%;">Project</th> </tr> </thead> <tbody> <tr> <td>Range: [-16384,16383] (Bit 15 should be a sign extension)</td> <td>CHV, BSW</td> </tr> <tr> <td>Specifies X origin of Drawing Rectangle (in whole pixels) relative to origin of the Color Buffer, used to map incoming (Draw Rectangle-relative) vertex positions to the Color Buffer space.</td> <td></td> </tr> </tbody> </table>	Project:	All	Format:	S15 in Pixels from Color Buffer origin (upper left corner).	Description	Project	Range: [-16384,16383] (Bit 15 should be a sign extension)	CHV, BSW	Specifies X origin of Drawing Rectangle (in whole pixels) relative to origin of the Color Buffer, used to map incoming (Draw Rectangle-relative) vertex positions to the Color Buffer space.	
Project:	All											
Format:	S15 in Pixels from Color Buffer origin (upper left corner).											
Description	Project											
Range: [-16384,16383] (Bit 15 should be a sign extension)	CHV, BSW											
Specifies X origin of Drawing Rectangle (in whole pixels) relative to origin of the Color Buffer, used to map incoming (Draw Rectangle-relative) vertex positions to the Color Buffer space.												

## 3DSTATE\_DS

<b>3DSTATE_DS</b>			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
The state used by DS is defined with this inline state packet			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		1Dh 3DSTATE_DS	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	7h Excludes DWord (0,1)	
	Project:	CHV, BSW	
	Format:	=n Total Length - 2	
1.2 Project: CHV, BSW	63:6	<b>Kernel Start Pointer</b>	
		Project:	CHV, BSW
		Format:	InstructionBaseOffset[63:6]Kernel
This field specifies the starting location of the kernel program run by threads spawned by this FF unit. It is specified as a 64-byte-granular offset from the Instruction Base Address. This field is ignored if DS Function Enable is DISABLED.			
	5:0	<b>Reserved</b>	
		Project:	All
		Format:	MBZ

<b>3DSTATE_DS</b>																				
3	31	<p><b>Single Domain Point Dispatch</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U1 Enumerated Type</td> </tr> </table> <p>This field can be used to force single domain point SIMD4x2 DS threads. This field is ignored if <b>SIMD8 Dispatch Enable</b> is set.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Multiple</td> <td>Dual domain point SIMD4x2 thread dispatches are allowed.</td> </tr> <tr> <td>1h</td> <td>Single</td> <td>Single domain point SIMD4x2 thread dispatches are forced.</td> </tr> </tbody> </table> <table border="1" style="width: 100%; margin-top: 10px;"> <thead> <tr> <th style="width: 80%;">Workaround</th> <th style="width: 20%;">Project</th> </tr> </thead> <tbody> <tr> <td>Workaround: The Single Domain Point Dispatch must always be set to 0.</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Project:	CHV, BSW	Format:	U1 Enumerated Type	Value	Name	Description	0h	Multiple	Dual domain point SIMD4x2 thread dispatches are allowed.	1h	Single	Single domain point SIMD4x2 thread dispatches are forced.	Workaround	Project	Workaround: The Single Domain Point Dispatch must always be set to 0.	CHV, BSW	
	Project:	CHV, BSW																		
	Format:	U1 Enumerated Type																		
Value	Name	Description																		
0h	Multiple	Dual domain point SIMD4x2 thread dispatches are allowed.																		
1h	Single	Single domain point SIMD4x2 thread dispatches are forced.																		
Workaround	Project																			
Workaround: The Single Domain Point Dispatch must always be set to 0.	CHV, BSW																			
30	<p><b>Vector Mask Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U1 Enumerated Type</td> </tr> </table> <p>Upon subsequent DS thread dispatches, this bit is loaded into the EU's Vector Mask Enable (VME, cr0.0[3]) thread state. Refer to EU documentation for the definition and use of VME state.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Dmask</td> <td>The EU will use the Dispatch Mask (supplied by the DS stage) for instruction execution.</td> </tr> <tr> <td>1h</td> <td>Vmask</td> <td>The EU will use the Vector Mask (derived from the Dispatch Mask) for instruction execution.</td> </tr> </tbody> </table> <table border="1" style="width: 100%; margin-top: 10px;"> <thead> <tr> <th style="text-align: center;">Programming Notes</th> </tr> </thead> <tbody> <tr> <td>Under normal conditions SW shall specify DMask, as the DS stage will provide a Dispatch Mask appropriate to SIMD4x2 or SIMD8 thread execution (as a function of dispatch mode). E.g., for SIMD4x2 thread execution, the DS stage will generate a Dispatch Mask that is equal to what the EU would use as the Vector Mask. For SIMD8 execution there is no known usage model for use of Vector Mask (as there is for PS shaders).</td> </tr> </tbody> </table>	Project:	CHV, BSW	Format:	U1 Enumerated Type	Value	Name	Description	0h	Dmask	The EU will use the Dispatch Mask (supplied by the DS stage) for instruction execution.	1h	Vmask	The EU will use the Vector Mask (derived from the Dispatch Mask) for instruction execution.	Programming Notes	Under normal conditions SW shall specify DMask, as the DS stage will provide a Dispatch Mask appropriate to SIMD4x2 or SIMD8 thread execution (as a function of dispatch mode). E.g., for SIMD4x2 thread execution, the DS stage will generate a Dispatch Mask that is equal to what the EU would use as the Vector Mask. For SIMD8 execution there is no known usage model for use of Vector Mask (as there is for PS shaders).				
Project:	CHV, BSW																			
Format:	U1 Enumerated Type																			
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Programming Notes																				
Under normal conditions SW shall specify DMask, as the DS stage will provide a Dispatch Mask appropriate to SIMD4x2 or SIMD8 thread execution (as a function of dispatch mode). E.g., for SIMD4x2 thread execution, the DS stage will generate a Dispatch Mask that is equal to what the EU would use as the Vector Mask. For SIMD8 execution there is no known usage model for use of Vector Mask (as there is for PS shaders).																				
29:27	<p><b>Sampler Count</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U3</td> </tr> </table> <p>Specifies how many samplers (in multiples of 4) the kernel uses. Used only for prefetching the associated sampler state entries. This field is ignored if DS Function Enable is DISABLED.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>No Samplers</td> <td>No samplers used</td> </tr> <tr> <td>1h</td> <td>1-4 Samplers</td> <td>between 1 and 4 samplers used</td> </tr> <tr> <td>2h</td> <td>5-8 Samplers</td> <td>between 5 and 8 samplers used</td> </tr> <tr> <td>3h</td> <td>9-12 Samplers</td> <td>between 9 and 12 samplers used</td> </tr> </tbody> </table>	Project:	CHV, BSW	Format:	U3	Value	Name	Description	0h	No Samplers	No samplers used	1h	1-4 Samplers	between 1 and 4 samplers used	2h	5-8 Samplers	between 5 and 8 samplers used	3h	9-12 Samplers	between 9 and 12 samplers used
Project:	CHV, BSW																			
Format:	U3																			
Value	Name	Description																		
0h	No Samplers	No samplers used																		
1h	1-4 Samplers	between 1 and 4 samplers used																		
2h	5-8 Samplers	between 5 and 8 samplers used																		
3h	9-12 Samplers	between 9 and 12 samplers used																		



<b>3DSTATE_DS</b>		
	4h	13-16 Samplers between 13 and 16 samplers used
26	<b>Reserved</b>	
	Project:	CHV, BSW
	Format:	MBZ
25:18	<b>Binding Table Entry Count</b>	
	Project:	CHV, BSW
	Format:	U8
<p>When HW Generated Binding Table is disabled: Specifies how many binding table entries the kernel uses. Used only for prefetching of the binding table entries and associated surface state. <b>Note:</b>For kernels using a large number of binding table entries, it may be wise to set this field to zero to avoid prefetching too many entries and thrashing the state cache. This field is ignored if DS Function Enable is DISABLED.</p> <p>When HW Generated Binding Table bit is enabled: This field indicates which cache lines (512bit units - 32 Binding Table Entry section) should be fetched. Each bit in this field corresponds to a cache line. Only the 1st 4 non-zero Binding Table entries of each 32 Binding Table entry section prefetched will have its surface state prefetched.</p>		
<b>Value</b>		<b>Name</b>
[0,255]		
<b>Programming Notes</b>		<b>Project</b>
When HW binding table bit is set, it is assumed that the Binding Table Entry Count field will be generated at JIT time.		CHV, BSW
17	<b>Thread Dispatch Priority</b>	
	Project:	CHV, BSW
	Format:	U1 Enumerated Type
<p>Specifies the priority of the thread for dispatch: This field is ignored if DS Function Enable is DISABLED.</p>		
<b>Value</b>	<b>Name</b>	<b>Description</b>
0h	Normal	Normal Priority
1h	High	High Priority
16	<b>Floating Point Mode</b>	
	Project:	CHV, BSW
	Format:	U1 Enumerated Type
<p>Specifies the initial floating point mode used by the dispatched thread. This field is ignored if DS Function Enable is DISABLED.</p>		
<b>Value</b>	<b>Name</b>	<b>Description</b>
0h	IEEE-754	Use IEEE-754 Rules
1h	Alternate	Use alternate rules

<b>3DSTATE_DS</b>				
	15	<b>Reserved</b>	Project: CHV, BSW	Format: MBZ
	14	<b>Accesses UAV</b>	Project: CHV, BSW	Format: Enable
		This bit gets loaded into EU CR0.1[12] (note the bit # difference). See Exceptions and ISA Execution Environment.		
		<b>Programming Notes</b>		
		This field must not be set when DS Function Enable is disabled.		
	13	<b>Illegal Opcode Exception Enable</b>	Project: CHV, BSW	Format: Enable
This bit gets loaded into EU CR0.1[12] (note the bit # difference). See Exceptions and ISA Execution Environment. This field is ignored if DS Function Enable is DISABLED.				
12:8	<b>Reserved</b>	Project: CHV, BSW	Format: MBZ	
	7	<b>Software Exception Enable</b>	Project: CHV, BSW	Format: Enable
This bit gets loaded into EU CR0.1[13] (note the bit # difference). See Exceptions and ISA Execution Environment. This field is ignored if DS Function Enable is DISABLED.				
6:0		<b>Reserved</b>	Project: CHV, BSW	Format: MBZ
	4..5 <b>Project:</b> CHV, BSW	63:10	<b>Scratch Space Base Pointer</b>	Project: CHV, BSW
Specifies the starting location of the scratch space area allocated to this FF unit as a 1K-byte aligned offset from the General State Base Address. If required, each thread spawned by this FF unit will be allocated some portion of this space, as specified by Per-Thread Scratch Space. The computed offset of the thread-specific portion will be passed in the thread payload as Scratch Space Offset. The thread is expected to utilize "stateless" DataPort read/write requests to access scratch space, where the DataPort will cause the General State Base Address to be added to the offset passed in the request header. This field is ignored if DS Function Enable is DISABLED.				

<b>3DSTATE_DS</b>											
	9:4	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ					
	Project:	CHV, BSW									
Format:	MBZ										
	3:0	<p><b>Per-Thread Scratch Space</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U4 power of 2 Bytes over 1K Bytes</td> </tr> </table> <p>Specifies the amount of scratch space to be allocated to each thread spawned by this FF unit. The driver must allocate enough contiguous scratch space, starting at the Scratch Space Base Pointer, to ensure that the Maximum Number of Threads can each get Per-Thread Scratch Space size without exceeding the driver-allocated scratch space. This field is ignored if DS Function Enable is DISABLED.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>[0,11]</td> <td>indicating [1K Bytes, 2M Bytes]</td> </tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>This amount is available to the kernel for information only. It will be passed verbatim (if not altered by the kernel) to the Data Port in any scratch space access messages, but the Data Port will ignore it.</p>	Project:	CHV, BSW	Format:	U4 power of 2 Bytes over 1K Bytes	Value	Name	[0,11]	indicating [1K Bytes, 2M Bytes]	
Project:	CHV, BSW										
Format:	U4 power of 2 Bytes over 1K Bytes										
Value	Name										
[0,11]	indicating [1K Bytes, 2M Bytes]										
6 <b>Project:</b> CHV, BSW	31:25	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ					
	Project:	CHV, BSW									
	Format:	MBZ									
	24:20	<p><b>Dispatch GRF Start Register For URB Data</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>GRFRegister[4:0]</td> </tr> </table> <p>Specifies the starting GRF register number for the URB portion (Constant + Vertices) of the thread payload. This field is ignored if DS Function Enable is DISABLED.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[0,31]</td> <td></td> <td>indicating GRF [R0, R31]</td> </tr> </tbody> </table>	Project:	CHV, BSW	Format:	GRFRegister[4:0]	Value	Name	Description	[0,31]	
Project:	CHV, BSW										
Format:	GRFRegister[4:0]										
Value	Name	Description									
[0,31]		indicating GRF [R0, R31]									
19:18	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ						
Project:	CHV, BSW										
Format:	MBZ										
17:11	<p><b>Patch URB Entry Read Length</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U7</td> </tr> </table> <p>Specifies how much data (in 256-bit units) is to be read from the Patch URB entry and passed in the DS thread payload. This field is ignored if DS Function Enable is DISABLED.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>[0,64]</td> <td></td> </tr> </tbody> </table>	Project:	CHV, BSW	Format:	U7	Value	Name	[0,64]			
Project:	CHV, BSW										
Format:	U7										
Value	Name										
[0,64]											

<b>3DSTATE_DS</b>				
	10	<b>Reserved</b>		
		Project:	CHV, BSW	
		Format:	MBZ	
	9:4	<b>Patch URB Entry Read Offset</b>		
		Project:	CHV, BSW	
		Format:	U6	
Specifies the offset (in 256-bit units) at which Patch URB data is to be read from the URB before being included in the thread payload. This field is ignored if DS Function Enable is DISABLED.				
		<b>Value</b>	<b>Name</b>	
		[0,63]		
	3:0	<b>Reserved</b>		
		Project:	CHV, BSW	
		Format:	MBZ	
<b>7</b> <b>Project:</b> CHV, BSW	31	<b>Reserved</b>		
		Project:	CHV, BSW	
		Format:	MBZ	
	30	<b>Reserved</b>		
		Project:	CHV, BSW	
		Format:	MBZ	
	29:21	<b>Maximum Number of Threads</b>		
		Project:	CHV, BSW	
		Format:	U9-1 Thread Count	
	Specifies the maximum number of simultaneous DS threads allowed to be active. Used to avoid using up the scratch space. Programming the value of the max threads over the number of threads based off number of threads supported in the execution units may improve performance since the architecture allows threads to be buffered between the check for max threads and the actual dispatch into the EU. Programming the max values to a number less than the number of threads supported in the execution units may reduce performance. This field is ignored if DS Function Enable is DISABLED.			
	<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>
	[0,503]		indicating thread count of [1,504]	CHV, BSW
	[0,79]		indicating thread count of [1,80]	CHV, BSW
	20:11	<b>Reserved</b>		
		Project:	CHV, BSW	
		Format:	MBZ	
	10	<b>Statistics Enable</b>		
		Project:	CHV, BSW	

<b>3DSTATE_DS</b>					
	<table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>If ENABLED, this FF unit will engage in statistics gathering. Refer to the Statistics Gathering section. If DISABLED, statistics information associated with this FF stage will be left unchanged. This field is ignored if DS Function Enable is DISABLED.</p>	Format:	Enable		
Format:	Enable				
9:5	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ
Project:	CHV, BSW				
Format:	MBZ				
4	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ
Project:	CHV, BSW				
Format:	MBZ				
3	<p><b>SIMD8 Dispatch Enable</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field is used to specify how DS threads are dispatched. The setting of this field must agree with how the DS kernel was compiled. If ENABLED, SIMD8 DS thread dispatches are performed. The <b>Single Domain Point Dispatch</b> field is ignored. If DISABLED, SIMD4x2 thread dispatches are performed. The <b>Single Domain Point Dispatch</b> field can be used to force single domain point dispatches.</p>	Project:	CHV, BSW	Format:	Enable
Project:	CHV, BSW				
Format:	Enable				
2	<p><b>Compute W Coordinate Enable</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>If ENABLED, the DS unit will (for each domain point) compute <math>W = 1 - (U + V)</math> and pass the result as a floating point value in the DS thread payload. If DISABLED, 0.0 will be passed. This field must only be ENABLED for the tessellation of TRI domains, where UVW coordinates are required. This field must be DISABLED for other domains (as they only require UV coordinates) otherwise the computed W coordinate is UNDEFINED. This field is ignored if DS Function Enable is DISABLED.</p>	Project:	CHV, BSW	Format:	Enable
Project:	CHV, BSW				
Format:	Enable				
1	<p><b>Cache Disable</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Disable</td> </tr> </table> <p>This bit controls the operation of the DS Cache. This field is ignored if DS Function Enable is DISABLED. If the DS Cache is DISABLED and the DS Function is ENABLED, the DS Cache is not used and all incoming domain points will be passed to DS threads. If the DS Cache is ENABLED and the DS Function is ENABLED, incoming domain points that do not hit in the DS Cache will be passed to DS threads. The DS Cache is invalidated whenever the DS Cache becomes DISABLED, whenever the DS Function Enable toggles, and between patches.</p>	Project:	CHV, BSW	Format:	Disable
Project:	CHV, BSW				
Format:	Disable				

<b>3DSTATE_DS</b>											
	0	<p><b>Function Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>If ENABLED, DS threads will be spawned to process incoming domain points which miss in the DS cache. If DISABLED, the DS stage goes into pass-through mode and performs no specific processing. This field is always used.</p> <table border="1" style="width: 100%; background-color: #e6f2ff;"> <tr> <th style="text-align: center;">Programming Notes</th> </tr> <tr> <td>The tessellation stages (HS, TE and DS) must be enabled/disabled as a group. I.e., draw commands can only be issued if all three stages are enabled or all three stages are disabled, otherwise the behavior is UNDEFINED.</td> </tr> </table>	Project:	CHV, BSW	Format:	Enable	Programming Notes	The tessellation stages (HS, TE and DS) must be enabled/disabled as a group. I.e., draw commands can only be issued if all three stages are enabled or all three stages are disabled, otherwise the behavior is UNDEFINED.			
	Project:	CHV, BSW									
	Format:	Enable									
	Programming Notes										
The tessellation stages (HS, TE and DS) must be enabled/disabled as a group. I.e., draw commands can only be issued if all three stages are enabled or all three stages are disabled, otherwise the behavior is UNDEFINED.											
<b>8</b> <b>Project:</b> CHV, BSW	31:28	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ					
	Project:	CHV, BSW									
	Format:	MBZ									
	27	<p><b>Reserved</b></p>									
26:21	<p><b>Vertex URB Entry Output Read Offset</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U6</td> </tr> </table> <p>Specifies the offset (in 256-bit units) at which Vertex URB data is to be read from the URB by SBE.</p> <table border="1" style="width: 100%; background-color: #e6f2ff;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">[0,63]</td> <td></td> </tr> </tbody> </table>	Project:	CHV, BSW	Format:	U6	Value	Name	[0,63]			
Project:	CHV, BSW										
Format:	U6										
Value	Name										
[0,63]											
20:16	<p><b>Vertex URB Entry Output Length</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U5</td> </tr> </table> <p>Specifies the amount of URB data written for each Vertex URB entry, in 256-bit register increments.</p> <table border="1" style="width: 100%; background-color: #e6f2ff;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">[1,16]</td> <td></td> </tr> </tbody> </table> <table border="1" style="width: 100%; background-color: #e6f2ff;"> <tr> <th style="text-align: center;">Programming Notes</th> </tr> <tr> <td>This length does not include the vertex header.</td> </tr> </table>	Project:	CHV, BSW	Format:	U5	Value	Name	[1,16]		Programming Notes	This length does not include the vertex header.
Project:	CHV, BSW										
Format:	U5										
Value	Name										
[1,16]											
Programming Notes											
This length does not include the vertex header.											
15:8	<p><b>User Clip Distance Clip Test Enable Bitmask</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Mask[8]</td> </tr> </table> <p>This 8 bit mask field selects which of the 8 user clip distances against which trivial reject / trivial accept / must clip determination needs to be made. DX10 allows simultaneous use of ClipDistance and Cull Distance test of up to 8 distances.</p>	Project:	CHV, BSW	Format:	Mask[8]						
Project:	CHV, BSW										
Format:	Mask[8]										

<b>3DSTATE_DS</b>					
7:0	<p><b>User Clip Distance Cull Test Enable Bitmask</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Mask[8]</td> </tr> </table> <p>This 8 bit mask field selects which of the 8 user clip distances against which trivial reject / trivial accept determination needs to be made (does not cause a must clip). DX10 allows simultaneous use of ClipDistance and Cull Distance test of up to 8 distances.</p>	Project:	CHV, BSW	Format:	Mask[8]
Project:	CHV, BSW				
Format:	Mask[8]				

## 3DSTATE\_DX9\_CONSTANT\_BUFFER\_POOL\_ALLOC

3DSTATE_DX9_CONSTANT_BUFFER_POOL_ALLOC						
Project:	CHV, BSW					
Source:	RenderCS					
Length Bias:	2					
This command sets up the Gather Pool for Gather Buffers.						
Programming Notes						
This command must only be programmed when resource streamer is enabled thru batch buffer start and MI_RS_CONTROL has not disabled resource streamer.						
DWord	Bit	Description				
0	31:29	<b>Command Type</b>				
		Default Value: 3h GFXPIPE Format: OpCode				
	28:27	<b>Command SubType</b>				
		Default Value: 3h GFXPIPE_3D Format: OpCode GFXPIPE_3D				
	26:24	<b>3D Command Opcode</b>				
		Default Value: 1h 3DSTATE_NONPIPELINED Format: OpCode				
	23:16	<b>3D Command Sub Opcode</b>				
Default Value: 1Bh 3DSTATE_DX9_CONSTANT_BUFFER_POOL_ALLOC Format: OpCode						
15:8	<b>Reserved</b>					
	Format: MBZ					
7:0	<b>DWord Length</b>					
	Format: =n Total Length - 2					
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>2h</td> <td>DWORD_COUNT_n [Default]</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Value	Name	Project	2h	DWORD_COUNT_n [Default]
Value	Name	Project				
2h	DWORD_COUNT_n [Default]	CHV, BSW				
1..2 <b>Project:</b> CHV, BSW	63:48	<b>Reserved</b>				
		Project: CHV, BSW Format: MBZ				
	47:13	<b>Dx9 Constant Buffer Pool Base Address</b>				
		Project: CHV, BSW				



<b>3DSTATE_DX9_CONSTANT_BUFFER_POOL_ALLOC</b>									
	<table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[47:13]Dx9_Constant_Buffer_Pool</td> </tr> <tr> <td colspan="2">Specifies the base address of the Dx9 Constant Buffer pool.</td> </tr> </table>	Format:	GraphicsAddress[47:13]Dx9_Constant_Buffer_Pool	Specifies the base address of the Dx9 Constant Buffer pool.					
Format:	GraphicsAddress[47:13]Dx9_Constant_Buffer_Pool								
Specifies the base address of the Dx9 Constant Buffer pool.									
12:11	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ				
Project:	CHV, BSW								
Format:	MBZ								
10	<p><b>Dx9 Constant Buffer Pool Enable</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>When this bit is set it enables HW Dx9 constants buffers. When this bit is cleared it disables HW Dx9 constant buffers, the local bits for the constant buffers are cleared and the buffers will not be save or restored as part of context.</p>	Project:	CHV, BSW	Format:	Enable				
Project:	CHV, BSW								
Format:	Enable								
9:7	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ				
Project:	CHV, BSW								
Format:	MBZ								
6:0	<p><b>Surface Object Control State</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MEMORY_OBJECT_CONTROL_STATE</td> </tr> </table> <p>Specifies the memory object control state for this surface.</p> <table border="1" style="background-color: #e6f2ff;"> <tr> <td colspan="2" style="text-align: center;"><b>Programming Notes</b></td> </tr> <tr> <td colspan="2">Bit 2 is not programmable and is always zero.</td> </tr> </table>	Project:	CHV, BSW	Format:	MEMORY_OBJECT_CONTROL_STATE	<b>Programming Notes</b>		Bit 2 is not programmable and is always zero.	
Project:	CHV, BSW								
Format:	MEMORY_OBJECT_CONTROL_STATE								
<b>Programming Notes</b>									
Bit 2 is not programmable and is always zero.									
3 <b>Project:</b> CHV, BSW	<p>31:13 <b>Dx9 Constant Buffer Pool Buffer Size</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U19</td> </tr> </table> <p>This field specifies the size of the buffer in 8K pages. Any access which straddle or go past the end of the buffer will return 0. Note that BufferSize=0 indicates that there is no valid data in the buffer.</p> <table border="1" style="background-color: #e6f2ff;"> <tr> <td colspan="2" style="text-align: center;"><b>Restriction</b></td> </tr> <tr> <td colspan="2">Programming size of zero is illegal in the case that the pool is enabled.</td> </tr> </table>	Project:	CHV, BSW	Format:	U19	<b>Restriction</b>		Programming size of zero is illegal in the case that the pool is enabled.	
Project:	CHV, BSW								
Format:	U19								
<b>Restriction</b>									
Programming size of zero is illegal in the case that the pool is enabled.									
12:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ				
Project:	CHV, BSW								
Format:	MBZ								

## 3DSTATE\_DX9\_CONSTANTB\_PS

3DSTATE_DX9_CONSTANTB_PS		
Project:	CHV, BSW	
Source:	RenderCS	
Length Bias:	2	
This command sets a DX9 constant Boolean register for PS.		
<b>Programming Notes</b>		
<ul style="list-style-type: none"> <li>The 3DSTATE_DX9_CONSTANTB_PS is a variable length command.</li> <li>Programming this command in batch buffer requires that all float, integer and boolean constants initialized prior to any commands or events that cause the constants to be written to memory.</li> </ul>		
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 3h GFXPIPE
	Format: OpCode	
	28:27	<b>Command SubType</b>
		Default Value: 3h GFXPIPE_3D
	Format: OpCode	
	26:24	<b>3D Command Opcode</b>
		Default Value: 0h GFXPIPE_PIPELINED
	Format: OpCode	
	23:16	<b>3D Command Sub Opcode</b>
		Default Value: 3Eh 3DSTATE_DX9_CONSTANTB_PS
	Format: OpCode	
	15:8	<b>Reserved</b>
		Project: All
Format: MBZ		
7:0	<b>DWord Length</b>	
	Project: All	
	Format: =n Total Length - 2	
	<b>Value</b>	<b>Name</b>
	0h	[Default]
0h-10h	Excludes DWord (0,1)	

<b>3DSTATE_DX9_CONSTANTB_PS</b>						
1	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ
	Project:	All				
	Format:	MBZ				
	15	<p><b>Global Constant Register</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>When this bit is set the global constant register set will be updated. When this bit is clear the local constant register set will be updated.</p>	Project:	All	Format:	U1
Project:	All					
Format:	U1					
14:4	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ	
Project:	All					
Format:	MBZ					
3:0	<p><b>Constant Register Index</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U4</td> </tr> </table> <p>This field specifies the index of 1st boolean to be updated.</p>	Project:	All	Format:	U4	
Project:	All					
Format:	U4					
2..n	31:0	<p><b>Entry</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 20%;">Format:</td> <td>DX9_CONSTANTB_ENTRY [CHV, BSW]</td> </tr> </table> <p>The nth boolean to be updated.</p>	Format:	DX9_CONSTANTB_ENTRY [CHV, BSW]		
Format:	DX9_CONSTANTB_ENTRY [CHV, BSW]					

## 3DSTATE\_DX9\_CONSTANTB\_VS

3DSTATE_DX9_CONSTANTB_VS			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
This command sets a DX9 constant Boolean register for PS.			
<b>Programming Notes</b>			
<ul style="list-style-type: none"> <li>The 3DSTATE_DX9_CONSTANTB_VS is a variable length command.</li> <li>Programming this command in batch buffer requires that all float, integer and boolean constants initialized prior to any commands or events that cause the constants to be written to memory.</li> </ul>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
Default Value:		0h GFXPIPE_PIPELINED	
Format:		OpCode	
23:16	<b>3D Command Sub Opcode</b>		
	Default Value:	3Dh 3DSTATE_DX9_CONSTANTB_VS	
	Format:	OpCode	
15:8	<b>Reserved</b>		
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Format:	=n Total Length - 2	
	<b>Value</b>	<b>Name</b>	
	0h	[Default]	
	0h-10h	Excludes DWord (0,1)	
1	31:16	<b>Reserved</b>	
		Format:	MBZ

<b>3DSTATE_DX9_CONSTANTB_VS</b>				
	15	<b>Global Constant Register</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Format:</td> <td style="width: 20%;">U1</td> </tr> </table> <p>When this bit is set the global constant register set will be updated. When this bit is clear the local constant register set will be updated.</p>	Format:	U1
	Format:	U1		
	14:4	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Format:</td> <td style="width: 20%;">MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			
3:0	<b>Constant Register Index</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Format:</td> <td style="width: 20%;">U4</td> </tr> </table> <p>This field specifies the index of 1st boolean to be updated.</p>	Format:	U4	
Format:	U4			
2..n	31:0	<b>Entry</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td style="width: 70%;">DX9_CONSTANTB_ENTRY [CHV, BSW]</td> </tr> </table> <p>The nth boolean to be updated.</p>	Format:	DX9_CONSTANTB_ENTRY [CHV, BSW]
Format:	DX9_CONSTANTB_ENTRY [CHV, BSW]			

## 3DSTATE\_DX9\_CONSTANTF\_PS

3DSTATE_DX9_CONSTANTF_PS			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
This command sets one or more DX9 constant float registers for PS.			
Programming Notes			
<ul style="list-style-type: none"> <li>The 3DSTATE_DX9_CONSTANTF_PS is a variable length command.</li> <li>Programming this command in batch buffer requires that all float, integer and boolean constants initialized prior to any commands or events that cause the constants to be written to memory.</li> </ul>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
Default Value:		0h GFXPIPE_PIPELINED	
Format:		OpCode	
23:16	<b>3D Command Sub Opcode</b>		
	Default Value:	3Ah 3DSTATE_DX9_CONSTANTF_PS	
	Format:	OpCode	
15:11	<b>Reserved</b>		
	Format:	MBZ	
10:0	<b>DWord Length</b>		
	Format:	=n Total Length - 2	
	<b>Value</b>	<b>Name</b>	
	1h	Excludes DWord (0,1) <b>[Default]</b>	
	1h-400h	multiples of 4	
1	31:16	<b>Reserved</b>	
		Format:	MBZ

<b>3DSTATE_DX9_CONSTANTF_PS</b>				
	15	<p><b>Global Constant Register</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Format:</td> <td style="width: 20%;">U1</td> </tr> </table> <p>When this bit is set the global constant register set will be updated. When this bit is clear the local constant register set will be updated.</p>	Format:	U1
	Format:	U1		
	14:8	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Format:</td> <td style="width: 20%;">MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			
7:0	<p><b>Constant Register Index</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Format:</td> <td style="width: 20%;">U8</td> </tr> </table> <p>This field specifies the index of 1st 4 component float to be updated.</p>	Format:	U8	
Format:	U8			
2..n	127:0	<p><b>Entry</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td style="width: 70%;">DX9_CONSTANTF_ENTRY [CHV, BSW]</td> </tr> </table> <p>The four components of the nth float to be updated.</p>	Format:	DX9_CONSTANTF_ENTRY [CHV, BSW]
Format:	DX9_CONSTANTF_ENTRY [CHV, BSW]			

## 3DSTATE\_DX9\_CONSTANTF\_VS

3DSTATE_DX9_CONSTANTF_VS			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
This command sets one or more DX9 constant float registers for VS.			
<b>Programming Notes</b>			
<ul style="list-style-type: none"> <li>The 3DSTATE_DX9_CONSTANTF_VS is a variable length command.</li> <li>Programming this command in batch buffer requires that all float, integer and boolean constants initialized prior to any commands or events that cause the constants to be written to memory.</li> </ul>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
Default Value:		0h GFXPIPE_PIPELINED	
Format:		OpCode	
23:16	<b>3D Command Sub Opcode</b>		
	Default Value:	39h 3DSTATE_DX9_CONSTANTF_VS	
	Format:	OpCode	
15:11	<b>Reserved</b>		
	Format:	MBZ	
10:0	<b>DWord Length</b>		
	Format:	=n Total Length - 2	
	<b>Value</b>	<b>Name</b>	
	1h	Excludes DWord (0,1) <b>[Default]</b>	
	1h-400h	multiples of 4	
1	31:16	<b>Reserved</b>	
		Format:	MBZ



<b>3DSTATE_DX9_CONSTANTF_VS</b>			
	<p>15 <b>Global Constant Register</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Format:</td> <td style="width: 20%;">U1</td> </tr> </table> <p>When this bit is set the global constant register set will be updated. When this bit is clear the local constant register set will be updated.</p>	Format:	U1
	Format:	U1	
	<p>14:8 <b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Format:</td> <td style="width: 20%;">MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ		
<p>7:0 <b>Constant Register Index</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Format:</td> <td style="width: 20%;">U8</td> </tr> </table> <p>This field specifies the index of 1st 4 component float to be updated.</p>	Format:	U8	
Format:	U8		
2..n	<p>127:0 <b>Entry</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td style="width: 70%;">DX9_CONSTANTF_ENTRY [CHV, BSW]</td> </tr> </table> <p>The four components of the nth float to be updated.</p>	Format:	DX9_CONSTANTF_ENTRY [CHV, BSW]
Format:	DX9_CONSTANTF_ENTRY [CHV, BSW]		

## 3DSTATE\_DX9\_CONSTANTI\_PS

3DSTATE_DX9_CONSTANTI_PS			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
This command sets one or more DX9 constant integer registers for PS.			
<b>Programming Notes</b>			
<ul style="list-style-type: none"> <li>The 3DSTATE_DX9_CONSTANTI_PS is a variable length command.</li> <li>Programming this command in batch buffer requires that all float, integer and boolean constants initialized prior to any commands or events that cause the constants to be written to memory.</li> </ul>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h GFXPIPE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		3Ch 3DSTATE_DX9_CONSTANTI_PS	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Format:	=n Total Length - 2	
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	1h	[Default]	Excludes DWord (0,1)
	0h-80h	multiples of 4	
1	31:16	<b>Reserved</b>	
		Format:	MBZ

<b>3DSTATE_DX9_CONSTANTI_PS</b>					
	15	<b>Global Constant Register</b>			
		<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>When this bit is set the global constant register set will be updated. When this bit is clear the local constant register set will be updated.</p>	Project:	All	Format:
	Project:	All			
	Format:	U1			
	14:5	<b>Reserved</b>			
		<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:
Project:	All				
Format:	MBZ				
4:0	<b>Constant Register Index</b>				
	<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U5</td> </tr> </table> <p>This field specifies the index of 1st 4 component integer to be updated.</p>	Project:	All	Format:	U5
	Project:	All			
Format:	U5				
2..n	127:0	<b>Entry</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>DX9_CONSTANTI_ENTRY [CHV, BSW]</td> </tr> </table> <p>The four components of the nth float to be updated.</p>	Format:	DX9_CONSTANTI_ENTRY [CHV, BSW]	
Format:	DX9_CONSTANTI_ENTRY [CHV, BSW]				

## 3DSTATE\_DX9\_CONSTANTI\_VS

3DSTATE_DX9_CONSTANTI_VS				
Project:	CHV, BSW			
Source:	RenderCS			
Length Bias:	2			
This command sets one or more DX9 constant integer registers for PS.				
<b>Programming Notes</b>				
<ul style="list-style-type: none"> <li>The 3DSTATE_DX9_CONSTANTI_VS is a variable length command.</li> <li>Programming this command in batch buffer requires that all float, integer and boolean constants initialized prior to any commands or events that cause the constants to be written to memory.</li> </ul>				
DWord	Bit	Description		
0	31:29	<b>Command Type</b>		
		Default Value:	3h GFXPIPE	
		Format:	OpCode	
	28:27	<b>Command SubType</b>		
		Default Value:	3h GFXPIPE_3D	
		Format:	OpCode	
	26:24	<b>3D Command Opcode</b>		
		Default Value:	0h GFXPIPE_PIPELINED	
		Format:	OpCode	
	23:16	<b>3D Command Sub Opcode</b>		
Default Value:		3Bh 3DSTATE_DX9_CONSTANTI_VS		
Format:		OpCode		
15:8	<b>Reserved</b>			
	Project:	All		
	Format:	MBZ		
7:0	<b>DWord Length</b>			
	Format:	=n Total Length - 2		
	<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>
	0h	[Default]	Excludes DWord (0,1)	CHV, BSW
	0h-80h	multiples of 4		CHV, BSW
1	31:16	<b>Reserved</b>		
		Format:	MBZ	

<b>3DSTATE_DX9_CONSTANTI_VS</b>						
	15	<p><b>Global Constant Register</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>When this bit is set the global constant register set will be updated. When this bit is clear the local constant register set will be updated.</p>	Project:	All	Format:	U1
	Project:	All				
	Format:	U1				
	14:5	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ
	Project:	All				
	Format:	MBZ				
4:0	<p><b>Constant Register Index</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U5</td> </tr> </table> <p>This field specifies the index of 1st 4 component integer to be updated.</p>	Project:	All	Format:	U5	
Project:	All					
Format:	U5					
2..n	127:0	<p><b>Entry</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>DX9_CONSTANTI_ENTRY [CHV, BSW]</td> </tr> </table> <p>The four components of the nth float to be updated.</p>	Format:	DX9_CONSTANTI_ENTRY [CHV, BSW]		
Format:	DX9_CONSTANTI_ENTRY [CHV, BSW]					

## 3DSTATE\_DX9\_GENERATE\_ACTIVE\_PS

3DSTATE_DX9_GENERATE_ACTIVE_PS			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
The 3DSTATE_DX9_GENERATE_ACTIVE_PS command is used to generate fixed functions' DX9 Constant Buffer. A DX9 Constant register is made active by writing it out to the constant buffer.			
Programming Notes			
Restriction: The global and local buffers are not initialized after reset. Any data written without being initialized will be undefined. DX9 constant buffers are written due to context save/restore or the Generate Active Command.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
		Default Value:	42h 3DSTATE_DX9_GENERATE_ACTIVE_PS
		Format:	OpCode
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>Dword Length</b>		
	Default Value:	0h Excludes Dword (0,1)	
	Project:	All	
	Format:	=n	
	Total Length - 2		
1	31:24	<b>Reserved</b>	
		Project:	All
		Format:	MBZ

<b>3DSTATE_DX9_GENERATE_ACTIVE_PS</b>											
23:13	<p><b>Pointer to PS Constant Buffer</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>ConstantBufferOffset[23:13]BINDING_TABLE_STATE*</td> </tr> </table> <p>Specifies the 8KB aligned address offset of the PS function's Dx9 constant buffer. This offset is relative to the DX9 Constant buffer Base Address.</p>	Project:	All	Format:	ConstantBufferOffset[23:13]BINDING_TABLE_STATE*						
Project:	All										
Format:	ConstantBufferOffset[23:13]BINDING_TABLE_STATE*										
12	<p><b>DX9 Enable</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>When this bit is set, the Resource Streamer will generate the PS constant buffer according to the DX9 rules:</p> <ol style="list-style-type: none"> <li>Valid local register are made active.</li> <li>Global register becomes active, unless the corresponding local register is valid.</li> <li>Local register valids are reset.</li> </ol> <p>When this bit is cleared, the Resource Streamer will generate the PS constant buffer according to the DX8 rules:</p> <ol style="list-style-type: none"> <li>Global register become active.</li> <li>Local register valids are reset.</li> </ol> <table border="1" style="width: 100%; text-align: center;"> <tr> <td><b>Programming Notes</b></td> </tr> </table> <p>In DX8 mode software will set all constants as globals, even ones locally defined within a shader.</p>	Project:	All	Format:	Enable	Format:	U1	<b>Programming Notes</b>			
Project:	All										
Format:	Enable										
Format:	U1										
<b>Programming Notes</b>											
11	<p><b>Clamp Enable</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>When this bit is set, the Resource Streamer will generate the PS constant buffer with the global values clamped to [-1,1]. When this bit is cleared, the Resource Streamer will generate the PS constant buffer without the global value clamped.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">Programming Notes</th> <th style="text-align: center;">Project</th> </tr> </thead> <tbody> <tr> <td>The clamping only affects the values written out to the constant buffer and not the on-die registers.</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Project:	All	Format:	Enable	Format:	U1	Programming Notes	Project	The clamping only affects the values written out to the constant buffer and not the on-die registers.	CHV, BSW
Project:	All										
Format:	Enable										
Format:	U1										
Programming Notes	Project										
The clamping only affects the values written out to the constant buffer and not the on-die registers.	CHV, BSW										
10:8	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ						
Project:	CHV, BSW										
Format:	MBZ										
7:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ						
Project:	All										
Format:	MBZ										

## 3DSTATE\_DX9\_GENERATE\_ACTIVE\_VS

3DSTATE_DX9_GENERATE_ACTIVE_VS			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
<p>The 3DSTATE_DX9_GENERATE_ACTIVE_VS command is used to generate fixed functions' DX9 Constant Buffer. A DX9 Constant register is made active by writing it out to the constant buffer.</p> <p>Programming Restriction: The global and local buffers are not initialized after reset. Any data written without being initialized will be undefined. DX9 constant buffers are written due to context save/restore or the Generate Active Command.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		41h 3DSTATE_DX9_GENERATE_ACTIVE_VS	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	0h Excludes DWord (0,1)	
	Format:	=n Total Length - 2	
1	31:24	<b>Reserved</b>	
		Format:	MBZ
	23:13	<b>Pointer to VS Constant Buffer</b>	
Format:		ConstantBufferOffset[23:13]	
<p>Specifies the 8KB aligned address offset of the VS function's Dx9 constant buffer. This offset is relative to the DX9 Constant buffer Base Address.</p>			



<b>3DSTATE_DX9_GENERATE_ACTIVE_VS</b>							
12	<p><b>DX9 Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>When this bit is set, the Resource Streamer will generate the VS constant buffer according to the DX9 rules:</p> <ol style="list-style-type: none"> <li>1. Valid local register are made active.</li> <li>2. Global register becomes active, unless the corresponding local register is valid.</li> <li>3. Local register valids are reset.</li> </ol> <p>When this bit is cleared, the Resource Streamer will generate the VS constant buffer according to the DX8 rules:</p> <ol style="list-style-type: none"> <li>1. Global register become active.</li> <li>2. Local register valids are reset.</li> </ol> <table border="1" style="width: 100%; background-color: #e6f2ff;"> <tr> <th colspan="2" style="text-align: center;">Programming Notes</th> </tr> </table> <p>In DX8 mode software will set all constants as globals, even ones locally defined within a shader.</p>	Format:	Enable	Programming Notes			
Format:	Enable						
Programming Notes							
11	<p><b>Clamp Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>When this bit is set, the Resource Streamer will generate the VS constant buffer with the global values clamped to [-1,1]. When this bit is cleared, the Resource Streamer will generate the VS constant buffer without the global value clamped.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 80%; text-align: center;">Programming Notes</th> <th style="text-align: center;">Project</th> </tr> </thead> <tbody> <tr> <td>The clamping only affects the values written out to the constant buffer and not the on-die registers.</td> <td style="text-align: center;">CHV, BSW</td> </tr> </tbody> </table>	Format:	Enable	Programming Notes	Project	The clamping only affects the values written out to the constant buffer and not the on-die registers.	CHV, BSW
Format:	Enable						
Programming Notes	Project						
The clamping only affects the values written out to the constant buffer and not the on-die registers.	CHV, BSW						
10:8	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ		
Project:	CHV, BSW						
Format:	MBZ						
7:0	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ				
Format:	MBZ						

## 3DSTATE\_DX9\_LOCAL\_VALID\_PS

<b>3DSTATE_DX9_LOCAL_VALID_PS</b>			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
This command sets the local valid bits for the DX9 Constant Buffer			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h GFXPIPE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		40h 3DSTATE_DX9_LOCAL_VALID_PS	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>Dword Length</b>		
	Default Value:	9h Excludes Dword (0,1)	
	Project:	CHV, BSW	
	Format:	=n Total Length - 2	
1..8	31:0	<b>Local ConstantF Valid Bits</b>	
		Project:	All
		Format:	U32
Each bit field when set indicates that the corresponding local register is valid. When the bit is clear it indicates the local register is invalid.			
9	31:0	<b>Local ConstantI Valid Bits</b>	
		Project:	CHV, BSW
		Format:	U32
Each bit field when set indicates that the corresponding local register is valid. When the bit is clear it indicates the local register is invalid.			

<b>3DSTATE_DX9_LOCAL_VALID_PS</b>					
10	31:16	<b>Reserved</b>			
		<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:
	Project:	All			
	Format:	MBZ			
	15:0	<b>Local ConstantB Valid Bits</b>			
		<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U16</td> </tr> </table>	Project:	CHV, BSW	Format:
Project:		CHV, BSW			
Format:	U16				
<p>Each bit field when set indicates that the corresponding local register is valid. When the bit is clear it indicates the local register is invalid.</p>					

## 3DSTATE\_DX9\_LOCAL\_VALID\_VS

3DSTATE_DX9_LOCAL_VALID_VS			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
This command sets the local valid bits for the DX9 Constant Buffer			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h GFXPIPE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
		Default Value:	3Fh 3DSTATE_DX9_LOCAL_VALID_VS
		Format:	OpCode
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	9h Excludes DWord (0,1)	
	Project:	CHV, BSW	
	Format:	=n Total Length - 2	
1..8	31:0	<b>Local ConstantF Valid Bits</b>	
		Project:	All
		Format:	U32
Each bit field when set indicates that the corresponding local register is valid. When the bit is clear it indicates the local register is invalid.			
9	31:0	<b>Local ConstantI Valid Bits</b>	
		Project:	CHV, BSW
		Format:	U32
Each bit field when set indicates that the corresponding local register is valid. When the bit is clear it indicates the local register is invalid.			

<b>3DSTATE_DX9_LOCAL_VALID_VS</b>					
10 <b>Project:</b> CHV, BSW	31:16	<b>Reserved</b>			
		<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:
	Project:	CHV, BSW			
	Format:	MBZ			
15:0	<b>Local ConstantB Valid Bits</b>				
	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U16</td> </tr> </table> <p>Each bit field when set indicates that the corresponding local register is valid. When the bit is clear it indicates the local register is invalid.</p>	Project:	CHV, BSW	Format:	U16
Project:	CHV, BSW				
Format:	U16				

## 3DSTATE\_GATHER\_CONSTANT\_DS

<b>3DSTATE_GATHER_CONSTANT_DS</b>		
Project:	CHV, BSW	
Source:	RenderCS	
Length Bias:	2	
<p>This command uses the constant buffer binding table entries to reference constant buffer surface states for the DS unit. The constant data in these is gathered and packed according to a gather table contained in this command.</p>		
<b>Programming Notes</b>		
The HW generated binding table must be enabled to use this command.		
The constant buffer block (group of aligned 16 binding table entries) must be set before this command is issued.		
If the surface type is NULL, any fetch using the surface state base address is not bound by the size of the surface state and the fetch still occurs.		
The length of the gather table is derived from the total length of the command. The command length is in DWords, but the gather table entries are 16 bits in length. If there is an unused odd entry at the end of the command the channel mask should be set to all 0s.		
When a 3DSTATE_GATHER_CONSTANT_* command is used there must be a matching 3DSTATE_CONSTANT_*. Furthermore the 3DSTATE_CONSTANT_* must occur in the same order as the 3DSTATE_GATHER_CONSTANT_*. For example if a 3DSTATE_GATHER_CONSTANT_VS occurs before a 3DSTATE_GATHER_CONSTANT_PS, then the 3DSTATE_CONSTANT_VS must occur before the 3DSTATE_CONSTANT_PS.		
If Gather pool is enabled, there must be a corresponding 3DSTATE_GATHER_CONSTANT command with any 3DSTATE_CONSTANT for any particular shader. To avoid any update to the Gather pool, and yet program the 3DSTATE_CONSTANT for a particular shader, send a 3DSTATE_GATHER_CONSTANT command with all valid bits set to zero.		
<p>The following commands must be executed after any 3DSTATE_GATHER_CONSTANT_* command that has Constant Buffer Valid greater than zero:</p> <ul style="list-style-type: none"> <li>•(N times, minimum number is 4) MI_RS_STORE_DATA_IMM –To force engine idle before executing the next instruction. Write must occur to address that will not corrupt memory:</li> <li>•Resource Streamer Flush = 1</li> <li>•3DSTATE_GATHER_CONSTANT_* (Ensures correct timing of sync between resource streamer and render pipeline)</li> <li>•The Constant Buffer Valid field should be zero and the Dword length equal to 1h.</li> <li>•3DSTATE_CONSTANT_*: •All values match the previous 3DSTATE_CONSTANT_*</li> </ul>		
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 3h GFXPIPE
	Format: OpCode	
	28:27	<b>Command SubType</b>
Default Value: 3h GFXPIPE_3D		
	Format: OpCode	

<b>3DSTATE_GATHER_CONSTANT_DS</b>													
	26:24	<b>3D Command Opcode</b>	Default Value: 0h 3DSTATE_PIPELINED	Format: OpCode									
	23:16	<b>3D Command Sub Opcode</b>	Default Value: 37h 3DSTATE_GATHER_CONSTANT_DS	Format: OpCode									
	15:8	<b>Reserved</b>	Format: MBZ										
	7:0	<b>DWord Length</b>	Format: =n	Total Length - 2									
			<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>DWORD_COUNT_n <b>[Default]</b></td> <td>excludes DWords 0,1</td> </tr> <tr> <td>[1,128]</td> <td>Range</td> <td>1-128 Entries</td> </tr> </tbody> </table>		Value	Name	Description	1	DWORD_COUNT_n <b>[Default]</b>	excludes DWords 0,1	[1,128]	Range	1-128 Entries
Value	Name	Description											
1	DWORD_COUNT_n <b>[Default]</b>	excludes DWords 0,1											
[1,128]	Range	1-128 Entries											
1	31:16	<b>Constant Buffer Valid</b>	Format: U16	This field specifies which of the 16 constant buffers are used in the push constant gather. If a bit is set it indicates the corresponding constant buffer is used. If a bit is clear it indicates the corresponding constant buffer is not used. If this field is zero it indicate that the gather buffer is not used.									
	15:12	<b>Constant Buffer Binding Table Block</b>	Format: U4	This field specifies the 16 entry block constant buffer in the binding table. The constant buffer entry block must be aligned on a 16 entry boundary.									
	11:2	<b>Reserved</b>	Format: MBZ										
	1	<b>Reserved</b>	Project: CHV, BSW	Format: MBZ									
	0	<b>Reserved</b>	Format: MBZ										
2	31:23	<b>Reserved</b>	Format: MBZ										
	22:6	<b>Gather Buffer Offset</b>	Format: GatherBufferOffset[22:6]	This field specifies the offset of the gather buffer within the Gather Pool									

<b>3DSTATE_GATHER_CONSTANT_DS</b>						
		<b>Programming Notes</b>				
		SW increments the offset by the size of the gather buffer in 512 bit units for each gather buffer generated.				
	5	<b>Constant Buffer Dx9 Generate Stall</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>When this bit is set the resource streamer will wait for the Dx9 constant buffer generator to be done before issuing this command to ensure buffer synchronization.</p>	Project:	CHV, BSW	Format:	Enable
Project:	CHV, BSW					
Format:	Enable					
	4	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ
Project:	All					
Format:	MBZ					
	3	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ
Project:	CHV, BSW					
Format:	MBZ					
	2:0	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ
Project:	All					
Format:	MBZ					
3..n	15:0	<b>Entry</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 20%;">Format:</td> <td>GATHER_CONSTANT_ENTRY [CHV, BSW]</td> </tr> </table>	Format:	GATHER_CONSTANT_ENTRY [CHV, BSW]		
Format:	GATHER_CONSTANT_ENTRY [CHV, BSW]					



## 3DSTATE\_GATHER\_CONSTANT\_GS

<b>3DSTATE_GATHER_CONSTANT_GS</b>		
Project:	CHV, BSW	
Source:	RenderCS	
Length Bias:	2	
<p>This command uses the constant buffer binding table entries to reference constant buffer surface states for GS unit. The constant data in these is gathered and packed according to a gather table contained in this command.</p>		
Programming Notes		
<p>The HW generated binding table must be enabled to use this command.</p>		
<p>The constant buffer block (group of aligned 16 binding table entries) must be set before this command is issued.</p>		
<p>If the surface type is NULL, any fetch using the surface state base address is not bound by the size of the surface state and the fetch still occurs.</p>		
<p>The length of the gather table is derived from the total length of the command. The command length is in DWords, but the gather table entries are 16 bits in length. If there is an unused odd entry at the end of the command the channel mask should be set to all 0s.</p>		
<p>When a 3DSTATE_GATHER_CONSTANT_* command is used there must be a matching 3DSTATE_CONSTANT_*. Furthermore the 3DSTATE_CONSTANT_* must occur in the same order as the 3DSTATE_GATHER_CONSTANT_*. For example if a 3DSTATE_GATHER_CONSTANT_VS occurs before a 3DSTATE_GATHER_CONSTANT_PS, then the 3DSTATE_CONSTANT_VS must occur before the 3DSTATE_CONSTANT_PS.</p>		
<p>If Gather pool is enabled, there must be a corresponding 3DSTATE_GATHER_CONSTANT command with any 3DSTATE_CONSTANT for any particular shader. To avoid any update to the Gather pool, and yet program the 3DSTATE_CONSTANT for a particular shader, send a 3DSTATE_GATHER_CONSTANT command with all valid bits set to zero.</p>		
<p>The following commands must be executed after any 3DSTATE_GATHER_CONSTANT_* command that has Constant Buffer Valid greater than zero: •(N times, minimum number is 4) MI_RS_STORE_DATA_IMM –To force engine idle before executing the next instruction. Write must occur to address that will not corrupt memory:                      •Resource Streamer Flush = 1                      •3DSTATE_GATHER_CONSTANT_* (Ensures correct timing of sync between resource streamer and render pipeline)                      •The Constant Buffer Valid field should be zero and the Dword length equal to 1h.                      •3DSTATE_CONSTANT_*: •All values match the previous 3DSTATE_CONSTANT_*</p>		
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 3h GFXPIPE
	Format: OpCode	
	28:27	<b>Command SubType</b>
Default Value: 3h GFXPIPE_3D		
		Format: OpCode

<b>3DSTATE_GATHER_CONSTANT_GS</b>													
	26:24	<b>3D Command Opcode</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Default Value:</td> <td>0h 3DSTATE_PIPELINED</td> </tr> <tr> <td>Format:</td> <td>OpCode</td> </tr> </table>	Default Value:	0h 3DSTATE_PIPELINED	Format:	OpCode							
	Default Value:	0h 3DSTATE_PIPELINED											
	Format:	OpCode											
	23:16	<b>3D Command Sub Opcode</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Default Value:</td> <td>35h 3DSTATE_GATHER_CONSTANT_GS</td> </tr> <tr> <td>Format:</td> <td>OpCode</td> </tr> </table>	Default Value:	35h 3DSTATE_GATHER_CONSTANT_GS	Format:	OpCode							
	Default Value:	35h 3DSTATE_GATHER_CONSTANT_GS											
	Format:	OpCode											
	15:8	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ									
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	7:0	<b>DWord Length</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>=n</td> </tr> </table> <p>Total Length - 2</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 55%;">Name</th> <th style="width: 30%;">Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>DWORD_COUNT_n <b>[Default]</b></td> <td>excludes DWords 0,1</td> </tr> <tr> <td>[1,128]</td> <td>Range</td> <td>1-128 Entries</td> </tr> </tbody> </table>	Format:	=n	Value	Name	Description	1	DWORD_COUNT_n <b>[Default]</b>	excludes DWords 0,1	[1,128]	Range	1-128 Entries
	Format:	=n											
Value	Name	Description											
1	DWORD_COUNT_n <b>[Default]</b>	excludes DWords 0,1											
[1,128]	Range	1-128 Entries											
1	31:16	<b>Constant Buffer Valid</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>U16</td> </tr> </table> <p>This field specifies which of the 16 constant buffers are used in the push constant gather. If a bit is set it indicates the corresponding constant buffer is used. If a bit is clear it indicates the corresponding constant buffer is not used. If this field is zero it indicate that the gather buffer is not used.</p>	Format:	U16									
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	15:12	<b>Constant Buffer Binding Table Block</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>U4</td> </tr> </table> <p>This field specifies the 16 entry block constant buffer in the binding table. The constant buffer entry block must be aligned on a 16 entry boundary.</p>	Format:	U4									
	Format:	U4											
	11:2	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ									
Format:	MBZ												
1	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ								
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Format:	MBZ												
0	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ										
Format:	MBZ												
2	31:23	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ									
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22:6	<b>Gather Buffer Offset</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>GatherBufferOffset[22:6]</td> </tr> </table> <p>This field specifies the offset of the gather buffer within the Gather Pool.</p>	Format:	GatherBufferOffset[22:6]										
Format:	GatherBufferOffset[22:6]												

<b>3DSTATE_GATHER_CONSTANT_GS</b>						
		<b>Programming Notes</b>				
		SW increments the offset by the size of the gather buffer in 512 bit units for each gather buffer generated.				
	5	<b>Constant Buffer Dx9 Generate Stall</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>When this bit is set the resource streamer will wait for the Dx9 constant buffer generator to be done before issuing this command to ensure buffer synchronization.</p>	Project:	CHV, BSW	Format:	Enable
Project:	CHV, BSW					
Format:	Enable					
	4	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ
Project:	All					
Format:	MBZ					
	3	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ
Project:	CHV, BSW					
Format:	MBZ					
	2:0	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ
Project:	All					
Format:	MBZ					
3..n	15:0	<b>Entry</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 20%;">Format:</td> <td>GATHER_CONSTANT_ENTRY [CHV, BSW]</td> </tr> </table>	Format:	GATHER_CONSTANT_ENTRY [CHV, BSW]		
Format:	GATHER_CONSTANT_ENTRY [CHV, BSW]					

## 3DSTATE\_GATHER\_CONSTANT\_HS

<b>3DSTATE_GATHER_CONSTANT_HS</b>		
Project:	CHV, BSW	
Source:	RenderCS	
Length Bias:	2	
<p>This command uses the constant buffer binding table entries to reference constant buffer surface states for HS unit. The constant data in these is gathered and packed according to a gather table contained in this command.</p>		
Programming Notes		
The HW generated binding table must be enabled to use this command.		
The constant buffer block (group of aligned 16 binding table entries) must be set before this command is issued.		
If the surface type is NULL, any fetch using the surface state base address is not bound by the size of the surface state and the fetch still occurs.		
The length of the gather table is derived from the total length of the command. The command length is in DWords, but the gather table entries are 16 bits in length. If there is an unused odd entry at the end of the command the channel mask should be set to all 0s.		
When a 3DSTATE_GATHER_CONSTANT_* command is used there must be a matching 3DSTATE_CONSTANT_*. Furthermore the 3DSTATE_CONSTANT_* must occur in the same order as the 3DSTATE_GATHER_CONSTANT_*. For example if a 3DSTATE_GATHER_CONSTANT_VS occurs before a 3DSTATE_GATHER_CONSTANT_PS, then the 3DSTATE_CONSTANT_VS must occur before the 3DSTATE_CONSTANT_PS.		
If Gather pool is enabled, there must be a corresponding 3DSTATE_GATHER_CONSTANT command with any 3DSTATE_CONSTANT for any particular shader. To avoid any update to the Gather pool, and yet program the 3DSTATE_CONSTANT for a particular shader, send a 3DSTATE_GATHER_CONSTANT command with all valid bits set to zero.		
<p>The following commands must be executed after any 3DSTATE_GATHER_CONSTANT_* command that has Constant Buffer Valid greater than zero:</p> <ul style="list-style-type: none"> <li>•(N times, minimum number is 4) MI_RS_STORE_DATA_IMM –To force engine idle before executing the next instruction. Write must occur to address that will not corrupt memory:</li> <li>•Resource Streamer Flush = 1</li> <li>•3DSTATE_GATHER_CONSTANT_* (Ensures correct timing of sync between resource streamer and render pipeline)</li> <li>•The Constant Buffer Valid field should be zero and the Dword length equal to 1h.</li> <li>•3DSTATE_CONSTANT_*: •All values match the previous 3DSTATE_CONSTANT_*</li> </ul>		
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 3h GFXPIPE
	Format: OpCode	
	28:27	<b>Command SubType</b>
Default Value: 3h GFXPIPE_3D		
		Format: OpCode

<b>3DSTATE_GATHER_CONSTANT_HS</b>													
	26:24	<b>3D Command Opcode</b>	Default Value: 0h 3DSTATE_PIPELINED	Format: OpCode									
	23:16	<b>3D Command Sub Opcode</b>	Default Value: 36h 3DSTATE_GATHER_CONSTANT_HS	Format: OpCode									
	15:8	<b>Reserved</b>	Format: MBZ										
	7:0	<b>DWord Length</b>	Format: =n	Total Length - 2									
			<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>DWORD_COUNT_n <b>[Default]</b></td> <td>excludes DWords 0,1</td> </tr> <tr> <td>[1,128]</td> <td>Range</td> <td>1-128 Entries</td> </tr> </tbody> </table>		Value	Name	Description	1	DWORD_COUNT_n <b>[Default]</b>	excludes DWords 0,1	[1,128]	Range	1-128 Entries
Value	Name	Description											
1	DWORD_COUNT_n <b>[Default]</b>	excludes DWords 0,1											
[1,128]	Range	1-128 Entries											
1	31:16	<b>Constant Buffer Valid</b>	Format: U16	This field specifies which of the 16 constant buffers are used in the push constant gather. If a bit is set it indicates the corresponding constant buffer is used. If a bit is clear it indicates the corresponding constant buffer is not used. If this field is zero it indicate that the gather buffer is not used.									
	15:12	<b>Constant Buffer Binding Table Block</b>	Format: U4	This field specifies the 16 entry block constant buffer in the binding table. The constant buffer entry block must be aligned on a 16 entry boundary.									
	11:2	<b>Reserved</b>	Format: MBZ										
	1	<b>Reserved</b>	Project: CHV, BSW	Format: MBZ									
	0	<b>Reserved</b>	Format: MBZ										
2	31:23	<b>Reserved</b>	Format: MBZ										
	22:6	<b>Gather Buffer Offset</b>	Format: GatherBufferOffset[22:6]	This field specifies the offset of the gather buffer within the Gather Pool.									

<b>3DSTATE_GATHER_CONSTANT_HS</b>						
		<b>Programming Notes</b>				
		SW increments the offset by the size of the gather buffer in 512 bit units for each gather buffer generated.				
	<b>5</b>	<b>Constant Buffer Dx9 Generate Stall</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>When this bit is set the resource streamer will wait for the Dx9 constant buffer generator to be done before issuing this command to ensure buffer synchronization.</p>	Project:	CHV, BSW	Format:	Enable
Project:	CHV, BSW					
Format:	Enable					
	<b>4</b>	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ
Project:	All					
Format:	MBZ					
	<b>3</b>	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ
Project:	CHV, BSW					
Format:	MBZ					
	<b>2:0</b>	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ
Project:	All					
Format:	MBZ					
3..n	15:0	<b>Entry</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 20%;">Format:</td> <td>GATHER_CONSTANT_ENTRY [CHV, BSW]</td> </tr> </table>	Format:	GATHER_CONSTANT_ENTRY [CHV, BSW]		
Format:	GATHER_CONSTANT_ENTRY [CHV, BSW]					

## 3DSTATE\_GATHER\_CONSTANT\_PS

<b>3DSTATE_GATHER_CONSTANT_PS</b>		
Project:	CHV, BSW	
Source:	RenderCS	
Length Bias:	2	
<p>This command uses the constant buffer binding table entries to reference constant buffer surface states for PS unit. The constant data in these is gathered and packed according to a gather table contained in this command.</p>		
Programming Notes		
The HW generated binding table must be enabled to use this command.		
The constant buffer block (group of aligned 16 binding table entries) must be set before this command is issued.		
If the surface type is NULL, any fetch using the surface state base address is not bound by the size of the surface state and the fetch still occurs.		
The length of the gather table is derived from the total length of the command. The command length is in DWords, but the gather table entries are 16 bits in length. If there is an unused odd entry at the end of the command the channel mask should be set to all 0s.		
When a 3DSTATE_GATHER_CONSTANT_* command is used there must be a matching 3DSTATE_CONSTANT_*. Furthermore the 3DSTATE_CONSTANT_* must occur in the same order as the 3DSTATE_GATHER_CONSTANT_*. For example if a 3DSTATE_GATHER_CONSTANT_VS occurs before a 3DSTATE_GATHER_CONSTANT_PS, then the 3DSTATE_CONSTANT_VS must occur before the 3DSTATE_CONSTANT_PS.		
If Gather pool is enabled, there must be a corresponding 3DSTATE_GATHER_CONSTANT command with any 3DSTATE_CONSTANT for any particular shader. To avoid any update to the Gather pool, and yet program the 3DSTATE_CONSTANT for a particular shader, send a 3DSTATE_GATHER_CONSTANT command with all valid bits set to zero.		
<p>The following commands must be executed after any 3DSTATE_GATHER_CONSTANT_* command that has Constant Buffer Valid greater than zero:</p> <ul style="list-style-type: none"> <li>•(N times, minimum number is 4) MI_RS_STORE_DATA_IMM –To force engine idle before executing the next instruction. Write must occur to address that will not corrupt memory:</li> <li>•Resource Streamer Flush = 1</li> <li>•3DSTATE_GATHER_CONSTANT_* (Ensures correct timing of sync between resource streamer and render pipeline)</li> <li>•The Constant Buffer Valid field should be zero and the Dword length equal to 1h.</li> <li>•3DSTATE_CONSTANT_*: •All values match the previous 3DSTATE_CONSTANT_*</li> </ul>		
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 3h GFXPIPE
	Format: OpCode	
	28:27	<b>Command SubType</b>
Default Value: 3h GFXPIPE_3D		
		Format: OpCode

<b>3DSTATE_GATHER_CONSTANT_PS</b>													
1	26:24	<b>3D Command Opcode</b> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>0h 3DSTATE_PIPELINED</td> </tr> <tr> <td>Format:</td> <td>OpCode</td> </tr> </table>	Default Value:	0h 3DSTATE_PIPELINED	Format:	OpCode							
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	Format:	OpCode											
	23:16	<b>3D Command Sub Opcode</b> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>38h 3DSTATE_GATHER_CONSTANT_PS</td> </tr> <tr> <td>Format:</td> <td>OpCode</td> </tr> </table>	Default Value:	38h 3DSTATE_GATHER_CONSTANT_PS	Format:	OpCode							
	Default Value:	38h 3DSTATE_GATHER_CONSTANT_PS											
	Format:	OpCode											
	15:8	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ									
	Format:	MBZ											
	7:0	<b>DWord Length</b> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>=n</td> </tr> </table> <p>Total Length - 2</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 55%;">Name</th> <th style="width: 30%;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">1</td> <td>DWORD_COUNT_n <b>[Default]</b></td> <td>excludes DWords 0,1</td> </tr> <tr> <td style="text-align: center;">[1,128]</td> <td>Range</td> <td>1-128 Entries</td> </tr> </tbody> </table>	Format:	=n	Value	Name	Description	1	DWORD_COUNT_n <b>[Default]</b>	excludes DWords 0,1	[1,128]	Range	1-128 Entries
	Format:	=n											
Value	Name	Description											
1	DWORD_COUNT_n <b>[Default]</b>	excludes DWords 0,1											
[1,128]	Range	1-128 Entries											
31:16	<b>Constant Buffer Valid</b> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>U16</td> </tr> </table> <p>This field specifies which of the 16 constant buffers are used in the push constant gather. If a bit is set it indicates the corresponding constant buffer is used. If a bit is clear it indicates the corresponding constant buffer is not used. If this field is zero it indicate that the gather buffer is not used.</p>	Format:	U16										
Format:	U16												
15:12	<b>Constant Buffer Binding Table Block</b> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>U4</td> </tr> </table> <p>This field specifies the 16 entry block constant buffer in the binding table. The constant buffer entry block must be aligned on a 16 entry boundary.</p>	Format:	U4										
Format:	U4												
11:2	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ										
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1:0	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ								
Project:	CHV, BSW												
Format:	MBZ												
2	31:23	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ									
	Format:	MBZ											
22:6	<b>Gather Buffer Offset</b> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>GatherBufferOffset[22:6]</td> </tr> </table> <p>This field specifies the offset of the gather buffer within the Gather Pool.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #e1eef6;">Programming Notes</th> </tr> </thead> <tbody> <tr> <td>SW increments the offset by the size of the gather buffer in 512 bit units for each gather buffer generated.</td> </tr> </tbody> </table>	Format:	GatherBufferOffset[22:6]	Programming Notes	SW increments the offset by the size of the gather buffer in 512 bit units for each gather buffer generated.								
Format:	GatherBufferOffset[22:6]												
Programming Notes													
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<b>3DSTATE_GATHER_CONSTANT_PS</b>						
	5	<b>Constant Buffer Dx9 Generate Stall</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>When this bit is set the resource streamer will wait for the Dx9 constant buffer generator to be done before issuing this command to ensure buffer synchronization.</p>	Project:	CHV, BSW	Format:	Enable
	Project:	CHV, BSW				
	Format:	Enable				
	4	<b>Constant Buffer Dx9 Enable</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>Enable</td> </tr> </table> <p>When this bit is set it indicates that the constant buffer is a HW generated Dx9 constant buffer. The resource streamer will wait for the Dx9 constant buffer generator to be done before issuing this command to ensure buffer synchronization. Additionally the Dx9 constant buffers are a single buffer but larger than 4KB. Internally the HW will treat the DX9 buffer as 2 constant buffers. When this bit is enable only the 1st constant buffer valid bit is set. The 2nd constant buffer surface pointer will automatically be the 1st pointer + 4KB.</p>	Format:	Enable		
Format:	Enable					
3	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ	
Project:	CHV, BSW					
Format:	MBZ					
2:0	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ			
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3..n	15:0	<b>Entry</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 20%;">Format:</td> <td>GATHER_CONSTANT_ENTRY [CHV, BSW]</td> </tr> </table>	Format:	GATHER_CONSTANT_ENTRY [CHV, BSW]		
Format:	GATHER_CONSTANT_ENTRY [CHV, BSW]					

## 3DSTATE\_GATHER\_CONSTANT\_VS

<b>3DSTATE_GATHER_CONSTANT_VS</b>		
Project:	CHV, BSW	
Source:	RenderCS	
Length Bias:	2	
<p>This command uses the constant buffer binding table entries to reference constant buffer surface states for VS unit. The constant data in these is gathered and packed according to a gather table contained in this command.</p>		
<b>Programming Notes</b>		
The HW generated binding table must be enabled to use this command.		
The constant buffer block (group of aligned 16 binding table entries) must be set before this command is issued.		
If the surface type is NULL, any fetch using the surface state base address is not bound by the size of the surface state and the fetch still occurs.		
The length of the gather table is derived from the total length of the command. The command length is in DWords, but the gather table entries are 16 bits in length. If there is an unused odd entry at the end of the command the channel mask should be set to all 0s.		
When a 3DSTATE_GATHER_CONSTANT_* command is used there must be a matching 3DSTATE_CONSTANT_*. Furthermore the 3DSTATE_CONSTANT_* must occur in the same order as the 3DSTATE_GATHER_CONSTANT_*. For example if a 3DSTATE_GATHER_CONSTANT_VS occurs before a 3DSTATE_GATHER_CONSTANT_PS, then the 3DSTATE_CONSTANT_VS must occur before the 3DSTATE_CONSTANT_PS.		
If Gather pool is enabled, there must be a corresponding 3DSTATE_GATHER_CONSTANT command with any 3DSTATE_CONSTANT for any particular shader. To avoid any update to the Gather pool, and yet program the 3DSTATE_CONSTANT for a particular shader, send a 3DSTATE_GATHER_CONSTANT command with all valid bits set to zero.		
<p>The following commands must be executed after any 3DSTATE_GATHER_CONSTANT_* command that has Constant Buffer Valid greater than zero:</p> <ul style="list-style-type: none"> <li>•(N times, minimum number is 4) MI_RS_STORE_DATA_IMM –To force engine idle before executing the next instruction. Write must occur to address that will not corrupt memory:</li> <li>•Resource Streamer Flush = 1</li> <li>•3DSTATE_GATHER_CONSTANT_* (Ensures correct timing of sync between resource streamer and render pipeline)</li> <li>•The Constant Buffer Valid field should be zero and the Dword length equal to 1h.</li> <li>•3DSTATE_CONSTANT_*: •All values match the previous 3DSTATE_CONSTANT_*</li> </ul>		
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 3h GFXPIPE
	Format: OpCode	
	28:27	<b>Command SubType</b>
Default Value: 3h GFXPIPE_3D		
		Format: OpCode

<b>3DSTATE_GATHER_CONSTANT_VS</b>												
	26:24	<b>3D Command Opcode</b> <table border="1"> <tr> <td>Default Value:</td> <td>0h 3DSTATE_PIPELINED</td> </tr> <tr> <td>Format:</td> <td>OpCode</td> </tr> </table>	Default Value:	0h 3DSTATE_PIPELINED	Format:	OpCode						
	Default Value:	0h 3DSTATE_PIPELINED										
	Format:	OpCode										
	23:16	<b>3D Command Sub Opcode</b> <table border="1"> <tr> <td>Default Value:</td> <td>34h 3DSTATE_GATHER_CONSTANT_VS</td> </tr> <tr> <td>Format:</td> <td>OpCode</td> </tr> </table>	Default Value:	34h 3DSTATE_GATHER_CONSTANT_VS	Format:	OpCode						
Default Value:	34h 3DSTATE_GATHER_CONSTANT_VS											
Format:	OpCode											
15:8	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ									
Format:	MBZ											
7:0	<b>DWord Length</b> <table border="1"> <tr> <td>Format:</td> <td>=n</td> </tr> </table> Total Length - 2 <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>DWORD_COUNT_n <b>[Default]</b></td> <td>excludes DWords 0,1</td> </tr> <tr> <td>[1,128]</td> <td>Range</td> <td>1-128 Entries</td> </tr> </tbody> </table>	Format:	=n	Value	Name	Description	0	DWORD_COUNT_n <b>[Default]</b>	excludes DWords 0,1	[1,128]	Range	1-128 Entries
Format:	=n											
Value	Name	Description										
0	DWORD_COUNT_n <b>[Default]</b>	excludes DWords 0,1										
[1,128]	Range	1-128 Entries										
1	31:16	<b>Constant Buffer Valid</b> <table border="1"> <tr> <td>Format:</td> <td>U16</td> </tr> </table> This field specifies which of the 16 constant buffers are used in the push constant gather. If a bit is set it indicates the corresponding constant buffer is used. If a bit is clear it indicates the corresponding constant buffer is not used. If this field is zero it indicate that the gather buffer is not used.	Format:	U16								
	Format:	U16										
	15:12	<b>Constant Buffer Binding Table Block</b> <table border="1"> <tr> <td>Format:</td> <td>U4</td> </tr> </table> This field specifies the 16 entry block constant buffer in the binding table. The constant buffer entry block must be aligned on a 16 entry boundary.	Format:	U4								
	Format:	U4										
11:2	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ									
Format:	MBZ											
1:0	<b>Reserved</b> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ							
Project:	CHV, BSW											
Format:	MBZ											
2	31:23	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ								
	Format:	MBZ										
22:6	<b>Gather Buffer Offset</b> <table border="1"> <tr> <td>Format:</td> <td>GatherBufferOffset[22:6]</td> </tr> </table> This field specifies the offset of the gather buffer within the Gather Pool. <table border="1"> <thead> <tr> <th style="text-align: center;">Programming Notes</th> </tr> </thead> <tbody> <tr> <td>SW increments the offset by the size of the gather buffer in 512 bit units for each gather buffer generated.</td> </tr> </tbody> </table>	Format:	GatherBufferOffset[22:6]	Programming Notes	SW increments the offset by the size of the gather buffer in 512 bit units for each gather buffer generated.							
Format:	GatherBufferOffset[22:6]											
Programming Notes												
SW increments the offset by the size of the gather buffer in 512 bit units for each gather buffer generated.												

<b>3DSTATE_GATHER_CONSTANT_VS</b>							
	5	<b>Constant Buffer Dx9 Generate Stall</b>	<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>When this bit is set the resource streamer will wait for the Dx9 constant buffer generator to be done before issuing this command to ensure buffer synchronization.</p>	Project:	CHV, BSW	Format:	Enable
	Project:	CHV, BSW					
	Format:	Enable					
	4	<b>Constant Buffer Dx9 Enable</b>	<table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>When this bit is set it indicates that the constant buffer is a HW generated Dx9 constant buffer. The resource streamer will wait for the Dx9 constant buffer generator to be done before issuing this command to ensure buffer synchronization. Additionally the Dx9 constant buffers are a single buffer but larger than 4KB. Internally the HW will treat the DX9 buffer as 2 constant buffers. When this bit is enable only the 1st constant buffer valid bit is set. The 2nd constant buffer surface pointer will automatically be the 1st pointer + 4KB.</p>	Format:	Enable		
Format:	Enable						
3	<b>Reserved</b>	<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ	
Project:	CHV, BSW						
Format:	MBZ						
2:0	<b>Reserved</b>	<table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ			
Format:	MBZ						
3..n	15:0	<b>Entry</b>	<table border="1"> <tr> <td>Format:</td> <td>GATHER_CONSTANT_ENTRY [CHV, BSW]</td> </tr> </table>	Format:	GATHER_CONSTANT_ENTRY [CHV, BSW]		
Format:	GATHER_CONSTANT_ENTRY [CHV, BSW]						

## 3DSTATE\_GATHER\_POOL\_ALLOC

3DSTATE_GATHER_POOL_ALLOC						
Project:	CHV, BSW					
Source:	RenderCS					
Length Bias:	2					
This command sets up the Gather Pool for Gather Buffers.						
<b>Programming Notes</b>						
If the Gather Constant Pool is enabled and RS is enabled, then for each 3DSTATE_CONSTANT_* command there must be a corresponding 3DSTATE_GATHER_CONSTANT_* command. If gather pool is enabled, then Buffer 1 of the 3DSTATE_CONSTANT command address will be an offset from the Gather Pool Base Address.						
The gather constants can only be enabled if the binding table generator is also enabled. This command must only be programmed when resource streamer is enabled thru batch buffer start and MI_RS_CONTROL has not disabled resource streamer.						
DWord	Bit	Description				
0	31:29	<b>Command Type</b>				
		Default Value:	3h GFXPIPE			
		Format:	OpCode			
	28:27	<b>Command SubType</b>				
		Default Value:	3h GFXPIPE_3D			
		Format:	OpCode			
	26:24	<b>3D Command Opcode</b>				
Default Value:		1h 3DSTATE_NONPIPELINED				
Format:		OpCode				
23:16	<b>3D Command Sub Opcode</b>					
	Default Value:	1Ah 3DSTATE_GATHER_POOL_ALLOC				
	Format:	OpCode				
15:8	<b>Reserved</b>					
	Format:	MBZ				
7:0	<b>DWord Length</b>					
	Format:	=n				
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>2h</td> <td>DWORD_COUNT_n [Default]</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Value	Name	Project	2h	DWORD_COUNT_n [Default]
Value	Name	Project				
2h	DWORD_COUNT_n [Default]	CHV, BSW				
1..2 <b>Project:</b> CHV, BSW	63:12	<b>Gather Pool Base Address</b>				
		Project:	CHV, BSW			
		Format:	GraphicsAddress[63:12]Gather_Pool			

<b>3DSTATE_GATHER_POOL_ALLOC</b>													
	GraphicsAddress [63:48] are ignored by the HW and assumed to be in correct canonical form [63:48] == [47].												
	<b>11 Gather Pool Enable</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>When this bit is set it enables HW gathering of push constants. When this bit is cleared it disables HW gathering of push constants.</p>	Project:	CHV, BSW	Format:	Enable								
	Project:	CHV, BSW											
	Format:	Enable											
	<b>10:7 Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ								
Project:	CHV, BSW												
Format:	MBZ												
<b>6:0 Memory Object Control State</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MEMORY_OBJECT_CONTROL_STATE</td> </tr> </table> <p>Specifies the memory object control state for this surface.</p> <table border="1" style="width: 100%; background-color: #e6f2ff;"> <tr> <th colspan="2" style="text-align: center;">Programming Notes</th> </tr> <tr> <td colspan="2">Bit 2 is not programmable and is always zero.</td> </tr> </table>	Project:	CHV, BSW	Format:	MEMORY_OBJECT_CONTROL_STATE	Programming Notes		Bit 2 is not programmable and is always zero.						
Project:	CHV, BSW												
Format:	MEMORY_OBJECT_CONTROL_STATE												
Programming Notes													
Bit 2 is not programmable and is always zero.													
<b>3 Project:</b> CHV, BSW	<b>31:12 Gather Pool Buffer Size</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U20</td> </tr> </table> <p>This field specifies the size of the buffer in 4K pages. Any access which straddle or go past the end of the buffer will return undefined data. Note that BufferSize=0 indicates that there is no valid data in the buffer.</p> <table border="1" style="width: 100%; background-color: #e6f2ff;"> <thead> <tr> <th style="width: 60%;">Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>[0,1048575]</td> <td></td> </tr> </tbody> </table> <table border="1" style="width: 100%; background-color: #e6f2ff;"> <tr> <th colspan="2" style="text-align: center;">Restriction</th> </tr> <tr> <td colspan="2">Programming size of zero is illegal in the case that the pool is enabled.</td> </tr> </table>	Project:	CHV, BSW	Format:	U20	Value	Name	[0,1048575]		Restriction		Programming size of zero is illegal in the case that the pool is enabled.	
	Project:	CHV, BSW											
	Format:	U20											
Value	Name												
[0,1048575]													
Restriction													
Programming size of zero is illegal in the case that the pool is enabled.													
<b>11:0 Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ									
Project:	CHV, BSW												
Format:	MBZ												

## 3DSTATE\_GS

<b>3DSTATE_GS</b>			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
Controls the GS stage hardware.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
Default Value:		0h 3DSTATE_PIPELINED	
Format:		OpCode	
23:16	<b>3D Command Sub Opcode</b>		
	Default Value:	11h 3DSTATE_GS	
	Format:	OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	8h Excludes DWord (0,1)	
	Format:	=n	
1..2	63:6	<b>Kernel Start Pointer</b>	
		Project:	All
		Format:	InstructionBaseOffset[63:6]Kernel
	This field specifies the starting location (1st GEN4 core instruction) of the kernel program run by threads spawned by this FF unit. It is specified as a 64-byte-granular offset from the Instruction Base Address.		
5:0	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
3	31	<b>Single Program Flow</b>	

<b>3DSTATE_GS</b>																							
		<p>Specifies the initial condition of the kernel program as either a single program flow (SIMD<sub>n</sub>x<sub>m</sub> with <math>m = 1</math>) or as multiple program flows (SIMD<sub>n</sub>x<sub>m</sub> with <math>m &gt; 1</math>). See CR0 description in ISA Execution Environment.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disable</td> <td>Single Program Flow disabled</td> </tr> <tr> <td>1h</td> <td>Enable</td> <td>Single Program Flow enabled</td> </tr> </tbody> </table>	Value	Name	Description	0h	Disable	Single Program Flow disabled	1h	Enable	Single Program Flow enabled												
Value	Name	Description																					
0h	Disable	Single Program Flow disabled																					
1h	Enable	Single Program Flow enabled																					
30	<b>Vector Mask Enable</b>	<p>Format: <span style="float: right;">U1 Enumerated Type</span></p> <p>Upon subsequent GS thread dispatches, this bit is loaded into the EU's Vector Mask Enable (VME, cr0.0[3]) thread state. Refer to EU documentation for the definition and use of VME state.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Dmask</td> <td>The EU will use the Dispatch Mask (supplied by the GS stage) for instruction execution.</td> </tr> <tr> <td>1h</td> <td>Vmask</td> <td>The EU will use the Vector Mask (derived from Dispatch Mask) for instruction execution.</td> </tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>Under normal conditions SW shall specify DMask, as the GS stage will provide a Dispatch Mask appropriate to SIMD4x2 or SIMD8 thread execution (as a function of dispatch mode). E.g., for SIMD4x2 execution, the GS stage will generate a Dispatch Mask that is equal to what the EU would use as the Vector Mask. For SIMD8 execution there is no known usage model for use of Vector Mask (as there is for PS shaders).</p>	Value	Name	Description	0h	Dmask	The EU will use the Dispatch Mask (supplied by the GS stage) for instruction execution.	1h	Vmask	The EU will use the Vector Mask (derived from Dispatch Mask) for instruction execution.												
Value	Name	Description																					
0h	Dmask	The EU will use the Dispatch Mask (supplied by the GS stage) for instruction execution.																					
1h	Vmask	The EU will use the Vector Mask (derived from Dispatch Mask) for instruction execution.																					
29:27	<b>Sampler Count</b>	<p>Format: <span style="float: right;">U3</span></p> <p>Specifies how many samplers (in multiples of 4) the geometry shader kernel uses. Used only for prefetching the associated sampler state entries.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>No Samplers</td> <td>No Samplers used</td> </tr> <tr> <td>1h</td> <td>1-4 Samplers</td> <td>Between 1 and 4 samplers used</td> </tr> <tr> <td>2h</td> <td>5-8 Samplers</td> <td>Between 5 and 8 samplers used</td> </tr> <tr> <td>3h</td> <td>9-12 Samplers</td> <td>Between 9 and 12 samplers used</td> </tr> <tr> <td>4h</td> <td>13-16 Samplers</td> <td>Between 13 and 16 samplers used</td> </tr> <tr> <td>5h-7h</td> <td>Reserved</td> <td></td> </tr> </tbody> </table>	Value	Name	Description	0h	No Samplers	No Samplers used	1h	1-4 Samplers	Between 1 and 4 samplers used	2h	5-8 Samplers	Between 5 and 8 samplers used	3h	9-12 Samplers	Between 9 and 12 samplers used	4h	13-16 Samplers	Between 13 and 16 samplers used	5h-7h	Reserved	
Value	Name	Description																					
0h	No Samplers	No Samplers used																					
1h	1-4 Samplers	Between 1 and 4 samplers used																					
2h	5-8 Samplers	Between 5 and 8 samplers used																					
3h	9-12 Samplers	Between 9 and 12 samplers used																					
4h	13-16 Samplers	Between 13 and 16 samplers used																					
5h-7h	Reserved																						
26	<b>Reserved</b>																						
25:18	<b>Binding Table Entry Count</b>	<p>Format: <span style="float: right;">U8</span></p> <p>When <b>HW Generated Binding Table</b> is disabled: Specifies how many binding table entries the kernel uses. Used only for prefetching of the binding table entries and associated surface state. Note: For kernels using a large number of binding table entries, it may be wise to set this field to zero to avoid prefetching too many entries and thrashing the state cache. When <b>HW Generated</b></p>																					



<b>3DSTATE_GS</b>																	
	<p><b>Binding Table</b> bit is enabled: This field indicates which cache lines (512bit units - 32 Binding Table Entry section) should be fetched. Each bit in this field corresponds to a cache line. Only the 1st 4 non-zero Binding Table entries of each 32 Binding Table entry section prefetched will have its surface state prefetched.</p>																
	<b>Programming Notes</b>																
	When HW binding table bit is set, it is assumed that the Binding Table Entry Count field will be generated at JIT time.																
17	<p><b>Thread Dispatch Priority</b> Specifies the priority of the thread for dispatch.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Normal</td> <td>Normal thread dispatch priority</td> </tr> <tr> <td>1h</td> <td>High</td> <td>High thread dispatch priority</td> </tr> </tbody> </table>			Value	Name	Description	0h	Normal	Normal thread dispatch priority	1h	High	High thread dispatch priority					
Value	Name	Description															
0h	Normal	Normal thread dispatch priority															
1h	High	High thread dispatch priority															
16	<p><b>Floating Point Mode</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> </table> <p>Specifies the initial floating point mode used by the dispatched thread.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>IEEE-754</td> <td>Use IEEE-754 Rules</td> <td>All</td> </tr> <tr> <td>1h</td> <td>Alternate</td> <td>Use alternate rules</td> <td>All</td> </tr> </tbody> </table>			Project:	All	Value	Name	Description	Project	0h	IEEE-754	Use IEEE-754 Rules	All	1h	Alternate	Use alternate rules	All
Project:	All																
Value	Name	Description	Project														
0h	IEEE-754	Use IEEE-754 Rules	All														
1h	Alternate	Use alternate rules	All														
15:14	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>			Format:	MBZ												
Format:	MBZ																
13	<p><b>Illegal Opcode Exception Enable</b></p> <table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This bit gets loaded into EU CR0.1[12] (note the bit # difference). See <i>Exceptions and ISA Execution Environment</i>.</p>			Format:	Enable												
Format:	Enable																
12	<p><b>Accesses UAV</b></p> <table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field must be set when GS has a UAV access.</p> <p style="text-align: center;"><b>Programming Notes</b></p> <p>This field must not be set when GS Function Enable is disabled.</p>			Format:	Enable												
Format:	Enable																
11	<p><b>Mask Stack Exception Enable</b></p> <table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This bit gets loaded into EU CR0.1[11]. See <i>Exceptions and ISA Execution Environment</i>.</p>			Format:	Enable												
Format:	Enable																
10:8	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>			Format:	MBZ												
Format:	MBZ																
7	<p><b>Software Exception Enable</b></p> <table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This bit gets loaded into EU CR0.1[13] (note the bit # difference). See <i>Exceptions and ISA Execution Environment</i>.</p>			Format:	Enable												
Format:	Enable																

<b>3DSTATE_GS</b>								
	6	<b>Reserved</b>						
	Format: MBZ							
	5:0	<b>Expected Vertex Count</b>						
Format: U6		Specifies the number of vertices per input object expected by the GS thread. Input topologies not matching this expect value are discarded. Note that <b>DiscardAdjacency</b> is also considered (e.g., if the value programmed is 3 and DiscardAdjacency is set, TRILIST_ADJ and TRISTRIP_ADJ topologies are <u>not</u> discarded as they will pass 3 vertices/object to the GS threads).						
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">[1,32]</td> <td></td> </tr> </tbody> </table>	Value	Name	[1,32]			
Value	Name							
[1,32]								
4..5	63:10	<b>Scratch Space Base Pointer</b>						
	Format: GeneralStateOffset[63:10]ScratchSpace							
	Specifies the starting location of the scratch space area allocated to this FF unit as a 1K-byte aligned offset from the General State Base Address. If required, each thread spawned by this FF unit will be allocated some portion of this space, as specified by Per-Thread Scratch Space. The computed offset of the thread-specific portion will be passed in the thread payload as Scratch Space Offset. The thread is expected to utilize "stateless" DataPort read/write requests to access scratch space, where the DataPort will cause the General State Base Address to be added to the offset passed in the request header. This field is ignored if VS Function Enable is DISABLED.							
	9:4	<b>Reserved</b>						
	Format: MBZ							
	3:0	<b>Per-Thread Scratch Space</b>						
	Format: U4 power of 2 Bytes over 1K Bytes							
	Specifies the amount of scratch space to be allocated to each thread spawned by this FF unit. The driver must allocate enough contiguous scratch space, starting at the Scratch Space Base Pointer, to ensure that the Maximum Number of Threads can each get Per-Thread Scratch Space size without exceeding the driver-allocated scratch space.							
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 20%; text-align: center;">Value</th> <th style="width: 20%; text-align: center;">Name</th> <th style="width: 60%; text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">[0,11]</td> <td></td> <td>indicating [1K Bytes, 2M Bytes]</td> </tr> </tbody> </table>		Value	Name	Description	[0,11]		indicating [1K Bytes, 2M Bytes]
	Value	Name	Description					
[0,11]		indicating [1K Bytes, 2M Bytes]						
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 80%; text-align: center;">Programming Notes</th> <th style="width: 20%; text-align: center;">Project</th> </tr> </thead> <tbody> <tr> <td>Temporary w/a: If Per-Thread Scratch space is greater than 0, GS Number of URB Entries must be less than or equal to the GS Maximum Number of Threads.</td> <td style="text-align: center;">CHV, BSW</td> </tr> </tbody> </table>		Programming Notes	Project	Temporary w/a: If Per-Thread Scratch space is greater than 0, GS Number of URB Entries must be less than or equal to the GS Maximum Number of Threads.	CHV, BSW			
Programming Notes	Project							
Temporary w/a: If Per-Thread Scratch space is greater than 0, GS Number of URB Entries must be less than or equal to the GS Maximum Number of Threads.	CHV, BSW							
6	31	<b>Reserved</b>						
	Project: All							
	Format: MBZ							
	30:29	<b>Reserved</b>						
Project: CHV, BSW								
Format: MBZ								

<b>3DSTATE_GS</b>					
28:23	<p><b>Output Vertex Size</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U6</td> </tr> </table> <p>[0,63] indicating [1,64] 16B units</p> <p>Specifies the size of each vertex stored in the GS output entry (following any Control Header data) as a number of 128-bit units (minus one).</p> <p style="text-align: center;"><b>Programming Notes</b></p> <p>Programming Restrictions: The vertex size must be programmed as a multiple of 32B units with the following exception: Rendering is disabled (as per SOL stage state) and the vertex size output by the GS thread is 16B. If rendering is enabled (as per SOL state) the vertex size must be programmed as a multiple of 32B units. In other words, the only time software can program a vertex size with an odd number of 16B units is when rendering is disabled.</p>	Project:	All	Format:	U6
	Project:	All			
	Format:	U6			
	22:17	<p><b>Output Topology</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>3DPrimType</td> </tr> </table> <p>This field specifies the topology type (3DPrimType) to be associated with GS-thread output vertices (if any).</p>	Project:	All	Format:
Project:		All			
Format:	3DPrimType				
16:11	<p><b>Vertex URB Entry Read Length</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Project:</td> <td>All</td> </tr> </table> <p>Specifies the amount of URB data read and passed in the thread payload for each Vertex URB entry, in 256-bit register increments.</p> <p style="text-align: center;"><b>Programming Notes</b></p> <p>Programming Restriction: This field must be a non-zero value if Include Vertex Handles is cleared to zero.</p>	Project:	All		
	Project:	All			
	10	<p><b>Include Vertex Handles</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Boolean</td> </tr> </table> <p>If set, all the input Vertex URB handles are included in the payload. These are referred to as "pull model" URB handles, as the thread will use them to read from the URB.</p> <p style="text-align: center;"><b>Programming Notes</b></p> <p>Programming Restriction: This field must be set if Vertex URB Entry Read Length is cleared to zero.</p>	Project:	All	Format:
Project:		All			
Format:		Boolean			
9:4	<p><b>Vertex URB Entry Read Offset</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U6</td> </tr> </table> <p>Specifies the offset (in 256-bit units) at which Vertex URB data is to be read from the URB before being included in the thread payload. This offset applies to all Vertex URB entries passed to the thread.</p>	Project:	All	Format:	U6
	Project:	All			
Format:	U6				

<b>3DSTATE_GS</b>												
3:0	<p><b>Dispatch GRF Start Register For URB Data</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U4</td> </tr> </table> <p>Specifies the starting GRF register number for the URB portion (Constant + Vertices) of the thread payload.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 20%;">Value</th> <th style="width: 20%;">Name</th> <th style="width: 40%;">Description</th> <th style="width: 20%;">Project</th> </tr> </thead> <tbody> <tr> <td>[0,15]</td> <td></td> <td>indicating GRF [R0, R15]</td> <td>CHV, BSW</td> </tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>If Include Vertex Handles is enabled (pull or hybrid handles case), then            For simd4x2:            For DUAL_OBJECT dispatch mode this field should be:  <math>((2 * \text{numVerticesPerObject}) + 8 - 1) / 8 + 1</math>            For SINGLE and DUAL_INSTANCE dispatch modes this field should be:  <math>(\text{numVerticesPerObject} + 8 - 1) / 8 + 1</math>            If Include Primitive ID is set, then add 1 to the value obtained by using the above            For simd8: For InstanceCount == 1: numVerticesPerObject + 2 For InstanceCount &gt; 1: 3</p>	Format:	U4	Value	Name	Description	Project	[0,15]		indicating GRF [R0, R15]	CHV, BSW	
	Format:	U4										
Value	Name	Description	Project									
[0,15]		indicating GRF [R0, R15]	CHV, BSW									
7	<p><b>31:24 Maximum Number of Threads</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 40%;">Format:</td> <td style="width: 60%;">U8/2-1 Thread Count</td> </tr> </table> <p>Specifies the maximum number of simultaneous threads allowed to be active. Used to avoid using up the scratch space. Programming the value of the max threads over the number of threads based off number of threads supported in the execution units may improve performance since the architecture allows threads to be buffered between the check for max threads and the actual dispatch into the EU. Programming the max values to a number less than the number of threads supported in the execution units may reduce performance.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 20%;">Value</th> <th style="width: 20%;">Name</th> <th style="width: 60%;">Description</th> </tr> </thead> <tbody> <tr> <td>[3,251]</td> <td></td> <td>indicating thread count of [8,504]</td> </tr> <tr> <td>[3,39]</td> <td></td> <td>indicating thread count of [8,80]</td> </tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>Note that this "Maximum Number of Threads" field is different from the other FF stages in that only an even number of threads.</p>	Format:	U8/2-1 Thread Count	Value	Name	Description	[3,251]		indicating thread count of [8,504]	[3,39]		indicating thread count of [8,80]
	Format:	U8/2-1 Thread Count										
Value	Name	Description										
[3,251]		indicating thread count of [8,504]										
[3,39]		indicating thread count of [8,80]										
23:20	<p><b>Control Data Header Size</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U4</td> </tr> </table> <p>Specifies the number of 32B units of control data header located at the start of the GS URB entry. The value 0 indicates there is no control data header, and Control Data Format is ignored. Software must ensure that the Control Data Header Size is sufficient to accommodate the maximum number of vertices output by the GS thread. It is UNDEFINED for a GS thread to report more output vertices than can be accommodated in a non-zero-sized header. (If the header size is zero, by definition neither cut nor StreamID bits are defined.)</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>[0,8]</td> <td>32B Units</td> </tr> </tbody> </table>	Format:	U4	Value	Name	[0,8]	32B Units					
	Format:	U4										
Value	Name											
[0,8]	32B Units											

## 3DSTATE\_GS

	19:15	<b>Instance Control</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 40%;">Format:</td> <td colspan="4">U5-1 #Instances</td> </tr> </table> <p>Specifies the number of instances (minus one) for each input object. To avoid confusion, this document uses the term "<b>InstanceCount</b>" to refer to InstanceControl+1, with a range of [1,32] If <b>InstanceCount&gt;1</b>, DUAL_OBJECT mode is invalid. Software will likely want to use DUAL_INSTANCE mode for higher performance, but SINGLE mode is also supported. When <b>InstanceCount=1</b> (one instance per object), software can decide which dispatch mode to use. DUAL_OBJECT mode would likely be the best choice for performance, followed by SINGLE mode. DUAL_INSTANCE mode is not recommended but is supported.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #e1eef6;"> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 50%;">Description</th> <th colspan="2"></th> </tr> </thead> <tbody> <tr> <td>[0,31]</td> <td></td> <td>Indicating [1,31] instances</td> <td colspan="2"></td> </tr> </tbody> </table>			Format:	U5-1 #Instances				Value	Name	Description			[0,31]		Indicating [1,31] instances												
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Value	Name	Description																												
[0,31]		Indicating [1,31] instances																												
	14:13	<b>Default Stream Id</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 40%;">Format:</td> <td colspan="4">U2</td> </tr> </table> <p>When the GS is enabled, unless the GS output entry contains StreamID bits in the control header, this field specifies the default StreamID associated with any GS-thread output vertices. When the GS is disabled, StreamID will be output as 0.</p>			Format:	U2																							
Format:	U2																													
	12:11	<b>Dispatch Mode</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 40%;">Format:</td> <td colspan="4">U2</td> </tr> </table> <p>This field specifies how the GS unit dispatches multiple instances and/or multiple objects.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #e1eef6;"> <th style="width: 10%;">Value</th> <th style="width: 10%;">Name</th> <th style="width: 50%;">Description</th> <th style="width: 30%;">Programming Notes</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Single</td> <td>Each thread shades a single instance of one object.</td> <td></td> </tr> <tr> <td>1h</td> <td>Dual Instance</td> <td>Each thread shades possibly two instances of one object. If the InstanceCount is odd, a trailing dispatch of only one instance will be made for each object received. Not recommended if InstanceCount = 1, assuming a kernel optimized for SINGLE or DUAL_OBJECT dispatch would outperform a kernel compiled for DUAL_INSTANCE but only passed one instance.</td> <td></td> </tr> <tr> <td>2h</td> <td>Dual Object</td> <td>Each thread shades one instance of possibly two objects. The GS unit attempt to pair objects together into one dispatch, but under some circumstances only one object may be dispatched (as controlled by the DispatchMask generated by the GS unit). Not valid for objects with more than 16 vertices per object. Not valid if InstanceCount &gt; 1 (more than one instance per object).</td> <td></td> </tr> <tr> <td>3h</td> <td>SIMD8</td> <td>Each thread shades up to 8 different objects or (if InstanceCount &gt; 1) 8 instances of a single object.</td> <td>Not valid for objects with more than 6 vertices per object.</td> </tr> </tbody> </table>			Format:	U2				Value	Name	Description	Programming Notes	0h	Single	Each thread shades a single instance of one object.		1h	Dual Instance	Each thread shades possibly two instances of one object. If the InstanceCount is odd, a trailing dispatch of only one instance will be made for each object received. Not recommended if InstanceCount = 1, assuming a kernel optimized for SINGLE or DUAL_OBJECT dispatch would outperform a kernel compiled for DUAL_INSTANCE but only passed one instance.		2h	Dual Object	Each thread shades one instance of possibly two objects. The GS unit attempt to pair objects together into one dispatch, but under some circumstances only one object may be dispatched (as controlled by the DispatchMask generated by the GS unit). Not valid for objects with more than 16 vertices per object. Not valid if InstanceCount > 1 (more than one instance per object).		3h	SIMD8	Each thread shades up to 8 different objects or (if InstanceCount > 1) 8 instances of a single object.	Not valid for objects with more than 6 vertices per object.
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<b>3DSTATE_GS</b>		
<b>Programming Notes</b>		
The GS must be allocated at least two URB handles or behavior is UNDEFINED for Dual Instance or Dual Object mode.		
At least 8 URB entries must be allocated in order to use SIMD8 DispatchMode.		
10	<b>Statistics Enable</b>	
Format:		Enable
This bit controls whether GS-unit-specific statistics register(s) can be incremented.		
<b>Value</b>	<b>Name</b>	<b>Description</b>
0h	Disable	GS_INVOCATIONS_COUNT and GS_PRIMITIVES_COUNT cannot increment
1h	Enable	GS_INVOCATIONS_COUNT and GS_PRIMITIVES_COUNT can increment
9:5	<b>Invocations Increment Value</b>	
Format:		U5
Specifies how much to increment the GS_INVOCATIONS_COUNT for each instance of each object. This control is provided to allow software to process multiple instances (from an API POV) in a single kernel invocation. In SINGLE dispatch mode, the counter will increment by this value for each dispatch (as it's only one instance of one object). In DUAL_INSTANCE mode, the counter will be incremented by the value if only one instance is included in the dispatch (i.e., the last odd instance), otherwise the counter will be incremented by twice this value. In DUAL_OBJECT dispatch mode, the counter will be incremented by the value if only one object is included in the dispatch (i.e., a forced dispatch of one object), otherwise the counter will be incremented by twice this value.		
<b>Value</b>	<b>Name</b>	<b>Description</b>
[0,31]		indicating an increment of [1,32]
4	<b>Include Primitive ID</b>	
Format:		Boolean
If set, R1 of the payload is written with Primitive ID value(s). If clear, these Primitive ID values are not included in the payload R1.		
3	<b>Hint</b>	
Format:		U1
This state bit is simply passed in GS thread payloads for use by the GS kernel - it has no other impact on hardware operation.		

## 3DSTATE\_GS

**2 Reorder Mode**  
 This bit controls how vertices of triangle objects resulting from TRISTRIP[\_ADJ][\_REV] topologies are [re]ordered when passed in the GS thread payload See Object Vertex Ordering table (below).

Value	Name	Description
0h	LEADING	Reorder the vertices of alternating triangles of a TRISTRIP[_ADJ] such that the leading (first) vertices are in consecutive order starting at v0. A similar reordering is performed on alternating triangles in a TRISTRIP_REV.
1h	TRAILING	Reorder the vertices of alternating triangles of a TRISTRIP[_ADJ] such that the trailing (last) vertices are in consecutive order starting at v2. A similar reordering is performed on alternating triangles in a TRISTRIP_REV.

### Programming Notes

Workaround: reorder mode must be set to REORDER\_LEADING and reordering must be done in the Geometry shader.

### Workaround

Workaround: To work around a CHV, BSW issue, reorder mode must be set to REORDER\_LEADING when GS is disabled.

**1 Discard Adjacency**

Format:	Enable
---------	--------

When set, adjacent vertices will not be passed in the GS payload when objects with adjacency are processed. Instead, only the non-adjacent vertices will be passed in the same fashion as the without-adjacency form of the primitive. Software should set this bit whenever a GS kernel is used that does not expect adjacent vertices. This allows both with-adjacency/without-adjacency variants of the primitive to be submitted to the pipeline (via 3DPRIMITIVE) - the GS unit will silently discard any adjacent vertices and present the GS thread with only the internal object. When clear, adjacent vertices will be passed to the GS thread, as dictated by the incoming primitive type. Software should only clear this bit when a GS kernel is used that does expect adjacent vertices. E.g., if the GS kernel is compiled to expect a TRIANGLE\_ADJ object, software must clear this bit. Software should also clear this bit if the GS kernel expects a POINT or PATCHLIST\_n object (which don't have with-adjacency variants).

The only hardware assistance is to allow the submission of a with-adjacency variant of a primitive when operating with a GS kernel that expects the without-adjacency variant of the object. (E.g., when the GS kernel is compiled to expect a TRIANGLE object, software should set this bit just in case a TRILIST\_ADJ is submitted to the pipeline.) Note that the GS unit is otherwise not aware of the object type that is expected by the GS kernel. It is up to software to ensure that the submitted primitive type (in 3DPRIMITIVE) is otherwise compatible with the object type expected by the GS kernel. (E.g., if the GS kernel expects a LINE\_ADJ object, only LINELIST\_ADJ or LINESTRIP\_ADJ should be submitted, otherwise the GS kernel will produce unpredictable results.) Also note that it is possible to craft a GS kernel which can accept any object type that's thrown at it by first examining the PrimType passed in the payload and then using this info to correctly interpret the number of vertices passed in the payload.

<b>3DSTATE_GS</b>													
8	0	<p><b>Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">Enable</td> </tr> </table> <p>Specifies whether the GS stage is enabled or disabled (pass-through).</p>	Format:	Enable									
	Format:	Enable											
	31	<p><b>Control Data Format</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U1</td> </tr> </table> <p>This field specifies the format of the control data header (if any).</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #e1eef6;"> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 70%;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0h</td> <td style="text-align: center;">CUT</td> <td>The control data header contains cut bits.</td> </tr> <tr> <td style="text-align: center;">1h</td> <td style="text-align: center;">SID</td> <td>The control data header contains StreamID bits. . Output Topology must be set to POINTLIST, or behavior is UNDEFINED.</td> </tr> </tbody> </table>	Format:	U1	Value	Name	Description	0h	CUT	The control data header contains cut bits.	1h	SID	The control data header contains StreamID bits. . Output Topology must be set to POINTLIST, or behavior is UNDEFINED.
	Format:	U1											
	Value	Name	Description										
	0h	CUT	The control data header contains cut bits.										
	1h	SID	The control data header contains StreamID bits. . Output Topology must be set to POINTLIST, or behavior is UNDEFINED.										
	30	<p><b>Static Output</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">Enable</td> </tr> </table> <p>Specifies whether the GS shader outputs a static number of vertices per invocation. If this bit is clear, the number of vertices output by each GS shader invocation is stored by the GS thread at the very beginning of the output URB entry (see GS URB Entry section below).</p>	Format:	Enable									
	Format:	Enable											
	29:27	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">MBZ</td> </tr> </table>	Format:	MBZ									
Format:	MBZ												
26:16	<p><b>Static Output Vertex Count</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td style="width: 70%;">U11 Count of object vertices</td> </tr> </table> <p>If GSEnable is set and StaticOutput is set, this field specifies the total number of vertices output each GS shader invocation. If <b>GSEnable</b> is set and StaticOutput is clear (variable GS output), the total number of vertices output by a GS shader invocation is stored by the thread at the very beginning of the output URB entry. This field is then ignored. (See GS URB Entry below).</p>	Format:	U11 Count of object vertices										
Format:	U11 Count of object vertices												
15:9	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">MBZ</td> </tr> </table>	Format:	MBZ										
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8:0	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">MBZ</td> </tr> </table>	Format:	MBZ										
Format:	MBZ												
9	31:28	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">MBZ</td> </tr> </table>	Format:	MBZ									
	Format:	MBZ											
	27	<p><b>Reserved</b></p>											
26:21	<p><b>Vertex URB Entry Output Read Offset</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U6</td> </tr> </table> <p>Specifies the offset (in 256-bit units) at which Vertex URB data is to be read from the URB by SBE.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #e1eef6;"> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">[0,63]</td> <td></td> </tr> </tbody> </table>	Format:	U6	Value	Name	[0,63]							
Format:	U6												
Value	Name												
[0,63]													



<b>3DSTATE_GS</b>							
20:16	<p><b>Vertex URB Entry Output Length</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>U5</td> </tr> </table> <p>Specifies the amount of URB data written for each Vertex URB entry, in 256-bit register increments.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>[1,16]</td> <td></td> </tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>This length does not include the vertex header.</p>	Format:	U5	Value	Name	[1,16]	
Format:	U5						
Value	Name						
[1,16]							
15:8	<p><b>User Clip Distance Clip Test Enable Bitmask</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>Enable[8]</td> </tr> </table> <p>This 8 bit mask field selects which of the 8 user clip distances against which trivial reject / trivial accept / must clip determination needs to be made. DX10 allows simultaneous use of ClipDistance and Cull Distance test of up to 8 distances.</p>	Format:	Enable[8]				
Format:	Enable[8]						
7:0	<p><b>User Clip Distance Cull Test Enable Bitmask</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>Enable[8]</td> </tr> </table> <p>This 8 bit mask field selects which of the 8 user clip distances against which trivial reject / trivial accept determination needs to be made (does not cause a must clip). DX10 allows simultaneous use of ClipDistance and Cull Distance test of up to 8 distances.</p>	Format:	Enable[8]				
Format:	Enable[8]						

## 3DSTATE\_HIER\_DEPTH\_BUFFER

<b>3DSTATE_HIER_DEPTH_BUFFER</b>				
Project:	CHV, BSW			
Source:	RenderCS			
Length Bias:	2			
Description		Project		
This command sets the surface state of the hierarchical depth buffer, delivered as a pipelined state command. However, the state change pipelining isn't completely transparent (see restriction below).				
WM HW will internally manage the draining pipe and flushing of the caches when this command is issued. The PIPE_CONTROL restrictions are removed.		CHV, BSW		
Programming Notes				
<p><b>Restriction: Prior to changing Depth/Stencil Buffer state (i.e., any combination of 3DSTATE_DEPTH_BUFFER, 3DSTATE_CLEAR_PARAMS, 3DSTATE_STENCIL_BUFFER, 3DSTATE_HIER_DEPTH_BUFFER) SW must first issue a pipelined depth stall (PIPE_CONTROL with Depth Stall bit set, followed by a pipelined depth cache flush (PIPE_CONTROL with Depth Flush Bit set, followed by another pipelined depth stall (PIPE_CONTROL with Depth Stall Bit set), unless SW can otherwise guarantee that the pipeline from WM onwards is already flushed (e.g., via a preceding MI_FLUSH).</b></p>				
DWord	Bit	Description		
0	31:29	<b>Command Type</b>		
		Default Value:	3h GFXPIPE	
		Format:	OpCode	
	28:27	<b>Command SubType</b>		
		Default Value:	3h GFXPIPE_3D	
		Format:	OpCode	
	26:24	<b>3D Command Opcode</b>		
		Default Value:	0h 3DSTATE_PIPELINED	
		Format:	OpCode	
	23:16	<b>3D Command Sub Opcode</b>		
		Default Value:	07h 3DSTATE_HIER_DEPTH_BUFFER	
		Format:	OpCode	
15:8	<b>Reserved</b>			
7:0	<b>Dword Length</b>			
	Format:	=n Total Length - 2		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">3h</td> <td>Excludes Dword (0,1) <b>[Default]</b></td> </tr> </tbody> </table>	Value	Name	3h
Value	Name			
3h	Excludes Dword (0,1) <b>[Default]</b>			

		<b>3DSTATE_HIER_DEPTH_BUFFER</b>		
1	31:25	<b>Hierarchical Depth Buffer Object Control State</b>		
		Project:	CHV, BSW	
		Format:	MEMORY_OBJECT_CONTROL_STATE	
	Specifies the memory object control state for the hierarchical depth buffer.			
24:23	<b>Reserved</b>			
		Project:	CHV, BSW	
		Format:	MBZ	
22:17	<b>Reserved</b>			
		Format:	MBZ	
16:0	<b>Surface Pitch</b>			
		Format:	U17-1 Pitch in Bytes	
	This field specifies the pitch of the hierarchical depth buffer in (#Bytes - 1).			
		<b>Value</b>	<b>Name</b>	
		[127, 1FFFFh]	corresponding to [128B, 128KB] also restricted to a multiple of 128B	
	<b>Programming Notes</b>			
Since this surface is tiled, the pitch specified must be a multiple of the tile pitch, in the range [128B, 128KB].				
2..3	63:0	<b>Surface Base Address</b>		
		Format:	GraphicsAddress[63:0]HierarchicalDepthBuffer	
		This field specifies the address of the buffer in Graphics Memory.		
		<b>Programming Notes</b>		
		The Hierarchical Depth Buffer can only be mapped to Main Memory (uncached).		
4	31:15	<b>Reserved</b>		
		Format:	MBZ	
	14:0	<b>Surface QPitch</b>		
			Project:	CHV, BSW
			Format:	QPitch[16:2]
<b>Description</b>				
This field specifies the distance in rows between array slices. It is used only in the following cases:				
<ul style="list-style-type: none"> <li>• <b>Surface Array</b> is enabled <i>OR</i></li> <li>• <b>Number of Multisamples</b> is not NUMSAMPLES_1 and <b>Multisampled Surface Storage Format</b> set to MSFMT_MSS <i>OR</i></li> <li>• <b>Surface Type</b> is SURFTYPE_CUBE</li> </ul>				

<b>3DSTATE_HIER_DEPTH_BUFFER</b>			
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	[4h, 1FFFCh]		in multiples of 4 (low 2 bits missing)
<b>Programming Notes</b>			
<p>This field must be set to an integer multiple of 8 (QPitch[2] MBZ) Software must ensure that this field is set to a value sufficiently large such that the array slices in the surface do not overlap. Refer to the Memory Data Formats section for information on how surfaces are stored in memory.</p>			

## 3DSTATE\_HS

3DSTATE_HS			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
Controls the HS stage hardware.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		1Bh 3DSTATE_HS	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Format:	=n	
	<b>Value</b>	<b>Name</b>	<b>Project</b>
	7	Excludes DWord (0,1) <b>[Default]</b>	CHV, BSW
1	31:30	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	29:27	<b>Sampler Count</b>	
		Project:	All
		Format:	U3
Specifies how many samplers (in multiples of 4) the HS kernels use. Used only for prefetching the associated sampler state entries.			

<b>3DSTATE_HS</b>				
	<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>
	0h	No Samplers	no samplers used	All
	1h	1-4 Samplers	between 1 and 4 samplers used	All
	2h	5-8 Samplers	between 5 and 8 samplers used	All
	3h	9-12 Samplers	between 9 and 12 samplers used	All
	4h	13-16 Samplers	between 13 and 16 samplers used	All
	5h-7h	Reserved	Reserved	All
26	<b>Reserved</b>			
	Project:		All	
	Format:		MBZ	
25:18	<b>Binding Table Entry Count</b>			
	Project:		All	
	Format:		U8	
	When HW Generated Binding Table is disabled: Specifies how many binding table entries the kernel uses. Used only for prefetching of the binding table entries and associated surface state. Note: For kernels using a large number of binding table entries, it may be wise to set this field to zero to avoid prefetching too many entries and thrashing the state cache.			
	<b>Programming Notes</b>			<b>Project</b>
	When HW binding table bit is set, it is assumed that the Binding Table Entry Count field will be generated at JIT time.			CHV, BSW
17	<b>Thread Dispatch Priority</b>			
	Project:		CHV, BSW	
	Specifies the priority of the thread for dispatch			
	<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>
	0h	Normal	Normal Priority	All
	1h	High	High Priority	All
16	<b>Floating Point Mode</b>			
	Project:		All	
	Specifies the initial floating point mode used by the dispatched thread.			
	<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>
	0h	IEEE-754	Use IEEE-754 Rules	All
	1h	alternate	Use alternate rules	All
15:14	<b>Reserved</b>			
	Project:		All	
	Format:		MBZ	

<b>3DSTATE_HS</b>						
	13	<b>Illegal Opcode Exception Enable</b>	Project: All	Format: Enable	This bit gets loaded into EU CR0.1[12] (note the bit # difference). See Exceptions and ISA Execution Environment.	
	12	<b>Software Exception Enable</b>	Project: CHV, BSW	Format: Enable	This bit gets loaded into EU CRO1[13] (note the bit # difference). See Exceptions and ISA Execution Environment.	
	11:8	<b>Reserved</b>	Project: All	Format: MBZ		
	7:0	<b>Reserved</b>	Project: CHV, BSW	Format: MBZ		
	2	31	<b>Enable</b>	Project: All	Format: Enable	Specifies whether the HS function is enabled or disabled (pass-through). If ENABLED MI_TOPOLOGY_FILTER must be used to silently discard any topologies that the HS kernel is not expecting. E.g., if the HS kernel is expecting PATCHLIST_32 topologies, MI_TOPOLOGY_FILTER must be set to PATCHLIST_32 so only those topologies can reach the enabled HS.
		<b>Programming Notes</b>				
		The tessellation stages (HS, TE and DS) must be enabled/disabled as a group. I.e., draw commands can only be issued if all three stages are enabled or all three stages are disabled, otherwise the behavior is UNDEFINED.				
		30	<b>Reserved</b>	Format: MBZ		
		29	<b>Statistics Enable</b>	Project: All	Format: Enable	This bit controls whether HS-unit-specific statistics register(s) will increment (for each patch).
	28:18	<b>Reserved</b>	Project: All	Format: MBZ		

		<b>3DSTATE_HS</b>													
	17	<b>Reserved</b>													
		Project:	CHV, BSW												
		Format:	MBZ												
	16:8	<b>Maximum Number of Threads</b>													
		Project:	CHV, BSW												
		Format:	U9-1												
		<p>Specifies the maximum number of simultaneous threads allowed to be active. Used to avoid using up the scratch space. Programming the value of the max threads over the number of threads based off number of threads supported in the execution units may improve performance since the architecture allows threads to be buffered between the check for max threads and the actual dispatch into the EU. Programming the max values to a number less than the number of threads supported in the execution units may reduce performance.</p>													
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>[0,503]</td> <td></td> <td>indicating thread count of [1,504]</td> <td>CHV, BSW</td> </tr> <tr> <td>[0,79]</td> <td></td> <td>indicating thread count of [1,80]</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Value	Name	Description	Project	[0,503]		indicating thread count of [1,504]	CHV, BSW	[0,79]		indicating thread count of [1,80]	CHV, BSW	
	Value	Name	Description	Project											
	[0,503]		indicating thread count of [1,504]	CHV, BSW											
[0,79]		indicating thread count of [1,80]	CHV, BSW												
7:4	<b>Reserved</b>														
	Format:	MBZ													
3:0	<b>Instance Count</b>														
	Format:	U4-1													
	<p>This field determines the number of threads (minus one) spawned per input patch. If the HS kernel uses a barrier function, software must restrict the <b>Instance Count</b> to the number of threads that can be simultaneously active within a subslice. Factors which must be considered includes scratch memory availability.</p>														
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[0,15]</td> <td></td> <td>representing [1,16] instances</td> </tr> </tbody> </table>	Value	Name	Description	[0,15]		representing [1,16] instances								
Value	Name	Description													
[0,15]		representing [1,16] instances													
	<b>Programming Notes</b>														
	<p>A pipe_control with cs stall must be sent whenever the HS_STATE.InstanceCount changes from 0 (no instancing) to &gt;0 (instancing) or when there is transition from HS_STATE.Enabled = false to (HS_STATE.Enabled = true &amp;&amp; InstanceCount &gt; 0 ).</p>														
3.4 <b>Project:</b> CHV, BSW	63:6	<b>Kernel Start Pointer</b>													
		Project:	CHV, BSW												
		Format:	InstructionBaseOffset[63:6]Kernel												
		<p>This field specifies the starting location (1st GEN core instruction) of the kernel program run by threads spawned by this FF unit. It is specified as a 64-byte-granular offset from the Instruction Base Address.</p>													
	5:0	<b>Reserved</b>													
		Project:	CHV, BSW												
		Format:	MBZ												



<b>3DSTATE_HS</b>													
5.6 <b>Project:</b> CHV, BSW	63:10	<b>Scratch Space Base Pointer</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>GeneralStateOffset[63:10]</td> </tr> </table> <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[0,31]</td> <td></td> <td>Specifies the location of the scratch space area allocated to this FF unit, specified as a 1KB-granular offset from the General State Base Address. If required, each thread spawned by this FF unit will be allocated some portion of this space, as specified by Per-Thread Scratch Space.</td> </tr> </tbody> </table>	Project:	CHV, BSW	Format:	GeneralStateOffset[63:10]	Value	Name	Description	[0,31]		Specifies the location of the scratch space area allocated to this FF unit, specified as a 1KB-granular offset from the General State Base Address. If required, each thread spawned by this FF unit will be allocated some portion of this space, as specified by Per-Thread Scratch Space.	
		Project:	CHV, BSW										
		Format:	GeneralStateOffset[63:10]										
		Value	Name	Description									
[0,31]		Specifies the location of the scratch space area allocated to this FF unit, specified as a 1KB-granular offset from the General State Base Address. If required, each thread spawned by this FF unit will be allocated some portion of this space, as specified by Per-Thread Scratch Space.											
9:4	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ								
	Project:	CHV, BSW											
	Format:	MBZ											
<b>Per-Thread Scratch Space</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U4 power of 2 Bytes over 1K Bytes</td> </tr> </table> <p>Specifies the amount of scratch space to be allocated to each thread spawned by this FF unit. The driver must allocate enough contiguous scratch space, starting at the Scratch Space Base Pointer, to ensure that the Maximum Number of Threads can each get Per-Thread Scratch Space size without exceeding the driver-allocated scratch space.</p> <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[0,11]</td> <td></td> <td>Indicating[1K Bytes, 2M Bytes</td> </tr> </tbody> </table>	Project:	CHV, BSW	Format:	U4 power of 2 Bytes over 1K Bytes	Value	Name	Description	[0,11]		Indicating[1K Bytes, 2M Bytes			
Project:	CHV, BSW												
Format:	U4 power of 2 Bytes over 1K Bytes												
Value	Name	Description											
[0,11]		Indicating[1K Bytes, 2M Bytes											
7 <b>Project:</b> CHV, BSW	31:29	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ							
		Project:	CHV, BSW										
	Format:	MBZ											
	28	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ									
		Format:	MBZ										
<b>Single Program Flow</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>Specifies the initial condition of the kernel program as either a single program flow (SIMD<sub>n</sub>x<sub>m</sub> with m = 1) or as multiple program flows (SIMD<sub>n</sub>x<sub>m</sub> with m &gt; 1). See CR0 description in <i>ISA Execution Environment</i>.</p> <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Reserved</td> <td></td> </tr> <tr> <td>1h</td> <td>Enable</td> <td>Single Program Flow Enabled</td> </tr> </tbody> </table>	Project:	CHV, BSW	Format:	Enable	Value	Name	Description	0h	Reserved		1h	Enable	Single Program Flow Enabled
Project:	CHV, BSW												
Format:	Enable												
Value	Name	Description											
0h	Reserved												
1h	Enable	Single Program Flow Enabled											
26	<b>Vector Mask Enable</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U1 Enumerated Type</td> </tr> </table>	Project:	CHV, BSW	Format:	U1 Enumerated Type								
	Project:	CHV, BSW											
Format:	U1 Enumerated Type												

<b>3DSTATE_HS</b>												
		<p>Upon subsequent HS thread dispatches, this bit is loaded into the EU's Vector Mask Enable (VME, cr0.0[3]) thread state. Refer to the EU documentation for the definition and use of VME state.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Dmask</td> <td>The EU will use the Dispatch Mask (supplied by the HS stage) for instruction execution.</td> </tr> <tr> <td>1h</td> <td>Vmask</td> <td>The EU will use the Vector Mask (derived from the Dispatch Mask) for instruction execution.</td> </tr> </tbody> </table>		Value	Name	Description	0h	Dmask	The EU will use the Dispatch Mask (supplied by the HS stage) for instruction execution.	1h	Vmask	The EU will use the Vector Mask (derived from the Dispatch Mask) for instruction execution.
Value	Name	Description										
0h	Dmask	The EU will use the Dispatch Mask (supplied by the HS stage) for instruction execution.										
1h	Vmask	The EU will use the Vector Mask (derived from the Dispatch Mask) for instruction execution.										
		<b>Programming Notes</b>										
		<p>Under normal conditions SW shall specify DMask, as the HS stage will provide a Dispatch Mask appropriate to SIMD4x2 or SIMD8 thread execution (as a function of dispatch mode). E.g., for SIMD4x2 thread execution, the HS stage will generate a Dispatch Mask that is equal to what the EU would use as a Vector Mask. For SIMD8 execution there is no known usage model for use of Vector Mask (as there is for PS shaders).</p>										
25	<b>Accesses UAV</b>	<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field must be set when HS has a UAV access</p>		Project:	CHV, BSW	Format:	Enable					
Project:	CHV, BSW											
Format:	Enable											
		<b>Programming Notes</b>										
		<p>This field must not be set when HS Function Enable is disabled.</p>										
24	<b>Include Vertex Handles</b>	<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Boolean</td> </tr> </table> <p>If set, all the input Vertex URB handles are included in payloads. This field is ignored if <b>HS Function Enable</b> is DISABLED.</p>		Project:	CHV, BSW	Format:	Boolean					
Project:	CHV, BSW											
Format:	Boolean											
		<b>Programming Notes</b>										
		<p><b>Programming Restriction:</b> This field must be set if value if <b>Vertex URB Entry Read Length</b> is cleared to zero.</p>										
23:19	<b>Dispatch GRF Start Register For URB Data</b>	<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U5</td> </tr> </table> <p>Specifies the starting GRF register number for the URB portion (Constant + Vertices) of the thread payload. This field is ignored if <b>HS Function Enable</b> is DISABLED.</p>		Project:	CHV, BSW	Format:	U5					
Project:	CHV, BSW											
Format:	U5											
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>[0,31]</td> <td></td> <td>indicating GRF [R0, R31]</td> <td>CHV, BSW</td> </tr> </tbody> </table>		Value	Name	Description	Project	[0,31]		indicating GRF [R0, R31]	CHV, BSW	
Value	Name	Description	Project									
[0,31]		indicating GRF [R0, R31]	CHV, BSW									
18:17	<b>Reserved</b>	<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>		Project:	CHV, BSW	Format:	MBZ					
Project:	CHV, BSW											
Format:	MBZ											

<b>3DSTATE_HS</b>				
16:11	<b>Vertex URB Entry Read Length</b>			
	Project: CHV, BSW			
	Format: U6			
	Specifies the amount of URB data read and passed in the thread payload for each Vertex URB entry, in 256-bit register increments. This field is ignored if HS Function Enable is DISABLED.			
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">[0,63]</td> <td></td> </tr> </tbody> </table>	Value	Name	[0,63]
Value	Name			
[0,63]				
<b>Programming Notes</b>				
<b>Programming Restriction:</b> This field must be a non-zero value if <b>Include Vertex Handles</b> is cleared to zero.				
10	<b>Reserved</b>			
	Project: CHV, BSW			
	Format: MBZ			
9:4	<b>Vertex URB Entry Read Offset</b>			
	Project: CHV, BSW			
	Format: U6			
	Specifies the offset (in 256-bit units) at which Vertex URB data is to be read from the URB before being included in the thread payload. This offset applies to all Vertex URB entries passed to the thread. This field is ignored if HS Function Enable is DISABLED.			
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">[0,63]</td> <td></td> </tr> </tbody> </table>	Value	Name	[0,63]
Value	Name			
[0,63]				
3:1	<b>Reserved</b>			
	Project: CHV, BSW			
	Format: MBZ			
0	<b>Reserved</b>			
	Project: CHV, BSW			
	Format: MBZ			
8 <b>Project:</b> CHV, BSW	31:0	<b>Reserved</b>		
		Project: CHV, BSW		
		Format: MBZ		

## 3DSTATE\_INDEX\_BUFFER

3DSTATE_INDEX_BUFFER			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
<p>This command is used to specify the current IB state used by the VF function. At most one IB is defined and active at any given time. NOTES: The IB must be specified before any RANDOM 3D_PRIMITIVE commands are issued It is possible to have vertex elements source completely from generated ID values and therefore not require any Index Buffer accesses. In this case, VF function will simply ignore the Index Buffer state.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
		Default Value:	0Ah 3DSTATE_INDEX_BUFFER
		Format:	OpCode
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	3h Excludes DWord (0,1)	
	Project:	All	
	Format:	=n Total Length - 2	
1	31:10	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	9:8	<b>Index Format</b>	
		Project:	All
		Format:	U2 Enumerated type
This field specifies the data format of the index buffer. All index values are UNSIGNED.			

<b>3DSTATE_INDEX_BUFFER</b>			
	<b>Value</b>	<b>Name</b>	<b>Project</b>
	0h	BYTE	All
	1h	WORD	All
	2h	DWORD	All
	7	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	6:0	<b>Memory Object Control State</b>	
		Project:	All
		Format:	MEMORY_OBJECT_CONTROL_STATE
		Specifies the memory object control state for this index buffer.	
2..3	63:0	<b>Buffer Starting Address</b>	
		Project:	All
		Format:	GraphicsAddress[63:0]Index_Buffer_Entry
		This field contains the size-aligned (as specified by Index Format) Graphics Address LSBs of the first element of interest within the index buffer. Software must program this value with the combination (sum) of the base address of the memory resource and the byte offset from the base address to the starting structure within the buffer.	
		<b>Programming Notes</b>	
		Index Buffers can only be allocated in linear (not tiled) graphics memory.	
4	31:0	<b>Buffer Size</b>	
		Project:	All
		Format:	U32 Count of bytes
		This field specifies the size of the buffer in bytes. Index accesses which straddle or go past the end of the buffer will return 0..Note that BufferSize=0 indicates that there is no valid data in the buffer.	
		<b>Value</b>	<b>Name</b>
		[0, FFFFFFFh]	

## 3DSTATE\_LINE\_STIPPLE

<b>3DSTATE_LINE_STIPPLE</b>			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
The 3DSTATE_LINE_STIPPLE command is used to specify state variables used in the Line Stipple function.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
Default Value:		1h 3DSTATE_NONPIPELINED	
Format:		OpCode	
23:16	<b>3D Command Sub Opcode</b>		
	Default Value:	08h 3DSTATE_LINE_STIPPLE	
	Format:	OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>Dword Length</b>		
	Default Value:	1h Excludes Dword (0,1)	
	Project:	All	
	Format:	=n Total Length - 2	
1	31	<b>Modify Enable (Current Repeat Counter, Current Stipple Index)</b>	
		Project:	All
		Format:	Enable
	Modify enable for <b>Current Repeat Counter</b> and <b>Current Stipple Index</b> fields.		
	<b>Programming Notes</b>		
It is provided only for HW-generated commands as part of context save/restore. SW must initialize the current repeat counter, current stipple count fields if it sets this bit to enable. SW must set this bit to reset the stipple count.			
	30	<b>Reserved</b>	

<b>3DSTATE_LINE_STIPPLE</b>									
	29:21 <b>Current Repeat Counter</b>								
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U9</td> </tr> </table> <p>This field sets the HW-internal repeat counter state. SW must initialize it to 1 if the modify enable is set.</p>	Project:	All	Format:	U9				
	Project:	All							
	Format:	U9							
20 <b>Reserved</b>									
<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ					
Project:	All								
Format:	MBZ								
	19:16 <b>Current Stipple Index</b>								
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U4</td> </tr> </table> <p>This field sets the HW-internal stipple pattern index. SW must initialize it to 0 if the modify enable is set.</p>	Project:	All	Format:	U4				
	Project:	All							
Format:	U4								
15:0 <b>Line Stipple Pattern</b>									
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>16 bit mask Bit 15 = most significant bit, Bit 0 = least significant bit</td> </tr> </table> <p>Specifies a pattern used to mask out bit specific pixels while rendering lines.</p>	Project:	All	Format:	16 bit mask Bit 15 = most significant bit, Bit 0 = least significant bit				
Project:	All								
Format:	16 bit mask Bit 15 = most significant bit, Bit 0 = least significant bit								
2	31:15 <b>Line Stipple Inverse Repeat Count</b>								
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U1.16</td> </tr> </table> <p>Range: [0.00390625, 1.0]</p> <p>Specifies the inverse (truncated) of the repeat count for the line stipple function.</p>	Project:	All	Format:	U1.16				
	Project:	All							
Format:	U1.16								
14:9 <b>Reserved</b>									
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ				
Project:	All								
Format:	MBZ								
	8:0 <b>Line Stipple Repeat Count</b>								
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U9</td> </tr> </table> <p>Specifies the repeat count for the line stipple function.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>[1, 256]</td> <td></td> </tr> </tbody> </table>	Project:	All	Format:	U9	Value	Name	[1, 256]	
	Project:	All							
Format:	U9								
Value	Name								
[1, 256]									

## 3DSTATE\_MONOFILTER\_SIZE

3DSTATE_MONOFILTER_SIZE			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
This state specifies the size of the filter which is used when filtering in MAPFILTER_MONO mode.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	1h 3DSTATE_NONPIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		11h 3DSTATE_MONOFILTER_SIZE	
Format:		OpCode	
15:8	<b>Reserved</b>		
	7:0	<b>DWord Length</b>	
Default Value:		0h Excludes DWord (0,1)	
Project:		All	
Format:		=n	
Total Length - 2			
1	31:6	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	5:3	<b>Monochrome Filter Width</b>	
		Project:	All
		Format:	U3
This field specifies the width of the monochrome filter. It is ignored if the monochrome filter is not enabled.			
<b>Value</b>		<b>Name</b>	
[1,7]			



<b>3DSTATE_MONOFILTER_SIZE</b>		
2:0	<b>Monochrome Filter Height</b>	
	Project: All	
	Format: U3	
	This field specifies the height of the monochrome filter. It is ignored if the monochrome filter is not enabled.	
	<b>Value</b>	<b>Name</b>
[1,7]		

## 3DSTATE\_MULTISAMPLE

3DSTATE_MULTISAMPLE			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
The 3DSTATE_MULTISAMPLE command is used to specify multisample state associated with the current render target/depth buffer.			
<b>Programming Notes</b>			
It is illegal to render to surfaces with multiple different values of the state fields in this command.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		0Dh 3DSTATE_MULTISAMPLE	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>Dword Length</b>		
	Default Value:	0h	
	Project:	All	
	Format:	=n Total Length - 2	
	Excludes Dword (0,1)		
1	31:6	<b>Reserved</b>	
		Project:	All
		Format:	MBZ

## 3DSTATE\_MULTISAMPLE

5	<b>Pixel Position Offset Enable</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td colspan="3">CHV, BSW</td> </tr> <tr> <td>Format:</td> <td colspan="3">U1</td> </tr> </table> <p>Enables the device to offset pixel positions by 0.5 both in horizontal and vertical directions.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th colspan="4" style="text-align: center; background-color: #e1eef6;">Programming Notes</th> </tr> <tr> <td colspan="4">                     Setting this field along with setting the Pixel Location to upper left and number of multisamples to greater than one will cause the device to offset pixel positions by 0.5 both in horizontal and vertical directions.                      It is to be noted this is done to adjust the pixel co-ordinate system to DX9 like, so any WM_HZ_OP screen space rectangles (eg: legacy HiZ Clear, Resolve etc) generated internally by driver in this mode needs to be aware of this offset adjustment and send the rectangles according to alignment restriction taking this offset adjustment into consideration.                      SW can choose to set this bit only for DX9 API. DX10/OGL API's should not have any effect by setting or not setting this bit.                 </td> </tr> </table>			Project:	CHV, BSW			Format:	U1			Programming Notes				Setting this field along with setting the Pixel Location to upper left and number of multisamples to greater than one will cause the device to offset pixel positions by 0.5 both in horizontal and vertical directions. It is to be noted this is done to adjust the pixel co-ordinate system to DX9 like, so any WM_HZ_OP screen space rectangles (eg: legacy HiZ Clear, Resolve etc) generated internally by driver in this mode needs to be aware of this offset adjustment and send the rectangles according to alignment restriction taking this offset adjustment into consideration. SW can choose to set this bit only for DX9 API. DX10/OGL API's should not have any effect by setting or not setting this bit.																			
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Format:	U1																																			
Programming Notes																																				
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4	<b>Pixel Location</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td colspan="3">All</td> </tr> <tr> <td>Format:</td> <td colspan="3">U1</td> </tr> </table> <p>This field specifies where the device evaluates "pixel" (vs. centroid or sample) values/attributes.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 20%;">Name</th> <th style="width: 50%;">Description</th> <th style="width: 15%;"></th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>CENTER</td> <td>Use the pixel center (0.5, 0.5 offset)</td> <td></td> </tr> <tr> <td>1h</td> <td>UL_CORNER</td> <td>Use the pixel upper-left corner</td> <td></td> </tr> </tbody> </table> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th colspan="3" style="text-align: center; background-color: #e1eef6;">Programming Notes</th> <th style="text-align: center; background-color: #e1eef6;">Project</th> </tr> </thead> <tbody> <tr> <td colspan="3">                     The programming of this field is assumed to be a function of the API being supported. Specifically, it is expected that OpenGL and DX10+ APIs require CENTER selection, while DX9- APIs require UL_CORNER selection.                 </td> <td></td> </tr> <tr> <td colspan="3">                     When 3DSTATE_RASTER::<b>ForcedSampleCount</b> is other than NUMRASTSAMPLES_0, this field must be 0h.                 </td> <td>CHV, BSW</td> </tr> </tbody> </table>			Project:	All			Format:	U1			Value	Name	Description		0h	CENTER	Use the pixel center (0.5, 0.5 offset)		1h	UL_CORNER	Use the pixel upper-left corner		Programming Notes			Project	The programming of this field is assumed to be a function of the API being supported. Specifically, it is expected that OpenGL and DX10+ APIs require CENTER selection, while DX9- APIs require UL_CORNER selection.				When 3DSTATE_RASTER:: <b>ForcedSampleCount</b> is other than NUMRASTSAMPLES_0, this field must be 0h.			CHV, BSW
Project:	All																																			
Format:	U1																																			
Value	Name	Description																																		
0h	CENTER	Use the pixel center (0.5, 0.5 offset)																																		
1h	UL_CORNER	Use the pixel upper-left corner																																		
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When 3DSTATE_RASTER:: <b>ForcedSampleCount</b> is other than NUMRASTSAMPLES_0, this field must be 0h.			CHV, BSW																																	
3:1	<b>Number of Multisamples</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td colspan="3">All</td> </tr> <tr> <td>Format:</td> <td colspan="3">U3</td> </tr> </table> <p>This field specifies how many samples/pixel exist in all RTs and the Depth Buffer, as <math>\log_2(\#samples)</math>. This field is valid regardless of the setting of <b>Multisample Rasterization Mode</b>.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 50%;">Description</th> <th style="width: 20%;">Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>1</td> <td>1 sample/pixel</td> <td>All</td> </tr> <tr> <td>1h</td> <td>2</td> <td>2 samples/pixel</td> <td>CHV, BSW</td> </tr> <tr> <td>2h</td> <td>4</td> <td>4 samples/pixel</td> <td>All</td> </tr> <tr> <td>3h</td> <td>8</td> <td>8 samples/pixel</td> <td>CHV, BSW</td> </tr> <tr> <td>5h-7h</td> <td>Reserved</td> <td></td> <td>All</td> </tr> </tbody> </table>			Project:	All			Format:	U3			Value	Name	Description	Project	0h	1	1 sample/pixel	All	1h	2	2 samples/pixel	CHV, BSW	2h	4	4 samples/pixel	All	3h	8	8 samples/pixel	CHV, BSW	5h-7h	Reserved		All
Project:	All																																			
Format:	U3																																			
Value	Name	Description	Project																																	
0h	1	1 sample/pixel	All																																	
1h	2	2 samples/pixel	CHV, BSW																																	
2h	4	4 samples/pixel	All																																	
3h	8	8 samples/pixel	CHV, BSW																																	
5h-7h	Reserved		All																																	

<b>3DSTATE_MULTISAMPLE</b>		
		<b>Programming Notes</b>
		The setting of this field must match the <b>Number of Multisamples</b> field in SURFACE_STATE of all bound render targets.
	0	<b>Reserved</b>
		Project: All
		Format: MBZ

## 3DSTATE\_POLY\_STIPPLE\_OFFSET

3DSTATE_POLY_STIPPLE_OFFSET			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
The 3DSTATE_POLY_STIPPLE_OFFSET command is used to specify the origin of the repeated screen-space Polygon Stipple Pattern as an X, Y offset from the Color Buffer origin.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	1h 3DSTATE_NONPIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		06h 3DSTATE_POLY_STIPPLE_OFFSET	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>Dword Length</b>		
	Default Value:	0h Excludes Dword (0,1)	
	Project:	All	
	Format:	=n Total Length - 2	
1	31:13	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	12:8	<b>Polygon Stipple X Offset</b>	
		Project:	All
		Format:	U5
Specifies a 5 bit x address offset in the poly stipple pattern			
	<b>Value</b>	<b>Name</b>	
	[0,31]		

<b>3DSTATE_POLY_STIPPLE_OFFSET</b>										
	7:5	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ				
	Project:	All								
Format:	MBZ									
	4:0	<b>Polygon Stipple Y Offset</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U5</td> </tr> </table> <p>Specifies a 5 bit y address offset in the poly stipple pattern</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">[0,31]</td> <td></td> </tr> </tbody> </table>	Project:	All	Format:	U5	Value	Name	[0,31]	
Project:	All									
Format:	U5									
Value	Name									
[0,31]										

## 3DSTATE\_POLY\_STIPPLE\_PATTERN

3DSTATE_POLY_STIPPLE_PATTERN			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
The 3DSTATE_POLY_STIPPLE_PATTERN command is used to specify the 32x32 Polygon Stipple Pattern used in the Polygon Stipple function of the WM unit.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	1h 3DSTATE_NONPIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		07h 3DSTATE_POLY_STIPPLE_PATTERN	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>Dword Length</b>		
	Default Value:	1Fh Excludes Dword (0,1)	
	Project:	All	
	Format:	=n Total Length - 2	
1..32	31:0	<b>Pattern Row</b> Project: All Format: 32 bit mask Bit 31 = upper left corner, Bit 0 = upper right corner of first row. Specifies a pattern used by Polygon Stipple to mask out specific pixels of every 32x32 area rendered.	

## 3DSTATE\_PS\_BLEND

3DSTATE_PS_BLEND			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		4Dh 3DSTATE_PS_BLEND	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Format:	=n	
	Total Length - 2		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0h	[Default]	Excludes Dword (0,1)
1	31	<b>Alpha To Coverage Enable</b>	
		Project:	All
		Format:	Enable
	If set, indicates that AlphaToCoverage is on RT[0], since this bit must be set the same for all RTs in the MRT case.		
	30	<b>Has Writeable RT</b>	
Project:		All	
Format:		Enable	
When set indicates the there is at least one non-null RT w/ at least one channel write enabled			



<b>3DSTATE_PS_BLEND</b>					
29	<p><b>Color Buffer Blend Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>When set indicates that RT[0] has color buffer blend enabled.</p>	Project:	All	Format:	Enable
Project:	All				
Format:	Enable				
28:24	<p><b>Source Alpha Blend Factor</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>3D_Color_Buffer_Blend_Factor</td> </tr> </table> <p>Indicates the "source factor" in alpha Color Buffer Blending stage for RT[0]</p>	Project:	All	Format:	3D_Color_Buffer_Blend_Factor
Project:	All				
Format:	3D_Color_Buffer_Blend_Factor				
23:19	<p><b>Destination Alpha Blend Factor</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>3D_Color_Buffer_Blend_Factor</td> </tr> </table> <p>Indicates the "destination factor" in alpha Color Buffer Blending stage for RT[0]</p>	Project:	All	Format:	3D_Color_Buffer_Blend_Factor
Project:	All				
Format:	3D_Color_Buffer_Blend_Factor				
18:14	<p><b>Source Blend Factor</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>3D_Color_Buffer_Blend_Factor</td> </tr> </table> <p>Indicates the "source factor" in Color Buffer Blending stage for RT[0]</p>	Project:	All	Format:	3D_Color_Buffer_Blend_Factor
Project:	All				
Format:	3D_Color_Buffer_Blend_Factor				
13:9	<p><b>Destination Blend Factor</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>3D_Color_Buffer_Blend_Factor</td> </tr> </table> <p>Indicates the "destination factor" in Color Buffer Blending stage for RT[0]</p>	Project:	All	Format:	3D_Color_Buffer_Blend_Factor
Project:	All				
Format:	3D_Color_Buffer_Blend_Factor				
8	<p><b>Alpha Test Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>Indicates the AlphaTestEnable for RT[0]</p>	Project:	All	Format:	Enable
Project:	All				
Format:	Enable				
7	<p><b>Independent Alpha Blend Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>Indicates the Independent Alpha Blend Enable for RT[0] When enabled, the other fields in this instruction control the combination of the alpha components in the Color Buffer Blend stage. When disabled, the alpha components are combined in the same fashion as the color components.</p>	Project:	All	Format:	Enable
Project:	All				
Format:	Enable				
6:0	<p><b>Reserved</b></p>				

## 3DSTATE\_PS

3DSTATE_PS			
Project:		CHV, BSW	
Source:		RenderCS	
Length Bias:		2	
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		20h 3DSTATE_PS	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	0Ah Excludes DWord (0,1)	
	Project:	All	
	Format:	=n Total Length - 2	
1..2	63:6	<b>Kernel Start Pointer 0</b>	
		Project:	All
		Format:	InstructionBaseOffset[63:6]Kernel
		Specifies the 64-byte aligned address offset of the first instruction in the kernel[0]. This pointer is relative to the <b>Instruction Base Address</b> .	
	5:0	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
3	31	<b>Single Program Flow</b>	
		Project:	All

### 3DSTATE\_PS

		<p>Single Program Flow (SPF) specifies the initial condition of the kernel program as either a single program flow (SIMDn<sub>xm</sub> with m = 1) or as multiple program flows (SIMDn<sub>xm</sub> with m &gt; 1). See CR0 description in ISA Execution Environment.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 55%;">Description</th> <th style="width: 15%;">Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Multiple</td> <td>Multiple Program Flows</td> <td>All</td> </tr> <tr> <td>1h</td> <td>Single</td> <td>Single Program Flows</td> <td>All</td> </tr> </tbody> </table>			Value	Name	Description	Project	0h	Multiple	Multiple Program Flows	All	1h	Single	Single Program Flows	All																						
Value	Name	Description	Project																																			
0h	Multiple	Multiple Program Flows	All																																			
1h	Single	Single Program Flows	All																																			
30	<b>Vector Mask Enable</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U1 Enumerated Type</td> </tr> </table> <p>When SPF=0, Vector Mask Enable (VME) specifies which mask to use to initialize the initial channel enables. When SPF=1, VME specifies which mask to use to generate execution channel enables.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 55%;">Description</th> <th style="width: 15%;">Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Dmask</td> <td>Channels are enabled based on the dispatch mask</td> <td>All</td> </tr> <tr> <td>1h</td> <td>Vmask</td> <td>Channels are enabled based on the vector mask</td> <td>All</td> </tr> </tbody> </table>			Project:	All	Format:	U1 Enumerated Type	Value	Name	Description	Project	0h	Dmask	Channels are enabled based on the dispatch mask	All	1h	Vmask	Channels are enabled based on the vector mask	All																		
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29:27	<b>Sampler Count</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> </table> <p>Specifies how many samplers (in multiples of 4) the vertex shader 0 kernel uses. Used only for prefetching the associated sampler state entries.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 55%;">Description</th> <th style="width: 15%;">Project</th> </tr> </thead> <tbody> <tr> <td>[0,4]</td> <td></td> <td></td> <td></td> </tr> <tr> <td>0h</td> <td>No Samplers</td> <td>no samplers used</td> <td>All</td> </tr> <tr> <td>1h</td> <td>1-4 Samplers</td> <td>between 1 and 4 samplers used</td> <td>All</td> </tr> <tr> <td>2h</td> <td>5-8 Samplers</td> <td>between 5 and 8 samplers used</td> <td>All</td> </tr> <tr> <td>3h</td> <td>9-12 Samplers</td> <td>between 9 and 12 samplers used</td> <td>All</td> </tr> <tr> <td>4h</td> <td>13-16 Samplers</td> <td>between 13 and 16 samplers used</td> <td>All</td> </tr> <tr> <td>5h-7h</td> <td></td> <td>Reserved</td> <td>All</td> </tr> </tbody> </table>			Project:	All	Value	Name	Description	Project	[0,4]				0h	No Samplers	no samplers used	All	1h	1-4 Samplers	between 1 and 4 samplers used	All	2h	5-8 Samplers	between 5 and 8 samplers used	All	3h	9-12 Samplers	between 9 and 12 samplers used	All	4h	13-16 Samplers	between 13 and 16 samplers used	All	5h-7h		Reserved	All
Project:	All																																					
Value	Name	Description	Project																																			
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5h-7h		Reserved	All																																			
26	<b>Single Precision Denormal Mode</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> </table> <p>Specifies the single precision denormal mode used by the dispatched thread.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 55%;">Description</th> <th style="width: 15%;">Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Flushed to Zero</td> <td>Single Precision denormals are flushed to zero</td> <td>All</td> </tr> <tr> <td>1h</td> <td>Retained</td> <td>Single Precision denormals are retained</td> <td>All</td> </tr> </tbody> </table>			Project:	All	Value	Name	Description	Project	0h	Flushed to Zero	Single Precision denormals are flushed to zero	All	1h	Retained	Single Precision denormals are retained	All																				
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25:18	<b>Binding Table Entry Count</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td colspan="2" style="text-align: center;"><b>Description</b></td> </tr> </table>			Project:	All	<b>Description</b>																															
Project:	All																																					
<b>Description</b>																																						

### 3DSTATE\_PS

		<p>Specifies how many binding table entries the kernel uses. Used only for prefetching of the binding table entries and associated surface state. <b>Note:</b> For kernels using a large number of binding table entries, it may be advantageous to set this field to zero to avoid prefetching too many entries and thrashing the state cache. This field is ignored if [PS Function Enable] is DISABLED.</p> <p>When [HW Generated Binding Table] bit is enabled: This field indicates which cache lines (512bit units - 32 Binding Table Entry section) should be fetched. Each bit in this field corresponds to a cache line. Only the 1st 4 non-zero Binding Table entries of each 32 Binding Table entry section prefetched will have its surface state prefetched. See 3D Pipeline for more information.</p>																								
		<b>Programming Notes</b>																								
		When HW binding table bit is set, it is assumed that the Binding Table Entry Count field will be generated at JIT time.																								
17	<b>Thread Dispatch Priority</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Project:</td> <td style="width: 30%;">All</td> </tr> </table> <p>Specifies the priority of the thread for dispatch.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 40%;">Description</th> <th style="width: 30%;">Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Normal</td> <td>Normal Priority</td> <td>All</td> </tr> <tr> <td>1h</td> <td>High</td> <td>High Priority</td> <td>All</td> </tr> </tbody> </table>			Project:	All	Value	Name	Description	Project	0h	Normal	Normal Priority	All	1h	High	High Priority	All								
Project:	All																									
Value	Name	Description	Project																							
0h	Normal	Normal Priority	All																							
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16	<b>Floating Point Mode</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Project:</td> <td style="width: 30%;">All</td> </tr> </table> <p>Specifies the floating point mode used by the dispatched thread.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 40%;">Description</th> <th style="width: 30%;">Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>IEEE-754</td> <td>Use IEEE-754 rules</td> <td>All</td> </tr> <tr> <td>1h</td> <td>Alternate</td> <td>Use alternate rules</td> <td>All</td> </tr> </tbody> </table>			Project:	All	Value	Name	Description	Project	0h	IEEE-754	Use IEEE-754 rules	All	1h	Alternate	Use alternate rules	All								
Project:	All																									
Value	Name	Description	Project																							
0h	IEEE-754	Use IEEE-754 rules	All																							
1h	Alternate	Use alternate rules	All																							
15:14	<b>Rounding Mode</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Project:</td> <td style="width: 30%;">All</td> </tr> </table> <p>Specifies the rounding mode used by the dispatched thread.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 40%;">Description</th> <th style="width: 30%;">Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>RTNE</td> <td>Round to Nearest Even</td> <td>All</td> </tr> <tr> <td>1h</td> <td>RU</td> <td>Round toward +infinity</td> <td>All</td> </tr> <tr> <td>2h</td> <td>RD</td> <td>Round toward -infinity</td> <td>All</td> </tr> <tr> <td>3h</td> <td>RTZ</td> <td>Round toward zero</td> <td>All</td> </tr> </tbody> </table>			Project:	All	Value	Name	Description	Project	0h	RTNE	Round to Nearest Even	All	1h	RU	Round toward +infinity	All	2h	RD	Round toward -infinity	All	3h	RTZ	Round toward zero	All
Project:	All																									
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13	<b>Illegal Opcode Exception Enable</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Project:</td> <td style="width: 30%;">All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This bit gets loaded into EU CR0.1[12] (note the bit # difference). See Exceptions and ISA Execution Environment.</p>			Project:	All	Format:	Enable																		
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<b>3DSTATE_PS</b>				
	12	<b>Reserved</b>	Project: All	Format: MBZ
	11	<b>Mask Stack Exception Enable</b>	Project: All	Format: Enable
	This bit gets loaded into EU CR0.1[12] (note the bit # difference). See Exceptions and ISA Execution Environment.			
	10:8	<b>Reserved</b>	Project: All	Format: MBZ
	7	<b>Software Exception Enable</b>	Project: All	Format: Enable
This bit gets loaded into EU CR0.1[13] (note the bit # difference). See Exceptions and ISA Execution Environment.				
4..5	6:0	<b>Reserved</b>	Project: All	Format: MBZ
	63:10	<b>Scratch Space Base Pointer</b>	Project: All	Format: GeneralStateOffset[63:10]ScratchSpace
	Specifies the 1k-byte aligned address offset to scratch space for use by the kernel. This pointer is relative to the General State Base Address.			
	<b>Programming Notes</b>			
	Scratch Space per slice is computed based on 4 sub-slices. SW must allocate scratch space enough so that each slice has 4 slices allowed.			
	9:4	<b>Reserved</b>	Project: All	Format: MBZ
	3:0	<b>Per Thread Scratch Space</b>	Project: All	Format: U4
	Specifies the amount of scratch space allowed to be used by each thread. The driver must allocate enough contiguous scratch space, pointed to by the Scratch Space Pointer, to ensure that the Maximum Number of Threads each get Per Thread Scratch Space size without exceeding the driver-allocated scratch space.			

		<b>3DSTATE_PS</b>	
		Value	Name
		[0,11]	indicating [1k bytes, 2M bytes] in powers of two
6	31:23	<b>Maximum Number of Threads Per PSD</b>	
		Project:	CHV, BSW
		Format:	U8-2 Representing Thread Count
		<b>Description</b>	
		Range = [0, 62] --> [2, 64] threads. Specifies the maximum number of simultaneous threads allowed to be active per PSD. Depending on the GT mode register, Number of PSDs in the system determine maximum number PS threads per configuration.	
		Has 2 PSDs therefore actual range for max PS threads is [4,128].	
		<b>Programming Notes</b>	
		If this field is changed between 3DPRIMITIVE commands, a PIPE_CONTROL command with <b>Stall at Pixel Scoreboard</b> set is required to be issued.	
		<b>Reserved</b>	
		22:12	
		Format:	MBZ
11	<b>Push Constant Enable</b>		
	Project:	All	
	Format:	Enable	
This field must be enabled if the sum of the <b>PS Constant Buffer [3:0] Read Length</b> fields in 3DSTATE_CONSTANT_PS is nonzero, and must be disabled if the sum is zero.			
10	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
9	<b>Reserved</b>		
	Project:	CHV, BSW	
	Format:	MBZ	
8	<b>Render Target Fast Clear Enable</b>		
	Project:	All	
	Format:	Enable	
This field is set to enable fast clear of the bound render targets. See "Render Target Fast Clear" for restrictions on enabling this field.			
7	<b>Reserved</b>		
	Project:	CHV, BSW	
	Format:	MBZ	

<b>3DSTATE_PS</b>																				
6	<p><b>Render Target Resolve Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field is set to enable clear value resolve on non-multisampled render targets. See "Render Target Resolve" for restrictions on enabling this field.</p>	Project:	CHV, BSW	Format:	Enable															
	Project:	CHV, BSW																		
Format:	Enable																			
5	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td></td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:		Format:	MBZ															
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4:3	<p><b>Position XY Offset Select</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U2 Enumerated Type</td> </tr> </table> <p>This field specifies if/what Position XY Offset values are passed in the PS payload. Note that these are per-slot (pixel/sample) offsets, and therefore separate from the subspan XY coordinates passed in R1.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #e1eef6;"> <th style="width: 15%;">Value</th> <th style="width: 30%;">Name</th> <th style="width: 55%;">Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>POSOFFSET_NONE</td> <td>No Position XY Offsets are included in the PS payload.</td> </tr> <tr> <td>1h</td> <td>Reserved</td> <td></td> </tr> <tr> <td>2h</td> <td>POSOFFSET_CENTROID</td> <td>Position XY Offsets will be passed in the PS payload, and these will reflect the Centroid position(s).</td> </tr> <tr> <td>3h</td> <td>POSOFFSET_SAMPLE</td> <td>Position XY Offsets will be passed in the PS payload, and these will reflect the multisample position(s).</td> </tr> </tbody> </table> <div style="border: 1px solid black; padding: 5px; margin-top: 10px;"> <p style="text-align: center; color: #0070c0; margin: 0;"><b>Programming Notes</b></p> <p>SW Recommendation: If the PS kernel needs the Position Offsets to compute a Position XY value, this field should match Position ZW Interpolation Mode to ensure a consistent position.xyzw computation</p> <p>If the PS kernel does not need the Position XY Offsets to compute a Position Value, then this field should be programmed to POSOFFSET_NONE, as the PS kernel should be using the various barycentric inputs to evaluate other-than-position attributes. However, this field can be used to pass Centroid or Sample offsets in the payload for special test modes (e.g., where barycentric coordinates are computed in the PS vs. being HW-generated and passed in the payload).</p> <p>MSDISPMODE_PERSAMPLE is required in order to select POSOFFSET_SAMPLE.</p> </div>	Project:	All	Format:	U2 Enumerated Type	Value	Name	Description	0h	POSOFFSET_NONE	No Position XY Offsets are included in the PS payload.	1h	Reserved		2h	POSOFFSET_CENTROID	Position XY Offsets will be passed in the PS payload, and these will reflect the Centroid position(s).	3h	POSOFFSET_SAMPLE	Position XY Offsets will be passed in the PS payload, and these will reflect the multisample position(s).
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2	<p><b>32 Pixel Dispatch Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>Enables the Windower to dispatch 8 subspans in one payload. Variable Pixel Dispatch in Section: Pixel Grouping (Dispatch size) control for valid pixel dispatch combinations.</p>	Project:	All	Format:	Enable															
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Format:	Enable																			

<b>3DSTATE_PS</b>									
1	<p><b>16 Pixel Dispatch Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>Enables the Windower to dispatch 4 subspans in one payload. Variable Pixel Dispatch in Section: Pixel Grouping (Dispatch size) control for valid pixel dispatch combinations.</p>	Project:	All	Format:	Enable				
	Project:	All							
Format:	Enable								
0	<p><b>8 Pixel Dispatch Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>Enables the Windower to dispatch 2 subspans from 1 object (polygon) in one payload. Variable Pixel Dispatch in Section: Pixel Grouping (Dispatch size) control for valid pixel dispatch combinations.</p> <table border="1" style="width: 100%; margin-top: 10px;"> <thead> <tr> <th style="text-align: center;">Programming Notes</th> <th style="text-align: center;">Project</th> </tr> </thead> <tbody> <tr> <td>When Render Target Fast Clear Enable is ENABLED or Render Target Resolve Type = RESOLVE_PARTIAL or RESOLVE_FULL, this bit must be DISABLED.</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Project:	All	Format:	Enable	Programming Notes	Project	When Render Target Fast Clear Enable is ENABLED or Render Target Resolve Type = RESOLVE_PARTIAL or RESOLVE_FULL, this bit must be DISABLED.	CHV, BSW
	Project:	All							
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Programming Notes	Project								
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	Format:	MBZ							
	<p>22:16 <b>Dispatch GRF Start Register For Constant/Setup Data 0</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>U7</td> </tr> </table> <p>Specifies the starting GRF register number for the Constant/Setup portion of the thread payload for kernel[0].</p> <table border="1" style="width: 100%; margin-top: 10px;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>[0,127]</td> <td></td> </tr> </tbody> </table>	Format:	U7	Value	Name	[0,127]			
	Format:	U7							
Value	Name								
[0,127]									
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Format:	MBZ								
<p>14:8 <b>Dispatch GRF Start Register For Constant/Setup Data 1</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U7</td> </tr> </table> <p>Specifies the starting GRF register number for the Constant/Setup portion of the thread payload for kernel[1].</p> <table border="1" style="width: 100%; margin-top: 10px;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>[0,127]</td> <td></td> </tr> </tbody> </table>	Project:	All	Format:	U7	Value	Name	[0,127]		
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Format:	U7								
Value	Name								
[0,127]									
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Format:	MBZ								



<b>3DSTATE_PS</b>						
	6:0	<b>Dispatch GRF Start Register For Constant/Setup Data 2</b>				
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U7</td> </tr> </table>	Project:	All	Format:	U7
	Project:	All				
	Format:	U7				
	Specifies the starting GRF register number for the Constant/Setup portion of the thread payload for kernel[2].					
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>[0,127]</td> <td></td> </tr> </tbody> </table>	Value	Name	[0,127]		
Value	Name					
[0,127]						
8..9	63:6	<b>Kernel Start Pointer 1</b>				
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>InstructionBaseOffset[63:6]Kernel</td> </tr> </table>	Project:	All	Format:	InstructionBaseOffset[63:6]Kernel
	Project:	All				
	Format:	InstructionBaseOffset[63:6]Kernel				
	Specifies the 64-byte aligned address offset of the first instruction in kernel[1]. This pointer is relative to the Instruction Base Address.					
5:0	<b>Reserved</b>					
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ
Project:	All					
Format:	MBZ					
10..11	63:6	<b>Kernel Start Pointer 2</b>				
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>InstructionBaseOffset[63:6]Kernel</td> </tr> </table>	Project:	All	Format:	InstructionBaseOffset[63:6]Kernel
	Project:	All				
	Format:	InstructionBaseOffset[63:6]Kernel				
	Specifies the 64-byte aligned address offset of the first instruction in kernel[2]. This pointer is relative to the <b>Instruction Base Address</b> .					
5:0	<b>Reserved</b>					
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ
Project:	All					
Format:	MBZ					

## 3DSTATE\_PS\_EXTRA

3DSTATE_PS_EXTRA			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		4fh 3DSTATE_PS_EXTRA	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	0h Excludes DWord (0,1)	
	Project:	All	
	Format:	=n	
	Total Length - 2		
1	31	<b>Pixel Shader Valid</b>	
		Project:	All
		Format:	Enable
	When set indicates a valid pixel shaderWhen this bit clear the rest of this command should also be clear.		
	30	<b>Pixel Shader Does not write to RT</b>	
Project:		All	
Format:		Enable	
When set indicates the pixel shader does not write to render target.			

### 3DSTATE\_PS\_EXTRA

29	<b>oMask Present to Render Target</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This bit is inserted in the PS payload header and made available to the DataPort (either via the message header or via header bypass) to indicate that oMask data from the shader (one or two phases) is included in Render Target Write messages. If present, the oMask data is used to mask off samples.</p>	Project:	All	Format:	Enable																
Project:	All																					
Format:	Enable																					
28	<b>Pixel Shader Kills Pixel</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This bit, if ENABLED, indicates that the PS kernel has the ability to kill (discard) pixels or samples, other than due to depth or stencil testing. This bit is required to be ENABLED in the following situations:</p> <ul style="list-style-type: none"> <li>The API pixel shader program contains "killpix" or "discard" instructions, or other code in the pixel shader kernel that can cause the final pixel mask to differ from the pixel mask received on dispatch.</li> </ul>	Project:	All	Format:	Enable																
Project:	All																					
Format:	Enable																					
27:26	<b>Pixel Shader Computed Depth Mode</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 40%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U2 Enumerated Type</td> </tr> </table> <p>This field specifies the computed depth mode for the pixel shader.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #e6f2ff;"> <th style="width: 15%;">Value</th> <th style="width: 20%;">Name</th> <th style="width: 65%;">Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>PSCDEPTH_OFF</td> <td>Pixel shader does not compute depth</td> </tr> <tr> <td>1h</td> <td>PSCDEPTH_ON</td> <td>Pixel shader computes depth with no guarantee as to its value</td> </tr> <tr> <td>2h</td> <td>PSCDEPTH_ON_GE</td> <td>Pixel shader computes depth and guarantees that oDepth &gt; = SourceDepth</td> </tr> <tr> <td>3h</td> <td>PSCDEPTH_ON_LE</td> <td>Pixel shader computes depth and guarantees that oDepth &lt; = SourceDepth</td> </tr> </tbody> </table> <div style="border: 1px solid black; padding: 5px; margin-top: 10px;"> <p style="text-align: center; color: #0070c0; margin: 0;"><b>Programming Notes</b></p> <p>If this field is set to any value other than PSCDEPTH_OFF, a multi-phase shader (i.e. dispatch RATE_COARSE or RATE_PIXEL with pixel/sample loops or sample loop respectively) must output depth and render targets only at the last phase.</p> </div>	Project:	All	Format:	U2 Enumerated Type	Value	Name	Description	0h	PSCDEPTH_OFF	Pixel shader does not compute depth	1h	PSCDEPTH_ON	Pixel shader computes depth with no guarantee as to its value	2h	PSCDEPTH_ON_GE	Pixel shader computes depth and guarantees that oDepth > = SourceDepth	3h	PSCDEPTH_ON_LE	Pixel shader computes depth and guarantees that oDepth < = SourceDepth	
Project:	All																					
Format:	U2 Enumerated Type																					
Value	Name	Description																				
0h	PSCDEPTH_OFF	Pixel shader does not compute depth																				
1h	PSCDEPTH_ON	Pixel shader computes depth with no guarantee as to its value																				
2h	PSCDEPTH_ON_GE	Pixel shader computes depth and guarantees that oDepth > = SourceDepth																				
3h	PSCDEPTH_ON_LE	Pixel shader computes depth and guarantees that oDepth < = SourceDepth																				
25	<b>Reserved</b>																					
24	<b>Pixel Shader Uses Source Depth</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This bit, if ENABLED, indicates that the PS kernel requires the source depth value (vPos.z) to be passed in the payload. The source depth value is interpolated according to the Position ZW Interpolation Mode state.</p>	Project:	All	Format:	Enable																
Project:	All																					
Format:	Enable																					

### 3DSTATE\_PS\_EXTRA

23	<p><b>Pixel Shader Uses Source W</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This bit, if ENABLED, indicates that the PS kernel requires the interpolated source W value (vPos.w) to be passed in the payload. The W value is interpolated according to the Position ZW Interpolation Mode state.</p>	Project:	All	Format:	Enable		
Project:	All						
Format:	Enable						
22	<p><b>Reserved</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ		
Project:	CHV, BSW						
Format:	MBZ						
21:18	<p><b>Reserved</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ		
Project:	CHV, BSW						
Format:	MBZ						
17	<p><b>Removed</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ		
Project:	CHV, BSW						
Format:	MBZ						
16:11	<p><b>Reserved</b></p>						
10	<p><b>Reserved</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ		
Project:	CHV, BSW						
Format:	MBZ						
9	<p><b>Reserved</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Project:</td> <td>CHV, BSW</td> </tr> </table>	Project:	CHV, BSW				
Project:	CHV, BSW						
8	<p><b>Attribute Enable</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field must be enabled if the Number of SF Output Attributes field in 3DSTATE_SBE is nonzero, and must be disabled if that field is zero.</p>	Format:	Enable				
Format:	Enable						
7	<p><b>Pixel Shader Disables Alpha To Coverage</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>When set indicates the pixel shader AlphaToCoverage should be disabled due to oMask output. The setting of this bit is API dependent.</p>	Project:	All	Format:	Enable		
Project:	All						
Format:	Enable						
6	<p><b>Pixel Shader Is Per Sample</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This bit, when ENABLED, indicates that the pixel shader is dispatched at the per sample shading rate. If the bit is DISABLED, the pixel shader is dispatched at the per pixel rate.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="text-align: center; background-color: #e6f2ff;"><b>Programming Notes</b></td> </tr> <tr> <td>This bit must NOT be set when PS is used to do clear MSRTs with Fast Clear Optimization</td> </tr> </table>	Project:	CHV, BSW	Format:	Enable	<b>Programming Notes</b>	This bit must NOT be set when PS is used to do clear MSRTs with Fast Clear Optimization
Project:	CHV, BSW						
Format:	Enable						
<b>Programming Notes</b>							
This bit must NOT be set when PS is used to do clear MSRTs with Fast Clear Optimization							

<b>3DSTATE_PS_EXTRA</b>		
		Enabled.
5	<b>Reserved</b>	
	Project:	CHV, BSW
	Format:	MBZ
4	<b>Reserved</b>	
	Project:	CHV, BSW
	Format:	MBZ
3	<b>Reserved</b>	
	Project:	CHV, BSW
	Format:	MBZ
2	<b>Pixel Shader Has UAV</b>	
	Project:	All
	Format:	Enable
	Format:	U1 Enumerated Type
	This field when set indicates that the pixel shader has a UAV attached to it.	
1	<b>Pixel Shader Uses Input Coverage Mask</b>	
	Project:	CHV, BSW
	Format:	Enable
	This bit, if ENABLED, indicates that the PS kernel requires the input coverage mask to be passed in the payload.	
0	<b>Reserved</b>	
	Project:	CHV, BSW
	Format:	MBZ

## 3DSTATE\_PUSH\_CONSTANT\_ALLOC\_DS

3DSTATE_PUSH_CONSTANT_ALLOC_DS		
Project:	CHV, BSW	
Source:	RenderCS	
Length Bias:	2	
This command sets up the URB configuration for DS Push Constant Buffer.		
Programming Notes		
Programming Restriction: <ul style="list-style-type: none"> <li>The sum of the Constant Buffer Offset and the Constant Buffer Size may not exceed the maximum value of the Constant Buffer Size.</li> <li>The sum of the constant length programmed in 3DSTATE_CONSTANT_DS must be equal or smaller then the size of the allocated space in the URB including the buffering for half cachelines. See <b>Push Constant URB Allocation section for more details</b>.</li> <li>The 3DSTATE_CONSTANT_DS must be reprogrammed prior to the next 3DPRIMITIVE command after programming the 3DSTATE_PUSH_CONSTANT_ALLOC_DS.</li> </ul>		
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 3h GFXPIPE
	Format: OpCode	
	28:27	<b>Command SubType</b>
		Default Value: 3h GFXPIPE_3D
	Format: OpCode	
	26:24	<b>3D Command Opcode</b>
		Default Value: 1h 3DSTATE_NONPIPELINED
	Format: OpCode	
	23:16	<b>3D Command Sub Opcode</b>
		Default Value: 14h 3DSTATE_PUSH_CONSTANT_ALLOC_DS
	Format: OpCode	
15:8	<b>Reserved</b>	
	Project: All	
Format: MBZ		
7:0	<b>DWord Length</b>	
	Default Value: 0h Excludes DWord (0,1)	
	Project: All	
Format: =n Total Length - 2		
<b>Programming Notes:</b> Workaround: This command must be followed by a PIPE_CONTROL with CS Stall bit set.		

<b>3DSTATE_PUSH_CONSTANT_ALLOC_DS</b>			
1	31:21	<b>Reserved</b>	
		Project: CHV, BSW	
		Format: MBZ	
	20:16	<b>Constant Buffer Offset</b>	
		Project: CHV, BSW	
		Format: U5	
		Specifies the offset of the DS constant buffer into the URB.	
		<b>Value</b>	<b>Name</b>
		[0,31] (0KB - 31KB) Increments of 2KB	
	15:6	<b>Reserved</b>	
		Project: CHV, BSW	
		Format: MBZ	
5:0	<b>Constant Buffer Size</b>		
	Project: CHV, BSW		
	Format: U6		
	Specifies the size of the DS constant buffer. This value will determine the amount of data the command stream can pre-fetch before the buffer is full. Value of zero is only valid when constants are not enabled for DS.		
	<b>Value</b>	<b>Name</b>	
	[0,32] (0KB - 32KB) Increments of 2KB		

## 3DSTATE\_PUSH\_CONSTANT\_ALLOC\_GS

3DSTATE_PUSH_CONSTANT_ALLOC_GS						
Project:	CHV, BSW					
Source:	RenderCS					
Length Bias:	2					
This command sets up the URB configuration for GS Push Constant Buffer.						
Programming Notes						
<ul style="list-style-type: none"> <li>The sum of the Constant Buffer Offset and the Constant Buffer Size may not exceed the maximum value of the Constant Buffer Size.</li> <li>The sum of the constant length programmed in 3DSTATE_CONSTANT_GS must be equal or smaller then the size of the allocated space in the URB including the buffering for half cachelines.</li> <li>The 3DSTATE_CONSTANT_GS must be reprogrammed prior to the next 3DPRIMITIVE command after programming the 3DSTATE_PUSH_CONSTANT_ALLOC_GS.</li> </ul>						
See Push Constant URB Allocation section for more details.						
DWord	Bit	Description				
0	31:29	<b>Command Type</b>				
		Default Value: 3h GFXPIPE Format: OpCode				
	28:27	<b>Command SubType</b>				
		Default Value: 3h GFXPIPE_3D Format: OpCode				
	26:24	<b>3D Command Opcode</b>				
		Default Value: 1h 3DSTATE_NONPIPELINED Format: OpCode				
	23:16	<b>3D Command Sub Opcode</b>				
		Default Value: 15h 3DSTATE_PUSH_CONSTANT_ALLOC_GS Format: OpCode				
	15:8	<b>Reserved</b>				
		Project: All Format: MBZ				
	7:0	<b>DWord Length</b>				
		Format: =n				
Total Length - 2						
<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>3DSTATE_PUSH_CONSTANT_ALLOC_GS <b>[Default]</b></td> <td>Excludes DWord (0,1)</td> </tr> </tbody> </table>		Value	Name	Description	0h	3DSTATE_PUSH_CONSTANT_ALLOC_GS <b>[Default]</b>
Value	Name	Description				
0h	3DSTATE_PUSH_CONSTANT_ALLOC_GS <b>[Default]</b>	Excludes DWord (0,1)				



<b>3DSTATE_PUSH_CONSTANT_ALLOC_GS</b>									
1	31:21	<b>Reserved</b>							
		<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ			
	Project:	CHV, BSW							
	Format:	MBZ							
	20:16	<b>Constant Buffer Offset</b>							
		Project:	CHV, BSW						
		Format:	U5						
		Specifies the offset of the GS constant buffer into the URB.							
			<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 20%;">Value</th> <th style="width: 60%;">Name</th> <th style="width: 20%;">Project</th> </tr> </thead> <tbody> <tr> <td>[0,31]</td> <td>(0KB - 31KB) Increments of 2KB</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Value	Name	Project	[0,31]	(0KB - 31KB) Increments of 2KB	CHV, BSW
	Value	Name	Project						
	[0,31]	(0KB - 31KB) Increments of 2KB	CHV, BSW						
	15:6	<b>Reserved</b>							
<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>		Project:	CHV, BSW	Format:	MBZ				
Project:	CHV, BSW								
Format:	MBZ								
5:0	<b>Constant Buffer Size</b>								
	Project:	CHV, BSW							
	Format:	U6							
	Specifies the size of the GS constant buffer. This value will determine the amount of data the command stream can pre-fetch before the buffer is full. Value of zero is only valid when constants are not enabled for GS.								
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 20%;">Value</th> <th style="width: 60%;">Name</th> <th style="width: 20%;">Project</th> </tr> </thead> <tbody> <tr> <td>[0,32]</td> <td>(0KB - 32KB) Increments of 2KB</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Value	Name	Project	[0,32]	(0KB - 32KB) Increments of 2KB	CHV, BSW	
Value	Name	Project							
[0,32]	(0KB - 32KB) Increments of 2KB	CHV, BSW							

## 3DSTATE\_PUSH\_CONSTANT\_ALLOC\_HS

DWord		Bit	Description
<b>3DSTATE_PUSH_CONSTANT_ALLOC_HS</b>			
Project:		CHV, BSW	
Source:		RenderCS	
Length Bias:		2	
This command sets up the URB configuration for HS Push Constant Buffer.			
<b>Programming Notes</b>			
Programming Restriction:			
<ul style="list-style-type: none"> <li>The sum of the Constant Buffer Offset and the Constant Buffer Size may not exceed the maximum value of the Constant Buffer Size.</li> <li>The sum of the constant length programmed in 3DSTATE_CONSTANT_HS must be equal or smaller than the size of the allocated space in the URB including the buffering for half cachelines. See <b>Push Constant URB Allocation</b> section for more details.</li> <li>The 3DSTATE_CONSTANT_HS must be reprogrammed prior to the next 3DPRIMITIVE command after programming the 3DSTATE_PUSH_CONSTANT_ALLOC_HS.</li> </ul>			
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	1h 3DSTATE_NONPIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
		Default Value:	13h 3DSTATE_PUSH_CONSTANT_ALLOC_HS
		Format:	OpCode
	15:8	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
7:0	<b>DWord Length</b>		
	Default Value:	0h Excludes DWord (0,1)	
	Project:	All	
	Format:	=n Total Length - 2	

<b>3DSTATE_PUSH_CONSTANT_ALLOC_HS</b>			
1	31:21	<b>Reserved</b>	
		Project: CHV, BSW	
		Format: MBZ	
	20:16	<b>Constant Buffer Offset</b>	
		Project: CHV, BSW	
		Format: U5	
		Specifies the offset of the HS constant buffer into the URB.	
		<b>Value</b>	<b>Name</b>
	[0,31]	(0KB - 31KB) Increments of 2KB	CHV, BSW
	15:6	<b>Reserved</b>	
		Project: CHV, BSW	
		Format: MBZ	
5:0	<b>Constant Buffer Size</b>		
	Project: CHV, BSW		
	Format: U6		
	Specifies the size of the HS constant buffer. This value will determine the amount of data the command stream can pre-fetch before the buffer is full. Value of zero is only valid when constants are not enabled for HS.		
	<b>Value</b>	<b>Name</b>	<b>Project</b>
[0,32]	(0KB - 32KB) Increments of 2KB	CHV, BSW	

## 3DSTATE\_PUSH\_CONSTANT\_ALLOC\_PS

DWord		Bit	Description
<b>3DSTATE_PUSH_CONSTANT_ALLOC_PS</b>			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
This command sets up the URB configuration for PS Push Constant Buffer.			
<b>Programming Notes</b>			
Restriction:			
<ul style="list-style-type: none"> <li>The sum of the Constant Buffer Offset and the Constant Buffer Size may not exceed the maximum value of the Constant Buffer Size.</li> <li>The sum of the constant length programmed in 3DSTATE_CONSTANT_PS must be equal or smaller than the size of the allocated space in the URB including the buffering for half cachelines. See <b>Push Constant URB Allocation</b> section for more details.</li> <li>The 3DSTATE_CONSTANT_PS must be reprogrammed prior to the next 3DPRIMITIVE command after programming the 3DSTATE_PUSH_CONSTANT_ALLOC_PS.</li> </ul>			
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	1h 3DSTATE_NONPIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
		Default Value:	16h 3DSTATE_PUSH_CONSTANT_ALLOC_PS
		Format:	OpCode
	15:8	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	7:0	<b>Dword Length</b>	
		Default Value:	0h Excludes Dword (0,1)
		Project:	All
		Format:	=n Total Length - 2

<b>3DSTATE_PUSH_CONSTANT_ALLOC_PS</b>			
1	31:21	<b>Reserved</b>	
		Project: CHV, BSW	
		Format: MBZ	
	20:16	<b>Constant Buffer Offset</b>	
		Project: CHV, BSW	
		Format: U5	
		Specifies the offset of the PS constant buffer into the URB.	
		<b>Value</b>	<b>Name</b>
	[0,31]	(0KB - 31KB) Increments of 2KB	CHV, BSW
	15:6	<b>Reserved</b>	
		Project: CHV, BSW	
		Format: MBZ	
5:0	<b>Constant Buffer Size</b>		
	Project: CHV, BSW		
	Format: U6		
	Specifies the size of the PS constant buffer. This value will determine the amount of data the command stream can pre-fetch before the buffer is full. Value of zero is only valid when constants are not enabled for PS.		
	<b>Value</b>	<b>Name</b>	<b>Project</b>
[0,32]	(0KB - 32KB) Increments of 2KB	CHV, BSW	

## 3DSTATE\_PUSH\_CONSTANT\_ALLOC\_VS

DWord		Bit	Description
<b>3DSTATE_PUSH_CONSTANT_ALLOC_VS</b>			
Project:		CHV, BSW	
Source:		RenderCS	
Length Bias:		2	
This command sets up the URB configuration for VS Push Constant Buffer.			
<b>Programming Notes</b>			
Programming Restriction:			
<ul style="list-style-type: none"> <li>The sum of the Constant Buffer Offset and the Constant Buffer Size may not exceed the maximum value of the Constant Buffer Size.</li> <li>The sum of the constant length programmed in 3DSTATE_CONSTANT_VS must be equal or smaller than the size of the allocated space in the URB including the buffering for half cachelines. See <b>Push Constant URB Allocation</b> section for more details.</li> <li>The 3DSTATE_CONSTANT_VS must be reprogrammed prior to the next 3DPRIMITIVE command after programming the 3DSTATE_PUSH_CONSTANT_ALLOC_VS.</li> </ul>			
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	1h 3DSTATE_NONPIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
		Default Value:	12h 3DSTATE_PUSH_CONSTANT_ALLOC_VS
		Format:	OpCode
	15:8	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
7:0	<b>DWord Length</b>		
	Default Value:	0h Excludes DWord (0,1)	
	Project:	All	
	Format:	=n Total Length - 2	

<b>3DSTATE_PUSH_CONSTANT_ALLOC_VS</b>			
1	31:21	<b>Reserved</b>	
		Project: CHV, BSW	
		Format: MBZ	
	20:16	<b>Constant Buffer Offset</b>	
		Project: CHV, BSW	
		Format: U5	
		Specifies the offset of the VS constant buffer into the URB.	
		<b>Value</b>	<b>Name</b>
	[0,31]	(0KB - 31KB) Increments of 2KB	CHV, BSW
	15:6	<b>Reserved</b>	
		Project: CHV, BSW	
		Format: MBZ	
5:0	<b>Constant Buffer Size</b>		
	Project: CHV, BSW		
	Format: U6		
	Specifies the size of the VS constant buffer. This value will determine the amount of data the command stream can pre-fetch before the buffer is full. Value of zero is only valid when constants are not enabled for VS.		
	<b>Value</b>	<b>Name</b>	<b>Project</b>
[0,32]	(0KB - 32KB) Increments of 2KB	CHV, BSW	

## 3DSTATE\_RASTER

3DSTATE_RASTER			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		50h 3DSTATE_RASTER	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	03h Excludes DWord (0,1)	
	Project:	All	
	Format:	=n	
	Total Length - 2		
1	31:28	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	27	<b>Reserved</b>	
		Project:	CHV, BSW
		Format:	MBZ
	26:24	<b>Reserved</b>	
		Project:	CHV, BSW
		Format:	MBZ



## 3DSTATE\_RASTER

23:22	<b>API Mode</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Project:</td> <td colspan="3">All</td> </tr> </table> <p>Software sets this field according to the API's version. These bits are set for DX9 or OGL/DX10.0/DX10.1+/DX11.1 per the following values.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 20%;">Value</th> <th style="width: 40%;">Name</th> <th style="width: 20%;">Project</th> <th style="width: 20%;"></th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>DX9/OGL</td> <td>All</td> <td></td> </tr> <tr> <td>1h</td> <td>DX10.0</td> <td>All</td> <td></td> </tr> <tr> <td>2h</td> <td>DX10.1+</td> <td>All</td> <td></td> </tr> <tr> <td>3h</td> <td>Reserved</td> <td>All</td> <td></td> </tr> </tbody> </table>			Project:	All			Value	Name	Project		0h	DX9/OGL	All		1h	DX10.0	All		2h	DX10.1+	All		3h	Reserved	All																	
Project:	All																																											
Value	Name	Project																																										
0h	DX9/OGL	All																																										
1h	DX10.0	All																																										
2h	DX10.1+	All																																										
3h	Reserved	All																																										
21	<b>Front Winding</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Project:</td> <td colspan="3">All</td> </tr> </table> <p>Determines whether a triangle object is considered "front facing" if the screen space vertex positions, when traversed in the order, result in a clockwise (CW) or counter-clockwise (CCW) winding order. Does not apply to points or lines.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 40%;">Name</th> <th style="width: 20%;">Description</th> <th style="width: 30%;">Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Clockwise</td> <td>FRONTWINDING_CW</td> <td>All</td> </tr> <tr> <td>1h</td> <td>Counter Clockwise <b>[Default]</b></td> <td>FRONTWINDING_CCW</td> <td>All</td> </tr> </tbody> </table>			Project:	All			Value	Name	Description	Project	0h	Clockwise	FRONTWINDING_CW	All	1h	Counter Clockwise <b>[Default]</b>	FRONTWINDING_CCW	All																								
Project:	All																																											
Value	Name	Description	Project																																									
0h	Clockwise	FRONTWINDING_CW	All																																									
1h	Counter Clockwise <b>[Default]</b>	FRONTWINDING_CCW	All																																									
20:18	<b>Forced Sample Count</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 40%;">Project:</td> <td colspan="3">All</td> </tr> <tr> <td>Format:</td> <td colspan="3">U3 Enumerated Type</td> </tr> </table> <p>This field specifies how many samples/pixel exist for RT Independent Rasterization</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 30%;">Name</th> <th style="width: 40%;">Description</th> <th style="width: 20%;">Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>NUMRASTSAMPLES_0</td> <td>No RT Independent Rasterization</td> <td>All</td> </tr> <tr> <td>1h</td> <td>NUMRASTSAMPLES_1</td> <td>1 rast-sample/pixel</td> <td>All</td> </tr> <tr> <td>2h</td> <td>NUMRASTSAMPLES_2</td> <td>2 rast-samples/pixel</td> <td>All</td> </tr> <tr> <td>3h</td> <td>NUMRASTSAMPLES_4</td> <td>4 rast-samples/pixel</td> <td>All</td> </tr> <tr> <td>4h</td> <td>NUMRASTSAMPLES_8</td> <td>8 rast-samples/pixel</td> <td>All</td> </tr> <tr> <td>5h</td> <td>NUMRASTSAMPLES_16</td> <td>16 rast-samples/pixel</td> <td>All</td> </tr> <tr> <td>6h-7h</td> <td>Reserved</td> <td></td> <td>All</td> </tr> </tbody> </table> <div style="border: 1px solid black; padding: 5px; margin-top: 10px;"> <p style="text-align: center; color: blue; font-weight: bold;">Programming Notes</p> <p>When 3DSTATE_MULTISAMPLE::Number of Multisamples != NUMSAMPLES_1, this field must be either NUMRASTSAMPLES_0 or NUMRASTSAMPLES_1.                  When 3DSTATE_MULTISAMPLE::Number of Multisamples == NUMSAMPLES_1, this field must not be NUMRASTSAMPLES_1.</p> </div>			Project:	All			Format:	U3 Enumerated Type			Value	Name	Description	Project	0h	NUMRASTSAMPLES_0	No RT Independent Rasterization	All	1h	NUMRASTSAMPLES_1	1 rast-sample/pixel	All	2h	NUMRASTSAMPLES_2	2 rast-samples/pixel	All	3h	NUMRASTSAMPLES_4	4 rast-samples/pixel	All	4h	NUMRASTSAMPLES_8	8 rast-samples/pixel	All	5h	NUMRASTSAMPLES_16	16 rast-samples/pixel	All	6h-7h	Reserved		All
Project:	All																																											
Format:	U3 Enumerated Type																																											
Value	Name	Description	Project																																									
0h	NUMRASTSAMPLES_0	No RT Independent Rasterization	All																																									
1h	NUMRASTSAMPLES_1	1 rast-sample/pixel	All																																									
2h	NUMRASTSAMPLES_2	2 rast-samples/pixel	All																																									
3h	NUMRASTSAMPLES_4	4 rast-samples/pixel	All																																									
4h	NUMRASTSAMPLES_8	8 rast-samples/pixel	All																																									
5h	NUMRASTSAMPLES_16	16 rast-samples/pixel	All																																									
6h-7h	Reserved		All																																									
17:16	<b>Cull Mode</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 40%;">Project:</td> <td colspan="3">All</td> </tr> <tr> <td>Format:</td> <td colspan="3">3D_CullMode</td> </tr> </table>			Project:	All			Format:	3D_CullMode																																		
Project:	All																																											
Format:	3D_CullMode																																											

<b>3DSTATE_RASTER</b>																							
	<p>Controls removal (culling) of triangle objects based on orientation. The cull mode only applies to triangle objects and does not apply to lines, points or rectangles.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>CULLMODE_BOTH</td> <td>All triangles are discarded (i.e., no triangle objects are drawn)</td> <td>All</td> </tr> <tr> <td>1h</td> <td>CULLMODE_NONE <b>[Default]</b></td> <td>No triangles are discarded due to orientation</td> <td>All</td> </tr> <tr> <td>2h</td> <td>CULLMODE_FRONT</td> <td>Triangles with a front-facing orientation are discarded</td> <td>All</td> </tr> <tr> <td>3h</td> <td>CULLMODE_BACK</td> <td>Triangles with a back-facing orientation are discarded</td> <td>All</td> </tr> </tbody> </table>			Value	Name	Description	Project	0h	CULLMODE_BOTH	All triangles are discarded (i.e., no triangle objects are drawn)	All	1h	CULLMODE_NONE <b>[Default]</b>	No triangles are discarded due to orientation	All	2h	CULLMODE_FRONT	Triangles with a front-facing orientation are discarded	All	3h	CULLMODE_BACK	Triangles with a back-facing orientation are discarded	All
Value	Name	Description	Project																				
0h	CULLMODE_BOTH	All triangles are discarded (i.e., no triangle objects are drawn)	All																				
1h	CULLMODE_NONE <b>[Default]</b>	No triangles are discarded due to orientation	All																				
2h	CULLMODE_FRONT	Triangles with a front-facing orientation are discarded	All																				
3h	CULLMODE_BACK	Triangles with a back-facing orientation are discarded	All																				
	<b>Programming Notes</b>																						
	Orientation determination is based on the setting of the Front Winding state.																						
15	<b>Reserved</b>																						
	Project:	All																					
	Format:	MBZ																					
14	<b>Force Multisampling</b>																						
	Project:	All																					
	This field provides a work around override for the computation of SF_INT::Multisample Rasterization Mode and WM_INT::Multisample Rasterization Mode.																						
	<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>																			
	0h	Normal	Multisampling mode is computed by HW according to formula for signal SF_INT::Multisample Rasterization Mode and WM_INT::Multisample Rasterization Mode in vol2a.11 3D Pipeline Windower [CHV, BSW] > Windower Pipelined State > 3DSTATE_WM > 3DSTATE_WM [CHV, BSW].	All																			
	1h	Force	Forces the DX Multisampling mode to be used directly	All																			
13	<b>Smooth Point Enable</b>																						
	Project:	CHV, BSW																					
	Format:	Enable																					
	Software sets this according to API. When OGL and smooth point rasterization is required, this bit must be set. HW ignores this bit for primitives other than points.																						
12	<b>DX Multisample Rasterization Enable</b>																						
	Project:	All																					
	Format:	Enable																					
	Software sets this according to the API's multisample enable																						
	<b>Programming Notes</b>																						

### 3DSTATE\_RASTER

	<p>This state only effects how the SF_INT/WM_INT::Multisample Rasterization Mode are set depending on some other states. This state mainly modifies the how the line rendering is done by setting SF_INT/WM_INT::Multisample Rasterization Mode to either OFF* or ON* . Please refer to table under SF_INT::Multisample Rasterization Mode.</p>																				
11:10	<p><b>DX Multisample Rasterization Mode</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U2 enumerated type</td> </tr> </table> <p>This field determines whether multisample rasterization is turned on/off, and how the pixel sample point(s) are defined. Software sets this according to the API's multisample state setting (if any)</p> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr style="background-color: #e1eef6;"> <th style="width: 15%;">Value</th> <th style="width: 60%;">Name</th> <th style="width: 25%;">Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>MSRASTMODE_OFF_PIXEL</td> <td>All</td> </tr> <tr> <td>1h</td> <td>MSRASTMODE_OFF_PATTERN</td> <td>All</td> </tr> <tr> <td>2h</td> <td>MSRASTMODE_ON_PIXEL</td> <td>All</td> </tr> <tr> <td>3h</td> <td>MSRASTMODE_ON_PATTERN</td> <td>All</td> </tr> </tbody> </table> <div style="background-color: #e1eef6; text-align: center; padding: 5px; margin-top: 10px;"><b>Programming Notes</b></div> <p>This field is used to directly set the SF_INT/WM_INT::Multisample Rasterization Mode when DX Multisample Rasterization Enable is set. Please refer to equation of SF_INT::Multisample Rasterization Mode.</p>		Project:	All	Format:	U2 enumerated type	Value	Name	Project	0h	MSRASTMODE_OFF_PIXEL	All	1h	MSRASTMODE_OFF_PATTERN	All	2h	MSRASTMODE_ON_PIXEL	All	3h	MSRASTMODE_ON_PATTERN	All
Project:	All																				
Format:	U2 enumerated type																				
Value	Name	Project																			
0h	MSRASTMODE_OFF_PIXEL	All																			
1h	MSRASTMODE_OFF_PATTERN	All																			
2h	MSRASTMODE_ON_PIXEL	All																			
3h	MSRASTMODE_ON_PATTERN	All																			
9	<p><b>Global Depth Offset Enable Solid</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>Enables computation and application of Global Depth Offset for SOLID objects.</p>		Project:	All	Format:	Enable															
Project:	All																				
Format:	Enable																				
8	<p><b>Global Depth Offset Enable Wireframe</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>Enables computation and application of Global Depth Offset when triangles are rendered in WIREFRAME mode.</p>		Project:	All	Format:	Enable															
Project:	All																				
Format:	Enable																				
7	<p><b>Global Depth Offset Enable Point</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>Enables computation and application of Global Depth Offset when triangles are rendered in POINT mode.</p>		Project:	All	Format:	Enable															
Project:	All																				
Format:	Enable																				
6:5	<p><b>Front Face Fill Mode</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> </table>		Project:	All																	
Project:	All																				

<b>3DSTATE_RASTER</b>			
	Format:	U2 enumerated type	
	This state controls how front-facing triangle and rectangle objects are rendered.		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0h	SOLID	Any triangle or rectangle object found to be front-facing is rendered as a solid object. This setting is required when rendering rectangle (RECTLIST) objects.
	1h	WIREFRAME	Any triangle object found to be front-facing is rendered as a series of lines along the triangle boundaries (as determined by the topology type and controlled by the vertex EdgeFlags).
	2h	POINT	Any triangle object found to be front-facing is rendered as a set of point primitives at the triangle vertices (as determined by the topology type and controlled by the vertex EdgeFlags).
	3h	Reserved	All
4:3	<b>Back Face Fill Mode</b>		
	Project:	All	
	Format:	U2 enumerated type	
	This state controls how back-facing triangle and rectangle objects are rendered.		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0h	SOLID	Any triangle or rectangle object found to be back-facing is rendered as a solid object. This setting is required when rendering rectangle (RECTLIST) objects.
	1h	WIREFRAME	Any triangle object found to be back-facing is rendered as a series of lines along the triangle boundaries (as determined by the topology type and controlled by the vertex EdgeFlags).
	2h	POINT	Any triangle object found to be back-facing is rendered as a set of point primitives at the triangle vertices (as determined by the topology type and controlled by the vertex EdgeFlags).
	3h	Reserved	All
2	<b>Antialiasing Enable</b>		
	Project:	All	
	Format:	Enable	
	This field enables "alpha-based" line antialiasing.		
	<b>Programming Notes</b>		
	This field must be disabled if any of the render targets have integer (UINT or SINT) surface format.		
1	<b>Scissor Rectangle Enable</b>		
	Project:	All	
	Format:	Enable	
	Enables operation of Scissor Rectangle.		

<b>3DSTATE_RASTER</b>						
0		<p><b>Viewport Z Clip Test Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field is used to control whether the Viewport Z extents (near, far) are considered in VertexClipTest.</p>	Project:	CHV, BSW	Format:	Enable
Project:	CHV, BSW					
Format:	Enable					
2	31:0	<p><b>Global Depth Offset Constant</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>IEEE_Float</td> </tr> </table> <p>Specifies the constant term in the Global Depth Offset function.</p>	Format:	IEEE_Float		
Format:	IEEE_Float					
3	31:0	<p><b>Global Depth Offset Scale</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>IEEE_Float</td> </tr> </table> <p>Specifies the scale term used in the Global Depth Offset function.</p>	Format:	IEEE_Float		
Format:	IEEE_Float					
4	31:0	<p><b>Global Depth Offset Clamp</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>IEEE_Float</td> </tr> </table> <p>Specifies the clamp term used in the Global Depth Offset function.</p>	Format:	IEEE_Float		
Format:	IEEE_Float					

## 3DSTATE\_SAMPLE\_MASK

<b>3DSTATE_SAMPLE_MASK</b>		
Project:	CHV, BSW	
Source:	RenderCS	
Length Bias:	2	
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 3h GFXPIPE
		Format: OpCode
	28:27	<b>Command SubType</b>
		Default Value: 3h GFXPIPE_3D
		Format: OpCode
	26:24	<b>3D Command Opcode</b>
Default Value: 0h 3DSTATE_PIPELINED		
Format: OpCode		
23:16	<b>3D Command Sub Opcode</b>	
	Default Value: 18h 3DSTATE_DX9_LOCAL_VALID_PS	
	Format: OpCode	
15:8	<b>Reserved</b>	
	Format: MBZ	
7:0	<b>Dword Length</b>	
	Default Value: 0h Excludes Dword (0,1)	
	Format: =n Total Length - 2	
1	31:16	<b>Reserved</b>
		Project: CHV, BSW
		Format: MBZ
	15:0	<b>Sample Mask</b>
Project:	CHV, BSW	
Format:	16 bit mask Right-justified bitmask (Bit 0 = Sample0). Number of bits that are used is determined by Num Multisamples (3DSTATE_MULTISAMPLE)	
<p>A per-multisample-position mask state variable that is immediately and unconditionally ANDed with the sample coverage mask as part of the rasterization process. This mask is applied prior to centroid selection. This mask must be ignored for centroid selection when RTIR is enabled i.e. Forced_Sample_Count &gt; 0.</p>		

## 3DSTATE\_SAMPLE\_MASK

### Programming Notes

- If **Number of Multisamples** is NUMSAMPLES\_1, bits 15:1 of this field will be zeroed by HW.
- If **NNumber of Multisamples** is NUMSAMPLES\_2, bits 15:2 of this field will be zeroed by HW.
- If **Number of Multisamples** is NUMSAMPLES\_4, bits 15:4 of this field will be zeroed by HW.
- If **Number of Multisamples** is NUMSAMPLES\_8, bits 15:8 of this field will be zeroed by HW.

## 3DSTATE\_SAMPLE\_PATTERN

3DSTATE_SAMPLE_PATTERN			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
<p>The 3DSTATE_SAMPLE_PATTERN command is used to specify the sample offsets for all multisample sample modes. The set of offset used will be selected based on the multisample mode. This is non-pipelined state.</p>			
Programming Notes			
<p>When programming the sample offsets (for NUMSAMPLES_4 or _8 and MSRASTMODE_xxx_PATTERN), the order of the samples 0 to 3 (or 7 for 8X, or 15 for 16X) must have monotonically increasing distance from the pixel center. This is required to get the correct centroid computation in the device.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	1h 3DSTATE_NONPIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		1Ch 3DSTATE_SAMPLE_PATTERN	
Format:		OpCode	
7:0	15:8	<b>Reserved</b>	
	7:0	<b>Dword Length</b>	
		Default Value:	7
		Format:	=n Total Length - 2
		Excludes Dword (0,1)	
1..4	31:0	<b>Reserved</b>	
5	31:28	<b>8x Sample7 X Offset</b>	
		Project:	All
		Format:	U0.4
		Subpixel X offset of Sample 7 relative to the UL pixel origin for 8x mode.	
		Range: [0,0.9375]	



<b>3DSTATE_SAMPLE_PATTERN</b>					
	27:24	<b>8x Sample7 Y Offset</b>	Project: All	Format: U0.4	Subpixel Y offset of Sample 7 relative to the UL pixel origin for 8x mode. Range: [0,0.9375]
	23:20	<b>8x Sample6 X Offset</b>	Project: All	Format: U0.4	Subpixel X offset of Sample 6 relative to the UL pixel origin for 8x mode. Range: [0,0.9375]
	19:16	<b>8x Sample6 Y Offset</b>	Project: All	Format: U0.4	Subpixel Y offset of Sample 6 relative to the UL pixel origin for 8x mode. Range: [0,0.9375]
	15:12	<b>8x Sample5 X Offset</b>	Project: All	Format: U0.4	Subpixel X offset of Sample 5 relative to the UL pixel origin for 8x mode. Range: [0,0.9375]
	11:8	<b>8x Sample5 Y Offset</b>	Project: All	Format: U0.4	Subpixel Y offset of Sample 5 relative to the UL pixel origin for 8x mode. Range: [0,0.9375]
	7:4	<b>8x Sample4 X Offset</b>	Project: All	Format: U0.4	Subpixel X offset of Sample 4 relative to the UL pixel origin for 8x mode. Range: [0,0.9375]

<b>3DSTATE_SAMPLE_PATTERN</b>						
6	3:0	<b>8x Sample4 Y Offset</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.4</td> </tr> </table> Subpixel Y offset of Sample 4 relative to the UL pixel origin for 8x mode. Range: [0,0.9375]	Project:	All	Format:	U0.4
	Project:	All				
	Format:	U0.4				
	31:28	<b>8x Sample3 X Offset</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.4</td> </tr> </table> Subpixel X offset of Sample 3 relative to the UL pixel origin for 8x mode. Range: [0,0.9375]	Project:	All	Format:	U0.4
	Project:	All				
Format:	U0.4					
27:24	<b>8x Sample3 Y Offset</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.4</td> </tr> </table> Subpixel Y offset of Sample 3 relative to the UL pixel origin for 8x mode. Range: [0,0.9375]	Project:	All	Format:	U0.4	
Project:	All					
Format:	U0.4					
23:20	<b>8x Sample2 X Offset</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.4</td> </tr> </table> Subpixel X offset of Sample 2 relative to the UL pixel origin for 8x mode. Range: [0,0.9375]	Project:	All	Format:	U0.4	
Project:	All					
Format:	U0.4					
19:16	<b>8x Sample2 Y Offset</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.4</td> </tr> </table> Subpixel Y offset of Sample 2 relative to the UL pixel origin for 8x mode. Range: [0,0.9375]	Project:	All	Format:	U0.4	
Project:	All					
Format:	U0.4					
15:12	<b>8x Sample1 X Offset</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.4</td> </tr> </table> Subpixel X offset of Sample 1 relative to the UL pixel origin for 8x mode. Range: [0,0.9375]	Project:	All	Format:	U0.4	
Project:	All					
Format:	U0.4					

<b>3DSTATE_SAMPLE_PATTERN</b>		
	11:8	<b>8x Sample1 Y Offset</b>
		Project: All
		Format: U0.4
		Subpixel Y offset of Sample 1 relative to the UL pixel origin for 8x mode. Range: [0,0.9375]
	7:4	<b>8x Sample0 X Offset</b>
		Project: All
		Format: U0.4
		Subpixel X offset of Sample 0 relative to the UL pixel origin for 8x mode. Range: [0,0.9375]
	3:0	<b>8x Sample0 Y Offset</b>
Project: All		
Format: U0.4		
Subpixel Y offset of Sample 0 relative to the UL pixel origin for 8x mode. Range: [0,0.9375]		
7	31:28	<b>4x Sample3 X Offset</b>
		Project: All
		Format: U0.4
		Subpixel X offset of Sample 3 relative to the UL pixel origin for 4x mode. Range: [0,0.9375]
	27:24	<b>4x Sample3 Y Offset</b>
		Project: All
		Format: U0.4
		Subpixel Y offset of Sample 3 relative to the UL pixel origin for 4x mode. Range: [0,0.9375]
	23:20	<b>4x Sample2 X Offset</b>
		Project: All
		Format: U0.4
		Subpixel X offset of Sample 2 relative to the UL pixel origin for 4x mode. Range: [0,0.9375]

<b>3DSTATE_SAMPLE_PATTERN</b>					
	19:16	<b>4x Sample2 Y Offset</b>	Project: All	Format: U0.4	Subpixel Y offset of Sample 2 relative to the UL pixel origin for 4x mode. Range: [0,0.9375]
	15:12	<b>4x Sample1 X Offset</b>	Project: All	Format: U0.4	Subpixel X offset of Sample 1 relative to the UL pixel origin for 4x mode. Range: [0,0.9375]
	11:8	<b>4x Sample1 Y Offset</b>	Project: All	Format: U0.4	Subpixel Y offset of Sample 1 relative to the UL pixel origin for 4x mode. Range: [0,0.9375]
	7:4	<b>4x Sample0 X Offset</b>	Project: All	Format: U0.4	Subpixel X offset of Sample 0 relative to the UL pixel origin for 4x mode. Range: [0,0.9375]
	3:0	<b>4x Sample0 Y Offset</b>	Project: All	Format: U0.4	Subpixel Y offset of Sample 0 relative to the UL pixel origin for 4x mode. Range: [0,0.9375]
8	31:24	<b>Reserved</b>			
	23:20	<b>1x Sample0 X Offset</b>	Project: All	Format: U0.4	Subpixel X offset of Sample 0 relative to the UL pixel origin for 1x mode. Range: [0,0.9375]

<b>3DSTATE_SAMPLE_PATTERN</b>						
	19:16	<b>1x Sample0 Y Offset</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.4</td> </tr> </table> Subpixel Y offset of Sample 0 relative to the UL pixel origin for 1x mode. Range: [0,0.9375]	Project:	All	Format:	U0.4
	Project:	All				
	Format:	U0.4				
	15:12	<b>2x Sample1 X Offset</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.4</td> </tr> </table> Subpixel X offset of Sample 1 relative to the UL pixel origin for 2x mode. Range: [0,0.9375]	Project:	All	Format:	U0.4
	Project:	All				
	Format:	U0.4				
	11:8	<b>2x Sample1 Y Offset</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.4</td> </tr> </table> Subpixel Y offset of Sample 1 relative to the UL pixel origin for 2x mode. Range: [0,0.9375]	Project:	All	Format:	U0.4
	Project:	All				
	Format:	U0.4				
	7:4	<b>2x Sample0 X Offset</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.4</td> </tr> </table> Subpixel X offset of Sample 0 relative to the UL pixel origin for 2x mode. Range: [0,0.9375]	Project:	All	Format:	U0.4
	Project:	All				
	Format:	U0.4				
	3:0	<b>2x Sample0 Y Offset</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.4</td> </tr> </table> Subpixel Y offset of Sample 0 relative to the UL pixel origin for 2x mode. Range: [0,0.9375]	Project:	All	Format:	U0.4
	Project:	All				
	Format:	U0.4				

## 3DSTATE\_SAMPLE\_PATTERN

3DSTATE_SAMPLE_PATTERN			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
<p>The 3DSTATE_SAMPLE_PATTERN command is used to specify the sample offsets for all multisample sample modes. The set of offset used will be selected based on the multisample mode. This is non-pipelined state.</p>			
Programming Notes			
<p>When programming the sample offsets (for NUMSAMPLES_4 or _8 and MSRASTMODE_xxx_PATTERN), the order of the samples 0 to 3 (or 7 for 8X) must have monotonically increasing distance from the pixel center. This is required to get the correct centroid computation in the device.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	1h 3DSTATE_NONPIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		1Ch 3DSTATE_SAMPLE_PATTERN	
Format:		OpCode	
15:8	<b>Reserved</b>		
	7:0	<b>Dword Length</b>	
		Default Value:	3
		Project:	All
		Format:	=n Total Length - 2
		Excludes Dword (0,1)	
1	31:28	<b>8x Sample7 X Offset</b>	
		Project:	All
		Format:	U0.4
		Subpixel X offset of Sample 7 relative to the UL pixel origin for 8x mode.	
		Range: [0,0.9375]	

<b>3DSTATE_SAMPLE_PATTERN</b>						
	27:24	<b>8x Sample7 Y Offset</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.4</td> </tr> </table> Subpixel Y offset of Sample 7 relative to the UL pixel origin for 8x mode. Range: [0,0.9375]	Project:	All	Format:	U0.4
	Project:	All				
	Format:	U0.4				
	23:20	<b>8x Sample6 X Offset</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.4</td> </tr> </table> Subpixel X offset of Sample 6 relative to the UL pixel origin for 8x mode. Range: [0,0.9375]	Project:	All	Format:	U0.4
	Project:	All				
	Format:	U0.4				
19:16	<b>8x Sample6 Y Offset</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.4</td> </tr> </table> Subpixel Y offset of Sample 6 relative to the UL pixel origin for 8x mode. Range: [0,0.9375]	Project:	All	Format:	U0.4	
Project:	All					
Format:	U0.4					
15:12	<b>8x Sample5 X Offset</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.4</td> </tr> </table> Subpixel X offset of Sample 5 relative to the UL pixel origin for 8x mode. Range: [0,0.9375]	Project:	All	Format:	U0.4	
Project:	All					
Format:	U0.4					
11:8	<b>8x Sample5 Y Offset</b> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>U0.4</td> </tr> </table> Subpixel Y offset of Sample 5 relative to the UL pixel origin for 8x mode. Range: [0,0.9375]	Format:	U0.4			
Format:	U0.4					
7:4	<b>8x Sample4 X Offset</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.4</td> </tr> </table> Subpixel X offset of Sample 4 relative to the UL pixel origin for 8x mode. Range: [0,0.9375]	Project:	All	Format:	U0.4	
Project:	All					
Format:	U0.4					
3:0	<b>8x Sample4 Y Offset</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.4</td> </tr> </table>	Project:	All	Format:	U0.4	
Project:	All					
Format:	U0.4					

<b>3DSTATE_SAMPLE_PATTERN</b>												
		<table border="1"> <tr> <td colspan="2">Subpixel Y offset of Sample 4 relative to the UL pixel origin for 8x mode.</td> </tr> <tr> <td colspan="2">Range: [0,0.9375]</td> </tr> </table>	Subpixel Y offset of Sample 4 relative to the UL pixel origin for 8x mode.		Range: [0,0.9375]							
Subpixel Y offset of Sample 4 relative to the UL pixel origin for 8x mode.												
Range: [0,0.9375]												
2	31:28	<table border="1"> <tr> <td colspan="2"><b>8x Sample3 X Offset</b></td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.4</td> </tr> <tr> <td colspan="2">Subpixel X offset of Sample 3 relative to the UL pixel origin for 8x mode.</td> </tr> <tr> <td colspan="2">Range: [0,0.9375]</td> </tr> </table>	<b>8x Sample3 X Offset</b>		Project:	All	Format:	U0.4	Subpixel X offset of Sample 3 relative to the UL pixel origin for 8x mode.		Range: [0,0.9375]	
		<b>8x Sample3 X Offset</b>										
		Project:	All									
		Format:	U0.4									
		Subpixel X offset of Sample 3 relative to the UL pixel origin for 8x mode.										
Range: [0,0.9375]												
27:24	<table border="1"> <tr> <td colspan="2"><b>8x Sample3 Y Offset</b></td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.4</td> </tr> <tr> <td colspan="2">Subpixel Y offset of Sample 3 relative to the UL pixel origin for 8x mode.</td> </tr> <tr> <td colspan="2">Range: [0,0.9375]</td> </tr> </table>	<b>8x Sample3 Y Offset</b>		Project:	All	Format:	U0.4	Subpixel Y offset of Sample 3 relative to the UL pixel origin for 8x mode.		Range: [0,0.9375]		
	<b>8x Sample3 Y Offset</b>											
	Project:	All										
	Format:	U0.4										
	Subpixel Y offset of Sample 3 relative to the UL pixel origin for 8x mode.											
Range: [0,0.9375]												
23:20	<table border="1"> <tr> <td colspan="2"><b>8x Sample2 X Offset</b></td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.4</td> </tr> <tr> <td colspan="2">Subpixel X offset of Sample 2 relative to the UL pixel origin for 8x mode.</td> </tr> <tr> <td colspan="2">Range: [0,0.9375]</td> </tr> </table>	<b>8x Sample2 X Offset</b>		Project:	All	Format:	U0.4	Subpixel X offset of Sample 2 relative to the UL pixel origin for 8x mode.		Range: [0,0.9375]		
	<b>8x Sample2 X Offset</b>											
	Project:	All										
	Format:	U0.4										
	Subpixel X offset of Sample 2 relative to the UL pixel origin for 8x mode.											
Range: [0,0.9375]												
19:16	<table border="1"> <tr> <td colspan="2"><b>8x Sample2 Y Offset</b></td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.4</td> </tr> <tr> <td colspan="2">Subpixel Y offset of Sample 2 relative to the UL pixel origin for 8x mode.</td> </tr> <tr> <td colspan="2">Range: [0,0.9375]</td> </tr> </table>	<b>8x Sample2 Y Offset</b>		Project:	All	Format:	U0.4	Subpixel Y offset of Sample 2 relative to the UL pixel origin for 8x mode.		Range: [0,0.9375]		
	<b>8x Sample2 Y Offset</b>											
	Project:	All										
	Format:	U0.4										
	Subpixel Y offset of Sample 2 relative to the UL pixel origin for 8x mode.											
Range: [0,0.9375]												
15:12	<table border="1"> <tr> <td colspan="2"><b>8x Sample1 X Offset</b></td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.4</td> </tr> <tr> <td colspan="2">Subpixel X offset of Sample 1 relative to the UL pixel origin for 8x mode.</td> </tr> <tr> <td colspan="2">Range: [0,0.9375]</td> </tr> </table>	<b>8x Sample1 X Offset</b>		Project:	All	Format:	U0.4	Subpixel X offset of Sample 1 relative to the UL pixel origin for 8x mode.		Range: [0,0.9375]		
	<b>8x Sample1 X Offset</b>											
	Project:	All										
	Format:	U0.4										
	Subpixel X offset of Sample 1 relative to the UL pixel origin for 8x mode.											
Range: [0,0.9375]												
11:8	<table border="1"> <tr> <td colspan="2"><b>8x Sample1 Y Offset</b></td> </tr> <tr> <td>Format:</td> <td>U0.4</td> </tr> <tr> <td colspan="2">Subpixel Y offset of Sample 1 relative to the UL pixel origin for 8x mode.</td> </tr> <tr> <td colspan="2">Range: [0,0.9375]</td> </tr> </table>	<b>8x Sample1 Y Offset</b>		Format:	U0.4	Subpixel Y offset of Sample 1 relative to the UL pixel origin for 8x mode.		Range: [0,0.9375]				
	<b>8x Sample1 Y Offset</b>											
	Format:	U0.4										
	Subpixel Y offset of Sample 1 relative to the UL pixel origin for 8x mode.											
	Range: [0,0.9375]											



<b>3DSTATE_SAMPLE_PATTERN</b>						
	7:4	<b>8x Sample0 X Offset</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.4</td> </tr> </table> Subpixel X offset of Sample 0 relative to the UL pixel origin for 8x mode. Range: [0,0.9375]	Project:	All	Format:	U0.4
	Project:	All				
Format:	U0.4					
3:0	<b>8x Sample0 Y Offset</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.4</td> </tr> </table> Subpixel Y offset of Sample 0 relative to the UL pixel origin for 8x mode. Range: [0,0.9375]	Project:	All	Format:	U0.4	
Project:	All					
Format:	U0.4					
3	31:28	<b>4x Sample3 X Offset</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.4</td> </tr> </table> Subpixel X offset of Sample 3 relative to the UL pixel origin for 4x mode. Range: [0,0.9375]	Project:	All	Format:	U0.4
	Project:	All				
	Format:	U0.4				
	27:24	<b>4x Sample3 Y Offset</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.4</td> </tr> </table> Subpixel Y offset of Sample 3 relative to the UL pixel origin for 4x mode. Range: [0,0.9375]	Project:	All	Format:	U0.4
Project:	All					
Format:	U0.4					
23:20	<b>4x Sample2 X Offset</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.4</td> </tr> </table> Subpixel X offset of Sample 2 relative to the UL pixel origin for 4x mode. Range: [0,0.9375]	Project:	All	Format:	U0.4	
Project:	All					
Format:	U0.4					
19:16	<b>4x Sample2 Y Offset</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U0.4</td> </tr> </table> Subpixel Y offset of Sample 2 relative to the UL pixel origin for 4x mode. Range: [0,0.9375]	Project:	All	Format:	U0.4	
Project:	All					
Format:	U0.4					

<b>3DSTATE_SAMPLE_PATTERN</b>						
	15:12	<b>4x Sample1 X Offset</b>	Project: All	Format: U0.4	Subpixel X offset of Sample 1 relative to the UL pixel origin for 4x mode. Range: [0,0.9375]	
	11:8	<b>4x Sample1 Y Offset</b>	Project: All	Format: U0.4	Subpixel Y offset of Sample 1 relative to the UL pixel origin for 4x mode. Range: [0,0.9375]	
	7:4	<b>4x Sample0 X Offset</b>	Project: All	Format: U0.4	Subpixel X offset of Sample 0 relative to the UL pixel origin for 4x mode. Range: [0,0.9375]	
	3:0	<b>4x Sample0 Y Offset</b>	Format: U0.4	Subpixel Y offset of Sample 0 relative to the UL pixel origin for 4x mode. Range: [0,0.9375]		
	4	31:24	<b>Reserved</b>	Project: All	Format: MBZ	
		23:20	<b>1x Sample0 X Offset</b>	Project: All	Format: U0.4	Subpixel X offset of Sample 0 relative to the UL pixel origin for 1x mode. Range: [0,0.9375]
		19:16	<b>1x Sample0 Y Offset</b>	Project: All	Format: U0.4	Subpixel Y offset of Sample 0 relative to the UL pixel origin for 1x mode. Range: [0,0.9375]

<b>3DSTATE_SAMPLE_PATTERN</b>			
	15:12	<b>2x Sample1 X Offset</b>	
		Project:	All
		Format:	U0.4
		Subpixel X offset of Sample 1 relative to the UL pixel origin for 2x mode.	
		Range: [0,0.9375]	
	11:8	<b>2x Sample1 Y Offset</b>	
		Project:	All
		Format:	U0.4
		Subpixel Y offset of Sample 1 relative to the UL pixel origin for 2x mode.	
		Range: [0,0.9375]	
	7:4	<b>2x Sample0 X Offset</b>	
		Project:	All
		Format:	U0.4
		Subpixel X offset of Sample 0 relative to the UL pixel origin for 2x mode.	
		Range: [0,0.9375]	
	3:0	<b>2x Sample0 Y Offset</b>	
Project:		All	
Format:		U0.4	
Subpixel Y offset of Sample 0 relative to the UL pixel origin for 2x mode.			
Range: [0,0.9375]			

## 3DSTATE\_SAMPLER\_PALETTE\_LOAD0

3DSTATE_SAMPLER_PALETTE_LOAD0			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
Description			
<p>The 3DSTATE_SAMPLER_PALETTE_LOAD0 instruction is used to load 32-bit values into the first texture palette. The texture palette is used whenever a texture with a paletted format (containing "Px [palette0]") is referenced by the sampler.</p> <p>This instruction is used to load all or a subset of the 256 entries of the first palette. Partial loads always start from the first (index 0) entry.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	Opcode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
	26:24	<b>3D Command Opcode</b>	
		Default Value:	1h 3DSTATE_NONPIPELINED
23:16	<b>3D Command Sub Opcode</b>		
	Default Value:	02h 3DSTATE_SAMPLER_PALETTE_LOAD0	
15:8	<b>Reserved</b>		
	Project:	All	
7:0	Format:	MBZ	
	<b>DWord Length</b>		
	Format:	=n	
	Total Length = 1 + entryCount - 2		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	[0,255]	Range	1-256 Entries
1..n	31:0	<b>Entry</b>	
	Format:	PALETTE_ENTRY	

## 3DSTATE\_SAMPLER\_PALETTE\_LOAD1

3DSTATE_SAMPLER_PALETTE_LOAD1			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
<p>The 3DSTATE_SAMPLER_PALETTE_LOAD1 instruction is used to load 32-bit values into the second texture palette. The second texture palette is used whenever a texture with a paletted format (containing "Px...[palette1]") is referenced by the sampler. This instruction is used to load all or a subset of the 256 entries of the second palette. Partial loads always start from the first (index 0) entry.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
Default Value:		1h 3DSTATE	
Format:		OpCode	
23:16	<b>3D Command Sub Opcode</b>		
	Default Value:	0Ch 3DSTATE_SAMPLER_PALETTE_LOAD1	
	Format:	OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	0h Excludes DWord (0,1)	
	Format:	=n Total Length - 2	
1..n	31:24	<b>Palette Alpha[0:N-1]</b>	
		Project:	All
	Format:	U8	
	Alpha channel loaded into the Nth entry of the texture color palette.		
23:16	<b>Palette Red[0:N-1]</b>		
	Project:	All	
	Format:	U8	
Alpha channel loaded into the Nth entry of the texture color palette.			

<b>3DSTATE_SAMPLER_PALETTE_LOAD1</b>						
	15:8	<b>Palette Green[0:N-1]</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>Alpha channel loaded into the Nth entry of the texture color palette.</p>	Project:	All	Format:	U8
	Project:	All				
Format:	U8					
	7:0	<b>Palette Blue[0:N-1]</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>Alpha channel loaded into the Nth entry of the texture color palette.</p>	Project:	All	Format:	U8
Project:	All					
Format:	U8					

## 3DSTATE\_SAMPLER\_STATE\_POINTERS\_DS

3DSTATE_SAMPLER_STATE_POINTERS_DS			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
The 3DSTATE_SAMPLER_STATE_POINTERS_DS command is used to define the location of DS SAMPLER_STATE table. Only some of the fixed functions utilize sampler state tables.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		2Dh 3DSTATE_SAMPLER_STATE_POINTERS_DS	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	0h DWORD_COUNT_n	
	Format:	=n	
1	31:5	<b>Pointer to DS Sampler State</b>	
		Project:	All
		Format:	DynamicStateOffset[31:5]SAMPLER_STATE*16
	Specifies the 32-byte aligned address offset of the DS function's SAMPLER_STATE table. This offset is relative to the Dynamic State Base Address.		
	4:0	<b>Reserved</b>	
Project:		All	
Format:		MBZ	

## 3DSTATE\_SAMPLER\_STATE\_POINTERS\_GS

3DSTATE_SAMPLER_STATE_POINTERS_GS			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
<p>The 3DSTATE_SAMPLER_STATE_POINTERS_GS command is used to define the location of GS SAMPLER_STATE table. Only some of the fixed functions utilize sampler state tables.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		2Eh 3DSTATE_SAMPLER_STATE_POINTERS_GS	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	0h DWORD_COUNT_n	
	Format:	=n	
1	31:5	<b>Pointer to GS Sampler State</b>	
		Project:	All
		Format:	DynamicStateOffset[31:5]SAMPLER_STATE*16
	<p>Specifies the 32-byte aligned address offset of the GS function's SAMPLER_STATE table. This offset is relative to the Dynamic State Base Address.</p>		
	4:0	<b>Reserved</b>	
Project:		All	
Format:		MBZ	



## 3DSTATE\_SAMPLER\_STATE\_POINTERS\_HS

3DSTATE_SAMPLER_STATE_POINTERS_HS			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
The 3DSTATE_SAMPLER_STATE_POINTERS_HS command is used to define the location of HS SAMPLER_STATE table. Only some of the fixed functions utilize sampler state tables.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		2Ch 3DSTATE_SAMPLER_STATE_POINTERS_HS	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	0h DWORD_COUNT_n	
	Format:	=n	
1	31:5	<b>Pointer to HS Sampler State</b>	
		Project:	All
		Format:	DynamicStateOffset[31:5]SAMPLER_STATE*16
	Specifies the 32-byte aligned address offset of the HS function's SAMPLER_STATE table. This offset is relative to the Dynamic State Base Address.		
	4:0	<b>Reserved</b>	
Project:		All	
Format:		MBZ	

## 3DSTATE\_SAMPLER\_STATE\_POINTERS\_PS

3DSTATE_SAMPLER_STATE_POINTERS_PS			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
The 3DSTATE_SAMPLER_STATE_POINTERS_PS command is used to define the location of PS SAMPLER_STATE table. Only some of the fixed functions utilize sampler state tables.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		2Fh 3DSTATE_SAMPLER_STATE_POINTERS_PS	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	0h DWORD_COUNT_n	
	Format:	=n	
1	31:5	<b>Pointer to PS Sampler State</b>	
		Project:	All
		Format:	DynamicStateOffset[31:5]SAMPLER_STATE*16
	Specifies the 32-byte aligned address offset of the PS function's SAMPLER_STATE table. This offset is relative to the Dynamic State Base Address.		
	4:0	<b>Reserved</b>	
Project:		All	
Format:		MBZ	

## 3DSTATE\_SAMPLER\_STATE\_POINTERS\_VS

3DSTATE_SAMPLER_STATE_POINTERS_VS			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
The 3DSTATE_SAMPLER_STATE_POINTERS_VS command is used to define the location of VS SAMPLER_STATE table. Only some of the fixed functions utilize sampler state tables.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		2Bh 3DSTATE_SAMPLER_STATE_POINTERS_VS	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	0h DWORD_COUNT_n	
	Format:	=n	
1	31:5	<b>Pointer to VS Sampler State</b>	
		Project:	All
		Format:	DynamicStateOffset[31:5]SAMPLER_STATE*16
	Specifies the 32-byte aligned address offset of the VS function's SAMPLER_STATE table. This offset is relative to the Dynamic State Base Address.		
	4:0	<b>Reserved</b>	
Project:		All	
Format:		MBZ	

## 3DSTATE\_SBE

3DSTATE_SBE			
Project:		CHV, BSW	
Source:		RenderCS	
Length Bias:		2	
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		1Fh 3DSTATE_SBE	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	02h Excludes DWord (0,1)	
	Project:	CHV, BSW	
	Format:	=n	
	Total Length - 2		
1	31:30	<b>Reserved</b>	
		Format:	MBZ
	29	<b>Force Vertex URB Entry Read Length</b>	
		Project:	CHV, BSW
Format:		Enable	
This field provides a work around override for the computation of SBE_INT::Vertex URB Entry Read Length. If asserted, 3DSTATE_SBE::Vertex URB Entry Read Length is be used directly. Otherwise, SBE_INT::Vertex URB Entry Read Length is computed normally.			
28	<b>Force Vertex URB Entry Read Offset</b>		
	Project:	CHV, BSW	

<b>3DSTATE_SBE</b>		
	Format:	Enable
	This field provides a work around override for the computation of SBE_INT::Vertex URB Entry Read Offset. If asserted, 3DSTATE_SBE::Vertex URB Entry Read Offset is be used directly. Otherwise, SBE_INT::Vertex URB Entry Read Offset is computed normally.	
27:22	<b>Number of SF Output Attributes</b>	
	Project:	CHV, BSW
	Format:	U6 count of attributes
	Specifies the number of vertex attributes passed from the SF stage to the WM stage (does not include Position).	
	<b>Value</b>	<b>Name</b>
	[0,32]	
21	<b>Attribute Swizzle Enable</b>	
	Format:	Enable
	Enables the SF to perform swizzling on (up to the first 16) vertex attributes. If DISABLED, all vertex attributes are passed through.	
20	<b>Point Sprite Texture Coordinate Origin</b>	
	This state controls how Point Sprite Texture Coordinates are generated (when enabled on a per-attribute basis by Point Sprite Texture Coordinate Enable).	
	<b>Value</b>	<b>Name</b> <b>Description</b>
	0h	UPPERLEFT      Top Left = (0,0,0,1)Bottom Left = (0,1,0,1)Bottom Right = (1,1,0,1)
	1h	LOWERLEFT      Top Left = (0,1,0,1)Bottom Left = (0,0,0,1)Bottom Right = (1,0,0,1)
19	<b>Primitive ID Override Component W</b>	
	Project:	CHV, BSW
	Format:	Enable
	If set, the W component of output attribute selected by Primitive ID Override Attribute Select is overridden with the Primitive ID.	
18	<b>Primitive ID Override Component Z</b>	
	Project:	CHV, BSW
	Format:	Enable
	If set, the Z component of output attribute selected by Primitive ID Override Attribute Select is overridden with the Primitive ID.	
17	<b>Primitive ID Override Component Y</b>	
	Project:	CHV, BSW
	Format:	Enable
	If set, the Y component of output attribute selected by Primitive ID Override Attribute Select is overridden with the Primitive ID.	

<b>3DSTATE_SBE</b>								
	16	<p><b>Primitive ID Override Component X</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>If set, the X component of output attribute selected by Primitive ID Override Attribute Select is overridden with the Primitive ID.</p>	Project:	CHV, BSW	Format:	Enable		
	Project:	CHV, BSW						
	Format:	Enable						
	15:11	<p><b>Vertex URB Entry Read Length</b></p> <table border="1"> <tr> <td>Format:</td> <td>U5</td> </tr> </table> <p>Specifies the amount of URB data read for each Vertex URB entry, in 256-bit register increments.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>[1,16]</td> <td></td> </tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>It is UNDEFINED to set this field to 0 indicating no Vertex URB data to be read. This field should be set to the minimum length required to read the maximum source attribute. The maximum source attribute is indicated by the maximum value of the enabled Attribute # Source Attribute if Attribute Swizzle Enable is set, Number of Output Attributes-1 if enable is not set.  <math>read\_length = \text{ceiling}((\text{max\_source\_attr} + 1) / 2)</math></p>	Format:	U5	Value	Name	[1,16]	
	Format:	U5						
Value	Name							
[1,16]								
10:5	<p><b>Vertex URB Entry Read Offset</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table> <p>Specifies the offset (in 256-bit units) at which Vertex URB data is to be read from the URB.</p>	Project:	CHV, BSW					
Project:	CHV, BSW							
4:0	<p><b>Primitive ID Override Attribute Select</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table> <p>Specifies which attribute is overridden w/ the Primitive ID</p> <p style="text-align: center;"><b>Programming Notes</b></p> <p>Set all Primitive ID Override Component Select X/Y/Z/W to 0 to indicate there is no Primitive ID override.</p>	Project:	CHV, BSW					
Project:	CHV, BSW							
2	<p>31:0 <b>Point Sprite Texture Coordinate Enable</b></p> <table border="1"> <tr> <td>Format:</td> <td>Enable[32]</td> </tr> </table> <p>When processing point primitives, the attributes from the incoming point vertex are typically copied to the point object corner vertices. However, if a bit is set in this field, the corresponding Attribute is selected as a Point Sprite Texture Coordinate, in which case each corner vertex is assigned a pre-defined texture coordinate as defined by the Point Sprite Texture Coordinate Origin state bit. Bit 0 corresponds to output Attribute 0.</p>	Format:	Enable[32]					
Format:	Enable[32]							
3	<p>31:0 <b>Constant Interpolation Enable</b></p> <table border="1"> <tr> <td>Format:</td> <td>Enable[32]</td> </tr> </table> <p>This field is a bitmask containing a Constant Interpolation Enable bit for each corresponding attribute. If a bit is set, that attribute will undergo constant interpolation, and the corresponding WrapShortest Enable bits (if defined) will be ignored. If a bit is clear, components which are not enabled for WrapShortest interpolation (if defined) will be linearly interpolated.</p>	Format:	Enable[32]					
Format:	Enable[32]							

## 3DSTATE\_SBE\_SWIZ

<b>3DSTATE_SBE_SWIZ</b>		
Project:	CHV, BSW	
Source:	RenderCS	
Length Bias:	2	
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 3h GFXPIPE
		Format: OpCode
	28:27	<b>Command SubType</b>
		Default Value: 3h GFXPIPE_3D
		Format: OpCode
	26:24	<b>3D Command Opcode</b>
		Default Value: 0h 3DSTATE_PIPELINED
		Format: OpCode
	23:16	<b>3D Command Sub Opcode</b>
Default Value: 51h 3DSTATE_SBE_SWIZ		
Format: OpCode		
15:8	<b>Reserved</b>	
	Format: MBZ	
7:0	7:0	<b>DWord Length</b>
		Default Value: 9h Excludes DWord (0,1)
		Format: =n
		Total Length - 2
1..8	15:0	<b>Attribute</b>
		Format: SF_OUTPUT_ATTRIBUTE_DETAIL
9..10	63:60	<b>Attribute 15 Wrap Shortest Enables</b>
		Format: WRAP_SHORTEST_ENABLE
	59:56	<b>Attribute 14 Wrap Shortest Enables</b>
		Format: WRAP_SHORTEST_ENABLE
	55:52	<b>Attribute 13 Wrap Shortest Enables</b>
Format: WRAP_SHORTEST_ENABLE		
51:48	<b>Attribute 12 Wrap Shortest Enables</b>	
	Format: WRAP_SHORTEST_ENABLE	
47:44	<b>Attribute 11 Wrap Shortest Enables</b>	
	Format: WRAP_SHORTEST_ENABLE	

<b>3DSTATE_SBE_SWIZ</b>		
	Format:	WRAP_SHORTEST_ENABLE
43:40	<b>Attribute 10 Wrap Shortest Enables</b>	
	Format:	WRAP_SHORTEST_ENABLE
39:36	<b>Attribute 09 Wrap Shortest Enables</b>	
	Format:	WRAP_SHORTEST_ENABLE
35:32	<b>Attribute 08 Wrap Shortest Enables</b>	
	Format:	WRAP_SHORTEST_ENABLE
31:28	<b>Attribute 07 Wrap Shortest Enables</b>	
	Format:	WRAP_SHORTEST_ENABLE
27:24	<b>Attribute 06 Wrap Shortest Enables</b>	
	Format:	WRAP_SHORTEST_ENABLE
23:20	<b>Attribute 05 Wrap Shortest Enables</b>	
	Format:	WRAP_SHORTEST_ENABLE
19:16	<b>Attribute 04 Wrap Shortest Enables</b>	
	Format:	WRAP_SHORTEST_ENABLE
15:12	<b>Attribute 03 Wrap Shortest Enables</b>	
	Format:	WRAP_SHORTEST_ENABLE
11:8	<b>Attribute 02 Wrap Shortest Enables</b>	
	Format:	WRAP_SHORTEST_ENABLE
7:4	<b>Attribute 01 Wrap Shortest Enables</b>	
	Format:	WRAP_SHORTEST_ENABLE
3:0	<b>Attribute 00 Wrap Shortest Enables</b>	
	Format:	WRAP_SHORTEST_ENABLE



## 3DSTATE\_SCISSOR\_STATE\_POINTERS

3DSTATE_SCISSOR_STATE_POINTERS			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
The 3DSTATE_SCISSOR_STATE_POINTERS command is used to define the location of the indirect SCISSOR_RECT state.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		0Fh 3DSTATE_SCISSOR_STATE_POINTERS	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	0h DWORD_COUNT_n	
	Format:	=n	
1	31:5	<b>Scissor Rect Pointer</b>	
		Project:	All
		Format:	DynamicStateOffset[31:5]SCISSOR_RECT*16
	Specifies the 32-byte aligned address offset of the SCISSOR_RECT state. This offset is relative to the <b>Dynamic State Base Address</b> .		
	4:0	<b>Reserved</b>	
Project:		All	
Format:		MBZ	

## 3DSTATE\_SF

<b>3DSTATE_SF</b>			
Project:		CHV, BSW	
Source:		RenderCS	
Length Bias:		2	
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		13h 3DSTATE_SF	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	2h Excludes DWord (0,1)	
	Format:	=n	
	Total Length - 2		
1	31:30	<b>Reserved</b>	
		Format:	MBZ
	29:12	<b>Line Width</b>	
Project:		CHV, BSW	
Format:		U11.7	
Range: [0.0, 2047.9921875]			
Controls width of line primitives. Setting a Line Width of 0.0 specifies the rasterization of the "thinnest" (one-pixel-wide), non-antialiased lines. Note that this effectively overrides the effect of AAEnable (though the AAEnable state variable is not modified).			

<b>3DSTATE_SF</b>											
	<table border="1" style="width: 100%;"> <tr> <th colspan="2" style="text-align: center;">Programming Notes</th> </tr> <tr> <td colspan="2">Software must not program a value of 0.0 when running in MSRASTMODE_ON_XXX modes - zero-width lines are not available when multisampling rasterization is enabled.</td> </tr> <tr> <th style="width: 80%;">Restriction</th> <th style="width: 20%;">Project</th> </tr> <tr> <td>Line widths higher than 40.0 will appear to be thinner than the programmed line width at certain angles. Software must expose the line widths higher than 40 to APIs only if the loss in quality is acceptable.</td> <td>CHV, BSW</td> </tr> <tr> <td>Software must set the "WM_CHIKEN1" register bits "1 and 3" when rendering the AA lines higher than Line width of "40.0".</td> <td>CHV, BSW</td> </tr> </table>	Programming Notes		Software must not program a value of 0.0 when running in MSRASTMODE_ON_XXX modes - zero-width lines are not available when multisampling rasterization is enabled.		Restriction	Project	Line widths higher than 40.0 will appear to be thinner than the programmed line width at certain angles. Software must expose the line widths higher than 40 to APIs only if the loss in quality is acceptable.	CHV, BSW	Software must set the "WM_CHIKEN1" register bits "1 and 3" when rendering the AA lines higher than Line width of "40.0".	CHV, BSW
Programming Notes											
Software must not program a value of 0.0 when running in MSRASTMODE_ON_XXX modes - zero-width lines are not available when multisampling rasterization is enabled.											
Restriction	Project										
Line widths higher than 40.0 will appear to be thinner than the programmed line width at certain angles. Software must expose the line widths higher than 40 to APIs only if the loss in quality is acceptable.	CHV, BSW										
Software must set the "WM_CHIKEN1" register bits "1 and 3" when rendering the AA lines higher than Line width of "40.0".	CHV, BSW										
11	<p><b>Legacy Global Depth Bias Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>Enables the SF to use the Global Depth Offset Constant state unmodified. If this bit is not set, the SF will scale the Global Depth Offset Constant as described in section Error! Reference source not found. of this document.</p> <table border="1" style="width: 100%;"> <tr> <th colspan="2" style="text-align: center;">Programming Notes</th> </tr> <tr> <td colspan="2">This bit should be set whenever non zero depth bias (Slope, Bias) values are used. Setting this bit may have some degradation of performance for some workloads.</td> </tr> </table>	Format:	Enable	Programming Notes		This bit should be set whenever non zero depth bias (Slope, Bias) values are used. Setting this bit may have some degradation of performance for some workloads.					
Format:	Enable										
Programming Notes											
This bit should be set whenever non zero depth bias (Slope, Bias) values are used. Setting this bit may have some degradation of performance for some workloads.											
10	<p><b>Statistics Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>If ENABLED, this FF unit will increment CL_PRIMITIVES_COUNT on behalf of the CLIP stage. If DISABLED, CL_PRIMITIVES_COUNT will be left unchanged.</p> <table border="1" style="width: 100%;"> <tr> <th colspan="2" style="text-align: center;">Programming Notes</th> </tr> <tr> <td colspan="2">This bit should be set whenever clipping is enabled and the Statistics Enable bit is set in CLIP_STATE. It should be cleared if clipping is disabled or Statistics Enable in CLIP_STATE is clear.</td> </tr> </table>	Project:	All	Format:	Enable	Programming Notes		This bit should be set whenever clipping is enabled and the Statistics Enable bit is set in CLIP_STATE. It should be cleared if clipping is disabled or Statistics Enable in CLIP_STATE is clear.			
Project:	All										
Format:	Enable										
Programming Notes											
This bit should be set whenever clipping is enabled and the Statistics Enable bit is set in CLIP_STATE. It should be cleared if clipping is disabled or Statistics Enable in CLIP_STATE is clear.											
9:2	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ								
Format:	MBZ										
1	<p><b>Viewport Transform Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This bit controls the Viewport Transform function.</p>	Format:	Enable								
Format:	Enable										
0	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ								
Format:	MBZ										
2	<p>31:29 <b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ								
	Format:	MBZ									
	28 <b>Reserved</b>										
27:18 <b>Reserved</b>											

<b>3DSTATE_SF</b>																	
	17:16	<b>Line End Cap Antialiasing Region Width</b>															
	Format: U2																
	This field specifies the distances over which the coverage of anti-aliased line end caps are computed.																
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>0.5 pixels</td> <td>0.5 pixels</td> </tr> <tr> <td>1h</td> <td>1.0 pixels</td> <td>1.0 pixels</td> </tr> <tr> <td>2h</td> <td>2.0 pixels</td> <td>2.0 pixels</td> </tr> <tr> <td>3h</td> <td>4.0 pixels</td> <td>4.0 pixels</td> </tr> </tbody> </table>		Value	Name	Description	0h	0.5 pixels	0.5 pixels	1h	1.0 pixels	1.0 pixels	2h	2.0 pixels	2.0 pixels	3h	4.0 pixels	4.0 pixels
	Value	Name	Description														
	0h	0.5 pixels	0.5 pixels														
	1h	1.0 pixels	1.0 pixels														
	2h	2.0 pixels	2.0 pixels														
	3h	4.0 pixels	4.0 pixels														
	15	<b>Reserved</b>															
Format: MBZ																	
14	<b>Reserved</b>																
Format: MBZ																	
13	<b>Reserved</b>																
12	<b>Reserved</b>																
11:0	<b>Reserved</b>																
Format: MBZ																	
3	31	<b>Last Pixel Enable</b>															
	Format: Enable																
	If ENABLED, the last pixel of a diamond line will be lit. This state will only affect the rasterization of Diamond lines (will not affect wide lines or anti-aliased lines).																
	<p style="text-align: center;"><b>Programming Notes</b></p> Last pixel is applied to all lines of a LINELIST, and only the last line of a LINESTRIP.																
	30:29	<b>Triangle Strip/List Provoking Vertex Select</b>															
	Format: 0-based vertex index																
	Selects which vertex of a triangle (in a triangle strip or list primitive) is considered the "provoking vertex". Used for flat shading of primitives. Does current implementation send provoking vertex first?																
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>0</td> </tr> <tr> <td>1h</td> <td>1</td> </tr> <tr> <td>2h</td> <td>2</td> </tr> <tr> <td>3h</td> <td>Reserved</td> </tr> </tbody> </table>		Value	Name	0h	0	1h	1	2h	2	3h	Reserved					
	Value	Name															
0h	0																
1h	1																
2h	2																
3h	Reserved																
28:27	<b>Line Strip/List Provoking Vertex Select</b>																
Project: All																	
Format: 0-based vertex index																	
Selects which vertex of a line (in a line strip or list primitive) is considered the "provoking vertex".																	

<b>3DSTATE_SF</b>			
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0h	0	Vertex 0
	1h	1	Vertex 1
	2h	Reserved	Reserved
	3h	Reserved	Reserved
26:25	<b>Triangle Fan Provoking Vertex Select</b>		
	Format:	0-based vertex index	
	Selects which vertex of a triangle (in a triangle fan primitive) is considered the "provoking vertex".		
	<b>Value</b>	<b>Name</b>	
	0h	0	
	1h	1	
	2h	2	
	3h	Reserved	
24:15	<b>Reserved</b>		
	Format:	MBZ	
14	<b>AA Line Distance Mode</b>		
	Format:	U1	
	This bit controls the distance computation for antialiased lines.		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	1h	AALINEDISTANCE_TRUE	True distance computation. This is the normal setting which should yield WHQL compliance.
13	<b>Smooth Point Enable</b>		
	Format:	Enable	
	Double Buffer Armed By:	Enables logic to draw smooth OGL Points	
	<b>Programming Notes</b>		
	If Enabled, SF will treat points in the same fashion that AA lines are processed		
12	<b>Vertex Sub Pixel Precision Select</b>		
	Format:	U1	
	Selects the number of fractional bits maintained in the vertex data		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0h	Disable	8 sub pixel precision bits maintained
	1h	Enable	4 sub pixel precision bits maintained

<b>3DSTATE_SF</b>											
11	<p><b>Point Width Source</b> Controls whether the point width passed on the vertex or from state is used for rendering point primitives.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0h</td> <td>Vertex</td> <td>Use Point Width on Vertex</td> </tr> <tr> <td style="text-align: center;">1h</td> <td>State <b>[Default]</b></td> <td>Use Point Width from State</td> </tr> </tbody> </table>		Value	Name	Description	0h	Vertex	Use Point Width on Vertex	1h	State <b>[Default]</b>	Use Point Width from State
Value	Name	Description									
0h	Vertex	Use Point Width on Vertex									
1h	State <b>[Default]</b>	Use Point Width from State									
10:0	<p><b>Point Width</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td>U8.3</td> </tr> <tr> <td colspan="2">Range: [0.125, 255.875] pixels</td> </tr> <tr> <td colspan="2">This field specifies the size (width) of point primitives in pixels. This field is overridden (though not overwritten) whenever point width information is passed in the FVF</td> </tr> </table>		Format:	U8.3	Range: [0.125, 255.875] pixels		This field specifies the size (width) of point primitives in pixels. This field is overridden (though not overwritten) whenever point width information is passed in the FVF				
Format:	U8.3										
Range: [0.125, 255.875] pixels											
This field specifies the size (width) of point primitives in pixels. This field is overridden (though not overwritten) whenever point width information is passed in the FVF											

## 3DSTATE\_SO\_BUFFER

3DSTATE_SO_BUFFER		
Project:	CHV, BSW	
Source:	RenderCS	
Length Bias:	2	
Programming Notes		Project
Foreach SO Buffer, the 3DSTATE_SO_BUFFER must only be sent once prior to each 3DPRIMITIVE command.		CHV, BSW
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 3h GFXPIPE Format: OpCode
	28:27	<b>Command SubType</b>
		Default Value: 3h GFXPIPE_3D Format: OpCode
	26:24	<b>3D Command Opcode</b>
		Default Value: 1h 3DSTATE_NONPIPELINED Format: OpCode
	23:16	<b>3D Command Sub Opcode</b>
Default Value: 18h 3DSTATE_SO_BUFFER Format: OpCode		
15:8	<b>Reserved</b>	
7:0	Format: MBZ	
	<b>DWord Length</b>	
1	31	<b>SO Buffer Enable</b>
		Format: Enable
If set, stream output to SO Buffer is enabled, , if 3DSTATE_STREAMOUT::SO Function ENABLE is also enabled..If clear, the SO Buffer is considered "not bound" and effectively treated as a zero-length buffer for the purposes of SO output and overflow detection. If an enabled stream's Stream to Buffer Selects includes this buffer it is by definition an overflow condition. That stream will cause no writes to occur, and only SO_PRIM_STORAGE_NEEDED[<stream>] will increment.		

<b>3DSTATE_SO_BUFFER</b>			
	30:29 <b>SO Buffer Index</b> Format: <table border="1" style="display: inline-table;"><tr><td> </td><td>U2</td></tr></table> Specifies which of the four SO Buffers is being defined.		U2
		U2	
	28:22 <b>SO Buffer Object Control State</b> Format: <table border="1" style="display: inline-table;"><tr><td> </td><td>MEMORY_OBJECT_CONTROL_STATE</td></tr></table> Specifies the memory object control state for the SO buffer.		MEMORY_OBJECT_CONTROL_STATE
		MEMORY_OBJECT_CONTROL_STATE	
	21 <b>Stream Offset Write Enable</b> Format: <table border="1" style="display: inline-table;"><tr><td> </td><td>Enable</td></tr></table> When set, this field allows the hardware to write SO_WRITE_OFFSET[Buffer#] as specified in the Stream Offset field. <b>Programming Notes</b> The field is operates irrespective of whether SO Buffer Enable is set or clear.		Enable
		Enable	
20 <b>Stream Output Buffer Offset Address Enable</b> Format: <table border="1" style="display: inline-table;"><tr><td> </td><td>Enable</td></tr></table> When set, this field allows the hardware to read/write the stream output buffer offset as specified in the "Stream Output Buffer Offset Address" field. <b>Programming Notes</b> The field is operates irrespective of whether SO Buffer Enable is set or clear.		Enable	
	Enable		
19:12 <b>Reserved</b> Format: <table border="1" style="display: inline-table;"><tr><td> </td><td>MBZ</td></tr></table>		MBZ	
	MBZ		
11:0 <b>Reserved</b> Format: <table border="1" style="display: inline-table;"><tr><td> </td><td>MBZ</td></tr></table>		MBZ	
	MBZ		
2..3	63:48 <b>Reserved</b> Format: <table border="1" style="display: inline-table;"><tr><td> </td><td>MBZ</td></tr></table>		MBZ
		MBZ	
	47:2 <b>Surface Base Address</b> Format: <table border="1" style="display: inline-table;"><tr><td> </td><td>GraphicsAddress[47:2]SurfaceBase</td></tr></table> This field specifies the starting DWord address of the buffer in Graphics Memory.		GraphicsAddress[47:2]SurfaceBase
	GraphicsAddress[47:2]SurfaceBase		
1:0 <b>Reserved</b> Format: <table border="1" style="display: inline-table;"><tr><td> </td><td>MBZ</td></tr></table>		MBZ	
	MBZ		
4	31:30 <b>Reserved</b> Format: <table border="1" style="display: inline-table;"><tr><td> </td><td>MBZ</td></tr></table>		MBZ
		MBZ	
29:0 <b>Surface Size</b> Format: <table border="1" style="display: inline-table;"><tr><td> </td><td>U30-1</td></tr></table> This field specifies the size of buffer in number DWords minus 1 of the buffer in Graphics Memory.		U30-1	
	U30-1		



<b>3DSTATE_SO_BUFFER</b>											
5..6	63:48	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ							
	Format:	MBZ									
	47:2	<p><b>Stream Output Buffer Offset Address</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 20%;">Format:</td> <td>GraphicsAddress[47:2]OutputBuffer</td> </tr> </table> <p>This field specifies the high 16 bits of address of the buffer in Graphics Memory where the Stream Output Buffer Offset is stored when all the data has been written. It is also used to fetch the stream Output buffer Offset when needed.</p>	Format:	GraphicsAddress[47:2]OutputBuffer							
Format:	GraphicsAddress[47:2]OutputBuffer										
1:0	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ								
Format:	MBZ										
7	31:0	<p><b>Stream Offset</b></p> <p>This field specifies the Offset in stream output buffer to start at, or whether to append to the end of an existing buffer. The Offset must be DWORD aligned. If Stream Offset is equal to 0xFFFFFFFF then load the value at the Stream Output Buffer Offset address into SO_WRITE_OFFSET[Buffer#]. Otherwise, SO_WRITE_OFFSET[Buffer#] = Stream Offset.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #e1eef6;"> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">FFFFFFFFh</td> <td></td> <td>Load the value at the Stream Output Buffer Offset address into MMIO_SO_OFFSET[ Buffer# ].</td> </tr> <tr> <td style="text-align: center;">xxxxxxxx xxxxxxxx xxxxxxxx xxxxxx00b</td> <td></td> <td>MMIO_SO_OFFSET[ Buffer# ] = Stream Offset</td> </tr> </tbody> </table>	Value	Name	Description	FFFFFFFFh		Load the value at the Stream Output Buffer Offset address into MMIO_SO_OFFSET[ Buffer# ].	xxxxxxxx xxxxxxxx xxxxxxxx xxxxxx00b		MMIO_SO_OFFSET[ Buffer# ] = Stream Offset
Value	Name	Description									
FFFFFFFFh		Load the value at the Stream Output Buffer Offset address into MMIO_SO_OFFSET[ Buffer# ].									
xxxxxxxx xxxxxxxx xxxxxxxx xxxxxx00b		MMIO_SO_OFFSET[ Buffer# ] = Stream Offset									

### 3DSTATE\_SO\_DECL\_LIST

3DSTATE_SO_DECL_LIST						
Project:		CHV, BSW				
Source:		RenderCS				
Length Bias:		2				
DWord	Bit	Description				
0	31:29	<b>Command Type</b>				
		Default Value:	3h GFXPIPE			
		Format:	OpCode			
	28:27	<b>Command SubType</b>				
		Default Value:	3h GFXPIPE_3D			
		Format:	OpCode			
	26:24	<b>3D Command Opcode</b>				
		Default Value:	1h 3DSTATE_NONPIPELINED			
		Format:	OpCode			
	23:16	<b>3D Command Sub Opcode</b>				
Default Value:		17h 3DSTATE_SO_DECL_LIST				
Format:		OpCode				
15:9	<b>Reserved</b>					
	Format:	MBZ				
8:0	<b>DWord Length</b>					
	Format:	=n Total Length - 2				
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[1,257]</td> <td>Excludes DWORD (0,1) 0-128 Entries</td> <td>Value = 2 * (# of SO_DECL quads) + 1</td> </tr> </tbody> </table>	Value	Name	Description	[1,257]	Excludes DWORD (0,1) 0-128 Entries
Value	Name	Description				
[1,257]	Excludes DWORD (0,1) 0-128 Entries	Value = 2 * (# of SO_DECL quads) + 1				
1	31:16	<b>Reserved</b>				
		Format:	MBZ			
	15:12	<b>Stream to Buffer Selects [3]</b>				
		Format: U4 bitmask Identifies to which SO Buffers stream 3 outputs. See Stream To Buffer Selects [0] field description.				
11:8	<b>Stream to Buffer Selects [2]</b>					
	Format: U4 bitmask Identifies to which SO Buffers stream 2 outputs. See Stream To Buffer Selects [0] field description.					

<b>3DSTATE_SO_DECL_LIST</b>												
	<p><b>7:4 Stream to Buffer Selects [1]</b></p> <table border="1"> <tr> <td>Format:</td> <td>U4 bitmask</td> </tr> </table> <p>Identifies to which SO Buffers stream 1 outputs. See Stream To Buffer Selects [0] field description.</p>	Format:	U4 bitmask									
	Format:	U4 bitmask										
<p><b>3:0 Stream to Buffer Selects [0]</b></p> <table border="1"> <tr> <td>Format:</td> <td>U4 bitmask</td> </tr> </table> <p>Identifies to which SO Buffers stream 0 outputs (irrespective of whether those buffers are enabled via 3DSTATE_STREAMOUT). Software is required to scan the SO_DECL list in order to provide this summary information. Note: For "inactive" streams, software must program this field to all zero (no buffers written to) and the corresponding Num Entries field to zero (no valid SO_DECLs).</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>1xxxb</td> <td>SO Buffer 3</td> </tr> <tr> <td>x1xxb</td> <td>SO Buffer 2</td> </tr> <tr> <td>xx1xb</td> <td>SO Buffer 1</td> </tr> <tr> <td>xxx1b</td> <td>SO Buffer 0</td> </tr> </tbody> </table>	Format:	U4 bitmask	Value	Name	1xxxb	SO Buffer 3	x1xxb	SO Buffer 2	xx1xb	SO Buffer 1	xxx1b	SO Buffer 0
Format:	U4 bitmask											
Value	Name											
1xxxb	SO Buffer 3											
x1xxb	SO Buffer 2											
xx1xb	SO Buffer 1											
xxx1b	SO Buffer 0											
2	<p><b>31:24 Num Entries [3]</b></p> <table border="1"> <tr> <td>Format:</td> <td>U8 #entries</td> </tr> </table> <p>Specifies the number of valid SO_DECL entries for Stream 3. (See notes in Num Entries [0] field description).</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>[0,128]</td> <td>entries</td> </tr> </tbody> </table>	Format:	U8 #entries	Value	Name	[0,128]	entries					
	Format:	U8 #entries										
Value	Name											
[0,128]	entries											
<p><b>23:16 Num Entries [2]</b></p> <table border="1"> <tr> <td>Format:</td> <td>U8 #entries</td> </tr> </table> <p>Specifies the number of valid SO_DECL entries for Stream 2. (See notes in Num Entries [0] field description).</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>[0,128]</td> <td>entries</td> </tr> </tbody> </table>	Format:	U8 #entries	Value	Name	[0,128]	entries						
Format:	U8 #entries											
Value	Name											
[0,128]	entries											
<p><b>15:8 Num Entries [1]</b></p> <table border="1"> <tr> <td>Format:</td> <td>U8 #entries</td> </tr> </table> <p>Specifies the number of valid SO_DECL entries for Stream 1. (See notes in Num Entries [0] field description).</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>[0,128]</td> <td>entries</td> </tr> </tbody> </table>	Format:	U8 #entries	Value	Name	[0,128]	entries						
Format:	U8 #entries											
Value	Name											
[0,128]	entries											

<b>3DSTATE_SO_DECL_LIST</b>				
	7:0	<b>Num Entries [0]</b>		
		Format: U8 #entries		
		Specifies the number of valid SO_DECL entries for Stream 0. Note that the SO_DECLs are programmed in groups of four (one SO_DECL for each of the four streams). Therefore the number of 2-DWord groups of SO_DECLs supplied in this command is derived from the stream(s) with the most valid SO_DECLs. The NumEntries value specific to each stream will indicate how many SO_DECLs are valid for that particular stream. Any trailing invalid SO_DECLs supplied for streams with fewer valid SO_DECLs will be ignored. It is legal to specify Num Entries = 0 for all four streams simultaneously. In this case there will be no SO_DECLs included in the command (only DW 0-2). Note that all Stream to Buffer Selects bits must be zero in this case (as no streams produce output).		
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">[0,128]</td> <td style="text-align: center;">entries</td> </tr> </tbody> </table>	Value	Name
Value	Name			
[0,128]	entries			
3..n	63:0	<b>Entry</b>		
		Format: SO_DECL_ENTRY [CHV, BSW]		

## 3DSTATE\_STENCIL\_BUFFER

<b>3DSTATE_STENCIL_BUFFER</b>			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
Description		Project	
This command sets the surface state of the separate stencil buffer, delivered as a pipelined state command. However, the state change pipelining isn't completely transparent (see restriction below).			
WM HW will internally manage the draining pipe and flushing of the caches when this command is issued. The PIPE_CONTROL restrictions are removed.		CHV, BSW	
Programming Notes		Project	
Restriction: Prior to changing Depth/Stencil Buffer state (i.e., any combination of 3DSTATE_DEPTH_BUFFER, 3DSTATE_CLEAR_PARAMS, 3DSTATE_STENCIL_BUFFER, 3DSTATE_HIER_DEPTH_BUFFER) SW must first issue a pipelined depth stall (PIPE_CONTROL with Depth Stall bit set, followed by a pipelined depth cache flush (PIPE_CONTROL with Depth Flush Bit set, followed by another pipelined depth stall (PIPE_CONTROL with Depth Stall Bit set), unless SW can otherwise guarantee that the pipeline from WM onwards is already flushed (e.g., via a preceding MI_FLUSH).			
The stencil buffer is always Tile-W		CHV, BSW	
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
		Default Value:	06h 3DSTATE_STENCIL_BUFFER
		Format:	OpCode
15:8	<b>Reserved</b>		
	Format:	MBZ	
7:0	<b>Dword Length</b>		
	Format:	=n Total Length - 2	

<b>3DSTATE_STENCIL_BUFFER</b>																
Value	Name	Project														
3h	Excludes Dword (0,1) <b>[Default]</b>	CHV, BSW														
1	31	<p><b>Stencil Buffer Enable</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>When set indicates that there is a valid stencil buffer.</p> <table border="1"> <tr> <th colspan="2" style="text-align: center;">Programming Notes</th> </tr> <tr> <td colspan="2">This bit should be "0" if Depth buffer surface format is D16_UNORM OR Depth buffer surface type is NULL.</td> </tr> </table>	Project:	CHV, BSW	Format:	U1	Programming Notes		This bit should be "0" if Depth buffer surface format is D16_UNORM OR Depth buffer surface type is NULL.							
Project:	CHV, BSW															
Format:	U1															
Programming Notes																
This bit should be "0" if Depth buffer surface format is D16_UNORM OR Depth buffer surface type is NULL.																
	30:29	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ												
Format:	MBZ															
	28:22	<p><b>Stencil Buffer Object Control State</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MEMORY_OBJECT_CONTROL_STATE</td> </tr> </table> <p>Specifies the memory object control state for the stencil buffer.</p>	Project:	CHV, BSW	Format:	MEMORY_OBJECT_CONTROL_STATE										
Project:	CHV, BSW															
Format:	MEMORY_OBJECT_CONTROL_STATE															
	21:17	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ												
Format:	MBZ															
	16:0	<p><b>Surface Pitch</b></p> <table border="1"> <tr> <td>Format:</td> <td>U17-1 Pitch in Bytes</td> </tr> </table> <p>This field specifies the pitch of the stencil buffer in (#Bytes - 1).</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">[127, 1FFFFh]</td> <td></td> <td>corresponding to [128B, 128KB]also restricted to a multiple of 128B</td> </tr> </tbody> </table> <table border="1"> <tr> <th colspan="2" style="text-align: center;">Programming Notes</th> </tr> <tr> <td colspan="2">Since this surface is tiled, the pitch specified must be a multiple of the tile pitch, in the range [128B, 128KB].</td> </tr> <tr> <td colspan="2">The pitch must be set to 2x the value computed based on width, as the stencil buffer is stored with two rows interleaved. For details on the separate stencil buffer storage format in memory, see GPU Overview (vol1a), Memory Data Formats, Surface Layout, 2D Surfaces, Stencil Buffer Layout (section 8.20.4.8).</td> </tr> </table>	Format:	U17-1 Pitch in Bytes	Value	Name	Description	[127, 1FFFFh]		corresponding to [128B, 128KB]also restricted to a multiple of 128B	Programming Notes		Since this surface is tiled, the pitch specified must be a multiple of the tile pitch, in the range [128B, 128KB].		The pitch must be set to 2x the value computed based on width, as the stencil buffer is stored with two rows interleaved. For details on the separate stencil buffer storage format in memory, see GPU Overview (vol1a), Memory Data Formats, Surface Layout, 2D Surfaces, Stencil Buffer Layout (section 8.20.4.8).	
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Since this surface is tiled, the pitch specified must be a multiple of the tile pitch, in the range [128B, 128KB].																
The pitch must be set to 2x the value computed based on width, as the stencil buffer is stored with two rows interleaved. For details on the separate stencil buffer storage format in memory, see GPU Overview (vol1a), Memory Data Formats, Surface Layout, 2D Surfaces, Stencil Buffer Layout (section 8.20.4.8).																
2..3 <b>Project:</b> CHV, BSW	63:0	<p><b>Surface Base Address</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[63:0]Stencil_Buffer</td> </tr> </table> <p>This field specifies the address of the buffer in Graphics Memory.</p> <table border="1"> <tr> <th colspan="2" style="text-align: center;">Programming Notes</th> </tr> <tr> <td colspan="2">The Stencil Buffer can only be mapped to Main Memory (uncached).</td> </tr> </table>	Project:	CHV, BSW	Format:	GraphicsAddress[63:0]Stencil_Buffer	Programming Notes		The Stencil Buffer can only be mapped to Main Memory (uncached).							
Project:	CHV, BSW															
Format:	GraphicsAddress[63:0]Stencil_Buffer															
Programming Notes																
The Stencil Buffer can only be mapped to Main Memory (uncached).																

<b>3DSTATE_STENCIL_BUFFER</b>							
4 <b>Project:</b> CHV, BSW	31:15	<b>Reserved</b>					
		<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ	
	Project:	CHV, BSW					
	Format:	MBZ					
	14:0	<b>Surface QPitch</b>					
		<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>QPitch[16:2]</td> </tr> </table>		Project:	CHV, BSW	Format:	QPitch[16:2]
		Project:	CHV, BSW				
		Format:	QPitch[16:2]				
		<b>Description</b>					
		This field specifies the distance in rows between array slices. It is used only in the following cases: <ul style="list-style-type: none"> <li>• <b>Surface Array</b> is enabled <i>OR</i></li> <li>• <b>Number of Multisamples</b> is not NUMSAMPLES_1 and <b>Multisampled Surface Storage Format</b> set to MSFMT_MSS <i>OR</i></li> <li>• <b>Surface Type</b> is SURFTYPE_CUBE</li> </ul>					
<b>Project</b>							
CHV, BSW							
<table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 25%;">Value</th> <th style="width: 25%;">Name</th> <th style="width: 50%;">Description</th> </tr> </thead> <tbody> <tr> <td>[4h,1FFFCh]</td> <td></td> <td>in multiples of 4 (low 2 bits missing)</td> </tr> </tbody> </table>		Value	Name	Description	[4h,1FFFCh]		in multiples of 4 (low 2 bits missing)
Value	Name	Description					
[4h,1FFFCh]		in multiples of 4 (low 2 bits missing)					
<b>Programming Notes</b>							
This field must be set to an integer multiple of 8 (QPitch[2] MBZ) Software must ensure that this field is set to a value sufficiently large such that the array slices in the surface do not overlap. Refer to the Memory Data Formats section for information on how surfaces are stored in memory.							

## 3DSTATE\_STREAMOUT

3DSTATE_STREAMOUT			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
This command contains pipelined state required by the SOL unit.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
		Default Value:	1Eh 3DSTATE_STREAMOUT
		Format:	OpCode
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	3h Excludes DWord (0,1)	
	Project:	CHV, BSW	
	Format:	=n Total Length - 2	
1	31	<b>SO Function Enable</b>	
		Project:	All
		Format:	U1
<p>If set, the SO function is enabled. Vertex data will be streamed out to memory (subject to overflow detection) as controlled by the various SO-related state variables. If clear, the SO function is disabled, and therefore no vertex data will be streamed out to memory. However, the Rendering Disable and Render Stream Select fields will still be used to determine which vertices (if any) are forwarded down the pipeline for (possible) rendering.</p>			



## 3DSTATE\_STREAMOUT

30	<b>API Rendering Disable</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>If set, Indicates the API wants the SO stage not to forward any topologies down the pipeline. If clear, Indicates the API wants the SO stage to forward topologies associated with <b>Render Stream Select</b> down the pipeline. This bit is used even if <b>SO Function Enable</b> is DISABLED.</p> <table border="1" style="width: 100%; border-collapse: collapse; background-color: #e6f2ff;"> <tr> <th style="text-align: center;">Programming Notes</th> </tr> </table> <p>The SOL unit generates an SOL_INT::Render_Enable which ultimately controls whether rendering occurs or not.</p>	Project:	CHV, BSW	Format:	U1	Programming Notes							
Project:	CHV, BSW													
Format:	U1													
Programming Notes														
29	<b>Reserved</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ								
Project:	All													
Format:	MBZ													
28:27	<b>Render Stream Select</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U2</td> </tr> </table> <table border="1" style="width: 100%; border-collapse: collapse; background-color: #e6f2ff;"> <tr> <th style="text-align: center;">Description</th> </tr> </table> <p>This field specifies which stream has been selected to be forwarded down the pipeline for possible rendering. Topologies from other streams will not be passed down the pipeline. If Rendering Disable is set, this field is ignored, as no topologies are sent down the pipeline.</p> <p>SO Function Enable must also be ENABLED in order for this field to select a stream for rendering. When <b>SO Function Enable</b> is DISABLED and Rendering Disable is cleared (i.e., rendering is enabled), StreamID is ignored downstream of the SO stage, allowing any stream to be rendered.</p>	Project:	All	Format:	U2	Description							
Project:	All													
Format:	U2													
Description														
26	<b>Reorder Mode</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> </table> <p>This bit controls how vertices of triangle objects in TRISTRIP[_ADJ] and TRISTRIP_REV are reordered for the purposes of stream-out only (does not impact rendering). See table in Input Buffering.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 75%;">Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>LEADING</td> <td>Reorder the vertices of alternating triangles of a TRISTRIP[_ADJ] such that the leading (first) vertices are in consecutive order starting at v0. A similar reordering is performed on alternating triangles in a TRISTRIP_REV.</td> </tr> <tr> <td>1h</td> <td>TRAILING</td> <td>Reorder the vertices of alternating triangles of a TRISTRIP[_ADJ] such that the trailing (last) vertices are in consecutive order starting at v2. A similar reordering is performed on alternating triangles in a TRISTRIP_REV.</td> </tr> </tbody> </table>	Project:	All	Value	Name	Description	0h	LEADING	Reorder the vertices of alternating triangles of a TRISTRIP[_ADJ] such that the leading (first) vertices are in consecutive order starting at v0. A similar reordering is performed on alternating triangles in a TRISTRIP_REV.	1h	TRAILING	Reorder the vertices of alternating triangles of a TRISTRIP[_ADJ] such that the trailing (last) vertices are in consecutive order starting at v2. A similar reordering is performed on alternating triangles in a TRISTRIP_REV.	
Project:	All													
Value	Name	Description												
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1h	TRAILING	Reorder the vertices of alternating triangles of a TRISTRIP[_ADJ] such that the trailing (last) vertices are in consecutive order starting at v2. A similar reordering is performed on alternating triangles in a TRISTRIP_REV.												
25	<b>SO Statistics Enable</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This bit controls whether StreamOutput statistics register(s) can be incremented.</p>	Project:	All	Format:	Enable								
Project:	All													
Format:	Enable													

<b>3DSTATE_STREAMOUT</b>				
	<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>
	0h	Disable	SO_NUM_PRIMS_WRITTEN[0..3] and SO_PRIM_STORAGE_NEEDED[0..3] registers cannot increment.	All
	1h	Enable	SO_NUM_PRIMS_WRITTEN[0..3] and SO_PRIM_STORAGE_NEEDED[0..3] registers can increment.	All
24:23	<b>Force Rendering</b>			
	Project:		CHV, BSW	
	This field provides a work around override for the computation of SOL_INT::Render_Enable			
	<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>
	0h	Normal	SOL_INT::Render_Enable is computed normally	All
	1h	Reserved		All
	2h	Force_Off	Forces the rendering to be disabled.	All
	3h	Force_on	Forces the rendering to be enabled.	All
22:12	<b>Reserved</b>			
	Project:		All	
	Format:		MBZ	
11:8	<b>Reserved</b>			
	Project:		CHV, BSW	
	Format:		MBZ	
7:0	<b>Reserved</b>			
	Project:		All	
	Format:		MBZ	
2	31:30	<b>Reserved</b>		
		Project:		All
		Format:		MBZ
	29	<b>Stream 3 Vertex Read Offset</b>		
		Project:	All	
		Format:	U1 count of 256-bit units	
	Specifies amount of data to skip over before reading back Stream 3 vertex data. (See <b>Stream 0 Vertex Read Offset</b> )			
	28:24	<b>Stream 3 Vertex Read Length</b>		
		Project:	All	
		Format:	U5-1 count of 256-bit units	
	(See Stream 0 Vertex Read Length)			
	23:22	<b>Reserved</b>		

<b>3DSTATE_STREAMOUT</b>					
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ
Project:	All				
Format:	MBZ				
21	<p><b>Stream 2 Vertex Read Offset</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U1 count of 256-bit units</td> </tr> </table> <p>Specifies amount of data to skip over before reading back Stream 2 vertex data. (See Stream 0 Vertex Read Offset)</p>	Project:	All	Format:	U1 count of 256-bit units
Project:	All				
Format:	U1 count of 256-bit units				
20:16	<p><b>Stream 2 Vertex Read Length</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U5-1 count of 256-bit units</td> </tr> </table>	Project:	All	Format:	U5-1 count of 256-bit units
Project:	All				
Format:	U5-1 count of 256-bit units				
15:14	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ
Project:	All				
Format:	MBZ				
13	<p><b>Stream 1 Vertex Read Offset</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U1 count of 256-bit units</td> </tr> </table> <p>Specifies amount of data to skip over before reading back Stream 1 vertex data. (See Stream 0 Vertex Read Offset)</p>	Project:	All	Format:	U1 count of 256-bit units
Project:	All				
Format:	U1 count of 256-bit units				
12:8	<p><b>Stream 1 Vertex Read Length</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U5-1 count of 256-bit units</td> </tr> </table> <p>(See Stream 0 Vertex Read Length)</p>	Project:	All	Format:	U5-1 count of 256-bit units
Project:	All				
Format:	U5-1 count of 256-bit units				
7:6	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ
Project:	All				
Format:	MBZ				
5	<p><b>Stream 0 Vertex Read Offset</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U1 count of 256-bit units</td> </tr> </table> <p>Specifies amount of data to skip over before reading back Stream 0 vertex data. Must be zero if the GS is enabled and the Output Vertex Size field in 3DSTATE_GS is programmed to 0 (i.e., one 16B unit).</p>	Project:	All	Format:	U1 count of 256-bit units
Project:	All				
Format:	U1 count of 256-bit units				
4:0	<p><b>Stream 0 Vertex Read Length</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U5-1 count of 256-bit units</td> </tr> </table>	Project:	All	Format:	U5-1 count of 256-bit units
Project:	All				
Format:	U5-1 count of 256-bit units				

<b>3DSTATE_STREAMOUT</b>									
	<p>Specifies amount of vertex data to read back for Stream 0 vertices, starting at the Stream 0 Vertex Read Offset location. Maximum readback is 17 256-bit units (34 128-bit vertex attributes). Read data past the end of the valid vertex data has undefined contents, and therefore shouldn't be used to source stream out data. Must be zero (i.e., read length = 256b) if the GS is enabled and the Output Vertex Size field in 3DSTATE_GS is programmed to 0 (i.e., one 16B unit).</p>								
<b>3</b> <b>Project:</b> CHV, BSW	<b>31:28</b> <b>Reserved</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ				
	Project:	CHV, BSW							
	Format:	MBZ							
	<b>27:16</b> <b>Buffer 1 Surface Pitch</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table>	Project:	CHV, BSW						
	Project:	CHV, BSW							
	<b>15:12</b> <b>Reserved</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ				
	Project:	CHV, BSW							
	Format:	MBZ							
	<b>11:0</b> <b>Buffer 0 Surface Pitch</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U12 pitch in Bytes</td> </tr> </table> <p>This field specifies the pitch of the SO buffer in #Bytes.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 30%;">Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>[0,2048]</td> <td>Must be 0 or a multiple of 4 Bytes.</td> </tr> </tbody> </table> <div style="text-align: center; background-color: #e6f2ff; padding: 5px; margin-top: 10px;"><b>Programming Notes</b></div> <p>A Surface Pitch of 0 indicates an un-bound buffer. No writes are performed. Surface Base Address is ignored.</p>	Project:	CHV, BSW	Format:	U12 pitch in Bytes	Value	Name	[0,2048]	Must be 0 or a multiple of 4 Bytes.
	Project:	CHV, BSW							
Format:	U12 pitch in Bytes								
Value	Name								
[0,2048]	Must be 0 or a multiple of 4 Bytes.								
<b>4</b> <b>Project:</b> CHV, BSW	<b>31:28</b> <b>Reserved</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ				
	Project:	CHV, BSW							
	Format:	MBZ							
	<b>27:16</b> <b>Buffer 3 Surface Pitch</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U12</td> </tr> </table>	Project:	CHV, BSW	Format:	U12				
	Project:	CHV, BSW							
	Format:	U12							
	<b>15:12</b> <b>Reserved</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ				
	Project:	CHV, BSW							
Format:	MBZ								
<b>11:0</b> <b>Buffer 2 Surface Pitch</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U12</td> </tr> </table>	Project:	CHV, BSW	Format:	U12					
Project:	CHV, BSW								
Format:	U12								

## 3DSTATE\_TE

3DSTATE_TE			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
For [CHV, BSW], the state used by TE is defined with this inline state packet.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
Default Value:		0h 3DSTATE_PIPELINED	
Format:		OpCode	
23:16	<b>3D Command Sub Opcode</b>		
	Default Value:	1Ch 3DSTATE_TE	
	Format:	OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	2h Excludes DWord (0,1)	
	Project:	All	
	Format:	=n Total Length - 2	
1	31:20	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	19	<b>Reserved</b>	
		Project:	CHV, BSW
		Format:	MBZ
18:16	<b>Reserved</b>		
	Project:	CHV, BSW	
	Format:	MBZ	

<b>3DSTATE_TE</b>				
15:14	<b>Reserved</b>			
	Project:	All		
	Format:	MBZ		
	13:12	<b>Partitioning</b>		
		Project:	All	
		Format:	U2	
		This field specifies how edges are partitioned based on tessellation factor.		
		<b>Value</b>	<b>Name</b>	<b>Description</b>
	0h	INTEGER	Outside/inside edges are divided into an integer number of equal-sized segments.	All
	1h	ODD_FRACTIONAL	Outside/inside edges are divided into an odd number of possibly-unequal-sized segments.	All
	2h	EVEN_FRACTIONAL	Outside/inside edges are divided into an even number of possibly-unequal-sized segments.	All
	11:10	<b>Reserved</b>		
		Project:	All	
		Format:	MBZ	
	9:8	<b>Output Topology</b>		
Project:		All		
Format:		U2		
This field specifies which primitive types are to be output.				
<b>Value</b>		<b>Name</b>	<b>Description</b>	<b>Project</b>
0h	POINT	Points are output (as POINTLIST topologies)	All	
1h	LINE	Lines are output (as LINESTRIP topologies). Only valid if ISOLINE domain is selected.	All	
2h	TRI_CW	Clockwise-ordered triangles are output (either as TRISTRIP, TRISTRIP_REV or TRILIST topologies). Not valid if ISOLINE domain is selected.	All	
3h	TRI_CCW	Count-clockwise-ordered triangles are output (either as TRISTRIP, TRISTRIP_REV or TRILIST topologies). Not valid if ISOLINE domain is selected.	All	
7:6	<b>Reserved</b>			
	Project:	All		
	Format:	MBZ		
5:4	<b>TE Domain</b>			
	Project:	All		
	Format:	U2		
This field specifies which type of domain is to be tessellated.				

<b>3DSTATE_TE</b>					
	<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>	
	0h	QUAD	2D (U, V) domain is tessellated	All	
	1h	TRI	Triangular (U, V, W) domain is tessellated	All	
	2h	ISOLINE	2D (U, V) domain is tessellated.	All	
	3	<b>Reserved</b>			
		Project:	All		
		Format:	MBZ		
	2:1	<b>TE Mode</b>			
		Project:	All		
		Format:	U2		
		When TE Enable is ENABLED, this field specifies the overall operation of the TE stage. This field is ignored if TE Enable is DISABLED.			
		<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>
		0h	HW_TESS	Normal HW Tessellation Mode. The TessFactors are read from the patch URB entry, and are used to perform fixed-function hardware tessellation of the specified domain.	All
		1h	SW_TESS	Software Tessellation Mode. The TE unit will pass down HS-thread-generated tessellated domain points instead of generating them itself from TessFactors. The TE unit will read the Domain Point Count and Domain Point Buffer Starting Address fields from the patch header, and if the count is 0 it will consider the patch culled and discard it. Otherwise the address is used to start fetching DOMAIN_POINT structures from memory and passing them down the pipeline to DS.	CHV, BSW
	0	<b>TE Enable</b>			
		Project:	All		
		Format:	Enable		
		If ENABLED, the TE stage will perform tessellation processing on incoming patch primitives. The TE Mode field determines how this tessellation operation proceeds. If DISABLED, the TE goes into pass-through mode. All other state fields are ignored.			
		<b>Programming Notes</b>			
		The tessellation stages (HS, TE and DS) must be enabled/disabled as a group. I.e., draw commands can only be issued if all three stages are enabled or all three stages are disabled, otherwise the behavior is UNDEFINED.			
2	31:0	<b>Maximum Tessellation Factor Odd</b>			
		Project:	All		
		Format:	IEEE_Float		
		This field specifies the maximum TessFactor for ODD_FRACTIONAL partitioning when in HW_TESS mode.			

<b>3DSTATE_TE</b>												
		<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td>[427c0000h,427c0000h]</td> <td>63 <b>[Default]</b></td> <td>Per API Spec, For normal operation software should set this value to 63.0</td> </tr> </tbody> </table>	Value	Name	Description	[427c0000h,427c0000h]	63 <b>[Default]</b>	Per API Spec, For normal operation software should set this value to 63.0				
Value	Name	Description										
[427c0000h,427c0000h]	63 <b>[Default]</b>	Per API Spec, For normal operation software should set this value to 63.0										
		<b>Programming Notes</b>										
		Note that ISOLINE's LineDensity TF is always subjected to INTEGER partitioning regardless of the Partitioning state.										
3	31:0	<p><b>Maximum Tessellation Factor Not Odd</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>IEEE_Float</td> </tr> </table> <p>This field specifies the maximum TessFactor for EVEN_FRACTIONAL or INTEGER partitioning when in HW_TESS mode.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td>[42800000h,42800000h]</td> <td>64 <b>[Default]</b></td> <td>Per API Spec, For normal operation software should set this value to 64.0</td> </tr> </tbody> </table>	Project:	All	Format:	IEEE_Float	Value	Name	Description	[42800000h,42800000h]	64 <b>[Default]</b>	Per API Spec, For normal operation software should set this value to 64.0
Project:	All											
Format:	IEEE_Float											
Value	Name	Description										
[42800000h,42800000h]	64 <b>[Default]</b>	Per API Spec, For normal operation software should set this value to 64.0										
		<b>Programming Notes</b>										
		Note that ISOLINE's LineDensity TF is always subjected to INTEGER partitioning regardless of the Partitioning state.										



## 3DSTATE\_URB\_DS

<b>3DSTATE_URB_DS</b>			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
Description			
<p>This command may not overlap with the push constants in the URB defined by the 3DSTATE_PUSH_CONSTANT_ALLOC_VS, 3DSTATE_PUSH_CONSTANT_ALLOC_DS, 3DSTATE_PUSH_CONSTANT_ALLOC_HS, and 3DSTATE_PUSH_CONSTANT_ALLOC_GS commands.</p> <p>The URB Starting Address and Number of URB Entries fields shall be programmed as if there is only one slice enabled. When more than one slice is enabled, hardware will (a) recompute the actual URB Starting Address based on the number of enabled slices and (b) multiply the Number of URB Entries by the number of enabled slices. Software shall ensure that the values programmed do not exceed the URB capacity of a single slice. Refer to the L3 allocation and programming guide for valid URB configurations.</p>			
Programming Notes			
<p>When programming DS URB state for the RCS 3D pipe, 3DSTATE_URB_VS, 3DSTATE_URB_HS, and 3DSTATE_URB_GS must also be programmed in order for the programming of this state to be valid.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
		Default Value:	32h 3DSTATE_URB_DS
		Format:	OpCode
	15:8	<b>Reserved</b>	
		Project:	All
Format:		MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	0h DWORD_COUNT_n	
	Project:	All	

<b>3DSTATE_URB_DS</b>				
		Format:	=n	
1	31:25	<b>DS URB Starting Address</b>		
		Project:	CHV, BSW	
		Format:	U7	
		Offset from the start of the URB memory where DS starts its allocation, specified in multiples of 8 KB.		
24:16	<b>DS URB Entry Allocation Size</b>			
	Project:	All		
	Format:	U9-1 Count of 512-bit units		
	Specifies the length of each URB entry owned by DS. This field is always used (even if DS Function Enable is DISABLED).			
15:0	<b>DS Number of URB Entries</b>			
	Project:	All		
	<b>Description</b>			
	Specifies the number of URB entries that are used by DS, based on only 1 slice enabled. When multiple slices are enabled, HW will multiply the value programmed by the number of slices in order to determine the total number of entries. SW shall ensure that the total number of entries does not exceed the relevant ValidValue range listed below. This field is always used (even if DS Function Enable is DISABLED).			
	If Domain Shader Thread Dispatch is Enabled then the minimum number of handles that must be allocated is 34 URB entries.			
<b>Programming Notes</b>				
DS Number of URB Entries must be divisible by 8 if the DS URB Entry Allocation Size is programmed to a value less than 9, which is 10 512-bit URB entries. "2:0" = reserved "000"				

## 3DSTATE\_URB\_GS

<b>3DSTATE_URB_GS</b>			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
Description			
<p>This command may not overlap with the push constants in the URB defined by the 3DSTATE_PUSH_CONSTANT_ALLOC_VS, 3DSTATE_PUSH_CONSTANT_ALLOC_DS, 3DSTATE_PUSH_CONSTANT_ALLOC_HS, and 3DSTATE_PUSH_CONSTANT_ALLOC_GS commands.</p> <p>The URB Starting Address and Number of URB Entries fields shall be programmed as if there is only one slice enabled. When more than one slice is enabled, hardware will (a) recompute the actual URB Starting Address based on the number of enabled slices and (b) multiply the Number of URB Entries by the number of enabled slices. Software shall ensure that the values programmed do not exceed the URB capacity of a single slice. Refer to the L3 allocation and programming guide for valid URB configurations</p>			
Programming Notes			
<p>When programming GS URB state for the RCS 3D pipe, 3DSTATE_URB_VS, 3DSTATE_URB_HS, and 3DSTATE_URB_DS must also be programmed in order for the programming of this state to be valid.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
		Default Value:	33h 3DSTATE_URB_GS
		Format:	OpCode
	15:8	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	7:0	<b>DWord Length</b>	
Default Value:		0h DWORD_COUNT_n	
Project:		All	

<b>3DSTATE_URB_GS</b>				
		Format:	=n	
1	31:25	<b>GS URB Starting Address</b>		
		Project:	CHV, BSW	
		Format:	U7	
		Offset from the start of the URB memory where GS starts its allocation, specified in multiples of 8 KB.		
		<b>Value</b>	<b>Name</b>	<b>Project</b>
	[0,48]			Device[SliceCount] == 1
	[4,48]			Device[SliceCount] GT 1
	24:16	<b>GS URB Entry Allocation Size</b>		
		Project:	All	
		Format:	U9-1 512-bit units	
Specifies the length of each URB entry owned by GS. This field is always used (even if GS Function Enable is DISABLED).				
15:0	<b>GS Number of URB Entries</b>			
	Project:	All		
	Specifies the number of URB entries that are used by GS, based on only 1 slice enabled. When multiple slices are enabled, HW will multiply the value programmed by the number of slices in order to determine the total number of entries. SW shall ensure that the total number of entries does not exceed the relevant ValidValue range listed below.			
	This field is always used (even if GS Function Enable is DISABLED).			
	<b>Value</b>	<b>Name</b>	<b>Project</b>	
	[0,960]		CHV, BSW	
	[0,256]		CHV, BSW	
	<b>Programming Notes</b>			
	Only if GS is disabled can this field be programmed to 0. If GS is enabled this field shall be programmed to a value greater than 0. For GS Dispatch Mode "Single", this field shall be programmed to a value greater than or equal to 1. For other GS Dispatch Modes, refer to the definition of Dispatch Mode (3DSTATE_GS) for minimum values of this field.			
	GS Number of URB Entries must be divisible by 8 if the GS URB Entry Allocation Size is less than 9 512-bit URB entries. "2:0" = reserved "000"			

## 3DSTATE\_URB\_HS

<b>3DSTATE_URB_HS</b>			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
Description			
<p>This command may not overlap with the push constants in the URB defined by the 3DSTATE_PUSH_CONSTANT_ALLOC_VS, 3DSTATE_PUSH_CONSTANT_ALLOC_DS, 3DSTATE_PUSH_CONSTANT_ALLOC_HS, and 3DSTATE_PUSH_CONSTANT_ALLOC_GS commands.</p> <p>The URB Starting Address and Number of URB Entries fields shall be programmed as if there is only one slice enabled. When more than one slice is enabled, hardware will (a) recompute the actual URB Starting Address based on the number of enabled slices and (b) multiply the Number of URB Entries by the number of enabled slices. Software shall ensure that the values programmed do not exceed the URB capacity of a single slice. Refer to the L3 allocation and programming guide for valid URB configurations</p>			
Programming Notes			
<p>When programming HS URB state for the RCS 3D pipe, 3DSTATE_URB_VS, 3DSTATE_URB_DS, and 3DSTATE_URB_GS must also be programmed in order for the programming of this state to be valid.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
		Default Value:	31h 3DSTATE_URB_HS
		Format:	OpCode
	15:8	<b>Reserved</b>	
		Project:	All
Format:		MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	0h DWORD_COUNT_n	
	Format:	=n	

<b>3DSTATE_URB_HS</b>															
1	31:25	<b>HS URB Starting Address</b>													
		Project:	CHV, BSW												
		Format:	U7												
		Offset from the start of the URB memory where HS starts its allocation, specified in multiples of 8 KB.													
			<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 25%;">Value</th> <th style="width: 25%;">Name</th> <th style="width: 25%;">Project</th> <th style="width: 25%;">Exists If</th> </tr> </thead> <tbody> <tr> <td>[0,48]</td> <td></td> <td></td> <td>Device[SliceCount] == 1</td> </tr> <tr> <td>[4,48]</td> <td></td> <td></td> <td>Device[SliceCount] GT 1</td> </tr> </tbody> </table>	Value	Name	Project	Exists If	[0,48]			Device[SliceCount] == 1	[4,48]			Device[SliceCount] GT 1
	Value	Name	Project	Exists If											
	[0,48]			Device[SliceCount] == 1											
	[4,48]			Device[SliceCount] GT 1											
			<table border="1" style="width: 100%; border-collapse: collapse;"> <tbody> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U9-1 Count of 512-bit units</td> </tr> </tbody> </table>	Project:	All	Format:	U9-1 Count of 512-bit units								
	Project:	All													
Format:	U9-1 Count of 512-bit units														
		Specifies the length of each URB entry owned by HS. This field is always used (even if HS Function Enable is DISABLED).													
15:0		<b>HS Number of URB Entries</b>													
		Project:	All												
		Specifies the number of URB entries that are used by HS, based on only 1 slice enabled. When multiple slices are enabled, HW will multiply the value programmed by the number of slices in order to determine the total number of entries. SW shall ensure that the total number of entries does not exceed the relevant ValidValue range listed below. This field is always used (even if HS Function Enable is DISABLED). Programming Restriction:HS Number of URB Entries must be divisible by 8 if the HS URB Entry Allocation Size is less than 9 512-bit URB entries."2:0" = reserved "000"													
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 30%;">Value</th> <th style="width: 30%;">Name</th> <th style="width: 40%;">Project</th> </tr> </thead> <tbody> <tr> <td>[0,504]</td> <td></td> <td>CHV, BSW</td> </tr> <tr> <td>[0,80]</td> <td></td> <td>CHV, BSW</td> </tr> </tbody> </table>	Value	Name	Project	[0,504]		CHV, BSW	[0,80]		CHV, BSW				
Value	Name	Project													
[0,504]		CHV, BSW													
[0,80]		CHV, BSW													

## 3DSTATE\_URB\_VS

<b>3DSTATE_URB_VS</b>			
Project:	CHV, BSW		
Source:	RenderCS, PositionCS		
Length Bias:	2		
Description			
VS URB Entry Allocation Size equal to 4(5 512-bit URB rows) may cause performance to decrease due to banking in the URB. Element sizes of 16 to 20 should be programmed with six 512-bit URB rows.			
This command may not overlap with the push constants in the URB defined by the 3DSTATE_PUSH_CONSTANT_ALLOC_VS, 3DSTATE_PUSH_CONSTANT_ALLOC_DS, 3DSTATE_PUSH_CONSTANT_ALLOC_HS, and 3DSTATE_PUSH_CONSTANT_ALLOC_GS commands.			
The offset and size should be programmed as if there is only one slice enabled. Hardware will grow the size based on the slice configuration. Software shall ensure that the values programmed do not exceed the URB capacity of one slice. Refer to the L3 allocation and programming guide for valid URB configurations.			
Programming Notes			
When programming VS URB state for the RCS 3D pipe, 3DSTATE_URB_HS, 3DSTATE_URB_DS, and 3DSTATE_URB_GS must also be programmed in order for the programming of this state to be valid.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
		Default Value:	30h 3DSTATE_URB_VS
		Format:	OpCode
	15:8	<b>Reserved</b>	
		Format:	MBZ
7:0	<b>DWord Length</b>		
	Default Value:	0h DWORD_COUNT_n	
	Project:	All	
	Format:	=n	

<b>3DSTATE_URB_VS</b>																		
1	31:25	<p><b>VS URB Starting Address</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U7</td> </tr> </table> <p>Offset from the start of the URB memory where VS starts its allocation, specified in multiples of 8 KB.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> <th>Exists If</th> </tr> </thead> <tbody> <tr> <td>[0,48]</td> <td></td> <td></td> <td>Device[SliceCount] == 1</td> </tr> <tr> <td>[4,48]</td> <td></td> <td></td> <td>Device[SliceCount] GT 1</td> </tr> </tbody> </table>	Project:	CHV, BSW	Format:	U7	Value	Name	Project	Exists If	[0,48]			Device[SliceCount] == 1	[4,48]			Device[SliceCount] GT 1
	Project:	CHV, BSW																
	Format:	U7																
Value	Name	Project	Exists If															
[0,48]			Device[SliceCount] == 1															
[4,48]			Device[SliceCount] GT 1															
24:16	<p><b>VS URB Entry Allocation Size</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U9-1 count of 512-bit units</td> </tr> </table> <p>Specifies the length of each URB entry owned by VS. This field is always used (even if VS Function Enable is DISABLED).</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>[0,9]</td> <td></td> <td>CHV, BSW</td> </tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>Programming Restriction: As the VS URB entry serves as both the per-vertex input and output of the VS shader, the VS URB Allocation Size must be sized to the maximum of the vertex input and output structures.</p>	Project:	All	Format:	U9-1 count of 512-bit units	Value	Name	Project	[0,9]		CHV, BSW							
Project:	All																	
Format:	U9-1 count of 512-bit units																	
Value	Name	Project																
[0,9]		CHV, BSW																
15:0	<p><b>VS Number of URB Entries</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U16</td> </tr> </table> <p>Specifies the number of URB entries that are used by VS, based on only 1 slice enabled. When multiple slices are enabled, HW will multiply the value programmed by the number of slices in order to determine the total number of entries. SW shall ensure that the total number of entries does not exceed the relevant ValidValue range listed below. This field is always used (even if VS Function Enable is DISABLED).</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>[64,2560]</td> <td></td> </tr> <tr> <td>[34,640]</td> <td></td> </tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>Programming Restriction: VS Number of URB Entries must be divisible by 8 if the VS URB Entry Allocation Size is less than 9 512-bit URB entries."2:0" = reserved "000b"</p> <p>When tessellation is enabled, the VS Number of URB Entries must be greater than or equal to 192.</p>	Project:	All	Format:	U16	Value	Name	[64,2560]		[34,640]								
Project:	All																	
Format:	U16																	
Value	Name																	
[64,2560]																		
[34,640]																		



## 3DSTATE\_VERTEX\_BUFFERS

<b>3DSTATE_VERTEX_BUFFERS</b>		
Project:	CHV, BSW	
Source:	RenderCS	
Length Bias:	2	
Description		
This command is used to specify VB state used by the VF function.		
[CHV, BSW]: Can specify from 1 to 33 VBs.		
The VertexBufferID field within a VERTEX_BUFFER_STATE structure indicates the specific VB. If a VB definition is not included in this command, its associated state is left unchanged and is available for use if previously defined.		
Programming Notes		
It is possible to have individual vertex elements sourced completely from generated ID values and therefore not require any vertex buffer accesses for that vertex element. In this case, VF function will simply ignore the VB state associated with that vertex element. If all enabled vertex elements have this characteristic, no VBs are required to process 3DPRIMITIVE commands. For example, this might arise when the user wants to perform all data lookups in the first shader, so only generated index values need to be passed down to it. In this extreme case, SW would not need to program any VB state, and therefore not need to issue any 3DSTATE_VERTEX_BUFFERS commands.		
For any 3DSTATE_VERTEX_BUFFERS command, at least one VERTEX_BUFFER_STATE structure must be included.		
VERTEX_BUFFER_STATE structures are 4 DWords for both VERTEXDATA buffers and INSTANCEDATA buffers.		
Inclusion of partial VERTEX_BUFFER_STATE structures is UNDEFINED.		
The order in which VBs are defined within this command can be arbitrary, though a vertex buffer must be defined only once in any given command (otherwise operation is UNDEFINED).		
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 03h GFXPIPE Format: Opcode
	28:27	<b>Command SubType</b>
		Default Value: 3h 3D Format: Opcode
	26:24	<b>3D Command Opcode</b>
		Default Value: 0h 3DSTATE_VERTEX_BUFFERS Format: Opcode
	23:16	<b>3D Command Sub Opcode</b>
		Default Value: 08h 3DSTATE_VERTEX_BUFFERS Format: Opcode

<b>3DSTATE_VERTEX_BUFFERS</b>			
	15:8	<b>Reserved</b>	
	7:0	<b>DWord Length</b>	
		Format:	=n
		n = 4b-1 (where b = # of buffer states included)	
		<b>Value</b>	<b>Name</b>
3	DWORD_COUNT_n <b>[Default]</b>		
[3,131]	1-33 Buffers	CHV, BSW	
1..n	127:0	<b>Vertex Buffer State</b>	
	Format:	VERTEX_BUFFER_STATE [CHV, BSW]	

## 3DSTATE\_VERTEX\_ELEMENTS

<b>3DSTATE_VERTEX_ELEMENTS</b>		
Project:	CHV, BSW	
Source:	RenderCS	
Length Bias:	2	
Description		
This is a variable-length command used to specify the active vertex elements. Each VERTEX_ELEMENT_STATE structure contains a Valid bit which determines which elements are used.		
[CHV, BSW]: Up to 34 elements.		
Programming Notes		
[CHV, BSW]: At least one VERTEX_ELEMENT_STATE structure must be included.		
The 3DSTATE_VERTEX_ELEMENTS must not be programmed more than once before each 3DPRIMITIVE command.		
Inclusion of partial VERTEX_ELEMENT_STATE structures is UNDEFINED.		
[CHV, BSW]: SW must ensure that at least one vertex element is defined prior to issuing a 3DPRIMITIVE command, or operation is UNDEFINED.		
[CHV, BSW]: There are no 'holes' allowed in the destination vertex: NOSTORE components must be overwritten by subsequent components unless they are the trailing DWords of the vertex. Software must explicitly chose some value (probably 0) to be written into DWords that would otherwise be 'holes'.		
[CHV, BSW]: Within a VERTEX_ELEMENT_STATE structure, if a Component Control field is set to something other than VFCOMP_STORE_SRC, no higher-numbered Component Control fields may be set to VFCOMP_STORE_SRC. In other words, only trailing components can be set to something other than VFCOMP_STORE_SRC.		
[CHV, BSW]: See additional restrictions listed in the command fields and VERTEX_ELEMENT_STATE description.		
[CHV, BSW]: Element[0] must be valid.		
[CHV, BSW]: All elements must be valid from Element[0] to the last valid element. (I.e. if Element[2] is valid then Element[1] and Element[0] must also be valid).		
[CHV, BSW]: The pitch between elements packed in the URB will always be 128 bits.		
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 03h GFXPIPE
	Format: Opcode	
	28:27	<b>Command SubType</b>
Default Value: 3h 3D		
Format: Opcode		

<b>3DSTATE_VERTEX_ELEMENTS</b>				
	26:24	<b>3D Command Opcode</b>		
		Default Value:	0h 3DSTATE_VERTEX_ELEMENTS	
	Format:	Opcode		
	23:16	<b>3D Command Sub Opcode</b>		
		Default Value:	09h 3DSTATE_VERTEX_ELEMENTS	
	Format:	Opcode		
	15:8	<b>Reserved</b>		
	7:0	<b>DWord Length</b>		
		Format:	=n	
		Vertex Element Count = (DWord Count + 1) / 2		
<b>Value</b>		<b>Name</b>	<b>Description</b>	
1		DWORD_COUNT_n <b>[Default]</b>	excludes DWords 0,1	
[1,67]	Range	1-34 Elements	CHV, BSW	
1..n	63:0	<b>Element</b>		
Format:		VERTEX_ELEMENT_STATE		

## 3DSTATE\_VF

<b>3DSTATE_VF</b>			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
This command is used to set various state variables in the VF stage.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
		Default Value:	0Ch 3DSTATE_VF
		Format:	OpCode
	15:12	<b>Reserved</b>	
		Project:	All
Format:		MBZ	
11	<b>Reserved</b>		
10	<b>Reserved</b>		
9	<b>Reserved</b>		
	Project:	CHV, BSW	
	Format:	MBZ	
8	<b>Indexed Draw Cut Index Enable</b>		
	Project:	All	
	Format:	Enable	
If ENABLED, vertex indices in RANDOM 3DPRIMITIVE commands are compared to the Cut Index (specified below). When the vertex index matches the Cut Index any previous topology is terminated.If DISABLED, vertex indices are not compared to the Cut Index and are used strictly as indices into vertex buffers.This field can only be enabled for certain primitive topology types. Refer to the table later in this section for details.			

<b>3DSTATE_VF</b>		
	7:0	<b>DWord Length</b>
		Default Value: 0h Excludes DWord (0,1)
		Project: All
		Format: =n Total Length - 2
1	31:0	<b>Cut Index</b>
		Project: All
<p>This field specifies the index value that is considered the "cut index" which vertex indices are compared to if a Cut Index Enable is set. The Cut Index is compared to the fetched (and possibly-sign-extended) vertex index, and if these values are equal, the current primitive topology is terminated. Note that, for index buffers &lt;32bpp, it is possible to set the Cut Index to a (large) value that will never match a sign-extended vertex index.</p>		

## 3DSTATE\_VF\_INSTANCING

3DSTATE_VF_INSTANCING			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
This command is used to control the "instancing" state associated with a specific vertex element.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		49h 3DSTATE_VF_INSTANCING	
Format:		OpCode	
15:8	<b>Reserved</b>		
7:0	<b>DWord Length</b>		
	Format:	=n Total Length - 2	
	<b>Value</b>	<b>Name</b>	
	1h	Excludes DWord (0,1) <b>[Default]</b>	
	43h	Context Restore	
1	31:9	<b>Reserved</b>	
	8	<b>Instancing Enable</b>	
		Format:	Enable
		<b>Value</b>	<b>Name</b>
0h	Disabled	This vertex element is not instanced and therefore vertices within instances can each receive different data for this vertex element. Within each instance, the source vertex data for this vertex element is determined according the the Vertex Access Type of the 3DPRIMITIVE command. Instance Data Step Rate is ignored for this vertex element.	

<b>3DSTATE_VF_INSTANCING</b>			
	1h	Enabled	This vertex element is instanced and therefore vertices within instances will receive the same data for this vertex element. The source pointer for this particular vertex element will be (a) initialized at the start of 3DPRIMITIVE processing, (b) held constant for all vertices within an instance, and (c) advanced between instances as a function of Instance Data Step Rate.
	7:6	<b>Reserved</b>	
		Format:	MBZ
	5:0	<b>Vertex Element Index</b>	
		Format:	U6
		This field identifies which vertex element state is to be modified by this command.	
		<b>Value</b>	<b>Name</b>
		[0,33]	
2	31:0	<b>Instance Data Step Rate</b>	If Instancing Enable is ENABLED, this field determines the rate at which data for this particular vertex element is changed between instances. Only after the number of instances specified by this field is generated is new (sequential) vertex element data provided. This process continues for each group of instances defined in the 3DPRIMITIVE command. For example, a value of 1 in this field causes new data to be supplied for this vertex element with each sequential (instance) group of vertices. A value of 2 causes every other instance group of vertices to be provided with new vertex element data. The special value of 0 causes all vertices of all instances generated by the 3DPRIMITIVE command to be provided with the same data for this vertex element. (The same effect can be achieved by setting this field to its maximum value.) If Instancing Enable is DISABLED, this field is ignored.



## 3DSTATE\_VF\_SGVS

<b>3DSTATE_VF_SGVS</b>			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
<p>This command is used to control the insertion of the VertexID and InstanceID System-Generated Values (SGVs) into an input Vertex URB Entry (VUE) (available as input to a VS thread). VertexID and InstanceID insertion can be individually controlled. The insertion locations are specified as 128-bit element locations (starting at the beginning of the VUE) and the 32-bit component within those specified elements. The SGV values can be inserted either (a) within a valid vertex element (in which case the value overwrites the value specified via 3DSTATE_VERTEX_ELEMENTS) or (b) beyond the last valid vertex element written to the URB. This permits some orthogonality between the programming of vertex elements (which typically is known at draw time) and programming of SGV insertion (which is associated with the shader). There are some restrictions however (see below). If an SGV is inserted beyond the last valid vertex element, zeroes are first inserted in the VUE after the last valid vertex element up to and including the vertex element receiving an SGV. If both of the SGVs are enabled for insertion, the zeroes will extend to the last (largest index) vertex element receiving an SGV. Then the SGV(s) are inserted.</p>			
<b>Programming Notes</b>			
<p><b>Programming Restrictions:</b></p> <ul style="list-style-type: none"> <li>It is INVALID to store both the VertexID and InstanceID in the same element/component location within the VUE.</li> <li>The states programmed by this command overwrite the state programmed by any previous commands. I.e., VertexID and InstanceID (if enabled) can only be inserted in one component of a vertex.</li> <li>It is INVALID to insert an SGV value past the end of the VUE entry (as determined by VS URB Entry Allocation Size) or past the 33rd vertex element. Therefore the programming of VS URB Entry Allocation Size needs to comprehend any SGV insertion requirements.</li> <li>It is INVALID to use this command to overwrite any portion of a 64-bit vertex element component.</li> <li>It is INVALID to use this command to overwrite a EdgeFlag vertex element component or any vertex element beyond it.</li> </ul>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode

<b>3DSTATE_VF_SGVS</b>																						
	23:16	<b>3D Command Sub Opcode</b>																				
		Default Value:	4Ah 3DSTATE_VF_SGVS																			
		Format:	OpCode																			
	15:8	<b>Reserved</b>																				
		Project:	All																			
		Format:	MBZ																			
	7:0	<b>DWord Length</b>																				
		Default Value:	0h Excludes DWord (0,1)																			
		Project:	All																			
		Format:	=n Total Length - 2																			
1	31	<b>InstanceID Enable</b>																				
		Project:	All																			
		Format:	Boolean																			
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disabled</td> <td>InstanceID is not inserted</td> <td>All</td> </tr> <tr> <td>1h</td> <td>Enabled</td> <td>InstanceID is inserted</td> <td>All</td> </tr> </tbody> </table>		Value	Name	Description	Project	0h	Disabled	InstanceID is not inserted	All	1h	Enabled	InstanceID is inserted	All								
	Value	Name	Description	Project																		
	0h	Disabled	InstanceID is not inserted	All																		
	1h	Enabled	InstanceID is inserted	All																		
	30:29	<b>InstanceID Component Number</b>																				
		Project:	All																			
		<p>If InstanceID Enable is ENABLED, this field specifies the 32-bit component location (within the 4-component VUE) where it is inserted.</p> <p>If InstanceID Enable is DISABLED, this field is ignored.</p>																				
<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>COMP_0</td> <td>If enabled, InstanceID is inserted in component 0 (.x)</td> <td>All</td> </tr> <tr> <td>1</td> <td>COMP_1</td> <td>If enabled, InstanceID is inserted in component 1 (.y)</td> <td>All</td> </tr> <tr> <td>2</td> <td>COMP_2</td> <td>If enabled, InstanceID is inserted in component 2 (.z)</td> <td>All</td> </tr> <tr> <td>3</td> <td>COMP_3</td> <td>If enabled, InstanceID is inserted in component 3 (.w)</td> <td>All</td> </tr> </tbody> </table>		Value	Name	Description	Project	0	COMP_0	If enabled, InstanceID is inserted in component 0 (.x)	All	1	COMP_1	If enabled, InstanceID is inserted in component 1 (.y)	All	2	COMP_2	If enabled, InstanceID is inserted in component 2 (.z)	All	3	COMP_3	If enabled, InstanceID is inserted in component 3 (.w)	All	
Value		Name	Description	Project																		
0		COMP_0	If enabled, InstanceID is inserted in component 0 (.x)	All																		
1		COMP_1	If enabled, InstanceID is inserted in component 1 (.y)	All																		
2	COMP_2	If enabled, InstanceID is inserted in component 2 (.z)	All																			
3	COMP_3	If enabled, InstanceID is inserted in component 3 (.w)	All																			
<b>Reserved</b>																						
21:16	<b>InstanceID Element Offset</b>																					
	Project:	All																				
	Format:	U6 Offset of 128-bit element																				
	<p>If InstanceID Enable is ENABLED, this field specifies the VUE element offset of the 128-bit element where it is to be inserted. The InstanceID Component Number specifies where in the specified element it is inserted.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>[0,33]</td> <td></td> </tr> </tbody> </table>		Value	Name	[0,33]																	
Value	Name																					
[0,33]																						

<b>3DSTATE_VF_SGVS</b>				
15	<b>VertexID Enable</b>			
	Project:		All	
	Format:		Boolean	
	<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>
	0h	Disabled	VertexID is not inserted	All
	1h	Enabled	VertexID is inserted	All
	14:13	<b>VertexID Component Number</b>		
		Project:		All
		If VertexID Enable is ENABLED, this field specifies the 32-bit component location (within the 4-component VUE) where it is inserted.If VertexID Enable is DISABLED, this field is ignored.		
		<b>Value</b>	<b>Name</b>	<b>Description</b>
0		COMP_0	If enabled, VertexID is inserted in component 0 (.x)	All
1		COMP_1	If enabled, VertexID is inserted in component 1 (.y)	All
2		COMP_2	If enabled, VertexID is inserted in component 2 (.z)	All
3	COMP_3	If enabled, VertexID is inserted in component 3 (.w)	All	
12:6	<b>Reserved</b>			
	Project:		All	
	Format:		MBZ	
5:0	<b>VertexID Element Offset</b>			
	Project:		All	
	Format:		U6 Offset of 128-bit element	
	If VertexID Enable is ENABLED, this field specifies the VUE element offset of the 128-bit element where it is to be inserted. The VertexID Component Number specifies where in the specified element it is inserted. This is also the vertex element index. If VertexID Enable is DISABLED, this field is ignored.			
<b>Value</b>		<b>Name</b>		
[0,33]				

## 3DSTATE\_VF\_STATISTICS

3DSTATE_VF_STATISTICS							
Project:	CHV, BSW						
Source:	RenderCS						
Length Bias:	1						
<p>The VF stage tracks two pipeline statistics, the number of vertices fetched and the number of objects generated. VF will increment the appropriate counter for each when statistics gathering is enabled by issuing the 3DSTATE_VF_STATISTICS command with the [Statistics Enable] bit set.</p>							
DWord	Bit	Description					
0	31:29	<b>Command Type</b>					
		Default Value:	3h GFXPIPE				
		Format:	Opcode				
	28:27	<b>Command SubType</b>					
		Format:	Opcode				
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>1h</td> <td>Pipelined, Single DWord <b>[Default]</b></td> <td>CHV, BSW</td> </tr> </tbody> </table>	Value	Name	Project	1h	Pipelined, Single DWord <b>[Default]</b>
	Value	Name	Project				
	1h	Pipelined, Single DWord <b>[Default]</b>	CHV, BSW				
	26:24	<b>3D Command Opcode</b>					
		Default Value:	0h 3DSTATE_PIPELINED				
Format:		Opcode					
GFXPIPE[28:27 = 1h, 26:24 = 0h, 23:16 = 0Bh] (Pipelined, Single DWord)							
23:16	<b>3D Command Sub Opcode</b>						
	Default Value:	0Bh 3DSTATE_VF_STATISTICS					
	Format:	Opcode					
	GFXPIPE[28:27 = 1h, 26:24 = 0h, 23:16 = 0Bh] (Pipelined, Single DWord)						
15:1	<b>Reserved</b>						
	Format:	MBZ					
0	<b>Statistics Enable</b>						
	Format:	Enable					
	<p>If ENABLED, VF will increment the pipeline statistics counters IA_VERTICES_COUNT and IA_PRIMITIVES_COUNT for each vertex fetched and each object output, respectively, for 3DPRIMITIVE commands issued subsequently. If DISABLED, these counters will not be incremented for subsequent 3DPRIMITIVE commands.</p>						

## 3DSTATE\_VF\_TOPOLOGY

3DSTATE_VF_TOPOLOGY			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
This command specifies the VF stage's Topology state which can be used to override the Primitive Topology Type in subsequent 3DPRIMITIVE commands.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		4Bh 3DSTATE_VF_TOPOLOGY	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	0h Excludes DWord (0,1)	
	Project:	All	
	Format:	=n Total Length - 2	
1	31:6	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	5:0	<b>Primitive Topology Type</b>	
		Project:	All
Format:		3D_Prim_Topo_Type [CHV, BSW] This field specifies the VF stage's Topology state.	

## 3DSTATE\_VIEWPORT\_STATE\_POINTERS\_CC

3DSTATE_VIEWPORT_STATE_POINTERS_CC			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
The 3DSTATE_VIEWPORT_STATE_POINTERS_CC command is used to define the location of fixed functions' viewport state table.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
Default Value:		0h 3DSTATE_PIPELINED	
Format:		OpCode	
23:16	<b>3D Command Sub Opcode</b>		
	Default Value:	23h 3DSTATE_VIEWPORT_STATE_POINTERS	
	Format:	OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	0h DWORD_COUNT_n	
	Format:	=n	
1	31:5	<b>CC Viewport Pointer</b>	
		Project:	All
		Format:	DynamicStateOffset[31:5]CC_VIEWPORT*16
	Specifies the 32-byte aligned address offset of the CC_VIEWPORT state. This offset is relative to the Dynamic State Base Address.		
4:0	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	

## 3DSTATE\_VIEWPORT\_STATE\_POINTERS\_SF\_CLIP

3DSTATE_VIEWPORT_STATE_POINTERS_SF_CLIP			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
The 3DSTATE_VIEWPORT_STATE_POINTERS_CLIP command is used to define the location of fixed functions' viewport state table.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
Default Value:		0h 3DSTATE_PIPELINED	
Format:		OpCode	
23:16	<b>3D Command Sub Opcode</b>		
	Default Value:	21h 3DSTATE_VIEWPORT_STATE_POINTERS_SF_CLIP	
	Format:	OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	0h DWORD_COUNT_n	
	Format:	=n	
1	31:6	<b>SF Clip Viewport Pointer</b>	
		Project:	All
		Format:	DynamicStateOffset[31:6]SF_CLIP_VIEWPORT*16
	Specifies the 64-byte aligned address offset of the SF_CLIP_VIEWPORT state. This offset is relative to the Dynamic State Base Address.		
5:0	<b>Reserved</b>		
	Project:		
	Format:	MBZ	

## 3DSTATE\_VS

3DSTATE_VS			
Project:	CHV, BSW		
Source:	RenderCS, PositionCS		
Length Bias:	2		
Description		Project	
This command specifies most of the state used by the Vertex Shader (VS) stage.		CHV, BSW	
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
		Default Value:	10h 3DSTATE_VS
		Format:	OpCode
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	7h Excludes DWord (0,1)	
	Project:	All	
	Format:	=n Total Length - 2	
1..2	63:6	<b>Kernel Start Pointer</b>	
		Project:	All
		Format:	InstructionBaseOffset[63:6]Kernel
This field specifies the starting location of the kernel program run by threads spawned by the VS pipeline stage. It is specified as a 64-byte-granular offset from the Instruction Base Address. This field is ignored if VS Function Enable is DISABLED.			
	5:0	<b>Reserved</b>	



<b>3DSTATE_VS</b>																											
3	31	<b>Single Vertex Dispatch</b>																									
	Project:																										
	Format:		U1 Enumerated Type																								
<p>When this bit is set, SIMD4x2 VS threads will only process a single vertex, otherwise SIMD4x2 threads will process either one or two vertices. This field is ignored if <b>SIMD8 Dispatch Enable</b> is set.</p>																											
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 10%;">Name</th> <th style="width: 60%;">Description</th> <th style="width: 20%;">Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Multiple</td> <td>Dual vertex SIMD4x2 thread dispatches are allowed.</td> <td>All</td> </tr> <tr> <td>1h</td> <td>Single</td> <td>Single vertex SIMD4x2 thread dispatches are forced.</td> <td>All</td> </tr> </tbody> </table>				Value	Name	Description	Project	0h	Multiple	Dual vertex SIMD4x2 thread dispatches are allowed.	All	1h	Single	Single vertex SIMD4x2 thread dispatches are forced.	All												
Value	Name	Description	Project																								
0h	Multiple	Dual vertex SIMD4x2 thread dispatches are allowed.	All																								
1h	Single	Single vertex SIMD4x2 thread dispatches are forced.	All																								
	30	<b>Vector Mask Enable</b>																									
Project:		All																									
<p>Upon subsequent VS thread dispatches, this bit is loaded into the EU's <b>Vector Mask Enable</b> (VME, cr0.0[3]) thread state. Refer to EU documentation for the definition and use of VME state.</p>																											
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 10%;">Name</th> <th style="width: 60%;">Description</th> <th style="width: 20%;">Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Dmask</td> <td>The EU will use the Dispatch Mask (supplied by the VS stage) for instruction execution.</td> <td>All</td> </tr> <tr> <td>1h</td> <td>Vmask</td> <td>The EU will use the Vector Mask (derived from the Dispatch Mask) for instruction execution.</td> <td>All</td> </tr> </tbody> </table>				Value	Name	Description	Project	0h	Dmask	The EU will use the Dispatch Mask (supplied by the VS stage) for instruction execution.	All	1h	Vmask	The EU will use the Vector Mask (derived from the Dispatch Mask) for instruction execution.	All												
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<b>Programming Notes</b>																											
<p>Under normal conditions SW shall specify DMask, as the VS stage will provide a Dispatch Mask appropriate to SIMD4x2 or SIMD8 thread execution (as a function of SIMD8 Dispatch Enable). E.g., for SIMD4x2 thread execution, the VS stage will generate a Dispatch Mask that is equal to what the EU would use as the Vector Mask. For SIMD8 execution there is no known usage model for use of Vector Mask (as there is for PS shaders).</p>																											
	29:27	<b>Sampler Count</b>																									
Project:		All																									
Format:		U3																									
<p>This field specifies (in multiples of 4) the number of sets of sampler state that will be prefetched for use by the VS kernel. While the prefetching of sampler state is optional and does not impact functionality, it may improve performance.</p> <p>This field is ignored if the Function Enable state is set to DISABLED.</p>																											
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 10%;">Name</th> <th style="width: 60%;">Description</th> <th style="width: 20%;">Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>No Samplers</td> <td>no samplers used</td> <td>All</td> </tr> <tr> <td>1h</td> <td>1-4 Samplers</td> <td>between 1 and 4 samplers used</td> <td>All</td> </tr> <tr> <td>2h</td> <td>5-8 Samplers</td> <td>between 5 and 8 samplers used</td> <td>All</td> </tr> <tr> <td>3h</td> <td>9-12 Samplers</td> <td>between 9 and 12 samplers used</td> <td>All</td> </tr> <tr> <td>4h</td> <td>13-16 Samplers</td> <td>between 13 and 16 samplers used</td> <td>All</td> </tr> </tbody> </table>				Value	Name	Description	Project	0h	No Samplers	no samplers used	All	1h	1-4 Samplers	between 1 and 4 samplers used	All	2h	5-8 Samplers	between 5 and 8 samplers used	All	3h	9-12 Samplers	between 9 and 12 samplers used	All	4h	13-16 Samplers	between 13 and 16 samplers used	All
Value	Name	Description	Project																								
0h	No Samplers	no samplers used	All																								
1h	1-4 Samplers	between 1 and 4 samplers used	All																								
2h	5-8 Samplers	between 5 and 8 samplers used	All																								
3h	9-12 Samplers	between 9 and 12 samplers used	All																								
4h	13-16 Samplers	between 13 and 16 samplers used	All																								
	26	<b>Reserved</b>																									

<b>3DSTATE_VS</b>				
	Project:	All		
	Format:	MBZ		
25:18	<b>Binding Table Entry Count</b>			
	Project:	All		
	Format:	U8		
	<b>Description</b>			
	<p>Specifies how many binding table entries the kernel uses. Used only for prefetching of the binding table entries and associated surface state.</p> <p>Note: For kernels using a large number of binding table entries, it may be wise to set this field to zero to avoid prefetching too many entries and thrashing the state cache.</p> <p>This field is ignored if VS Function Enable is DISABLED.</p> <p><b>When HW Generated Binding Table bit is enabled:</b> This field indicates which cache lines (512bit units - 32 Binding Table Entry section) should be fetched. Each bit in this field corresponds to a cache line. Only the 1st 4 non-zero Binding Table entries of each 32 Binding Table entry section prefetched will have its surface state prefetched.</p>			
	<b>Value</b>		<b>Name</b>	
	[0,255]			
	<b>Programming Notes</b>			<b>Project</b>
	When HW binding table bit is set, it is assumed that the Binding Table Entry Count field will be generated at JIT time.			CHV, BSW
	17	<b>Thread Dispatch Priority</b>		
Project:		All		
Format:		U1 Enumerated Type		
Specifies the priority of the thread for dispatch: This field is ignored if VS Function Enable is DISABLED.				
<b>Value</b>		<b>Name</b>	<b>Description</b>	<b>Project</b>
0h	Normal	Normal Priority	All	
1h	High	High Priority	All	
16	<b>Floating Point Mode</b>			
	Project:	All		
	Format:	U1 Enumerated Type		
	Specifies the initial floating point mode used by the dispatched thread. This field is ignored if VS Function Enable is DISABLED.			
	<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>
0h	IEEE-754	Use IEEE-754 Rules	All	
1h	Alternate	Use Alternate Rules	All	

<b>3DSTATE_VS</b>				
	15:14	<b>Reserved</b>	Project: All	Format: MBZ
	13	<b>Illegal Opcode Exception Enable</b>	Project: All	Format: Enable
	This bit gets loaded into EU CR0.1[12] (note the bit # difference). See Exceptions and ISA Execution Environment. This field is ignored if VS Function Enable is DISABLED.			
	12	<b>Accesses UAV</b>	Format: Enable	
	This field must be set when VS has a UAV access.			
	<b>Programming Notes</b>			<b>Project</b>
	This field must not be set when VS Function Enable is disabled.			
	Workaround: If the vertex shader is the last shader to have UAV access, a PIPE_CONTROL with <b>CS_STALL</b> must be sent before the 3dprimitive using the UAV access.			CHV, BSW
	11:8	<b>Reserved</b>		
	7	<b>Software Exception Enable</b>	Project: All	Format: Enable
This bit gets loaded into EU CR0.1[13] (note the bit # difference). See Exceptions and ISA Execution Environment. This field is ignored if VS Function Enable is DISABLED.				
6:0	<b>Reserved</b>	Project: All	Format: MBZ	
4..5	63:10	<b>Scratch Space Base Pointer</b>	Project: All	Format: GeneralStateOffset[63:10]ScratchSpace
Specifies the starting location of the scratch space area allocated to this FF unit as a 1K-byte aligned offset from the General State Base Address. If required, each thread spawned by this FF unit will be allocated some portion of this space, as specified by Per-Thread Scratch Space. The computed offset of the thread-specific portion will be passed in the thread payload as Scratch Space Offset. The thread is expected to utilize "stateless" DataPort read/write requests to access scratch space, where the DataPort will cause the General State Base Address to be added to the offset passed in the request header. This field is ignored if VS Function Enable is DISABLED. In 64b OS all pointers need to be seen by SW as 48b. HW does not support a Scratch Space Base Pointer larger than 32b, therefore SW must ensure the scratch space base offset upper is set to 0's. But the DWORD must be in the command for SW to right the pointer to.				

<b>3DSTATE_VS</b>												
	9:4	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ						
	Project:	All										
	Format:	MBZ										
	3:0	<p><b>Per-Thread Scratch Space</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U4 power of 2 Bytes over 1K Bytes</td> </tr> </table> <p>Specifies the amount of scratch space to be allocated to each thread spawned by this FF unit. The driver must allocate enough contiguous scratch space, starting at the Scratch Space Base Pointer, to ensure that the Maximum Number of Threads can each get Per-Thread Scratch Space size without exceeding the driver-allocated scratch space. This field is ignored if VS Function Enable is DISABLED.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[0,11]</td> <td></td> <td>Indicating [1K Bytes, 2M Bytes]</td> </tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>This amount is available to the kernel for information only. It will be passed verbatim (if not altered by the kernel) to the Data Port in any scratch space access messages, but the Data Port will ignore it.</p>	Project:	All	Format:	U4 power of 2 Bytes over 1K Bytes	Value	Name	Description	[0,11]		Indicating [1K Bytes, 2M Bytes]
Project:	All											
Format:	U4 power of 2 Bytes over 1K Bytes											
Value	Name	Description										
[0,11]		Indicating [1K Bytes, 2M Bytes]										
6	31:25	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ								
Format:	MBZ											
	24:20	<p><b>Dispatch GRF Start Register For URB Data</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U5</td> </tr> </table> <p>Specifies the starting GRF number for the URB portion (URB constants and vertices) of the thread payload. This field is ignored if VS Function Enable is DISABLED.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[0,31]</td> <td></td> <td>indicating GRF [R0, R31]</td> </tr> </tbody> </table>	Project:	All	Format:	U5	Value	Name	Description	[0,31]		indicating GRF [R0, R31]
Project:	All											
Format:	U5											
Value	Name	Description										
[0,31]		indicating GRF [R0, R31]										
	19:17	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ						
Project:	All											
Format:	MBZ											
	16:11	<p><b>Vertex URB Entry Read Length</b></p> <table border="1"> <tr> <td>Format:</td> <td>U6</td> </tr> </table> <p>Specifies the number of pairs of 128-bit vertex elements to be passed into the payload for each vertex. This field is ignored if VS Function Enable is DISABLED. For SIMD4x2 dispatch, each vertex element requires one GRF of payload data, therefore the number of GRFs with vertex data will be double the value programmed in this field. For SIMD8 dispatch, each vertex element requires 4 GRFs of payload data, therefore the number of GRFs with vertex data will be 8 times the value programmed in this field. The EU limit of 128 GRFs imposes a maximum limit of 30 elements per vertex pushed into the payload, though the practical limit may be lower. If input vertices exceed</p>	Format:	U6								
Format:	U6											

<b>3DSTATE_VS</b>																			
		<p>the practical limit, software must decide between resorting to pulling elements during thread execution or dropping back to SIMD4x2 dispatch. Note that the VUE is used for both input and output, so when using the pull-model software must ensure inputs are not overwritten before last use.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[1,63]</td> <td></td> <td>if SIMD8 dispatch disabled</td> </tr> <tr> <td>[0,15]</td> <td></td> <td>if SIMD8 dispatch enabled</td> </tr> </tbody> </table>		Value	Name	Description	[1,63]		if SIMD8 dispatch disabled	[0,15]		if SIMD8 dispatch enabled							
Value	Name	Description																	
[1,63]		if SIMD8 dispatch disabled																	
[0,15]		if SIMD8 dispatch enabled																	
	10	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>		Project:	All	Format:	MBZ												
Project:	All																		
Format:	MBZ																		
	9:4	<p><b>Vertex URB Entry Read Offset</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U6</td> </tr> </table> <p>Specifies the offset (in 256-bit units) at which Vertex URB data is to be read from the URB before being included in the thread payload. This offset applies to all Vertex URB entries passed to the thread. This field is ignored if VS Function Enable is DISABLED.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>[0,63]</td> <td></td> </tr> </tbody> </table>		Project:	All	Format:	U6	Value	Name	[0,63]									
Project:	All																		
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	3:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>		Project:	All	Format:	MBZ												
Project:	All																		
Format:	MBZ																		
7	31:23	<p><b>Maximum Number of Threads</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U9-1 Thread count</td> </tr> </table> <p>Specifies the maximum number of simultaneous threads allowed to be active. Used to avoid using up the scratch space. Programming the value of the max threads over the number of threads based off number of threads supported in the execution units may improve performance since the architecture allows threads to be buffered between the check for max threads and the actual dispatch into the EU. Programming the max values to a number less than the number of threads supported in the execution units may reduce performance. This field is ignored if VS Function Enable is DISABLED.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>[0,503]</td> <td></td> <td>indicating thread count of [1,504]</td> <td>CHV, BSW</td> </tr> <tr> <td>[0,79]</td> <td></td> <td>indicating thread count of [1,80]</td> <td>CHV, BSW</td> </tr> </tbody> </table>		Project:	CHV, BSW	Format:	U9-1 Thread count	Value	Name	Description	Project	[0,503]		indicating thread count of [1,504]	CHV, BSW	[0,79]		indicating thread count of [1,80]	CHV, BSW
Project:	CHV, BSW																		
Format:	U9-1 Thread count																		
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[0,503]		indicating thread count of [1,504]	CHV, BSW																
[0,79]		indicating thread count of [1,80]	CHV, BSW																
	22	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>		Project:	CHV, BSW	Format:	MBZ												
Project:	CHV, BSW																		
Format:	MBZ																		
	21:11	<p><b>Reserved</b></p>																	

<b>3DSTATE_VS</b>						
10	<p><b>Statistics Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>If ENABLED, the VS stage will perform statistics gathering. See the Statistics Gathering subsection. If DISABLED, statistics information associated with the VS stage will be left unchanged.</p>	Project:	All	Format:	Enable	
Project:	All					
Format:	Enable					
9	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ	
Project:	CHV, BSW					
Format:	MBZ					
8:3	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ	
Project:	All					
Format:	MBZ					
2	<p><b>SIMD8 Dispatch Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field determines how VS threads are dispatched and how the thread payloads are generated. The setting of this field must agree with how the VS kernel was compiled. If ENABLED, SIMD8 VS thread dispatches are performed. The <b>Single Vertex Dispatch</b> field is ignored. If DISABLED, SIMD4x2 thread dispatches are performed. The <b>Single Vertex Dispatch</b> field can be used to force single-vertex dispatches.</p>	Project:	All	Format:	Enable	
Project:	All					
Format:	Enable					
1	<p><b>Vertex Cache Disable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Disable</td> </tr> </table> <p>This bit controls the operation of the Vertex Cache. This field is always used. If the Vertex Cache is DISABLED and the VS Function is ENABLED, the Vertex Cache is not used and all incoming vertices will be passed to VS threads. If the Vertex Cache is ENABLED and the VS Function is ENABLED, only incoming vertices that do not hit in the Vertex Cache will be passed to VS threads. If the Vertex Cache is ENABLED and the VS Function is DISABLED, input vertices that miss in the Vertex Cache will be assembled and written to the URB (by the VF stage), and subsequently passed through the VS stage unmodified (i.e, no VS threads are spawned). The Vertex Cache is invalidated whenever the Vertex Cache becomes DISABLED, whenever the VS Function Enable toggles, between 3DPRIMITIVE commands and between instances within a 3DPRIMITIVE command.</p> <table border="1" style="width: 100%; background-color: #e6f2ff;"> <tr> <td style="text-align: center;"><b>Programming Notes</b></td> </tr> </table> <p>See the Vertex Caching subsection for details on implicit Vertex Cache disabling.</p>	Project:	All	Format:	Disable	<b>Programming Notes</b>
Project:	All					
Format:	Disable					
<b>Programming Notes</b>						

<b>3DSTATE_VS</b>																									
0	<p><b>Function Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This bit determines whether or not the VS stage spawns VS threads, which comprises the bulk of the VS stage functionality.                      If ENABLED, VS threads may be spawned to process VF-generated vertices before the resulting vertices are passed down the pipeline.                      If DISABLED, VF-generated vertices will pass thru the VS function and are sent down the pipeline unmodified. The Vertex Cache (if enabled) is still available.</p>	Format:	Enable																						
Format:	Enable																								
8	<p>31:28 <b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>27 <b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td></td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>26:21 <b>Vertex URB Entry Output Read Offset</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U6</td> </tr> </table> <p>Specifies the offset (in 256-bit units) at which Vertex URB data is to be read from the URB by the Setup Back-End (SBE) function. The offset programmed will specify the start of Attribute 0 to be passed in subsequent Pixel Shader thread payloads. Refer to the Attribute Interpolator Setup documentation.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>[0,63]</td> <td></td> </tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>As the vertex header data located at the start of the Vertex URB entry is typically only used by 3D pipeline FFs (i.e., Clipper, Setup FrontEnd) and not required as interpolated attributes in Pixel Shader threads, it is expected that SW will program this Start Offset skip over the vertex header.                      This offset value is ignored if SBE's Number of SF Attributes state is programmed to 0 (i.e., no attributes are defined beyond the position read from the Vertex Header)</p> <p>20:16 <b>Vertex URB Entry Output Length</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U5</td> </tr> </table> <p>Specifies the amount of Vertex Attribute URB data to be read by the Setup Back-End function for each Vertex URB entry, in 256-bit units. The attribute data will be read starting at the offset specified by the Vertex URB Entry Output Read Offset state.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>[1,16]</td> <td></td> </tr> </tbody> </table>	Project:	All	Format:	MBZ	Project:		Format:	MBZ	Project:	All	Format:	U6	Value	Name	[0,63]		Project:	All	Format:	U5	Value	Name	[1,16]	
Project:	All																								
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Project:	All																								
Format:	U5																								
Value	Name																								
[1,16]																									

<b>3DSTATE_VS</b>					
	<table border="1"> <tr> <th colspan="2" style="text-align: center;">Programming Notes</th> </tr> <tr> <td colspan="2">This length value is ignored if SBE's Number of SF Attributes state is programmed to 0 (i.e., no attributes are defined beyond the position read from the Vertex Header).</td> </tr> </table>	Programming Notes		This length value is ignored if SBE's Number of SF Attributes state is programmed to 0 (i.e., no attributes are defined beyond the position read from the Vertex Header).	
Programming Notes					
This length value is ignored if SBE's Number of SF Attributes state is programmed to 0 (i.e., no attributes are defined beyond the position read from the Vertex Header).					
15:8	<p><b>User Clip Distance Clip Test Enable Bitmask</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>mask[8]</td> </tr> </table> <p>This 8 bit mask field selects which of the 8 Clip Distance Values (if any) are to be included in the Clip stage's trivial reject / trivial accept / must clip determination function. The ClipDistance Values (if present) are located in DW8-15 of the VUE Vertex Header located at the beginning of VUE URB entries. Bit 0 of this field corresponds to Clip Distance Value 0.</p>	Project:	All	Format:	mask[8]
Project:	All				
Format:	mask[8]				
7:0	<p><b>User Clip Distance Cull Test Enable Bitmask</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>mask[8]</td> </tr> </table> <p>This 8 bit mask field selects which of the 8 Clip Distance Values (if any) are to be included in the Clip stage's trivial reject / trivial accept determination function. Note that must clip determination is not included in this function. The ClipDistance Values (if present) are located in DW8-15 of the VUE Vertex Header located at the beginning of VUE URB entries. Bit 0 of this field corresponds to Clip Distance Value 0.</p>	Project:	All	Format:	mask[8]
Project:	All				
Format:	mask[8]				



## 3DSTATE\_WM\_CHROMAKEY

<b>3DSTATE_WM_CHROMAKEY</b>			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		4Ch 3DSTATE_WM_CHROMAKEY	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>Dword Length</b>	Default Value:	0h Excludes Dword (0,1)
		Project:	All
		Format:	=n
		Total Length - 2	
1	31	<b>ChromaKey Kill Enable</b>	
		Project:	All
		Format:	Enable
	If ENABLED, indicates that at least one of the attached samplers has ChromaKeyKill enabled.		
	30:0	<b>Reserved</b>	
Project:		All	
Format:		MBZ	

## 3DSTATE\_WM\_DEPTH\_STENCIL

3DSTATE_WM_DEPTH_STENCIL			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
This command replaces the indirect state DEPTH_STENCIL_STATE with an inline state command.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		4Eh 3DSTATE_WM_DEPTH_STENCIL	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>Dword Length</b>	Project:	All
		Format:	=n
		Total Length - 2	
	<b>Value</b>	<b>Name</b>	<b>Project</b>
	01h	Excludes Dword (0,1) <b>[Default]</b>	CHV, BSW
1	31:29	<b>Stencil Fail Op</b>	
		Project:	All
		Format:	3D_Stencil_Operation [CHV, BSW]
	This field specifies the operation to perform on the Stencil Buffer when the (front face) stencil test fails.		
	<b>Programming Notes</b>		
if all three stencil ops (Stencil Fail, Stencil Pass Depth Fail, and Stencil Pass Depth Pass) are KEEP, ZERO, or REPLACE, the stencil buffer is not read.			

<b>3DSTATE_WM_DEPTH_STENCIL</b>				
28:26	<b>Stencil Pass Depth Fail Op</b>			
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>3D_Stencil_Operation [CHV, BSW]</td> </tr> </table> <p>This field specifies the operation to perform on the Stencil Buffer when the (front face) stencil test passes but the depth pass fails.</p>	Project:	All	Format:
Project:	All			
Format:	3D_Stencil_Operation [CHV, BSW]			
25:23	<b>Stencil Pass Depth Pass Op</b>			
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>3D_Stencil_Operation [CHV, BSW]</td> </tr> </table> <p>This field specifies the operation to perform on the Stencil Buffer when the (front face) stencil test passes but the depth test passes.</p>	Project:	All	Format:
Project:	All			
Format:	3D_Stencil_Operation [CHV, BSW]			
22:20	<b>Backface Stencil Test Function</b>			
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>3D_Compare_Function</td> </tr> </table>	Project:	All	Format:
Project:	All			
Format:	3D_Compare_Function			
19:17	<b>Backface Stencil Fail Op</b>			
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>3D_Stencil_Operation [CHV, BSW]</td> </tr> </table>	Project:	All	Format:
Project:	All			
Format:	3D_Stencil_Operation [CHV, BSW]			
16:14	<b>Backface Stencil Pass Depth Fail Op</b>			
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>3D_Stencil_Operation [CHV, BSW]</td> </tr> </table> <p>This field specifies the operation to perform on the Stencil Buffer when the stencil test passes but the depth pass fails.</p>	Project:	All	Format:
Project:	All			
Format:	3D_Stencil_Operation [CHV, BSW]			
13:11	<b>Backface Stencil Pass Depth Pass Op</b>			
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>3D_Stencil_Operation [CHV, BSW]</td> </tr> </table> <p>This field specifies the operation to perform on the Stencil Buffer when the stencil test passes and the depth pass passes (or is disabled).</p>	Project:	All	Format:
Project:	All			
Format:	3D_Stencil_Operation [CHV, BSW]			
10:8	<b>Stencil Test Function</b>			
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>3D_Compare_Function</td> </tr> </table> <p>This field specifies the comparison function used in the (front face) StencilTest function.</p>	Project:	All	Format:
Project:	All			
Format:	3D_Compare_Function			
7:5	<b>Depth Test Function</b>			
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>3D_Compare_Function</td> </tr> </table> <p>Specifies the comparison function used in DepthTest function.</p>	Project:	All	Format:
Project:	All			
Format:	3D_Compare_Function			

<b>3DSTATE_WM_DEPTH_STENCIL</b>				
<b>Programming Notes</b>				
If the Depth Test Function is ALWAYS or NEVER, the depth buffer is not read.				
<b>4</b>	<b>Double Sided Stencil Enable</b>			
	Project:	All		
	Format:	Enable		
	Enable doubled sided stencil operations.			
	<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>
	0h	False	Double Sided Stencil Disabled	All
	1h	True	Double Sided Stencil Enabled	All
	<b>Programming Notes</b>			
	<ul style="list-style-type: none"> <li>• Back-facing primitives have a vertex winding order opposite to the currently selected Front Winding state.</li> <li>• Culling of primitives is not affected by the double sided stencil state</li> <li>• Back-facing primitives will be rendered, honoring all current device state, as though it were a front-facing primitive with no implicitly overloaded state.</li> </ul>			
	<b>3</b>	<b>Stencil Test Enable</b>		
Project:		All		
Format:		Enable		
Enables StencilTest function of the Pixel Processing pipeline.				
<b>Programming Notes</b>				
If any of the render targets are YUV format, this field must be disabled.				
<b>2</b>	<b>Stencil Buffer Write Enable</b>			
	Project:	All		
	Format:	Enable		
	Enables writes to the Stencil Buffer.			
	<b>Programming Notes</b>			
	If this field is enabled, Stencil Test Enable must also be enabled.			
<b>1</b>	<b>Depth Test Enable</b>			
	Project:	All		
	Format:	Enable		
	Enables the DepthTest function of the Pixel Processing pipeline.			
	<b>Value</b>	<b>Name</b>	<b>Project</b>	
	0h	Disable	All	
	1h	Enable	All	
<b>Programming Notes</b>				

<b>3DSTATE_WM_DEPTH_STENCIL</b>																	
	<p>If any of the render targets are YUV format, this field must be disabled.</p>																
0	<p><b>Depth Buffer Write Enable</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>Enables writes to the Depth Buffer.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Programming Notes</th> <th style="text-align: center;">Project</th> </tr> </thead> <tbody> <tr> <td>A Depth Buffer must be defined before enabling writes to it, or operation is UNDEFINED.</td> <td></td> </tr> <tr> <td>This bit must not be set when WM_INT::RT Independent Rasterization Enable is true.</td> <td>CHV, BSW</td> </tr> </tbody> </table> <table border="1"> <thead> <tr> <th style="text-align: center;">Workaround</th> <th style="text-align: center;">Project</th> </tr> </thead> <tbody> <tr> <td>If Depth_Test_Enable = 1 AND Depth_Test_func = EQUAL, the Depth_Write_Enable must be set to 0</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Project:	All	Format:	Enable	Programming Notes	Project	A Depth Buffer must be defined before enabling writes to it, or operation is UNDEFINED.		This bit must not be set when WM_INT::RT Independent Rasterization Enable is true.	CHV, BSW	Workaround	Project	If Depth_Test_Enable = 1 AND Depth_Test_func = EQUAL, the Depth_Write_Enable must be set to 0	CHV, BSW		
Project:	All																
Format:	Enable																
Programming Notes	Project																
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Workaround	Project																
If Depth_Test_Enable = 1 AND Depth_Test_func = EQUAL, the Depth_Write_Enable must be set to 0	CHV, BSW																
2	<p>31:24 <b>Stencil Test Mask</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This field specifies a bit mask applied to stencil test values. Both the stencil reference value and value read from the stencil buffer will be logically ANDed with this mask before the stencil comparison test is performed.</p> <p>23:16 <b>Stencil Write Mask</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This field specifies a bit mask applied to stencil buffer writes. Only those stencil buffer bits corresponding to bits set in this mask will be modified.</p> <p>15:8 <b>Backface Stencil Test Mask</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This field specifies a bit mask applied to backface stencil test values. Both the stencil reference value and value read from the stencil buffer will be logically ANDed with this mask before the stencil comparison test is performed.</p> <p>7:0 <b>Backface Stencil Write Mask</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This field specifies a bit mask applied to backface stencil buffer writes. Only those stencil buffer bits corresponding to bits set in this mask will be modified.</p>	Project:	All	Format:	U8	Project:	All	Format:	U8	Project:	All	Format:	U8	Project:	All	Format:	U8
Project:	All																
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## 3DSTATE\_WM

3DSTATE_WM			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		14h 3DSTATE_WM	
Format:		OpCode	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	0h Excludes DWord (0,1)	
	Project:	All	
	Format:	=n	
	Total Length - 2		
1	31	<b>Statistics Enable</b>	
		Project:	All
		Format:	Enable
	<p>If ENABLED, the Windower and pixel pipeline will engage in statistics gathering. If DISABLED, statistics information associated with this FF stage will be left unchanged. See Statistics Gathering.</p>		
	<p style="text-align: center;"><b>Programming Notes</b></p> <p>This bit must be disabled if any of these bits is set: 3DSTATE_WM::<b>Legacy Depth Buffer Clear</b>, 3DSTATE_WM::<b>Legacy Hierarchical Depth Buffer Resolve Enable</b> or 3DSTATE_WM::<b>Legacy Depth Buffer Resolve Enable</b>.</p>		

<b>3DSTATE_WM</b>					
30	<p><b>Legacy Depth Buffer Clear Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>When set, the depth buffer is initialized as a side-effect of rendering pixels.</p> <p style="text-align: center;"><b>Programming Notes</b></p> <p>If this field is enabled,</p> <ol style="list-style-type: none"> <li>1. the <b>Depth Test Enable</b> field in DEPTH_STENCIL_STATE must be disabled.</li> <li>2. 3DSTATE_DEPTH_BUFFER::Depth Write Enable must be set.</li> <li>3. 3DSTATE_DEPTH_BUFFER::Stencil Write Enable must be set if 3DSTATE_STENCIL_BUFFER::Stencil buffer enable is set. Additionally the following must be set to the correct values.                             <ol style="list-style-type: none"> <li>1. DEPTH_STENCIL_STATE::Stencil Write Mask must be 0xFF</li> <li>2. DEPTH_STENCIL_STATE::Stencil Test Mask must be 0xFF</li> <li>3. DEPTH_STENCIL_STATE::Back Face Stencil Write Mask must be 0xFF</li> <li>4. DEPTH_STENCIL_STATE::Back Face Stencil Test Mask must be 0xFF</li> </ol> </li> </ol> <p>Refer to section 0 "Depth Buffer Clear" for additional restrictions when this field is enabled. If this field is enabled, <b>Pixel Shader Kill Pixel</b> must be disabled.</p>	Project:	All	Format:	Enable
Project:	All				
Format:	Enable				
29	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ
Project:	All				
Format:	MBZ				
28	<p><b>Legacy Depth Buffer Resolve Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>When set, the depth buffer is made to be consistent with the hierarchical depth buffer as a side-effect of rendering pixels. This is intended to be used when the depth buffer is to be used as a surface outside of the 3D rendering operation.</p> <p style="text-align: center;"><b>Programming Notes</b></p> <p>If this field is enabled,</p> <ol style="list-style-type: none"> <li>1. the <b>Legacy Depth Buffer Clear</b> and <b>Legacy Hierarchical Depth Buffer Resolve Enable</b> fields must both be disabled.</li> <li>2. 3DSTATE_DEPTH_BUFFER::Depth Write Enable must be set.</li> </ol> <p>Refer to section 11.5.4.2 "Depth Buffer Resolve" for additional restrictions when this field is enabled. <b>If Hierarchical Depth Buffer Enable</b> is disabled, enabling this field will have no effect.</p>	Project:	All	Format:	Enable
Project:	All				
Format:	Enable				
27	<p><b>Legacy Hierarchical Depth Buffer Resolve Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>When set, the hierarchical depth buffer is made to be consistent with the depth buffer as a side-effect of rendering pixels. This is intended to be used when the depth buffer has been modified</p>	Project:	All	Format:	Enable
Project:	All				
Format:	Enable				

### 3DSTATE\_WM

	outside of the 3D rendering operation.			
	<b>Programming Notes</b>			
	<p>If this field is enabled,</p> <ol style="list-style-type: none"> <li>1. the <b>Legacy Depth Buffer Clear</b> and <b>Legacy Depth Buffer Resolve Enable</b> fields must both be disabled.</li> <li>2. 3DSTATE_DEPTH_BUFFER::Depth Write Enable must be set.</li> </ol> <p>Refer to section 11.5.4.3 "Hierarchical Depth Buffer Resolve" for additional restrictions when this field is enabled. If <b>Hierarchical Depth Buffer Enable</b> is disabled, enabling this field will have no effect. <b>Performance Note:</b> expect the hierarchical depth buffer's impact on performance to be reduced for some period of time after this operation is performed, as the hierarchical depth buffer is initialized to a state that makes it ineffective. Further rendering will tend to bring the hierarchical depth buffer back to a more effective state.</p>			
26	<b>Legacy Diamond Line Rasterization</b>			
	Project:	All		
	Format:	Enable		
	<p>This bit, if ENABLED, indicates that the Windower will rasterize zero width lines using the DX9 rasterization rules. If DISABLED, the Windower will rasterize zero width lines using the DX10 rasterization rules (see Strips Fans chapter).</p>			
25:23	<b>Reserved</b>			
	Project:	All		
	Format:	MBZ		
22:21	<b>Early Depth/Stencil Control</b>			
	Project:	CHV, BSW		
	Format:	U2 Enumerated Type		
	<p>This field specifies the behavior of early depth/stencil test.</p>			
	<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>
	0h	NORMAL	Depth/Stencil Test/Write behaves as if it happens post-shader, however the pixel shader is not necessarily executed if the pixel fails depth or stencil test (this is the legacy behavior)	All
	1h	PSEXEC	Depth/Stencil Test/Write behaves as if it happens post-shader, and the pixel shader is executed if the pixel fails depth or stencil test (although pre-shader actions such as primitive inclusion, stipple, etc. will still cause the shader not to execute)	All
	2h	PREPS	Depth/Stencil Test/Write behaves as if it happens pre-shader. The pixel shader is not executed if the pixel fails depth or stencil test. Depth and stencil writes occur even if the pixel is killed by the shader or post-shader by alpha test, etc. Depth output by the pixel shader is ignored.	All
	3h	Reserved		All



<b>3DSTATE_WM</b>																									
<b>Programming Notes</b>																									
The Early Depth/Stencil Control field cannot be set to PREPS (value = 2h) if ForceKillpix = ForceON or Forced Thread Dispatch = ForceON																									
20:19	<b>Reserved</b>																								
18:17	<p><b>Position ZW Interpolation Mode</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U2 Enumerated Type</td> </tr> </table> <p>This field elects "interpolation mode" associated with the Position Z (source depth) and W coordinates passed in the PS payload when the PS requires Position as input. This field does not determine whether these coordinates are actually included in the payload (see Pixel Shader Requires Depth, Pixel Shader Requires W).</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>INTERP_PIXEL</td> <td>Evaluate Z &amp; W at the pixel center or UL corner (as specified by Pixel Location of 3DSTATE_MULTISAMPLE)</td> <td>All</td> </tr> <tr> <td>1h</td> <td>Reserved</td> <td></td> <td>All</td> </tr> <tr> <td>2h</td> <td>INTERP_CENTROID</td> <td></td> <td>All</td> </tr> <tr> <td>3h</td> <td>INTERP_SAMPLE</td> <td></td> <td>All</td> </tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>WM_INT::RT Independent Rasterization Enable must be disabled in order to select INTERP_SAMPLE.</p> <p>MSDISPMODE_PERSAMPLE is required in order to select INTERP_SAMPLE.</p>	Project:	All	Format:	U2 Enumerated Type	Value	Name	Description	Project	0h	INTERP_PIXEL	Evaluate Z & W at the pixel center or UL corner (as specified by Pixel Location of 3DSTATE_MULTISAMPLE)	All	1h	Reserved		All	2h	INTERP_CENTROID		All	3h	INTERP_SAMPLE		All
Project:	All																								
Format:	U2 Enumerated Type																								
Value	Name	Description	Project																						
0h	INTERP_PIXEL	Evaluate Z & W at the pixel center or UL corner (as specified by Pixel Location of 3DSTATE_MULTISAMPLE)	All																						
1h	Reserved		All																						
2h	INTERP_CENTROID		All																						
3h	INTERP_SAMPLE		All																						
16:11	<p><b>Barycentric Interpolation Mode</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable[6]</td> </tr> </table> <p>Controls which barycentric interpolation terms must be passed into the pixel shader kernel. Bit 0: Perspective Pixel Location barycentric is required Bit 1: Perspective Centroid barycentric is required Bit 2: Perspective Sample barycentric is required Bit 3: Non-perspective Pixel Location barycentric is required Bit 4: Non-perspective Centroid barycentric is required Bit 5: Non-perspective Sample barycentric is required</p> <p style="text-align: center;"><b>Programming Notes</b></p> <p>If contiguous dispatch modes are enabled, only bit 3 (non-perspective pixel location) can be set, all other bits in this field must be zero. Pixel Location below refers to either the upper left corner or pixel center depending on the <b>Pixel Location</b> state of 3DSTATE_MULTISAMPLING). MSDISPMODE_PERSAMPLE is required in order to select Perspective Sample or Non-perspective Sample barycentric coordinates.</p>	Project:	All	Format:	Enable[6]																				
Project:	All																								
Format:	Enable[6]																								
10	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ																				
Project:	All																								
Format:	MBZ																								

<b>3DSTATE_WM</b>				
9:8	<b>Line End Cap Antialiasing Region Width</b>			
	Project:	All		
	Format:	U2		
	This field specifies the distances over which the coverage of anti-aliased line end caps are computed.			
	<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>
	0h	0.5 pixels	0.5 pixels	All
	1h	1.0 pixels	1.0 pixels	All
	2h	2.0 pixels	2.0 pixels	All
	3h	4.0 pixels	4.0 pixels	All
	7:6	<b>Line Antialiasing Region Width</b>		
Project:		All		
Format:		U2		
This field specifies the distance over which the anti-aliased line coverage is computed.				
<b>Value</b>		<b>Name</b>	<b>Description</b>	<b>Project</b>
0h		0.5 pixels	0.5 pixels	All
1h		1.0 pixels	1.0 pixels	All
2h		2.0 pixels	2.0 pixels	All
3h		4.0 pixels	4.0 pixels	All
5		<b>Reserved</b>		
	Project:	All		
	Format:	MBZ		
4	<b>Polygon Stipple Enable</b>			
	Project:	All		
	Format:	Enable		
Enables the Polygon Stipple function.				
3	<b>Line Stipple Enable</b>			
	Project:	All		
	Format:	Enable		
Enables the Line Stipple function.				
2	<b>Point Rasterization Rule</b>			
	Project:	All		
	Format:	3D_RasterizationRule		
	This field specifies the rasterization rules to be applied whenever the edges of a point primitive fall exactly on a pixel sampling point.			
<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>	

3DSTATE_WM				
	0h	RASTRULE_UPPER_LEFT	To match "normal" upper left rules for surface primitives	All
	1h	RASTRULE_UPPER_RIGHT	To match OpenGL point rasterization rules (round to + infinity, where this is the upper right direction wrt OpenGL screen origin of lower left).	All
	1:0	<b>Reserved</b>		

## 3DSTATE\_WM\_HZ\_OP

<b>3DSTATE_WM_HZ_OP</b>			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
This command provides for clearing Z and/or stencil or resolving either HZ buffer or Z buffer.			
<b>Programming Notes</b>			
3DSTATE_MULTISAMPLE packet must be used prior to this packet to change the Number of Multisamples. This packet must not be used to change Number of Multisamples in a rendering sequence.			
3DSTATE_RASTER if used must be programmed prior to using this packet.			
This command does support predication from the use of the MI_PREDICATE register. To predicate depth clears and resolves on [CHV, BSW] you must fall back to using the 3D_PRIMITIVE or GPGPU_WALKER commands.			
As this command generates an implicit rectangle, SW must make sure any MMIO register writes following WM_HZ_OP must be preceded by <b>PIPE_CONTROL</b> with <b>Command Streamer Stall Enable</b> bit set.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
		Default Value:	52h 3DSTATE_WM_HZ_OP
		Format:	OpCode
	15:8	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
7:0	<b>Dword Length</b>		
	Default Value:	03h Excludes Dword (0,1)	
	Project:	All	
	Format:	=n	

<b>3DSTATE_WM_HZ_OP</b>										
		Total Length - 2								
1	31	<p><b>Stencil Buffer Clear Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>When set, the stencil buffer is initialized.</p> <table border="1" style="width: 100%; background-color: #e6f2ff;"> <tr> <th style="text-align: center;">Programming Notes</th> </tr> </table> <p>If this field is enabled,</p> <ol style="list-style-type: none"> <li>the <b>Depth Buffer Resolve Enable</b> and <b>Hierarchical Depth Buffer Resolve Enable</b> fields must both be disabled.</li> <li>3DSTATE_DEPTH_BUFFER::Stencil Write Enable must be set if 3DSTATE_STENCIL_BUFFER::Stencil buffer enable is set.</li> </ol>	Project:	All	Format:	Enable	Programming Notes			
	Project:	All								
	Format:	Enable								
	Programming Notes									
30	<p><b>Depth Buffer Clear Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>When set, the depth buffer is initialized.</p> <table border="1" style="width: 100%; background-color: #e6f2ff;"> <tr> <th style="text-align: center;">Programming Notes</th> </tr> </table> <p>If this field is enabled,</p> <ol style="list-style-type: none"> <li>the <b>Depth Buffer Resolve Enable</b> and <b>Hierarchical Depth Buffer Resolve Enable</b> fields must both be disabled.</li> <li>3DSTATE_DEPTH_BUFFER::Depth Write Enable must be set.</li> </ol>	Project:	All	Format:	Enable	Programming Notes				
Project:	All									
Format:	Enable									
Programming Notes										
29	<p><b>Scissor Rectangle Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>Enables operation of Scissor Rectangle.</p> <table border="1" style="width: 100%; background-color: #e6f2ff;"> <tr> <th style="text-align: center;">Programming Notes</th> </tr> </table> <p>In order get the functionality right if this bit is disabled, driver must clip the clear rectangle to scissor rectangle if scissor test is enabled before clearing.</p> <table border="1" style="width: 100%; background-color: #e6f2ff;"> <tr> <th style="text-align: center;">Workaround</th> <th style="text-align: center;">Project</th> </tr> </table> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Workaround: Due to a Hardware issue this bit must not be set.</td> <td>CHV, BSW</td> </tr> </table>	Project:	All	Format:	Enable	Programming Notes	Workaround	Project	Workaround: Due to a Hardware issue this bit must not be set.	CHV, BSW
Project:	All									
Format:	Enable									
Programming Notes										
Workaround	Project									
Workaround: Due to a Hardware issue this bit must not be set.	CHV, BSW									
28	<p><b>Depth Buffer Resolve Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>When set, the depth buffer is made to be consistent with the hierarchical depth buffer as a side-effect of rendering pixels. This is</p>	Project:	All	Format:	Enable					
Project:	All									
Format:	Enable									

<b>3DSTATE_WM_HZ_OP</b>									
	<p>intended to be used when the depth buffer is to be used as a surface outside of the 3D rendering operation.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th colspan="2" style="text-align: center;"><b>Programming Notes</b></th> </tr> </thead> <tbody> <tr> <td colspan="2"> <p>If this field is enabled,</p> <ol style="list-style-type: none"> <li>the <b>Depth Buffer Clear</b> and <b>Hierarchical Depth Buffer Resolve Enable</b> fields must both be disabled.</li> <li>3DSTATE_DEPTH_BUFFER::Depth Write Enable must be set.</li> </ol> <p>Refer to section 11.5.4.2 "Depth Buffer Resolve" for additional restrictions when this field is enabled. If <b>Hierarchical Depth Buffer Enable</b> is disabled, enabling this field will have no effect.</p> </td> </tr> </tbody> </table>	<b>Programming Notes</b>		<p>If this field is enabled,</p> <ol style="list-style-type: none"> <li>the <b>Depth Buffer Clear</b> and <b>Hierarchical Depth Buffer Resolve Enable</b> fields must both be disabled.</li> <li>3DSTATE_DEPTH_BUFFER::Depth Write Enable must be set.</li> </ol> <p>Refer to section 11.5.4.2 "Depth Buffer Resolve" for additional restrictions when this field is enabled. If <b>Hierarchical Depth Buffer Enable</b> is disabled, enabling this field will have no effect.</p>					
<b>Programming Notes</b>									
<p>If this field is enabled,</p> <ol style="list-style-type: none"> <li>the <b>Depth Buffer Clear</b> and <b>Hierarchical Depth Buffer Resolve Enable</b> fields must both be disabled.</li> <li>3DSTATE_DEPTH_BUFFER::Depth Write Enable must be set.</li> </ol> <p>Refer to section 11.5.4.2 "Depth Buffer Resolve" for additional restrictions when this field is enabled. If <b>Hierarchical Depth Buffer Enable</b> is disabled, enabling this field will have no effect.</p>									
27	<p><b>Hierarchical Depth Buffer Resolve Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>When set, the hierarchical depth buffer is made to be consistent with the depth buffer as a side-effect of rendering pixels. This is intended to be used when the depth buffer has been modified outside of the 3D rendering operation.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th colspan="2" style="text-align: center;"><b>Programming Notes</b></th> </tr> </thead> <tbody> <tr> <td colspan="2"> <p>If this field is enabled,</p> <ol style="list-style-type: none"> <li>the <b>Depth Buffer Clear</b> and <b>Depth Buffer Resolve Enable</b> fields must both be disabled.</li> <li>3DSTATE_DEPTH_BUFFER::Depth Write Enable must be set.</li> </ol> <p>Refer to section 11.5.4.3 "Hierarchical Depth Buffer Resolve" for additional restrictions when this field is enabled. If <b>Hierarchical Depth Buffer Enable</b> is disabled, enabling this field will have no effect. <b>Performance Note:</b> expect the hierarchical depth buffer's impact on performance to be reduced for some period of time after this operation is performed, as the hierarchical depth buffer is initialized to a state that makes it ineffective. Further rendering will tend to bring the hierarchical depth buffer back to a more effective state.</p> </td> </tr> </tbody> </table>	Project:	All	Format:	Enable	<b>Programming Notes</b>		<p>If this field is enabled,</p> <ol style="list-style-type: none"> <li>the <b>Depth Buffer Clear</b> and <b>Depth Buffer Resolve Enable</b> fields must both be disabled.</li> <li>3DSTATE_DEPTH_BUFFER::Depth Write Enable must be set.</li> </ol> <p>Refer to section 11.5.4.3 "Hierarchical Depth Buffer Resolve" for additional restrictions when this field is enabled. If <b>Hierarchical Depth Buffer Enable</b> is disabled, enabling this field will have no effect. <b>Performance Note:</b> expect the hierarchical depth buffer's impact on performance to be reduced for some period of time after this operation is performed, as the hierarchical depth buffer is initialized to a state that makes it ineffective. Further rendering will tend to bring the hierarchical depth buffer back to a more effective state.</p>	
Project:	All								
Format:	Enable								
<b>Programming Notes</b>									
<p>If this field is enabled,</p> <ol style="list-style-type: none"> <li>the <b>Depth Buffer Clear</b> and <b>Depth Buffer Resolve Enable</b> fields must both be disabled.</li> <li>3DSTATE_DEPTH_BUFFER::Depth Write Enable must be set.</li> </ol> <p>Refer to section 11.5.4.3 "Hierarchical Depth Buffer Resolve" for additional restrictions when this field is enabled. If <b>Hierarchical Depth Buffer Enable</b> is disabled, enabling this field will have no effect. <b>Performance Note:</b> expect the hierarchical depth buffer's impact on performance to be reduced for some period of time after this operation is performed, as the hierarchical depth buffer is initialized to a state that makes it ineffective. Further rendering will tend to bring the hierarchical depth buffer back to a more effective state.</p>									
26	<p><b>Pixel Position Offset Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U1 Enumerated Type</td> </tr> </table> <p>Enables the device to offset pixel positions by 0.5 both in horizontal and vertical directions.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th colspan="2" style="text-align: center;"><b>Programming Notes</b></th> </tr> </thead> <tbody> <tr> <td colspan="2"> <p>Setting this field along with setting the Pixel Location to upper left and number of multisamples to greater than one will cause the device to offset pixel positions by 0.5 both in horizontal and vertical</p> </td> </tr> </tbody> </table>	Project:	All	Format:	U1 Enumerated Type	<b>Programming Notes</b>		<p>Setting this field along with setting the Pixel Location to upper left and number of multisamples to greater than one will cause the device to offset pixel positions by 0.5 both in horizontal and vertical</p>	
Project:	All								
Format:	U1 Enumerated Type								
<b>Programming Notes</b>									
<p>Setting this field along with setting the Pixel Location to upper left and number of multisamples to greater than one will cause the device to offset pixel positions by 0.5 both in horizontal and vertical</p>									

### 3DSTATE\_WM\_HZ\_OP

		directions.It is to be noted this is done to adjust the pixel coordinate system to DX9 like, so any WM_HZ_OP screen space rectangles (eg: legacy HiZ Clear, Resolve etc) generated internally by driver in this mode needs to be aware of this offset adjustment and send the rectangles according to alignment restriction taking this offset adjustment into consideration. SW can choose to set this bit only for DX9 API. DX10/OGL API's should not have any effect by setting or not setting this bit.																																
25	<b>Full Surface Depth Clear</b>	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>Setting this field to "1" along with "Depth buffer clear" will cause all the pixels/samples in an 8x4 block in the HIZ buffer to be cleared. If "Stc-buffer clear" is also set, then all pixels/samples in a 8x8 block of STC buffer will be cleared to the stc-ref value. Software must set this only when the APP requires the entire Depth surface to be cleared. Setting this field to "1" for STC-buffer only clear without "depth buffer clear" will cause all the pixels/samples in an 8x8 block in the STC buffer to get the stc-ref value.</p>	Project:	All	Format:	Enable																												
Project:	All																																	
Format:	Enable																																	
24	<b>Reserved</b>	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ																												
Project:	All																																	
Format:	MBZ																																	
23:16	<b>Stencil Clear Value</b>	<table border="1"> <tr> <td>Format:</td> <td>U8.0</td> </tr> </table> <p>This field specifies the stencil clear value.</p>	Format:	U8.0																														
Format:	U8.0																																	
15:13	<b>Number of Multisamples</b>	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U3 Enumerated Type</td> </tr> </table> <p>This field specifies how many samples/pixel exist in the Depth Buffer and Stencil buffers, as <math>\log_2(\#samples)</math>.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>1</td> <td>1 sample/pixel</td> <td>All</td> </tr> <tr> <td>1h</td> <td>2</td> <td>2 samples/pixel</td> <td>All</td> </tr> <tr> <td>2h</td> <td>4</td> <td>4 samples/pixel</td> <td>All</td> </tr> <tr> <td>3h</td> <td>8</td> <td>8 samples/pixel</td> <td>All</td> </tr> <tr> <td>4h</td> <td>Reserved</td> <td></td> <td>CHV, BSW</td> </tr> <tr> <td>5h-7h</td> <td>Reserved</td> <td></td> <td>All</td> </tr> </tbody> </table>	Project:	All	Format:	U3 Enumerated Type	Value	Name	Description	Project	0h	1	1 sample/pixel	All	1h	2	2 samples/pixel	All	2h	4	4 samples/pixel	All	3h	8	8 samples/pixel	All	4h	Reserved		CHV, BSW	5h-7h	Reserved		All
Project:	All																																	
Format:	U3 Enumerated Type																																	
Value	Name	Description	Project																															
0h	1	1 sample/pixel	All																															
1h	2	2 samples/pixel	All																															
2h	4	4 samples/pixel	All																															
3h	8	8 samples/pixel	All																															
4h	Reserved		CHV, BSW																															
5h-7h	Reserved		All																															

<b>3DSTATE_WM_HZ_OP</b>												
	12:0	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> </table>	Project:	All								
Project:	All											
<p style="text-align: center;">2</p> <p><b>Programming Notes:</b> The clear rectangle x and y min and max values must be shifted by the LOD level; i.e. the hardware does not include the LOD in this function. Hence to clear any particular X, Y from the base level, to clear the contents at level "LOD" use (X»LOD) and (Y»LOD).</p>	31:16	<b>Clear Rectangle Y Min</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U16 in Pixels from Depth Buffer origin (upper left corner)</td> </tr> </table> <p>Specifies Ymin value of (inclusive) of clear rectangle with the Depth Buffer, used for clipping. Pixels with Y coordinates less than Ymin will not be affected.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>[0,16383]</td> <td>(Device ignores bits 31:30)</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Project:	All	Format:	U16 in Pixels from Depth Buffer origin (upper left corner)	Value	Name	Project	[0,16383]	(Device ignores bits 31:30)	CHV, BSW
	Project:	All										
Format:	U16 in Pixels from Depth Buffer origin (upper left corner)											
Value	Name	Project										
[0,16383]	(Device ignores bits 31:30)	CHV, BSW										
	15:0	<b>Clear Rectangle X Min</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U16 in Pixels from Depth Buffer origin (upper left corner)</td> </tr> </table> <p>Specifies Xmin value of (inclusive) of clear rectangle with the Depth Buffer, used for clipping. Pixels with X coordinates less than or equal to Xmin will not be affected.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>[0,16383]</td> <td>(Device ignores bits 15:14)</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Project:	All	Format:	U16 in Pixels from Depth Buffer origin (upper left corner)	Value	Name	Project	[0,16383]	(Device ignores bits 15:14)	CHV, BSW
Project:	All											
Format:	U16 in Pixels from Depth Buffer origin (upper left corner)											
Value	Name	Project										
[0,16383]	(Device ignores bits 15:14)	CHV, BSW										
<p style="text-align: center;">3</p> <p><b>Programming Notes:</b> See the programming note in the previous DWORD for the Min values.</p> <p>The clear rectangle x and y min and max values must be shifted by the LOD level; i.e. the hardware does not include the LOD in this function. Hence to clear any particular X, Y from the base level, to clear the contents at level "LOD" use (X»LOD) and (Y»LOD). Hence the max values must be less than or equal to: ( Surface Width » LOD ) and ( Surface Height » LOD ) for X Max and Y Max respectively.</p>	31:16	<b>Clear Rectangle Y Max</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U16 in Pixels from Depth Buffer origin (lower right corner)</td> </tr> </table> <p>Specifies Ymax value of (exclusive) of clear rectangle with the Depth Buffer, used for clipping. Pixels with Y coordinates greater than Ymax will be not be cleared.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>[0,16383]</td> <td>(Device ignores bits 31:30)</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Project:	All	Format:	U16 in Pixels from Depth Buffer origin (lower right corner)	Value	Name	Project	[0,16383]	(Device ignores bits 31:30)	CHV, BSW
	Project:	All										
Format:	U16 in Pixels from Depth Buffer origin (lower right corner)											
Value	Name	Project										
[0,16383]	(Device ignores bits 31:30)	CHV, BSW										
	15:0	<b>Clear Rectangle X Max</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U16 in Pixels from Depth Buffer origin (lower right corner)</td> </tr> </table> <p>Specifies Xmax value of (exclusive) of clear rectangle with the Depth Buffer, used for clipping. Pixels with X coordinates greater than or equal to Xmax will be not be affected.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>[0,16383]</td> <td>(Device ignores bits 15:14)</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Project:	All	Format:	U16 in Pixels from Depth Buffer origin (lower right corner)	Value	Name	Project	[0,16383]	(Device ignores bits 15:14)	CHV, BSW
Project:	All											
Format:	U16 in Pixels from Depth Buffer origin (lower right corner)											
Value	Name	Project										
[0,16383]	(Device ignores bits 15:14)	CHV, BSW										
<p style="text-align: center;">4</p>	31:16	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ						
	Project:	All										
Format:	MBZ											
	15:0	<b>Sample Mask</b>										



<b>3DSTATE_WM_HZ_OP</b>			
	<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Project:</td> <td style="width: 30%;">All</td> </tr> </table>	Project:	All
Project:	All		
	<p>Format: Right-justified bitmask (Bit 0 = Sample0). Number of bits that are used is determined by Num Multisamples (3DSTATE_WM_HZ_OP)</p>		
	<p>A per-multisample-position mask state variable that is immediately and unconditionally ANDed with the sample coverage mask as part of the rasterization process. This mask is applied prior to centroid selection.</p>		
	<p><b>Programming Notes</b></p>		
	<p>If Number of Multisamples is NUMSAMPLES_1, bits 15:1 of this field will be zeroed by HW.If Number of Multisamples is NUMSAMPLES_2, bits 15:2 of this field will be zeroed by HW.If Number of Multisamples is NUMSAMPLES_4, bits 15:4 of this field will be zeroed by HW.If Number of Multisamples is NUMSAMPLES_8, bits 15:8 of this field will be zeroed by HW.</p>		

## A64 Byte Scattered Write MSD

MSD1W_A64_BS - A64 Byte Scattered Write MSD								
Project:	CHV, BSW							
Source:	DataPort 1							
Length Bias:	1							
Family:	Scattered R/W							
Group:	Byte Scattered R/W							
DWord	Bit	Description						
0	19	<b>Header Present</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_MHF [CHV, BSW]</td> </tr> </table> Indicates that the message forbids a header	Project:	All	Format:	MDC_MHF [CHV, BSW]		
	Project:	All						
	Format:	MDC_MHF [CHV, BSW]						
	18:14	<b>Message Type</b> <table border="1"> <tr> <td>Default Value:</td> <td>1Ah</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> A64 Scattered Write message	Default Value:	1Ah	Project:	All	Format:	Opcode
	Default Value:	1Ah						
	Project:	All						
	Format:	Opcode						
	13	<b>Reserved</b>						
12	<b>Reserved</b>							
11:10	<b>Data Elements</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_A64_DS [CHV, BSW]</td> </tr> </table> Specifies the number of data elements to be read or written	Project:	All	Format:	MDC_A64_DS [CHV, BSW]			
Project:	All							
Format:	MDC_A64_DS [CHV, BSW]							
9:8	<b>A64 Scattered Message Subtype</b> <table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> Byte Read/Write subtype	Default Value:	0h	Project:	All	Format:	Opcode	
Default Value:	0h							
Project:	All							
Format:	Opcode							
7:0	<b>Binding Table Index</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_STATELESS [CHV, BSW]</td> </tr> </table> Specifies the message is stateless	Project:	All	Format:	MDC_STATELESS [CHV, BSW]			
Project:	All							
Format:	MDC_STATELESS [CHV, BSW]							

## A64 Dword Scattered Read MSD

MSD1R_A64_DWS - A64 Dword Scattered Read MSD			
Project:	CHV, BSW		
Source:	DataPort 1		
Length Bias:	1		
Family:	Scattered R/W		
Group:	DW Scattered R/W		
DWord	Bit	Description	
0	19	<b>Header Present</b>	
		Project: All	
		Format: MDC_MHF [CHV, BSW]	
			Indicates that the message forbids a header
	18:14	<b>Message Type</b>	
		Default Value:	10h
		Project:	All
Format:		Opcode	
		A64 Scattered Read message	
13	<b>Invalidate After Read</b>		
	Project:	All	
	Format:	MDC_IAR [CHV, BSW]	
		Specifies if L3 cache lines accessed by the message should be invalidated after the read occurs	
12	<b>Reserved</b>		
11:10	<b>Data Elements</b>		
	Project:	All	
	Format:	MDC_A64_DS [CHV, BSW]	
		Specifies the number of data elements to be read or written	
9:8	<b>A64 Scattered Message Subtype</b>		
	Default Value:	1h	
	Project:	All	
	Format:	Opcode	
		Dword Read/Write subtype	
7:0	<b>Binding Table Index</b>		
	Project:	All	
	Format:	MDC_STATELESS [CHV, BSW]	
		Specifies the message is stateless	

## A64 Dword Scattered Write MSD

<b>MSD1W_A64_DWS - A64 Dword Scattered Write MSD</b>								
Project:	CHV, BSW							
Source:	DataPort 1							
Length Bias:	1							
Family:	Scattered R/W							
Group:	DW Scattered R/W							
DWord	Bit	Description						
0	19	<p><b>Header Present</b></p> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_MHF [CHV, BSW]</td> </tr> </table> <p>Indicates that the message forbids a header</p>	Project:	All	Format:	MDC_MHF [CHV, BSW]		
	Project:	All						
	Format:	MDC_MHF [CHV, BSW]						
	18:14	<p><b>Message Type</b></p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>1Ah</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>A64 Scattered Write message</p>	Default Value:	1Ah	Project:	All	Format:	Opcode
	Default Value:	1Ah						
	Project:	All						
Format:	Opcode							
13	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>Ignored</p>	Project:	All	Format:	MBZ			
Project:	All							
Format:	MBZ							
12	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Ignore</td> </tr> </table> <p>Ignored</p>	Project:	CHV, BSW	Format:	Ignore			
Project:	CHV, BSW							
Format:	Ignore							
11:10	<p><b>Data Elements</b></p> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_A64_DS [CHV, BSW]</td> </tr> </table> <p>Specifies the number of data elements to be read or written</p>	Project:	All	Format:	MDC_A64_DS [CHV, BSW]			
Project:	All							
Format:	MDC_A64_DS [CHV, BSW]							
9:8	<p><b>A64 Scattered Message Subtype</b></p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>1h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Dword Read/Write subtype</p>	Default Value:	1h	Project:	All	Format:	Opcode	
Default Value:	1h							
Project:	All							
Format:	Opcode							

## MSD1W\_A64\_DWS - A64 Dword Scattered Write MSD

	7:0	<b>Binding Table Index</b>	
		Project:	All
		Format:	MDC_STATELESS [CHV, BSW]
		Specifies the message is stateless	

## A64 Dword SIMD4x2 Untyped Atomic Integer Binary with Return Data Operation MSD

MSD1R_A64_DWAI2_4x2 - A64 Dword SIMD4x2 Untyped Atomic Integer Binary with Return Data Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Atomic Operation	
Group:	Dword Untyped Atomic Integer Binary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHF [CHV, BSW]
		The message forbids a header
18:14	<b>Message Type</b>	Default Value: 13h
		Project: All
		Format: Opcode
		A64 Untyped Atomic Integer Operation SIMD4x2 message
13	<b>Return Data Control</b>	Default Value: 1h
		Project: All
		Format: Opcode
		Specifies that return data is sent back to the thread.
12	<b>Data Width</b>	Default Value: 0h
		Project: All
		Format: Opcode
		Operations are on 32-bit integers
11:8	<b>Atomic Integer Operation</b>	Project: All
		Format: MDC_AOP2 [CHV, BSW]
		Specifies the atomic integer operation to be performed.

MSD1R_A64_DWAI2_4x2 - A64 Dword SIMD4x2 Untyped Atomic Integer Binary with Return Data Operation MSD						
	7:0	<p><b>Binding Table Index</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_STATELESS [CHV, BSW]</td> </tr> </table> <p>Specifies the message is stateless</p>	Project:	All	Format:	MDC_STATELESS [CHV, BSW]
Project:	All					
Format:	MDC_STATELESS [CHV, BSW]					

## A64 Dword SIMD4x2 Untyped Atomic Integer Binary Write Only Operation MSD

MSD1W_A64_DWAI2_4x2 - A64 Dword SIMD4x2 Untyped Atomic Integer Binary Write Only Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Atomic Operation	
Group:	Dword Untyped Atomic Integer Binary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHF [CHV, BSW]
		The message forbids a header
18:14	<b>Message Type</b>	Default Value: 13h
		Project: All
		Format: Opcode
		A64 Untyped Atomic Integer Operation SIMD4x2 message
13	<b>Return Data Control</b>	Default Value: 0h
		Project: All
		Format: Opcode
		Specifies that no return data is sent back to the thread.
12	<b>Data Width</b>	Default Value: 0h
		Project: All
		Format: Opcode
		Operations are on 32-bit integers
11:8	<b>Atomic Integer Operation</b>	Project: All
		Format: MDC_AOP2 [CHV, BSW]
		Specifies the atomic integer operation to be performed.



<b>MSD1W_A64_DWAI2_4x2 - A64 Dword SIMD4x2 Untyped Atomic Integer Binary Write Only Operation MSD</b>						
	7:0	<p><b>Binding Table Index</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_STATELESS [CHV, BSW]</td> </tr> </table> <p>Specifies the message is stateless</p>	Project:	All	Format:	MDC_STATELESS [CHV, BSW]
Project:	All					
Format:	MDC_STATELESS [CHV, BSW]					

## A64 Dword SIMD4x2 Untyped Atomic Integer Ternary with Return Data Operation MSD

MSD1R_A64_DWAI3_4x2 - A64 Dword SIMD4x2 Untyped Atomic Integer Ternary with Return Data Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Atomic Operation	
Group:	Dword Untyped Atomic Integer Ternary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHF [CHV, BSW]
		The message forbids a header
18:14	<b>Message Type</b>	Default Value: 13h
		Project: All
		Format: Opcode
		A64 Untyped Atomic Integer Operation SIMD4x2 message
13	<b>Return Data Control</b>	Default Value: 1h
		Project: All
		Format: Opcode
		Specifies that return data is sent back to the thread.
12	<b>Data Width</b>	Default Value: 0h
		Project: All
		Format: Opcode
		Operations are on 32-bit integers
11:8	<b>Atomic Integer Operation</b>	Project: CHV, BSW
		Format: MDC_AOP3S [CHV, BSW]
		Specifies the atomic integer operation to be performed.

<b>MSD1R_A64_DWAI3_4x2 - A64 Dword SIMD4x2 Untyped Atomic Integer Ternary with Return Data Operation MSD</b>		
		<b>Workaround</b>
		CMPWR_2W Operation is not supported in A64 SIMD4x2.
	7:0	<b>Binding Table Index</b>
		Project: All
		Format: MDC_STATELESS [CHV, BSW]
		Specifies the message is stateless

## A64 Dword SIMD4x2 Untyped Atomic Integer Trinary Write Only Operation MSD

MSD1W_A64_DWAI3_4x2 - A64 Dword SIMD4x2 Untyped Atomic Integer Trinary Write Only Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Atomic Operation	
Group:	Dword Untyped Atomic Integer Trinary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHF [CHV, BSW]
		The message forbids a header
18:14	<b>Message Type</b>	Default Value: 13h
		Project: All
		Format: Opcode
		A64 Untyped Atomic Integer Operation SIMD4x2 message
13	<b>Return Data Control</b>	Default Value: 0h
		Project: All
		Format: Opcode
		Specifies that no return data is sent back to the thread.
12	<b>Data Width</b>	Default Value: 0h
		Project: All
		Format: Opcode
		Operations are on 32-bit integers
11:8	<b>Atomic Integer Operation</b>	Project: CHV, BSW
		Format: MDC_AOP3S [CHV, BSW]
		Specifies the atomic integer operation to be performed.

<b>MSD1W_A64_DWAI3_4x2 - A64 Dword SIMD4x2 Untyped Atomic Integer Trinary Write Only Operation MSD</b>									
	<table border="1"> <tr> <th colspan="2" style="text-align: center;">Workaround</th> </tr> <tr> <td colspan="2">CMPWR_2W is not supported by A64 SIMD4x2.</td> </tr> </table>	Workaround		CMPWR_2W is not supported by A64 SIMD4x2.					
Workaround									
CMPWR_2W is not supported by A64 SIMD4x2.									
7:0	<table border="1"> <tr> <th colspan="2">Binding Table Index</th> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_STATELESS [CHV, BSW]</td> </tr> <tr> <td colspan="2">Specifies the message is stateless</td> </tr> </table>	Binding Table Index		Project:	All	Format:	MDC_STATELESS [CHV, BSW]	Specifies the message is stateless	
Binding Table Index									
Project:	All								
Format:	MDC_STATELESS [CHV, BSW]								
Specifies the message is stateless									

## A64 Dword SIMD4x2 Untyped Atomic Integer Unary with Return Data Operation MSD

MSD1R_A64_DWAI1_4x2 - A64 Dword SIMD4x2 Untyped Atomic Integer Unary with Return Data Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Atomic Operation	
Group:	Dword Untyped Atomic Integer Unary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHF [CHV, BSW]
		The message forbids a header
18:14	<b>Message Type</b>	Default Value: 13h
		Project: All
		Format: Opcode
		A64 Untyped Atomic Integer Operation SIMD4x2 message
13	<b>Return Data Control</b>	Default Value: 1h
		Project: All
		Format: Opcode
		Specifies that return data is sent back to the thread.
12	<b>Data Width</b>	Default Value: 0h
		Project: All
		Format: Opcode
		Operations are on 32-bit integers
11:8	<b>Atomic Integer Operation</b>	Project: All
		Format: MDC_AOP1 [CHV, BSW]
		Specifies the atomic integer operation to be performed.

<b>MSD1R_A64_DWAI1_4x2 - A64 Dword SIMD4x2 Untyped Atomic Integer Unary with Return Data Operation MSD</b>							
	<table border="1" style="width: 100%;"> <tr> <td style="width: 15%; text-align: center; vertical-align: top;">7:0</td> <td> <p><b>Binding Table Index</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_STATELESS [CHV, BSW]</td> </tr> </table> <p>Specifies the message is stateless</p> </td> </tr> </table>	7:0	<p><b>Binding Table Index</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_STATELESS [CHV, BSW]</td> </tr> </table> <p>Specifies the message is stateless</p>	Project:	All	Format:	MDC_STATELESS [CHV, BSW]
7:0	<p><b>Binding Table Index</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_STATELESS [CHV, BSW]</td> </tr> </table> <p>Specifies the message is stateless</p>	Project:	All	Format:	MDC_STATELESS [CHV, BSW]		
Project:	All						
Format:	MDC_STATELESS [CHV, BSW]						

## A64 Dword SIMD4x2 Untyped Atomic Integer Unary Write Only Operation MSD

MSD1W_A64_DWAI1_4x2 - A64 Dword SIMD4x2 Untyped Atomic Integer Unary Write Only Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Atomic Operation	
Group:	Dword Untyped Atomic Integer Unary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHF [CHV, BSW]
		The message forbids a header
18:14	<b>Message Type</b>	Default Value: 13h
		Project: All
		Format: Opcode
		A64 Untyped Atomic Integer Operation SIMD4x2 message
13	<b>Return Data Control</b>	Default Value: 0h
		Project: All
		Format: Opcode
		Specifies that no return data is sent back to the thread.
12	<b>Data Width</b>	Default Value: 0h
		Project: All
		Format: Opcode
		Operations are on 32-bit integers
11:8	<b>Atomic Integer Operation</b>	Project: All
		Format: MDC_AOP1 [CHV, BSW]
		Specifies the atomic integer operation to be performed.



<b>MSD1W_A64_DWAI1_4x2 - A64 Dword SIMD4x2 Untyped Atomic Integer Unary Write Only Operation MSD</b>						
	7:0	<p><b>Binding Table Index</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_STATELESS [CHV, BSW]</td> </tr> </table> <p>Specifies the message is stateless</p>	Project:	All	Format:	MDC_STATELESS [CHV, BSW]
Project:	All					
Format:	MDC_STATELESS [CHV, BSW]					

## A64 Dword Untyped Atomic Integer Binary with Return Data Operation MSD

MSD1R_A64_DWAI2 - A64 Dword Untyped Atomic Integer Binary with Return Data Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Atomic Operation	
Group:	Dword Untyped Atomic Integer Binary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHF [CHV, BSW]
		The message forbids a header
18:14	<b>Message Type</b>	Default Value: 12h
		Project: All
		Format: Opcode
		A64 Untyped Atomic Integer Operation message
13	<b>Return Data Control</b>	Default Value: 1h
		Project: All
		Format: Opcode
		Specifies that return data is sent back to the thread.
12	<b>Data Width</b>	Default Value: 0h
		Project: All
		Format: Opcode
		Operations are on 32-bit integers
11:8	<b>Atomic Integer Operation</b>	Project: All
		Format: MDC_AOP2 [CHV, BSW]
		Specifies the atomic integer operation to be performed.

<b>MSD1R_A64_DWAI2 - A64 Dword Untyped Atomic Integer Binary with Return Data Operation MSD</b>							
	<table border="1" style="width: 100%;"> <tr> <td style="width: 10%; text-align: center; vertical-align: top;">7:0</td> <td> <p><b>Binding Table Index</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_STATELESS [CHV, BSW]</td> </tr> </table> <p>Specifies the message is stateless</p> </td> </tr> </table>	7:0	<p><b>Binding Table Index</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_STATELESS [CHV, BSW]</td> </tr> </table> <p>Specifies the message is stateless</p>	Project:	All	Format:	MDC_STATELESS [CHV, BSW]
7:0	<p><b>Binding Table Index</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_STATELESS [CHV, BSW]</td> </tr> </table> <p>Specifies the message is stateless</p>	Project:	All	Format:	MDC_STATELESS [CHV, BSW]		
Project:	All						
Format:	MDC_STATELESS [CHV, BSW]						

## A64 Dword Untyped Atomic Integer Binary Write Only Operation MSD

MSD1W_A64_DWAI2 - A64 Dword Untyped Atomic Integer Binary Write Only Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Atomic Operation	
Group:	Dword Untyped Atomic Integer Binary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHF [CHV, BSW]
		The message forbids a header
18:14	<b>Message Type</b>	Default Value: 12h
		Project: All
		Format: Opcode
		A64 Untyped Atomic Integer Operation message
13	<b>Return Data Control</b>	Default Value: 0h
		Project: All
		Format: Opcode
		Specifies that no return data is sent back to the thread.
12	<b>Data Width</b>	Default Value: 0h
		Project: All
		Format: Opcode
		Operations are on 32-bit integers
11:8	<b>Atomic Integer Operation</b>	Project: All
		Format: MDC_AOP2 [CHV, BSW]
		Specifies the atomic integer operation to be performed.

## MSD1W\_A64\_DWAI2 - A64 Dword Untyped Atomic Integer Binary Write Only Operation MSD

	7:0	<b>Binding Table Index</b>	
		Project:	All
		Format:	MDC_STATELESS [CHV, BSW]
		Specifies the message is stateless	

## A64 Dword Untyped Atomic Integer Ternary with Return Data Operation MSD

MSD1R_A64_DWAI3 - A64 Dword Untyped Atomic Integer Ternary with Return Data Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Atomic Operation	
Group:	Dword Untyped Atomic Integer Ternary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHF [CHV, BSW]
		The message forbids a header
18:14	<b>Message Type</b>	Default Value: 12h
		Project: All
		Format: Opcode
		A64 Untyped Atomic Integer Operation message
13	<b>Return Data Control</b>	Default Value: 1h
		Project: All
		Format: Opcode
		Specifies that return data is sent back to the thread.
12	<b>Data Width</b>	Default Value: 0h
		Project: All
		Format: Opcode
		Operations are on 32-bit integers
11:8	<b>Atomic Integer Operation</b>	Project: All
		Format: MDC_AOP3 [CHV, BSW]
		Specifies the atomic integer operation to be performed.

## MSD1R\_A64\_DWAI3 - A64 Dword Untyped Atomic Integer Trinary with Return Data Operation MSD

	7:0	<b>Binding Table Index</b>	
		Project:	All
		Format:	MDC_STATELESS [CHV, BSW]
		Specifies the message is stateless	

## A64 Dword Untyped Atomic Integer Trinary Write Only Operation MSD

MSD1W_A64_DWAI3 - A64 Dword Untyped Atomic Integer Trinary Write Only Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Atomic Operation	
Group:	Dword Untyped Atomic Integer Trinary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHF [CHV, BSW]
		The message forbids a header
18:14	<b>Message Type</b>	Default Value: 12h
		Project: All
		Format: Opcode
		A64 Untyped Atomic Integer Operation message
13	<b>Return Data Control</b>	Default Value: 0h
		Project: All
		Format: Opcode
		Specifies that no return data is sent back to the thread.
12	<b>Data Width</b>	Default Value: 0h
		Project: All
		Format: Opcode
		Operations are on 32-bit integers
11:8	<b>Atomic Integer Operation</b>	Project: All
		Format: MDC_AOP3 [CHV, BSW]
		Specifies the atomic integer operation to be performed.



## MSD1W\_A64\_DWAI3 - A64 Dword Untyped Atomic Integer Trinary Write Only Operation MSD

	7:0	<b>Binding Table Index</b>	
		Project:	All
		Format:	MDC_STATELESS [CHV, BSW]
		Specifies the message is stateless	

## A64 Dword Untyped Atomic Integer Unary with Return Data Operation MSD

MSD1R_A64_DWAI1 - A64 Dword Untyped Atomic Integer Unary with Return Data Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Atomic Operation	
Group:	Dword Untyped Atomic Integer Unary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHF [CHV, BSW]
		The message forbids a header
18:14	<b>Message Type</b>	Default Value: 12h
		Project: All
		Format: Opcode
		A64 Untyped Atomic Integer Operation message
13	<b>Return Data Control</b>	Default Value: 1h
		Project: All
		Format: Opcode
		Specifies that return data is sent back to the thread.
12	<b>Data Width</b>	Default Value: 0h
		Project: All
		Format: Opcode
		Operations are on 32-bit integers
11:8	<b>Atomic Integer Operation</b>	Project: All
		Format: MDC_AOP1 [CHV, BSW]
		Specifies the atomic integer operation to be performed.

MSD1R_A64_DWAI1 - A64 Dword Untyped Atomic Integer Unary with Return Data Operation MSD						
	7:0	<p><b>Binding Table Index</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_STATELESS [CHV, BSW]</td> </tr> </table> <p>Specifies the message is stateless</p>	Project:	All	Format:	MDC_STATELESS [CHV, BSW]
Project:	All					
Format:	MDC_STATELESS [CHV, BSW]					

## A64 Dword Untyped Atomic Integer Unary Write Only Operation MSD

MSD1W_A64_DWAI1 - A64 Dword Untyped Atomic Integer Unary Write Only Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Atomic Operation	
Group:	Dword Untyped Atomic Integer Unary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHF [CHV, BSW]
		The message forbids a header
18:14	<b>Message Type</b>	Default Value: 12h
		Project: All
		Format: Opcode
		A64 Untyped Atomic Integer Operation message
13	<b>Return Data Control</b>	Default Value: 0h
		Project: All
		Format: Opcode
		Specifies that no return data is sent back to the thread.
12	<b>Data Width</b>	Default Value: 0h
		Project: All
		Format: Opcode
		Operations are on 32-bit integers
11:8	<b>Atomic Integer Operation</b>	Project: All
		Format: MDC_AOP1 [CHV, BSW]
		Specifies the atomic integer operation to be performed.

## MSD1W\_A64\_DWAI1 - A64 Dword Untyped Atomic Integer Unary Write Only Operation MSD

	7:0	<b>Binding Table Index</b>	
		Project:	All
		Format:	MDC_STATELESS [CHV, BSW]
		Specifies the message is stateless	

## A64 Hword Block Read MSD

<b>MSD1R_A64_HWB - A64 Hword Block Read MSD</b>					
Project:	CHV, BSW				
Source:	DataPort 1				
Length Bias:	1				
Family:	Block R/W				
Group:	HW Block R/W				
DWord	Bit	Description			
0	19	<b>Header Present</b>			
		<table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_MHR [CHV, BSW]</td> </tr> </table> <p>Indicates that the message requires a header.</p>	Project:	All	Format:
	Project:	All			
	Format:	MDC_MHR [CHV, BSW]			
	18:14	<b>Message Type</b>			
		Default Value:	14h		
Project:		All			
Format:		Opcode			
A64 Oword Block Read message					
13	<b>Invalidate After Read</b>				
	<table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_IAR [CHV, BSW]</td> </tr> </table> <p>Specifies if L3 cache lines accessed by the message should be invalidated after the read occurs</p>	Project:	All	Format:	MDC_IAR [CHV, BSW]
Project:	All				
Format:	MDC_IAR [CHV, BSW]				
12:11	<b>A64 Block Message Subtype</b>				
	Default Value:	3h			
	Project:	All			
Format:		Opcode			
Hword Block Read/Write subtype					
10:8	<b>Data Elements</b>				
	<table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_A64_DB_HW [CHV, BSW]</td> </tr> </table> <p>Specifies the number of contiguous Hwords to be read or written</p>	Project:	All	Format:	MDC_A64_DB_HW [CHV, BSW]
Project:	All				
Format:	MDC_A64_DB_HW [CHV, BSW]				
7:0	<b>Binding Table Index</b>				
	Project:	All			
	Format:	MDC_STATELESS [CHV, BSW]			
Specifies the message is stateless					

## A64 Hword Block Write MSD

MSD1W_A64_HWB - A64 Hword Block Write MSD			
Project:	CHV, BSW		
Source:	DataPort 1		
Length Bias:	1		
Family:	Block R/W		
Group:	HW Block R/W		
DWord	Bit	Description	
0	19	<b>Header Present</b>	
		Project: All	
		Format: MDC_MHR [CHV, BSW]	
	Indicates that the message requires a header.		
	18:14	<b>Message Type</b>	
		Default Value: 15h	
Project: All			
Format: Opcode			
A64 Hword Block Write message			
13	<b>Reserved</b>		
	Project: All		
	Format: MBZ		
Ignored			
12:11	<b>A64 Block Message Subtype</b>		
	Default Value: 3h		
	Project: All		
	Format: Opcode		
Hword Block Read/Write subtype			
10:8	<b>Data Elements</b>		
	Project: All		
	Format: MDC_A64_DB_HW [CHV, BSW]		
Specifies the number of contiguous Hwords to be read or written			
7:0	<b>Binding Table Index</b>		
	Project: All		
	Format: MDC_STATELESS [CHV, BSW]		
Specifies the message is stateless			

## A64 Oword Block Read MSD

MSD1R_A64_OWB - A64 Oword Block Read MSD			
Project:	CHV, BSW		
Source:	DataPort 1		
Length Bias:	1		
Family:	Block R/W		
Group:	OW Block R/W		
DWord	Bit	Description	
0	19	<b>Header Present</b>	
		Project: All Format: MDC_MHR [CHV, BSW] Indicates that the message requires a header.	
	18:14	<b>Message Type</b>	
		Default Value: 14h Project: All Format: Opcode A64 Oword Block Read message	
		13	<b>Invalidate After Read</b>
			Project: All Format: MDC_IAR [CHV, BSW] Specifies if L3 cache lines accessed by the message should be invalidated after the read occurs
12:11	<b>A64 Block Message Subtype</b>		
	Default Value: 0h Project: All Format: Opcode Oword Block Read/Write subtype		
	10:8	<b>Data Elements</b>	
Project: All Format: MDC_A64_DB_OW [CHV, BSW] Specifies the number of contiguous Owords to be read or written			
7:0	<b>Binding Table Index</b>		
	Project: All Format: MDC_STATELESS [CHV, BSW] Specifies the message is stateless		



## A64 Oword Block Write MSD

MSD1W_A64_OWB - A64 Oword Block Write MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Block R/W	
Group:	OW Block R/W	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHR [CHV, BSW]
	Indicates that the message requires a header.	
	18:14	<b>Message Type</b>
		Default Value: 15h
Project: All		
Format: Opcode		
A64 Oword Block Write message		
13	<b>Reserved</b>	
	Project: All	
	Format: MBZ	
Ignored		
12:11	<b>A64 Block Message Subtype</b>	
	Default Value: 0h	
	Project: All	
	Format: Opcode	
Oword Block Read/Write subtype		
10:8	<b>Data Elements</b>	
	Project: All	
	Format: MDC_A64_DB_OW [CHV, BSW]	
Specifies the number of contiguous Owords to be read or written		
7:0	<b>Binding Table Index</b>	
	Project: All	
	Format: MDC_STATELESS [CHV, BSW]	
Specifies the message is stateless		

## A64 Oword Dual Block Read MSD

MSD1R_A64_OWDB - A64 Oword Dual Block Read MSD			
Project:	CHV, BSW		
Source:	DataPort 1		
Length Bias:	1		
Family:	Block R/W		
Group:	OW Dual Block R/W		
DWord	Bit	Description	
0	19	<b>Header Present</b>	
		Project: All	
		Format: MDC_MHR [CHV, BSW]	
			Indicates that the message requires a header.
	18:14	<b>Message Type</b>	
		Default Value:	14h
		Project:	All
		Format:	Opcode
			A64 Oword Block Read message
	13	<b>Invalidate After Read</b>	
Project:		All	
Format:		MDC_IAR [CHV, BSW]	
		Specifies if L3 cache lines accessed by the message should be invalidated after the read occurs	
12:11	<b>A64 Block Message Subtype</b>		
	Default Value:	2h	
	Project:	All	
	Format:	Opcode	
		Oword Dual Block Read/Write subtype	
10:8	<b>Data Elements</b>		
	Project:	All	
	Format:	MDC_A64_DB_OWDB	
		Specifies the number of contiguous Owords to be read or written	
7:0	<b>Binding Table Index</b>		
	Project:	All	
	Format:	MDC_STATELESS [CHV, BSW]	
		Specifies the message is stateless	

## A64 Oword Dual Block Write MSD

MSD1W_A64_OWDB - A64 Oword Dual Block Write MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Block R/W	
Group:	OW Dual Block R/W	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHR [CHV, BSW]
	Indicates that the message requires a header.	
	18:14	<b>Message Type</b>
		Default Value: 15h
Project: All		
Format: Opcode		
A64 Oword Block Write message		
13	<b>Reserved</b>	
	Project: All	
	Format: MBZ	
Ignored		
12:11	<b>A64 Block Message Subtype</b>	
	Default Value: 2h	
	Project: All	
	Format: Opcode	
Oword Dual Block Read/Write subtype		
10:8	<b>Data Elements</b>	
	Project: All	
	Format: MDC_A64_DB_OWD	
Specifies the number of contiguous Owords to be read or written		
7:0	<b>Binding Table Index</b>	
	Project: All	
	Format: MDC_STATELESS [CHV, BSW]	
Specifies the message is stateless		

## A64 Oword Unaligned Block Read MSD

MSD1R_A64_OWUB - A64 Oword Unaligned Block Read MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Block R/W	
Group:	OW Unaligned Block R/W	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHR [CHV, BSW]
	Indicates that the message requires a header.	
	18:14	<b>Message Type</b>
		Default Value: 14h
Project: All		
Format: Opcode		
A64 Oword Block Read message		
13	<b>Reserved</b>	
	Project: All	
	Format: MBZ	
Ignored		
12:11	<b>A64 Block Message Subtype</b>	
	Default Value: 1h	
	Project: All	
	Format: Opcode	
Oword Unaligned Block Read subtype		
10:8	<b>Data Elements</b>	
	Project: All	
	Format: MDC_A64_DB_OW [CHV, BSW]	
Specifies the number of contiguous Owords to be read		
7:0	<b>Binding Table Index</b>	
	Project: All	
	Format: MDC_STATELESS [CHV, BSW]	
Specifies the message is stateless		

## A64 Qword Scattered Write MSD

MSD1W_A64_QWS - A64 Qword Scattered Write MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Scattered R/W	
Group:	QW Scattered R/W	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHF [CHV, BSW]
	Indicates that the message forbids a header	
	18:14	<b>Message Type</b>
		Default Value: 1Ah
Project: All		
Format: Opcode		
A64 Scattered Write message		
13	<b>Reserved</b>	
	Project: All	
	Format: MBZ	
Ignored		
12	<b>Reserved</b>	
	Project: CHV, BSW	
	Format: Ignore	
Ignored		
11:10	<b>Data Elements</b>	
	Project: All	
	Format: MDC_A64_DS [CHV, BSW]	
Specifies the number of data elements to be read or written		
9:8	<b>A64 Scattered Message Subtype</b>	
	Default Value: 2h	
	Project: All	
	Format: Opcode	
Qword Read/Write subtype		

## MSD1W\_A64\_QWS - A64 Qword Scattered Write MSD

	7:0	<b>Binding Table Index</b>	
		Project:	All
		Format:	MDC_STATELESS [CHV, BSW]
Specifies the message is stateless			

## A64 Qword SIMD4x2 Untyped Atomic Integer Binary with Return Data Operation MSD

MSD1R_A64_QWAI2_4x2 - A64 Qword SIMD4x2 Untyped Atomic Integer Binary with Return Data Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Atomic Operation	
Group:	Qword Untyped Atomic Integer Binary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHF [CHV, BSW]
		The message forbids a header
18:14	<b>Message Type</b>	Default Value: 13h
		Project: All
		Format: Opcode
		A64 Untyped Atomic Integer Operation SIMD4x2 message
13	<b>Return Data Control</b>	Default Value: 1h
		Project: All
		Format: Opcode
		Specifies that return data is sent back to the thread.
12	<b>Data Width</b>	Default Value: 1h
		Project: All
		Format: Opcode
		Operations are on 64-bit integers
11:8	<b>Atomic Integer Operation</b>	Project: All
		Format: MDC_AOP2 [CHV, BSW]
		Specifies the atomic integer operation to be performed.

## MSD1R\_A64\_QWAI2\_4x2 - A64 Qword SIMD4x2 Untyped Atomic Integer Binary with Return Data Operation MSD

	7:0	<b>Binding Table Index</b>	
		Project:	All
		Format:	MDC_STATELESS [CHV, BSW]
		Specifies the message is stateless	



## A64 Qword SIMD4x2 Untyped Atomic Integer Binary Write Only Operation MSD

MSD1W_A64_QWAI2_4x2 - A64 Qword SIMD4x2 Untyped Atomic Integer Binary Write Only Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Atomic Operation	
Group:	Qword Untyped Atomic Integer Binary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHF [CHV, BSW]
		The message forbids a header
18:14	<b>Message Type</b>	Default Value: 13h
		Project: All
		Format: Opcode
		A64 Untyped Atomic Integer Operation SIMD4x2 message
13	<b>Return Data Control</b>	Default Value: 0h
		Project: All
		Format: Opcode
		Specifies that no return data is sent back to the thread.
12	<b>Data Width</b>	Default Value: 1h
		Project: All
		Format: Opcode
		Operations are on 64-bit integers
11:8	<b>Atomic Integer Operation</b>	Project: All
		Format: MDC_AOP2 [CHV, BSW]
		Specifies the atomic integer operation to be performed.

## MSD1W\_A64\_QWAI2\_4x2 - A64 Qword SIMD4x2 Untyped Atomic Integer Binary Write Only Operation MSD

	7:0	<b>Binding Table Index</b>	
		Project:	All
		Format:	MDC_STATELESS [CHV, BSW]
		Specifies the message is stateless	

## A64 Qword SIMD4x2 Untyped Atomic Integer Ternary with Return Data Operation MSD

MSD1R_A64_QWAI3_4x2 - A64 Qword SIMD4x2 Untyped Atomic Integer Ternary with Return Data Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Atomic Operation	
Group:	Qword Untyped Atomic Integer Ternary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHF [CHV, BSW]
		The message forbids a header
18:14	<b>Message Type</b>	Default Value: 13h
		Project: All
		Format: Opcode
		A64 Untyped Atomic Integer Operation SIMD4x2 message
13	<b>Return Data Control</b>	Default Value: 1h
		Project: All
		Format: Opcode
		Specifies that return data is sent back to the thread.
12	<b>Data Width</b>	Default Value: 1h
		Project: All
		Format: Opcode
		Operations are on 64-bit integers
11:8	<b>Atomic Integer Operation</b>	Project: CHV, BSW
		Specifies the atomic integer operation to be performed.
		<b>Workaround</b>
		CMPWR_2W is not supported in A64 SIMD4x2

<b>MSD1R_A64_QWAI3_4x2 - A64 Qword SIMD4x2 Untyped Atomic Integer Ternary with Return Data Operation MSD</b>									
	<table border="1" style="width: 100%;"> <tr> <td style="width: 15%; text-align: center; vertical-align: top;">7:0</td> <td> <b>Binding Table Index</b> </td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_STATELESS [CHV, BSW]</td> </tr> <tr> <td colspan="2">Specifies the message is stateless</td> </tr> </table>	7:0	<b>Binding Table Index</b>	Project:	All	Format:	MDC_STATELESS [CHV, BSW]	Specifies the message is stateless	
7:0	<b>Binding Table Index</b>								
Project:	All								
Format:	MDC_STATELESS [CHV, BSW]								
Specifies the message is stateless									

## A64 Qword SIMD4x2 Untyped Atomic Integer Ternary Write Only Operation MSD

MSD1W_A64_QWAI3_4x2 - A64 Qword SIMD4x2 Untyped Atomic Integer Ternary Write Only Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Atomic Operation	
Group:	Qword Untyped Atomic Integer Ternary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHF [CHV, BSW]
		The message forbids a header
18:14	<b>Message Type</b>	Default Value: 13h
		Project: All
		Format: Opcode
		A64 Untyped Atomic Integer Operation SIMD4x2 message
13	<b>Return Data Control</b>	Default Value: 0h
		Project: All
		Format: Opcode
		Specifies that no return data is sent back to the thread.
12	<b>Data Width</b>	Default Value: 1h
		Project: All
		Format: Opcode
		Operations are on 64-bit integers
11:8	<b>Atomic Integer Operation</b>	Project: CHV, BSW
		Format: MDC_AOP3S [CHV, BSW]
		Specifies the atomic integer operation to be performed.

<b>MSD1W_A64_QWAI3_4x2 - A64 Qword SIMD4x2 Untyped Atomic Integer Trinary Write Only Operation MSD</b>		
		<b>Workaround</b>
		CMPWR_2W is not supported in A64 SIMD4x2.
	7:0	<b>Binding Table Index</b>
		Project: All
		Format: MDC_STATELESS [CHV, BSW]
		Specifies the message is stateless

## A64 Qword SIMD4x2 Untyped Atomic Integer Unary with Return Data Operation MSD

MSD1R_A64_QWAI1_4x2 - A64 Qword SIMD4x2 Untyped Atomic Integer Unary with Return Data Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Atomic Operation	
Group:	Qword Untyped Atomic Integer Unary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHF [CHV, BSW]
		The message forbids a header
18:14	<b>Message Type</b>	Default Value: 13h
		Project: All
		Format: Opcode
		A64 Untyped Atomic Integer Operation SIMD4x2 message
13	<b>Return Data Control</b>	Default Value: 1h
		Project: All
		Format: Opcode
		Specifies that return data is sent back to the thread.
12	<b>Data Width</b>	Default Value: 1h
		Project: All
		Format: Opcode
		Operations are on 64-bit integers
11:8	<b>Atomic Integer Operation</b>	Project: All
		Format: MDC_AOP1 [CHV, BSW]
		Specifies the atomic integer operation to be performed.

<b>MSD1R_A64_QWAI1_4x2 - A64 Qword SIMD4x2 Untyped Atomic Integer Unary with Return Data Operation MSD</b>	
	7:0
<b>Binding Table Index</b>	
Specifies the message is stateless	



## A64 Qword SIMD4x2 Untyped Atomic Integer Unary Write Only Operation MSD

MSD1W_A64_QWAI1_4x2 - A64 Qword SIMD4x2 Untyped Atomic Integer Unary Write Only Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Atomic Operation	
Group:	Qword Untyped Atomic Integer Unary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHF [CHV, BSW]
		The message forbids a header
18:14	<b>Message Type</b>	Default Value: 13h
		Project: All
		Format: Opcode
		A64 Untyped Atomic Integer Operation SIMD4x2 message
13	<b>Return Data Control</b>	Default Value: 0h
		Project: All
		Format: Opcode
		Specifies that no return data is sent back to the thread.
12	<b>Data Width</b>	Default Value: 1h
		Project: All
		Format: Opcode
		Operations are on 64-bit integers
11:8	<b>Atomic Integer Operation</b>	Project: All
		Format: MDC_AOP1 [CHV, BSW]
		Specifies the atomic integer operation to be performed.

## MSD1W\_A64\_QWAI1\_4x2 - A64 Qword SIMD4x2 Untyped Atomic Integer Unary Write Only Operation MSD

	7:0	<b>Binding Table Index</b>	
		Project:	All
		Format:	MDC_STATELESS [CHV, BSW]
		Specifies the message is stateless	

## A64 Qword Untyped Atomic Integer Binary with Return Data Operation MSD

MSD1R_A64_QWAI2 - A64 Qword Untyped Atomic Integer Binary with Return Data Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Atomic Operation	
Group:	Qword Untyped Atomic Integer Binary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHF [CHV, BSW]
		The message forbids a header
18:14	<b>Message Type</b>	Default Value: 12h
		Project: All
		Format: Opcode
		A64 Untyped Atomic Integer Operation message
13	<b>Return Data Control</b>	Default Value: 1h
		Project: All
		Format: Opcode
		Specifies that return data is sent back to the thread.
12	<b>Data Width</b>	Default Value: 1h
		Project: All
		Format: Opcode
		Operations are on 64-bit integers
11:8	<b>Atomic Integer Operation</b>	Project: All
		Format: MDC_AOP2 [CHV, BSW]
		Specifies the atomic integer operation to be performed.

## MSD1R\_A64\_QWAI2 - A64 Qword Untyped Atomic Integer Binary with Return Data Operation MSD

	7:0	<b>Binding Table Index</b>	
		Project:	All
		Format:	MDC_STATELESS [CHV, BSW]
		Specifies the message is stateless	

## A64 Qword Untyped Atomic Integer Binary Write Only Operation MSD

MSD1W_A64_QWAI2 - A64 Qword Untyped Atomic Integer Binary Write Only Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Atomic Operation	
Group:	Qword Untyped Atomic Integer Binary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
	Format: MDC_MHF [CHV, BSW]	
	The message forbids a header	
	18:14	<b>Message Type</b>
Default Value: 12h		
Project: All		
Format: Opcode		
A64 Untyped Atomic Integer Operation message		
13	<b>Return Data Control</b>	
	Default Value: 0h	
	Project: All	
	Format: Opcode	
Specifies that no return data is sent back to the thread.		
12	<b>Data Width</b>	
	Default Value: 1h	
	Project: All	
	Format: Opcode	
Operations are on 64-bit integers		
11:8	<b>Atomic Integer Operation</b>	
	Project: All	
	Format: MDC_AOP2 [CHV, BSW]	
Specifies the atomic integer operation to be performed.		

## MSD1W\_A64\_QWAI2 - A64 Qword Untyped Atomic Integer Binary Write Only Operation MSD

	7:0	<b>Binding Table Index</b>	
		Project:	All
		Format:	MDC_STATELESS [CHV, BSW]
		Specifies the message is stateless	

## A64 Qword Untyped Atomic Integer Ternary with Return Data Operation MSD

MSD1R_A64_QWAI3 - A64 Qword Untyped Atomic Integer Ternary with Return Data Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Atomic Operation	
Group:	Qword Untyped Atomic Integer Ternary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHF [CHV, BSW]
		The message forbids a header
18:14	<b>Message Type</b>	Default Value: 12h
		Project: All
		Format: Opcode
		A64 Untyped Atomic Integer Operation message
13	<b>Return Data Control</b>	Default Value: 1h
		Project: All
		Format: Opcode
		Specifies that return data is sent back to the thread.
12	<b>Data Width</b>	Default Value: 1h
		Project: All
		Format: Opcode
		Operations are on 64-bit integers
11:8	<b>Atomic Integer Operation</b>	Project: CHV, BSW
		Format: MDC_AOP3S [CHV, BSW]
		Specifies the atomic integer operation to be performed.

## MSD1R\_A64\_QWAI3 - A64 Qword Untyped Atomic Integer Trinary with Return Data Operation MSD

		<b>Workaround</b>	
		CMPWR_2W is not supported in A64 QWord SIMD8.	
	7:0	<b>Binding Table Index</b>	
		Project:	All
Format:		MDC_STATELESS [CHV, BSW]	
			Specifies the message is stateless



## A64 Qword Untyped Atomic Integer Trinary Write Only Operation MSD

MSD1W_A64_QWAI3 - A64 Qword Untyped Atomic Integer Trinary Write Only Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Atomic Operation	
Group:	Qword Untyped Atomic Integer Trinary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHF [CHV, BSW]
		The message forbids a header
18:14	<b>Message Type</b>	Default Value: 12h
		Project: All
		Format: Opcode
		A64 Untyped Atomic Integer Operation message
13	<b>Return Data Control</b>	Default Value: 0h
		Project: All
		Format: Opcode
		Specifies that no return data is sent back to the thread.
12	<b>Data Width</b>	Default Value: 1h
		Project: All
		Format: Opcode
		Operations are on 64-bit integers
11:8	<b>Atomic Integer Operation</b>	Project: CHV, BSW
		Format: MDC_AOP3S [CHV, BSW]
		Specifies the atomic integer operation to be performed.

## MSD1W\_A64\_QWAI3 - A64 Qword Untyped Atomic Integer Trinary Write Only Operation MSD

		<b>Workaround</b>	
		CMPWR_2W is not supported in A64 QWord SIMD8.	
	7:0	<b>Binding Table Index</b>	
		Project:	All
		Format:	MDC_STATELESS [CHV, BSW]
		Specifies the message is stateless	

## A64 Qword Untyped Atomic Integer Unary with Return Data Operation MSD

MSD1R_A64_QWAI1 - A64 Qword Untyped Atomic Integer Unary with Return Data Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Atomic Operation	
Group:	Qword Untyped Atomic Integer Unary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHF [CHV, BSW]
		The message forbids a header
18:14	<b>Message Type</b>	Default Value: 12h
		Project: All
		Format: Opcode
		A64 Untyped Atomic Integer Operation message
13	<b>Return Data Control</b>	Default Value: 1h
		Project: All
		Format: Opcode
		Specifies that return data is sent back to the thread.
12	<b>Data Width</b>	Default Value: 1h
		Project: All
		Format: Opcode
		Operations are on 64-bit integers
11:8	<b>Atomic Integer Operation</b>	Project: All
		Format: MDC_AOP1 [CHV, BSW]
		Specifies the atomic integer operation to be performed.

## MSD1R\_A64\_QWAI1 - A64 Qword Untyped Atomic Integer Unary with Return Data Operation MSD

	7:0	<b>Binding Table Index</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_STATELESS [CHV, BSW]</td> </tr> </table> <p>Specifies the message is stateless</p>	Project:	All	Format:	MDC_STATELESS [CHV, BSW]
Project:	All					
Format:	MDC_STATELESS [CHV, BSW]					

## A64 Qword Untyped Atomic Integer Unary Write Only Operation MSD

MSD1W_A64_QWAI1 - A64 Qword Untyped Atomic Integer Unary Write Only Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Atomic Operation	
Group:	Qword Untyped Atomic Integer Unary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHF [CHV, BSW]
		The message forbids a header
18:14		<b>Message Type</b>
		Default Value: 12h
		Project: All
		Format: Opcode
		A64 Untyped Atomic Integer Operation message
13		<b>Return Data Control</b>
		Default Value: 0h
		Project: All
		Format: Opcode
		Specifies that no return data is sent back to the thread.
12		<b>Data Width</b>
		Default Value: 1h
		Project: All
		Format: Opcode
		Operations are on 64-bit integers
11:8		<b>Atomic Integer Operation</b>
		Project: All
		Format: MDC_AOP1 [CHV, BSW]
		Specifies the atomic integer operation to be performed.

## MSD1W\_A64\_QWAI1 - A64 Qword Untyped Atomic Integer Unary Write Only Operation MSD

	7:0	<b>Binding Table Index</b>	
		Project:	All
		Format:	MDC_STATELESS [CHV, BSW]
		Specifies the message is stateless	

## A64 Untyped Surface Read MSD

MSD1R_A64_US - A64 Untyped Surface Read MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Surface R/W	
Group:	Scattered Untyped Surface R/W	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHF [CHV, BSW]
	Indicates that the message forbids a header	
	18:14	<b>Message Type</b>
Default Value:		11h
Project:		All
Format:		Opcode
A64 Untyped Surface Read message		
13:12	<b>SIMD Mode</b>	
	Project:	All
	Format:	MDC_SM3 [CHV, BSW]
Specifies the SIMD mode of the message (number of slots processed)		
11:8	<b>Channel Mask</b>	
	Project:	All
	Format:	MDC_CMASK [CHV, BSW]
Specifies which RGBA channels are included in the message payload.		
7:0	<b>Binding Table Index</b>	
	Project:	All
	Format:	MDC_STATELESS [CHV, BSW]
Specifies the message is stateless		

## A64 Untyped Surface Write MSD

MSD1W_A64_US - A64 Untyped Surface Write MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Surface R/W	
Group:	Scattered Untyped Surface R/W	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHF [CHV, BSW]
	Indicates that the message forbids a header	
	18:14	<b>Message Type</b>
Default Value: 19h		
Project: All		
Format: Opcode		
A64 Untyped Surface Write message		
13:12	<b>SIMD Mode</b>	
	Project: All	
	Format: MDC_SM3 [CHV, BSW]	
Specifies the SIMD mode of the message (number of slots processed)		
11:8	<b>Channel Mask</b>	
	Project: All	
	Format: MDC_UW_CMASK [CHV, BSW]	
Specifies which RGBA channels are included in the message payload.		
7:0	<b>Binding Table Index</b>	
	Project: All	
	Format: MDC_STATELESS [CHV, BSW]	
Specifies the message is stateless		



## Addition

<b>add - Addition</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
The add instruction performs component-wise addition of src0 and src1 and stores the results in dst. Addition of two floating-point numbers follows rules in add (IEEE mode) or add (ALT mode).			
Format: [(pred)] add[.cmod] (exec_size) dst src0 src1			
Programming Notes			
Use a source modifier with add to implement subtraction.			
Syntax			
[(pred)] add[.cmod] (exec_size) reg reg reg [(pred)] add[.cmod] (exec_size) reg reg imm32			
Pseudocode			
Evaluate(WrEn); for ( n = 0; n < exec_size; n++ ) { if ( WrEn.chan[n] ) { dst.chan[n] = src0.chan[n] + src1.chan[n]; } }			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	Y	Y	Y
Src Types	Dst Types	Project	
*B,*W,*D	*B,*W,*D		
*B,*W,*D	F		
F	F		
DF	DF	CHV, BSW	
HF	HF	CHV, BSW	
*B,*W,*D	HF	CHV, BSW	
*W,*D,*Q	*W,*D,*Q	CHV, BSW	
HF, F	HF, F	CHV, BSW	
DWord	Bit	Description	
0..3	127:64	<b>RegSource</b>	
		Exists If:	(([RegSource][Src1.RegFile]!='IMM')
	Format:	EU_INSTRUCTION_SOURCES_REG_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>	
Exists If:		(([ImmSource][Src1.RegFile]='IMM')	
Format:	EU_INSTRUCTION_SOURCES_REG_IMM [CHV, BSW]		

<b>add - Addition</b>		
	63:32	<b>Operand Controls</b> Format: EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]
	31:0	<b>Header</b> Format: EU_INSTRUCTION_HEADER [CHV, BSW]

## Addition with Carry

<b>addc - Addition with Carry</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
<p>The addc instruction performs component-wise addition of src0 and src1 and stores the results in dst; it also stores the carry into acc. If the operation produces a carry out, 0x00000001 is stored in acc, else 0x00000000 is stored in acc.</p>			
Format: [(pred)] addc[.cmod] (exec_size) dst src0 src1			
Restriction			
AccWrEn is required. The accumulator is an implicit destination and thus cannot be an explicit destination operand.			
Syntax			
[(pred)] addc[.cmod] (exec_size) reg reg reg [(pred)] addc[.cmod] (exec_size) reg reg imm32			
Pseudocode			
Evaluate(WrEn); for ( n = 0; n < exec_size; n++ ) { if ( WrEn.chan[n] ) { dst.chan[n] = src0.chan[n] + src1.chan[n]; acc.chan[n] = carry(src0.chan[n] + src1.chan[n]); } }			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	Y	N	N
Src Types	Dst Types		
UD	UD		
DWord	Bit	Description	
0..3	127:64	<b>RegSource</b>	
		Exists If:	([RegSource][Src1.RegFile]!='IMM')
	Format:	EU_INSTRUCTION_SOURCES_REG_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>	
Exists If:		([ImmSource][Src1.RegFile]='IMM')	
Format:	EU_INSTRUCTION_SOURCES_REG_IMM [CHV, BSW]		
63:32	<b>Operand Controls</b>		
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]	
31:0	<b>Header</b>		
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]	

# Arithmetic Shift Right

<b>asr - Arithmetic Shift Right</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
<p>Perform component-wise arithmetic right shift of the bits in src0 by the shift count indicated in src1, storing the results in dst. If src0 has a signed type, insert copies of src0's sign bit in the number of MSBs indicated by the shift count. Otherwise insert 0 bits. In QWord mode, the shift count is taken from the low six bits of src1 regardless of the src1 type and treated as an unsigned integer in the range 0 to 63. Otherwise the shift count is taken from the low five bits of src1 regardless of the src1 type and treated as an unsigned integer in the range 0 to 31. The operation uses QWord mode if src0 or dst has the Q or UQ type but not if src1 is the only operand with the Q or UQ type. For positive values, this operation is <math>src0 / 2^{shiftCount}</math> and for negative values, this operation is <math>src0 / 2^{shiftCount} - 1</math>.</p>			
Format: [(pred)] asr[.cmod] (exec_size) dst src0 src1			
Programming Notes			
If src0 is -1, the result is -1 regardless of the shift count.			
For unsigned src0 types, asr and shr produce the same result.			
Syntax			
[(pred)] asr[.cmod] (exec_size) reg reg reg [(pred)] asr[.cmod] (exec_size) reg reg imm32			
Pseudocode			
<pre>Evaluate(WrEn); for ( n = 0; n &lt; exec_size; n++ ) { if ( WrEn.channel[n] ) { shiftCnt = src0 or dst has Q or UQ type ? src1.chan[n] &amp; 0x3F : src1.chan[n] &amp; 0x1F if (src0.chan[n] &gt;= 0) { dst.chan[n] = src0.chan[n] » shiftCnt; } else { int maskLSB = pow(2, shiftCnt) - 1; if ( maskLSB &amp; src0.chan[n] == 0 ) { dst.chan[n] = sign(src0.chan[n]) * ((abs)src0.chan[n] » shiftCnt); } else { dst.chan[n] = sign(src0.chan[n]) * ((abs)src0.chan[n] » shiftCnt) - 1; } } }</pre>			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	Y	Y	Y
Src Types	Dst Types	Project	
*B,*W,*D	*B,*W,*D		
*W,*D,*Q	*W,*D,*Q	CHV, BSW	
DWord	Bit	Description	
0..3	127:64	<b>RegSource</b>	
		Exists If:	([(RegSource)][Src1.RegFile]!='IMM')
	Format:	EU_INSTRUCTION_SOURCES_REG_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>	
Exists If:		([(ImmSource)][Src1.RegFile]=='IMM')	
Format:	EU_INSTRUCTION_SOURCES_REG_IMM [CHV, BSW]		

<b>asr - Arithmetic Shift Right</b>				
	63:32	<b>Operand Controls</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 15%;">Format:</td> <td>EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]</td> </tr> </table>	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]		
31:0	<b>Header</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 15%;">Format:</td> <td>EU_INSTRUCTION_HEADER [CHV, BSW]</td> </tr> </table>	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]	
Format:	EU_INSTRUCTION_HEADER [CHV, BSW]			

## Average

<b>avg - Average</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
<p>The avg instruction performs component-wise integer average of src0 and src1 and stores the results in dst. An integer average uses integer upward rounding. It is equivalent to increment one to the addition of src0 and src1 and then apply an arithmetic right shift to this intermediate value.</p>			
<p>Format: The avg instruction performs component-wise integer average of src0 and src1 and stores the results in dst. An integer average uses integer upward rounding. It is equivalent to increment one to the addition of src0 and src1 and then apply an arithmetic right shift to this intermediate value.</p>			
<b>Syntax</b>			
[[pred)] avg[.cmod] (exec_size) reg reg reg [(pred)] avg[.cmod] (exec_size) reg reg imm32			
<b>Pseudocode</b>			
Evaluate(WrEn); for ( n = 0; n < exec_size; n++ ) { if ( WrEn.chan[n] ) { dst.chan[n] = (src0.chan[n] + src1.chan[n] + 1) » 1; // Use arithmetic shift right. } }			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	Y	Y	Y
Src Types	Dst Types		
*B,*W,*D	*B,*W,*D		
DWord	Bit	Description	
0..3	127:64	<b>RegSource</b>	
		Exists If:	([RegSource][Src1.RegFile]!='IMM')
	Format:	EU_INSTRUCTION_SOURCES_REG_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>	
Exists If:		([ImmSource][Src1.RegFile]='IMM')	
Format:	EU_INSTRUCTION_SOURCES_REG_IMM [CHV, BSW]		
63:32	<b>Operand Controls</b>		
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]	
31:0	<b>Header</b>		
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]	

## Bit Field Extract

<b>bfe - Bit Field Extract</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
<p>Component-wise extract a bit field from src2 using the bit field width from src0 and the bit field offset from src1. Store the extracted bit field value in the low bits of dst and sign extend (if D type) or zero extend (if UD type). The width and offset values are from the low five bits of src0 and src1 respectively, or src0 &amp; 0x1f and src1 &amp; 0x1f. If width is zero, the result is zero. If offset + width &gt; 32 then the extracted bit field is bits offset to 31 of src2, extracting only 32 - offset bits, less than width as the bit field cannot extend past the MSB of the source value. Otherwise extract width bits extending from bit positions offset to offset + width - 1.</p>			
Format: [(pred)] bfe (exec_size) dst src0 src1 src2			
Restriction			
No accumulator access, implicit or explicit.			
All three-source instructions have certain restrictions, described in Instruction Formats [CHV, BSW].			
Syntax			
[(pred)] bfe (exec_size) reg reg reg reg			
Pseudocode			
<pre>Evaluate(WrEn); for ( n = 0; n &lt; exec_size; n++ ) { if ( WrEn.chan[n] ) { UD width = src0.chan[n][4:0]; UD offset = src1.chan[n][4:0]; if ( width == 0 ) { dst.chan[n] = 0x00000000; } else if ( (width + offset) &lt; 32 ) { dst.chan[n] = src2.chan[n] &lt;&lt; (32 - width - offset); if (src2 is signed) { dst.chan[n] = dst.chan[n] &gt;&gt; (32 - width); // pad sign bit of dst.chan } else { dst.chan[n] = dst.chan[n] &gt;&gt; (32 - width); // pad 0 } } else { if ( src2 is signed ) { dst.chan[n] = src2.chan[n] &gt;&gt; offset; // pad sign bit } else { dst.chan[n] = src2.chan[n] &gt;&gt; offset; // pad 0 } } }</pre>			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	N	N	N
Src Types	Dst Types		
UD	UD		
D	D		
DWord	Bit	Description	
0..3	127:126	<b>Reserved</b> Format: <span style="border: 1px solid black; padding: 2px;">MBZ</span>	
	125:106	<b>Source 2</b> Format: <span style="border: 1px solid black; padding: 2px;">EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC [CHV, BSW]</span>	
	105	<b>Reserved</b> Format: <span style="border: 1px solid black; padding: 2px;">MBZ</span>	

<b>bfe - Bit Field Extract</b>		
104:85	<b>Source 1</b>	
	Format:	EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC [CHV, BSW]
84	<b>Reserved</b>	
	Format:	MBZ
83:64	<b>Source 0</b>	
	Format:	EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC [CHV, BSW]
63:56	<b>Destination Register Number</b>	
	Format:	DstRegNum [CHV, BSW]
55:53	<b>Destination Subregister Number</b>	
	Format:	DstSubRegNum[2:0]
52:49	<b>Destination Channel Enable</b>	
	Format:	ChanEn[4]
<p>Four channel enables are defined for controlling which channels are written into the destination region. These channel mask bits are applied in a modulo-four manner to all ExecSize channels. There is 1-bit Channel Enable for each channel within the group of 4. If the bit is cleared, the write for the corresponding channel is disabled. If the bit is set, the write is enabled. Mnemonics for the bit being set for the group of 4 are x, y, z, and w, respectively, where x corresponds to Channel 0 in the group and w corresponds to channel 3 in the group</p>		
48:42	<b>Reserved</b>	
	Project:	CHV, BSW
	Format:	MBZ
41:40	<b>Source 2 Modifier</b>	
	Exists If:	/// ([Property[Source Modifier] == 'true')
	Format:	SrcMod [CHV, BSW]
39:38	<b>Source 1 Modifier</b>	
	Exists If:	/// ([Property[Source Modifier] == 'true')
	Format:	SrcMod [CHV, BSW]
41:36	<b>Reserved</b>	
	Exists If:	/// ([Property[Source Modifier] == 'false')
	Format:	MBZ
37:36	<b>Source 0 Modifier</b>	
	Exists If:	/// ([Property[Source Modifier] == 'true')
	Format:	SrcMod [CHV, BSW]
35	<b>Reserved</b>	
	Format:	MBZ
34	<b>Reserved</b>	



<b>bfe - Bit Field Extract</b>			
33	<p><b>Flag Subregister Number</b> This field contains the flag subregister number for instructions with a non-zero Conditional Modifier.</p>		
32	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ		
31:0	<p><b>Header</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 25%;">Format:</td> <td style="width: 75%;">EU_INSTRUCTION_HEADER [CHV, BSW]</td> </tr> </table>	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]
Format:	EU_INSTRUCTION_HEADER [CHV, BSW]		

## Bit Field Insert 1

<b>bfi1 - Bit Field Insert 1</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
<p>The bfi1 instruction is the first instruction in a two-instruction macro for bfi (Bit Field Insert). The bfi1 instruction component-wise generates mask with control from src0 and src1 and stores the results in dst. The mask is used in the bfi2 instruction to generate the final result of bfi. Create a bit mask corresponding to the bit field width and offset in src0 and src1. Store the bit mask in dst. The mask has all bits in the bit field set to 1 and all other bits as 0. The width and offset values are from the low five bits of src0 and src1 respectively, or src0 &amp; 0x1f and src1 &amp; 0x1f. If width is zero, the result is zero. The bfi macro has four source operands: src0 - bit field width in low five bits, src1 - bit field offset/starting bit position in low five bits, src2 - bit field value to insert, using only the number of least significant bits given by width in src0, and src3 - overall value into which the bit field is inserted, providing all bits other than the inserted bits for the result value. bfi dst src0 src1 src2 src3 //            Translates to these two instructions: bfi1 dst src0 src1 bfi2 dst dst src2 src3</p>			
Format: [(pred)] bfi1 (exec_size) dst src0 src1			
Programming Notes			
No accumulator access, implicit or explicit.			
Syntax			
[(pred)] bfi1 (exec_size) reg reg reg [(pred)] bfi1 (exec_size) reg reg imm32			
Pseudocode			
Evaluate(WrEn); for ( n = 0; n < exec_size; n++ ) { if ( WrEn.chan[n] ) { UD width = src0.chan[n][4:0]; UD offset = src1.chan[n][4:0]; dst = ((1 « width) - 1) « offset; } }			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	N	N	N
Src Types	Dst Types		
UD	UD		
D	D		
DWord	Bit	Description	
0..3	127:64	<b>RegSource</b>	
		Exists If:	((RegSource)[Src1.RegFile]!='IMM')
	Format:	EU_INSTRUCTION_SOURCES_REG_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>	
Exists If:		((ImmSource)[Src1.RegFile]='IMM')	
Format:	EU_INSTRUCTION_SOURCES_REG_IMM [CHV, BSW]		

<b>bfi1 - Bit Field Insert 1</b>				
	63:32	<b>Operand Controls</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 15%;">Format:</td> <td>EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]</td> </tr> </table>	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]		
31:0	<b>Header</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 15%;">Format:</td> <td>EU_INSTRUCTION_HEADER [CHV, BSW]</td> </tr> </table>	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]	
Format:	EU_INSTRUCTION_HEADER [CHV, BSW]			

## Bit Field Insert 2

<b>bfi2 - Bit Field Insert 2</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
<p>The bfi2 instruction is the second instruction in a two-instruction macro for bfi (Bit Field Insert). The bfi2 instruction component-wise performs the bitfield insert operation on src1 and src2 based on the mask in src0. Use the mask in src0 to take a bit field value from the low bits of src1 and combine it with the value from src2 (so src2 provides all bits other than those masked out and replaced by the bit field value). Store the result in dst. The bfi macro has four source operands: src0 - bit field width in low five bits, src1 - bit field offset/starting bit position in low five bits, src2 - bit field value to insert, using only the number of least significant bits given by width in src0, and src3 - overall value into which the bit field is inserted, providing all bits other than the inserted bits for the result value. bfi dst src0 src1 src2 src3 // Translates to these two instructions: bfi1 dst src0 src1 bfi2 dst dst src2 src3</p>			
Format: [(pred)] bfi2 (exec_size) dst src0 src1 src2			
Restriction			Project
No accumulator access, implicit or explicit.			
All three-source instructions have certain restrictions, described in Instruction Formats [CHV, BSW].			CHV, BSW
Syntax			
[(pred)] bfi2 (exec_size) reg reg reg reg			
Pseudocode			
<pre>Evaluate(WrEn); for ( n = 0; n &lt; exec_size; n++ ) { if ( WrEn.chan[n] ) { UD offset = LZD(reverse(src0.chan[n]))-1; // offset is the number of LSB zero bits below the bit mask which has all 1s. // width (implied by the logic) is the number of 1 bits in the mask value, which should be all 1s. dst.chan[n] = ((src1.chan[n] &lt;&lt; offset) &amp; src0.chan[n])   (src2.chan[n] &amp; ! src0.chan[n]); }</pre>			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	N	N	N
Src Types	Dst Types		
UD	UD		
D	D		
DWord	Bit	Description	
0..3	127:126	<b>Reserved</b>	
		Format:	MBZ
	125:106	<b>Source 2</b>	
		Format:	EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC [CHV, BSW]

<b>bfi2 - Bit Field Insert 2</b>		
105	<b>Reserved</b>	Format: MBZ
104:85	<b>Source 1</b>	Format: EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC [CHV, BSW]
84	<b>Reserved</b>	Format: MBZ
83:64	<b>Source 0</b>	Format: EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC [CHV, BSW]
63:56	<b>Destination Register Number</b>	Format: DstRegNum [CHV, BSW]
55:53	<b>Destination Subregister Number</b>	Format: DstSubRegNum[2:0]
52:49	<b>Destination Channel Enable</b>	Format: ChanEn[4] Four channel enables are defined for controlling which channels are written into the destination region. These channel mask bits are applied in a modulo-four manner to all ExecSize channels. There is 1-bit Channel Enable for each channel within the group of 4. If the bit is cleared, the write for the corresponding channel is disabled. If the bit is set, the write is enabled. Mnemonics for the bit being set for the group of 4 are x, y, z, and w, respectively, where x corresponds to Channel 0 in the group and w corresponds to channel 3 in the group
48:42	<b>Reserved</b>	Format: MBZ
41:40	<b>Source 2 Modifier</b>	Exists If: <code>///<code>([Property[Source Modifier]] == 'true')</code> Format: SrcMod [CHV, BSW]</code>
39:38	<b>Source 1 Modifier</b>	Exists If: <code>///<code>([Property[Source Modifier]] == 'true')</code> Format: SrcMod [CHV, BSW]</code>
41:36	<b>Reserved</b>	Exists If: <code>///<code>([Property[Source Modifier]] == 'false')</code> Format: MBZ</code>
37:36	<b>Source 0 Modifier</b>	Exists If: <code>///<code>([Property[Source Modifier]] == 'true')</code> Format: SrcMod [CHV, BSW]</code>
35	<b>Reserved</b>	Format: MBZ

<b>bfi2 - Bit Field Insert 2</b>		
34	<b>Reserved</b>	
	Format:	MBZ
	33	<b>Flag Subregister Number</b> This field contains the flag subregister number for instructions with a non-zero Conditional Modifier.
	32	<b>Reserved</b>
	Format:	MBZ
31:0	<b>Header</b>	
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]

## Bit Field Reverse

<b>bfrev - Bit Field Reverse</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
The bfrev instruction component-wise reverses all the bits in src0 and stores the results in dst.			
Format: [(pred)] bfrev (exec_size) dst src0			
Restriction			
No accumulator access, implicit or explicit.			
Syntax			
[(pred)] bfrev (exec_size) reg reg [(pred)] bfrev (exec_size) reg imm32			
Pseudocode			
Evaluate(WrEn); for ( n = 0; n < exec_size; n++ ) { if ( WrEn.chan[n] ) { for ( idx = 0; idx < 32; idx++ ) { dst.chan[n][idx] = src0.chan[n][31-idx]; } } }			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	N	N	N
Src Types	Dst Types		
UD	UD		
DWord	Bit	Description	
0..3	127:64	<b>RegSource</b>	
		Exists If:	([Operand Controls][Src0.RegFile]!='IMM')
	Format:	EU_INSTRUCTION_SOURCES_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>	
Exists If:		([Operand Controls][Src0.RegFile]='IMM')	
Format:	EU_INSTRUCTION_SOURCES_IMM32 [CHV, BSW]		
63:32	<b>Operand Controls</b>		
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]	
31:0	<b>Header</b>		
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]	

## Branch Converging

<b>brc - Branch Converging</b>								
Project:	CHV, BSW							
Source:	Eulsa							
Length Bias:	4							
Description								
<p>The brc instruction redirects the execution forward or backward to the instruction pointed by (current IP + offset). The jump will occur if all channels are branched away. UIP should reference the instruction where all channels are expected to come together. JIP should reference the end of the innermost conditional block.</p> <p>In GEN binary, JIP and UIP use locations src1 and src0 respectively when immediate and location src0 when reg64, where reg64 is accessed as paired DWord (regioning being &lt;2;2,1&gt;). dst must be IP. When the offsets are immediate, src0 regfile must be immediate.</p> <p>Format: [(pred)] brc (exec_size) JIP UIP</p>								
Restriction								
A brc instruction cannot use the Switch instruction option.								
Syntax								
[(pred)] brc (exec_size) imm32 imm32 [(pred)] brc (exec_size) reg64								
Pseudocode								
<pre>Evaluate(WrEn); for ( n = 0; n &lt; 32; n++ ) { if ( WrEn[n] ) { PclP[n] = IP + UIP; } else { PclP[n] = IP + 1; } } if ( all PclP != IP + 1 ) { // for all channels Jump(IP + JIP); }</pre>								
Errata	Description							
	A brc instruction must not be followed by any instruction requiring register indirect access on source operands.							
Predication	Conditional Modifier	Saturation	Source Modifier	Src Types				
Y	N	N	N	D				
DWord	Bit	Description						
0..3	127:96	<b>JIP</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>S31</td> </tr> </table> <p>The byte-aligned jump distance if a jump is taken for the channel.</p>			Project:	CHV, BSW	Format:	S31
	Project:	CHV, BSW						
Format:	S31							
95:64	<b>UIP</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>S31</td> </tr> </table> <p>The byte aligned jump distance if a jump is taken for the instruction.</p>			Project:	CHV, BSW	Format:	S31	
Project:	CHV, BSW							
Format:	S31							



<b>brc - Branch Converging</b>		
	63:32	<b>Operand Control</b> Format: EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]
	31:0	<b>Header</b> Format: EU_INSTRUCTION_HEADER [CHV, BSW]

## Branch Diverging

<b>brd - Branch Diverging</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
Description			
The brd instruction redirects the execution forward or backward to the instruction pointed by (current IP + offset). The jump will occur if any channels are branched away.			
In GEN binary, JIP is at location src1 when immediate and at location src0 when reg32, where reg32 is accessed as a scalar DWord. The ip register must be used (for example, by the assembler) as dst.			
Format: [(pred)] brd (exec_size) JIP			
Restriction			Project
A brd instruction cannot use the Switch instruction option.			CHV, BSW
Syntax			Project
[(pred)] brd (exec_size) imm32 [(pred)] brd (exec_size) reg32			CHV, BSW
Pseudocode			
Evaluate(WrEn); for ( n = 0; n < 32; n++ ) { if ( WrEn[n] ) { PclP[n] = IP + JIP; } else { PclP[n] = IP + 1; } } if ( any PclP == ExIP + JIP ) { // any channel Jump(ExIP + JIP); }			
Errata	Description		Project
	A brd instruction must not be followed by any instruction requiring register indirect access on source operands.		CHV, BSW
Predication	Conditional Modifier	Saturation	Source Modifier
Y	N	N	N
Src Types			
D			
DWord	Bit	Description	
0..3	127:96	<b>JIP</b>	
		Project:	CHV, BSW
		Format:	S31
		Jump Target Offset. The relative offset in bytes if a jump is taken for the instruction.	
	95	<b>Source 0 Address Immediate [9] Sign Bit</b>	
		Project:	CHV, BSW

<b>brd - Branch Diverging</b>		
94:91	<b>Src1.SrcType</b>	
	Project:	CHV, BSW
	Format:	SrcType [CHV, BSW]
90:89	<b>Src1.RegFile</b>	
	Project:	CHV, BSW
	Format:	RegFile [CHV, BSW]
88:64	<b>Source 0</b>	
	Exists If:	(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]== 'Align16')
	Format:	EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN16 [CHV, BSW]
88:64	<b>Source 0</b>	
	Exists If:	(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]== 'Align1')
	Format:	EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN1 [CHV, BSW]
63:32	<b>Operand Control</b>	
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]
31:0	<b>Header</b>	
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]

# Break

<b>break - Break</b>							
Project:	CHV, BSW						
Source:	Eulsa						
Length Bias:	4						
Description							
<p>The break instruction is used to early-out from the inner most loop, or early out from the inner most switch block. When used in a loop, upon execution, the break instruction terminates the loop for all execution channels enabled. If all the enabled channels hit the break instruction, jump to the instruction referenced by JIP. JIP should be the offset to the end of the inner most conditional or loop block, UIP should be the offset to the while instruction of the loop block. If SPF is ON, the UIP must be used to update IP; JIP is not used in this case</p> <p>The following table describes the two 32-bit instruction pointer offsets. Both the JIP and UIP are signed 32-bit numbers, added to IP pre-increment. In GEN binary, JIP and UIP are at locations src0 and src1 and must be of type DW (signed DWord integer). When the offsets are immediate, src0 regfile must be immediate.</p> <p>Format: [(pred)] break (exec_size) JIP UIP</p>							
Restriction							
The execution size of break instruction must be same as execution size of the corresponding while instruction.							
The execution size of break instruction must be same as execution size of the corresponding while instruction.							
Syntax		Project					
[(pred)] break (exec_size) imm16 imm16		CHV, BSW					
Pseudocode							
Evaluate(WrEn); for ( n = 0; n < exec_size; n++ ) { if ( WrEn.channel[n] ) { PclP[n] = IP + UIP; else { PclP[n] = IP + 1; } } if ( PclP != (IP + 1) ) { // all channels Jump(IP + JIP); }							
Errata	Description		Project				
	A break instruction must not be followed by any instruction requiring register indirect access on source operands.		CHV, BSW				
Predication	Conditional Modifier	Saturation	Source Modifier				
Y	N	N	N				
DWord	Bit	Description					
0..3	127:96	<b>JIP</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>S31</td> </tr> </table> <p>The byte-aligned jump distance if a jump is taken for the channel.</p>		Project:	CHV, BSW	Format:	S31
Project:	CHV, BSW						
Format:	S31						

<b>break - Break</b>						
	95:64	<p><b>UIP</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>S31</td> </tr> </table> <p>The byte aligned jump distance if a jump is taken for the instruction.</p>	Project:	CHV, BSW	Format:	S31
	Project:	CHV, BSW				
	Format:	S31				
63:32	<p><b>Operand Control</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 20%;">Format:</td> <td>EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]</td> </tr> </table>	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]			
Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]					
31:0	<p><b>Header</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 20%;">Format:</td> <td>EU_INSTRUCTION_HEADER [CHV, BSW]</td> </tr> </table>	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]			
Format:	EU_INSTRUCTION_HEADER [CHV, BSW]					

## Byte Scattered Read MSD

<b>MSDOR_BS - Byte Scattered Read MSD</b>		
Project:	CHV, BSW	
Source:	DataPort 0	
Length Bias:	1	
Family:	Scattered R/W	
Group:	Byte Scattered R/W	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: Enable
	If set, indicates that the message includes the header.	
	18	<b>Legacy Message</b>
		Default Value: 0h
Project: All		
Format: Opcode		
Legacy Message		
17:14	<b>Message Type</b>	
	Default Value: 04h	
	Project: All	
	Format: Opcode	
Byte Scattered Read message		
13	<b>Reserved</b>	
	Project: CHV, BSW	
	Format: MBZ	
Ignored		
12	<b>Reserved</b>	
	Project: All	
	Format: MBZ	
Ignored		
11:10	<b>Data Elements</b>	
	Project: All	
	Format: MDC_DS [CHV, BSW]	
Specifies the number of Bytes to be read or written per Dword		

<b>MSDOR_BS - Byte Scattered Read MSD</b>		
	9	<b>Reserved</b>
		Project: All
		Format: MBZ
		Ignored
	8	<b>SIMD Mode</b>
		Project: All
		Format: MDC_SM2 [CHV, BSW]
		Specifies the SIMD mode of the message (number of slots processed)
	7:0	<b>Binding Table Index</b>
		Project: All
Format: MDC_BTS_SLM_A32 [CHV, BSW]		
Specifies the Binding Table Index for the message		

## Byte Scattered Write MSD

<b>MSD0W_BS - Byte Scattered Write MSD</b>		
Project:	CHV, BSW	
Source:	DataPort 0	
Length Bias:	1	
Family:	Scattered R/W	
Group:	Byte Scattered R/W	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: Enable
	If set, indicates that the message includes the header.	
	18	<b>Legacy Message</b>
		Default Value: 0h
Project: All		
Format: Opcode		
Legacy Message		
17:14	<b>Message Type</b>	
	Default Value: 0Ch	
	Project: All	
	Format: Opcode	
Byte Scattered Write message		
13:12	<b>Reserved</b>	
	Project: All	
	Format: MBZ	
Ignored		
11:10	<b>Data Elements</b>	
	Project: All	
	Format: MDC_DS [CHV, BSW]	
Specifies the number of Bytes to be read or written per Dword		
9	<b>Reserved</b>	
	Project: All	
	Format: MBZ	
Ignored		



<b>MSD0W_BS - Byte Scattered Write MSD</b>						
	8	<p><b>SIMD Mode</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_SM2 [CHV, BSW]</td> </tr> </table> <p>Specifies the SIMD mode of the message (number of slots processed)</p>	Project:	All	Format:	MDC_SM2 [CHV, BSW]
	Project:	All				
Format:	MDC_SM2 [CHV, BSW]					
	7:0	<p><b>Binding Table Index</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_BTS_SLM_A32 [CHV, BSW]</td> </tr> </table> <p>Specifies the Binding Table Index for the message</p>	Project:	All	Format:	MDC_BTS_SLM_A32 [CHV, BSW]
Project:	All					
Format:	MDC_BTS_SLM_A32 [CHV, BSW]					

# Call

<b>call - Call</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
Description			
<p>The call instruction jumps to a subroutine. It can be predicated or non-predicated. If non-predicated, all enabled channels jump to the subroutine. If predicated, only the channels enabled by PMask jump to the subroutine; the rest of the channels move to the next instruction after the call instruction. If none of the channels jump into the subroutine, the call instruction is treated as a nop. In case of a jump, the call instruction stores the return IP onto the first DWord of the destination register and stores the CallMask in the second DWord of the destination register. When SPF is on, the predication control must be scalar.</p> <p>The following table describes JIP, the jump offset. JIP can be an immediate or register value. When a jump occurs, this value is added to IP pre-increment. For CHV, BSW, in GEN binary, JIP is at location src1 when immediate and at location src0 when in a register. The IP register must be put (for example, by the assembler) at dst location. When offsets are immediate, src0 must be null.</p> <p>Format: [(pred)] call (exec_size) dst JIP</p>			
Restriction			
The call instruction must have DWord source and destination type, and the destination must be QWord aligned.			
A call instruction must use a Switch			
A call instruction must be followed by an instruction that supports Switch. When call takes a jump, the first instruction must have a Switch.			
Syntax			
[(pred)] call (exec_size) reg imm32 [(pred)] call (exec_size) reg reg32			
Pseudocode			
<pre>Evaluate(WrEn); for ( n = 0; n &lt; exec_size; n++ ) { if (WrEn.chan[n] ) { PclP[n] = IP + JIP; CallMask[n] = 1; } else { PclP[n] = IP + 1; CallMask[n] = 0; } } if ( PclP[n] != (IP + 1) ) { // any channel jumped dst.chan[0] = IP + 1; dst.chan[1] = CallMask; Jump(IP + JIP); }</pre>			
Errata	Description		
	A call instruction must not be followed by any instruction requiring register indirect access on source operands.		
Predication	Conditional Modifier	Saturation	Source Modifier
Y	N	N	N
Dst Types			
D, UD			

DWord	Bit	Description	
0..3	127:96	<b>JIP</b>	
		Project: CHV, BSW	
		Format: S31	
			Jump Target Offset. The relative offset in bytes if a jump is taken for the instruction.
	95	<b>Source 0 Address Immediate [9] Sign Bit</b>	
		Project: CHV, BSW	
	94:91	<b>Src1.SrcType</b>	
		Project: CHV, BSW	
		Format: SrcType [CHV, BSW]	
	90:89	<b>Src1.RegFile</b>	
Project: CHV, BSW			
Format: RegFile [CHV, BSW]			
88:64	<b>Source 0</b>		
	Exists If: (Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]='Align16')		
	Format: EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN16 [CHV, BSW]		
88:64	<b>Source 0</b>		
	Exists If: (Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]='Align1')		
	Format: EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN1 [CHV, BSW]		
63:32	<b>Operand Control</b>		
	Format: EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]		
31:0	<b>Header</b>		
	Format: EU_INSTRUCTION_HEADER [CHV, BSW]		

## Call Absolute

<b>calla - Call Absolute</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
<p>The calla instruction jumps to a subroutine. It can be predicated or non-predicated. If non-predicated, all enabled channels jump to the subroutine. If predicated, only the channels enabled by PMask jump to the subroutine; the rest of the channels move to the next instruction after the calla instruction. If none of the channels jump into the subroutine, the calla instruction is treated as a nop. In case of a jump, the call instruction stores the return IP onto the first DWord of the destination register and stores the CallMask in the second DWord of the destination register. If SPF is ON, none of the PclP are updated. When SPF is on, the predication control must be scalar. The difference between calla and call is that calla uses JIP as the IP value rather than adding it to the IP value.</p>			
Format: [(pred)] calla (exec_size) dst JIP			
<b>Restriction</b>			
The calla instruction must have DWord source and destination type, and the destination must be QWord-aligned.			
The src0 regioning control must be <2;2,1>			
<b>Syntax</b>		<b>Project</b>	
[(pred)] calla (exec_size) reg imm32		CHV, BSW	
<b>Pseudocode</b>			
<pre>Evaluate(WrEn); for ( n = 0; n &lt; exec_size; n++ ) { if ( WrEn.channel[n] ) { PclP[n] = JIP; CallMask[n] = 1; } else { PclP[n] = IP + 1; CallMask[n] = 0; } } if ( PclP[n] != (IP + 1) ) { // any channel jumped dst.chan[0] = IP + 1; dst.chan[1] = CallMask; Jump(JIP); }</pre>			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	N	N	N
<b>Dst Types</b>			
D, UD			
DWord	Bit	<b>Description</b>	
0..3	127:96	<b>JIP</b>	
		Project:	CHV, BSW
		Format:	S31
		Jump Target Offset. The relative offset in bytes if a jump is taken for the instruction.	
	95	<b>Source 0 Address Immediate [9] Sign Bit</b>	
		Project:	CHV, BSW

<b>calla - Call Absolute</b>		
94:91	<b>Src1.SrcType</b>	
	Project:	CHV, BSW
	Format:	SrcType [CHV, BSW]
90:89	<b>Src1.RegFile</b>	
	Project:	CHV, BSW
	Format:	RegFile [CHV, BSW]
88:64	<b>Source 0</b>	
	Exists If:	(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]='Align16')
	Format:	EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN16 [CHV, BSW]
88:64	<b>Source 0</b>	
	Exists If:	(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]='Align1')
	Format:	EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN1 [CHV, BSW]
63:32	<b>Operand Control</b>	
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]
31:0	<b>Header</b>	
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]

## Compare

<b>cmp - Compare</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
<p>The cmp instruction performs component-wise comparison of src0 and src1 and stores the results in the selected flag register and in dst. It takes component-wise subtraction of src0 and src1, evaluating the conditional code (excluding NS signal) based on the conditional modifier, and storing the conditional bits in bit-packed form in the destination flag register and all bits of dst channels. If the dst is not null, for the enabled channels, then all bits of the destination channel will contain the flag value for the channel. When the instruction operates on packed word format, one general register may store up to 16 such comparison results. In DWord format, one general register may store up to 8 results. A conditional modifier must be specified; the conditional modifier field cannot be 0000b. The comparison does not use the NS (NaN source) signals, as described in the Creating Conditional Flags section. Accordingly the conditional modifier should not be .u (unordered). For each enabled channel 0b or 1b is assigned to the appropriate flag bit and 0/all zeros or all ones (e.g, byte 0xFF, word 0xFFFF, DWord 0xFFFFFFFF) is assigned to dst. When any source type is floating-point, the cmp instruction obeys the rules described in the tables in the Floating Point Modes section of the Data Types chapter.</p>			
Format: [(pred)] cmp[.cmod] (exec_size) dst src0 src1			
<b>Restriction</b>			
Accumulator cannot be destination, implicit or explicit. The destination must be a general register or the null register.			
<b>Syntax</b>			
[(pred)] cmp[.cmod] (exec_size) reg reg reg [(pred)] cmp[.cmod] (exec_size) reg reg imm32			
<b>Pseudocode</b>			
Evaluate(WrEn); for ( n = 0; n < exec_size; n++ ) { bitMask[n] = 0; if ( WrEn.chan[n] ) { results[n] = src0.chan[n] - src1.chan[n]; bitMask[n] = Condition(results[n]); dst.chan[n] = bitMask[n]; // All bits for dst channel } } flag# = bitMask;			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	Y	N	Y
Src Types	Dst Types	Project	
*B,*W,*D	*B,*W,*D		
*B,*W,*D	F		
F	F		
DF	DF	CHV, BSW	
HF	HF	CHV, BSW	

<b>cmp - Compare</b>		
*B,*W,*D	HF	CHV, BSW
*W,*D,*Q	*W,*D,*Q	CHV, BSW
HF, F	HF, F	CHV, BSW
DWord	Bit	Description
0..3	127:64	<b>RegSource</b>
		Exists If: ([RegSource][Src1.RegFile]!='IMM')
	Format: EU_INSTRUCTION_SOURCES_REG_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>
Exists If: ([ImmSource][Src1.RegFile]=='IMM')		
Format: EU_INSTRUCTION_SOURCES_REG_IMM [CHV, BSW]		
63:32	<b>Operand Controls</b>	
	Format: EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]	
31:0	<b>Header</b>	
	Format: EU_INSTRUCTION_HEADER [CHV, BSW]	

# Compare NaN

cmpn - Compare NaN			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
<p>The cmpn instruction performs component-wise special-NaN comparison of src0 and src1 and stores the results in the selected flag register and in dst. It takes component-wise subtraction of src0 and src1, evaluating the conditional signals including NS based on the conditional modifier, and storing the conditional flag bits in bit-packed form in the destination flag register and all bits of dst channels. If the dst is not null, for the enabled channels, then all bits of the destination channel will contain the flag value for the channel. When the instruction operates on packed word format, one general register may store up to 16 such comparison results. In DWord format, one general register may store up to 8 results. A conditional modifier must be specified; the conditional modifier field cannot be 0000b. More information about the conditional signals used is in the Creating Conditional Flags section. For each enabled channel 0b or 1b is assigned to the appropriate flag bit and 0/all zeros or all ones (e.g, byte 0xFF, word 0xFFFF, DWord 0xFFFFFFFF) is assigned to dst. Min/Max instructions use cmpn to select the destination from the input sources (see the Min Max of Floating Point Numbers section for details).</p>			
<p>Format: [(pred)] cmpn[.cmod] (exec_size) dst src0 src1</p>			
Restriction			
<p>Accumulator cannot be destination, implicit or explicit. The destination must be a general register or the null register.</p>			
<p>.l and .ge are the only two conditional modifiers are supported for this instruction.</p>			
Syntax			
<p>[(pred)] cmpn[.cmod] (exec_size) reg reg reg [(pred)] cmpn[.cmod] (exec_size) reg reg imm32</p>			
Pseudocode			
<pre>Evaluate(WrEn); for ( n = 0; n &lt; exec_size; n++ ) { bitMask[n] = 0; if ( WrEn.chan[n] ) { results[n] = src0.chan[n] - src1.chan[n]; bitMask[n] = ConditionNaN(results[n]); dst.chan[n][0] = bitMask[n]; // All bits for dst channel } } flag# = bitMask;</pre>			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	Y	N	Y
Src Types	Dst Types	Project	
*B,*W,*D	*B,*W,*D		
*B,*W,*D	F		
F	F		
DF	DF	CHV, BSW	
HF	HF	CHV, BSW	



DWord	Bit	Description
0..3	127:64	<b>RegSource</b>
		Exists If: ([RegSource][Src1.RegFile]!='IMM')
	Format: EU_INSTRUCTION_SOURCES_REG_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>
		Exists If: ([ImmSource][Src1.RegFile]=='IMM')
	Format: EU_INSTRUCTION_SOURCES_REG_IMM [CHV, BSW]	
	63:32	<b>Operand Controls</b>
		Format: EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]
31:0	<b>Header</b>	
	Format: EU_INSTRUCTION_HEADER [CHV, BSW]	

## Conditional Select

<b>csel - Conditional Select</b>					
Project:	CHV, BSW				
Source:	Eulsa				
Length Bias:	4				
<p>The csel instruction selectively moves components in src0 or src1 to the dst based on the result of the compare of src2 with zero. If the channel condition is true, data in src0 is moved into dst. Otherwise, data in src1 is moved into dst. The csel instruction provides the function of a cmp followed by sel. The instruction must not be used if cmpn is required. The instruction does not update the flag register.</p> <p>The comparison follows the same rule as cmp instruction for that data type.</p>					
Format: csel (exec_size) dst src0 src1 src2					
Syntax					
csel[.cmod] (exec_size) reg reg reg					
Pseudocode					
<pre>Evaluate(WrEn); for ( n = 0; n &lt; exec_size; n++ ) { bitMask[n] = 0; if ( EMask.chan[n] ) { result[n] = src2.chan[n] - 0; bitMask[n] = Condition(result[n]); if (bitMask[n] = 1) { dst.chan[n] = src0.chan[n]; } else { dst.chan[n] = src1.chan[n]; } } }</pre>					
Predication	Conditional Modifier	Saturation	Source Modifier		
N	Y	Y	Y		
Src Types	Dst Types				
F	F				
DWord	Bit	Description			
0..3	127:126	<b>Reserved</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td style="width: 100px; text-align: center;">MBZ</td></tr></table>			MBZ
		MBZ			
	125:106	<b>Source 2</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td style="width: 200px; text-align: center;">EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC [CHV, BSW]</td></tr></table>			EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC [CHV, BSW]
		EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC [CHV, BSW]			
	105	<b>Reserved</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td style="width: 100px; text-align: center;">MBZ</td></tr></table>			MBZ
		MBZ			
104:85	<b>Source 1</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td style="width: 200px; text-align: center;">EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC [CHV, BSW]</td></tr></table>			EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC [CHV, BSW]	
	EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC [CHV, BSW]				
84	<b>Reserved</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td style="width: 100px; text-align: center;">MBZ</td></tr></table>			MBZ	
	MBZ				
83:64	<b>Source 0</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td style="width: 200px; text-align: center;">EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC [CHV, BSW]</td></tr></table>			EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC [CHV, BSW]	
	EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC [CHV, BSW]				

<b>csel - Conditional Select</b>		
63:56	<b>Destination Register Number</b>	
	Format:	DstRegNum [CHV, BSW]
55:53	<b>Destination Subregister Number</b>	
	Format:	DstSubRegNum[2:0]
52:49	<b>Destination Channel Enable</b>	
	Format:	ChanEn[4]
<p>Four channel enables are defined for controlling which channels are written into the destination region. These channel mask bits are applied in a modulo-four manner to all ExecSize channels. There is 1-bit Channel Enable for each channel within the group of 4. If the bit is cleared, the write for the corresponding channel is disabled. If the bit is set, the write is enabled. Mnemonics for the bit being set for the group of 4 are x, y, z, and w, respectively, where x corresponds to Channel 0 in the group and w corresponds to channel 3 in the group</p>		
48:42	<b>Reserved</b>	
	Format:	MBZ
41:40	<b>Source 2 Modifier</b>	
	Exists If:	//([Property[Source Modifier]== 'true')
	Format:	SrcMod [CHV, BSW]
39:38	<b>Source 1 Modifier</b>	
	Exists If:	//([Property[Source Modifier]== 'true')
	Format:	SrcMod [CHV, BSW]
41:36	<b>Reserved</b>	
	Exists If:	//([Property[Source Modifier]== 'false')
	Format:	MBZ
37:36	<b>Source 0 Modifier</b>	
	Exists If:	//([Property[Source Modifier]== 'true')
	Format:	SrcMod [CHV, BSW]
35	<b>Reserved</b>	
	Format:	MBZ
34	<b>Reserved</b>	
	Format:	MBZ
33	<b>Flag Subregister Number</b>	
	This field contains the flag subregister number for instructions with a non-zero Conditional Modifier.	
32	<b>Reserved</b>	
	Format:	MBZ
31:0	<b>Header</b>	
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]

## Conditional Send Message

<b>sendc - Conditional Send Message</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
<p>The sendc instruction has the same behavior as the send instruction except the following. sendc first checks the dependent threads inside the Thread Dependency Register. There are up to 8 dependent threads in the TDR register. The sendc instruction executes only when all the dependent threads in the TDR register are retired. Wait for dependencies in the TDR Register to clear, then send a message stored in registers starting at src to a shared function identified by exdesc along with control from desc with a general register writeback location at dst.</p>			
Format: [(pred)] sendc (exec_size) dst src0 exdesc desc			
Restriction			
The sendc instruction has the same restrictions as the send instruction.			
Pseudocode			
<pre>if ( TDR[7] ...    TDR[2]    TDR[1]    TDR[0] ) { wait; } Evaluate(WrEn); MsgChEnable = WrEn; SourceReg = src0.RegNum; MessageEnqueue(MsgChEnable, ResponseReg, SourceReg, desc, exdesc);</pre>			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	N	N	N
DWord	Bit	Description	
0..3	127:96	<b>Message</b>	
		Format:	EU_INSTRUCTION_OPERAND_SEND_MSG [CHV, BSW]
	95:89	<b>Flags</b>	
		Format:	EU_INSTRUCTION_FLAGS
	88:64	<b>Source 0</b>	
		Exists If:	(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]== 'Align1')
	Format:	EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN1 [CHV, BSW]	
88:64	<b>Source 0</b>		
	Exists If:	(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]== 'Align16')	
	Format:	EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN16 [CHV, BSW]	
63:32	<b>Operand Control</b>		
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]	
31:28	<b>Controls B</b>		
	Format:	EU_INSTRUCTION_CONTROLS_B [CHV, BSW]	

<b>sendc - Conditional Send Message</b>		
	27:24	<b>Shared Function ID (SFID)</b>
		Format: SFID [CHV, BSW]
	23:8	<b>Controls A</b>
		Format: EU_INSTRUCTION_CONTROLS_A [CHV, BSW]
	7	<b>Reserved</b>
		Format: MBZ
	6:0	<b>Opcode</b>
		Format: EU_OPCODE [CHV, BSW]

## Constant Cache Dword Scattered Read MSD

MSD_CC_DWS - Constant Cache Dword Scattered Read MSD							
Project:	CHV, BSW						
Source:	Read-Only DataPort						
Length Bias:	1						
Family:	Scattered R/W						
Group:	DW Scattered R/W						
DWord	Bit	Description					
0	19	<b>Header Present</b>					
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>If set, indicates that the message includes the header.</p>	Project:	All	Format:	Enable	
	Project:	All					
	Format:	Enable					
	18	<b>Legacy Message</b>					
		<table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Legacy Message</p>	Default Value:	0h	Project:	All	Format:
Default Value:		0h					
Project:	All						
Format:	Opcode						
<table border="1"> <tr> <td>Default Value:</td> <td>03h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Dword Scattered Read message</p>	Default Value:	03h	Project:	All	Format:	Opcode	
Default Value:	03h						
Project:	All						
Format:	Opcode						
13	<b>Invalidate After Read</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_IAR [CHV, BSW]</td> </tr> </table> <p>Specifies if L3 cache lines accessed by the message should be invalidated after the read occurs</p>	Project:	All	Format:	MDC_IAR [CHV, BSW]		
Project:	All						
Format:	MDC_IAR [CHV, BSW]						
12	<b>Reserved</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>Ignored</p>	Project:	All	Format:	MBZ		
Project:	All						
Format:	MBZ						
11:10	<b>Reserved</b>						
	<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ		
Project:	CHV, BSW						
Format:	MBZ						

## MSD\_CC\_DWS - Constant Cache Dword Scattered Read MSD

9	<b>Legacy SIMD Mode</b>	
	Default Value:	1h
	Project:	All
	Format:	Opcode
	Must be set for compatibility.	
8	<b>SIMD Mode</b>	
	Project:	All
	Format:	MDC_SM2 [CHV, BSW]
	Specifies the SIMD mode of the message (number of slots processed)	
7:0	<b>Binding Table Index</b>	
	Project:	All
	Format:	MDC_BTS [CHV, BSW]
	Specifies the Binding Table Index for the message	

## Constant Cache Oword Block Read MSD

MSD_CC_OWB - Constant Cache Oword Block Read MSD		
Project:	CHV, BSW	
Source:	Read-Only DataPort	
Length Bias:	1	
Family:	Block R/W	
Group:	OW Block R/W	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHR [CHV, BSW]
	Indicates that the message requires a header.	
	18	<b>Reserved</b>
		Project: All
Format: MBZ		
Ignored		
17:14	<b>Message Type</b>	
	Default Value: 00h	
	Project: All	
	Format: Opcode	
Oword Block Read Constant Cache message		
13	<b>Invalidate After Read</b>	
	Project: All	
	Format: MDC_IAR [CHV, BSW]	
Specifies if L3 cache lines accessed by the message should be invalidated after the read occurs		
12:11	<b>Reserved</b>	
	Project: All	
	Format: MBZ	
Ignored		
10:8	<b>Data Elements</b>	
	Project: All	
	Format: MDC_DB_OW [CHV, BSW]	
Specifies the number of contiguous Owords to be read or written		



## MSD\_CC\_OWB - Constant Cache Oword Block Read MSD

	7:0	<b>Binding Table Index</b>	
		Project:	All
		Format:	MDC_BTS [CHV, BSW]
		Specifies the Binding Table Index for the message	

## Constant Cache Oword Dual Block Read MSD

MSD_CC_OWDB - Constant Cache Oword Dual Block Read MSD							
Project:	CHV, BSW						
Source:	Read-Only DataPort						
Length Bias:	1						
Family:	Block R/W						
Group:	OW Dual Block R/W						
DWord	Bit	Description					
0	19	<b>Header Present</b>					
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>If set, indicates that the message includes the header.</p>	Project:	All	Format:	Enable	
	Project:	All					
	Format:	Enable					
	18	<b>Reserved</b>					
<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>Ignored</p>		Project:	All	Format:	MBZ		
Project:	All						
Format:	MBZ						
17:14	<b>Message Type</b>						
	<table border="1"> <tr> <td>Default Value:</td> <td>02h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Oword Block Read message</p>	Default Value:	02h	Project:	All	Format:	Opcode
	Default Value:	02h					
Project:	All						
Format:	Opcode						
13	<b>Invalidate After Read</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_IAR [CHV, BSW]</td> </tr> </table> <p>Specifies if L3 cache lines accessed by the message should be invalidated after the read occurs</p>	Project:	All	Format:	MDC_IAR [CHV, BSW]		
Project:	All						
Format:	MDC_IAR [CHV, BSW]						
12:10	<b>Reserved</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>Ignored</p>	Project:	All	Format:	MBZ		
Project:	All						
Format:	MBZ						
9:8	<b>Data Elements</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_DB_OWD [CHV, BSW]</td> </tr> </table> <p>Specifies the number of contiguous Owords to be read or written</p>	Project:	All	Format:	MDC_DB_OWD [CHV, BSW]		
Project:	All						
Format:	MDC_DB_OWD [CHV, BSW]						

## MSD\_CC\_OWDB - Constant Cache Oword Dual Block Read MSD

	7:0	<b>Binding Table Index</b>	
		Project:	All
		Format:	MDC_BTS [CHV, BSW]
		Specifies the Binding Table Index for the message	

## Constant Cache Oword Unaligned Block Read MSD

MSD_CC_OWUB - Constant Cache Oword Unaligned Block Read MSD							
Project:	CHV, BSW						
Source:	Read-Only DataPort						
Length Bias:	1						
Family:	Block R/W						
Group:	OW Unaligned Block R/W						
DWord	Bit	Description					
0	19	<b>Header Present</b>					
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_MHR [CHV, BSW]</td> </tr> </table> <p>Indicates that the message requires a header.</p>	Project:	All	Format:	MDC_MHR [CHV, BSW]	
	Project:	All					
	Format:	MDC_MHR [CHV, BSW]					
	18	<b>Reserved</b>					
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>Ignored</p>	Project:	All	Format:	MBZ	
Project:	All						
Format:	MBZ						
17:14	<b>Message Type</b>						
	<table border="1"> <tr> <td>Default Value:</td> <td>01h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Oword Unaligned Block Read Constant Cache message</p>	Default Value:	01h	Project:	All	Format:	Opcode
	Default Value:	01h					
Project:	All						
Format:	Opcode						
<b>Reserved</b>							
13:11	<b>Reserved</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>Ignored</p>	Project:	All	Format:	MBZ		
Project:	All						
Format:	MBZ						
10:8	<b>Data Elements</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_DB_OW [CHV, BSW]</td> </tr> </table> <p>Specifies the number of contiguous Owords to be read</p>	Project:	All	Format:	MDC_DB_OW [CHV, BSW]		
Project:	All						
Format:	MDC_DB_OW [CHV, BSW]						
7:0	<b>Binding Table Index</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_BTS [CHV, BSW]</td> </tr> </table> <p>Specifies the Binding Table Index for the message</p>	Project:	All	Format:	MDC_BTS [CHV, BSW]		
Project:	All						
Format:	MDC_BTS [CHV, BSW]						

## Continue

<b>cont - Continue</b>							
Project:	CHV, BSW						
Source:	Eulsa						
Length Bias:	4						
Description							
<p>The cont instruction disables execution for the subset of channels for the remainder of the current loop iteration. Channels remain disabled until right before the while instruction or right before the condition check code block for the while instruction. If all enabled channels hit this instruction, jump to the instruction referenced by JIP where execution continues. UIP should always reference the loop's associated while instruction. JIP should point to the last instruction of the inner most conditional block if the cont instruction is inside a conditional block. In case of the break instruction directly under the loop, the JIP and the UIP are the same. If SPF is ON, the UIP must be used to update IP; JIP is not used in this case.</p> <p>The following table describes the two 32-bit instruction pointer offsets. Both the JIP and UIP are signed 32-bit numbers, added to IP pre-increment. In GEN binary, JIP and UIP are at locations src0 and src1 and must be of type DW (signed DWord integer). When the offsets are immediate, src0 regfile must be immediate.</p> <p>Format: [(pred)] cont (exec_size) JIP UIP</p>							
Restriction							
The execution size must be the same for the while, break, and cont instructions of the same code block.							
Syntax							
[(pred)] cont (exec_size) imm32 imm32							
Pseudocode							
<pre>Evaluate(WrEn); for ( n = 0; n &lt; exec_size; n++ ) { if ( WrEn.channel[n] ) { if ( PMask[n] ) { // PMask is for all channels enabled for the cont instruction. PclP[n] = IP + UIP; } else { PclP[n] = IP + 1; } } } for ( n = exec_size; n &lt; 32; n++ ) { PclP[n] = IP + 1; } if ( PclP != (IP + 1) ) { // all channels true Jump(IP + JIP); }</pre>							
Errata	Description						
	A cont instruction must not be followed by any instruction requiring register indirect access on source operands.						
Predication	Conditional Modifier	Saturation	Source Modifier				
Y	N	N	N				
DWord	Bit	Description					
0..3	127:96	<b>JIP</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>S31</td> </tr> </table> <p>The byte-aligned jump distance if a jump is taken for the channel.</p>		Project:	CHV, BSW	Format:	S31
Project:	CHV, BSW						
Format:	S31						

<b>cont - Continue</b>						
	95:64	<p><b>UIP</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>S31</td> </tr> </table> <p>The byte aligned jump distance if a jump is taken for the instruction.</p>	Project:	CHV, BSW	Format:	S31
	Project:	CHV, BSW				
	Format:	S31				
63:32	<p><b>Operand Control</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 20%;">Format:</td> <td>EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]</td> </tr> </table>	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]			
Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]					
31:0	<p><b>Header</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 20%;">Format:</td> <td>EU_INSTRUCTION_HEADER [CHV, BSW]</td> </tr> </table>	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]			
Format:	EU_INSTRUCTION_HEADER [CHV, BSW]					

## Count Bits Set

<b>cbit - Count Bits Set</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
The cbit instruction counts component-wise the total bits set in src0 and stores the resulting counts in dst.			
Format: [(pred)] cbit (exec_size) dst src0			
Restriction			
No accumulator access, implicit or explicit.			
Syntax			
[(pred)] cbit (exec_size) reg reg [(pred)] cbit (exec_size) reg imm32			
Pseudocode			
Evaluate(WrEn); for ( n = 0; n < exec_size; n++ ) { if ( WrEn.chan[n] ) { UD cnt = 0; UD val = src0.chan[n]; while ( val ) { if ( val & 1 ) { cnt ++; } val = val >> 1; } dst.chan[n] = cnt; } }			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	N	N	N
Src Types	Dst Types		
UB, UW, UD	UD		
DWord	Bit	Description	
0..3	127:64	<b>RegSource</b>	
		Exists If:	((Operand Controls)[Src0.RegFile]!='IMM')
	Format:	EU_INSTRUCTION_SOURCES_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>	
Exists If:		((Operand Controls)[Src0.RegFile]='IMM')	
Format:	EU_INSTRUCTION_SOURCES_IMM32 [CHV, BSW]		
63:32	<b>Operand Controls</b>		
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]	
31:0	<b>Header</b>		
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]	

## Dot Product 2

<b>dp2 - Dot Product 2</b>					
Project:	CHV, BSW				
Source:	Eulsa				
Length Bias:	4				
<p>The dp2 instruction performs a two-wide dot product on four-tuple vector basis and storing the same scalar result per four tuple to all four channels in dst. This instruction is similar to dp4 except that every third and fourth element of src0 (post-source-swizzle if present) are not involved in the computation. The dot product of two vectors of equal length is the sum of the products of each pair of corresponding elements. The dp4 instruction includes all four elements of each vector in the dot product. The dp3 instruction includes the first three elements of each vector in the dot product.</p>					
Format: [(pred)] dp2[.cmod] (exec_size) dst src0 src1					
Restriction					
Execution size cannot be less than 4.					
Horizontal strides must be 1.					
Source operands cannot be accumulators.					
Syntax					
[(pred)] dp2[.cmod] (exec_size) reg reg reg [(pred)] dp2[.cmod] (exec_size) reg reg imm32					
Pseudocode					
<pre>Evaluate(WrEn); for ( n = 0; n &lt; exec_size; n += 4 ) { fTmp = src0.chan[n] * src1.chan[n] + src0.chan[n+1] * src1.chan[n+1]; if ( WrEn.chan[n] ) dst.chan[n] = fTmp; if ( WrEn.chan[n+1] ) dst.chan[n+1] = fTmp; if ( WrEn.chan[n+2] ) dst.chan[n+2] = fTmp; if ( WrEn.chan[n+3] ) dst.chan[n+3] = fTmp; }</pre>					
Predication	Conditional Modifier	Saturation	Source Modifier	Src Types	Dst Types
Y	Y	Y	Y	F	F
DWord	Bit	Description			
0..3	127:64	<b>RegSource</b>			
		Exists If:	([RegSource][Src1.RegFile]!='IMM')		
	Format:	EU_INSTRUCTION_SOURCES_REG_REG [CHV, BSW]			
	127:64	<b>ImmSource</b>			
Exists If:		([ImmSource][Src1.RegFile]='IMM')			
Format:	EU_INSTRUCTION_SOURCES_REG_IMM [CHV, BSW]				
63:32	<b>Operand Controls</b>				
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]			
31:0	<b>Header</b>				
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]			



## Dot Product 3

<b>dp3 - Dot Product 3</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
<p>The dp3 instruction performs a three-wide dot product on four-tuple vector basis and storing the same scalar result per four tuple to all four channels in dst. This instruction is similar to dp4 except that every fourth element of src0 (post-source-swizzle if present) is not involved in the computation. The dot product of two vectors of equal length is the sum of the products of each pair of corresponding elements. The dp4 instruction includes all four elements of each vector in the dot product. The dp2 instruction includes the first two elements of each vector in the dot product.</p>			
Format: [(pred)] dp3[.cmod] (exec_size) dst src0 src1			
Restriction			
Execution size cannot be less than 4.			
Horizontal strides must be 1.			
Source operands cannot be accumulators.			
Syntax			
[(pred)] dp3[.cmod] (exec_size) reg reg reg [(pred)] dp3[.cmod] (exec_size) reg reg imm32			
Pseudocode			
<pre>Evaluate(WrEn); for ( n = 0; n &lt; exec_size; n += 4 ) { fTmp = src0.chan[n] * src1.chan[n] + src0.chan[n+1] * src1.chan[n+1] + src0.chan[n+2] * src1.chan[n+2]; if ( WrEn.chan[n] ) dst.chan[n] = fTmp; if ( WrEn.chan[n+1] ) dst.chan[n+1] = fTmp; if ( WrEn.chan[n+2] ) dst.chan[n+2] = fTmp; if ( WrEn.chan[n+3] ) dst.chan[n+3] = fTmp; }</pre>			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	Y	Y	Y
Src Types	Dst Types		
F	F		
DWord	Bit	Description	
0..3	127:64	<b>RegSource</b>	
		Exists If:	([RegSource][Src1.RegFile]!='IMM')
	Format:	EU_INSTRUCTION_SOURCES_REG_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>	
Exists If:		([ImmSource][Src1.RegFile]=='IMM')	
Format:	EU_INSTRUCTION_SOURCES_REG_IMM [CHV, BSW]		

<b>dp3 - Dot Product 3</b>				
	63:32	<b>Operand Controls</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 15%;">Format:</td> <td>EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]</td> </tr> </table>	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]		
31:0	<b>Header</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 15%;">Format:</td> <td>EU_INSTRUCTION_HEADER [CHV, BSW]</td> </tr> </table>	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]	
Format:	EU_INSTRUCTION_HEADER [CHV, BSW]			

## Dot Product 4

<b>dp4 - Dot Product 4</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
<p>The dp4 instruction performs a four-wide dot product on four-tuple vector basis and storing the same scalar result per four tuple to all four channels in dst. The dot product of two vectors of equal length is the sum of the products of each pair of corresponding elements.</p>			
Format: <code>[(pred)] dp4[.cmod] (exec_size) dst src0 src1</code>			
Restriction			
Execution size cannot be less than 4.			
Horizontal strides must be 1.			
Source operands cannot be accumulators.			
Syntax			
<code>[(pred)] dp4[.cmod] (exec_size) reg reg reg [(pred)] dp4[.cmod] (exec_size) reg reg imm32</code>			
Pseudocode			
<pre>Evaluate(WrEn); for ( n = 0; n &lt; exec_size; n += 4 ) { fTmp = src0.chan[n] * src1.chan[n] + src0.chan[n+1] * src1.chan[n+1] + src0.chan[n+2] * src1.chan[n+2] + src0.chan[n+3] * src1.chan[n+3]; if ( WrEn.chan[n] ) dst.chan[n] = fTmp; if ( WrEn.chan[n+1] ) dst.chan[n+1] = fTmp; if ( WrEn.chan[n+2] ) dst.chan[n+2] = fTmp; if ( WrEn.chan[n+3] ) dst.chan[n+3] = fTmp; }</pre>			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	Y	Y	Y
Src Types	Dst Types		
F	F		
DWord	Bit	Description	
0..3	127:64	<b>RegSource</b>	
		Exists If:	<code>[(RegSource)][Src1.RegFile]!='IMM'</code>
	Format:	<code>EU_INSTRUCTION_SOURCES_REG_REG [CHV, BSW]</code>	
	127:64	<b>ImmSource</b>	
Exists If:		<code>[(ImmSource)][Src1.RegFile]='IMM'</code>	
Format:	<code>EU_INSTRUCTION_SOURCES_REG_IMM [CHV, BSW]</code>		
63:32	<b>Operand Controls</b>		
Format:	<code>EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]</code>		
31:0	<b>Header</b>		
	Format:	<code>EU_INSTRUCTION_HEADER [CHV, BSW]</code>	

## Dot Product Homogeneous

<b>dph - Dot Product Homogeneous</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
<p>The dph instruction performs a four-wide homogeneous dot product on four-tuple vector basis and storing the same scalar result per four tuple to all four channels in dst. This instruction is similar to dp4 except that every fourth element of src0 (post-source-swizzle if present) is forced to 1.0f. Use the dp4 instruction to do a four-wide dot product that includes all elements of src0 and src1.</p>			
Format: [(pred)] dph[.cmod] (exec_size) dst src0 src1			
Restriction			
Execution size cannot be less than 4.			
Horizontal strides must be 1.			
Source operands cannot be accumulators.			
Syntax			
[(pred)] dph[.cmod] (exec_size) reg reg reg [(pred)] dph[.cmod] (exec_size) reg reg imm32			
Pseudocode			
<pre>Evaluate(WrEn); for ( n = 0; n &lt; exec_size; n += 4 ) { fTmp = src0.chan[n] * src1.chan[n] + src0.chan[n+1] * src1.chan[n+1] + src0.chan[n+2] * src1.chan[n+2] + src1.chan[n+3]; // Use 1.0f in place of src0.chan[n+3]. if ( WrEn.chan[n] ) dst.chan[n] = fTmp; if ( WrEn.chan[n+1] ) dst.chan[n+1] = fTmp; if ( WrEn.chan[n+2] ) dst.chan[n+2] = fTmp; if ( WrEn.chan[n+3] ) dst.chan[n+3] = fTmp; }</pre>			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	Y	Y	Y
Src Types	Dst Types		
F	F		
DWord	Bit	Description	
0..3	127:64	<b>RegSource</b>	
		Exists If:	([RegSource][Src1.RegFile]!='IMM')
	Format:		EU_INSTRUCTION_SOURCES_REG_REG [CHV, BSW]
	127:64	<b>ImmSource</b>	
Exists If:		([ImmSource][Src1.RegFile]='IMM')	
Format:		EU_INSTRUCTION_SOURCES_REG_IMM [CHV, BSW]	
63:32	<b>Operand Controls</b>		
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]	
31:0	<b>Header</b>		
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]	

## Dword Atomic Counter Binary with Return Data Operation MSD

MSD1R_DWAC2 - Dword Atomic Counter Binary with Return Data Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Atomic Operation	
Group:	Dword Atomic Counter Binary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHR [CHV, BSW]
	Indicates that the message requires a header	
	18:14	<b>Message Type</b>
		Default Value: 0Bh
Project: All		
Format: Opcode		
Atomic Counter Operation message		
13	<b>Return Data Control</b>	
	Default Value: 1h	
	Project: All	
	Format: Opcode	
Specifies that return data is sent back to the thread.		
12	<b>SIMD Mode</b>	
	Project: All	
	Format: MDC_SM2RS [CHV, BSW]	
Specifies the SIMD mode of the message (number of slots processed)		
11:8	<b>Atomic Integer Operation</b>	
	Project: All	
	Format: MDC_AOP2 [CHV, BSW]	
Specifies the atomic integer operation to be performed.		
7:0	<b>Binding Table Index</b>	
	Project: All	
	Format: MDC_BTS [CHV, BSW]	
Specifies the Binding Table Index for the message		

## Dword Atomic Counter Binary Write Only Operation MSD

<b>MSD1W_DWAC2 - Dword Atomic Counter Binary Write Only Operation MSD</b>			
Project:	CHV, BSW		
Source:	DataPort 1		
Length Bias:	1		
Family:	Untyped Atomic Operation		
Group:	Dword Atomic Counter Binary Operation		
DWord	Bit	Description	
0	19	<b>Header Present</b>	
		Project: All	
		Format: MDC_MHR [CHV, BSW]	
		Indicates that the message requires a header	
	18:14	<b>Message Type</b>	
		Default Value: 0Bh	
		Project: All	
		Format: Opcode	
			Atomic Counter Operation message
	13	<b>Return Data Control</b>	
		Default Value: 0h	
		Project: All	
Format: Opcode			
		Specifies that no return data is sent back to the thread.	
12	<b>SIMD Mode</b>		
	Project: All		
	Format: MDC_SM2RS [CHV, BSW]		
		Specifies the SIMD mode of the message (number of slots processed)	
11:8	<b>Atomic Integer Operation</b>		
	Project: All		
	Format: MDC_AOP2 [CHV, BSW]		
		Specifies the atomic integer operation to be performed.	
7:0	<b>Binding Table Index</b>		
	Project: All		
	Format: MDC_BTS [CHV, BSW]		
		Specifies the Binding Table Index for the message	

## Dword Atomic Counter Unary with Return Data Operation MSD

MSD1R_DWAC1 - Dword Atomic Counter Unary with Return Data Operation MSD			
Project:	CHV, BSW		
Source:	DataPort 1		
Length Bias:	1		
Family:	Untyped Atomic Operation		
Group:	Dword Atomic Counter Unary Operation		
DWord	Bit	Description	
0	19	<b>Header Present</b>	
		Project: All	
		Format: MDC_MHR [CHV, BSW]	
			Indicates that the message requires a header
	18:14	<b>Message Type</b>	
		Default Value: 0Bh	
		Project: All	
		Format: Opcode	
			Atomic Counter Operation message
	13	<b>Return Data Control</b>	
Default Value: 1h			
Project: All			
Format: Opcode			
		Specifies that return data is sent back to the thread.	
12	<b>SIMD Mode</b>		
	Project: All		
	Format: MDC_SM2RS [CHV, BSW]		
		Specifies the SIMD mode of the message (number of slots processed)	
11:8	<b>Atomic Integer Operation</b>		
	Project: All		
	Format: MDC_AOP1 [CHV, BSW]		
		Specifies the atomic integer operation to be performed.	
7:0	<b>Binding Table Index</b>		
	Project: All		
	Format: MDC_BTS [CHV, BSW]		
		Specifies the Binding Table Index for the message	

## Dword Atomic Counter Unary Write Only Operation MSD

<b>MSD1W_DWAC1 - Dword Atomic Counter Unary Write Only Operation MSD</b>								
Project:	CHV, BSW							
Source:	DataPort 1							
Length Bias:	1							
Family:	Untyped Atomic Operation							
Group:	Dword Atomic Counter Unary Operation							
DWord	Bit	Description						
0	19	<b>Header Present</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_MHR [CHV, BSW]</td> </tr> </table> <p>Indicates that the message requires a header</p>	Project:	All	Format:	MDC_MHR [CHV, BSW]		
	Project:	All						
	Format:	MDC_MHR [CHV, BSW]						
	18:14	<b>Message Type</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td>0Bh</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Atomic Counter Operation message</p>	Default Value:	0Bh	Project:	All	Format:	Opcode
	Default Value:	0Bh						
	Project:	All						
	Format:	Opcode						
	13	<b>Return Data Control</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td>0h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Specifies that no return data is sent back to the thread.</p>	Default Value:	0h	Project:	All	Format:	Opcode
	Default Value:	0h						
	Project:	All						
Format:	Opcode							
12	<b>SIMD Mode</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_SM2RS [CHV, BSW]</td> </tr> </table> <p>Specifies the SIMD mode of the message (number of slots processed)</p>	Project:	All	Format:	MDC_SM2RS [CHV, BSW]			
Project:	All							
Format:	MDC_SM2RS [CHV, BSW]							
11:8	<b>Atomic Integer Operation</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_AOP1 [CHV, BSW]</td> </tr> </table> <p>Specifies the atomic integer operation to be performed.</p>	Project:	All	Format:	MDC_AOP1 [CHV, BSW]			
Project:	All							
Format:	MDC_AOP1 [CHV, BSW]							
7:0	<b>Binding Table Index</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_BTS [CHV, BSW]</td> </tr> </table> <p>Specifies the Binding Table Index for the message</p>	Project:	All	Format:	MDC_BTS [CHV, BSW]			
Project:	All							
Format:	MDC_BTS [CHV, BSW]							



## Dword Scattered Read MSD

MSD0R_DWS - Dword Scattered Read MSD		
Project:	CHV, BSW	
Source:	DataPort 0	
Length Bias:	1	
Family:	Scattered R/W	
Group:	DW Scattered R/W	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: Enable
	If set, indicates that the message includes the header.	
	18	<b>Legacy Message</b>
		Default Value: 0h
Project: All		
Format: Opcode		
Legacy Message		
17:14	<b>Message Type</b>	
	Default Value: 03h	
	Project: All	
	Format: Opcode	
Dword Scattered Read message		
13	<b>Invalidate After Read</b>	
	Project: All	
	Format: MDC_IAR [CHV, BSW]	
Specifies if L3 cache lines accessed by the message should be invalidated after the read occurs		
12	<b>Reserved</b>	
	Project: All	
	Format: MBZ	
Ignored		
11:10	<b>Reserved</b>	
	Project: CHV, BSW	
	Format: MBZ	
Ignored		

<b>MSD0R_DWS - Dword Scattered Read MSD</b>			
9	<b>Legacy SIMD Mode</b>		
	Default Value:	1h	
	Project:	All	
	Format:	Opcode	
	Must be set for compatibility.		
	8	<b>SIMD Mode</b>	
		Project:	All
		Format:	MDC_SM2 [CHV, BSW]
		Specifies the SIMD mode of the message (number of slots processed)	
	7:0	<b>Binding Table Index</b>	
Project:		CHV, BSW	
Format:		MDC_BTS_A32 [CHV, BSW]	
Specifies the Binding Table Index for the message			

## Dword Scattered Write MSD

<b>MSD0W_DWS - Dword Scattered Write MSD</b>		
Project:	CHV, BSW	
Source:	DataPort 0	
Length Bias:	1	
Family:	Scattered R/W	
Group:	DW Scattered R/W	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: Enable
	If set, indicates that the message includes the header.	
	18	<b>Legacy Message</b>
		Default Value: 0h
Project: All		
Format: Opcode		
Legacy Message		
17:14	<b>Message Type</b>	
	Default Value: 0Bh	
	Project: All	
	Format: Opcode	
Dword Scattered Write message		
13:12	<b>Reserved</b>	
	Project: All	
	Format: MBZ	
Ignored		
11:10	<b>Reserved</b>	
	Project: CHV, BSW	
	Format: MBZ	
Ignored		
9	<b>Legacy SIMD Mode</b>	
	Default Value: 1h	
	Project: All	
	Format: Opcode	
Must be set for compatibility.		

<b>MSD0W_DWS - Dword Scattered Write MSD</b>						
	8	<p><b>SIMD Mode</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_SM2 [CHV, BSW]</td> </tr> </table> <p>Specifies the SIMD mode of the message (number of slots processed)</p>	Project:	All	Format:	MDC_SM2 [CHV, BSW]
	Project:	All				
Format:	MDC_SM2 [CHV, BSW]					
	7:0	<p><b>Binding Table Index</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MDC_BTS_A32 [CHV, BSW]</td> </tr> </table> <p>Specifies the Binding Table Index for the message</p>	Project:	CHV, BSW	Format:	MDC_BTS_A32 [CHV, BSW]
Project:	CHV, BSW					
Format:	MDC_BTS_A32 [CHV, BSW]					

## Dword SIMD4x2 Atomic Counter Binary with Return Data Operation MSD

MSD1R_DWAC2_4x2 - Dword SIMD4x2 Atomic Counter Binary with Return Data Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Atomic Operation	
Group:	Dword Atomic Counter Binary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHR [CHV, BSW]
	Indicates that the message requires a header	
	18:14	<b>Message Type</b>
		Default Value: 0Ch
Project: All		
Format: Opcode		
Atomic Counter Operation SIMD4x2 message		
13	<b>Return Data Control</b>	
	Default Value: 1h	
	Project: All	
	Format: Opcode	
Specifies that return data is sent back to the thread.		
12	<b>Reserved</b>	
11:8	<b>Atomic Integer Operation</b>	
	Project: All	
	Format: MDC_AOP2 [CHV, BSW]	
	Specifies the atomic integer operation to be performed.	
7:0	<b>Binding Table Index</b>	
	Project: All	
	Format: MDC_BTS [CHV, BSW]	
	Specifies the Binding Table Index for the message	

## Dword SIMD4x2 Atomic Counter Binary Write Only Operation MSD

### MSD1W\_DWAC2\_4x2 - Dword SIMD4x2 Atomic Counter Binary Write Only Operation MSD

Project: CHV, BSW  
 Source: DataPort 1  
 Length Bias: 1  
 Family: Untyped Atomic Operation  
 Group: Dword Atomic Counter Binary Operation

DWord	Bit	Description					
0	19	<b>Header Present</b>					
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_MHR [CHV, BSW]</td> </tr> </table> <p>Indicates that the message requires a header</p>	Project:	All	Format:	MDC_MHR [CHV, BSW]	
	Project:	All					
	Format:	MDC_MHR [CHV, BSW]					
	18:14	<b>Message Type</b>					
<table border="1"> <tr> <td>Default Value:</td> <td>0Ch</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Atomic Counter Operation SIMD4x2 message</p>		Default Value:	0Ch	Project:	All	Format:	Opcode
Default Value:		0Ch					
Project:	All						
Format:	Opcode						
<table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Specifies that no return data is sent back to the thread.</p>	Default Value:	0h	Project:	All	Format:	Opcode	
Default Value:	0h						
Project:	All						
Format:	Opcode						
12	<b>Reserved</b>						
11:8	<b>Atomic Integer Operation</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_AOP2 [CHV, BSW]</td> </tr> </table> <p>Specifies the atomic integer operation to be performed.</p>	Project:	All	Format:	MDC_AOP2 [CHV, BSW]		
Project:	All						
Format:	MDC_AOP2 [CHV, BSW]						
7:0	<b>Binding Table Index</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_BTS [CHV, BSW]</td> </tr> </table> <p>Specifies the Binding Table Index for the message</p>	Project:	All	Format:	MDC_BTS [CHV, BSW]		
Project:	All						
Format:	MDC_BTS [CHV, BSW]						

## Dword SIMD4x2 Atomic Counter Unary with Return Data Operation MSD

MSD1R_DWAC1_4x2 - Dword SIMD4x2 Atomic Counter Unary with Return Data Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Atomic Operation	
Group:	Dword Atomic Counter Unary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHR [CHV, BSW]
	Indicates that the message requires a header	
	18:14	<b>Message Type</b>
		Default Value: 0Ch
Project: All		
Format: Opcode		
Atomic Counter Operation SIMD4x2 message		
13	<b>Return Data Control</b>	
	Default Value: 1h	
	Project: All	
	Format: Opcode	
Specifies that return data is sent back to the thread.		
12	<b>Reserved</b>	
11:8	<b>Atomic Integer Operation</b>	
	Project: All	
	Format: MDC_AOP1 [CHV, BSW]	
	Specifies the atomic integer operation to be performed.	
7:0	<b>Binding Table Index</b>	
	Project: All	
	Format: MDC_BTS [CHV, BSW]	
	Specifies the Binding Table Index for the message	

## Dword SIMD4x2 Atomic Counter Unary Write Only Operation MSD

### MSD1W\_DWAC1\_4x2 - Dword SIMD4x2 Atomic Counter Unary Write Only Operation MSD

Project: CHV, BSW  
 Source: DataPort 1  
 Length Bias: 1  
 Family: Untyped Atomic Operation  
 Group: Dword Atomic Counter Unary Operation

DWord	Bit	Description					
0	19	<b>Header Present</b>					
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_MHR [CHV, BSW]</td> </tr> </table> <p>Indicates that the message requires a header</p>	Project:	All	Format:	MDC_MHR [CHV, BSW]	
	Project:	All					
	Format:	MDC_MHR [CHV, BSW]					
	18:14	<b>Message Type</b>					
		<table border="1"> <tr> <td>Default Value:</td> <td>0Ch</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Atomic Counter Operation SIMD4x2 message</p>	Default Value:	0Ch	Project:	All	Format:
Default Value:		0Ch					
Project:	All						
Format:	Opcode						
<b>Return Data Control</b>							
<table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Specifies that no return data is sent back to the thread.</p>	Default Value:	0h	Project:	All	Format:	Opcode	
Default Value:	0h						
Project:	All						
Format:	Opcode						
12	<b>Reserved</b>						
11:8	<b>Atomic Integer Operation</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_AOP1 [CHV, BSW]</td> </tr> </table> <p>Specifies the atomic integer operation to be performed.</p>	Project:	All	Format:	MDC_AOP1 [CHV, BSW]		
Project:	All						
Format:	MDC_AOP1 [CHV, BSW]						
7:0	<b>Binding Table Index</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_BTS [CHV, BSW]</td> </tr> </table> <p>Specifies the Binding Table Index for the message</p>	Project:	All	Format:	MDC_BTS [CHV, BSW]		
Project:	All						
Format:	MDC_BTS [CHV, BSW]						



## Dword SIMD4x2 Typed Atomic Integer Binary with Return Data Operation MSD

MSD1R_DWTAI2_4x2 - Dword SIMD4x2 Typed Atomic Integer Binary with Return Data Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Typed Atomic Operation	
Group:	Dword Typed Atomic Integer Binary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHP [CHV, BSW]
	If set, indicates that the message includes the header.	
	18:14	<b>Message Type</b>
		Default Value: 07h
Project: All		
Format: Opcode		
Typed Atomic Integer Operation SIMD4x2 message		
13	<b>Return Data Control</b>	
	Default Value: 1h	
	Project: All	
	Format: Opcode	
Specifies that return data is sent back to the thread.		
12	<b>Reserved</b>	
11:8	<b>Atomic Integer Operation</b>	
	Project: All	
	Format: MDC_AOP2 [CHV, BSW]	
	Specifies the atomic integer operation to be performed.	
7:0	<b>Binding Table Index</b>	
	Project: All	
	Format: MDC_BTS [CHV, BSW]	
	Specifies the Binding Table Index for the message	

## Dword SIMD4x2 Typed Atomic Integer Binary Write Only Operation MSD

MSD1W_DWTAI2_4x2 - Dword SIMD4x2 Typed Atomic Integer Binary Write Only Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Typed Atomic Operation	
Group:	Dword Typed Atomic Integer Binary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHP [CHV, BSW]
	If set, indicates that the message includes the header.	
	18:14	<b>Message Type</b>
		Default Value: 07h
Project: All		
Format: Opcode		
Typed Atomic Integer Operation SIMD4x2 message		
13	<b>Return Data Control</b>	
	Default Value: 0h	
	Project: All	
	Format: Opcode	
Specifies that no return data is sent back to the thread.		
12	<b>Reserved</b>	
11:8	<b>Atomic Integer Operation</b>	
	Project: All	
	Format: MDC_AOP2 [CHV, BSW]	
	Specifies the atomic integer operation to be performed.	
7:0	<b>Binding Table Index</b>	
	Project: All	
	Format: MDC_BTS [CHV, BSW]	
	Specifies the Binding Table Index for the message	

## Dword SIMD4x2 Typed Atomic Integer Trinary with Return Data Operation MSD

MSD1R_DWTAI3_4x2 - Dword SIMD4x2 Typed Atomic Integer Trinary with Return Data Operation MSD							
Project:	CHV, BSW						
Source:	DataPort 1						
Length Bias:	1						
Family:	Typed Atomic Operation						
Group:	Dword Typed Atomic Integer Trinary Operation						
DWord	Bit	Description					
0	19	<b>Header Present</b>					
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_MHP [CHV, BSW]</td> </tr> </table> <p>If set, indicates that the message includes the header.</p>	Project:	All	Format:	MDC_MHP [CHV, BSW]	
	Project:	All					
	Format:	MDC_MHP [CHV, BSW]					
	18:14	<b>Message Type</b>					
		<table border="1"> <tr> <td>Default Value:</td> <td>07h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Typed Atomic Integer Operation SIMD4x2 message</p>	Default Value:	07h	Project:	All	Format:
Default Value:		07h					
Project:	All						
Format:	Opcode						
<b>Return Data Control</b>							
13	<table border="1"> <tr> <td>Default Value:</td> <td>1h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Specifies that return data is sent back to the thread.</p>	Default Value:	1h	Project:	All	Format:	Opcode
Default Value:	1h						
Project:	All						
Format:	Opcode						
12	<b>Reserved</b>						
11:8	<b>Atomic Integer Operation</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_AOP3S [CHV, BSW]</td> </tr> </table> <p>Specifies the atomic integer operation to be performed.</p>	Project:	All	Format:	MDC_AOP3S [CHV, BSW]		
Project:	All						
Format:	MDC_AOP3S [CHV, BSW]						
7:0	<b>Binding Table Index</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_BTS [CHV, BSW]</td> </tr> </table> <p>Specifies the Binding Table Index for the message</p>	Project:	All	Format:	MDC_BTS [CHV, BSW]		
	Project:	All					
Format:	MDC_BTS [CHV, BSW]						

## Dword SIMD4x2 Typed Atomic Integer Trinary Write Only Operation MSD

MSD1W_DWTAI3_4x2 - Dword SIMD4x2 Typed Atomic Integer Trinary Write Only Operation MSD							
Project:	CHV, BSW						
Source:	DataPort 1						
Length Bias:	1						
Family:	Typed Atomic Operation						
Group:	Dword Typed Atomic Integer Trinary Operation						
DWord	Bit	Description					
0	19	<b>Header Present</b>					
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_MHP [CHV, BSW]</td> </tr> </table> <p>If set, indicates that the message includes the header.</p>	Project:	All	Format:	MDC_MHP [CHV, BSW]	
	Project:	All					
	Format:	MDC_MHP [CHV, BSW]					
	18:14	<b>Message Type</b>					
		<table border="1"> <tr> <td>Default Value:</td> <td>07h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Typed Atomic Integer Operation SIMD4x2 message</p>	Default Value:	07h	Project:	All	Format:
Default Value:		07h					
Project:	All						
Format:	Opcode						
<b>Return Data Control</b>							
<table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Specifies that no return data is sent back to the thread.</p>	Default Value:	0h	Project:	All	Format:	Opcode	
Default Value:	0h						
Project:	All						
Format:	Opcode						
12	<b>Reserved</b>						
11:8	<b>Atomic Integer Operation</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_AOP3S [CHV, BSW]</td> </tr> </table> <p>Specifies the atomic integer operation to be performed.</p>	Project:	All	Format:	MDC_AOP3S [CHV, BSW]		
Project:	All						
Format:	MDC_AOP3S [CHV, BSW]						
7:0	<b>Binding Table Index</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_BTS [CHV, BSW]</td> </tr> </table> <p>Specifies the Binding Table Index for the message</p>	Project:	All	Format:	MDC_BTS [CHV, BSW]		
Project:	All						
Format:	MDC_BTS [CHV, BSW]						

## Dword SIMD4x2 Typed Atomic Integer Unary with Return Data Operation MSD

MSD1R_DWTAI1_4x2 - Dword SIMD4x2 Typed Atomic Integer Unary with Return Data Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Typed Atomic Operation	
Group:	Dword Typed Atomic Integer Unary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
	Format: MDC_MHP [CHV, BSW]	
	If set, indicates that the message includes the header.	
	18:14	<b>Message Type</b>
		Default Value: 07h
Project: All		
Format: Opcode		
Typed Atomic Integer Operation SIMD4x2 message		
13	<b>Return Data Control</b>	
	Default Value: 1h	
	Project: All	
Format: Opcode		
Specifies that return data is sent back to the thread.		
12	<b>Reserved</b>	
11:8	<b>Atomic Integer Operation</b>	
	Project: All	
	Format: MDC_AOP1 [CHV, BSW]	
Specifies the atomic integer operation to be performed.		
7:0	<b>Binding Table Index</b>	
	Project: All	
	Format: MDC_BTS [CHV, BSW]	
Specifies the Binding Table Index for the message		

## Dword SIMD4x2 Typed Atomic Integer Unary Write Only Operation MSD

MSD1W_DWTAI1_4x2 - Dword SIMD4x2 Typed Atomic Integer Unary Write Only Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Typed Atomic Operation	
Group:	Dword Typed Atomic Integer Unary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHP [CHV, BSW]
	If set, indicates that the message includes the header.	
	18:14	<b>Message Type</b>
		Default Value: 07h
Project: All		
Format: Opcode		
Typed Atomic Integer Operation SIMD4x2 message		
13	<b>Return Data Control</b>	
	Default Value: 0h	
	Project: All	
Format: Opcode		
Specifies that no return data is sent back to the thread.		
12	<b>Reserved</b>	
11:8	<b>Atomic Integer Operation</b>	
	Project: All	
	Format: MDC_AOP1 [CHV, BSW]	
Specifies the atomic integer operation to be performed.		
7:0	<b>Binding Table Index</b>	
	Project: All	
	Format: MDC_BTS [CHV, BSW]	
Specifies the Binding Table Index for the message		

## Dword SIMD4x2 Untyped Atomic Integer Binary with Return Data Operation MSD

MSD1R_DWAI2_4x2 - Dword SIMD4x2 Untyped Atomic Integer Binary with Return Data Operation MSD							
Project:	CHV, BSW						
Source:	DataPort 1						
Length Bias:	1						
Family:	Untyped Atomic Operation						
Group:	Dword Untyped Atomic Integer Binary Operation						
DWord	Bit	Description					
0	19	<b>Header Present</b>					
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_MHP [CHV, BSW]</td> </tr> </table> <p>If set, indicates that the message includes the header.</p>	Project:	All	Format:	MDC_MHP [CHV, BSW]	
	Project:	All					
	Format:	MDC_MHP [CHV, BSW]					
	18:14	<b>Message Type</b>					
<table border="1"> <tr> <td>Default Value:</td> <td>03h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Untyped Atomic Integer Operation SIMD4x2 message</p>		Default Value:	03h	Project:	All	Format:	Opcode
Default Value:		03h					
Project:	All						
Format:	Opcode						
<table border="1"> <tr> <td>Default Value:</td> <td>1h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Specifies that return data is sent back to the thread.</p>	Default Value:	1h	Project:	All	Format:	Opcode	
Default Value:	1h						
Project:	All						
Format:	Opcode						
12	<b>Reserved</b>						
11:8	<b>Atomic Integer Operation</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_AOP2 [CHV, BSW]</td> </tr> </table> <p>Specifies the atomic integer operation to be performed.</p>	Project:	All	Format:	MDC_AOP2 [CHV, BSW]		
Project:	All						
Format:	MDC_AOP2 [CHV, BSW]						
7:0	<b>Binding Table Index</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_BTS_SLM_A32 [CHV, BSW]</td> </tr> </table> <p>Specifies the Binding Table Index for the message</p>	Project:	All	Format:	MDC_BTS_SLM_A32 [CHV, BSW]		
Project:	All						
Format:	MDC_BTS_SLM_A32 [CHV, BSW]						

## Dword SIMD4x2 Untyped Atomic Integer Binary Write Only Operation MSD

MSD1W_DWAI2_4x2 - Dword SIMD4x2 Untyped Atomic Integer Binary Write Only Operation MSD							
Project:	CHV, BSW						
Source:	DataPort 1						
Length Bias:	1						
Family:	Untyped Atomic Operation						
Group:	Dword Untyped Atomic Integer Binary Operation						
DWord	Bit	Description					
0	19	<b>Header Present</b>					
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_MHP [CHV, BSW]</td> </tr> </table> <p>If set, indicates that the message includes the header.</p>	Project:	All	Format:	MDC_MHP [CHV, BSW]	
	Project:	All					
	Format:	MDC_MHP [CHV, BSW]					
	18:14	<b>Message Type</b>					
<table border="1"> <tr> <td>Default Value:</td> <td>03h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Untyped Atomic Integer Operation SIMD4x2 message</p>		Default Value:	03h	Project:	All	Format:	Opcode
Default Value:		03h					
Project:	All						
Format:	Opcode						
<table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Specifies that no return data is sent back to the thread.</p>	Default Value:	0h	Project:	All	Format:	Opcode	
Default Value:	0h						
Project:	All						
Format:	Opcode						
12	<b>Reserved</b>						
11:8	<b>Atomic Integer Operation</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_AOP2 [CHV, BSW]</td> </tr> </table> <p>Specifies the atomic integer operation to be performed.</p>	Project:	All	Format:	MDC_AOP2 [CHV, BSW]		
Project:	All						
Format:	MDC_AOP2 [CHV, BSW]						
7:0	<b>Binding Table Index</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_BTS_SLM_A32 [CHV, BSW]</td> </tr> </table> <p>Specifies the Binding Table Index for the message</p>	Project:	All	Format:	MDC_BTS_SLM_A32 [CHV, BSW]		
	Project:	All					
Format:	MDC_BTS_SLM_A32 [CHV, BSW]						



## Dword SIMD4x2 Untyped Atomic Integer Trinary with Return Data Operation MSD

MSD1R_DWAI3_4x2 - Dword SIMD4x2 Untyped Atomic Integer Trinary with Return Data Operation MSD							
Project:	CHV, BSW						
Source:	DataPort 1						
Length Bias:	1						
Family:	Untyped Atomic Operation						
Group:	Dword Untyped Atomic Integer Trinary Operation						
DWord	Bit	Description					
0	19	<b>Header Present</b>					
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_MHP [CHV, BSW]</td> </tr> </table> <p>If set, indicates that the message includes the header.</p>	Project:	All	Format:	MDC_MHP [CHV, BSW]	
	Project:	All					
	Format:	MDC_MHP [CHV, BSW]					
	18:14	<b>Message Type</b>					
<table border="1"> <tr> <td>Default Value:</td> <td>03h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Untyped Atomic Integer Operation SIMD4x2 message</p>		Default Value:	03h	Project:	All	Format:	Opcode
Default Value:		03h					
Project:	All						
Format:	Opcode						
<table border="1"> <tr> <td>Default Value:</td> <td>1h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Specifies that return data is sent back to the thread.</p>	Default Value:	1h	Project:	All	Format:	Opcode	
Default Value:	1h						
Project:	All						
Format:	Opcode						
12	<b>Reserved</b>						
11:8	<b>Atomic Integer Operation</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_AOP3 [CHV, BSW]</td> </tr> </table> <p>Specifies the atomic integer operation to be performed.</p>	Project:	All	Format:	MDC_AOP3 [CHV, BSW]		
Project:	All						
Format:	MDC_AOP3 [CHV, BSW]						
7:0	<b>Binding Table Index</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_BTS_SLM_A32 [CHV, BSW]</td> </tr> </table> <p>Specifies the Binding Table Index for the message</p>	Project:	All	Format:	MDC_BTS_SLM_A32 [CHV, BSW]		
Project:	All						
Format:	MDC_BTS_SLM_A32 [CHV, BSW]						

## Dword SIMD4x2 Untyped Atomic Integer Trinary Write Only Operation MSD

MSD1W_DWAI3_4x2 - Dword SIMD4x2 Untyped Atomic Integer Trinary Write Only Operation MSD							
Project:	CHV, BSW						
Source:	DataPort 1						
Length Bias:	1						
Family:	Untyped Atomic Operation						
Group:	Dword Untyped Atomic Integer Trinary Operation						
DWord	Bit	Description					
0	19	<b>Header Present</b>					
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_MHP [CHV, BSW]</td> </tr> </table> <p>If set, indicates that the message includes the header.</p>	Project:	All	Format:	MDC_MHP [CHV, BSW]	
	Project:	All					
	Format:	MDC_MHP [CHV, BSW]					
	18:14	<b>Message Type</b>					
<table border="1"> <tr> <td>Default Value:</td> <td>03h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Untyped Atomic Integer Operation SIMD4x2 message</p>		Default Value:	03h	Project:	All	Format:	Opcode
Default Value:		03h					
Project:	All						
Format:	Opcode						
<table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Specifies that no return data is sent back to the thread.</p>	Default Value:	0h	Project:	All	Format:	Opcode	
Default Value:	0h						
Project:	All						
Format:	Opcode						
12	<b>Reserved</b>						
11:8	<b>Atomic Integer Operation</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_AOP3 [CHV, BSW]</td> </tr> </table> <p>Specifies the atomic integer operation to be performed.</p>	Project:	All	Format:	MDC_AOP3 [CHV, BSW]		
Project:	All						
Format:	MDC_AOP3 [CHV, BSW]						
7:0	<b>Binding Table Index</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_BTS_SLM_A32 [CHV, BSW]</td> </tr> </table> <p>Specifies the Binding Table Index for the message</p>	Project:	All	Format:	MDC_BTS_SLM_A32 [CHV, BSW]		
Project:	All						
Format:	MDC_BTS_SLM_A32 [CHV, BSW]						

## Dword SIMD4x2 Untyped Atomic Integer Unary with Return Data Operation MSD

MSD1R_DWAI1_4x2 - Dword SIMD4x2 Untyped Atomic Integer Unary with Return Data Operation MSD							
Project:	CHV, BSW						
Source:	DataPort 1						
Length Bias:	1						
Family:	Untyped Atomic Operation						
Group:	Dword Untyped Atomic Integer Unary Operation						
DWord	Bit	Description					
0	19	<b>Header Present</b>					
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_MHP [CHV, BSW]</td> </tr> </table> <p>If set, indicates that the message includes the header.</p>	Project:	All	Format:	MDC_MHP [CHV, BSW]	
	Project:	All					
	Format:	MDC_MHP [CHV, BSW]					
	18:14	<b>Message Type</b>					
<table border="1"> <tr> <td>Default Value:</td> <td>03h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Untyped Atomic Integer Operation SIMD4x2 message</p>		Default Value:	03h	Project:	All	Format:	Opcode
Default Value:		03h					
Project:	All						
Format:	Opcode						
<table border="1"> <tr> <td>Default Value:</td> <td>1h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Specifies that return data is sent back to the thread.</p>	Default Value:	1h	Project:	All	Format:	Opcode	
Default Value:	1h						
Project:	All						
Format:	Opcode						
12	<b>Reserved</b>						
11:8	<b>Atomic Integer Operation</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_AOP1 [CHV, BSW]</td> </tr> </table> <p>Specifies the atomic integer operation to be performed.</p>	Project:	All	Format:	MDC_AOP1 [CHV, BSW]		
Project:	All						
Format:	MDC_AOP1 [CHV, BSW]						
7:0	<b>Binding Table Index</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_BTS_SLM_A32 [CHV, BSW]</td> </tr> </table> <p>Specifies the Binding Table Index for the message</p>	Project:	All	Format:	MDC_BTS_SLM_A32 [CHV, BSW]		
	Project:	All					
Format:	MDC_BTS_SLM_A32 [CHV, BSW]						

## Dword SIMD4x2 Untyped Atomic Integer Unary Write Only Operation MSD

MSD1W_DWAI1_4x2 - Dword SIMD4x2 Untyped Atomic Integer Unary Write Only Operation MSD							
Project:	CHV, BSW						
Source:	DataPort 1						
Length Bias:	1						
Family:	Untyped Atomic Operation						
Group:	Dword Untyped Atomic Integer Unary Operation						
DWord	Bit	Description					
0	19	<b>Header Present</b>					
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_MHP [CHV, BSW]</td> </tr> </table> <p>If set, indicates that the message includes the header.</p>	Project:	All	Format:	MDC_MHP [CHV, BSW]	
	Project:	All					
	Format:	MDC_MHP [CHV, BSW]					
	18:14	<b>Message Type</b>					
<table border="1"> <tr> <td>Default Value:</td> <td>03h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Untyped Atomic Integer Operation SIMD4x2 message</p>		Default Value:	03h	Project:	All	Format:	Opcode
Default Value:		03h					
Project:	All						
Format:	Opcode						
<table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Specifies that no return data is sent back to the thread.</p>	Default Value:	0h	Project:	All	Format:	Opcode	
Default Value:	0h						
Project:	All						
Format:	Opcode						
12	<b>Reserved</b>						
11:8	<b>Atomic Integer Operation</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_AOP1 [CHV, BSW]</td> </tr> </table> <p>Specifies the atomic integer operation to be performed.</p>	Project:	All	Format:	MDC_AOP1 [CHV, BSW]		
Project:	All						
Format:	MDC_AOP1 [CHV, BSW]						
7:0	<b>Binding Table Index</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_BTS_SLM_A32 [CHV, BSW]</td> </tr> </table> <p>Specifies the Binding Table Index for the message</p>	Project:	All	Format:	MDC_BTS_SLM_A32 [CHV, BSW]		
	Project:	All					
Format:	MDC_BTS_SLM_A32 [CHV, BSW]						

## Dword Typed Atomic Integer Binary with Return Data Operation MSD

<b>MSD1R_DWTAI2 - Dword Typed Atomic Integer Binary with Return Data Operation MSD</b>			
Project:	CHV, BSW		
Source:	DataPort 1		
Length Bias:	1		
Family:	Typed Atomic Operation		
Group:	Dword Typed Atomic Integer Binary Operation		
DWord	Bit	Description	
0	19	<b>Header Present</b>	
		Project: All	
		Format: MDC_MHP [CHV, BSW]	
		If set, indicates that the message includes the header.	
	18:14	<b>Message Type</b>	
		Default Value: 06h	
		Project: All	
		Format: Opcode	
			Typed Atomic Integer Operation message
	13	<b>Return Data Control</b>	
Default Value: 1h			
Project: All			
Format: Opcode			
		Specifies that return data is sent back to the thread.	
12	<b>Slot Group</b>		
	Project: All		
	Format: MDC_SG2 [CHV, BSW]		
		Specifies the Slot Group mode of the message (which slots are processed)	
11:8	<b>Atomic Integer Operation</b>		
	Project: All		
	Format: MDC_AOP2 [CHV, BSW]		
		Specifies the atomic integer operation to be performed.	
7:0	<b>Binding Table Index</b>		
	Project: All		
	Format: MDC_BTS [CHV, BSW]		
		Specifies the Binding Table Index for the message	

## Dword Typed Atomic Integer Binary Write Only Operation MSD

### MSD1W\_DWTAI2 - Dword Typed Atomic Integer Binary Write Only Operation MSD

Project: CHV, BSW  
 Source: DataPort 1  
 Length Bias: 1  
 Family: Typed Atomic Operation  
 Group: Dword Typed Atomic Integer Binary Operation

DWord	Bit	Description					
0	19	<b>Header Present</b>					
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_MHP [CHV, BSW]</td> </tr> </table> <p>If set, indicates that the message includes the header.</p>	Project:	All	Format:	MDC_MHP [CHV, BSW]	
	Project:	All					
	Format:	MDC_MHP [CHV, BSW]					
	18:14	<b>Message Type</b>					
		<table border="1"> <tr> <td>Default Value:</td> <td>06h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Typed Atomic Integer Operation message</p>	Default Value:	06h	Project:	All	Format:
Default Value:		06h					
Project:	All						
Format:	Opcode						
<b>Return Data Control</b>							
<table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Specifies that no return data is sent back to the thread.</p>	Default Value:	0h	Project:	All	Format:	Opcode	
Default Value:	0h						
Project:	All						
Format:	Opcode						
12	<b>Slot Group</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_SG2 [CHV, BSW]</td> </tr> </table> <p>Specifies the Slot Group mode of the message (which slots are processed)</p>	Project:	All	Format:	MDC_SG2 [CHV, BSW]		
Project:	All						
Format:	MDC_SG2 [CHV, BSW]						
11:8	<b>Atomic Integer Operation</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_AOP2 [CHV, BSW]</td> </tr> </table> <p>Specifies the atomic integer operation to be performed.</p>	Project:	All	Format:	MDC_AOP2 [CHV, BSW]		
Project:	All						
Format:	MDC_AOP2 [CHV, BSW]						
7:0	<b>Binding Table Index</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_BTS [CHV, BSW]</td> </tr> </table> <p>Specifies the Binding Table Index for the message</p>	Project:	All	Format:	MDC_BTS [CHV, BSW]		
Project:	All						
Format:	MDC_BTS [CHV, BSW]						

## Dword Typed Atomic Integer Trinary with Return Data Operation MSD

<b>MSD1R_DWTAI3 - Dword Typed Atomic Integer Trinary with Return Data Operation MSD</b>		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Typed Atomic Operation	
Group:	Dword Typed Atomic Integer Trinary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHP [CHV, BSW]
	If set, indicates that the message includes the header.	
	18:14	<b>Message Type</b>
		Default Value: 06h
Project: All		
Format: Opcode		
Typed Atomic Integer Operation message		
13	<b>Return Data Control</b>	
	Default Value: 1h	
	Project: All	
	Format: Opcode	
Specifies that return data is sent back to the thread.		
12	<b>Slot Group</b>	
	Project: All	
	Format: MDC_SG2 [CHV, BSW]	
Specifies the Slot Group mode of the message (which slots are processed)		
11:8	<b>Atomic Integer Operation</b>	
	Project: All	
	Format: MDC_AOP3S [CHV, BSW]	
Specifies the atomic integer operation to be performed.		
7:0	<b>Binding Table Index</b>	
	Project: All	
	Format: MDC_BTS [CHV, BSW]	
Specifies the Binding Table Index for the message		

## Dword Typed Atomic Integer Trinary Write Only Operation MSD

<b>MSD1W_DWTAI3 - Dword Typed Atomic Integer Trinary Write Only Operation MSD</b>								
Project:	CHV, BSW							
Source:	DataPort 1							
Length Bias:	1							
Family:	Typed Atomic Operation							
Group:	Dword Typed Atomic Integer Trinary Operation							
DWord	Bit	Description						
0	19	<b>Header Present</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_MHP [CHV, BSW]</td> </tr> </table> <p>If set, indicates that the message includes the header.</p>	Project:	All	Format:	MDC_MHP [CHV, BSW]		
	Project:	All						
	Format:	MDC_MHP [CHV, BSW]						
	18:14	<b>Message Type</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Default Value:</td> <td>06h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Typed Atomic Integer Operation message</p>	Default Value:	06h	Project:	All	Format:	Opcode
	Default Value:	06h						
	Project:	All						
Format:	Opcode							
13	<b>Return Data Control</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Default Value:</td> <td>0h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Specifies that no return data is sent back to the thread.</p>	Default Value:	0h	Project:	All	Format:	Opcode	
Default Value:	0h							
Project:	All							
Format:	Opcode							
12	<b>Slot Group</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_SG2 [CHV, BSW]</td> </tr> </table> <p>Specifies the Slot Group mode of the message (which slots are processed)</p>	Project:	All	Format:	MDC_SG2 [CHV, BSW]			
Project:	All							
Format:	MDC_SG2 [CHV, BSW]							
11:8	<b>Atomic Integer Operation</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_AOP3S [CHV, BSW]</td> </tr> </table> <p>Specifies the atomic integer operation to be performed.</p>	Project:	All	Format:	MDC_AOP3S [CHV, BSW]			
Project:	All							
Format:	MDC_AOP3S [CHV, BSW]							
7:0	<b>Binding Table Index</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_BTS [CHV, BSW]</td> </tr> </table> <p>Specifies the Binding Table Index for the message</p>	Project:	All	Format:	MDC_BTS [CHV, BSW]			
Project:	All							
Format:	MDC_BTS [CHV, BSW]							



## Dword Typed Atomic Integer Unary with Return Data Operation MSD

MSD1R_DWTAI1 - Dword Typed Atomic Integer Unary with Return Data Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Typed Atomic Operation	
Group:	Dword Typed Atomic Integer Unary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHP [CHV, BSW]
	If set, indicates that the message includes the header.	
	18:14	<b>Message Type</b>
		Default Value: 06h
Project: All		
Format: Opcode		
Typed Atomic Integer Operation message		
13	<b>Return Data Control</b>	
	Default Value: 1h	
	Project: All	
	Format: Opcode	
Specifies that return data is sent back to the thread.		
12	<b>Slot Group</b>	
	Project: All	
	Format: MDC_SG2 [CHV, BSW]	
Specifies the Slot Group mode of the message (which slots are processed)		
11:8	<b>Atomic Integer Operation</b>	
	Project: All	
	Format: MDC_AOP1 [CHV, BSW]	
Specifies the atomic integer operation to be performed.		
7:0	<b>Binding Table Index</b>	
	Project: All	
	Format: MDC_BTS [CHV, BSW]	
Specifies the Binding Table Index for the message		

## Dword Typed Atomic Integer Unary Write Only Operation MSD

MSD1W_DWTAI1 - Dword Typed Atomic Integer Unary Write Only Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Typed Atomic Operation	
Group:	Dword Typed Atomic Integer Unary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
	Format: MDC_MHP [CHV, BSW]	
	If set, indicates that the message includes the header.	
	18:14	<b>Message Type</b>
		Default Value: 06h
		Project: All
		Format: Opcode
	Typed Atomic Integer Operation message	
	13	<b>Return Data Control</b>
Default Value: 0h		
Project: All		
Format: Opcode		
Specifies that no return data is sent back to the thread.		
12	<b>Slot Group</b>	
	Project: All	
	Format: MDC_SG2 [CHV, BSW]	
Specifies the Slot Group mode of the message (which slots are processed)		
11:8	<b>Atomic Integer Operation</b>	
	Project: All	
	Format: MDC_AOP1 [CHV, BSW]	
Specifies the atomic integer operation to be performed.		
7:0	<b>Binding Table Index</b>	
	Project: All	
	Format: MDC_BTS [CHV, BSW]	
Specifies the Binding Table Index for the message		

## Dword Untyped Atomic Integer Binary with Return Data Operation MSD

MSD1R_DWAI2 - Dword Untyped Atomic Integer Binary with Return Data Operation MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Atomic Operation	
Group:	Dword Untyped Atomic Integer Binary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHP [CHV, BSW]
	If set, indicates that the message includes the header.	
	18:14	<b>Message Type</b>
		Default Value: 02h
Project: All		
Format: Opcode		
Untyped Atomic Integer Operation message		
13	<b>Return Data Control</b>	
	Default Value: 1h	
	Project: All	
	Format: Opcode	
Specifies that return data is sent back to the thread.		
12	<b>SIMD Mode</b>	
	Project: All	
	Format: MDC_SM2R [CHV, BSW]	
Specifies the SIMD mode of the message (number of slots processed)		
11:8	<b>Atomic Integer Operation</b>	
	Project: All	
	Format: MDC_AOP2 [CHV, BSW]	
Specifies the atomic integer operation to be performed.		
7:0	<b>Binding Table Index</b>	
	Project: All	
	Format: MDC_BTS_SLM_A32 [CHV, BSW]	
	Specifies the Binding Table Index for the message	

## Dword Untyped Atomic Integer Binary Write Only Operation MSD

### MSD1W\_DWAI2 - Dword Untyped Atomic Integer Binary Write Only Operation MSD

Project: CHV, BSW  
 Source: DataPort 1  
 Length Bias: 1  
 Family: Untyped Atomic Operation  
 Group: Dword Untyped Atomic Integer Binary Operation

DWord	Bit	Description						
0	19	<b>Header Present</b>						
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_MHP [CHV, BSW]</td> </tr> </table> <p>If set, indicates that the message includes the header.</p>	Project:	All	Format:	MDC_MHP [CHV, BSW]		
	Project:	All						
	Format:	MDC_MHP [CHV, BSW]						
	18:14	<b>Message Type</b>						
		<table border="1"> <tr> <td>Default Value:</td> <td>02h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Untyped Atomic Integer Operation message</p>	Default Value:	02h	Project:	All	Format:	Opcode
		Default Value:	02h					
Project:		All						
Format:	Opcode							
<b>Return Data Control</b>								
<table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Specifies that no return data is sent back to the thread.</p>	Default Value:	0h	Project:	All	Format:	Opcode		
Default Value:	0h							
Project:	All							
Format:	Opcode							
12	<b>SIMD Mode</b>							
<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_SM2R [CHV, BSW]</td> </tr> </table> <p>Specifies the SIMD mode of the message (number of slots processed)</p>	Project:	All	Format:	MDC_SM2R [CHV, BSW]				
Project:	All							
Format:	MDC_SM2R [CHV, BSW]							
11:8	<b>Atomic Integer Operation</b>							
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_AOP2 [CHV, BSW]</td> </tr> </table> <p>Specifies the atomic integer operation to be performed.</p>	Project:	All	Format:	MDC_AOP2 [CHV, BSW]			
Project:	All							
Format:	MDC_AOP2 [CHV, BSW]							
7:0	<b>Binding Table Index</b>							
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_BTS_SLM_A32 [CHV, BSW]</td> </tr> </table> <p>Specifies the Binding Table Index for the message</p>	Project:	All	Format:	MDC_BTS_SLM_A32 [CHV, BSW]			
	Project:	All						
Format:	MDC_BTS_SLM_A32 [CHV, BSW]							

## Dword Untyped Atomic Integer Ternary with Return Data Operation MSD

<b>MSD1R_DWAI3 - Dword Untyped Atomic Integer Ternary with Return Data Operation MSD</b>		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Atomic Operation	
Group:	Dword Untyped Atomic Integer Ternary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHP [CHV, BSW]
		If set, indicates that the message includes the header.
	18:14	<b>Message Type</b>
		Default Value: 02h
Project: All		
Format: Opcode		
		Untyped Atomic Integer Operation message
13	<b>Return Data Control</b>	
	Default Value: 1h	
	Project: All	
	Format: Opcode	
		Specifies that return data is sent back to the thread.
12	<b>SIMD Mode</b>	
	Project: All	
	Format: MDC_SM2R [CHV, BSW]	
		Specifies the SIMD mode of the message (number of slots processed)
11:8	<b>Atomic Integer Operation</b>	
	Project: All	
	Format: MDC_AOP3 [CHV, BSW]	
		Specifies the atomic integer operation to be performed.
7:0	<b>Binding Table Index</b>	
	Project: All	
	Format: MDC_BTS_SLM_A32 [CHV, BSW]	
		Specifies the Binding Table Index for the message

## Dword Untyped Atomic Integer Ternary Write Only Operation MSD

### MSD1W\_DWAI3 - Dword Untyped Atomic Integer Ternary Write Only Operation MSD

Project: CHV, BSW  
 Source: DataPort 1  
 Length Bias: 1  
 Family: Untyped Atomic Operation  
 Group: Dword Untyped Atomic Integer Ternary Operation

DWord	Bit	Description					
0	19	<b>Header Present</b>					
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_MHP [CHV, BSW]</td> </tr> </table> <p>If set, indicates that the message includes the header.</p>	Project:	All	Format:	MDC_MHP [CHV, BSW]	
	Project:	All					
	Format:	MDC_MHP [CHV, BSW]					
	18:14	<b>Message Type</b>					
		<table border="1"> <tr> <td>Default Value:</td> <td>02h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Untyped Atomic Integer Operation message</p>	Default Value:	02h	Project:	All	Format:
Default Value:		02h					
Project:	All						
Format:	Opcode						
<b>Return Data Control</b>							
13	<table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Specifies that no return data is sent back to the thread.</p>	Default Value:	0h	Project:	All	Format:	Opcode
Default Value:	0h						
Project:	All						
Format:	Opcode						
12	<b>SIMD Mode</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_SM2R [CHV, BSW]</td> </tr> </table> <p>Specifies the SIMD mode of the message (number of slots processed)</p>	Project:	All	Format:	MDC_SM2R [CHV, BSW]		
Project:	All						
Format:	MDC_SM2R [CHV, BSW]						
11:8	<b>Atomic Integer Operation</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_AOP3 [CHV, BSW]</td> </tr> </table> <p>Specifies the atomic integer operation to be performed.</p>	Project:	All	Format:	MDC_AOP3 [CHV, BSW]		
Project:	All						
Format:	MDC_AOP3 [CHV, BSW]						
7:0	<b>Binding Table Index</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_BTS_SLM_A32 [CHV, BSW]</td> </tr> </table> <p>Specifies the Binding Table Index for the message</p>	Project:	All	Format:	MDC_BTS_SLM_A32 [CHV, BSW]		
Project:	All						
Format:	MDC_BTS_SLM_A32 [CHV, BSW]						

## Dword Untyped Atomic Integer Unary with Return Data Operation MSD

<b>MSD1R_DWAI1 - Dword Untyped Atomic Integer Unary with Return Data Operation MSD</b>		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Untyped Atomic Operation	
Group:	Dword Untyped Atomic Integer Unary Operation	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHP [CHV, BSW]
		If set, indicates that the message includes the header.
	18:14	<b>Message Type</b>
		Default Value: 02h
Project: All		
Format: Opcode		
		Untyped Atomic Integer Operation message
13	<b>Return Data Control</b>	
	Default Value: 1h	
	Project: All	
	Format: Opcode	
		Specifies that return data is sent back to the thread.
12	<b>SIMD Mode</b>	
	Project: All	
	Format: MDC_SM2R [CHV, BSW]	
		Specifies the SIMD mode of the message (number of slots processed)
11:8	<b>Atomic Integer Operation</b>	
	Project: All	
	Format: MDC_AOP1 [CHV, BSW]	
		Specifies the atomic integer operation to be performed.
7:0	<b>Binding Table Index</b>	
	Project: All	
	Format: MDC_BTS_SLM_A32 [CHV, BSW]	
		Specifies the Binding Table Index for the message

## Dword Untyped Atomic Integer Unary Write Only Operation MSD

### MSD1W\_DWAI1 - Dword Untyped Atomic Integer Unary Write Only Operation MSD

Project: CHV, BSW  
 Source: DataPort 1  
 Length Bias: 1  
 Family: Untyped Atomic Operation  
 Group: Dword Untyped Atomic Integer Unary Operation

DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHP [CHV, BSW]
		If set, indicates that the message includes the header.
	18:14	<b>Message Type</b>
		Default Value: 02h
		Project: All
Format: Opcode Untyped Atomic Integer Operation message		
13	<b>Return Data Control</b>	
	Default Value: 0h	
	Project: All	
	Format: Opcode Specifies that no return data is sent back to the thread.	
12	<b>SIMD Mode</b>	
	Project: All	
	Format: MDC_SM2R [CHV, BSW] Specifies the SIMD mode of the message (number of slots processed)	
11:8	<b>Atomic Integer Operation</b>	
	Project: All	
	Format: MDC_AOP1 [CHV, BSW] Specifies the atomic integer operation to be performed.	
7:0	<b>Binding Table Index</b>	
	Project: All	
	Format: MDC_BTS_SLM_A32 [CHV, BSW] Specifies the Binding Table Index for the message	



## End If

<b>endif - End If</b>							
Project:	CHV, BSW						
Source:	Eulsa						
Length Bias:	4						
Description							
<p>The endif instruction terminates an if/else/endif block of code. It restores execution to the channels that were active prior to the if/else/endif block. The endif instruction is also used to hop out of nested conditionals by jumping to the end of the next outer conditional block when all channels are disabled.</p> <p>The following table describes the 32-bit JIP. In GEN binary, JIP is at location src1 and must be of type D (signed DWord integer). JIP must be an immediate operand, it is a signed 32-bit number. This value is added to IP pre-increment.</p>							
Format: endif JIP							
Restriction							
Predication is not allowed.							
The execution size must be the same for the if, else, and endif instructions of the same code block.							
Syntax	Project						
endif (exec_size) imm32	CHV, BSW						
Pseudocode							
Evaluate(WrEn); if ( WrEn == 0 ) { // all channels false Jump(IP + JIP); }							
Errata	Description						
	An endif instruction must not be followed by any instruction requiring register indirect access on source operands.						
Predication	Conditional Modifier	Saturation	Source Modifier				
N	N	N	N				
DWord	Bit	Description					
0..3	127:96	<b>JIP</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>S31</td> </tr> </table> <p>Jump Target Offset. The relative offset in bytes if a jump is taken for the instruction.</p>		Project:	CHV, BSW	Format:	S31
	Project:	CHV, BSW					
Format:	S31						
95	<b>Source 0 Address Immediate [9] Sign Bit</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table>		Project:	CHV, BSW			
Project:	CHV, BSW						

<b>endif - End If</b>						
	94:91	<b>Src1.SrcType</b> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>SrcType [CHV, BSW]</td> </tr> </table>	Project:	CHV, BSW	Format:	SrcType [CHV, BSW]
	Project:	CHV, BSW				
	Format:	SrcType [CHV, BSW]				
	90:89	<b>Src1.RegFile</b> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>RegFile [CHV, BSW]</td> </tr> </table>	Project:	CHV, BSW	Format:	RegFile [CHV, BSW]
	Project:	CHV, BSW				
	Format:	RegFile [CHV, BSW]				
88:64	<b>Source 0</b> <table border="1"> <tr> <td>Exists If:</td> <td>(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]='Align16')</td> </tr> <tr> <td>Format:</td> <td>EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN16 [CHV, BSW]</td> </tr> </table>	Exists If:	(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]='Align16')	Format:	EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN16 [CHV, BSW]	
Exists If:	(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]='Align16')					
Format:	EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN16 [CHV, BSW]					
88:64	<b>Source 0</b> <table border="1"> <tr> <td>Exists If:</td> <td>(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]='Align1')</td> </tr> <tr> <td>Format:</td> <td>EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN1 [CHV, BSW]</td> </tr> </table>	Exists If:	(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]='Align1')	Format:	EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN1 [CHV, BSW]	
Exists If:	(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]='Align1')					
Format:	EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN1 [CHV, BSW]					
63:32	<b>Operand Control</b> <table border="1"> <tr> <td>Format:</td> <td>EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]</td> </tr> </table>	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]			
Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]					
31:0	<b>Header</b> <table border="1"> <tr> <td>Format:</td> <td>EU_INSTRUCTION_HEADER [CHV, BSW]</td> </tr> </table>	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]			
Format:	EU_INSTRUCTION_HEADER [CHV, BSW]					

## Extended Math Function

<b>math - Extended Math Function</b>	
Project:	CHV, BSW
Source:	Eulsa
Length Bias:	4
<p>The math instruction performs extended math function on the components in src0, or src0 and src1, and write the output to the channels of dst. The type of extended math function are based on the FC[3:0] encoding in the table below.</p>	
<p>Format: [(pred)] math (exec_size) dst src0 src1 &lt;FC&gt;</p>	
Restriction	
Accumulator access is allowed only for ieee macro functions.	
The math instruction does not support indirect addressing modes.	
The only supported rounding mode for math instruction is Round to Nearest Even.	
INT DIV function does not support SIMD16. INT DIV function does not support simultaneous write to two registers. INT DIV function does not support source modifiers.	
The FDIV function is not supported in ALT_MODE.	
The math instruction can use GRF or immediates as source. The source formats for immediates must be one of the source formats supported by math operation.	
DepCtrl must not be used.	
The math instruction must use GRF as destination.	
The supported regioning mode for math instruction is align1 and align16. The following restrictions apply for align1 mode: Scalar source is supported. Source and destination horizontal stride must be the same. Regioning must ensure Src.Vstride = Src.Width * Src.Hstride . Source and destination offset must be the same, except the case of scalar source.	
Math Operation rules when float and half-floats are mixed between source or between source and destination operands. The half-float operand must be interleaved in the register for align1 and the source and destination register offset must be the same to DW granularity. For align16, the half-float operand is allowed to be packed.	
The execution size must be no more than 8 when half-floats are used in source or destination operand.	
The source operand must not span two registers if the destination operand spans just one register Example: Case (a) // Allowed. The source must be strided by 2. the offset is allowed to select between lower/upper 16b math (8) r10:f r11.0<16;8,2>:hf 0x01 math (8) r10:f r11.1<16;8,2>:hf 0x01 math (8) r10:f r11.0<16;8,2>:hf r12.1<16;8,2>:hf 0x09 Case (b) // Allowed. The destination must be strided by 2. The offset is allowed to selecte between lower/upper 16b math (8) r10.0<2>:hf r11.0<8;8,1>:f math (8) r10.1<2>:hf r11.0<8;8,1>:f 0x01 math (8) r10.0<2>:hf r11.0<16;8,2>:hf r12.0<16;8,2>:hf 0x09 Case (c) // Allowed. Destination has stride of 2. The offset is allowed to select between uppoer/lower 16b math (8) r10.0<2>:hf r11.0<8;8,1>:f r12.1<16;8,2>:hf 0x09 math (8) r10.1<2>:hf r11.1<16;8,2>:hf r12.0<8;8,1>:f 0x09 Case (d) // Not Allowed. Destination is half- float but is not interleaved. math (8) r10.0<1>:hf r11.0<8;8,1>:f Case (e) // Not Allowed. Source is half-float but	

## math - Extended Math Function

not interleaved math (8) r10.0<2>:hf r11.0<8;8,1>:f r12.0<8;8,1>:hf 0x09 Case (f) // Not Allowed. Source operand spans 2 registers while destination spans one register. math (8) r83.8<1>:hf r12.4<4;4,1>:f null 0x02

Math Operation rules when half-floats are used on both source and destination operands. The execution size must be 8. The half-float source must be packed or interleaved. When interleaving, both source and destination must be interleaved. Example: Case (a) // Allowed. The source and destination are packed or interleaved math (8) r10.0:hf r11.0<8;8,1>:hf 0x01 math (8) r10.0<2>:hf r11.0<16;8,2>:hf 0x01 math (8) r10.8:hf r11.0<8;8,1>:hf 0x01 math (8) r10.8<2>:hf r11.0<16;8,2>:hf 0x01

For FDVI and POW, half-float destination data type is not allowed.

For one source math operations src1 must be NULL.

### Syntax

[(pred)] math (exec\_size) reg reg reg imm4

### Pseudocode

```

Evaluate(WrEn);
for (n = 0; n < exec_size; n++) {
    if (WrEn.channel[n] == 1) {
        switch FC[3:0] {
            case 1h:
                dst.channel[n] = rcp(src0.channel[n]);
            case 2h:
                dst.channel[n] = log(src0.channel[n]);
            case 3h:
                dst.channel[n] = exp(src0.channel[n]);
            case 4h:
                dst.channel[n] = sqrt(src0.channel[n]);
            case 5h:
                dst.channel[n] = rsq(src0.channel[n]);
            case 6h:
                dst.channel[n] = sin(src0.channel[n]);
            case 7h:
                dst.channel[n] = cos(src0.channel[n]);
            case 9h: // src0 / src1
                dst.channel[n] = fdiv(src0.channel[n], src1.channel[n]);
            case Ah:
                dst.channel[n] = pow(src0.channel[n], src1/channel[n]);
            case Bh: // src0 / src1
                idiv(src0.channel[n], src1.channel[n]);
                dst.channel[n] = quotient;
                dst+1.channel[n] = remainder;
            case Ch:
                idiv(src0.channel[n], src1.channel[n]);
                dst.channel[n] = quotient;
            case Dh:
                idiv(src0.channel[n], src1.channel[n]);
                dst.channel[n] = remainder;
        }
    }
}

```

math - Extended Math Function			
Predication	Conditional Modifier	Saturation	Source Modifier [CHV, BSW]
Y	N	Y	Y
Src Types	Dst Types	Project	
F	F		
D	D		
UD	UD		
F/HF	F/HF	CHV, BSW	
DWord	Bit	Description	
0..3	127:64	<b>RegSource</b> Format: EU_INSTRUCTION_SOURCES_REG_REG [CHV, BSW]	
	63:32	<b>Operand Control</b> Format: EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]	
	31:28	<b>Controls B</b> Format: EU_INSTRUCTION_CONTROLS_B [CHV, BSW]	
	27:24	<b>Function Control (FC)</b> Format: FC [CHV, BSW]	
	23:8	<b>Controls A</b> Format: EU_INSTRUCTION_CONTROLS_A [CHV, BSW]	
	7	<b>Reserved</b> Format: MBZ	
	6:0	<b>Opcode</b> Format: EU_OPCODE [CHV, BSW]	

## Find First Bit from LSB Side

<b>fbl - Find First Bit from LSB Side</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
The fbl instruction counts component-wise the number of LSB 0 bits before the first 1 bit in src0, storing that number in dst.			
Format: [(pred)] fbl (exec_size) dst src0			
Programming Notes			
If src0 contains no 1 bits, store 0xFFFFFFFF in dst.			
Restriction			
No accumulator access, implicit or explicit.			
Syntax			
[(pred)] fbl (exec_size) reg reg [(pred)] fbl (exec_size) reg imm32			
Pseudocode			
<pre>Evaluate(WrEn); for ( n = 0; n &lt; exec_size; n++ ) { if ( WrEn.chan[n] ) { UD cnt = 0; UD udScalar = src0.chan[n]; while ( (udScalar &amp; 1) == 0 &amp;&amp; cnt != 32 ) { cnt ++; udScalar = udScalar &gt;&gt; 1; } if ( src0.chan[n] == 0x00000000 ) { dst.chan[n] = 0xFFFFFFFF; } else { dst.chan[n] = cnt; } } }</pre>			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	N	N	N
Src Types	Dst Types		
UD	UD		
DWord	Bit	Description	
0..3	127:64	<b>RegSource</b>	
		Exists If:	([(Operand Controls])[Src0.RegFile]!='IMM')
	Format:	EU_INSTRUCTION_SOURCES_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>	
Exists If:		([(Operand Controls])[Src0.RegFile]='IMM')	
Format:	EU_INSTRUCTION_SOURCES_IMM32 [CHV, BSW]		
63:32	<b>Operand Controls</b>		
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]	
31:0	<b>Header</b>		
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]	

## Find First Bit from MSB Side

<b>fbh - Find First Bit from MSB Side</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
<p>If src0 is unsigned, the fbh instruction counts component-wise the leading zeros from src0 and stores the resulting counts in dst. If src0 is signed and positive, the fbh instruction counts component-wise the leading zeros from src0 and stores the resulting counts in dst. If src0 is signed and negative, the fbh instruction counts component-wise the leading ones from src0 and stores the resulting counts in dst.</p>			
Format: [(pred)] fbh (exec_size) dst src0			
Programming Notes			
If src0 is zero, store 0xFFFFFFFF in dst.			
If src0 is signed and is -1 (0xFFFFFFFF), store 0xFFFFFFFF in dst.			
Restriction			
No accumulator access, implicit or explicit.			
Syntax			
[(pred)] fbh (exec_size) reg reg [(pred)] fbh (exec_size) reg imm32			
Pseudocode			
<pre>Evaluate(WrEn); for ( n = 0; n &lt; exec_size; n++ ) { if ( WrEn.chan[n] ) { UD cnt = 0; if ( src0 is unsigned ) { UD udScalar = src0.chan[n]; while ( (udScalar &amp; (1 &lt;&lt; 31)) == 0 &amp;&amp; cnt != 32 ) { cnt ++; udScalar = udScalar &lt;&lt; 1; } if ( src0.chan[n] == 0x00000000 ) { dst.chan[n] = 0xFFFFFFFF; } else { dst.chan[n] = cnt; } } else { // src0 is signed. D dScalar = src0.chan[n]; bit cval = dScalar[31]; while ((dScalar &amp; (1 &lt;&lt; 31)) == cval &amp;&amp; cnt != 32 ) { cnt ++; dScalar = dScalar &lt;&lt; 1; } if ( (src0.chan[n] == 0xFFFFFFFF)    (src0.chan[n] == 0x00000000) ) { dst.chan[n] = 0xFFFFFFFF; } else { dst.chan[n] = cnt; } } }</pre>			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	N	N	N
Src Types	Dst Types		
D, UD	UD		
DWord	Bit	Description	
0..3	127:64	<b>RegSource</b>	
		Exists If:	([Operand Controls][Src0.RegFile]!='IMM')
	Format:	EU_INSTRUCTION_SOURCES_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>	
Exists If:		([Operand Controls][Src0.RegFile]='IMM')	
Format:	EU_INSTRUCTION_SOURCES_IMM32 [CHV, BSW]		

<b>fbh - Find First Bit from MSB Side</b>		
	63:32	<b>Operand Controls</b> Format: EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]
	31:0	<b>Header</b> Format: EU_INSTRUCTION_HEADER [CHV, BSW]



## Fraction

<b>frc - Fraction</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
<p>The frc instruction computes, component-wise, the truncate-to-minus-infinity fractional values of src0 and stores the results in dst. The results, in the range of [0.0, 1.0], are the fractional portion of the source data. The result is in the range [0.0, 1.0] irrespective of the rounding mode. Floating-point fraction computation follows the rules in the following tables, based on the current floating-point mode.</p>			
Format: [(pred)] frc[.cmod] (exec_size) dst src0			
<b>Workaround</b>			
<p>When the Rounding Mode in cr0.0 is not Round Down, the result from frc must be followed by compare and select instructions to avoid a result of 1.0. Those latter instructions must use the :ud type. For example:                      cmp.ne.f0.0 null r4:ud 0x3f800000:ud (f0.0)sel r5:f r4:ud 0x3f7ffff:ud</p>			
<b>Syntax</b>			
[(pred)] frc[.cmod] (exec_size) reg reg [(pred)] frc[.cmod] (exec_size) reg imm32			
<b>Pseudocode</b>			
Evaluate(WrEn); for ( n = 0; n < exec_size; n++ ) { if ( WrEn.chan[n] ) { dst.chan[n] = src0.chan[n] - floor(src0.chan[n]); } }			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	Y	N	Y
Src Types	Dst Types		
F	F		
DWord	Bit	Description	
0..3	127:64	<b>RegSource</b>	
		Exists If:	(([Operand Controls][Src0.RegFile]!='IMM')
	Format:	EU_INSTRUCTION_SOURCES_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>	
Exists If:		(([Operand Controls][Src0.RegFile]='IMM')	
Format:	EU_INSTRUCTION_SOURCES_IMM32 [CHV, BSW]		
63:32	<b>Operand Controls</b>		
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]	
31:0	<b>Header</b>		
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]	

## Goto

<b>goto - Goto</b>	
Project:	CHV, BSW
Source:	Eulsa
Length Bias:	4
<p>The goto instruction directs the instruction pointer to the offset specified by the UIP offset or to the next IP based on the BranchCtrl bit in the instruction. The active channels that are predicated on this instruction will take the IP + UIP path when BranchCtrl is set else the channels take IP + 1. The active channels that are not predicated on this instruction will be made inactive and waiting to be joined at the join IP. The join IP is IP + UIP when BranchCtrl is clear else it is the next IP.</p> <p>When there are no active channels the instruction pointer will move to IP + JIP.</p> <p>The goto instruction is used in conjunction with a join instruction. A goto deactivates some channels that are reactivated at some program-specified join instruction. See the join instruction for the activation rules.</p> <p>The goto and join instructions enable unstructured program control flow. These instructions must be used with additional care where dangling channels can result without proper compiler checks, meaning that it is expected that programs will navigate through these paths to reactivate the channels. Hardware does not provide native checks or reconvergence.</p> <p>The following table describes the two 32-bit instruction pointer offsets. Both the JIP and UIP are signed 32-bit numbers, added to IP pre-increment. In GEN binary, JIP and UIP are at locations src0 and src1 and must be of type DW (signed DWord integer).</p> <p>If SPF is ON, none of the PcIP are updated.</p>	
Format: [(pred)] goto (exec_size) JIP UIP BranchCtrl	
<b>Restriction</b>	
Cannot have a goto in the body and the corresponding join in the function or the subroutine. Similarly the brd and brc.	
<b>Syntax</b>	
[(pred)] goto (exec_size) imm32 imm32 BranchCtrl	
<b>Pseudocode</b>	
<pre> Evaluate(WrEn); for ( n = 0; n &lt; exec size; n++ ) { if ( WrEn.chan[n] ) { // for the predicated active channels if ( BranchCtrl ) { PcIP[n] = IP + UIP; } else { PcIP[n] = IP + 1; } } else { // join IP, for the active non predicated channels if ( BranchCtrl ) { PcIP[n] = IP + 1; } else { PcIP[n] = IP + UIP; } } } if ( BranchCtrl ) { // if (PcIP != (IP + UIP) ) { // for all channels if (PcIP != (IP + 1) ) { // for all channels Jump(IP + JIP); } else { Jump(IP + 1); } } else { Jump(IP + UIP); } } else { // if (PcIP != (IP + 1) ) { // for all channels Jump(IP + JIP); } else { Jump(IP + 1); } } </pre>	
<b>Errata</b>	<b>Description</b>
	A goto instruction must not be followed by any instruction requiring register indirect access on source operands.

<b>goto - Goto</b>				
Predication	Conditional Modifier	Saturation	Source Modifier	
Y	N	N	N	
DWord	Bit	Description		
0..3	127:96	<b>JIP</b>		
		Project:	CHV, BSW	
	Format:	S31		
	The byte-aligned jump distance if a jump is taken for the channel.			
95:64	<b>UIP</b>			
	Project:	CHV, BSW		
	Format:	S31		
The byte aligned jump distance if a jump is taken for the instruction.				
63:32	<b>Operand Control</b>			
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]		
31:0	<b>Header</b>			
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]		

## GPGPU\_CSR\_BASE\_ADDRESS

<b>GPGPU_CSR_BASE_ADDRESS</b>									
Project:	CHV, BSW								
Source:	PRM								
Length Bias:	2								
The GPGPU_CSR_BASE_ADDRESS command sets the base pointers for EU and L3 to Context Save and Restore EU State and SLM for <b>GPGPU</b> mid.									
Programming Notes			Project						
Execution of this command causes a full pipeline flush, thus its use should be minimized for higher performance. State and instruction caches are flushed on completion of the flush.			CHV, BSW						
SW must always program PIPE_CONTROL with "CS Stall" and "Render Target Cache Flush Enable" set prior to programming GPGPU_CSR_BASE_ADDRESS command for GPGPU workloads i.e when pipeline select is GPGPU via PIPELINE_SELECT command. This is required to achieve better GPGPU preemption latencies for certain programming sequences. If programming PIPE_CONTROL has performance implications then preemption latencies can be trade off against performance by not implementing this programming note.			CHV, BSW						
DWord	Bit	Description							
0	31:29	<b>Command Type</b>							
		Default Value:	3h GFXPIPE						
		Format:	Opcode						
	28:27	<b>Command SubType</b>							
		Default Value:	0h GFXPIPE_COMMON						
		Format:	Opcode						
	26:24	<b>3D Command Opcode</b>							
		Default Value:	1h GFXPIPE_NONPIPELINED						
		Format:	Opcode						
	23:16	<b>3D Command Sub Opcode</b>							
		Default Value:	04h GPGPU_CSR_BASE_ADDRESS						
		Format:	Opcode						
15:8	<b>Reserved</b>								
	Format:	MBZ							
7:0	<b>DWord Length</b>								
	Format:	=n Total Length -2							
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> <th style="text-align: center;">Project</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">1h</td> <td style="text-align: center;">[Default]</td> <td>Excludes DWord(0,1)</td> <td style="text-align: center;">CHV, BSW</td> </tr> </tbody> </table>		Value	Name	Description	Project	1h	[Default]	Excludes DWord(0,1)
Value	Name	Description	Project						
1h	[Default]	Excludes DWord(0,1)	CHV, BSW						

<b>GPGPU_CSR_BASE_ADDRESS</b>						
1..2 <b>Project:</b> CHV, BSW	63:12	<b>GPGPU CSR Base Address High</b>				
		<table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[63:12]</td> </tr> </table>	Project:	CHV, BSW	Format:	GraphicsAddress[63:12]
		Project:	CHV, BSW			
	Format:	GraphicsAddress[63:12]				
Specifies the 256K-byte aligned base address for GPGPU context GraphicsAddress [63:48] are ignored by the HW and assumed to be in correct canonical form [63:48] == [47].						
11:0	<b>Reserved</b>					
		<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ
Project:	All					
Format:	MBZ					

## GPGPU\_WALKER

GPGPU_WALKER			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
Programming Notes			
If the threads spawned by this command are required to observe memory writes performed by threads spawned from a previous command, software must precede this command with a command that performs a memory flush (e.g., MI_FLUSH).			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h Media
		Format:	OpCode
	26:24	<b>Media Command Opcode</b>	
		Default Value:	1h GPGPU_WALKER
		Format:	OpCode
	23:16	<b>SubOpcode</b>	
Default Value:		05h GPGPU_WALKER SubOp	
Format:		OpCode	
15:11	<b>Reserved</b>		
	Format:	MBZ	
10	<b>Indirect Parameter Enable</b>		
	Format:	Enable	
If set, the values in DW 7, 10, 12 are ignored and replaced by the current values of the corresponding GPGPU_xxx MMIO registers:			
<ul style="list-style-type: none"> <li>• GPGPU_DISPATCHDIMX (instead of DW7)</li> <li>• GPGPU_DISPATCHDIMY (instead of DW10)</li> <li>• GPGPU_DISPATCHDIMZ (instead of DW12)</li> </ul>			
9	<b>Reserved</b>		
	Format:	MBZ	

<b>GPGPU_WALKER</b>										
	8	<p><b>Predicate Enable</b></p> <table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>If set, this command is executed (or not) depending on the current value of the MI Predicate internal state bit. This command is ignored only if <b>PredicateEnable</b> is set and the Predicate state bit is 0.</p>	Format:	Enable						
	Format:	Enable								
	7:0	<p><b>DWord Length</b></p> <table border="1"> <tr> <td>Format:</td> <td>=n Total Length - 2</td> </tr> </table> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0Dh</td> <td>DWORD_COUNT_n [Default]</td> <td>Excludes DWord (0,1)</td> </tr> </tbody> </table>	Format:	=n Total Length - 2	Value	Name	Description	0Dh	DWORD_COUNT_n [Default]	Excludes DWord (0,1)
Format:	=n Total Length - 2									
Value	Name	Description								
0Dh	DWORD_COUNT_n [Default]	Excludes DWord (0,1)								
1	31:8	<b>Reserved</b>								
	7:6	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ						
	Format:	MBZ								
5:0	<p><b>Interface Descriptor Offset</b></p> <table border="1"> <tr> <td>Format:</td> <td>U6</td> </tr> </table> <p>This field specifies the offset from the interface descriptor base pointer to the interface descriptor which will be applied to this object. It is specified in units of interface descriptors.</p>	Format:	U6							
Format:	U6									
2	31:17	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ						
	Format:	MBZ								
16:0	<p><b>Indirect Data Length</b></p> <table border="1"> <tr> <td>Format:</td> <td>U17 in bytes</td> </tr> </table> <p>This field provides the length in bytes of the indirect data. A value zero indicates that indirect data fetching is disabled - subsequently, the Indirect Data Start Address field is ignored. If Indirect Data is enabled, it is assumed that CURBE is not being used except for cross-thread constant data. This field must have the same alignment as the Indirect Object Data Start Address. It must be DQWord (32-byte) aligned. As the indirect data are sent directly to URB, the total size of Indirect data must be less than 63,488 (2048 URB lines - 64 lines for Interface Descriptors).</p> <table border="1"> <thead> <tr> <th>Workaround</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>The indirect payload is limited to 4032 bytes or less.</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Format:	U17 in bytes	Workaround	Project	The indirect payload is limited to 4032 bytes or less.	CHV, BSW			
Format:	U17 in bytes									
Workaround	Project									
The indirect payload is limited to 4032 bytes or less.	CHV, BSW									
3	31:6	<p><b>Indirect Data Start Address</b></p> <table border="1"> <tr> <td>Format:</td> <td>IndirectObjectOffset[31:6]</td> </tr> </table> <p>This field specifies the Graphics Memory starting address of the data to be loaded into the kernel for processing. This pointer is relative to the <b>Indirect Object Base Address</b>. Hardware ignores this field if indirect data is not present. Alignment of this address depends on the mode of operation. It is the 64-byte aligned address of the indirect data.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[0 - 512MB]</td> <td></td> <td>(Bits 31:29 MBZ)</td> </tr> </tbody> </table>	Format:	IndirectObjectOffset[31:6]	Value	Name	Description	[0 - 512MB]		(Bits 31:29 MBZ)
Format:	IndirectObjectOffset[31:6]									
Value	Name	Description								
[0 - 512MB]		(Bits 31:29 MBZ)								

<b>GPGPU_WALKER</b>														
	5:0	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ										
Format:	MBZ													
4	31:30	<p><b>SIMD Size</b></p> <p>This field determines the size of the payload and the number of bits of the execution mask that are expected. The kernel pointed to by the interface descriptor should match the SIMD declared here.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 70%;">Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>SIMD8</td> <td>8 LSBs of the execution mask are used</td> </tr> <tr> <td>1</td> <td>SIMD16</td> <td>16 LSBs used in execution mask</td> </tr> <tr> <td>2</td> <td>SIMD32</td> <td>32 bits of execution mask used</td> </tr> </tbody> </table>	Value	Name	Description	0	SIMD8	8 LSBs of the execution mask are used	1	SIMD16	16 LSBs used in execution mask	2	SIMD32	32 bits of execution mask used
		Value	Name	Description										
		0	SIMD8	8 LSBs of the execution mask are used										
		1	SIMD16	16 LSBs used in execution mask										
	2	SIMD32	32 bits of execution mask used											
	29:22	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ										
	Format:	MBZ												
	21:16	<p><b>Thread Depth Counter Maximum</b></p> <p>The maximum value of the thread depth counter. Since the counter starts at 0, the depth is this value + 1.  <b>(Thread_Depth_Max+1)*(Thread_Height_Max+1)*(Thread_Width_Max+1)</b> must equal <b>Number of Threads in GPGPU Thread Group</b> in the Interface Descriptor.</p>												
15:14	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ											
Format:	MBZ													
13:8	<p><b>Thread Height Counter Maximum</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>U6-1</td> </tr> </table> <p>The maximum value of the thread height counter. The height is this value + 1.</p>	Format:	U6-1											
Format:	U6-1													
7:6	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ											
Format:	MBZ													
5:0	<p><b>Thread Width Counter Maximum</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>U6-1</td> </tr> </table> <p>The maximum value of the thread width counter. The height is this value + 1.</p>	Format:	U6-1											
Format:	U6-1													
5	31:0	<p><b>Thread Group ID Starting X</b></p> <p>This is the initial value of the X component of the thread group. When X reaches the maximum value it rolls around to this value.</p>												
6	31:0	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ										
Format:	MBZ													
7	31:0	<p><b>Thread Group ID X Dimension</b></p> <p>The X dimension of the thread group (maximum X is dimension -1)</p>												
8	31:0	<p><b>Thread Group ID Starting Y</b></p> <p>This is the initial value of the Y component of the thread group. When Y reaches the maximum value it rolls around to this value.</p>												



<b>GPGPU_WALKER</b>		
9	31:0	<b>Reserved</b>
		Format: <span style="float: right;">MBZ</span>
10	31:0	<b>Thread Group ID Y Dimension</b> The Y dimension of the thread group (maximum Y is dimension -1)
11	31:0	<b>Thread Group ID Starting/Resume Z</b> This is the initial value of the Z component of the thread group.
12	31:0	<b>Thread Group ID Z Dimension</b> The Z dimension of the thread group (maximum Z is dimension -1)
13	31:0	<b>Right Execution Mask</b> The execution mask used for threads on the right (maximum X) of the thread group.
14	31:0	<b>Bottom Execution Mask</b> The execution mask used for threads on the bottom (maximum Y) of the thread group.

## Half Precision HI8DS Render Target Write MSD

<b>MSD_RTWH_HI8DS - Half Precision HI8DS Render Target Write MSD</b>			
Project:	CHV, BSW		
Source:	Render Cache DataPort		
Length Bias:	1		
Family:	Other		
Group:	Render Target R/W		
DWord	Bit	Description	
0	31	<b>Reserved</b>	
	30	<b>Message Precision Subtype</b>	
		Default Value:	1h
		Project:	CHV, BSW
		Format:	Opcode
			Half precision data message
29		<b>Reserved</b>	
		Project:	All
		Format:	MBZ
		Ignored	
28:25		<b>Message Length</b>	
		Project:	All
		Format:	U4
		Specifies the number of 256-bit GRF registers sent as the message payload (including the header). Valid value ranges are 1 to 15.	
24:20		<b>Response Length</b>	
		Project:	All
		Format:	U5
		Specifies the number of 256-bit GRF registers expected as the message response payload. Valid value ranges are 0 to 16.	
19		<b>Header Present</b>	
		Project:	All
		Format:	MDC_MHP [CHV, BSW]
		If set, indicates that the message includes the 2-register header.	

## MSD\_RTWH\_HI8DS - Half Precision HI8DS Render Target Write MSD

18	<b>Reserved</b>		
17:14	<b>Message Type</b>		
	Default Value:	0Ch	
	Project:	All	
	Format:	Opcode	
Render Target Write message			
13	<b>Reserved</b>		
12	<b>Last Render Target Select</b>		
	Project:	All	
	Format:	Enable	
<p>This bit must be set on the last render target write message sent for each group of pixels. For single render target pixel shaders, this bit is set on all render target write messages. For multiple render target pixel shaders, this bit is set only on messages sent to the last render target. This bit must be zero for SIMD8 Image Write message. In general, when threads are not launched by 3D FF, this bit must be zero.</p>			
<b>Programming Notes</b>			
<p>When a pixel shader has render target writes at finer granularity than the dispatch rate, last render target write to a null surface must be present at the dispatch rate with this bit set. In particular, if a kernel is dispatched at pixel rate and it only writes to render targets at sample-rate, it must include a pixel-rate render target write to a null surface with Last Render Target Select bit enabled.</p>			
11	<b>Slot Group Select</b>		
	Project:	All	
	Format:	MDC_RT_SGS [CHV, BSW]	
<p>This field selects whether slots 15:0 or slots 31:16 are used for bypassed data.</p>			
10:8	<b>Render Target Message Subtype</b>		
	Default Value:	3h	
	Project:	All	
	Format:	Opcode	
<p>SIMD8 dual source message. Use slots [15:8] for pixel enables, X/Y addresses, and oMask.</p>			
<b>Programming Notes</b>			
<p>The above slots indicated are within the 16 slots selected by Slot Group Select. If SLOTGRP_HI is selected, slots [31:24] are referenced instead of [15:8].</p>			
7:0	<b>Binding Table Index</b>		
	Project:	All	
	Format:	MDC_BTS [CHV, BSW]	
<p>Specifies the Binding Table Index for the message</p>			

## Half Precision LO8DS Render Target Write MSD

MSD_RTWH_LO8DS - Half Precision LO8DS Render Target Write MSD		
Project:	CHV, BSW	
Source:	Render Cache DataPort	
Length Bias:	1	
Family:	Other	
Group:	Render Target R/W	
DWord	Bit	Description
0	31	<b>Reserved</b>
		Project: All
		Format: MBZ
	Ignored	
	30	<b>Message Precision Subtype</b>
Default Value: 1h		
Project: CHV, BSW		
Format: Opcode		
Half precision data message		
29	<b>Reserved</b>	
28:25	<b>Message Length</b>	
	Project: All	
	Format: U4	
Specifies the number of 256-bit GRF registers sent as the message payload (including the header). Valid value ranges are 1 to 15.		
24:20	<b>Response Length</b>	
	Project: All	
	Format: U5	
Specifies the number of 256-bit GRF registers expected as the message response payload. Valid value ranges are 0 to 16.		
19	<b>Header Present</b>	
	Project: All	
	Format: MDC_MHP [CHV, BSW]	
If set, indicates that the message includes the 2-register header.		

## MSD\_RTWH\_LO8DS - Half Precision LO8DS Render Target Write MSD

18	<b>Reserved</b>		
17:14	<b>Message Type</b>		
	Default Value:	0Ch	
	Project:	All	
	Format:	Opcode	
Render Target Write message			
13	<b>Reserved</b>		
12	<b>Last Render Target Select</b>		
	Project:	All	
	Format:	Enable	
<p>This bit must be set on the last render target write message sent for each group of pixels. For single render target pixel shaders, this bit is set on all render target write messages. For multiple render target pixel shaders, this bit is set only on messages sent to the last render target. This bit must be zero for SIMD8 Image Write message. In general, when threads are not launched by 3D FF, this bit must be zero.</p>			
<b>Programming Notes</b>			
<p>When a pixel shader has render target writes at finer granularity than the dispatch rate, last render target write to a null surface must be present at the dispatch rate with this bit set. In particular, if a kernel is dispatched at pixel rate and it only writes to render targets at sample-rate, it must include a pixel-rate render target write to a null surface with Last Render Target Select bit enabled.</p>			
11	<b>Slot Group Select</b>		
	Project:	All	
	Format:	MDC_RT_SGS [CHV, BSW]	
This field selects whether slots 15:0 or slots 31:16 are used for bypassed data.			
10:8	<b>Render Target Message Subtype</b>		
	Default Value:	2h	
	Project:	All	
	Format:	Opcode	
SIMD8 dual source message. Use slots [7:0] for pixel enables, X/Y addresses, and oMask.			
<b>Programming Notes</b>			
The above slots indicated are within the 16 slots selected by Slot Group Select. If SLOTGRP_HI is selected, slots [23:16] are referenced instead of [7:0].			
7:0	<b>Binding Table Index</b>		
	Project:	All	
	Format:	MDC_BTS [CHV, BSW]	
Specifies the Binding Table Index for the message			

## Half Precision REP16 Render Target Write MSD

MSD_RTWH_REP16 - Half Precision REP16 Render Target Write MSD		
Project:	CHV, BSW	
Source:	Render Cache DataPort	
Length Bias:	1	
Family:	Other	
Group:	Render Target R/W	
DWord	Bit	Description
0	31	<b>Reserved</b>
		Project: All
		Format: MBZ
	Ignored	
	30	<b>Message Precision Subtype</b>
Default Value: 1h		
Project: CHV, BSW		
Format: Opcode		
Half precision data message		
29	<b>Reserved</b>	
	Project: All	
	Format: MBZ	
Ignored		
28:25	<b>Message Length</b>	
	Project: All	
	Format: U4	
Specifies the number of 256-bit GRF registers sent as the message payload (including the header). Valid value ranges are 1 to 15.		
24:20	<b>Response Length</b>	
	Project: All	
	Format: U5	
Specifies the number of 256-bit GRF registers expected as the message response payload. Valid value ranges are 0 to 16.		

## MSD\_RTWH\_REP16 - Half Precision REP16 Render Target Write MSD

19	<b>Header Present</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_MHP [CHV, BSW]</td> </tr> </table>	Project:	All	Format:	MDC_MHP [CHV, BSW]	<p>If set, indicates that the message includes the 2-register header.</p>		
Project:	All								
Format:	MDC_MHP [CHV, BSW]								
18	<b>Reserved</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ	Ignored		
Project:	CHV, BSW								
Format:	MBZ								
17:14	<b>Message Type</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td>0Ch</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table>	Default Value:	0Ch	Project:	All	Format:	Opcode	Render Target Write message
Default Value:	0Ch								
Project:	All								
Format:	Opcode								
13	<b>Reserved</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ	Ignored		
Project:	CHV, BSW								
Format:	MBZ								
12	<b>Last Render Target Select</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table>	Project:	All	Format:	Enable	<p>This bit must be set on the last render target write message sent for each group of pixels. For single render target pixel shaders, this bit is set on all render target write messages. For multiple render target pixel shaders, this bit is set only on messages sent to the last render target. This bit must be zero for SIMD8 Image Write message. In general, when threads are not launched by 3D FF, this bit must be zero.</p> <div style="border: 1px solid black; background-color: #e6f2ff; padding: 5px; text-align: center; margin: 10px 0;"><b>Programming Notes</b></div> <p>When a pixel shader has render target writes at finer granularity than the dispatch rate, last render target write to a null surface must be present at the dispatch rate with this bit set. In particular, if a kernel is dispatched at pixel rate and it only writes to render targets at sample-rate, it must include a pixel-rate render target write to a null surface with Last Render Target Select bit enabled.</p>		
Project:	All								
Format:	Enable								
11	<b>Slot Group Select</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_RT_SGS [CHV, BSW]</td> </tr> </table>	Project:	All	Format:	MDC_RT_SGS [CHV, BSW]	This field selects whether slots 15:0 or slots 31:16 are used for bypassed data.		
Project:	All								
Format:	MDC_RT_SGS [CHV, BSW]								

## MSD\_RTWH\_REP16 - Half Precision REP16 Render Target Write MSD

10:8	<b>Render Target Message Subtype</b>	
	Default Value:	1h
	Project:	All
	Format:	Opcode
	SIMD16 Single source message with replicated data. Use slots [15:0] for pixel enables, X/Y addresses, and oMask.	
	<b>Programming Notes</b>	
	The above slots indicated are within the 16 slots selected by Slot Group Select. If SLOTGRP_HI is selected, slots [31:16] are referenced instead of [15:0].	
7:0	<b>Binding Table Index</b>	
	Project:	All
	Format:	MDC_BTS [CHV, BSW]
	Specifies the Binding Table Index for the message	



## Half Precision SIMD8 Render Target Write MSD

<b>MSD_RTWH_SIMD8 - Half Precision SIMD8 Render Target Write MSD</b>			
Project:	CHV, BSW		
Source:	Render Cache DataPort		
Length Bias:	1		
Family:	Other		
Group:	Render Target R/W		
DWord	Bit	Description	
0	31	<b>Reserved</b>	
	30	<b>Message Precision Subtype</b>	
		Default Value:	1h
		Project:	CHV, BSW
		Format:	Opcode
			Half precision data message
29		<b>Reserved</b>	
		Project:	All
		Format:	MBZ
		Ignored	
28:25		<b>Message Length</b>	
		Project:	All
		Format:	U4
		Specifies the number of 256-bit GRF registers sent as the message payload (including the header). Valid value ranges are 1 to 15.	
24:20		<b>Response Length</b>	
		Project:	All
		Format:	U5
		Specifies the number of 256-bit GRF registers expected as the message response payload. Valid value ranges are 0 to 16.	
19		<b>Header Present</b>	
		Project:	All
		Format:	MDC_MHP [CHV, BSW]
		If set, indicates that the message includes the 2-register header.	

## MSD\_RTWH\_SIMD8 - Half Precision SIMD8 Render Target Write MSD

18	<b>Reserved</b>		
17:14	<b>Message Type</b>		
	Default Value:	0Ch	
	Project:	All	
	Format:	Opcode	
Render Target Write message			
13	<b>Reserved</b>		
12	<b>Last Render Target Select</b>		
	Project:	All	
	Format:	Enable	
<p>This bit must be set on the last render target write message sent for each group of pixels. For single render target pixel shaders, this bit is set on all render target write messages. For multiple render target pixel shaders, this bit is set only on messages sent to the last render target. This bit must be zero for SIMD8 Image Write message. In general, when threads are not launched by 3D FF, this bit must be zero.</p>			
<b>Programming Notes</b>			
<p>When a pixel shader has render target writes at finer granularity than the dispatch rate, last render target write to a null surface must be present at the dispatch rate with this bit set. In particular, if a kernel is dispatched at pixel rate and it only writes to render targets at sample-rate, it must include a pixel-rate render target write to a null surface with Last Render Target Select bit enabled.</p>			
11	<b>Slot Group Select</b>		
	Project:	All	
	Format:	MDC_RT_SGS [CHV, BSW]	
This field selects whether slots 15:0 or slots 31:16 are used for bypassed data.			
10:8	<b>Render Target Message Subtype</b>		
	Default Value:	4h	
	Project:	All	
	Format:	Opcode	
SIMD8 single source message. Use slots [7:0] for pixel enables, X/Y addresses, and oMask.			
<b>Programming Notes</b>			
The above slots indicated are within the 16 slots selected by Slot Group Select. If SLOTGRP_HI is selected, slots [23:16] are referenced instead of [7:0].			
7:0	<b>Binding Table Index</b>		
	Project:	All	
	Format:	MDC_BTS [CHV, BSW]	
Specifies the Binding Table Index for the message			

## Half Precision SIMD16 Render Target Write MSD

MSD_RTWH_SIMD16 - Half Precision SIMD16 Render Target Write MSD		
Project:	CHV, BSW	
Source:	Render Cache DataPort	
Length Bias:	1	
Family:	Other	
Group:	Render Target R/W	
DWord	Bit	Description
0	31	<b>Reserved</b>
		Project: All
		Format: MBZ
	Ignored	
	30	<b>Message Precision Subtype</b>
Default Value: 1h		
Project: CHV, BSW		
Format: Opcode		
Half precision data message		
29	<b>Reserved</b>	
	Project: All	
	Format: MBZ	
Ignored		
28:25	<b>Message Length</b>	
	Project: All	
	Format: U4	
Specifies the number of 256-bit GRF registers sent as the message payload (including the header). Valid value ranges are 1 to 15.		
24:20	<b>Response Length</b>	
	Project: All	
	Format: U5	
Specifies the number of 256-bit GRF registers expected as the message response payload. Valid value ranges are 0 to 16.		

## MSD\_RTWH\_SIMD16 - Half Precision SIMD16 Render Target Write MSD

19	<b>Header Present</b>	
	Project:	All
	Format:	MDC_MHP [CHV, BSW]
	If set, indicates that the message includes the 2-register header.	
18	<b>Reserved</b>	
	Project:	CHV, BSW
	Format:	MBZ
Ignored		
17:14	<b>Message Type</b>	
	Default Value:	0Ch
	Project:	All
	Format:	Opcode
Render Target Write message		
13	<b>Reserved</b>	
	Project:	CHV, BSW
	Format:	MBZ
Ignored		
12	<b>Last Render Target Select</b>	
	Project:	All
	Format:	Enable
	<p>This bit must be set on the last render target write message sent for each group of pixels. For single render target pixel shaders, this bit is set on all render target write messages. For multiple render target pixel shaders, this bit is set only on messages sent to the last render target. This bit must be zero for SIMD8 Image Write message. In general, when threads are not launched by 3D FF, this bit must be zero.</p>	
<b>Programming Notes</b>		
<p>When a pixel shader has render target writes at finer granularity than the dispatch rate, last render target write to a null surface must be present at the dispatch rate with this bit set. In particular, if a kernel is dispatched at pixel rate and it only writes to render targets at sample-rate, it must include a pixel-rate render target write to a null surface with Last Render Target Select bit enabled.</p>		
11	<b>Slot Group Select</b>	
	Project:	All
	Format:	MDC_RT_SGS [CHV, BSW]
This field selects whether slots 15:0 or slots 31:16 are used for bypassed data.		

## MSD\_RTWH\_SIMD16 - Half Precision SIMD16 Render Target Write MSD

10:8	<b>Render Target Message Subtype</b>	
	Default Value:	0h
	Project:	All
	Format:	Opcode
SIMD16 Single source message. Use slots [15:0] for pixel enables, X/Y addresses, and oMask.		
<b>Programming Notes</b>		
The above slots indicated are within the 16 slots selected by Slot Group Select. If SLOTGRP_HI is selected, slots [31:16] are referenced instead of [15:0].		
7:0	<b>Binding Table Index</b>	
	Project:	All
	Format:	MDC_BTS [CHV, BSW]
Specifies the Binding Table Index for the message		

# Halt

<b>halt - Halt</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
Description			
<p>The halt instruction temporarily suspends execution for all enabled compute channels. Upon execution, the enabled channels are sent to the instruction at (IP + UIP), if all channels are enabled at HALT, jump to the instruction at (IP + JIP). If the halt instruction is not inside any conditional code block, the values of JIP and UIP should be the same. If the halt instruction is inside a conditional code block, the UIP should be the end of the program and the JIP should be the end of the inner most conditional code block. The UIP must point to a HALT Instruction. If SPF is ON, the UIP must be used to update IP; JIP is not used in this case.</p> <p>The following table describes the two 32-bit instruction pointer offsets. Both the JIP and UIP are signed 32-bit numbers, added to IP pre-increment. In GEN binary, JIP and UIP are at locations src0 and src1 and must be of type DW (signed DWord integer). When the offsets are immediate, src0 regfile must be immediate.</p> <p>Format: [(pred)] halt (exec_size) JIP UIP</p>			
Restriction			
dst and src0 must be NULL.			
Syntax	Project		
[(pred)] halt (exec_size) imm32 imm32	CHV, BSW		
Pseudocode			
<pre>Evaluate(WrEn); for ( n = 0; n &lt; 32; n++ ) { if ( WrEn.channel[n] ) { PclP[n] = IP + UIP; else { PclP[n] = IP + 1; } } if ( PclP != (IP + 1) ) { // for all channels Jump(IP + JIP); }</pre>			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	N	N	N
DWord	Bit	Description	
0.3	127:96	<b>JIP</b> Project: CHV, BSW Format: S31 The byte-aligned jump distance if a jump is taken for the channel.	
	95:64	<b>UIP</b> Project: CHV, BSW Format: S31 The byte aligned jump distance if a jump is taken for the instruction.	

<b>halt - Halt</b>		
	63:32	<b>Operand Control</b> Format: EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]
	31:0	<b>Header</b> Format: EU_INSTRUCTION_HEADER [CHV, BSW]

## HCP\_BSD\_OBJECT

<b>HCP_BSD_OBJECT</b>			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>The HCP is selected with the <b>Media Instruction Opcode "7h"</b> for all HCP Commands. Each HCP command has assigned a media instruction command as defined in DWord 0, BitField 22:16.</p>			
<p>The HCP_BSD_OBJECT command fetches the HEVC bit stream for a slice starting with the first byte in the slice. The bit stream ends with the last non-zero bit of the frame and does not include any zero-padding at the end of the bit stream. There can be multiple slices in a HEVC frame and thus this command can be issued multiple times per frame.</p>			
<p>The HCP_BSD_OBJECT command must be the last command issued in the sequence of batch commands before the HCP starts decoding. Prior to issuing this command, it is assumed that all configuration parameters in the HCP have been loaded including workload configuration registers and configuration tables. When this command is issued, the HCP is waiting for bit stream data to be presented to the shift register.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline Type</b>	
		Default Value:	2h
		Format:	OpCode
	26:23	<b>Media Instruction Opcode</b>	
		Default Value:	7h Codec/Engine Name
		Format:	OpCode
		Codec/Engine Name = HCP = 7h	
	22:16	<b>Media Instruction Command</b>	
		Default Value:	20h HCP_BSD_OBJECT_STATE
		Format:	OpCode
	15:12	<b>Reserved</b>	
		Format:	MBZ
11:0	<b>Dword Length</b>		
	Format:	U12	
	(Excludes Dwords 0, 1).		
	<b>Value</b>	<b>Name</b>	
1h			



<b>HCP_BSD_OBJECT</b>									
1	31:0	<b>Indirect BSD Data Length</b>							
		Project:	CHV, BSW						
		Format:	U32						
		<p>Specifies the length in bytes of the bitstream data for the current slice. It includes the first byte of the slice and the last non-zero byte of the in the slice. Specifically, the zero-padding bytes (if present) and the next start-code are excluded.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> <th style="text-align: center;">Project</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">[0,268435455]</td> <td>Data_Length_with_28_bits_only</td> <td>Valid range is only from 0 to 268435455, which is corresponding to lower 28 bits. This restriction is for old project which only use 28 bits data length.</td> <td style="text-align: center;">CHV, BSW</td> </tr> </tbody> </table>		Value	Name	Description	Project	[0,268435455]	Data_Length_with_28_bits_only
Value	Name	Description	Project						
[0,268435455]	Data_Length_with_28_bits_only	Valid range is only from 0 to 268435455, which is corresponding to lower 28 bits. This restriction is for old project which only use 28 bits data length.	CHV, BSW						
2	31:29	<b>Reserved</b>							
		Format:	MBZ						
	28:0	<b>Indirect Data Start Address</b>							
	Format:	U29	<p>Specifies the byte-aligned graphics memory starting address of the slice bit stream relative to the <b>BSD Indirect Object Base Address</b>.</p>						

## HCP\_IND\_OBJ\_BASE\_ADDR\_STATE

<b>HCP_IND_OBJ_BASE_ADDR_STATE</b>			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>The HCP is selected with the <b>Media Instruction Opcode "7h"</b> for all HCP Commands. Each HCP command has assigned a media instruction command as defined in DWord 0, BitField 22:16.</p> <p>The HCP_IND_OBJ_BASE_ADDR_STATE command is used to define the indirect object base address of the stream in graphics memory. This is a frame level command. (Is it frame or picture level?) This is a picture level state command and is issued in both encoding and decoding processes.</p>			
<b>Compressed Header Format</b>			
<b>Fields</b>	<b>Bits</b>		
Bin	0	Kernel Binarized Syntax	
Probability select	1	0 -> indicates probability 128 1 -> indicates probability 256	
Repeat to pack a Cacheline			
<b>Partition1 and TileSize record</b>			
<b>Fields</b>	<b>Bits</b>		
Tile Size	31:0	Partition1 Size is 16-bit value, Tile Size is 32-bit value	
AddressOffset	63:32	Cacheline Address Offset to be Modified	
Offset	69:64	Byte offset to be Modified	
16-bit vs 32-bit update	70	0: Update 16-bit; 1: Update 32-bit	
Reserved	511:71		
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline Type</b>	
		Default Value:	2h
		Format:	OpCode
	26:23	<b>Media Instruction Opcode</b>	
		Default Value:	7h Codec/Engine Name
		Format:	OpCode
Codec/Engine Name = HCP = 7h			

<b>HCP_IND_OBJ_BASE_ADDR_STATE</b>									
	22:16	<b>Media Instruction Command</b> <table border="1"> <tr> <td>Default Value:</td> <td>3h HCP_IND_OBJ_BASE_ADDR_STATE</td> </tr> <tr> <td>Format:</td> <td>OpCode</td> </tr> </table>	Default Value:	3h HCP_IND_OBJ_BASE_ADDR_STATE	Format:	OpCode			
	Default Value:	3h HCP_IND_OBJ_BASE_ADDR_STATE							
	Format:	OpCode							
15:12	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ						
Format:	MBZ								
11:0	<b>Dword Length</b> <table border="1"> <tr> <td>Format:</td> <td>=n</td> </tr> </table> <p>(Excludes Dwords 0, 1).</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>4h</td> <td></td> <td>CHV, BSW</td> </tr> </tbody> </table>	Format:	=n	Value	Name	Project	4h		CHV, BSW
Format:	=n								
Value	Name	Project							
4h		CHV, BSW							
1..2 <b>Project:</b> All	63:0	<b>HCP Indirect Bitstream Object Base Address</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>SplitBaseAddress4KByteAligned</td> </tr> </table> <p>Specifies the 4K-byte aligned memory base address for the read-only indirect data object pointed in the HCP_BSD_OBJECT command for fetching (reading) the compressed Slice Data.</p>	Project:	All	Format:	SplitBaseAddress4KByteAligned			
Project:	All								
Format:	SplitBaseAddress4KByteAligned								
3 <b>Project:</b> All	31:0	<b>HCP Indirect Bitstream Object Memory Address Attributes</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MemoryAddressAttributes [CHV, BSW]</td> </tr> </table>	Project:	All	Format:	MemoryAddressAttributes [CHV, BSW]			
Project:	All								
Format:	MemoryAddressAttributes [CHV, BSW]								
4..5 <b>Project:</b> All	63:0	<b>HCP Indirect Bitstream Object Access Upper Bound</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>SplitBaseAddress4KByteAligned</td> </tr> </table> <p>Decoder only.</p> <p>This field specifies the 4K-byte aligned maximum memory address access by the indirect data object in the HCP_BSD_OBJECT command for the slice bit stream. Indirect data accessed at this address or greater will cause the HCP to stop issuing requests to the GAC and the BSP VLD will then only receive zeros until a slice done is received.</p> <p>Setting this field to 0 will cause this range to be ignored by the HCP.</p>	Project:	All	Format:	SplitBaseAddress4KByteAligned			
Project:	All								
Format:	SplitBaseAddress4KByteAligned								
6..13 <b>Project:</b> CHV, BSW	31:0	<b>Reserved</b> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ			
Project:	CHV, BSW								
Format:	MBZ								

## HCP\_PIC\_STATE

<b>HCP_PIC_STATE</b>			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>The HCP is selected with the <b>Media Instruction Opcode "7h"</b> for all HCP Commands. Each HCP command has assigned a media instruction command as defined in DWord 0, BitField 22:16.</p> <p>This is a picture level command and is issued only once per workload for both encoding and decoding processes.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline Type</b>	
		Default Value:	2h
		Format:	OpCode
	26:23	<b>Media Instruction Opcode</b>	
		Default Value:	7h Codec/Engine Name
		Format:	OpCode
		Codec/Engine Name = HCP = 7h	
22:16	<b>Media Instruction Command</b>		
	Default Value:	10h HCP_PIC_STATE	
	Format:	OpCode	
15:12	<b>Reserved</b>		
	Format:	MBZ	
11:0	<b>Dword Length</b>		
	Format:	=n	
	(Excludes Dwords 0, 1).		
	<b>Value</b>	<b>Name</b>	
	11h		
1	31:26	<b>Reserved</b>	
		Project:	CHV, BSW
		Format:	MBZ

<b>HCP_PIC_STATE</b>		
25:16	<b>FrameHeightInMinCbMinus1</b>	
	Project: CHV, BSW	
	Format: U10	
	Specifies the height of each decoded picture in units of minimum coding block size.	
	<b>Value</b>	<b>Name</b>
	[0-4122]	
	<b>Programming Notes</b>	
	The decoded picture height in units of luma samples equals	
	<ul style="list-style-type: none"> <li>• <math>(\text{FrameHeightInMinCbMinus1} + 1) *</math></li> <li>• <math>(1 \ll (\log_2\_min\_coding\_block\_size\_minus3 + 3))</math></li> </ul>	
	In CHV, BSW, the maximum frame height being support is 7968 pixels only	CHV, BSW
14:10	<b>Reserved</b>	
9:0	<b>FrameWidthInMinCbMinus1</b>	
	Project: CHV, BSW	
	Format: U10	
	Specifies the width of each decoded picture in units of minimum coding block size.	
	<b>Value</b>	<b>Name</b>
	[0-4122]	
	<b>Programming Notes</b>	
	The decoded picture width in units of luma samples equals	
	<ul style="list-style-type: none"> <li>• <math>(\text{FrameWidthInMinCbMinus1} + 1) *</math></li> <li>• <math>(1 \ll (\log_2\_min\_coding\_block\_size\_minus3 + 3))</math></li> </ul>	
2	<b>Reserved</b>	
	Project:	
	Format: MBZ	
	<b>MaxPCMSize</b>	
	Format: U2	
	Specifies the largest allowed PCM coding block size.	
	<b>Value</b>	<b>Name</b>
	3	64x64
	2	32x32
	1	16x16
0	8x8	

<b>HCP_PIC_STATE</b>											
9:8	<b>MinPCMSize</b> Format: <span style="float: right;">U2</span> Specifies the smallest allowed PCM coding block size.										
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">3</td> <td>64x64</td> </tr> <tr> <td style="text-align: center;">2</td> <td>32x32</td> </tr> <tr> <td style="text-align: center;">1</td> <td>16x16</td> </tr> <tr> <td style="text-align: center;">0</td> <td>8x8</td> </tr> </tbody> </table>	Value	Name	3	64x64	2	32x32	1	16x16	0	8x8
	Value	Name									
	3	64x64									
2	32x32										
1	16x16										
0	8x8										
7:6	<b>MaxTUSize</b> Format: <span style="float: right;">U2</span> Specifies the largest allowed transform block size.										
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">3</td> <td>32x32</td> </tr> <tr> <td style="text-align: center;">2</td> <td>16x16</td> </tr> <tr> <td style="text-align: center;">1</td> <td>8x8</td> </tr> <tr> <td style="text-align: center;">0</td> <td>4x4</td> </tr> </tbody> </table>	Value	Name	3	32x32	2	16x16	1	8x8	0	4x4
	Value	Name									
	3	32x32									
2	16x16										
1	8x8										
0	4x4										
5:4	<b>MinTUSize</b> Format: <span style="float: right;">U2</span> Specifies the smallest allowed transform block size.										
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">3</td> <td>32x32</td> </tr> <tr> <td style="text-align: center;">2</td> <td>16x16</td> </tr> <tr> <td style="text-align: center;">1</td> <td>8x8</td> </tr> <tr> <td style="text-align: center;">0</td> <td>4x4</td> </tr> </tbody> </table>	Value	Name	3	32x32	2	16x16	1	8x8	0	4x4
	Value	Name									
	3	32x32									
2	16x16										
1	8x8										
0	4x4										
3:2	<b>CtbSize (LCUSize)</b> Format: <span style="float: right;">U2</span> Specifies the coding tree block size.										
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">3</td> <td>64x64</td> </tr> <tr> <td style="text-align: center;">2</td> <td>32x32</td> </tr> <tr> <td style="text-align: center;">1</td> <td>16x16</td> </tr> <tr> <td style="text-align: center;">0</td> <td>illegal/reserved</td> </tr> </tbody> </table>	Value	Name	3	64x64	2	32x32	1	16x16	0	illegal/reserved
	Value	Name									
	3	64x64									
2	32x32										
1	16x16										
0	illegal/reserved										
<b>Programming Notes</b>											
LCU is restricted based on the picture size.											

<b>HCP_PIC_STATE</b>														
	1:0	<p><b>MinCUSize</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U2</td> </tr> </table> <p>Specifies the smallest coding block size.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>3</td> <td>64x64</td> </tr> <tr> <td>2</td> <td>32x32</td> </tr> <tr> <td>1</td> <td>16x16</td> </tr> <tr> <td>0</td> <td>8x8</td> </tr> </tbody> </table>	Format:	U2	Value	Name	3	64x64	2	32x32	1	16x16	0	8x8
	Format:	U2												
Value	Name													
3	64x64													
2	32x32													
1	16x16													
0	8x8													
3	31:3	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Project:</td> <td style="width: 30%;"></td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:		Format:	MBZ								
	Project:													
	Format:	MBZ												
2	<p><b>InsertTestFlag</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U1</td> </tr> </table> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>[Default]</td> </tr> <tr> <td>1h</td> <td></td> </tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>Encoder only. CABAC 0 Word Insertion Test Enable (Encoder Only) This bit will modify CABAC K equation so that a positive K value can be generated easily. This is done for validation purpose only. In normal usage this bit should be set to 0. Regular equation for generating 'K' value when CABAC 0 Word Insertion Test Enable is set to 0. <math>K = \{ [ ((96 * pic\_bin\_count()) - (RawMinCUBits * PicSizeInMinCUs * 3) + 1023) / 1024 ] - bytes\_in\_picture \} / 3</math> Modified equation when CABAC 0 Word Insertion Test Enable bit set to 1. <math>K = \{ [ ((1536 * pic\_bin\_count()) - (RawMinCUBits * PicSizeInMinCUs * 3) + 1023) / 1024 ] - bytes\_in\_picture \} / 3</math></p>	Format:	U1	Value	Name	0h	[Default]	1h						
Format:	U1													
Value	Name													
0h	[Default]													
1h														
1	<p><b>CurPicIsl</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U1</td> </tr> </table> <p>Specifies that the current picture is comprised solely of I slices and that there are no P or B slices in the picture.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 20%;">Value</th> <th style="width: 80%;">Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Current picture has at least one P or B slice</td> </tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>This bit should be set to "0".                      Note: The value of "1" setting ("Current picture is comprised solely of I slices") is REMOVED.                      This bit is used for hardware optimization only. There is not enough information to set this bit to "1" correctly.</p>	Format:	U1	Value	Name	0	Current picture has at least one P or B slice							
Format:	U1													
Value	Name													
0	Current picture has at least one P or B slice													
	0	<p><b>ColPicIsl</b></p>												

<b>HCP_PIC_STATE</b>														
		<table border="1"> <tr> <td>Format:</td> <td>U1</td> </tr> <tr> <td colspan="2">Specifies that the collocated picture is comprised solely of I slices and that there are no P or B slices in the picture.</td> </tr> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> <tr> <td style="text-align: center;">0</td> <td>Collocated picture has at least one P or B slice</td> </tr> <tr> <th colspan="2" style="text-align: center;">Programming Notes</th> </tr> <tr> <td colspan="2">This bit should be set to "0". Note: The value of "1" setting ("Collocated picture is comprised solely of I slices") is REMOVED. This bit is used for hardware optimization only. There is not enough information to set this bit to "1" correctly.</td> </tr> </table>	Format:	U1	Specifies that the collocated picture is comprised solely of I slices and that there are no P or B slices in the picture.		Value	Name	0	Collocated picture has at least one P or B slice	Programming Notes		This bit should be set to "0". Note: The value of "1" setting ("Collocated picture is comprised solely of I slices") is REMOVED. This bit is used for hardware optimization only. There is not enough information to set this bit to "1" correctly.	
Format:	U1													
Specifies that the collocated picture is comprised solely of I slices and that there are no P or B slices in the picture.														
Value	Name													
0	Collocated picture has at least one P or B slice													
Programming Notes														
This bit should be set to "0". Note: The value of "1" setting ("Collocated picture is comprised solely of I slices") is REMOVED. This bit is used for hardware optimization only. There is not enough information to set this bit to "1" correctly.														
4	31:28	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ										
	Format:	MBZ												
	27	<b>CU packet structure</b>												
	26	<b>strong_intra_smoothing_enable_flag</b> <table border="1"> <tr> <td>Format:</td> <td>U1</td> </tr> </table>	Format:	U1										
	Format:	U1												
	25	<b>transquant_bypass_enable_flag</b> <table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> <tr> <td style="text-align: center;">0</td> <td>Disable</td> <td>cu_transquant_bypass is not supported</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Enable</td> <td>cu_transquant_bypass is supported</td> </tr> </table>	Format:	Enable	Value	Name	Description	0	Disable	cu_transquant_bypass is not supported	1	Enable	cu_transquant_bypass is supported	
	Format:	Enable												
	Value	Name	Description											
	0	Disable	cu_transquant_bypass is not supported											
	1	Enable	cu_transquant_bypass is supported											
24	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ											
Format:	MBZ													
23	<b>amp_enabled_flag</b> <table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> <tr> <td style="text-align: center;">0</td> <td>Disable</td> <td>Asymmetric motion partitions cannot be used in coding tree blocks.</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Enable</td> <td>Support asymmetric motion partitions, i.e. PartMode equal to PART_2NxN, PART_2NxN, PART_nLx2N, or PART_nRx2N.</td> </tr> </table>	Format:	Enable	Value	Name	Description	0	Disable	Asymmetric motion partitions cannot be used in coding tree blocks.	1	Enable	Support asymmetric motion partitions, i.e. PartMode equal to PART_2NxN, PART_2NxN, PART_nLx2N, or PART_nRx2N.		
Format:	Enable													
Value	Name	Description												
0	Disable	Asymmetric motion partitions cannot be used in coding tree blocks.												
1	Enable	Support asymmetric motion partitions, i.e. PartMode equal to PART_2NxN, PART_2NxN, PART_nLx2N, or PART_nRx2N.												
22	<b>transform_skip_enabled_flag</b> <table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> <tr> <td style="text-align: center;">0</td> <td>Disable</td> <td>transform_skip_flag is not supported in the residual coding</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Enable</td> <td>transform_skip_flag is supported</td> </tr> </table>	Format:	Enable	Value	Name	Description	0	Disable	transform_skip_flag is not supported in the residual coding	1	Enable	transform_skip_flag is supported		
Format:	Enable													
Value	Name	Description												
0	Disable	transform_skip_flag is not supported in the residual coding												
1	Enable	transform_skip_flag is supported												
21	<b>BottomField</b>													



<b>HCP_PIC_STATE</b>		
	Format:	U1
	<b>Value</b>	<b>Name</b>
	0	Bottom Field
	1	Top Field
<b>Programming Notes</b>		
Must be zero for encoder only		
20	<b>FieldPic</b>	
	Format:	U1
	<b>Value</b>	<b>Name</b>
	0	Video Frame
	1	Video Field
<b>Programming Notes</b>		
Must be zero for encoder only.		
19	<b>weighted_pred_flag</b>	
	Format:	U1
18	<b>weighted_bipred_flag</b>	
	Format:	U1
17	<b>tiles_enabled_flag</b>	
	Format:	U1
16	<b>entropy_coding_sync_enabled_flag</b>	
	Format:	U1
15	<b>loop_filter_across_tiles_enabled_flag</b>	
	Format:	U1
14	<b>Reserved</b>	
	Format:	MBZ
13	<b>sign_data_hiding_flag</b>	
	Format:	Enable
	<b>Value</b>	<b>Name</b>
	0	Disable
	1	Enable
	<b>Description</b>	
	Specifies that sign bit hiding is disabled.	
	Specifies that sign bit hiding is enabled.	
<b>Programming Notes</b>		

<b>HCP_PIC_STATE</b>			
	Currently not supported in encoder, so must be set to 0 for encoding session.		
12:10	<b>log2_parallel_merge_level_minus2</b>		
	Format:	U3	
	<b>Value</b>	<b>Name</b> <b>Programming Notes</b>	
	[0,4]	Valid Range      The value of log2_parallel_merge_level_minus2 shall be in the range of 0 to Log2CtbSizeYCbLog2SizeY - 2, inclusive.	
	<b>Programming Notes</b>		
For encoder, always set to 0 (Intel restriction).			
9	<b>constrained_intra_pred_flag</b>		
	Format:	U1	
	<b>Programming Notes</b>		
For encoder, always set to 0 to disable this (Intel restriction).			
8	<b>pcm_loop_filter_disable_flag</b>		
	Format:	U1	
7:6	<b>diff_cu_qp_delta_depth (or named as max_dqp_depth)</b>		
	Format:	U2	
	<b>Programming Notes</b>		
	cu_qp_delta_enabled_flag = 1 and Max_DQP_Level = 0 is supported.		
	cu_qp_delta_enabled_flag/max_dqp_depth: 1/0: has cu qp delta. (cu depth <= max_dqp_depth) will have cu qp delta coded. Only allow QP change across LCU, no change across CU.		
Must be zero for encoder			
5	<b>cu_qp_delta_enabled_flag</b>		
	Format:	U1	
	<b>Value</b>	<b>Name</b> <b>Description</b>	
	0	Disable	Does not allow QP change at CU level, the same QP is used for the entire LCU. Max_DQP_Level = 0 (i.e. diff_cu_qp_delta_depath = 0).
	1	Enable	Allow QP change at CU level. MAX_DQP_level can be >0.
	<b>Programming Notes</b>		
cu_qp_delta_enabled_flag = 1 and Max_DQP_Level = 0 is supported.			
4	<b>pcm_enabled_flag</b>		
	Format:	U1	

<b>HCP_PIC_STATE</b>		
	3	<b>sample_adaptive_offset_enabled_flag</b> Format: U1 <hr/> <div style="text-align: center;"><b>Programming Notes</b></div> Restriction: HW does not support SAO filtering for LCU size 16x16 Should be set to 0 if slice_sao_luma_flag==0 and slice_sao_chroma_flag==0.
	2:0	<b>Reserved</b> Format: MBZ
5	31:30	<b>Reserved</b> Format: MBZ
	23:20	<b>pcm_sample_bit_depth_luma_minus1</b> Format: U4
	19:16	<b>pcm_sample_bit_depth_chroma_minus1</b> Format: U4
	15:13	<b>max_transform_hierarchy_depth_inter (or named as tu_max_depth_inter)</b> Format: U3 Maximum TU split depths for inter blocks. <div style="text-align: center;"><b>Programming Notes</b></div> For encoder, always set to 2 to allow max 2 levels of split. For more splitting, rely on CU split to match the content (Intel restriction).
	12:10	<b>max_transform_hierarchy_depth_intra (or named as tu_max_depth_intra)</b> Format: U3 Maximum TU split depth for intra blocks. <div style="text-align: center;"><b>Programming Notes</b></div> For encoder, always set to 2 to allow max 2 levels of split. For more splitting, rely on CU split to match the content (Intel restriction).
	9:5	<b>pic_cr_qp_offset</b> Format: U5
	4:0	<b>pic_cb_qp_offset</b> Format: U5
6..18	31:0	<b>Reserved</b> Project: CHV, BSW Format: MBZ

## HCP\_PIPE\_BUF\_ADDR\_STATE

<b>HCP_PIPE_BUF_ADDR_STATE</b>				
Project:	CHV, BSW			
Source:	VideoCS			
Length Bias:	2			
<p>The HCP is selected with the <b>Media Instruction Opcode "7h"</b> for all HCP Commands. Each HCP command has assigned a media instruction command as defined in DWord 0, BitField 22:16.</p> <p>This state command provides the memory base addresses for the row store buffer and reconstructed picture output buffers required by the HCP.</p> <p>This is a picture level state command and is shared by both encoding and decoding processes.</p>				
<b>Programming Notes</b>				
<p>All pixel surface addresses must be 4K byte aligned. There is a max of 8 Reference Picture Buffer Addresses, and all share the same third address DW in specifying 48-bit address.</p>				
DWord	Bit	Description		
0	31:29	<b>Command Type</b>		
		Default Value:	3h PARALLEL_VIDEO_PIPE	
		Format:	OpCode	
	28:27	28:27	<b>Pipeline Type</b>	
			Default Value:	2h
			Format:	OpCode
	26:23	26:23	<b>Media Instruction Opcode</b>	
			Default Value:	7h Codec/Engine Name
			Format:	OpCode
			Codec/Engine Name = HCP = 7h	
	22:16	22:16	<b>Media Instruction Command</b>	
			Default Value:	2h HCP_PIPE_BUF_ADDR_STATE
Format:			OpCode	
15:12	15:12	<b>Reserved</b>		
		Format:	MBZ	
11:0	11:0	<b>Dword Length</b>		
		Format:	=n	
		(Excludes Dwords 0, 1).		
		<b>Value</b>	<b>Name</b>	
		5Ch		

<b>HCP_PIPE_BUF_ADDR_STATE</b>						
1..2	63:0	<p><b>Decoded Picture</b></p> <table border="1"> <tr> <td>Format:</td> <td>SplitBaseAddress4ByteAligned</td> </tr> </table> <p>Frame buffer address for the final decoded picture YUV output.</p>	Format:	SplitBaseAddress4ByteAligned		
Format:	SplitBaseAddress4ByteAligned					
3	31:0	<p><b>Decoded Picture Memory Address Attributes</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MemoryAddressAttributes [CHV, BSW]</td> </tr> </table>	Project:	CHV, BSW	Format:	MemoryAddressAttributes [CHV, BSW]
Project:	CHV, BSW					
Format:	MemoryAddressAttributes [CHV, BSW]					
4..5	63:0	<p><b>Deblocking Filter Line Buffer</b></p> <table border="1"> <tr> <td>Format:</td> <td>SplitBaseAddress64ByteAligned</td> </tr> </table> <p>Base address of the filter line buffer (read/write) used by the Deblocking Filter.</p>	Format:	SplitBaseAddress64ByteAligned		
Format:	SplitBaseAddress64ByteAligned					
6	31:0	<p><b>Deblocking Filter Line Buffer Memory Address Attributes</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MemoryAddressAttributes [CHV, BSW]</td> </tr> </table>	Project:	CHV, BSW	Format:	MemoryAddressAttributes [CHV, BSW]
Project:	CHV, BSW					
Format:	MemoryAddressAttributes [CHV, BSW]					
7..8	63:0	<p><b>Deblocking Filter Tile Line Buffer</b></p> <table border="1"> <tr> <td>Format:</td> <td>SplitBaseAddress64ByteAligned</td> </tr> </table> <p>Base address of the tile line buffer (read/write) used by the Deblocking Filter.</p>	Format:	SplitBaseAddress64ByteAligned		
Format:	SplitBaseAddress64ByteAligned					
9	31:0	<p><b>Deblocking Filter Tile Line Buffer Memory Address Attributes</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MemoryAddressAttributes [CHV, BSW]</td> </tr> </table>	Project:	CHV, BSW	Format:	MemoryAddressAttributes [CHV, BSW]
Project:	CHV, BSW					
Format:	MemoryAddressAttributes [CHV, BSW]					
10..11	63:0	<p><b>Deblocking Filter Tile Column Buffer</b></p> <table border="1"> <tr> <td>Format:</td> <td>SplitBaseAddress64ByteAligned</td> </tr> </table> <p>Base address of the tile column buffer (read/write) used by the Deblocking Filter.</p>	Format:	SplitBaseAddress64ByteAligned		
Format:	SplitBaseAddress64ByteAligned					
12	31:0	<p><b>Deblocking Filter Tile Column Buffer Memory Address Attributes</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MemoryAddressAttributes [CHV, BSW]</td> </tr> </table>	Project:	CHV, BSW	Format:	MemoryAddressAttributes [CHV, BSW]
Project:	CHV, BSW					
Format:	MemoryAddressAttributes [CHV, BSW]					
13..14	63:0	<p><b>Metadata Line Buffer</b></p> <table border="1"> <tr> <td>Format:</td> <td>SplitBaseAddress64ByteAligned</td> </tr> </table> <p>Base address for the Metadata Line buffer.</p>	Format:	SplitBaseAddress64ByteAligned		
Format:	SplitBaseAddress64ByteAligned					
15	31:0	<p><b>Metadata Line Buffer Memory Address Attributes</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MemoryAddressAttributes [CHV, BSW]</td> </tr> </table>	Project:	CHV, BSW	Format:	MemoryAddressAttributes [CHV, BSW]
Project:	CHV, BSW					
Format:	MemoryAddressAttributes [CHV, BSW]					
16..17	63:0	<p><b>Metadata Tile Line Buffer</b></p> <table border="1"> <tr> <td>Format:</td> <td>SplitBaseAddress64ByteAligned</td> </tr> </table> <p>Base address for the Metadata Tile Line buffer.</p>	Format:	SplitBaseAddress64ByteAligned		
Format:	SplitBaseAddress64ByteAligned					

<b>HCP_PIPE_BUF_ADDR_STATE</b>		
18	31:0	<b>Metadata Tile Line Buffer Memory Address Attributes</b>
		Project: CHV, BSW
		Format: MemoryAddressAttributes [CHV, BSW]
19..20	63:0	<b>Metadata Tile Column Buffer</b>
		Format: SplitBaseAddress64ByteAligned
		Base address for the Metadata Tile Column buffer.
21	31:0	<b>Metadata Tile Column Buffer Memory Address Attributes</b>
		Project: CHV, BSW
		Format: MemoryAddressAttributes [CHV, BSW]
22..23	63:0	<b>SAO Line Buffer</b>
		Format: SplitBaseAddress64ByteAligned
		Base address for the SAO Line buffer.
24	31:0	<b>SAO Line Buffer Memory Address Attributes</b>
		Project: CHV, BSW
		Format: MemoryAddressAttributes [CHV, BSW]
25..26	63:0	<b>SAO Tile Line Buffer</b>
		Format: SplitBaseAddress64ByteAligned
		Base address for the SAO Tile Line buffer.
27	31:0	<b>SAO Tile Line Buffer Memory Address Attributes</b>
		Project: CHV, BSW
		Format: MemoryAddressAttributes [CHV, BSW]
28..29	63:0	<b>SAO Tile Column Buffer</b>
		Format: SplitBaseAddress64ByteAligned
		Base address for the SAO Tile Column buffer.
30	31:0	<b>SAO Tile Column Buffer Memory Address Attributes</b>
		Project: CHV, BSW
		Format: MemoryAddressAttributes [CHV, BSW]
31..32	63:0	<b>Current Motion Vector Temporal Buffer</b>
		Format: SplitBaseAddress64ByteAligned
		Base address for the Current Motion Vector Temporal buffer.
33	31:0	<b>Current Motion Vector Temporal Buffer Memory Address Attributes</b>
		Project: CHV, BSW
		Format: MemoryAddressAttributes [CHV, BSW]

<b>HCP_PIPE_BUF_ADDR_STATE</b>								
34..35	63:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ				
Format:	MBZ							
36	31:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ		
Project:	CHV, BSW							
Format:	MBZ							
37..52	63:0	<p><b>Reference Picture Base Address (RefAddr[0-7])</b></p> <table border="1"> <tr> <td>Format:</td> <td>SplitBaseAddress64ByteAligned[8]</td> </tr> </table> <p>Base address of the reference picture buffer.</p> <table border="1"> <tr> <td colspan="2" style="text-align: center;"><b>Programming Notes</b></td> </tr> <tr> <td colspan="2">Must be 4k byte aligned.</td> </tr> </table>	Format:	SplitBaseAddress64ByteAligned[8]	<b>Programming Notes</b>		Must be 4k byte aligned.	
Format:	SplitBaseAddress64ByteAligned[8]							
<b>Programming Notes</b>								
Must be 4k byte aligned.								
53	31:0	<p><b>Reference Picture Base Address Memory Address Attributes</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MemoryAddressAttributes [CHV, BSW]</td> </tr> </table>	Project:	CHV, BSW	Format:	MemoryAddressAttributes [CHV, BSW]		
Project:	CHV, BSW							
Format:	MemoryAddressAttributes [CHV, BSW]							
54..59	31:0	<b>Reserved</b>						
60..61	63:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table>	Project:	CHV, BSW				
Project:	CHV, BSW							
62	31:0	<b>Reserved</b>						
63..65 <b>Project:</b> CHV, BSW	31:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ		
Project:	CHV, BSW							
Format:	MBZ							
66..81	63:0	<p><b>Collocated Motion Vector Temporal Buffer[0-7]</b></p> <table border="1"> <tr> <td>Format:</td> <td>SplitBaseAddress64ByteAligned[8]</td> </tr> </table> <p>Base address for the Collocated Motion Vector Temporal buffer.</p> <p>Specifies the 64 byte aligned buffer address for Collocated Motion Vector Temporal Buffer. For VP9, only index 0 is required to have a valid address.</p>	Format:	SplitBaseAddress64ByteAligned[8]				
Format:	SplitBaseAddress64ByteAligned[8]							
82	31:0	<p><b>Collocated Motion Vector Temporal Buffer[0-7] Memory Address Attributes</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MemoryAddressAttributes [CHV, BSW]</td> </tr> </table>	Project:	CHV, BSW	Format:	MemoryAddressAttributes [CHV, BSW]		
Project:	CHV, BSW							
Format:	MemoryAddressAttributes [CHV, BSW]							
83..84	63:0	<p><b>VP9 Probability Buffer Read/Write</b></p> <table border="1"> <tr> <td>Format:</td> <td>SplitBaseAddress64ByteAligned</td> </tr> </table> <p>Specifies the 64 byte aligned buffer address for VP9 Probability Buffer. Hardware reads in the probability for decode and write out the modified probability for future frames. Driver needs to program the Initial VP9 Probability for decoding the current frame. For Key Frame, it should contain the default Key Frame Probability. For non-Key Frame, it could be a default (non-Key) or one of the 8 Reference Buffers Probability. Driver must provide a valid Initial VP9 Probability buffer.</p>	Format:	SplitBaseAddress64ByteAligned				
Format:	SplitBaseAddress64ByteAligned							

<b>HCP_PIPE_BUF_ADDR_STATE</b>		
85	31:0	<b>VP9 Probability Buffer Read/Write Memory Address Attributes</b> Format: MemoryAddressAttributes [CHV, BSW]
86..87	63:0	<b>VP9 Segment ID Buffer Read/Write</b> Format: SplitBaseAddress64ByteAligned Specifies the 64 byte aligned buffer address for VP9 SegmentID buffer. This should contain the writeout SegmentID from previous frame and will be used to predict SegmentID for the current frame. Hardware will write out SegmentID of the current frame in the same address for the next frame.
88	31:0	<b>VP9 Segment ID buffer Read/Write Memory Address Attributes</b> Format: MemoryAddressAttributes [CHV, BSW]
89..90	63:0	<b>VP9 HVD Line Rowstore Buffer Read/Write</b> Format: SplitBaseAddress64ByteAligned Specifies the 64 byte aligned buffer address for HVD Line Rowstore Buffer (bitstream decoder).
91	31:0	<b>VP9 HVD Line Rowstore buffer Read/Write Memory Address Attributes</b> Format: MemoryAddressAttributes [CHV, BSW]
92..93	63:0	<b>VP9 HVD Tile Rowstore Buffer Read/Write</b> Format: SplitBaseAddress64ByteAligned Specifies the 64 byte aligned buffer address for HVD Tile Rowstore Buffer (bitstream decoder).
94	31:0	<b>VP9 HVD Tile Rowstore buffer Read/Write Memory Address Attributes</b> Format: MemoryAddressAttributes [CHV, BSW]
95..96	63:48	<b>MBZ: Reserved</b>
97	31:0	<b>SAO Streamout Data Destination buffer Read/Write Memory Address Attributes</b> Format: MemoryAddressAttributes [CHV, BSW]



## HCP\_PIPE\_MODE\_SELECT

HCP_PIPE_MODE_SELECT			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>The HCP is selected with the <b>Media Instruction Opcode "7h"</b> for all HCP Commands. Each HCP command has assigned a media instruction command as defined in DWord 0, BitField 22:16.</p> <p>The workload for the HCP is based upon a single frame decode. There are no states saved between frame decodes in the HCP. Once the bit stream DMA is configured with the HCP_BSD_OBJECT command, and the bit stream is presented to the HCP, the frame decode will begin.</p> <p>The HCP_PIPE_MODE_SELECT command is responsible for general pipeline level configuration that would normally be set once for a single stream encode or decode and would not be modified on a frame workload basis.</p> <p>This is a picture level state command and is shared by both encoding and decoding processes.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline Type</b>	
		Default Value:	2h
		Format:	OpCode
	26:23	<b>Media Instruction Opcode</b>	
		Default Value:	7h Codec/Engine Name
		Format:	OpCode
		Codec/Engine Name = HCP = 7h	
22:16	<b>Media Instruction Command</b>		
	Default Value:	0h HCP_PIPE_MODE_SELECT	
	Format:	OpCode	
15:12	<b>Reserved</b>		
	Format:	MBZ	
11:0	<b>DWord Length</b>		
	Format:	=n	
	(Excludes Dwords 0, 1).		
	<b>Value</b>	<b>Name</b>	<b>Project</b>
	2h	Value_2	CHV, BSW
1	31:24	<b>Reserved</b>	

<b>HCP_PIPE_MODE_SELECT</b>										
2	23:17	<b>Reserved</b>								
	Format: _____ MBZ									
	16:13	<b>Reserved</b>								
	Project: _____ CHV, BSW									
	Format: _____ MBZ									
	12	<b>Reserved</b>								
	Project: _____ CHV, BSW									
	11	<b>Reserved</b>								
	Project: _____ CHV, BSW									
	Format: _____ MBZ									
	10	<b>Reserved</b>								
	Project: _____ CHV, BSW									
	9	<b>Reserved</b>								
	Project: _____ CHV, BSW									
	8	<b>Reserved</b>								
Project: _____ CHV, BSW										
7:5	<b>Codec Standard Select</b>									
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>HEVC</td> </tr> <tr> <td style="text-align: center;">1</td> <td>VP9</td> </tr> </tbody> </table>		Value	Name	0	HEVC	1	VP9			
Value	Name									
0	HEVC									
1	VP9									
4	<b>Reserved</b>									
3	<b>Pic Status/Error Report Enable</b>									
Format: _____ Enable										
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 10%;">Name</th> <th style="width: 80%;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Disable</td> <td>Disable status/error reporting</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Enable</td> <td>Status/Error reporting is written out once per picture. The Pic Status/Error Report ID in DWord3 along with the status/error status bits are packed into one cache line and written to the Status/Error Buffer address in the HCP_PIPE_BUF_ADDR_STATE command. Must be zero for encoder mode.</td> </tr> </tbody> </table>		Value	Name	Description	0	Disable	Disable status/error reporting	1	Enable	Status/Error reporting is written out once per picture. The Pic Status/Error Report ID in DWord3 along with the status/error status bits are packed into one cache line and written to the Status/Error Buffer address in the HCP_PIPE_BUF_ADDR_STATE command. Must be zero for encoder mode.
Value	Name	Description								
0	Disable	Disable status/error reporting								
1	Enable	Status/Error reporting is written out once per picture. The Pic Status/Error Report ID in DWord3 along with the status/error status bits are packed into one cache line and written to the Status/Error Buffer address in the HCP_PIPE_BUF_ADDR_STATE command. Must be zero for encoder mode.								
2	<b>Reserved</b>									
Project: _____ CHV, BSW										
1:0	<b>Reserved</b>									
Project: _____ CHV, BSW										
Format: _____ MBZ										
2	31:0	<b>Media Soft-Reset Counter (per 1000 clocks)</b>								
Format: _____ U32										

<b>HCP_PIPE_MODE_SELECT</b>													
		<p>In decoder modes, this counter value specifies the number of clocks (per 1000) of GAC inactivity before a media soft-reset is applied to the HCP. If counter value is set to 0, the media soft-reset feature is disabled and no reset will occur.</p> <p>In encoder modes, this counter must be set to 0 to disable media soft reset. This feature is not supported for the encoder.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Project</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Disable</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Value	Name	Project	0	Disable	CHV, BSW					
Value	Name	Project											
0	Disable	CHV, BSW											
3	31:0	<p><b>Pic Status/Error Report ID</b></p> <table border="1"> <tr> <td>Format:</td> <td style="text-align: center;">U32</td> </tr> </table> <p>The Pic Status/Error Report ID is a unique 32-bit unsigned integer assigned to each picture status/error output. Must be zero for encoder mode.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>32-bit unsigned</td> <td>Unique ID Number</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Reserved</td> <td></td> </tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>Software must program different Status/Error Buffer addresses between pictures; otherwise the hardware might overwrite previously written data.</p>	Format:	U32	Value	Name	Description	0	32-bit unsigned	Unique ID Number	1	Reserved	
Format:	U32												
Value	Name	Description											
0	32-bit unsigned	Unique ID Number											
1	Reserved												

## HCP\_QM\_STATE

<b>HCP_QM_STATE</b>									
Project:	CHV, BSW								
Source:	VideoCS								
Length Bias:	2								
<p>The HCP is selected with the <b>Media Instruction Opcode "7h"</b> for all HCP Commands. Each HCP command has assigned a media instruction command as defined in DWord 0, BitField 22:16.</p> <p>The HCP_QM_STATE command loads the custom HEVC quantization tables into local RAM and may be issued up to 20 times: 3x Colour Component plus 2x intra/inter plus 4x SizeID minus 4 for the 32x32 chroma components.</p> <p>When the scaling_list_enable_flag is set to disable, the scaling matrix is still sent to the decoder, and with all entries programmed to the same value = 16.</p> <p>This is a picture level state command and is issued in both encoding and decoding processes.</p>									
<p>DWords 2-17 form a table for the DCT coefficients, 4 8-bit coefficients/DWord.</p> <ul style="list-style-type: none"> <li>• Size 4x4 for SizeID0, DWords 2-5.</li> <li>• Size 8x8 for SizeID1/2/3, DWords 2-17.</li> </ul>									
SizeID 0 (Table 4-10)									
	<b>4x4</b>	<b>[31:24]</b>	<b>[23:16]</b>	<b>[15:8]</b>	<b>[7:0]</b>				
DWord 2	AC(0,3)	AC(0,2)	AC(0,1)	DC					
DWord 3	AC(1,3)	AC(1,2)	AC(1,1)	AC(1,0)					
DWord 4	AC(2,3)	AC(2,2)	AC(2,1)	AC(2,0)					
DWord 5	AC(3,3)	AC(3,2)	AC(3,1)	AC(3,0)					
SizeID 1, 2, 3 (Table 4-11)									
	<b>8x8</b>	<b>[31:24]</b>	<b>[23:16]</b>	<b>[15:8]</b>	<b>[7:0]</b>	<b>[31:24]</b>	<b>[23:16]</b>	<b>[15:8]</b>	<b>[7:0]</b>
DWord 3,2	AC(0,7)	AC(0,6)	AC(0,5)	AC(0,4)	AC(0,3)	AC(0,2)	AC(0,1)	DC	
DWord 5,4	AC(1,7)	AC(1,6)	AC(1,5)	AC(1,4)	AC(1,3)	AC(1,2)	AC(1,1)	AC(1,0)	
DWord 7,6	AC(2,7)	AC(2,6)	AC(2,5)	AC(2,4)	AC(2,3)	AC(2,2)	AC(2,1)	AC(2,0)	
DWord 9,8	AC(3,7)	AC(3,6)	AC(3,5)	AC(3,4)	AC(3,3)	AC(3,2)	AC(3,1)	AC(3,0)	
DWord 11,10	AC(4,7)	AC(4,6)	AC(4,5)	AC(4,4)	AC(4,3)	AC(4,2)	AC(4,1)	AC(4,0)	
DWord 13,12	AC(5,7)	AC(5,6)	AC(5,5)	AC(5,4)	AC(5,3)	AC(5,2)	AC(5,1)	AC(5,0)	
DWord 15,14	AC(6,7)	AC(6,6)	AC(6,5)	AC(6,4)	AC(6,3)	AC(6,2)	AC(6,1)	AC(6,0)	
DWord 17,16	AC(7,7)	AC(7,6)	AC(7,5)	AC(7,4)	AC(7,3)	AC(7,2)	AC(7,1)	AC(7,0)	
DWord	Bit	Description							
0	31:29	<b>Command Type</b>							
		Default Value:				3h PARALLEL_VIDEO_PIPE			
		Format:				OpCode			

<b>HCP_QM_STATE</b>													
	28:27	<b>Pipeline Type</b> <table border="1"> <tr> <td>Default Value:</td> <td>2h</td> </tr> <tr> <td>Format:</td> <td>OpCode</td> </tr> </table>	Default Value:	2h	Format:	OpCode							
	Default Value:	2h											
	Format:	OpCode											
	26:23	<b>Media Instruction Opcode</b> <table border="1"> <tr> <td>Default Value:</td> <td>7h Codec/Engine Name</td> </tr> <tr> <td>Format:</td> <td>OpCode</td> </tr> </table> Codec/Engine Name = HCP = 7h	Default Value:	7h Codec/Engine Name	Format:	OpCode							
	Default Value:	7h Codec/Engine Name											
Format:	OpCode												
22:16	<b>Media Instruction Command</b> <table border="1"> <tr> <td>Default Value:</td> <td>4h HCP_QM_STATE</td> </tr> <tr> <td>Format:</td> <td>OpCode</td> </tr> </table>	Default Value:	4h HCP_QM_STATE	Format:	OpCode								
Default Value:	4h HCP_QM_STATE												
Format:	OpCode												
15:12	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ										
Format:	MBZ												
11:0	<b>Dword Length</b> <table border="1"> <tr> <td>Format:</td> <td>=n</td> </tr> </table> (Excludes Dwords 0, 1). <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>10h</td> <td></td> </tr> </tbody> </table>	Format:	=n	Value	Name	10h							
Format:	=n												
Value	Name												
10h													
1	31	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ									
	Format:	MBZ											
	30:13	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ									
	Format:	MBZ											
12:5	<b>DC Coefficient</b> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> Specifies the 8-bit DC coefficient for SizeID 2 and 3. <table border="1"> <thead> <tr> <th colspan="2" style="text-align: center;">Programming Notes</th> </tr> </thead> <tbody> <tr> <td colspan="2">The DC Coefficient must be set to zero for SizeID 0 and 1.</td> </tr> <tr> <td colspan="2">The DC Coefficient must be set to scaling_list_dc_coef_minus8 + 8 for SizeID 2 and 3.</td> </tr> </tbody> </table>	Format:	U8	Programming Notes		The DC Coefficient must be set to zero for SizeID 0 and 1.		The DC Coefficient must be set to scaling_list_dc_coef_minus8 + 8 for SizeID 2 and 3.					
Format:	U8												
Programming Notes													
The DC Coefficient must be set to zero for SizeID 0 and 1.													
The DC Coefficient must be set to scaling_list_dc_coef_minus8 + 8 for SizeID 2 and 3.													
4:3	<b>Color Component</b> <table border="1"> <tr> <td>Format:</td> <td>U2</td> </tr> </table> Encoder: When RDOQ is enabled, scaling list for all 3 color components must be same. So this field is set to always 0. <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Luma</td> </tr> <tr> <td>1</td> <td>Chroma Cb</td> </tr> <tr> <td>2</td> <td>Chroma Cr</td> </tr> <tr> <td>3</td> <td>Reserved</td> </tr> </tbody> </table>	Format:	U2	Value	Name	0	Luma	1	Chroma Cb	2	Chroma Cr	3	Reserved
Format:	U2												
Value	Name												
0	Luma												
1	Chroma Cb												
2	Chroma Cr												
3	Reserved												

<b>HCP_QM_STATE</b>																	
	2:1	<b>SizeID</b>															
		Format: <span style="float: right;">U2</span>															
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 15%;">Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>4x4</td> <td></td> </tr> <tr> <td>1</td> <td>8x8</td> <td></td> </tr> <tr> <td>2</td> <td>16x16</td> <td></td> </tr> <tr> <td>3</td> <td>32x32</td> <td>(Illegal Value for Colour Component Chroma Cr and Cb.)</td> </tr> </tbody> </table>	Value	Name	Description	0	4x4		1	8x8		2	16x16		3	32x32	(Illegal Value for Colour Component Chroma Cr and Cb.)
		Value	Name	Description													
		0	4x4														
	1	8x8															
	2	16x16															
	3	32x32	(Illegal Value for Colour Component Chroma Cr and Cb.)														
	0	<b>Prediction Type</b>															
	Format: <span style="float: right;">U1</span>																
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Intra</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Inter</td> </tr> </tbody> </table>	Value	Name	0	Intra	1	Inter											
Value	Name																
0	Intra																
1	Inter																
2..17	511:0	<b>See Tables 4-10 and 4-11</b>															

## HCP\_REF\_IDX\_STATE

HCP_REF_IDX_STATE			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>The HCP is selected with the <b>Media Instruction Opcode "7h"</b> for all HCP Commands. Each HCP command has assigned a media instruction command as defined in DWord 0, BitField 22:16.</p> <p>This is a slice level command used in both encoding and decoding processes. For decoder, it is issued with the HCP_BSD_OBJECT command.</p> <p>Unlike AVC, HEVC allows 16 reference idx entries in each of the L0 and L1 list for a progressive picture. Hence, a max total 32 reference idx in both lists together. The same when the picture is a field picture. Regardless the number of reference idx entries, there are only max 8 reference pictures exist at any one time. Multiple reference idx can point to the same reference picture and can optionally pic a top or bottom field, or frame.</p> <p>For P-Slice, this command is issued only once, representing L0 list. For B-Slice, this command can be issued up to two times, one for L0 list and one for L1 list.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline Type</b>	
		Default Value:	2h
		Format:	OpCode
	26:23	<b>Media Instruction Opcode</b>	
		Default Value:	7h Codec/Engine Name
		Format:	OpCode
		Codec/Engine Name = HCP = 7h	
	22:16	<b>Media Instruction Command</b>	
		Default Value:	12h HCP_REF_IDX_STATE
		Format:	OpCode
	15:12	<b>Reserved</b>	
Format:		MBZ	
11:0	<b>Dword Length</b>		
	Format:	=n	
	(Excludes Dwords 0, 1).		
	<b>Value</b>	<b>Name</b>	
	10h		

<b>HCP_REF_IDX_STATE</b>								
1	31:5	<b>Reserved</b>						
	4:1	<b>num_ref_idx_l[RefPicListNum]_active_minus1</b> Format: <span style="float: right;">U4</span> num_ref_idx_l[RefPicListNum]_active_minus1 <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">[0-14]</td> <td></td> </tr> </tbody> </table>	Value	Name	[0-14]			
	Value	Name						
	[0-14]							
0	<b>RefPicListNum</b> Format: <span style="float: right;">U1</span> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 25%; text-align: center;">Value</th> <th style="width: 75%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Reference Picture List 0</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Reference Picture List 1</td> </tr> </tbody> </table>	Value	Name	0	Reference Picture List 0	1	Reference Picture List 1	
Value	Name							
0	Reference Picture List 0							
1	Reference Picture List 1							
2..17	31:16	<b>Reserved</b> Format: <span style="float: right;">MBZ</span>						
	15	<b>list_entry_IX[i]: bottom_field_flag</b> Format: <span style="float: right;">U1</span> Where X is the RefPicListNum and i is the list entry number 0 through 15. DW2 corresponds to i=0, DW17 corresponds to i=15. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 40%; text-align: center;">Value</th> <th style="width: 60%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Bottom Field</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Top Field</td> </tr> </tbody> </table> <div style="border: 1px solid black; padding: 5px; margin-top: 5px; text-align: center;"> <b>Programming Notes</b>            Not supported in encoder mode.         </div>	Value	Name	0	Bottom Field	1	Top Field
	Value	Name						
	0	Bottom Field						
	1	Top Field						
14	<b>list_entry_IX[i]: field_pic_flag</b> Format: <span style="float: right;">U1</span> Where X is the RefPicListNum and i is the list entry number 0 through 15. DW2 corresponds to i=0, DW17 corresponds to i=15. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 40%; text-align: center;">Value</th> <th style="width: 60%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Video Frame</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Video Field</td> </tr> </tbody> </table> <div style="border: 1px solid black; padding: 5px; margin-top: 5px; text-align: center;"> <b>Programming Notes</b>            Not supported in encoder mode.         </div>	Value	Name	0	Video Frame	1	Video Field	
Value	Name							
0	Video Frame							
1	Video Field							
13	<b>list_entry_IX[i]: LongTermReference</b> Format: <span style="float: right;">U1</span> Where X is the RefPicListNum and i is the list entry number 0 through 15. DW2 corresponds to i=0, DW17 corresponds to i=15.							



<b>HCP_REF_IDX_STATE</b>									
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Short term reference</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Long term reference</td> </tr> </tbody> </table>	Value	Name	0	Short term reference	1	Long term reference		
Value	Name								
0	Short term reference								
1	Long term reference								
12	<p><b>luma_weight_IX_flag[i]</b></p> <table border="1"> <tr> <td>Format:</td> <td style="text-align: center;">U1</td> </tr> </table> <p>Where X is the RefPicListNum and i is the list entry number 0 through 15. DW2 corresponds to i=0, DW17 corresponds to i=15.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Default weighted prediction for luma</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Explicit weighted prediction for Luma</td> </tr> </tbody> </table>	Format:	U1	Value	Name	0	Default weighted prediction for luma	1	Explicit weighted prediction for Luma
Format:	U1								
Value	Name								
0	Default weighted prediction for luma								
1	Explicit weighted prediction for Luma								
11	<p><b>chroma_weight_IX_flag[i]</b></p> <table border="1"> <tr> <td>Format:</td> <td style="text-align: center;">U1</td> </tr> </table> <p>Where X is the RefPicListNum and i is the list entry number 0 through 15. DW2 corresponds to i=0, DW17 corresponds to i=15.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Default weighted prediction for Chroma</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Explicit weighted prediction for Chroma</td> </tr> </tbody> </table>	Format:	U1	Value	Name	0	Default weighted prediction for Chroma	1	Explicit weighted prediction for Chroma
Format:	U1								
Value	Name								
0	Default weighted prediction for Chroma								
1	Explicit weighted prediction for Chroma								
10:8	<p><b>list_entry_IX[i]: Reference Picture Frame ID (RefAddr[0-7])</b></p> <table border="1"> <tr> <td>Format:</td> <td style="text-align: center;">U3</td> </tr> </table> <p>Where X is the RefPicListNum and i is the list entry number 0 through 15. DW2 corresponds to i=0, DW17 corresponds to i=15.</p> <p>The reference picture frame ID identifies the reference picture associated with the base address defined in <b>Reference Picture Address (RefAddr[0-7])</b> in the HCP_PIPE_BUF_ADDR_STATE command.</p>	Format:	U3						
Format:	U3								
7:0	<p><b>list_entry_IX[i]: Reference Picture tb Value</b></p> <table border="1"> <tr> <td>Format:</td> <td style="text-align: center;">U8</td> </tr> </table> <p>Where X is the RefPicListNum and i is the list entry number 0 through 15. DW2 corresponds to i=0, DW17 corresponds to i=15.</p> <p>clip(-128,127, CurrentPOC - RefPOC), where RefPOC is the POC value of the reference picture. 8-bit signed.</p> <p>See the "Derivation process for temporal luma motion vector prediction" in the HEVC standard.</p>	Format:	U8						
Format:	U8								

## HCP\_SLICE\_STATE

HCP_SLICE_STATE			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>The HCP is selected with the <b>Media Instruction Opcode "7h"</b> for all HCP Commands. Each HCP command has assigned a media instruction command as defined in DWord 0, BitField 22:16.</p> <p>This is a slice level command used in both encoding and decoding processes. For decoder, it is issued with the HCP_BSD_OBJECT command.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline Type</b>	
		Default Value:	2h
		Format:	OpCode
	26:23	<b>Media Instruction Opcode</b>	
		Default Value:	7h Codec/Engine Name
		Format:	OpCode
		Codec/Engine Name = HCP = 7h	
22:16	<b>Media Instruction Command</b>		
	Default Value:	14h HCP_SLICE_STATE	
	Format:	OpCode	
15:12	<b>Reserved</b>		
	Format:	MBZ	
11:0	<b>Dword Length</b>		
	Format:	=n	
	(Excludes Dwords 0, 1).		
	<b>Value</b>	<b>Name</b>	<b>Project</b>
4h		CHV, BSW	
1	31:25	<b>Reserved</b>	
		Format:	MBZ
	24:16	<b>SliceStartCtbY or (slice_start_lcu_y encoder)</b>	
Format:	U9		
Specifies the starting row address of the first coding tree block in the current slice.			

<b>HCP_SLICE_STATE</b>		
	15:9	<b>Reserved</b> Format: MBZ
	8:0	<b>SliceStartCtbX or (slice_start_lcu_x encoder)</b> Format: U9 Specifies the starting column address of the first coding tree block in the current slice.
2	31:25	<b>Reserved</b> Format: MBZ
	24:16	<b>NextSliceStartCtbY or (next_slice_start_lcu_y encoder)</b> Format: U9 Specifies the starting row address of the first coding tree block in the next slice. Must be set to zero when the current slice is the last slice of a picture. For the single slice per frame case, the only slice is also the last slice, so this parameter should be set to a number larger than the frame height (at least +1).
	15	<b>Reserved</b> Project: CHV, BSW
	14:9	<b>Reserved</b> Format: MBZ
	8:0	<b>NextSliceStartCtbX or (next_slice_start_lcu_x encoder)</b> Format: U9 Specifies the starting column address of the first coding tree block in the next slice. Must be set to zero when the current slice is the last slice of a picture. For the single slice per frame case, the only slice is also the last slice, so this parameter should be set to a number larger than the frame width (at least +1).
3	31:24	<b>Reserved</b> Format: MBZ
	23	<b>Reserved</b> Project: Format: MBZ
	22	<b>Reserved</b> Project: CHV, BSW
	21:17	<b>slice_cr_qp_offset</b> Format: S4  For deblocking purpose, the pic and slice level cr qp offset must be provided separately. PAK needs to perform $final\_chroma\_cr\_qp\_offset = pic\_cr\_qp\_offset + slice\_cr\_qp\_offset$ .

<b>HCP_SLICE_STATE</b>																																																					
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr><td>14h</td><td>-12</td></tr> <tr><td>15h</td><td>-11</td></tr> <tr><td>16h</td><td>-10</td></tr> <tr><td>17h</td><td>-9</td></tr> <tr><td>18h</td><td>-8</td></tr> <tr><td>19h</td><td>-7</td></tr> <tr><td>1Ah</td><td>-6</td></tr> <tr><td>1Bh</td><td>-5</td></tr> <tr><td>1Ch</td><td>-4</td></tr> <tr><td>1Dh</td><td>-3</td></tr> <tr><td>1Eh</td><td>-2</td></tr> <tr><td>1Fh</td><td>-1</td></tr> <tr><td>0h</td><td>0</td></tr> <tr><td>1h</td><td>1</td></tr> <tr><td>2h</td><td>2</td></tr> <tr><td>3h</td><td>3</td></tr> <tr><td>4h</td><td>4</td></tr> <tr><td>5h</td><td>5</td></tr> <tr><td>6h</td><td>6</td></tr> <tr><td>7h</td><td>7</td></tr> <tr><td>8h</td><td>8</td></tr> <tr><td>9h</td><td>9</td></tr> <tr><td>10h</td><td>10</td></tr> <tr><td>11h</td><td>11</td></tr> <tr><td>12h</td><td>12</td></tr> </tbody> </table>	Value	Name	14h	-12	15h	-11	16h	-10	17h	-9	18h	-8	19h	-7	1Ah	-6	1Bh	-5	1Ch	-4	1Dh	-3	1Eh	-2	1Fh	-1	0h	0	1h	1	2h	2	3h	3	4h	4	5h	5	6h	6	7h	7	8h	8	9h	9	10h	10	11h	11	12h	12
Value	Name																																																				
14h	-12																																																				
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16h	-10																																																				
17h	-9																																																				
18h	-8																																																				
19h	-7																																																				
1Ah	-6																																																				
1Bh	-5																																																				
1Ch	-4																																																				
1Dh	-3																																																				
1Eh	-2																																																				
1Fh	-1																																																				
0h	0																																																				
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10h	10																																																				
11h	11																																																				
12h	12																																																				
	<p style="text-align: center;"><b>Programming Notes</b></p> <p>The valid value is from -12 to 12 (or 14h to 0Ch).</p>																																																				
16:12	<p><b>slice_cb_qp_offset</b></p> <table border="1"> <tr> <td>Format:</td> <td>S4</td> </tr> </table> <p>For deblocking purpose, the pic and slice level cb qp offset must be provided separately. PAK needs to perform <math>\text{final\_chroma\_cb\_qp\_offset} = \text{pic\_cb\_qp\_offset} + \text{slice\_cb\_qp\_offset}</math>.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>14h</td> <td>-12</td> </tr> </tbody> </table>	Format:	S4	Value	Name	14h	-12																																														
Format:	S4																																																				
Value	Name																																																				
14h	-12																																																				

<b>HCP_SLICE_STATE</b>		
	15h	-11
	16h	-10
	17h	-9
	18h	-8
	19h	-7
	1Ah	-6
	1Bh	-5
	1Ch	-4
	1Dh	-3
	1Eh	-2
	1Fh	-1
	0h	0
	1h	1
	2h	2
	3h	3
	4h	4
	5h	5
	6h	6
	7h	7
	8h	8
	9h	9
	10h	10
	11h	11
	12h	12
<b>Programming Notes</b>		
The valid value is from -12 to 12 (or 14h to 0Ch).		
11:6	<b>SliceQp</b>	
	Format:	U6
	Specifies the initial absolute value of QPy quantization parameter for the slice as defined in the Slice Header Semantics section of the HEVC standard. This signifies only the magnitude of SliceQp. In 8 bit, SliceQp only goes from 0 to 51. But in 10 bit, it needs to go from -12 to 51. There is a sign bit specifies at bit [3] below.	
5	<b>slice_temporal_mvp_enable_flag</b>	
	Format:	U1

<b>HCP_SLICE_STATE</b>																
4	<p><b>dependent_slice_flag</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U1</td> </tr> </table> <p>Decoder only.</p>	Format:	U1													
	Format:	U1														
	<p><b>LastSliceofPic</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U1</td> </tr> </table> <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th style="width: 20%;">Value</th> <th style="width: 80%;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Not the last slice of the picture</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Last slice of the picture</td> </tr> </tbody> </table>	Format:	U1	Value	Name	0	Not the last slice of the picture	1	Last slice of the picture							
Format:	U1															
Value	Name															
0	Not the last slice of the picture															
1	Last slice of the picture															
<p><b>slice_type</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U2</td> </tr> </table> <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th style="width: 20%;">Value</th> <th style="width: 80%;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>B-slice</td> </tr> <tr> <td style="text-align: center;">1</td> <td>P-slice</td> </tr> <tr> <td style="text-align: center;">2</td> <td>I-slice</td> </tr> <tr> <td style="text-align: center;">3</td> <td>Illegal/Reserved</td> </tr> </tbody> </table>	Format:	U2	Value	Name	0	B-slice	1	P-slice	2	I-slice	3	Illegal/Reserved				
Format:	U2															
Value	Name															
0	B-slice															
1	P-slice															
2	I-slice															
3	Illegal/Reserved															
4	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">MBZ</td> </tr> </table>	Format:	MBZ													
	Format:	MBZ														
	<p><b>CollocatedRefIDX</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U3</td> </tr> </table> <p>Collocated Motion Vector Temporal Buffer Index.</p>	Format:	U3													
Format:	U3															
<p><b>MaxMergeIDX</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U3</td> </tr> </table> <p>MaxNumMergeCand = 5 - five_minus_max_num_merge_cand - 1.</p> <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">2</td> <td style="text-align: center;">2</td> </tr> <tr> <td style="text-align: center;">3</td> <td style="text-align: center;">3</td> </tr> <tr> <td style="text-align: center;">4</td> <td style="text-align: center;">4</td> </tr> </tbody> </table> <table border="1" style="width: 100%; margin-top: 10px;"> <thead> <tr> <th style="text-align: center; color: blue;">Programming Notes</th> </tr> </thead> <tbody> <tr> <td style="padding: 5px;">                     The valid value is from 0 to 4                      (MaxNumMergeCand = 5 - five_minus_max_num_merge_cand - 1)                 </td> </tr> </tbody> </table>	Format:	U3	Value	Name	0	0	1	1	2	2	3	3	4	4	Programming Notes	The valid value is from 0 to 4 (MaxNumMergeCand = 5 - five_minus_max_num_merge_cand - 1)
Format:	U3															
Value	Name															
0	0															
1	1															
2	2															
3	3															
4	4															
Programming Notes																
The valid value is from 0 to 4 (MaxNumMergeCand = 5 - five_minus_max_num_merge_cand - 1)																

<b>HCP_SLICE_STATE</b>			
22	<b>cabac_init_flag</b>		
	Format:	U1	
	21:19	<b>luma_log2_weight_denom</b>	
		Format:	U3
	18:16	<b>ChromaLog2WeightDenom</b>	
		Format:	U3
	15	<b>collocated_from_I0_flag</b>	
		Format:	U1
	14	<b>isLowDelay</b>	
		Format:	U1
	If the POCs of all pictures in both lists are less than the current POC, then set to one, else set to zero.		
	13	<b>mvd_l1_zero_flag</b>	
		Format:	U1
	Decoder only.		
12	<b>slice_sao_luma_flag</b>		
	Format:	U1	
	<b>Programming Notes</b>		
Note: For encoder, all Slices must have same setting within a picture			
11	<b>slice_sao_chroma_flag</b>		
	Format:	U1	
	<b>Programming Notes</b>		
Note: For encoder, all Slices must have same setting within a picture			
10	<b>slice_loop_filter_across_slices_enabled_flag</b>		
	Format:	U1	
	<b>Programming Notes</b>		
Note: For the encoder, this bit must be set to zero (hardware restriction).			
9	<b>Reserved</b>		
8:5	<b>slice_beta_offset_div2 or (final Beta_Offset_div2 Encoder)</b>		
	Format:	S3	
	Deblocking filter beta offset. Specified in 2's comp.		
	<b>Value</b>	<b>Name</b>	
[1101b,0011b]		[-3,3]	

<b>HCP_SLICE_STATE</b>				
	4:1	<b>slice_tc_offset_div2 or (final tc_offset_div2 Encoder)</b>		
		Format: <span style="float: right;">S3</span>		
		Deblocking filter tc offset. Specified in 2's comp.		
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 70%; text-align: center;">Value</th> <th style="width: 30%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>[1101b,0011b]</td> <td>[-3,3]</td> </tr> </tbody> </table>	Value	Name
Value	Name			
[1101b,0011b]	[-3,3]			
0	<b>slice_header_disable_deblocking_filter_flag</b>			
	Format: <span style="float: right;">U1</span>			
5	31:16	<b>Reserved</b>		
		Format: <span style="float: right;">MBZ</span>		
	15:0	<b>SliceHeaderLength</b>		
		Format: <span style="float: right;">U16</span>		
		Decoder only.		
		Specifies the length in bytes of the slice header including the start code. The starting byte of the slice header in the bit stream buffer is indicated by the Indirect Data Start Address in the HCP_BSD_OBJECT command. The ending byte of the slice header in the same bit stream buffer is indicated by the last byte prior to the slice data (CABAC).		
6..8	31:0	<b>Reserved</b>		
		Project: <span style="float: right;">CHV, BSW</span>		
		Format: <span style="float: right;">MBZ</span>		



## HCP\_SURFACE\_STATE

<b>HCP_SURFACE_STATE</b>				
Project:	CHV, BSW			
Source:	VideoCS			
Length Bias:	2			
<p>The HCP is selected with the <b>Media Instruction Opcode "7h"</b> for all HCP Commands. Each HCP command has assigned a media instruction command as defined in DWord 0, BitField 22:16.</p> <p>The HCP_SURFACE_STATE command is responsible for defining the frame buffer pitch and the offset of the chroma component.</p> <p>This is a picture level state command and is shared by both encoding and decoding processes.</p> <p>Note : Only NV12 and Tile Y are being supported for HEVC. Hence full pitch and interleaved UV is always in use. U and V Xoffset must be set to 0; U and V Yoffset must be 16-pixel aligned. This Surface State is not the same as that of the 3D engine and of the MFX pipeline.</p>				
DWord	Bit	Description		
0	31:29	<b>Command Type</b>		
		Default Value:	3h PARALLEL_VIDEO_PIPE	
		Format:	OpCode	
	28:27		<b>Pipeline Type</b>	
			Default Value:	2h
			Format:	OpCode
	26:23		<b>Media Instruction Opcode</b>	
Default Value:			7h Codec/Engine Name	
Format:			OpCode	
Codec/Engine Name = HCP = 7h				
22:16		<b>Media Instruction Command</b>		
		Default Value:	1h HCP_SURFACE_STATE	
		Format:	OpCode	
15:12		<b>Reserved</b>		
		Format:	MBZ	
11:0		<b>Dword Length</b>		
		Format:	U12	
		(Excludes Dwords 0, 1).		
		<b>Value</b>	<b>Name</b>	
1	31:28	<b>Surface Id</b>		
		Format:	U4	

<b>HCP_SURFACE_STATE</b>			
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0h	HEVC: For current decoded Picture	8-bit uncompressed data
	1h	Source Input Picture (encoder)	8-bit uncompressed data
	2h	Prev Reference Picture	(VP9 only) Previous Reference
	3h	Golden Reference Picture	(VP9 only) Golden Reference
	4h	AltRef Reference Picture	(VP9 only) AltRef Reference
	5h	Reference Picture	
	27:17	<b>Reserved</b>	
		Format:	MBZ
	16:0	<b>Surface Pitch Minus1</b>	
		Format:	U17-1
		This field specifies the surface pitch in (#Bytes - 1).	
		<b>Programming Notes</b>	
		<ul style="list-style-type: none"> <li>For tiled surfaces, the pitch must be a multiple of the tile width.</li> <li>If <b>Half Pitch for Chroma</b> is set, this field must be a multiple of two tile widths for tiled surfaces, or a multiple of 2 bytes for linear surfaces.</li> </ul>	
		<b>For Y-tiled surfaces: Range = [127, 524287]-&gt;[128B,256KB] = [1 tile, 2048 tiles].</b>	
2	27:15	<b>Reserved</b>	
		Format:	MBZ
	14:0	<b>Y Offset for U(Cb) in pixel</b>	
		Format:	U15_Pixel_Row_Offset
		This field specifies the vertical offset in rows from the <b>Surface Base Address</b> to the start (origin) of the U(Cb) plane or the interleaved UV plane if <b>Interleave Chroma</b> is enabled. This field is only used for PLANAR surface formats.	
		<b>Programming Notes</b>	
		<ul style="list-style-type: none"> <li>For PLANAR_420 surface formats, the alignment of this field follows the tile mode described in bits 14:13 of the <b>Memory Address Attributes</b> table.</li> <li>TileY (legacy 4k) - 32 pixel aligned</li> <li>TileYF (New 4k) - 64 pixel aligned</li> <li>TileYS (64k) - 256 pixel aligned</li> </ul>	

## HCP\_TILE\_STATE

<b>HCP_TILE_STATE</b>		
Project:	CHV, BSW	
Source:	VideoCS	
Length Bias:	2	
<p>The HCP is selected with the <b>Media Instruction Opcode "7h"</b> for all HCP Commands. Each HCP command has assigned a media instruction command as defined in DWord 0, BitField 22:16.</p>		
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 3h PARALLEL_VIDEO_PIPE
		Format: OpCode
	28:27	<b>Pipeline Type</b>
		Default Value: 2h
		Format: OpCode
	26:23	<b>Media Instruction Opcode</b>
Default Value: 7h Codec/Engine Name		
Format: OpCode Codec/Engine Name = HCP = 7h		
22:16	<b>Media Instruction Command</b>	
	Default Value: 11h HCP_TILE_STATE	
	Format: OpCode	
15:12	<b>Reserved</b>	
	Format: MBZ	
11:0	<b>Dword Length</b>	
	Format: U12 (Excludes Dwords 0, 1).	
	<b>Value</b>	<b>Name</b>
	Bh	
1	31:10	<b>Reserved</b>
		Format: MBZ
9:5	<b>NumTileColumnsMinus1</b>	Format: U5
		Specifies the number of tile columns in Ctbs per picture.

<b>HCP_TILE_STATE</b>				
	4:0	<b>NumTileRowsMinus1</b> Format: <table border="1" style="width: 100%;"><tr><td style="width: 80%;"></td><td style="width: 20%; text-align: center;">U5</td></tr></table> Specifies the number of tile rows in Ctbs per picture.		U5
	U5			
2	31:24	<b>Ctb column position of tile column 3</b> Format: <table border="1" style="width: 100%;"><tr><td style="width: 80%;"></td><td style="width: 20%; text-align: center;">U8</td></tr></table>		U8
		U8		
	23:16	<b>Ctb column position of tile column 2</b> Format: <table border="1" style="width: 100%;"><tr><td style="width: 80%;"></td><td style="width: 20%; text-align: center;">U8</td></tr></table>		U8
		U8		
15:8	<b>Ctb column position of tile column 1</b> Format: <table border="1" style="width: 100%;"><tr><td style="width: 80%;"></td><td style="width: 20%; text-align: center;">U8</td></tr></table>		U8	
	U8			
7:0	<b>Ctb column position of tile column 0</b> Format: <table border="1" style="width: 100%;"><tr><td style="width: 80%;"></td><td style="width: 20%; text-align: center;">U8</td></tr></table>		U8	
	U8			
3	31:24	<b>Ctb column position of tile column 7</b> Format: <table border="1" style="width: 100%;"><tr><td style="width: 80%;"></td><td style="width: 20%; text-align: center;">U8</td></tr></table>		U8
		U8		
	23:16	<b>Ctb column position of tile column 6</b> Format: <table border="1" style="width: 100%;"><tr><td style="width: 80%;"></td><td style="width: 20%; text-align: center;">U8</td></tr></table>		U8
		U8		
15:8	<b>Ctb column position of tile column 5</b> Format: <table border="1" style="width: 100%;"><tr><td style="width: 80%;"></td><td style="width: 20%; text-align: center;">U8</td></tr></table>		U8	
	U8			
7:0	<b>Ctb column position of tile column 4</b> Format: <table border="1" style="width: 100%;"><tr><td style="width: 80%;"></td><td style="width: 20%; text-align: center;">U8</td></tr></table>		U8	
	U8			
4	31:24	<b>Ctb column position of tile column 11</b> Format: <table border="1" style="width: 100%;"><tr><td style="width: 80%;"></td><td style="width: 20%; text-align: center;">U8</td></tr></table>		U8
		U8		
	23:16	<b>Ctb column position of tile column 10</b> Format: <table border="1" style="width: 100%;"><tr><td style="width: 80%;"></td><td style="width: 20%; text-align: center;">U8</td></tr></table>		U8
		U8		
15:8	<b>Ctb column position of tile column 9</b> Format: <table border="1" style="width: 100%;"><tr><td style="width: 80%;"></td><td style="width: 20%; text-align: center;">U8</td></tr></table>		U8	
	U8			
7:0	<b>Ctb column position of tile column 8</b> Format: <table border="1" style="width: 100%;"><tr><td style="width: 80%;"></td><td style="width: 20%; text-align: center;">U8</td></tr></table>		U8	
	U8			
5	31:24	<b>Ctb column position of tile column 15</b> Format: <table border="1" style="width: 100%;"><tr><td style="width: 80%;"></td><td style="width: 20%; text-align: center;">U8</td></tr></table>		U8
		U8		
	23:16	<b>Ctb column position of tile column 14</b> Format: <table border="1" style="width: 100%;"><tr><td style="width: 80%;"></td><td style="width: 20%; text-align: center;">U8</td></tr></table>		U8
		U8		
15:8	<b>Ctb column position of tile column 13</b> Format: <table border="1" style="width: 100%;"><tr><td style="width: 80%;"></td><td style="width: 20%; text-align: center;">U8</td></tr></table>		U8	
	U8			
7:0	<b>Ctb column position of tile column 12</b> Format: <table border="1" style="width: 100%;"><tr><td style="width: 80%;"></td><td style="width: 20%; text-align: center;">U8</td></tr></table>		U8	
	U8			

<b>HCP_TILE_STATE</b>		
6	31:24	<b>Ctb column position of tile column 19</b> Format:   U8
	23:16	<b>Ctb column position of tile column 18</b> Format:   U8
	15:8	<b>Ctb column position of tile column 17</b> Format:   U8
	7:0	<b>Ctb column position of tile column 16</b> Format:   U8
7	31:24	<b>Ctb row position of tile row 3</b> Format:   U8
	23:16	<b>Ctb row position of tile row 2</b> Format:   U8
	15:8	<b>Ctb row position of tile row 1</b> Format:   U8
	7:0	<b>Ctb row position of tile row 0</b> Format:   U8
8	31:24	<b>Ctb row position of tile row 7</b> Format:   U8
	23:16	<b>Ctb row position of tile row 6</b> Format:   U8
	15:8	<b>Ctb row position of tile row 5</b> Format:   U8
	7:0	<b>Ctb row position of tile row 4</b> Format:   U8
9	31:24	<b>Ctb row position of tile row 11</b> Format:   U8
	23:16	<b>Ctb row position of tile row 10</b> Format:   U8
	15:8	<b>Ctb row position of tile row 9</b> Format:   U8
	7:0	<b>Ctb row position of tile row 8</b> Format:   U8
10	31:24	<b>Ctb row position of tile row 15</b> Format:   U8

<b>HCP_TILE_STATE</b>		
	23:16	<b>Ctb row position of tile row 14</b> Format: U8
	15:8	<b>Ctb row position of tile row 13</b> Format: U8
	7:0	<b>Ctb row position of tile row 12</b> Format: U8
11	31:24	<b>Ctb row position of tile row 19</b> Format: U8
	23:16	<b>Ctb row position of tile row 18</b> Format: U8
	15:8	<b>Ctb row position of tile row 17</b> Format: U8
	7:0	<b>Ctb row position of tile row 16</b> Format: U8
12	31:16	<b>Reserved</b> Format: MBZ
	15:8	<b>Ctb row position of tile row 21</b> Format: U8
	7:0	<b>Ctb row position of tile row 20</b> Format: U8

## HCP\_WEIGHTOFFSET\_STATE

<b>HCP_WEIGHTOFFSET_STATE</b>			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>The HCP is selected with the <b>Media Instruction Opcode "7h"</b> for all HCP Commands. Each HCP command has assigned a media instruction command as defined in DWord 0, BitField 22:16.</p> <p>This slice level command is issued in both the encoding and decoding processes, if the weighted_pred_flag or weighted_bipred_flag equals one. If zero, then this command is not issued. Weight Prediction Values are provided in this command. Only Explicit Weight Prediction is supported in encoder.</p> <p>For P-Slice, this command is issued only once together with HCP_REF_IDX_STATE Command for L0 list. For B-Slice, this command can be issued up to two times together with HCP_REF_IDX_STATE Command, one for L0 list and one for L1 list.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline Type</b>	
		Default Value:	2h
		Format:	OpCode
	26:23	<b>Media Instruction Opcode</b>	
		Default Value:	7h Codec/Engine Name
		Format:	OpCode
			Codec/Engine Name = HCP = 7h
22:16	<b>Media Instruction Command</b>		
	Default Value:	13h HCP_WEIGHTOFFSET_STATE	
	Format:	OpCode	
15:12	<b>Reserved</b>		
	Format:	MBZ	
11:0	<b>Dword Length</b>		
	Format:	=n	
	(Excludes Dwords 0, 1).		
	<b>Value</b>	<b>Name</b>	<b>Project</b>
		20h                      32	
1	31:1	<b>Reserved</b>	

<b>HCP_WEIGHTOFFSET_STATE</b>									
	<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ						
Format:	MBZ								
0	<p><b>RefPicListNum</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>U1</td> </tr> </table> <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th style="width: 20%;">Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Reference Picture List 0</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Reference Picture List 1</td> </tr> </tbody> </table>	Format:	U1	Value	Name	0	Reference Picture List 0	1	Reference Picture List 1
Format:	U1								
Value	Name								
0	Reference Picture List 0								
1	Reference Picture List 1								
2..17	<p>31:16 <b>Reserved</b></p> <p>15:8 <b>luma_offset_IX[i]</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>U8</td> </tr> </table> <p>Where X is the RefPicListNum and i is the list entry number 0 through 15. DW2 corresponds to i=0, DW17 corresponds to i=15.</p> <p>Valid only if explicit weighted prediction for luma is enabled, otherwise must be zero.</p> <p>7:0 <b>delta_luma_weight_IX[i]</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>U8</td> </tr> </table> <p>Where X is the RefPicListNum and i is the list entry number 0 through 15. DW2 corresponds to i=0, DW17 corresponds to i=15.</p> <p>Valid only if explicit weighted prediction for luma is enabled, otherwise must be zero.</p>	Format:	U8	Format:	U8				
Format:	U8								
Format:	U8								
18..33	<p>31:24 <b>ChromaOffsetLX [i][1]</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>U8</td> </tr> </table> <p>Where X is the RefPicListNum and i is the list entry number 0 through 15. DW2 corresponds to i=0, DW17 corresponds to i=15.</p> <p>Valid only if explicit weighted prediction for chroma is enabled, otherwise must be zero.</p> <p>23:16 <b>delta_chroma_weight_IX[i][1]</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>U8</td> </tr> </table> <p>Where X is the RefPicListNum and i is the list entry number 0 through 15. DW2 corresponds to i=0, DW17 corresponds to i=15.</p> <p>Valid only if explicit weighted prediction for chroma is enabled, otherwise must be zero.</p> <p>15:8 <b>ChromaOffsetLX[i][0]</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>U8</td> </tr> </table> <p>Where X is the RefPicListNum and i is the list entry number 0 through 15. DW2 corresponds to i=0, DW17 corresponds to i=15.</p> <p>Valid only if explicit weighted prediction for chroma is enabled, otherwise must be zero.</p>	Format:	U8	Format:	U8	Format:	U8		
Format:	U8								
Format:	U8								
Format:	U8								



<b>HCP_WEIGHTOFFSET_STATE</b>			
7:0	<p><b>delta_chroma_weight_IX[i][0]</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U8</td> </tr> </table> <p>Where X is the RefPicListNum and i is the list entry number 0 through 15. DW2 corresponds to i=0, DW17 corresponds to i=15.</p> <p>Valid only if explicit weighted prediction for chroma is enabled, otherwise must be zero.</p>	Format:	U8
Format:	U8		

## HI8DS Render Target Write MSD

<b>MSD_RTW_HI8DS - HI8DS Render Target Write MSD</b>								
Project:	CHV, BSW							
Source:	Render Cache DataPort							
Length Bias:	1							
Family:	Other							
Group:	Render Target R/W							
DWord	Bit	Description						
0	31	<b>Reserved</b>						
	30	<b>Message Precision Subtype</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>0h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Full precision data message</p>	Default Value:	0h	Project:	All	Format:	Opcode
	Default Value:	0h						
	Project:	All						
	Format:	Opcode						
	29	<b>Reserved</b>						
	28:25	<b>Message Length</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U4</td> </tr> </table> <p>Specifies the number of 256-bit GRF registers sent as the message payload (including the header). Valid value ranges are 1 to 15.</p>	Project:	All	Format:	U4		
	Project:	All						
	Format:	U4						
	24:20	<b>Response Length</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U5</td> </tr> </table> <p>Specifies the number of 256-bit GRF registers expected as the message response payload. Valid value ranges are 0 to 16.</p>	Project:	All	Format:	U5		
Project:	All							
Format:	U5							
19	<b>Header Present</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 40%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_MHP [CHV, BSW]</td> </tr> </table> <p>If set, indicates that the message includes the 2-register header.</p>	Project:	All	Format:	MDC_MHP [CHV, BSW]			
Project:	All							
Format:	MDC_MHP [CHV, BSW]							
18	<b>Reserved</b>							
17:14	<b>Message Type</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>0Ch</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Render Target Write message</p>	Default Value:	0Ch	Project:	All	Format:	Opcode	
Default Value:	0Ch							
Project:	All							
Format:	Opcode							

## MSD\_RTW\_HI8DS - HI8DS Render Target Write MSD

13	<b>Reserved</b>		
	Project:	CHV, BSW	
	Format:	MBZ	
	Ignored		
12	<b>Last Render Target Select</b>		
	Project:	All	
	Format:	Enable	
	<p>This bit must be set on the last render target write message sent for each group of pixels. For single render target pixel shaders, this bit is set on all render target write messages. For multiple render target pixel shaders, this bit is set only on messages sent to the last render target. This bit must be zero for SIMD8 Image Write message. In general, when threads are not launched by 3D FF, this bit must be zero.</p>		
	<b>Programming Notes</b>		
	<p>When a pixel shader has render target writes at finer granularity than the dispatch rate, last render target write to a null surface must be present at the dispatch rate with this bit set. In particular, if a kernel is dispatched at pixel rate and it only writes to render targets at sample-rate, it must include a pixel-rate render target write to a null surface with Last Render Target Select bit enabled.</p>		
11	<b>Slot Group Select</b>		
	Project:	All	
	Format:	MDC_RT_SGS [CHV, BSW]	
	This field selects whether slots 15:0 or slots 31:16 are used for bypassed data.		
10:8	<b>Render Target Message Subtype</b>		
	Default Value:	3h	
	Project:	All	
	Format:	Opcode	
	SIMD8 dual source message. Use slots [15:8] for pixel enables, X/Y addresses, and oMask.		
	<b>Programming Notes</b>		
	The above slots indicated are within the 16 slots selected by Slot Group Select. If SLOTGRP_HI is selected, slots [31:24] are referenced instead of [15:8].		
7:0	<b>Binding Table Index</b>		
	Project:	All	
	Format:	MDC_BTS [CHV, BSW]	
	Specifies the Binding Table Index for the message		

# Illegal

<b>illegal - Illegal</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
<p>The Illegal Opcode Exception Enable flag in cr0.1 is normally set so the normal processing of an illegal opcode is to transfer control to the System Routine. Instruction dispatch treats any unused 8-bit opcode (including bit 7 of the instruction, reserved for future opcode expansion) as if it is the illegal opcode. The illegal opcode is zero because that byte value is more likely than most to be read via a wayward instruction pointer. The illegal instruction is an instruction only in the same way that a NULL pointer in software is a pointer. Both are special values indicating invalid instances.</p>			
Format: illegal			
<b>Restriction</b>			
The illegal instruction takes no instruction options.			
<b>Syntax</b>			
illegal			
<b>Pseudocode</b>			
{ Set the Illegal Opcode Exception Status bit in cr0.1. if ( Illegal Opcode Exception Enable is set in cr0.1 ) { Transfer control to the System Routine (return address to AIP, IP = SIP). } }			
Predication	Conditional Modifier	Saturation	Source Modifier
N	N	N	N
DWord	Bit	Description	
0.3	127:7	<b>Reserved</b>	
		Format:	MBZ
	6:0	<b>Opcode</b>	
		Format:	EU_OPCODE [CHV, BSW]

## Integer Subtraction with Borrow

<b>subb - Integer Subtraction with Borrow</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
<p>The subb instruction performs component-wise subtraction of src0 and src1 and stores the results in dst, it also stores the borrow into acc. If the operation produces a borrow (src0 &lt; src1), write 0x00000001 to acc, else write 0x00000000 to acc.</p>			
Format: [(pred)] subb[.cmod] (exec_size) dst src0 src1			
Restriction			
AccWrEn is required. The accumulator is an implicit destination and thus cannot be an explicit destination operand.			
Syntax			
[(pred)] subb[.cmod] (exec_size) reg reg reg [(pred)] subb[.cmod] (exec_size) reg reg imm32			
Pseudocode			
Evaluate(WrEn); for ( n = 0; n < exec_size; n++ ) { if ( WrEn.chan[n] ) { dst.chan[n] = src0.chan[n] - src1.chan[n]; acc.chan[n] = borrow(src.chan[n] - src1.chan[n]); } }			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	N	Y	N
Src Types	Dst Types		
UD	UD		
DWord	Bit	Description	
0..3	127:64	<b>RegSource</b>	
		Exists If:	(([RegSource][Src1.RegFile]!='IMM')
	Format:	EU_INSTRUCTION_SOURCES_REG_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>	
Exists If:		([ImmSource][Src1.RegFile]='IMM')	
Format:	EU_INSTRUCTION_SOURCES_REG_IMM [CHV, BSW]		
63:32	<b>Operand Controls</b>		
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]	
31:0	<b>Header</b>		
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]	

## Join

<b>join - Join</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
<p>The join instruction makes the inactive channels active at the join IP if those channels are predicated. Any deactivated channels due to a goto instruction match the join IP are activated (qualified with predicates at join). If no IP is matched at this join, the program goes to the next IP with the active channels which followed the program path up to the join instruction. If no active channels are present after executing the join instruction, the program jumps to the offset specified by JIP instead of next IP. The join instruction is used in conjunction with a goto instruction. The join activates channels that are deactivated by the goto instruction. See the goto instruction for the deactivation rules. The goto and join instructions enable unstructured program control flow. These instructions must be used with additional care where dangling channels can result without proper compiler checks, meaning that it is expected that programs will navigate through these paths to reactivate the channels. Hardware does not provide native checks or reconvergence. The following table describes the 32-bit JIP. In GEN binary, JIP is at location src1 and must be of type D (signed DWord integer). JIP must be an immediate operand and is a signed 32-bit number. This value is added to IP pre-increment. If SPF is ON, none of the PclP are updated.</p>			
Format: [(pred)] join (exec_size) JIP			
<b>Programming Notes</b>			
An index of 0 does nothing, continuing execution with the next instruction.			
An index of -16 (if the jmpI instruction is in native format) or -8 (if the jmpI instruction is in compact format) is an infinite loop on the jmpI instruction.			
<b>Restriction</b>			
The {NoMask} instruction option must be specified.			
The index data type must be D (Signed DWord Integer).			
<b>Syntax</b>			
[(pred)] join (exec_size) imm32			
<b>Pseudocode</b>			
Evaluate(WrEn); for ( n = 0; n < exec_size; n++ ) { if (WrEn.chan[n] ) { // for the predicated channels and the remaining channels PclP[n] = IP + 1; } } if ( PclP != (IP + 1) ) { // for all channels when no channels are activated and no other active channels Jump(IP + JIP); }			
<b>Errata</b>	<b>Description</b>		
	A join instruction must not be followed by any instruction requiring register indirect access on source operands.		
<b>Predication</b>	<b>Conditional Modifier</b>	<b>Saturation</b>	<b>Source Modifier</b>
Y	N	N	N

DWord	Bit	Description
0..3	127:96	<b>JIP</b>
		Project: CHV, BSW
		Format: S31 Jump Target Offset. The relative offset in bytes if a jump is taken for the instruction.
	95	<b>Source 0 Address Immediate [9] Sign Bit</b>
	Project: CHV, BSW	
	94:91	<b>Src1.SrcType</b>
		Project: CHV, BSW Format: SrcType [CHV, BSW]
	90:89	<b>Src1.RegFile</b>
		Project: CHV, BSW Format: RegFile [CHV, BSW]
	88:64	<b>Source 0</b>
Exists If: (Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]='Align16') Format: EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN16 [CHV, BSW]		
88:64	<b>Source 0</b>	
	Exists If: (Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]='Align1') Format: EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN1 [CHV, BSW]	
63:32	<b>Operand Control</b>	
	Format: EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]	
31:0	<b>Header</b>	
	Format: EU_INSTRUCTION_HEADER [CHV, BSW]	

## Jump Indexed

<b>jmp_i - Jump Indexed</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
Description			
<p>The jmp_i instruction redirects program execution to an index offset relative to the post-incremented instruction pointer. The index is a signed integer value, with positive or zero integers for forward jumps, and negative integers for backward jumps. Note: Unlike other flow control instructions, the offset used by jmp_i is relative to the incremented instruction pointer rather than the IP value for the instruction itself. In GEN binary, index is at location src1. The ip register must be put (for example, by the assembler) at the dst and src0 locations. Predication is allowed to provide conditional jump with a scalar condition. As the execution size is 1, the first channel of PMASK (flags post prediction control and negate) is used to determine whether the jump is taken or not. If the condition is false, the jump is not taken and execution continues with the next instruction.</p>			
Format: [(pred)] jmp_i (1) index {NoMask}			
Programming Notes			
An index of 0 does nothing, continuing execution with the next instruction.			
An index of -16 (if the jmp_i instruction is in native format) or -8 (if the jmp_i instruction is in compact format) is an infinite loop on the jmp_i instruction.			
Restriction			
The execution size must be 1.			
The {NoMask} instruction option must be specified.			
The index data type must be D (Signed DWord Integer).			
QtrCtrl must not be used for jmp_i instruction.			
Syntax			
[(pred)] jmp_i (1) reg32 {NoMask} [(pred)] jmp_i (1) imm32 {NoMask}			
Pseudocode			
Evaluate(WrEn); if ( WrEn != 0 ) { Jump(IP + 1 + index ); // IP + 1 is a pseudocode idiom for the IP of the following instruction. }			
Errata	Description		
	A jmp_i instruction must not be followed by any instruction requiring register indirect access on source operands.		
Predication	Conditional Modifier	Saturation	Source Modifier
Y	N	N	N



<b>jmpj - Jump Indexed</b>		
<b>Src Types</b>		
D		
DWord	Bit	Description
0..3	127:96	<b>JIP</b>
		Project: CHV, BSW
		Format: S31 Jump Target Offset. The relative offset in bytes if a jump is taken for the instruction.
	95	<b>Source 0 Address Immediate [9] Sign Bit</b>
		Project: CHV, BSW
	94:91	<b>Src1.SrcType</b>
		Project: CHV, BSW
		Format: SrcType [CHV, BSW]
	90:89	<b>Src1.RegFile</b>
		Project: CHV, BSW
	Format: RegFile [CHV, BSW]	
88:64	<b>Source 0</b>	
	Exists If: (Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]='Align16')	
	Format: EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN16 [CHV, BSW]	
88:64	<b>Source 0</b>	
	Exists If: (Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]='Align1')	
	Format: EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN1 [CHV, BSW]	
63:32	<b>Operand Control</b>	
	Format: EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]	
31:0	<b>Header</b>	
	Format: EU_INSTRUCTION_HEADER [CHV, BSW]	

## Leading Zero Detection

<b>lzd - Leading Zero Detection</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
The lzd instruction counts component-wise the leading zeros from src0 and stores the resulting counts in dst. If src0 is zero, store 32 in dst.			
Format: [(pred)] lzd[.cmod] (exec_size) dst src0			
Restriction			
Accumulator cannot be destination, implicit or explicit.			
Syntax			
[(pred)] lzd[.cmod] (exec_size) reg reg [(pred)] lzd[.cmod] (exec_size) reg reg			
Pseudocode			
Evaluate(WrEn); for ( n = 0; n < exec_size; n++ ) { if ( WrEn.chan[n] ) { UD udScalar = src0.chan[n]; UD cnt = 0; while ( (udScalar & (1 << 31)) == 0 && cnt != 32 ) { cnt ++; udScalar = udScalar << 1; } dst.chan[n] = cnt; } }			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	Y	Y	Y
Src Types	Dst Types		
D, UD	UD		
DWord	Bit	Description	
0..3	127:64	<b>RegSource</b>	
		Exists If:	([Operand Controls][Src0.RegFile]!='IMM')
	Format:	EU_INSTRUCTION_SOURCES_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>	
Exists If:		([Operand Controls][Src0.RegFile]='IMM')	
Format:	EU_INSTRUCTION_SOURCES_IMM32 [CHV, BSW]		
63:32	<b>Operand Controls</b>		
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]	
31:0	<b>Header</b>		
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]	

## Line

<b>line - Line</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
<p>The line instruction computes a component-wise line equation (<math>v = p * u + q</math> where <math>u, v</math> are vectors and <math>p, q</math> are scalars) of <code>src0</code> and <code>src1</code> and stores the results in <code>dst</code>. <code>src1</code> is the input vector <math>u</math>. <code>src0</code> provides input scalars <math>p</math> and <math>q</math>, where <math>p</math> is the scalar value based on the region description of <code>src0</code> and <math>q</math> is the scalar value implied from <code>src0</code> region. Specifically, <math>q</math> is the fourth component of the 4-tuple (128-bit aligned) that <math>p</math> belongs to.</p>			
Format: <code>[(pred)] line[.cmod] (exec_size) dst src0 src1</code>			
Restriction			
This is a specialized instruction that only supports an execution size (ExecSize) of 8 or 16.			
The <code>src0</code> region must be a replicated scalar (with <code>HorzStride == VertStride == 0</code> ).			
<code>src0</code> must specify <code>.0</code> or <code>.4</code> as the subregister number, corresponding to a subregister byte offset of 0 or 16.			
Source operands cannot be accumulators.			
Syntax			
<code>[(pred)] line[.cmod] (exec_size) reg reg reg [(pred)] line[.cmod] (exec_size) reg reg imm32</code>			
Pseudocode			
<pre>Evaluate(WrEn); for ( n = 0; n &lt; exec_size; n++ ) { dwP = src0.RegNum.SubRegNum[bits4:2]; // A DWord-aligned scalar. dwQ = src0.RegNum.(SubRegNum[bit4]   0x8); // Fourth component. if ( WrEn.chan[n] ) { dst.chan[n] = dwP * src1.chan[n] + dwQ; } }</pre>			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	Y	Y	Y
Src Types	Dst Types		
F	F		
DWord	Bit	Description	
0..3	127:64	<b>RegSource</b>	
		Exists If:	<code>!([RegSource][Src1.RegFile] == 'IMM')</code>
	Format:	<code>EU_INSTRUCTION_SOURCES_REG_REG [CHV, BSW]</code>	
	127:64	<b>ImmSource</b>	
Exists If:		<code>!([ImmSource][Src1.RegFile] == 'IMM')</code>	
Format:	<code>EU_INSTRUCTION_SOURCES_REG_IMM [CHV, BSW]</code>		
63:32	<b>Operand Controls</b>		
Format:	<code>EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]</code>		
31:0	<b>Header</b>		
	Format:	<code>EU_INSTRUCTION_HEADER [CHV, BSW]</code>	

## Linear Interpolation

<b>Irp - Linear Interpolation</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
The Irp instruction takes component-wise multiplication of src0 and src1, and adds the result to the component-wise multiplication of src2 and (1 - src0), and then stores the final results in dst.			
Format: [(pred)] Irp[.cmod] (exec_size) dst src0 src1 src2			
<b>Restriction</b>			
The vertical stride (VertStride) is overloaded to 4 in HW for 3-source instructions.			
The overflow conditional modifier (.o) is not allowed.			
No explicit accumulator access because this is a three-source instruction. AccWrEn is allowed for implicitly updating the accumulator.			
All three-source instructions have certain restrictions, described in Instruction Formats [CHV, BSW].			
<b>Syntax</b>			
[(pred)] Irp[.cmod] (exec_size) reg reg reg			
<b>Pseudocode</b>			
Evaluate(WrEn); for ( n = 0; n < exec_size; n++ ) { if ( WrEn.chan[n] ) { dst.chan[n] = src1.chan[n] * src0.chan[n] + src2.chan[n] * (1.0 - src0.chan[n]); } }			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	N	Y	Y
Src Types	Dst Types		
F	F		
DWord	Bit	<b>Description</b>	
0..3	127:126	<b>Reserved</b> Format: MBZ	
	125:106	<b>Source 2</b> Format: EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC [CHV, BSW]	
	105	<b>Reserved</b> Format: MBZ	
	104:85	<b>Source 1</b> Format: EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC [CHV, BSW]	
	84	<b>Reserved</b> Format: MBZ	

<b>Irp - Linear Interpolation</b>		
83:64	<b>Source 0</b>	Format: EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC [CHV, BSW]
63:56	<b>Destination Register Number</b>	Format: DstRegNum [CHV, BSW]
55:53	<b>Destination Subregister Number</b>	Format: DstSubRegNum[2:0]
52:49	<b>Destination Channel Enable</b>	Format: ChanEn[4] Four channel enables are defined for controlling which channels are written into the destination region. These channel mask bits are applied in a modulo-four manner to all ExecSize channels. There is 1-bit Channel Enable for each channel within the group of 4. If the bit is cleared, the write for the corresponding channel is disabled. If the bit is set, the write is enabled. Mnemonics for the bit being set for the group of 4 are x, y, z, and w, respectively, where x corresponds to Channel 0 in the group and w corresponds to channel 3 in the group
48:42	<b>Reserved</b>	
41:40	<b>Source 2 Modifier</b>	Exists If: $\text{!}([Property[Source\ Modifier]=='true'])$ Format: SrcMod [CHV, BSW]
39:38	<b>Source 1 Modifier</b>	Exists If: $\text{!}([Property[Source\ Modifier]=='true'])$ Format: SrcMod [CHV, BSW]
41:36	<b>Reserved</b>	Exists If: $\text{!}([Property[Source\ Modifier]=='false'])$ Format: MBZ
37:36	<b>Source 0 Modifier</b>	Exists If: $\text{!}([Property[Source\ Modifier]=='true'])$ Format: SrcMod [CHV, BSW]
35	<b>Reserved</b>	
34	<b>Reserved</b>	Format: MBZ
33	<b>Flag Subregister Number</b>	This field contains the flag subregister number for instructions with a non-zero Conditional Modifier.
32	<b>Reserved</b>	Format: MBZ
31:0	<b>Header</b>	Format: EU_INSTRUCTION_HEADER [CHV, BSW]

## LO8DS Render Target Write MSD

MSD_RTW_LO8DS - LO8DS Render Target Write MSD			
Project:	CHV, BSW		
Source:	Render Cache DataPort		
Length Bias:	1		
Family:	Other		
Group:	Render Target R/W		
DWord	Bit	Description	
0	31	<b>Reserved</b>	
	30	<b>Message Precision Subtype</b>	
		Default Value:	0h
		Project:	All
		Format:	Opcode
			Full precision data message
	29	<b>Reserved</b>	
	28:25	<b>Message Length</b>	
		Project:	All
		Format:	U4
		Specifies the number of 256-bit GRF registers sent as the message payload (including the header). Valid value ranges are 1 to 15.	
24:20	<b>Response Length</b>		
	Project:	All	
	Format:	U5	
		Specifies the number of 256-bit GRF registers expected as the message response payload. Valid value ranges are 0 to 16.	
19	<b>Header Present</b>		
	Project:	All	
	Format:	MDC_MHP [CHV, BSW]	
		If set, indicates that the message includes the 2-register header.	
18	<b>Reserved</b>		
17:14	<b>Message Type</b>		
	Default Value:	0Ch	
	Project:	All	
	Format:	Opcode	
		Render Target Write message	

<b>MSD_RTW_LO8DS - LO8DS Render Target Write MSD</b>								
13	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>Ignored</p>	Project:	CHV, BSW	Format:	MBZ			
Project:	CHV, BSW							
Format:	MBZ							
12	<p><b>Last Render Target Select</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This bit must be set on the last render target write message sent for each group of pixels. For single render target pixel shaders, this bit is set on all render target write messages. For multiple render target pixel shaders, this bit is set only on messages sent to the last render target. This bit must be zero for SIMD8 Image Write message. In general, when threads are not launched by 3D FF, this bit must be zero.</p> <table border="1" style="width: 100%; background-color: #e6f2ff;"> <tr> <th style="text-align: center;">Programming Notes</th> </tr> </table> <p>When a pixel shader has render target writes at finer granularity than the dispatch rate, last render target write to a null surface must be present at the dispatch rate with this bit set. In particular, if a kernel is dispatched at pixel rate and it only writes to render targets at sample-rate, it must include a pixel-rate render target write to a null surface with Last Render Target Select bit enabled.</p>	Project:	All	Format:	Enable	Programming Notes		
Project:	All							
Format:	Enable							
Programming Notes								
11	<p><b>Slot Group Select</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_RT_SGS [CHV, BSW]</td> </tr> </table> <p>This field selects whether slots 15:0 or slots 31:16 are used for bypassed data.</p>	Project:	All	Format:	MDC_RT_SGS [CHV, BSW]			
Project:	All							
Format:	MDC_RT_SGS [CHV, BSW]							
10:8	<p><b>Render Target Message Subtype</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Default Value:</td> <td>2h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>SIMD8 dual source message. Use slots [7:0] for pixel enables, X/Y addresses, and oMask.</p> <table border="1" style="width: 100%; background-color: #e6f2ff;"> <tr> <th style="text-align: center;">Programming Notes</th> </tr> </table> <p>The above slots indicated are within the 16 slots selected by Slot Group Select. If SLOTGRP_HI is selected, slots [23:16] are referenced instead of [7:0].</p>	Default Value:	2h	Project:	All	Format:	Opcode	Programming Notes
Default Value:	2h							
Project:	All							
Format:	Opcode							
Programming Notes								
7:0	<p><b>Binding Table Index</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_BTS [CHV, BSW]</td> </tr> </table> <p>Specifies the Binding Table Index for the message</p>	Project:	All	Format:	MDC_BTS [CHV, BSW]			
Project:	All							
Format:	MDC_BTS [CHV, BSW]							

# Logic And

<b>and - Logic And</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
<p>The and instruction performs component-wise logic AND operation between src0 and src1 and stores the results in dst. Register source operands can use source modifiers: Any source modifier is logical, optionally changing a source value <i>s</i> to <math>\sim s</math> (inverting all source bits). This capability allows expressions like a AND (NOT b) to be calculated with one instruction. This operation does not produce sign or overflow conditions. Only the .e/z or .ne/.nz conditional modifiers should be used.</p>			
Format: Source modifier is not allowed if source is an accumulator.			
<b>Restriction</b>			
Source modifier is not allowed if source is an accumulator.			
<b>Syntax</b>			
[(pred)] and[.cmod] (exec_size) reg reg reg [(pred)] and[.cmod] (exec_size) reg reg imm32			
<b>Pseudocode</b>			
Evaluate(WrEn); for ( n = 0; n < exec_size; n++ ) { if ( WrEn.chan[n] ) { dst.chan[n] = src0.chan[n] & src1.chan[n]; } }			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	Y	N	N
Src Types	Dst Types	Project	
*B,*W,*D	*B,*W,*D		
*W,*D,*Q	*W,*D,*Q	CHV, BSW	
DWord	Bit	Description	
0..3	127:64	<b>RegSource</b>	
		Exists If:	((RegSource)[Src1.RegFile]!='IMM')
	Format:	EU_INSTRUCTION_SOURCES_REG_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>	
Exists If:		((ImmSource)[Src1.RegFile]='IMM')	
Format:	EU_INSTRUCTION_SOURCES_REG_IMM [CHV, BSW]		
63:32	<b>Operand Controls</b>		
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]	
31:0	<b>Header</b>		
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]	



## Logic Not

<b>not - Logic Not</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
Description			
<p>The not instruction performs logical NOT operation (or one's complement) of src0 and storing the results in dst. This operation does not produce sign or overflow conditions. Only the .e/z or .ne/.nz conditional modifiers should be used.</p> <p>A register source operand can use a source modifier: Any source modifier is logical, optionally changing a source value s to ~s (inverting all source bits). Such a source modifier is not particularly useful with the not instruction, as it changes the effect of not to just copying bits.</p> <p>Format: [(pred)] not[.cmod] (exec_size) dst src0</p>			
Restriction			
Source modifier is not allowed if source is an accumulator.			
Syntax			
[(pred)] not[.cmod] (exec_size) reg reg [(pred)] not[.cmod] (exec_size) reg imm32			
Pseudocode			
Evaluate(WrEn); for ( n = 0; n < exec_size; n++ ) { if ( WrEn.chan[n] ) { dst.chan[n] = ~ src0.chan[n]; } }			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	N	N	Y
Src Types	Dst Types	Project	
*B,*W,*D	*B,*W,*D		
*W,*D,*Q	*W,*D,*Q	CHV, BSW	
DWord	Bit	Description	
0..3	127:64	<b>RegSource</b>	
		Exists If:	(([Operand Controls][Src0.RegFile]!='IMM')
	Format:	EU_INSTRUCTION_SOURCES_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>	
Exists If:		(([Operand Controls][Src0.RegFile]='IMM')	
Format:	EU_INSTRUCTION_SOURCES_IMM32 [CHV, BSW]		
63:32	<b>Operand Controls</b>		
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]	
31:0	<b>Header</b>		
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]	

## Logic Or

<b>or - Logic Or</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
Description			
<p>The or instruction performs component-wise logic OR operation between src0 and src1 and stores the results in dst. This operation does not produce sign or overflow conditions. Only the .e/.z or .ne/.nz conditional modifiers should be used.</p> <p>Register source operands can use source modifiers: Any source modifier is logical, optionally changing a source value s to ~s (inverting all source bits). This capability allows expressions like a OR (NOT b) to be calculated with one instruction.</p> <p>Format: [(pred)] or[.cmod] (exec_size) dst src0 src1</p>			
Restriction			
Source modifier is not allowed if source is an accumulator.			
Syntax			
[(pred)] or[.cmod] (exec_size) reg reg reg [(pred)] or[.cmod] (exec_size) reg reg imm32			
Pseudocode			
<pre>Evaluate(WrEn); for ( n = 0; n &lt; exec_size; n++ ) { if ( WrEn.chan[n] ) { dst.chan[n] = src0.chan[n]   src1.chan[n]; } }</pre>			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	N	N	Y
Src Types	Dst Types	Project	
*B,*W,*D	*B,*W,*D		
*W,*D,*Q	*W,*D,*Q	CHV, BSW	
DWord	Bit	Description	
0..3	127:64	<b>RegSource</b>	
		Exists If:	([RegSource][Src1.RegFile]!='IMM')
	Format:	EU_INSTRUCTION_SOURCES_REG_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>	
Exists If:		([ImmSource][Src1.RegFile]='IMM')	
Format:	EU_INSTRUCTION_SOURCES_REG_IMM [CHV, BSW]		
63:32	<b>Operand Controls</b>		
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]	
31:0	<b>Header</b>		
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]	

## Logic Xor

<b>xor - Logic Xor</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
Description			
<p>The xor instruction performs component-wise logic XOR operation between src0 and src1 and stores the results in dst. This operation does not produce sign or overflow conditions. Only the .e/z or .ne/nz conditional modifiers should be used.</p> <p>Register source operands can use source modifiers: Any source modifier is logical, optionally changing a source value s to ~s (inverting all source bits). This capability allows expressions like a XOR (NOT b) to be calculated with one instruction.</p> <p>Format: [(pred)] xor[.cmod] (exec_size) dst src0 src1</p>			
Restriction			
Source modifier is not allowed if source is an accumulator.			
Syntax			
[(pred)] xor[.cmod] (exec_size) reg reg reg [(pred)] xor[.cmod] (exec_size) reg reg imm32			
Pseudocode			
Evaluate(WrEn); for ( n = 0; n < exec_size; n++ ) { if ( WrEn.chan[n] ) { dst.chan[n] = src0.chan[n] ^ src1.chan[n];}}			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	N	N	Y
Src Types	Dst Types	Project	
*B,*W,*D	*B,*W,*D		
*W,*D,*Q	*W,*D,*Q	CHV, BSW	
DWord	Bit	Description	
0..3	127:64	<b>RegSource</b>	
		Exists If:	((RegSource)[Src1.RegFile]!='IMM')
	Format:	EU_INSTRUCTION_SOURCES_REG_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>	
Exists If:		((ImmSource)[Src1.RegFile]='IMM')	
Format:	EU_INSTRUCTION_SOURCES_REG_IMM [CHV, BSW]		
63:32	<b>Operand Controls</b>		
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]	
31:0	<b>Header</b>		
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]	

## MEDIA\_CURBE\_LOAD

MEDIA_CURBE_LOAD						
Project:	CHV, BSW					
Source:	RenderCS					
Length Bias:	2					
Workaround: See "GPGPU Command Workarounds" section for additional programming constraints for this command.						
DWord	Bit	Description				
0	31:29	<b>Command Type</b>				
		Default Value:	3h GFXPIPE			
		Format:	OpCode			
	28:27	<b>Pipeline</b>				
		Default Value:	2h Media			
		Format:	OpCode			
	26:24	<b>Media Command Opcode</b>				
		Default Value:	0h MEDIA_CURBE_LOAD			
		Format:	OpCode			
	23:16	<b>SubOpcode</b>				
Default Value:		1h MEDIA_CURBE_LOAD SubOp				
Format:		OpCode				
15:0	<b>DWord Length</b>					
	Project:	All				
	Format:	=n Total Length - 2				
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>2h</td> <td>DWORD_COUNT_n [Default]</td> <td>Excludes DWord (0,1)</td> </tr> </tbody> </table>	Value	Name	Description	2h	DWORD_COUNT_n [Default]
Value	Name	Description				
2h	DWORD_COUNT_n [Default]	Excludes DWord (0,1)				
1	31:0	<b>Reserved</b>				
2	31:17	<b>Reserved</b>				
	16:0	<b>CURBE Total Data Length</b>				
		Project:	All			
Format:	U17 In Bytes					
		<table border="1"> <thead> <tr> <th>Description</th> </tr> </thead> <tbody> <tr> <td>This field provides the length in bytes of the CURBE data. This field must have the same alignment as the Curbe Object Data Start Address.As the CURBE data are sent directly to ROB, range is limited to CURBE Allocation Size.</td> </tr> <tr> <td>This field must be 64-byte aligned.</td> </tr> </tbody> </table>	Description	This field provides the length in bytes of the CURBE data. This field must have the same alignment as the Curbe Object Data Start Address.As the CURBE data are sent directly to ROB, range is limited to CURBE Allocation Size.	This field must be 64-byte aligned.	
Description						
This field provides the length in bytes of the CURBE data. This field must have the same alignment as the Curbe Object Data Start Address.As the CURBE data are sent directly to ROB, range is limited to CURBE Allocation Size.						
This field must be 64-byte aligned.						

<b>MEDIA_CURBE_LOAD</b>														
3	31:0	<p><b>CURBE Data Start Address</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>DynamicStateOffset[31:0] CURBE</td> </tr> </table> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 80%; text-align: center;">Description</th> <th style="width: 20%; text-align: center;">Project</th> </tr> </thead> <tbody> <tr> <td>Specifies the 64-byte aligned address of the CURBE data. This pointer is relative to the <b>Dynamics Base Address</b>.</td> <td style="text-align: center;">CHV, BSW</td> </tr> </tbody> </table> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 60%; text-align: center;">Value</th> <th style="width: 40%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">[0, FFFFFFFFh]</td> <td></td> </tr> </tbody> </table>	Project:	All	Format:	DynamicStateOffset[31:0] CURBE	Description	Project	Specifies the 64-byte aligned address of the CURBE data. This pointer is relative to the <b>Dynamics Base Address</b> .	CHV, BSW	Value	Name	[0, FFFFFFFFh]	
Project:	All													
Format:	DynamicStateOffset[31:0] CURBE													
Description	Project													
Specifies the 64-byte aligned address of the CURBE data. This pointer is relative to the <b>Dynamics Base Address</b> .	CHV, BSW													
Value	Name													
[0, FFFFFFFFh]														

## MEDIA\_INTERFACE\_DESCRIPTOR\_LOAD

MEDIA_INTERFACE_DESCRIPTOR_LOAD								
Project:	CHV, BSW							
Source:	RenderCS							
Length Bias:	2							
A Media_State_Flush should be used before this command to ensure that the temporary Interface Descriptor storage is cleared.								
Workaround: See "GPGPU Command Workarounds" section for additional programming constraints for this command.								
DWord	Bit	Description						
0	31:29	<b>Command Type</b>						
		Default Value:	3h GFXPIPE					
		Format:	OpCode					
	28:27	<b>Pipeline</b>						
		Default Value:	2h Media					
		Format:	OpCode					
	26:24	<b>Media Command Opcode</b>						
		Default Value:	0h MEDIA_INTERFACE_DESCRIPTOR_LOAD					
		Format:	OpCode					
	23:16	<b>SubOpcode</b>						
Default Value:		2h MEDIA_INTERFACE_DESCRIPTOR_LOAD SubOp						
Format:		OpCode						
15:0	<b>DWord Length</b>							
	Format:	=n Total Length - 2						
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>2h</td> <td>DWORD_COUNT_n [Default]</td> <td>Excludes DWord (0,1)</td> </tr> </tbody> </table>	Value	Name	Description	2h	DWORD_COUNT_n [Default]	Excludes DWord (0,1)	
Value	Name	Description						
2h	DWORD_COUNT_n [Default]	Excludes DWord (0,1)						
1	31:0	<b>Reserved</b>						
2	31:17	<b>Reserved</b>						
	16:0	<b>Interface Descriptor Total Length</b>						
		Format:	U17 In bytes					
<p>This field provides the length in bytes of the Interface Descriptor data. This field must have the same alignment as the Interface Descriptor Data Start Address. It must be DQWord (32-byte) aligned. As the Interface Descriptor data are sent directly to ROB, range is limited to CURBE Allocation Size.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>[32,2048]</td> <td>[1,64] interface descriptor entries</td> <td>CHV, BSW</td> </tr> </tbody> </table>			Value	Name	Project	[32,2048]	[1,64] interface descriptor entries	CHV, BSW
Value	Name	Project						
[32,2048]	[1,64] interface descriptor entries	CHV, BSW						

<b>MEDIA_INTERFACE_DESCRIPTOR_LOAD</b>																				
3	31:0	<b>Interface Descriptor Data Start Address</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 15%;">Format:</td> <td>DynamicStateOffset[31:0]INTERFACE_DESCRIPTOR_DATA</td> </tr> <tr> <td colspan="2" style="text-align: center;"><b>Description</b></td> </tr> <tr> <td colspan="2">This bit specifies the <u>64-byte</u> aligned address of the Interface Descriptor data. This pointer is relative to the Dynamics Base Address.</td> </tr> <tr> <td colspan="2" style="text-align: right;"><b>Project</b></td> </tr> <tr> <td colspan="2">CHV, BSW</td> </tr> <tr> <td colspan="2" style="text-align: center;"><b>Value</b></td> </tr> <tr> <td colspan="2">[0, FFFFFFFFh]</td> </tr> <tr> <td colspan="2" style="text-align: center;"><b>Name</b></td> </tr> <tr> <td colspan="2"></td> </tr> </table>	Format:	DynamicStateOffset[31:0]INTERFACE_DESCRIPTOR_DATA	<b>Description</b>		This bit specifies the <u>64-byte</u> aligned address of the Interface Descriptor data. This pointer is relative to the Dynamics Base Address.		<b>Project</b>		CHV, BSW		<b>Value</b>		[0, FFFFFFFFh]		<b>Name</b>			
Format:	DynamicStateOffset[31:0]INTERFACE_DESCRIPTOR_DATA																			
<b>Description</b>																				
This bit specifies the <u>64-byte</u> aligned address of the Interface Descriptor data. This pointer is relative to the Dynamics Base Address.																				
<b>Project</b>																				
CHV, BSW																				
<b>Value</b>																				
[0, FFFFFFFFh]																				
<b>Name</b>																				

## MEDIA\_OBJECT

<b>MEDIA_OBJECT</b>			
Project:		CHV, BSW	
Source:		RenderCS	
Length Bias:		2	
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Media Command Pipeline</b>	
		Default Value:	2h Media
		Format:	OpCode
	26:24	<b>Media Command Opcode</b>	
		Default Value:	1h MEDIA_OBJECT
		Format:	OpCode
	23:16	<b>Media Command Sub-Opcode</b>	
		Default Value:	0h MEDIA_OBJECT SubOp
		Format:	OpCode
	15:0	<b>DWord Length</b>	
		Default Value:	4h DWORD_COUNT_n
		Project:	CHV, BSW
Format:		=n Total Length - 2	
<p>Excludes DWords 0,1 <b>Generic Mode:</b> DWord Length = N+4, where N is in the range of [0,504]. The maximum is 504 DW (equivalent to 63 8-DW registers). When both inline and indirect data are fetched for this command, the total size in 8-DW registers must be less than 112 (with both inline data length N and indirect data length rounded up to 8-DW aligned individually). The minimal inline data length is 0.</p>			
1	31:8	<b>Reserved</b>	
	7:6	<b>Reserved</b>	
		Format:	MBZ
	5:0	<b>Interface Descriptor Offset</b>	
		Project:	CHV, BSW
Format:		U6	
<p>This field specifies the offset from the interface descriptor base pointer to the interface descriptor which will be applied to this object. It is specified in units of interface descriptors.</p>			



<b>MEDIA_OBJECT</b>																		
2	31	<p><b>Children Present</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>Enable</td> </tr> </table> <p>Indicates that the root thread may send spawn messages to spawn child threads and/or synchronized root threads. If Children Present is not set, TS signals VFE to dereference the URB handle immediately after it receives acknowledgement from TD that the thread is dispatched. If Children Present is set, the URB handle is forwarded to the root thread and serves as the return URB handle for the root thread. TS does not signal deference at the time of dispatch. TS signals URB handle deference only when it receives a resource dereference message from the thread. <i>In order avoid deadlock, such dereference must be issued once and only once for each URB handle.</i></p>	Format:	Enable														
	Format:	Enable																
	30:27	<b>Reserved</b>																
	26:25	<b>Reserved</b>																
	24	<p><b>Thread Synchronization</b></p> <p>This field when set indicates that the dispatch of the thread originated from this command is based on the "spawn root thread" message.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>No thread synchronization</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Thread dispatch is synchronized by the 'spawn root thread' message</td> </tr> </tbody> </table>	Value	Name	0	No thread synchronization	1	Thread dispatch is synchronized by the 'spawn root thread' message										
	Value	Name																
	0	No thread synchronization																
	1	Thread dispatch is synchronized by the 'spawn root thread' message																
	23	<b>Reserved</b>																
	22	<p><b>Force Destination</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table> <p>If set, bits 20:17 are used to determine the destination of this dispatch, if clear the destination will be chosen based on load.</p>	Project:	CHV, BSW														
Project:	CHV, BSW																	
21	<p><b>Use Scoreboard</b></p> <p>This field specifies whether the thread associated with this command uses hardware scoreboard. Only when this field is set, the scoreboard control fields in the VFE Dword are valid. If this field is cleared, the thread associated with this command bypasses hardware scoreboard.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Not using scoreboard</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Using scoreboard</td> </tr> </tbody> </table>	Value	Name	0	Not using scoreboard	1	Using scoreboard											
Value	Name																	
0	Not using scoreboard																	
1	Using scoreboard																	
20:19	<p><b>Slice Destination Select</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This bit along with the subslice destination select determines the slice that this thread must be sent to. Ignored if <b>Force Destination</b> = 0, or if product only has 1 slice.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">00b</td> <td>Slice 0</td> <td></td> </tr> <tr> <td style="text-align: center;">01b</td> <td>Slice 1</td> <td>Cannot be used in products without a Slice 1.</td> </tr> <tr> <td style="text-align: center;">10b</td> <td>Slice 2</td> <td>Cannot be used in products without a Slice 2.</td> </tr> <tr> <td style="text-align: center;">11b</td> <td>Reserved</td> <td></td> </tr> </tbody> </table>	Project:	CHV, BSW	Value	Name	Description	00b	Slice 0		01b	Slice 1	Cannot be used in products without a Slice 1.	10b	Slice 2	Cannot be used in products without a Slice 2.	11b	Reserved	
Project:	CHV, BSW																	
Value	Name	Description																
00b	Slice 0																	
01b	Slice 1	Cannot be used in products without a Slice 1.																
10b	Slice 2	Cannot be used in products without a Slice 2.																
11b	Reserved																	

<b>MEDIA_OBJECT</b>																		
	<p>18:17 <b>SubSlice Destination Select</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This field selects the SubSlice that this thread must be sent to. Ignored if <b>Force Destination</b> = 0</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>11b</td> <td>Reserved</td> <td>CHV, BSW</td> </tr> <tr> <td>10b</td> <td>SubSlice 2</td> <td></td> </tr> <tr> <td>01b</td> <td>SubSlice 1</td> <td></td> </tr> <tr> <td>00b</td> <td>SubSlice 0</td> <td></td> </tr> </tbody> </table>	Project:	CHV, BSW	Value	Name	Project	11b	Reserved	CHV, BSW	10b	SubSlice 2		01b	SubSlice 1		00b	SubSlice 0	
	Project:	CHV, BSW																
Value	Name	Project																
11b	Reserved	CHV, BSW																
10b	SubSlice 2																	
01b	SubSlice 1																	
00b	SubSlice 0																	
	<p>16:0 <b>Indirect Data Length</b></p> <table border="1"> <tr> <td>Format:</td> <td>U17 In bytes</td> </tr> </table> <p>This field provides the length in bytes of the indirect data. A value zero indicates that indirect data fetching is disabled - subsequently, the Indirect Data Start Address field is ignored. This field must have the same alignment as the Indirect Object Data Start Address. It must be DQWord (32-byte) aligned. As the indirect data are sent directly to URB, range is limited to 496 DW. When both inline and indirect data are fetched for this command, the total size in 8-DW registers must be less than 112 (with both inline data length and indirect data length rounded up to 8-DW aligned).</p>	Format:	U17 In bytes															
Format:	U17 In bytes																	
3	<p>31:0 <b>Indirect Data Start Address</b></p> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[31:0]</td> </tr> </table> <p style="text-align: center;"><b>Description</b></p> <p>This field specifies the Graphics Memory starting address of the data to be loaded into the kernel for processing. This pointer is relative to the <b>Indirect Object Base Address</b>. Hardware ignores this field if indirect data is not present. Alignment of this address depends on the mode of operation.</p> <p>This field specifies the 64-byte aligned address of the indirect data.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>[0,512MB]</td> <td></td> </tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>Bits 31:29 MBZ</p>	Format:	GraphicsAddress[31:0]	Value	Name	[0,512MB]												
Format:	GraphicsAddress[31:0]																	
Value	Name																	
[0,512MB]																		
4	<p>31:25 <b>Reserved</b></p>																	
	<p>24:16 <b>Scoreboard Y</b></p> <table border="1"> <tr> <td>Project:</td> <td></td> </tr> <tr> <td>Format:</td> <td>U9</td> </tr> </table> <p>This field provides the Y term of the scoreboard value of the current thread.</p>	Project:		Format:	U9													
	Project:																	
Format:	U9																	
<p>15:9 <b>Reserved</b></p>																		

<b>MEDIA_OBJECT</b>						
	8:0	<p><b>Scoreboard X</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td></td> </tr> <tr> <td>Format:</td> <td>U9</td> </tr> </table> <p>This field provides the X term of the scoreboard value of the current thread.</p>	Project:		Format:	U9
Project:						
Format:	U9					
5	31:20	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td></td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:		Format:	MBZ
	Project:					
	Format:	MBZ				
	19:16	<p><b>Scoreboard Color</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td></td> </tr> <tr> <td>Format:</td> <td>U4</td> </tr> </table> <p>This field specifies which dependency color the current thread belongs to. It affects the dependency scoreboard control.</p>	Project:		Format:	U4
	Project:					
Format:	U4					
15:8	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ			
Format:	MBZ					
7:0	<p><b>Scoreboard Mask</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td></td> </tr> <tr> <td>Format:</td> <td>Boolean</td> </tr> </table> <p>Each bit indicates the corresponding dependency scoreboard is dependent on. This field is AND'd with the corresponding Scoreboard Mask field in the MEDIA_VFE_STATE command. <b>Bit n (for n = 0...7):</b> Scoreboard n is dependent, where bit 0 maps to n = 0.</p>	Project:		Format:	Boolean	
Project:						
Format:	Boolean					
6..n	31:0	<p><b>Inline Data</b></p> <p>Generic Mode: The format of this data is specified by software. Hardware does not interpret this data; it merely passes it to the kernel for processing. The total size for the inline data and indirect data must not exceed 112 registers.</p>				

## MEDIA\_OBJECT\_GRPID

<b>MEDIA_OBJECT_GRPID</b>			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
<p>The MEDIA_OBJECT_GRPID command is a variation of MEDIA_OBJECT which includes a group id which is used to allocate and track Barriers and Shared Local Memory. The Interface Descriptor is used to specify how much SLM is needed and how many threads will be reporting to the Barrier. All MEDIA_OBJECT_GRPIDs with the same group id should have the same interface descriptor and be dispatched to the same Tslice – the dispatcher will ensure this if Force Destination = 0, but software must ensure this if Force Destination = 1. Software should also ensure that all the threads needed for the Barrier will fit into a Tslice, or the Barrier will never be satisfied. Either SLM or a barrier must be used with MEDIA_OBJECT_GRPID, if neither is needed then a MEDIA_OBJECT must be used instead.</p> <p>MEDIA_OBJECT_GRPID supports the GPGPU version of payload delivery – either indirect or CURBE can be split between the threads in a group (per-thread payload), as well as a section which is sent to all threads (cross-thread payload). See the GPGPU payload section. For indirect, the same pointer must be sent with all the commands associated with the thread group for payload splitting to work properly. Inline data is not split, but the payload attached to each command is sent with that thread. Only one of inline, indirect, or CURBE is allowed, but at least one form of payload must be sent.</p> <p>MEDIA_STATE_FLUSH with the watermark bit must be placed between groups created by MEDIA_OBJECT_GRPID. The Interface Descriptor associated with the watermark must match the Interface Descriptor used for the following group.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Media Command Pipeline</b>	
		Default Value:	2h Media
		Format:	OpCode
	26:24	<b>Media Command Opcode</b>	
		Default Value:	1h MEDIA_OBJECT_GRPID
		Format:	OpCode
	23:16	<b>Media Command Sub-Opcode</b>	
		Default Value:	6h MEDIA_OBJECT_GRPID SubOp
		Format:	OpCode
	15:0	<b>DWord Length</b>	
		Default Value:	5h DWORD_COUNT_n
		Format:	=n Total Length - 2
Excludes DWords 0,1 <b>Generic Mode:</b> DWord Length = N+5, where N is in the range of [0,504].			

<b>MEDIA_OBJECT_GRPID</b>																
		The maximum is 504 DW (equivalent to 63 8-DW registers). When both inline and indirect data are fetched for this command, the total size in 8-DW registers must be less than 112 (with both inline data length N and indirect data length rounded up to 8-DW aligned individually). The minimal inline data length is 0.														
1	31:8	<b>Reserved</b>														
	7:6	<b>Reserved</b>														
	Format: <table border="1" style="width: 100%;"><tr><td style="width: 60%;"></td><td style="width: 40%;">MBZ</td></tr></table>			MBZ												
		MBZ														
5:0	<b>Interface Descriptor Offset</b>															
Format: <table border="1" style="width: 100%;"><tr><td style="width: 60%;"></td><td style="width: 40%;">U6</td></tr></table>			U6	This field specifies the offset from the interface descriptor base pointer to the interface descriptor which will be applied to this object. It is specified in units of interface descriptors.												
	U6															
		<table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>[0,30]</td> <td></td> </tr> </tbody> </table>	Value	Name	[0,30]											
Value	Name															
[0,30]																
2	31:24	<b>Reserved</b>														
	Format: <table border="1" style="width: 100%;"><tr><td style="width: 60%;"></td><td style="width: 40%;">MBZ</td></tr></table>			MBZ												
		MBZ														
	23	<b>End of Thread Group</b>														
	This bit indicates that this dispatch is the last for the current thread group.															
	22	<b>Force Destination</b>														
	Project: <table border="1" style="width: 100%;"><tr><td style="width: 50%;"></td><td style="width: 50%;">CHV, BSW</td></tr></table>			CHV, BSW												
	CHV, BSW															
If set, bits 20:17 are used to determine the destination of this dispatch, if clear the destination will be chosen based on load.																
21	<b>Use Scoreboard</b>															
	Project: <table border="1" style="width: 100%;"><tr><td style="width: 70%;"></td><td style="width: 30%;"></td></tr></table>															
	This field specifies whether the thread associated with this command uses hardware scoreboard. Only when this field is set, the scoreboard control fields in the VFE Dword are valid. If this field is cleared, the thread associated with this command bypasses hardware scoreboard.															
	<table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 30%;">Value</th> <th style="width: 70%;">Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Not using scoreboard</td> </tr> <tr> <td>1</td> <td>Using scoreboard</td> </tr> </tbody> </table>		Value	Name	0	Not using scoreboard	1	Using scoreboard								
Value	Name															
0	Not using scoreboard															
1	Using scoreboard															
20:19	<b>Slice Destination Select</b>															
This bit along with the Tslice destination select determines the slice that this thread must be sent to. Ignored if <b>Force Destination</b> = 0, or if product only has 1 slice.																
<table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 70%;">Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Slice 0</td> <td></td> </tr> <tr> <td>01b</td> <td>Slice 1</td> <td>Cannot be used in products without a Slice 1.</td> </tr> <tr> <td>10b</td> <td>Slice 2</td> <td>Cannot be used in products without a Slice 2.</td> </tr> <tr> <td>11b</td> <td>Reserved</td> <td></td> </tr> </tbody> </table>		Value	Name	Description	00b	Slice 0		01b	Slice 1	Cannot be used in products without a Slice 1.	10b	Slice 2	Cannot be used in products without a Slice 2.	11b	Reserved	
Value	Name	Description														
00b	Slice 0															
01b	Slice 1	Cannot be used in products without a Slice 1.														
10b	Slice 2	Cannot be used in products without a Slice 2.														
11b	Reserved															

<b>MEDIA_OBJECT_GRPID</b>																			
	18:17	<p><b>SubSlice Destination Select</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This field selects the SubSlice that this thread must be sent to. Ignored if <b>Force Destination</b> = 0</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 25%;">Value</th> <th style="width: 40%;">Name</th> <th style="width: 35%;">Project</th> </tr> </thead> <tbody> <tr> <td>11b</td> <td>Reserved</td> <td>CHV, BSW</td> </tr> <tr> <td>10b</td> <td>SubSlice 2</td> <td></td> </tr> <tr> <td>01b</td> <td>SubSlice 1</td> <td></td> </tr> <tr> <td>00b</td> <td>SubSlice 0</td> <td></td> </tr> </tbody> </table>	Project:	CHV, BSW	Value	Name	Project	11b	Reserved	CHV, BSW	10b	SubSlice 2		01b	SubSlice 1		00b	SubSlice 0	
	Project:	CHV, BSW																	
Value	Name	Project																	
11b	Reserved	CHV, BSW																	
10b	SubSlice 2																		
01b	SubSlice 1																		
00b	SubSlice 0																		
	16:0	<p><b>Indirect Data Length</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>U17 In bytes</td> </tr> </table> <p>This field provides the length in bytes of the indirect data. A value zero indicates that indirect data fetching is disabled - subsequently, the Indirect Data Start Address field is ignored. This field must have the same alignment as the Indirect Object Data Start Address. It must be DQWord (32-byte) aligned. As the indirect data are sent directly to URB, range is limited to 496 DW. When both inline and indirect data are fetched for this command, the total size in 8-DW registers must be less than 112 (with both inline data length and indirect data length rounded up to 8-DW aligned).</p>	Format:	U17 In bytes															
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3	31:0	<p><b>Indirect Data Start Address</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>GraphicsAddress[31:0]</td> </tr> </table> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 80%;">Description</th> <th style="width: 20%;">Project</th> </tr> </thead> <tbody> <tr> <td>This field specifies the Graphics Memory starting address of the data to be loaded into the kernel for processing. This pointer is relative to the <b>Indirect Object Base Address</b>. Hardware ignores this field if indirect data is not present. Alignment of this address depends on the mode of operation.</td> <td></td> </tr> <tr> <td>It is the 64-byte aligned address of the indirect data.</td> <td>CHV, BSW</td> </tr> </tbody> </table> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 30%;">Value</th> <th style="width: 30%;">Name</th> <th style="width: 40%;">Description</th> </tr> </thead> <tbody> <tr> <td>[0-512MB]</td> <td></td> <td>Bits 31:29 MBZ</td> </tr> </tbody> </table>	Format:	GraphicsAddress[31:0]	Description	Project	This field specifies the Graphics Memory starting address of the data to be loaded into the kernel for processing. This pointer is relative to the <b>Indirect Object Base Address</b> . Hardware ignores this field if indirect data is not present. Alignment of this address depends on the mode of operation.		It is the 64-byte aligned address of the indirect data.	CHV, BSW	Value	Name	Description	[0-512MB]		Bits 31:29 MBZ			
Format:	GraphicsAddress[31:0]																		
Description	Project																		
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Value	Name	Description																	
[0-512MB]		Bits 31:29 MBZ																	
4	31:25	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ															
	Format:	MBZ																	
	24:16	<p><b>Scoreboard Y</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td></td> </tr> <tr> <td>Format:</td> <td>U9</td> </tr> </table> <p>This field provides the Y term of the scoreboard value of the current thread.</p>	Project:		Format:	U9													
Project:																			
Format:	U9																		
15:9	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ																
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<b>MEDIA_OBJECT_GRPID</b>						
	8:0	<p><b>Scoreboard X</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Project:</td> <td></td> </tr> <tr> <td>Format:</td> <td>U9</td> </tr> </table> <p>This field provides the X term of the scoreboard value of the current thread.</p>	Project:		Format:	U9
Project:						
Format:	U9					
5	31:20	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Project:</td> <td></td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:		Format:	MBZ
	Project:					
	Format:	MBZ				
	19:16	<p><b>Scoreboard Color</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Project:</td> <td></td> </tr> <tr> <td>Format:</td> <td>U4</td> </tr> </table> <p>This field specifies which dependency color the current thread belongs to. It affects the dependency scoreboard control.</p>	Project:		Format:	U4
	Project:					
Format:	U4					
15:8	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ			
Format:	MBZ					
7:0	<p><b>Scoreboard Mask</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Project:</td> <td></td> </tr> <tr> <td>Format:</td> <td>Boolean</td> </tr> </table> <p>Each bit indicates the corresponding dependency scoreboard is dependent on. This field is AND'd with the corresponding Scoreboard Mask field in the MEDIA_VFE_STATE command. <b>Bit n (for n = 0...7):</b> Scoreboard n is dependent, where bit 0 maps to n = 0.</p>	Project:		Format:	Boolean	
Project:						
Format:	Boolean					
6	31:0	<p><b>GroupID</b></p> <p>A unique identifying number which describes the threads which share a barrier and/or SLM. Reuse of numbers is allowed as long as the old group is not currently running.</p>				
7..n	31:0	<p><b>Inline Data</b></p> <p>The format of this data is specified by software. Hardware does not interpret this data; it merely passes it to the kernel for processing. The total size for the inline data and indirect data must not exceed 112 registers.</p>				

## MEDIA\_OBJECT\_PRT

MEDIA_OBJECT_PRT			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
<p>command is for generating Persistent Root Thread for the media pipeline. It only supports loading of inline data but not indirect data. This command should be used for a root thread that might have to be present in the system for a period longer than the certain minimal context-switch interrupt latency. It has to honor the context interrupt signal to terminate upon request. It should also handle replay from the interrupted point upon context restore (the same thread being dispatched more than once). In contrary, if a thread is not a Persistent Root Thread, if dispatched, it must run to completion. The command can be used in all VFE modes, except VLD mode.</p> <p>For simplification, _PRT command has a fixed size of 16 DWORD</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h Media
		Format:	OpCode
	26:24	<b>Media Command Opcode</b>	
		Default Value:	1h MEDIA_OBJECT_PRT
		Format:	OpCode
	23:16	<b>SubOpcode</b>	
Default Value:		2h MEDIA_OBJECT_PRT SubOp	
Format:		OpCode	
15:0	<b>DWord Length</b>	Project:	CHV, BSW
		Format:	=n Total Length - 2
		Note: Regardless of the mode, inline data must be present in this command. The command size must fit within 16 dwords.	
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0Eh	DWORD_COUNT_n <b>[Default]</b>	Excludes DWord (0,1)
1	31:6	<b>Reserved</b>	
		Format:	MBZ



<b>MEDIA_OBJECT_PRT</b>										
	5:0	<p><b>Interface Descriptor Offset</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U6</td> </tr> </table> <p>This field specifies the offset from the interface descriptor base pointer to the interface descriptor which will be applied to this object. It is specified in units of interface descriptors.</p>	Project:	CHV, BSW	Format:	U6				
	Project:	CHV, BSW								
Format:	U6									
2	31	<p><b>Children Present</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>Enable</td> </tr> </table> <p>Indicates that the root thread may send spawn messages to spawn child threads and/or synchronized root threads. If Children Present is not set, TS signals VFE to dereference the URB handle immediately after it receives acknowledgement from TD that the thread is dispatched. If Children Present is set, the URB handle is forwarded to the root thread and serves as the return URB handle for the root thread. TS does not signal dereference at the time of dispatch. TS signals URB handle dereference only when it receives a resource dereference message from the thread. In order avoid deadlock, such de-reference must be issued once and only once for each URB handle.</p>	Format:	Enable						
	Format:	Enable								
	30:24	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ						
	Format:	MBZ								
	23	<p><b>PRT_Fence Needed</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field specifies that a PRT_Fence is generated after dispatching the thread associated with this MEDIA_OBJECT_PRT. The PRT_Fence prevents additional threads following this persistent root thread until a thread spawn message is sent. The PRT_Fence is generated on first dispatch of the persistent root, as well as on re-dispatches of the persistent root after context restore.</p>	Format:	Enable						
Format:	Enable									
22	<p><b>PRT_FenceType</b></p> <p>This field specifies the type of fence the PRT thread uses. If this field is set to 0, the fence is set at the end of the root thread queue. It will block the dispatch of the next root thread, but allowed these root threads to be populated through VFE to the root thread queue in TS. If this field is set to 1, the fence is set at the entry of VFE, similar to the fence set by the MEDIA_STATE_FLUSH command. No more command can go into the media pipe until a thread spawn message is sent (by the PRT). This field is only valid when PRT_Fence Needed is set to 1. Otherwise, it is ignored by hardware.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Root thread queue</td> <td>Root thread queue fence</td> </tr> <tr> <td>1h</td> <td>VFE state flush</td> <td>VFE state flush fence</td> </tr> </tbody> </table>	Value	Name	Description	0h	Root thread queue	Root thread queue fence	1h	VFE state flush	VFE state flush fence
Value	Name	Description								
0h	Root thread queue	Root thread queue fence								
1h	VFE state flush	VFE state flush fence								
21:0	<b>Reserved</b>									
3	31:0	<b>Reserved</b>								
4..15	31:0	<p><b>Inline Data</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>U32</td> </tr> </table>	Format:	U32						
Format:	U32									

## MEDIA\_OBJECT\_WALKER

<b>MEDIA_OBJECT_WALKER</b>			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h Media
		Format:	OpCode
	26:24	<b>Media Command Opcode</b>	
		Default Value:	1h MEDIA_OBJECT_WALKER
		Format:	OpCode
	23:16	<b>SubOpcode</b>	
Default Value:		03h MEDIA_OBJECT_WALKER SubOp	
Format:		OpCode	
15:0	<b>DWord Length</b>		
	Default Value:	0Fh DWORD_COUNT_n	
	Format:	=n Total Length - 2	
	<p><b>Note:</b> If this field is greater than 15, it indicates that inline data is present. If present, inline data is common for all threads generated from this command, If this field is 15, it indicates that inline data is not present. It should be noted that unlike other media object command, inline data is optional for this command.</p>		
1	31:8	<b>Reserved</b>	
	7:6	<b>Reserved</b>	
		Format:	Reserved
5:0	<b>Interface Descriptor Offset</b>		
	Project:	CHV, BSW	
	Format:	U6	
	<p>This field specifies the offset from the interface descriptor base pointer to the interface descriptor which will be applied to this object. It is specified in units of interface descriptors.</p>		
2	31	<b>Children Present</b>	
Format:		Boolean	

<b>MEDIA_OBJECT_WALKER</b>							
	<p>Indicates that the root thread may send spawn messages to spawn child threads and/or synchronized root threads. If Children Present is not set, TS signals VFE to dereference the URB handle immediately after it receives acknowledgement from TD that the thread is dispatched. If Children Present is set, the URB handle is forwarded to the root thread and serves as the return URB handle for the root thread. TS does not signal deference at the time of dispatch. TS signals URB handle deference only when it receives a resource dereference message from the thread. <i>In order avoid deadlock, such dereference must be issued once and only once for each URB handle.</i></p>						
30:25	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ				
Format:	MBZ						
24	<p><b>Thread Synchronization</b> This field when set indicates that the dispatch of the thread originated from this command is based on the "spawn root thread" message.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>No thread synchronization</td> </tr> <tr> <td>1</td> <td>Thread dispatch is synchronized by the 'spawn root thread' message</td> </tr> </tbody> </table>	Value	Name	0	No thread synchronization	1	Thread dispatch is synchronized by the 'spawn root thread' message
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23:22	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ				
Format:	MBZ						
21	<p><b>Use Scoreboard</b> This field specifies whether the thread associated with this command uses hardware scoreboard. Only when this field is set, the scoreboard control fields in the VFE Dword are valid. If this field is cleared, the thread associated with this command bypasses hardware scoreboard.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Not using scoreboard</td> </tr> <tr> <td>1</td> <td>Using scoreboard</td> </tr> </tbody> </table>	Value	Name	0	Not using scoreboard	1	Using scoreboard
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1	Using scoreboard						
20:17	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ				
Format:	MBZ						
16:0	<p><b>Indirect Data Length</b></p> <table border="1"> <tr> <td>Format:</td> <td>U17 in bytes</td> </tr> </table> <p>This field provides the length in bytes of the indirect data. A value zero indicates that indirect data fetching is disabled - subsequently, the Indirect Data Start Address field is ignored. This field must have the same alignment as the Indirect Object Data Start Address. It must be DQWord (32-byte) aligned. As the indirect data are sent directly to URB, range is limited to 496 DW. When both inline and indirect data are fetched for this command, the total size in 8-DW registers must be less than or equal to 63 (with both inline data length and indirect data length rounded up to 8-DW aligned).</p>	Format:	U17 in bytes				
Format:	U17 in bytes						
3	<p>31:0 <b>Indirect Data Start Address</b></p> <table border="1"> <tr> <td>Format:</td> <td>IndirectObjectOffset[31:0]</td> </tr> </table>	Format:	IndirectObjectOffset[31:0]				
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<b>MEDIA_OBJECT_WALKER</b>																									
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5	31:8	<p><b>Group ID Loop Select</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td style="text-align: center;">CHV, BSW</td> </tr> </table> <p>This bit field chooses which of the nested loops of the walker are used to identify threads which share a group id and therefore a shared barrier and SLM. The programmer must ensure that each group will fit into a single subslice. When barriers are enabled every group must have the same number of threads matching the number specified in the Interface Descriptor.</p> <table border="1" style="width: 100%; margin-top: 10px;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td></td> <td>Groups are not created, barriers and SLM are not allocated</td> </tr> <tr> <td style="text-align: center;">1</td> <td></td> <td>Each complete iteration of the Color loop defines a group, the group id is the concatenation of the Outer global, Inner global, Outer local, Mid local and Inner local loop execution counts.</td> </tr> <tr> <td style="text-align: center;">2</td> <td></td> <td>Each complete iteration of the Inner local loop and Color loop defines a group, the group id is the concatenation of the Outer global loop to the Mid local loop execution counts.</td> </tr> <tr> <td style="text-align: center;">3</td> <td></td> <td>Each complete iteration of the Mid local loop and lower loops defines a group, the group id is the concatenation of the Outer global loop to the Outer local loop execution counts.</td> </tr> <tr> <td style="text-align: center;">4</td> <td></td> <td>Each complete iteration of the Outer local loop and lower loops defines a group, the group id is the concatenation of the Outer global loop and the Inner global loop execution counts.</td> </tr> <tr> <td style="text-align: center;">5</td> <td></td> <td>Each complete iteration of the Inner global loop and lower loops defines a group, the group id is the Outer global loop execution count.</td> </tr> </tbody> </table>	Project:	CHV, BSW	Value	Name	Description	0		Groups are not created, barriers and SLM are not allocated	1		Each complete iteration of the Color loop defines a group, the group id is the concatenation of the Outer global, Inner global, Outer local, Mid local and Inner local loop execution counts.	2		Each complete iteration of the Inner local loop and Color loop defines a group, the group id is the concatenation of the Outer global loop to the Mid local loop execution counts.	3		Each complete iteration of the Mid local loop and lower loops defines a group, the group id is the concatenation of the Outer global loop to the Outer local loop execution counts.	4		Each complete iteration of the Outer local loop and lower loops defines a group, the group id is the concatenation of the Outer global loop and the Inner global loop execution counts.	5		Each complete iteration of the Inner global loop and lower loops defines a group, the group id is the Outer global loop execution count.
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	7:0	<p><b>Scoreboard Mask</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td style="text-align: center;">Boolean</td> </tr> </table> <p>Each bit indicates the corresponding dependency scoreboard is dependent on. This field is AND'd with the corresponding Scoreboard Mask field in the MEDIA_VFE_STATE. All threads generated by this walker command share the same dynamic mask. <b>Bit n (for n = 0...7):</b> Scoreboard n is dependent, where bit 0 maps to n = 0.</p>	Format:	Boolean																					
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<b>MEDIA_OBJECT_WALKER</b>		
6	31:29	<b>Reserved</b> Project: CHV, BSW
	28	<b>Reserved</b> Format: MBZ
	27:24	<b>Color Count Minus One</b> Format: U4 This field specifies the number of repeat of the inner most loop of the walker. Each repeated walk position is assigned with an incremental Color number. The Color number together with the X and Y position of the thread is used for dependency scoreboard control. <b>Usage Example:</b> This allows multiple sets of dependency threads to be dispatched.
	23:21	<b>Reserved</b> Format: MBZ
	20:16	<b>Middle Loop Extra Steps</b> Format: U5
	15:14	<b>Reserved</b> Format: MBZ
	13:12	<b>Local Mid-Loop Unit Y</b> Format: S1
	11:10	<b>Reserved</b> Format: MBZ
	9:8	<b>Mid-Loop Unit X</b> Format: S1
	7:0	<b>Reserved</b> Format: MBZ
7	31:26	<b>Reserved</b> Format: MBZ
	25:16	<b>Global Loop Exec Count</b> Format: U10
	15:10	<b>Reserved</b> Format: MBZ
	9:0	<b>Local Loop Exec Count</b> Format: U10
8	31:25	<b>Reserved</b> Format: MBZ
	24:16	<b>Block Resolution Y</b> Format: U9

<b>MEDIA_OBJECT_WALKER</b>				
		Vertical resolution of the local loop.		
	15:9	<b>Reserved</b> Format: <table border="1" style="width: 100%;"><tr><td style="width: 80%;"></td><td style="width: 20%;">MBZ</td></tr></table>		MBZ
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		MBZ		
	24:16	<b>Local Start Y</b> Format: <table border="1" style="width: 100%;"><tr><td style="width: 80%;"></td><td style="width: 20%;">U9</td></tr></table> Starting vertical position of the local loop.		U9
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10	31:25	<b>Reserved</b> Format: <table border="1" style="width: 100%;"><tr><td style="width: 80%;"></td><td style="width: 20%;">MBZ</td></tr></table>		MBZ
		MBZ		
	24:16	Project: <table border="1" style="width: 100%;"><tr><td style="width: 80%;"></td><td style="width: 20%;">CHV, BSW</td></tr></table>		CHV, BSW
			CHV, BSW	
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	MBZ			
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		MBZ		
	25:16	<b>Local Outer Loop Stride Y</b> Format: <table border="1" style="width: 100%;"><tr><td style="width: 80%;"></td><td style="width: 20%;">S9</td></tr></table> Vertical stride of the local outer loop, in 2's complement.		S9
	S9			
15:10	<b>Reserved</b> Format: <table border="1" style="width: 100%;"><tr><td style="width: 80%;"></td><td style="width: 20%;">MBZ</td></tr></table>		MBZ	
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<b>MEDIA_OBJECT_WALKER</b>				
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	25:16	<p><b>Local Inner Loop Unit Y</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">S9</td> </tr> </table> <p>Vertical stride of the local inner loop, in 2's complement.</p>	Format:	S9
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<b>MEDIA_OBJECT_WALKER</b>				
		Starting horizontal location of the global loop, in 2's complement.		
15	31:26	<b>Reserved</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td> </td><td>MBZ</td></tr></table>		MBZ
		MBZ		
	25:16	<b>Global Outer Loop Stride Y</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td> </td><td>S9</td></tr></table> Vertical stride of the global outer loop, in 2's complement.		S9
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15:10	<b>Reserved</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td> </td><td>MBZ</td></tr></table>		MBZ	
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	S9			
16	31:26	<b>Reserved</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td> </td><td>MBZ</td></tr></table>		MBZ
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	S9			
17..n	31:0	<b>Inline Data</b>		



## MEDIA\_STATE\_FLUSH

<b>MEDIA_STATE_FLUSH</b>				
Project:	CHV, BSW			
Source:	RenderCS			
Length Bias:	2			
<p>This command updates the Message Gateway state. In particular, it updates the state for a selected Interface Descriptor. This command can be considered same as a MI_Flush except that only media parser will get flushed instead of the entire 3D/media render pipeline. The command should be programmed prior to new Media state, curbe and/or interface descriptor commands when switching to a new context or programming new state for the same context. With this command, pipelined state change is allowed for the media pipe. It should be cautious when using this command when child_present flag in the media state is enabled. This is because that CURBE state as well as Interface Descriptor state are shared between root threads and child threads. Changing these states while child threads are generated on the fly may cause unexpected behavior. Combining with MI_ARB_ON/OFF command, it is possible to support interruptability with the following command sequence where interrupt may be allowed only when MI_ARB_ON_OFF is ON: MEDIA_STATE_FLUSH VFE_STATE // VFE will hold CS if watermark isn't met MI_ARB_OFF // There must be at least one VFE command before this one MEDIA_OBJECT .... MI_ARB_ON</p>				
DWord	Bit	Description		
0	31:29	<b>Command Type</b>		
		Default Value:	3h GFXPIPE	
		Format:	OpCode	
	28:27	<b>Pipeline</b>		
		Default Value:	2h Media	
		Format:	OpCode	
	26:24	<b>Media Command Opcode</b>		
		Default Value:	0h MEDIA_STATE_FLUSH	
		Format:	OpCode	
	23:16	<b>SubOpcode</b>		
		Default Value:	4h MEDIA_STATE_FLUSH SubOp	
		Format:	OpCode	
	15:0	<b>DWord Length</b>	Project:	All
			Format:	=n Total Length - 2
<b>Value</b>		<b>Name</b>	<b>Description</b>	
0h		DWORD_COUNT_n [Default]	Excludes DWord (0,1)	
1	31:9	<b>Reserved</b>		
		Project:	All	

<b>MEDIA_STATE_FLUSH</b>		
	Format:	MBZ
8	<b>Reserved</b>	
	Project:	N, CHV, BSW
7	<b>Flush to GO</b>	
	Project:	CHV, BSW
	Format:	Enable
	This bit indicates that the write data out of this thread group should be flushed to the point where it is visible to following commands.	
	<b>Workaround</b>	<b>Project</b>
	Use PIPE_CONTROL with CS stall and DC flush bits set, in place of MEDIA_STATE_FLUSH with Flush-to-GO set, to work around a preemption boundary condition.	CHV, BSW*:A0
6	<b>Watermark Required</b>	
	Project:	All
	This is a single bit specifying if the MEDIA_STATE_FLUSH should stall further commands until there is enough room in a half-slice for the following thread group. The characteristics of the thread group are specified in the Interface Descriptor Offset. If set, the MEDIA_STATE_FLUSH stalls CS until there are enough threads in a half-slice, and enough SLM available in the same half-slice, and a free barrier if one is required. An Interface Descriptors can be updated after a Watermarked MEDIA_STATE_FLUSH only if it has not been used in the current context. Reusing an interface descriptor requires that this bit is clear to ensure the ID cache is reloaded. If clear, the MEDIA_STATE_FLUSH stalls CS until the TDL has dispatched the last thread, allowing the CURBE and Interface Descriptors to be updated by following commands.	
	<b>Programming Notes</b>	<b>Project</b>
	The Interface Descriptor Offset used for the flush must be the same as that used for the GPGPU_OBJECTs. GPGPU_WALKER automatically checks the Watermark conditions before starting a thread, so this bit should not be set before GPGPU_WALKER.	CHV, BSW
	If pre-emption is used, the WatermarkRequired bit must not be set.	CHV, BSW*:A0
5:0	<b>Interface Descriptor Offset</b>	
	Format:	U6
	This field specifies the offset from the interface descriptor base pointer to the interface descriptor which describes what resources are required to meet the watermark.	

## MEDIA\_VFE\_STATE

<b>MEDIA_VFE_STATE</b>								
Project:	CHV, BSW							
Source:	RenderCS							
Length Bias:	2							
<p>A stalling PIPE_CONTROL is required before MEDIA_VFE_STATE unless the only bits that are changed are scoreboard related: Scoreboard Enable, Scoreboard Type, Scoreboard Mask, Scoreboard * Delta. For these scoreboard related states, a MEDIA_STATE_FLUSH is sufficient.</p> <ul style="list-style-type: none"> <li>MEDIA_STATE_FLUSH (optional, only if barrier dependency is needed)</li> <li>MEDIA_INTERFACE_DESCRIPTOR_LOAD (optional)</li> </ul>								
DWord	Bit	Description						
0	31:29	<b>Command Type</b>						
		Default Value:	3h GFXPIPE					
		Format:	OpCode					
	28:27	<b>Pipeline</b>						
		Default Value:	2h Media					
		Format:	OpCode					
	26:24	<b>Media Command Opcode</b>						
		Default Value:	0h MEDIA_VFE_STATE					
		Format:	OpCode					
	23:16	<b>SubOpcode</b>						
Default Value:		0h MEDIA_VFE_STATE SubOp						
Format:		OpCode						
15:0	<b>DWord Length</b>	Format:	=n Total Length - 2					
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>07h</td> <td>DWORD_COUNT_n [Default]</td> <td>Excludes DWord (0,1)</td> </tr> </tbody> </table>		Value	Name	Description	07h	DWORD_COUNT_n [Default]
	Value	Name	Description					
	07h	DWORD_COUNT_n [Default]	Excludes DWord (0,1)					
1	31:10	<b>Scratch Space Base Pointer</b>						
		Format:	GeneralStateOffset[31:10]					
	Specifies the 1k-byte aligned address offset to scratch space for use by the kernel. This pointer is relative to the <b>General State Base Address</b> .							
9:8	<b>Reserved</b>	Format:	MBZ					
	7:4	<b>Stack Size</b>						

<b>MEDIA_VFE_STATE</b>											
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[0,11]</td> <td></td> <td>indicating [1KBytes, 2MBytes]</td> </tr> </tbody> </table>	Value	Name	Description	[0,11]		indicating [1KBytes, 2MBytes]			
Value	Name	Description									
[0,11]		indicating [1KBytes, 2MBytes]									
		<b>Programming Notes</b>									
		Since the stack uses the upper portion of the scratch space, <b>Stack Size = &lt; Per Thread Scratch Space</b>									
	3:0	<b>Per Thread Scratch Space</b>									
		Format:	U4								
		Specifies the amount of scratch space allowed to be used by each thread. The driver must allocate enough contiguous scratch space, pointed to by the Scratch Space Pointer, to ensure that the maximum threads in the device each get Per Thread Scratch Space size without exceeding the driver-allocated scratch space.									
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>[0,11]</td> <td></td> <td>indicating [1k bytes, 2 Mbytes]: 0 -&gt; 1k, 1-&gt;2k, 2-&gt;4k, 3-&gt;8k ... 11-&gt;2M</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Value	Name	Description	Project	[0,11]		indicating [1k bytes, 2 Mbytes]: 0 -> 1k, 1->2k, 2->4k, 3->8k ... 11->2M	CHV, BSW	
Value	Name	Description	Project								
[0,11]		indicating [1k bytes, 2 Mbytes]: 0 -> 1k, 1->2k, 2->4k, 3->8k ... 11->2M	CHV, BSW								
2	31:16	<b>Reserved</b>									
		Format:	MBZ								
	15:0	<b>Scratch Space Base Pointer High</b>									
		Format:	GeneralStateOffset[47:32]								
		This field specifies the high 16 bits of starting address of the Scratch Space Base Pointer									
3	31:16	<b>Maximum Number of Threads</b>									
		Format:	U16-1 representing thread count								
		Range: [0, n-1] where n = (# EUs) * (# threads/EU). See <i>Graphics Processing Engine</i> for listing of #EUs and #threads in each device.									
		Specifies the maximum number of simultaneous root threads allowed to be active. Used to avoid potential deadlock. If child threads are not planning on being used then this field can be set to its maximum value and there will be no thread limit beyond what is currently available in the system; the maximum value can include threads in slices that have been shut down for power reasons. For GPGPU threads the maximum value must be used.									
		<b>Programming Notes</b>									
		MSB will be zero due to the range limit below.									
	15:8	<b>Number of URB Entries</b>									
		Format:	U8								
		Specifies the number of URB entries that are used by the unit.									
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>[1,64]</td> <td></td> <td>[1,64] Entries</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Value	Name	Description	Project	[1,64]		[1,64] Entries	CHV, BSW	
Value	Name	Description	Project								
[1,64]		[1,64] Entries	CHV, BSW								

<b>MEDIA_VFE_STATE</b>																
		<b>Programming Notes</b>														
		Please note that 0 is not allowed for this field.														
	7	<p><b>Reset Gateway Timer</b> This field controls the reset of the timestamp counter maintained in Message Gateway.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Maintaining the existing timestamp state</td> </tr> <tr> <td>1h</td> <td>Resetting relative timer and latching the global timestamp</td> </tr> </tbody> </table>	Value	Name	0h	Maintaining the existing timestamp state	1h	Resetting relative timer and latching the global timestamp								
Value	Name															
0h	Maintaining the existing timestamp state															
1h	Resetting relative timer and latching the global timestamp															
	6	<p><b>Bypass Gateway Control</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This field configures Gateway to use a simple message protocol.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Maintaining OpenGateway/ForwardMsg/CloseGateway protocol (legacy mode)</td> </tr> <tr> <td>1h</td> <td>Bypassing OpenGateway/CloseGateway protocol</td> </tr> </tbody> </table>	Project:	CHV, BSW	Value	Name	0h	Maintaining OpenGateway/ForwardMsg/CloseGateway protocol (legacy mode)	1h	Bypassing OpenGateway/CloseGateway protocol						
Project:	CHV, BSW															
Value	Name															
0h	Maintaining OpenGateway/ForwardMsg/CloseGateway protocol (legacy mode)															
1h	Bypassing OpenGateway/CloseGateway protocol															
	5:3	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ										
Project:	CHV, BSW															
Format:	MBZ															
	2	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ												
Format:	MBZ															
	1:0	<b>Reserved</b>														
4	31:8	<b>Reserved</b>														
	7:4	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ												
	Format:	MBZ														
	3:2	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ										
Project:	CHV, BSW															
Format:	MBZ															
1:0	<p><b>Slice Disable</b> This field disables dispatch to slices and subslices for Media and GPGPU applications. It is used to limit the amount of scratch space that needs to be allocated for a context. If a particular configuration doesn't have slice or subslice then there is no impact to disabling it.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td></td> <td>All subslices are enabled.</td> </tr> <tr> <td>01b</td> <td></td> <td>Slice 2 and 1 are disabled, only Slice 0 with all subslices is enabled.</td> </tr> <tr> <td>10b</td> <td></td> <td>Reserved</td> </tr> <tr> <td>11b</td> <td></td> <td>Slice 2 and 1 are disabled, only Slice 0 with only subslice 0 enabled.</td> </tr> </tbody> </table>	Value	Name	Description	00b		All subslices are enabled.	01b		Slice 2 and 1 are disabled, only Slice 0 with all subslices is enabled.	10b		Reserved	11b		Slice 2 and 1 are disabled, only Slice 0 with only subslice 0 enabled.
Value	Name	Description														
00b		All subslices are enabled.														
01b		Slice 2 and 1 are disabled, only Slice 0 with all subslices is enabled.														
10b		Reserved														
11b		Slice 2 and 1 are disabled, only Slice 0 with only subslice 0 enabled.														
5	31:16	<p><b>URB Entry Allocation Size</b></p> <table border="1"> <tr> <td>Format:</td> <td>U16</td> </tr> </table>	Format:	U16												
Format:	U16															

<b>MEDIA_VFE_STATE</b>									
	<p>Specifies the length of each URB entry used by the unit, in 256-bit register increments. ROB address for URB starts after CURBE Allocated region. (URB Entry Allocation Size * Number of URB Entries) + CURBE Allocation Size + Number of Interface Descriptors) must be &lt;= (number of bytes allocated for the URB in L3CNTLREG / 32 bytes per entry). Note: Number of Interface Descriptors is 64.</p> <p>If SLM is enabled for GPGPU work then the number of available entries will be 1/2 the maximum URB entries.</p> <p style="text-align: center;"><b>Programming Notes</b></p> <p>When Inline data is used with MEDIA_OBJECT or MEDIA_OBJECT_WALKER, then the URB entry allocation size must match the Inline data size. If Indirect data is being used with MEDIA_OBJECT or GPGPU_WALKER then the allocation size must be sufficient for the Indirect data. If both Inline and Indirect are being used, then the allocation size must match the sum of the Inline and Indirect.</p>								
15:0	<p><b>CURBE Allocation Size</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>U16</td> </tr> </table> <p>Specifies the total length allocated for CURBE, in 256-bit register increments. ROB address for CURBE starts at address 64. (URB Entry Allocation Size * Number of URB Entries) + CURBE Allocation Size + Interface Descriptor Entries) must be less than or equal to the number of entries in the URB as described in <b>Configurations</b>. Interface Descriptor Entries is 64</p> <p>If SLM is enabled for GPGPU work then the number of available entries will be ½ the maximum URB entries.</p> <p style="text-align: center;"><b>Programming Notes</b></p> <p>CURBE Allocation Size should be 0 for GPGPU workloads that uses indirect instead of CURBE.</p>	Format:	U16						
Format:	U16								
6	<p>31 <b>Scoreboard Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td></td> </tr> </table> <p>This field enables and disables the hardware scoreboard in the Media Pipeline. If this field is cleared, hardware ignores the following scoreboard state fields.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Scoreboard disabled</td> </tr> <tr> <td>1h</td> <td>Scoreboard enabled</td> </tr> </tbody> </table>	Project:		Value	Name	0h	Scoreboard disabled	1h	Scoreboard enabled
Project:									
Value	Name								
0h	Scoreboard disabled								
1h	Scoreboard enabled								
	<p>30 <b>Scoreboard Type</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td></td> </tr> </table> <p>This field selects the type of scoreboard in use.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Stalling Scoreboard</td> </tr> <tr> <td>1h</td> <td>Non-Stalling Scoreboard</td> </tr> </tbody> </table>	Project:		Value	Name	0h	Stalling Scoreboard	1h	Non-Stalling Scoreboard
Project:									
Value	Name								
0h	Stalling Scoreboard								
1h	Non-Stalling Scoreboard								
29:16	<b>Reserved</b>								

<b>MEDIA_VFE_STATE</b>					
	15:8	<b>Reserved</b>			
		<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:
Project:	CHV, BSW				
Format:	MBZ				
	7:0	<b>Scoreboard Mask</b>			
		<table border="1"> <tr> <td>Project:</td> <td></td> </tr> <tr> <td>Format:</td> <td>Enable[8]</td> </tr> </table> <p>Each bit indicates the corresponding dependency scoreboard is enabled. The scoreboard is based on the relative (X, Y) distance from the current threads' (X, Y) position. <b>Bit n (for n = 0...7):</b> Score n is enabled.</p>	Project:		Format:
Project:					
Format:	Enable[8]				
7	31:28	<b>Scoreboard 3 Delta Y</b>			
		<table border="1"> <tr> <td>Project:</td> <td></td> </tr> <tr> <td>Format:</td> <td>S3</td> </tr> </table> <p>Relative vertical distance of the dependent instance assigned to scoreboard 3, in the form of 2's compliment.</p> <p style="text-align: center;"><b>Programming Notes</b></p> <p>MBZ if scoreboard is disabled.</p>	Project:		Format:
	Project:				
	Format:	S3			
	27:24	<b>Scoreboard 3 Delta X</b>			
<table border="1"> <tr> <td>Project:</td> <td></td> </tr> <tr> <td>Format:</td> <td>S3</td> </tr> </table> <p>Relative horizontal distance of the dependent instance assigned to scoreboard 3, in the form of 2's compliment.</p> <p style="text-align: center;"><b>Programming Notes</b></p> <p>MBZ if scoreboard is disabled.</p>		Project:		Format:	S3
Project:					
Format:	S3				
23:20	<b>Scoreboard 2 Delta Y</b>				
	<table border="1"> <tr> <td>Project:</td> <td></td> </tr> <tr> <td>Format:</td> <td>S3</td> </tr> </table> <p>Relative vertical distance of the dependent instance assigned to scoreboard 2, in the form of 2's compliment.</p> <p style="text-align: center;"><b>Programming Notes</b></p> <p>MBZ if scoreboard is disabled.</p>	Project:		Format:	S3
Project:					
Format:	S3				
19:16	<b>Scoreboard 2 Delta X</b>				
	<table border="1"> <tr> <td>Project:</td> <td></td> </tr> <tr> <td>Format:</td> <td>S3</td> </tr> </table> <p>Relative horizontal distance of the dependent instance assigned to scoreboard 2, in the form of 2's compliment.</p> <p style="text-align: center;"><b>Programming Notes</b></p> <p>MBZ if scoreboard is disabled.</p>	Project:		Format:	S3
Project:					
Format:	S3				

<b>MEDIA_VFE_STATE</b>													
	<table border="1"> <tr> <td>15:12</td> <td><b>Scoreboard 1 Delta Y</b></td> </tr> <tr> <td>Project:</td> <td></td> </tr> <tr> <td>Format:</td> <td>S3</td> </tr> <tr> <td colspan="2">Relative vertical distance of the dependent instance assigned to scoreboard 1, in the form of 2's compliment.</td> </tr> <tr> <td colspan="2" style="text-align: center;"><b>Programming Notes</b></td> </tr> <tr> <td colspan="2">MBZ if scoreboard is disabled.</td> </tr> </table>	15:12	<b>Scoreboard 1 Delta Y</b>	Project:		Format:	S3	Relative vertical distance of the dependent instance assigned to scoreboard 1, in the form of 2's compliment.		<b>Programming Notes</b>		MBZ if scoreboard is disabled.	
	15:12	<b>Scoreboard 1 Delta Y</b>											
	Project:												
	Format:	S3											
Relative vertical distance of the dependent instance assigned to scoreboard 1, in the form of 2's compliment.													
<b>Programming Notes</b>													
MBZ if scoreboard is disabled.													
<table border="1"> <tr> <td>11:8</td> <td><b>Scoreboard 1 Delta X</b></td> </tr> <tr> <td>Project:</td> <td></td> </tr> <tr> <td>Format:</td> <td>S3</td> </tr> <tr> <td colspan="2">Relative horizontal distance of the dependent instance assigned to scoreboard 1, in the form of 2's compliment.</td> </tr> <tr> <td colspan="2" style="text-align: center;"><b>Programming Notes</b></td> </tr> <tr> <td colspan="2">MBZ if scoreboard is disabled.</td> </tr> </table>	11:8	<b>Scoreboard 1 Delta X</b>	Project:		Format:	S3	Relative horizontal distance of the dependent instance assigned to scoreboard 1, in the form of 2's compliment.		<b>Programming Notes</b>		MBZ if scoreboard is disabled.		
11:8	<b>Scoreboard 1 Delta X</b>												
Project:													
Format:	S3												
Relative horizontal distance of the dependent instance assigned to scoreboard 1, in the form of 2's compliment.													
<b>Programming Notes</b>													
MBZ if scoreboard is disabled.													
<table border="1"> <tr> <td>7:4</td> <td><b>Scoreboard 0 Delta Y</b></td> </tr> <tr> <td>Project:</td> <td></td> </tr> <tr> <td>Format:</td> <td>S3</td> </tr> <tr> <td colspan="2">Relative vertical distance of the dependent instance assigned to scoreboard 0, in the form of 2's compliment.</td> </tr> <tr> <td colspan="2" style="text-align: center;"><b>Programming Notes</b></td> </tr> <tr> <td colspan="2">MBZ if scoreboard is disabled.</td> </tr> </table>	7:4	<b>Scoreboard 0 Delta Y</b>	Project:		Format:	S3	Relative vertical distance of the dependent instance assigned to scoreboard 0, in the form of 2's compliment.		<b>Programming Notes</b>		MBZ if scoreboard is disabled.		
7:4	<b>Scoreboard 0 Delta Y</b>												
Project:													
Format:	S3												
Relative vertical distance of the dependent instance assigned to scoreboard 0, in the form of 2's compliment.													
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<table border="1"> <tr> <td>3:0</td> <td><b>Scoreboard 0 Delta X</b></td> </tr> <tr> <td>Project:</td> <td></td> </tr> <tr> <td>Format:</td> <td>S3</td> </tr> <tr> <td colspan="2">Relative horizontal distance of the dependent instance assigned to scoreboard 0, in the form of 2's compliment.</td> </tr> <tr> <td colspan="2" style="text-align: center;"><b>Programming Notes</b></td> </tr> <tr> <td colspan="2">MBZ if scoreboard is disabled.</td> </tr> </table>	3:0	<b>Scoreboard 0 Delta X</b>	Project:		Format:	S3	Relative horizontal distance of the dependent instance assigned to scoreboard 0, in the form of 2's compliment.		<b>Programming Notes</b>		MBZ if scoreboard is disabled.		
3:0	<b>Scoreboard 0 Delta X</b>												
Project:													
Format:	S3												
Relative horizontal distance of the dependent instance assigned to scoreboard 0, in the form of 2's compliment.													
<b>Programming Notes</b>													
MBZ if scoreboard is disabled.													
8	<table border="1"> <tr> <td>31:28</td> <td><b>Scoreboard 7 Delta Y</b></td> </tr> <tr> <td>Project:</td> <td></td> </tr> <tr> <td>Format:</td> <td>S3</td> </tr> <tr> <td colspan="2">Relative vertical distance of the dependent instance assigned to scoreboard 7, in the form of 2's compliment.</td> </tr> <tr> <td colspan="2" style="text-align: center;"><b>Programming Notes</b></td> </tr> <tr> <td colspan="2">MBZ if scoreboard is disabled.</td> </tr> </table>	31:28	<b>Scoreboard 7 Delta Y</b>	Project:		Format:	S3	Relative vertical distance of the dependent instance assigned to scoreboard 7, in the form of 2's compliment.		<b>Programming Notes</b>		MBZ if scoreboard is disabled.	
	31:28	<b>Scoreboard 7 Delta Y</b>											
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27:24	<b>Scoreboard 7 Delta X</b>												
Project:													
Format:	S3												



<b>MEDIA_VFE_STATE</b>									
	<p>Relative horizontal distance of the dependent instance assigned to scoreboard 7, in the form of 2's compliment.</p> <table border="1" style="width: 100%; text-align: center;"> <tr> <td colspan="2"><b>Programming Notes</b></td> </tr> <tr> <td colspan="2">MBZ if scoreboard is disabled.</td> </tr> </table>	<b>Programming Notes</b>		MBZ if scoreboard is disabled.					
<b>Programming Notes</b>									
MBZ if scoreboard is disabled.									
23:20	<p><b>Scoreboard 6 Delta Y</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Project:</td> <td></td> </tr> <tr> <td>Format:</td> <td>S3</td> </tr> </table> <p>Relative vertical distance of the dependent instance assigned to scoreboard 6, in the form of 2's compliment.</p> <table border="1" style="width: 100%; text-align: center;"> <tr> <td colspan="2"><b>Programming Notes</b></td> </tr> <tr> <td colspan="2">MBZ if scoreboard is disabled.</td> </tr> </table>	Project:		Format:	S3	<b>Programming Notes</b>		MBZ if scoreboard is disabled.	
Project:									
Format:	S3								
<b>Programming Notes</b>									
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19:16	<p><b>Scoreboard 6 Delta X</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Project:</td> <td></td> </tr> <tr> <td>Format:</td> <td>S3</td> </tr> </table> <p>Relative horizontal distance of the dependent instance assigned to scoreboard 6, in the form of 2's compliment.</p> <table border="1" style="width: 100%; text-align: center;"> <tr> <td colspan="2"><b>Programming Notes</b></td> </tr> <tr> <td colspan="2">MBZ if scoreboard is disabled.</td> </tr> </table>	Project:		Format:	S3	<b>Programming Notes</b>		MBZ if scoreboard is disabled.	
Project:									
Format:	S3								
<b>Programming Notes</b>									
MBZ if scoreboard is disabled.									
15:12	<p><b>Scoreboard 5 Delta Y</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Project:</td> <td></td> </tr> <tr> <td>Format:</td> <td>S3</td> </tr> </table> <p>Relative vertical distance of the dependent instance assigned to scoreboard 5, in the form of 2's compliment.</p> <table border="1" style="width: 100%; text-align: center;"> <tr> <td colspan="2"><b>Programming Notes</b></td> </tr> <tr> <td colspan="2">MBZ if scoreboard is disabled.</td> </tr> </table>	Project:		Format:	S3	<b>Programming Notes</b>		MBZ if scoreboard is disabled.	
Project:									
Format:	S3								
<b>Programming Notes</b>									
MBZ if scoreboard is disabled.									
11:8	<p><b>Scoreboard 5 Delta X</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Project:</td> <td></td> </tr> <tr> <td>Format:</td> <td>S3</td> </tr> </table> <p>Relative horizontal distance of the dependent instance assigned to scoreboard 5, in the form of 2's compliment.</p> <table border="1" style="width: 100%; text-align: center;"> <tr> <td colspan="2"><b>Programming Notes</b></td> </tr> <tr> <td colspan="2">MBZ if scoreboard is disabled.</td> </tr> </table>	Project:		Format:	S3	<b>Programming Notes</b>		MBZ if scoreboard is disabled.	
Project:									
Format:	S3								
<b>Programming Notes</b>									
MBZ if scoreboard is disabled.									
7:4	<p><b>Scoreboard 4 Delta Y</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Project:</td> <td></td> </tr> <tr> <td>Format:</td> <td>S3</td> </tr> </table> <p>Relative vertical distance of the dependent instance assigned to scoreboard 4, in the form of 2's compliment.</p>	Project:		Format:	S3				
Project:									
Format:	S3								

<b>MEDIA_VFE_STATE</b>													
	<table border="1"> <tr> <th colspan="2" style="text-align: center;">Programming Notes</th> </tr> <tr> <td colspan="2">MBZ if scoreboard is disabled.</td> </tr> </table>	Programming Notes		MBZ if scoreboard is disabled.									
Programming Notes													
MBZ if scoreboard is disabled.													
3:0	<table border="1"> <tr> <th colspan="2"><b>Scoreboard 4 Delta X</b></th> </tr> <tr> <td>Project:</td> <td></td> </tr> <tr> <td>Format:</td> <td>S3</td> </tr> <tr> <td colspan="2">Relative horizontal distance of the dependent instance assigned to scoreboard 4, in the form of 2's compliment.</td> </tr> <tr> <th colspan="2" style="text-align: center;">Programming Notes</th> </tr> <tr> <td colspan="2">MBZ if scoreboard is disabled.</td> </tr> </table>	<b>Scoreboard 4 Delta X</b>		Project:		Format:	S3	Relative horizontal distance of the dependent instance assigned to scoreboard 4, in the form of 2's compliment.		Programming Notes		MBZ if scoreboard is disabled.	
<b>Scoreboard 4 Delta X</b>													
Project:													
Format:	S3												
Relative horizontal distance of the dependent instance assigned to scoreboard 4, in the form of 2's compliment.													
Programming Notes													
MBZ if scoreboard is disabled.													

## Media Block Read MSD

<b>MSD1R_MB - Media Block Read MSD</b>			
Project:	CHV, BSW		
Source:	DataPort 1		
Length Bias:	1		
Family:	Other		
Group:	Media Block R/W		
DWord	Bit	Description	
0	19	<b>Header Present</b>	
		Project: All	
		Format: MDC_MHR [CHV, BSW]	
		Indicates that the message requires a header.	
		<b>Message Type</b>	
18:14		Default Value: 04h	
		Project: All	
		Format: Opcode	
		Media Block Read message	
13:11		<b>Reserved</b>	
		Project: All	
		Format: MBZ	
Ignored			
10:8		<b>Vertical Line Stride Override</b>	
		Project: All	
		Format: MDC_VLSO [CHV, BSW]	
If enabled, specifies the Vertical Line Stride and Vertical Line Stride Offset override fields.			
7:0		<b>Binding Table Index</b>	
		Project: All	
		Format: MDC_BTS [CHV, BSW]	
Specifies the Binding Table Index for the message			

## Media Block Write MSD

<b>MSD1W_MB - Media Block Write MSD</b>									
Project:	CHV, BSW								
Source:	DataPort 1								
Length Bias:	1								
Family:	Other								
Group:	Media Block R/W								
DWord	Bit	Description							
0	19	<b>Header Present</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_MHR [CHV, BSW]</td> </tr> </table> <p>Indicates that the message requires a header.</p>	Project:	All	Format:	MDC_MHR [CHV, BSW]			
		Project:	All						
		Format:	MDC_MHR [CHV, BSW]						
		18:14	<b>Message Type</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Default Value:</td> <td>0Ah</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Media Block Write message</p>	Default Value:	0Ah	Project:	All	Format:	Opcode
			Default Value:	0Ah					
Project:	All								
Format:	Opcode								
13:11	<b>Reserved</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>Ignored</p>	Project:	All	Format:	MBZ				
	Project:	All							
	Format:	MBZ							
10:8	<b>Vertical Line Stride Override</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_VLSO [CHV, BSW]</td> </tr> </table> <p>If enabled, specifies the Vertical Line Stride and Vertical Line Stride Offset override fields.</p>	Project:	All	Format:	MDC_VLSO [CHV, BSW]				
	Project:	All							
	Format:	MDC_VLSO [CHV, BSW]							
7:0	<b>Binding Table Index</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_BTS [CHV, BSW]</td> </tr> </table> <p>Specifies the Binding Table Index for the message</p>	Project:	All	Format:	MDC_BTS [CHV, BSW]				
	Project:	All							
	Format:	MDC_BTS [CHV, BSW]							

## Media Transpose Read MSD

<b>MSD1R_TT - Media Transpose Read MSD</b>							
Project:	CHV, BSW						
Source:	DataPort 1						
Length Bias:	1						
Family:	Other						
Group:	Transpose Read						
DWord	Bit	Description					
0	19	<p><b>Header Present</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_MHR [CHV, BSW]</td> </tr> </table> <p>Indicates that the message requires a header.</p>	Project:	All	Format:	MDC_MHR [CHV, BSW]	
	Project:	All					
	Format:	MDC_MHR [CHV, BSW]					
	18:14	<p><b>Message Type</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Transpose Read message</p>	Default Value:	00h	Project:	All	Format:
Default Value:	00h						
Project:	All						
Format:	Opcode						
13:8	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>Ignored</p>	Project:	All	Format:	MBZ		
Project:	All						
Format:	MBZ						
7:0	<p><b>Binding Table Index</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_BTS [CHV, BSW]</td> </tr> </table> <p>Specifies the Binding Table Index for the message</p>	Project:	All	Format:	MDC_BTS [CHV, BSW]		
Project:	All						
Format:	MDC_BTS [CHV, BSW]						

## Memory Fence MSD

<b>MSD_MEMFENCE - Memory Fence MSD</b>		
Project:	CHV, BSW	
Source:	DataPort 0	
Length Bias:	1	
Family:	Other	
Group:	Memory Fence	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHP [CHV, BSW]
	Indicates that the message requires a header.	
	18	<b>Legacy Message</b>
Default Value: 0h		
Project: All		
Format: Opcode		
Legacy Message		
17:14	<b>Message Type</b>	
	Default Value: 07h	
	Project: All	
	Format: Opcode	
Memory Fence message		
13	<b>Commit</b>	
	Project: All	
	Format: Enable	
Specifies whether control is returned to the thread only after the fence has been honored.		
12:9	<b>L3 Flush</b>	
	The L3 Flush control is one of the following GSYNC signals.	
	<b>Value</b>	<b>Name</b>
	<b>Description</b>	
	0h	Disabled <b>[Default]</b>
<b>Programming Notes</b>		
If multiple caches need to be flushed, the commands need to be sent separately.		
8	<b>Reserved</b>	
7:0	<b>Reserved</b>	

## MFC\_AVC\_PAK\_OBJECT

<b>MFC_AVC_PAK_OBJECT</b>			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>The MFC_AVC_PAK_OBJECT command is the second primitive command for the AVC Encoding Pipeline. The same command is used for both CABAC and CAVLC modes. The MV Data portion of the bitstream is loaded as indirect data object. Before issuing a MFC_AVC_PAK_OBJECT command, all AVC MFX states need to be valid. Therefore the commands used to set these states need to have been issued prior to the issue of this command. MB record must be consecutive with no gaps, hence we do not need MB(x,y) in each MB command. Internal counter will keep track of the current MB address, starting from the Start_MB_In_Slice loaded at the beginning of each slice. MFC_AVC_PAK_OBJECT command follows the MbType definition like MFD. Many fields in this command are identical to that in VME output. This is intended to reduce software converting overhead from VME to PAK. Encoding statistical data such as the total size of the output bitstream are provided through MMIO registers. Software may access these registers through MI_STORE_REGISTER_MEM command.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h MFC_AVC_PAK_OBJECT
		Format:	OpCode
	26:24	<b>Media Command Opcode</b>	
		Default Value:	1h AVC_ENC
		Format:	OpCode
	23:21	<b>SubOpcode A</b>	
		Default Value:	2h
		Format:	OpCode
	20:16	<b>SubOpcode B</b>	
		Default Value:	9h
Format:		OpCode	
15:12	<b>Reserved</b>		
	Format:	MBZ	
11:0	<b>DWord Length</b>	Format:	=n Length -2
	<b>Value</b>	<b>Name</b>	<b>Project</b>
	000Ah	DWORD_COUNT_n [Default]	CHV, BSW

<b>MFC_AVC_PAK_OBJECT</b>					
1	31:10	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">MBZ</td> </tr> </table>	Format:	MBZ	
	Format:	MBZ			
9:0	<p><b>Indirect PAK-MV Data Length</b></p> <p>This field provides the length in bytes of the indirect data, which contains all the MVs for the current MB (in any partitioning and subpartitioning form). A value zero indicates that indirect data fetching is disabled - subsequently, the Indirect PAK-MV Data Start Address field is ignored. This field must have the same alignment as the Indirect PAK-MV Data Start Address. This field must be DW aligned (since each MV is 4 bytes in size). Driver has to derived this field from MVsize (MVquantity in DXVA, exact size) *4 bytes per MV.</p>				
2	31:29	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">MBZ</td> </tr> </table>	Format:	MBZ	
	Format:	MBZ			
28:0	<p><b>Indirect PAK-MV Data Start Address Offset</b></p> <p>This field specifies the memory starting address (offset) of the MV data to be fetched into PAK Subsystem for processing. This pointer is relative to the MFC Indirect PAK-MV Object Base Address. Hardware ignores this field if indirect data is not present, i.e. the Indirect PAK-MV Data Length is set to 0. It is a Dword aligned address in all AVC encoding configuration, since each MV is 4 bytes in size.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 60%;">Value</th> <th style="width: 40%;">Name</th> </tr> </thead> <tbody> <tr> <td>[0,512MB)</td> <td></td> </tr> </tbody> </table>	Value	Name	[0,512MB)	
Value	Name				
[0,512MB)					
3..10	31:0	<p><b>Inline Data</b></p> <p>All the required MB level controls and parameters for encoding are captured as inline data of the MFC_AVC_PAK_OBJECT command. It has a fixed size of 8 DWs. Its definition is described in the next section.</p>			



## MFC\_JPEG\_HUFF\_TABLE\_STATE

MFC_JPEG_HUFF_TABLE_STATE			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>This Huffman table commands contains both DC and AC tables for either luma or chroma. Once a Huffman table has been defined for a particular destination, it replaces the previous tables stored in that destination and shall be used in the remaining Scans of the current image. Two Huffman tables for luma and chroma will be sent to H/W, and chroma table is used for both U and V.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h MFC_JPEG_HUFF_TABLE_STATE
		Format:	OpCode
	26:24	<b>Media Command Opcode</b>	
		Default Value:	7h JPEG
		Format:	OpCode
	23:21	<b>SubOpcode A</b>	
Default Value:		2h Common	
Format:		OpCode	
20:16	<b>SubOpcode B</b>		
	Default Value:	3h MEDIA_	
	Format:	OpCode	
15:12	<b>Reserved</b>		
	Format:	MBZ	
11:0	<b>DWord Length</b>		
	Default Value:	0AEh Excludes DWord (0,1)	
	Format:	=n Total Length - 2	
1	31:1	<b>Reserved</b>	
		Format:	MBZ
	0	<b>Huff Table ID</b>	
		Format:	U1
<p>Huffman table destination identifier will specify one of two destinations at the encoder into which the Huffman table must be stored.</p>			

<b>MFC_JPEG_HUFF_TABLE_STATE</b>											
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 20%; text-align: center;">Value</th> <th style="width: 30%; text-align: center;">Name</th> <th style="width: 50%; text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td></td> <td>Huffman table 0</td> </tr> <tr> <td style="text-align: center;">1</td> <td></td> <td>Huffman table 1</td> </tr> </tbody> </table>	Value	Name	Description	0		Huffman table 0	1		Huffman table 1
Value	Name	Description									
0		Huffman table 0									
1		Huffman table 1									
2..13	31:0	<p><b>DC_TABLE</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 10%;">Format:</td> <td>3Bytes: Byte0 for Code length, Byte1 and Byte2 for Code word, and Byte3 for dummy</td> </tr> </table> <p>12 categories with code length and code word. Each run/size has 1-byte code length, and 2-byte code word.</p>	Format:	3Bytes: Byte0 for Code length, Byte1 and Byte2 for Code word, and Byte3 for dummy							
Format:	3Bytes: Byte0 for Code length, Byte1 and Byte2 for Code word, and Byte3 for dummy										
14..175	31:0	<p><b>AC_TABLE</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 10%;">Format:</td> <td>3Bytes: Byte0 for Code length, Byte1 and Byte2 for Code word, and Byte3 for dummy</td> </tr> </table> <p>162 run/size with code length and code word. Each run/size has 1-byte code length, and 2-byte code word.</p>	Format:	3Bytes: Byte0 for Code length, Byte1 and Byte2 for Code word, and Byte3 for dummy							
Format:	3Bytes: Byte0 for Code length, Byte1 and Byte2 for Code word, and Byte3 for dummy										

## MFC\_JPEG\_SCAN\_OBJECT

<b>MFC_JPEG_SCAN_OBJECT</b>				
Project:	CHV, BSW			
Source:	VideoCS			
Length Bias:	2			
Encoder Only				
DWord	Bit	Description		
0	31:29	<b>Command Type</b>		
		Default Value:	3h PARALLEL_VIDEO_PIPE	
		Format:	OpCode	
	28:27		<b>Pipeline</b>	
			Default Value:	2h MFC_JPEG_SCAN_OBJECT
			Format:	OpCode
	26:24		<b>Media Command Opcode</b>	
			Default Value:	7h JPEG_ENC
			Format:	OpCode
	23:21		<b>SubOpcode A</b>	
Default Value:			2h	
Format:			OpCode	
20:16		<b>SubOpcode B</b>		
		Default Value:	9h	
		Format:	OpCode	
15:12		<b>Reserved</b>		
		Format:	MBZ	
11:0		<b>DWord Length</b>		
		Default Value:	001h Excludes DWord (0,1)	
		Format:	=n Total Length - 2	
1	31:26	<b>Reserved</b>		
		Format:	MBZ	
	25:0	<b>MCU Count</b>		
		Format:	U26	
<p>This field indicates the number of MCUs in the Scan. <math>MCU\ Count = M_x \times M_y</math> The number of MCUs in a row: <math>M_x = (X + (H_1 * 8 - 1)) / (H_1 * 8)</math> The number of MCUs in a column: <math>M_y = (Y + (V_1 * 8 - 1)) / (V_1 * 8)</math> X: The number of samples per line in Y-image Y: The number of lines in Y-image H1: Horizontal sampling factor of Y-image in the Frame header V1: Vertical sampling factor of Y-image in the Frame header</p>				

<b>MFC_JPEG_SCAN_OBJECT</b>																						
2	31:25	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">MBZ</td> </tr> </table>	Format:	MBZ																		
	Format:	MBZ																				
24:22	<p><b>Huffman AC Table</b></p> <p>AC Huffman table destination selector specifies one of two possible AC table destinations for each Y, U, V, or R, G, B. The AC Huffman tables must have been loaded in destination 0 and 1 by the time of issuing MFC_JPEG_HUFF_TABLE_STATE Command.</p> <p>If AC table 0 is used for Y and AC table 1 is used for U and V, it will be set to 110b. If AC table 0 is used for R, G, and B, it will be set to 000b and so on. Refer to the table below for the summary of actions.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 70%;">Description</th> </tr> </thead> <tbody> <tr> <td>0XXb</td> <td>Bit24 (V0)</td> <td>The third image component must use the AC table 0.</td> </tr> <tr> <td>1XXb</td> <td>Bit24 (V1)</td> <td>The third image component must use the AC table 1.</td> </tr> <tr> <td>X0Xb</td> <td>Bit23 (U0)</td> <td>The second image component must use the AC table 0.</td> </tr> <tr> <td>X1Xb</td> <td>Bit23 (U1)</td> <td>The second image component must use the AC table 1.</td> </tr> <tr> <td>XX0b</td> <td>Bit22 (Y0)</td> <td>The first image component must use the AC table 0.</td> </tr> <tr> <td>XX1b</td> <td>Bit22 (Y1)</td> <td>The first image component must use the AC table 1.</td> </tr> </tbody> </table> <p style="text-align: center;"><b>Restriction</b></p> <p>When InputSurfaceFormatYUV = RGB, because the order of input image components can be RGB, GBR, BGR, or YUV, <b>Bit22</b> is used for the first image component, <b>Bit23</b> is used for the second image component, and <b>Bit24</b> is used for the third image component.</p>	Value	Name	Description	0XXb	Bit24 (V0)	The third image component must use the AC table 0.	1XXb	Bit24 (V1)	The third image component must use the AC table 1.	X0Xb	Bit23 (U0)	The second image component must use the AC table 0.	X1Xb	Bit23 (U1)	The second image component must use the AC table 1.	XX0b	Bit22 (Y0)	The first image component must use the AC table 0.	XX1b	Bit22 (Y1)	The first image component must use the AC table 1.
Value	Name	Description																				
0XXb	Bit24 (V0)	The third image component must use the AC table 0.																				
1XXb	Bit24 (V1)	The third image component must use the AC table 1.																				
X0Xb	Bit23 (U0)	The second image component must use the AC table 0.																				
X1Xb	Bit23 (U1)	The second image component must use the AC table 1.																				
XX0b	Bit22 (Y0)	The first image component must use the AC table 0.																				
XX1b	Bit22 (Y1)	The first image component must use the AC table 1.																				
21	21	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">MBZ</td> </tr> </table>	Format:	MBZ																		
	Format:	MBZ																				
20:18	<p><b>Huffman DC Table</b></p> <p>DC Huffman table destination selector specifies one of two possible DC table destinations for each Y, U, V, or R, G, B. The DC Huffman tables shall have been loaded in destination 0 and 1 by the time of issuing MFC_JPEG_HUFF_TABLE_STATE Command.</p> <p>if DC table 0 is used for Y and DC table 1 is used for U and V, it will be set to 110b. If DC table 0 is used for R, G, and B, it will be set to 000b and so on. Refer to the table below for the summary of actions.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 70%;">Description</th> </tr> </thead> <tbody> <tr> <td>0XXb</td> <td>Bit20 (V0)</td> <td>The third image component must use the DC table 0.</td> </tr> <tr> <td>1XXb</td> <td>Bit20 (V1)</td> <td>The third image component must use the DC table 1.</td> </tr> <tr> <td>X0Xb</td> <td>Bit19 (U0)</td> <td>The second image component must use the DC table 0.</td> </tr> <tr> <td>X1Xb</td> <td>Bit19 (U1)</td> <td>The second image component must use the DC table 1.</td> </tr> <tr> <td>XX0b</td> <td>Bit18 (Y0)</td> <td>The first image component must use the DC table 0.</td> </tr> <tr> <td>XX1b</td> <td>Bit18 (Y1)</td> <td>The first image component must use the DC table 1.</td> </tr> </tbody> </table>	Value	Name	Description	0XXb	Bit20 (V0)	The third image component must use the DC table 0.	1XXb	Bit20 (V1)	The third image component must use the DC table 1.	X0Xb	Bit19 (U0)	The second image component must use the DC table 0.	X1Xb	Bit19 (U1)	The second image component must use the DC table 1.	XX0b	Bit18 (Y0)	The first image component must use the DC table 0.	XX1b	Bit18 (Y1)	The first image component must use the DC table 1.
Value	Name	Description																				
0XXb	Bit20 (V0)	The third image component must use the DC table 0.																				
1XXb	Bit20 (V1)	The third image component must use the DC table 1.																				
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X1Xb	Bit19 (U1)	The second image component must use the DC table 1.																				
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XX1b	Bit18 (Y1)	The first image component must use the DC table 1.																				

<b>MFC_JPEG_SCAN_OBJECT</b>											
<b>Restriction</b>											
When InputSurfaceFormatYUV = RGB, because the order of input image components can be RGB, GBR, BGR, YUV, <b>Bit18</b> is used for the first image component, <b>Bit19</b> is used for the second image component, and <b>Bit20</b> is used for the third image component.											
17	<b>Head Present Flag</b> If this flag is set to 0, then no MFC_JPEG_PAK_INSERT_OBJECT commands will be sent. If this flag is set to 1, then one or more MFC_JPEG_PAK_INSERT_OBJECT commands will be sent after MFC_JPEG_SCAN_OBJECT command.										
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 10%;">Name</th> <th style="width: 80%;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td></td> <td>No insertion into the output bitstream buffer before Scan encoded bitstream</td> </tr> <tr> <td style="text-align: center;">1</td> <td></td> <td>Headers, tables, App data insertion into the output bitstream buffer. HW will insert the insertion data before the Scan encoded bitstream.</td> </tr> </tbody> </table>			Value	Name	Description	0		No insertion into the output bitstream buffer before Scan encoded bitstream	1		Headers, tables, App data insertion into the output bitstream buffer. HW will insert the insertion data before the Scan encoded bitstream.
Value	Name	Description									
0		No insertion into the output bitstream buffer before Scan encoded bitstream									
1		Headers, tables, App data insertion into the output bitstream buffer. HW will insert the insertion data before the Scan encoded bitstream.									
16	<b>Is Last Scan</b> If this flag is set, then HW will insert EOI (0xFFD9) to the end of Scan encoded bitstream.										
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 10%;">Name</th> <th style="width: 80%;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td></td> <td>Not the last Scan.</td> </tr> <tr> <td style="text-align: center;">1</td> <td></td> <td>Indicates that the current Scan is the last one.</td> </tr> </tbody> </table>			Value	Name	Description	0		Not the last Scan.	1		Indicates that the current Scan is the last one.
Value	Name	Description									
0		Not the last Scan.									
1		Indicates that the current Scan is the last one.									
15:0	<b>Restart Interval</b> Format: <span style="float: right;">U16</span> Specifies the number of MCUs in an ECS, except for the last ECS. Restart maker is inserted periodically and it separates the two neighboring ECSs.										
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0-FFFFh</td> <td></td> </tr> </tbody> </table>			Value	Name	0-FFFFh						
Value	Name										
0-FFFFh											
<b>Programming Notes</b>											
A value of '0' implies that the Scan Data has a single ECS.											

## MFC\_MPEG2\_PAK\_OBJECT

<b>MFC_MPEG2_PAK_OBJECT</b>			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>The MFC_MPEG2_PAK_OBJECT command is the second primitive command for the MPEG-2 Encoding Pipeline. Different from AVC, the MV Data portion of the bitstream is loaded as part of MB control data. Before issuing a MFC_MPEG2_PAK_OBJECT command, all MPEG2_MFX states need to be valid. Therefore the commands used to set these states need to have been issued prior to the issue of this command. MB record must be consecutive with no gaps, hence we do not need MB(x,y) in each MB command. Internal counter will keep track of the current MB address, starting from the Start_MB_In_Slice loaded at the beginning of each slice.</p> <p>MFC_MPEG2_PAK_OBJECT command follows the MbType definition like MFD. Many fields in this command are identical to that in VME output. This is intended to reduce software converting overhead from VME to PAK. Encoding statistical data such as the total size of the output bitstream are provided through MMIO registers. Software may access these registers through MI_STORE_REGISTER_MEM command.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h MFC_AVC_PAK_INSERT_OBJECT
		Format:	OpCode
	26:24	<b>Media Command Opcode</b>	
		Default Value:	3h MPEG2
		Format:	OpCode
	23:21	<b>SubOpcode A</b>	
		Default Value:	2h ENC
		Format:	OpCode
	20:16	<b>SubOpcode B</b>	
		Default Value:	9h MEDIA_
		Format:	OpCode
	15:12	<b>Reserved</b>	
	11:0	<b>DWord Length</b>	
		Default Value:	0007h Excludes DWord (0,1)
Project:		All	
Format:		=n Total Length - 2	

## MFC\_MPEG2\_PAK\_OBJECT

1..8	31:0	<b>Inline Data</b> All the required MB level controls and parameters for encoding are captured as inline data of the MFC_MPEG2_PAK_OBJECT command. It has a fixed size of 8 DWs. Its definition is described in the next section
------	------	---

## MFC\_MPEG2\_SLICEGROUP\_STATE

MFC_MPEG2_SLICEGROUP_STATE			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>This is a slice group level command and can be issued multiple times within a picture that is comprised of multiple slice groups. The same command is used for AVC encoder (PAK mode) and decoder (VLD and IT modes).</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h MFX_MPEG2_SLICEGROUP_STATE
		Format:	OpCode
	26:24	<b>Media Command Opcode</b>	
		Default Value:	3h MPEG2
		Format:	OpCode
	23:21	<b>SubOpcode A</b>	
Default Value:		2h MEDIA_	
Format:		OpCode	
20:16	<b>SubOpcode B</b>		
	Default Value:	3h MEDIA_	
	Format:	OpCode	
15:12	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
11:0	<b>DWord Length</b>	Default Value:	6h Excludes DWord (0,1)
		Project:	All
		Format:	=n Total Length - 2
1	31	<p><b>MbRateCtrlFlag- RateControlCounterEnable (Encoder-only)</b></p> <p>To enable the accumulation of bit allocation for rate controlThis field enables hardware Rate Control logic. The rest of the RC control fields are only valid when this field is set to 1. Otherwise, hardware ignores these fields.Note: To reset MB level rate control (QRC), we need to set both bits MbRateCtrlFlag and MbRateCtrlReset to 1 in the new slice</p>	



<b>MFC_MPEG2_SLICEGROUP_STATE</b>																		
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disable</td> <td>All</td> </tr> <tr> <td>1h</td> <td>Enable</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Project	0h	Disable	All	1h	Enable	All							
Value	Name	Project																
0h	Disable	All																
1h	Enable	All																
30	<b>MbRateCtrlReset- ResetRateControlCounter (Encoder-only)</b> To reset the bit allocation accumulation counter to 0 to restart the rate control.																	
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disable</td> <td>Not reset</td> <td>All</td> </tr> <tr> <td>1h</td> <td>Enable</td> <td>reset</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	0h	Disable	Not reset	All	1h	Enable	reset	All				
Value	Name	Description	Project															
0h	Disable	Not reset	All															
1h	Enable	reset	All															
29:28	<b>MbRateCtrlMode- RC Trigggle Mode (Encoder-only)</b>																	
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td></td> <td>Always Rate Control, whereas RC becomes active if sum_act &gt; sum_target or sum_act &lt; sum_target</td> </tr> <tr> <td>01b</td> <td></td> <td>Gentle Rate Control, whereas RC becomes active if sum_act &gt; upper_midpt or sum_act &lt; lower_midpt</td> </tr> <tr> <td>10b</td> <td></td> <td>Loose Rate Control, whereas RC becomes active if sum_act &gt; sum_max or sum_act &lt; sum_min</td> </tr> <tr> <td>11b</td> <td></td> <td>Reserved</td> </tr> </tbody> </table>	Value	Name	Description	00b		Always Rate Control, whereas RC becomes active if sum_act > sum_target or sum_act < sum_target	01b		Gentle Rate Control, whereas RC becomes active if sum_act > upper_midpt or sum_act < lower_midpt	10b		Loose Rate Control, whereas RC becomes active if sum_act > sum_max or sum_act < sum_min	11b		Reserved		
Value	Name	Description																
00b		Always Rate Control, whereas RC becomes active if sum_act > sum_target or sum_act < sum_target																
01b		Gentle Rate Control, whereas RC becomes active if sum_act > upper_midpt or sum_act < lower_midpt																
10b		Loose Rate Control, whereas RC becomes active if sum_act > sum_max or sum_act < sum_min																
11b		Reserved																
27:24	<b>MbRateCtrlParam- RC Stable Tolerance (Encoder-only)</b>																	
	Format:	U4																
	This field specifies the tolerance required to deactivate RC once it has been triggered.																	
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>[0, 15]</td> <td></td> </tr> </tbody> </table>	Value	Name	[0, 15]														
Value	Name																	
[0, 15]																		
23	<b>RateCtrlPanicFlag - RC Panic Enable (Encoder-only)</b> If this field is set to 1, RC enters panic mode when sum_act > sum_max. RC Panic Type field controls what type of panic behavior is invoked.																	
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Disable</td> <td>All</td> </tr> <tr> <td>1</td> <td>Enable</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Project	0	Disable	All	1	Enable	All								
Value	Name	Project																
0	Disable	All																
1	Enable	All																
22	<b>RateCtrlPanicType - RC Panic Type (Encoder-only)</b> This field selects between two RC Panic methods. If it is set to 0, in panic mode, the macroblock QP is maxed out, setting to requested QP + QP_max_pos_mod. If it is set to 1, for an intra macroblock, AC CBPs are set to zero (note that DC CBPs are not modified). For inter macroblocks, AC and DC CBPs are forced to zero.																	
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td></td> <td>QP Panic</td> </tr> <tr> <td>1h</td> <td></td> <td>CBP Panic</td> </tr> </tbody> </table>	Value	Name	Description	0h		QP Panic	1h		CBP Panic								
Value	Name	Description																
0h		QP Panic																
1h		CBP Panic																
21	<b>Reserved</b>																	

<b>MFC_MPEG2_SLICEGROUP_STATE</b>															
20	<p><b>SkipConvDisabled - MB Type Skip Conversion Disable (Encoder-only)</b>                      This field is only valid for a P or B slice. It must be zero for other slice types. Rules are provided in Section 2.3.3.1.6</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Enable</td> <td>Enable skip type conversion</td> <td>All</td> </tr> <tr> <td>1h</td> <td>Disable</td> <td>Disable skip type conversion</td> <td>All</td> </tr> </tbody> </table>			Value	Name	Description	Project	0h	Enable	Enable skip type conversion	All	1h	Disable	Disable skip type conversion	All
Value	Name	Description	Project												
0h	Enable	Enable skip type conversion	All												
1h	Disable	Disable skip type conversion	All												
19	<p><b>IsLastSliceGrp</b>                      IsLastSliceGrp = 1 if the current slice group is the last slice group of a picture; 0 otherwise. It is used by the zero filling in the Minimum Frame Size test.</p>														
18	<p><b>BitstreamOutputFlag - Compressed BitStream Output Disable Flag (Encoder-only)</b></p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Enable</td> <td>enable the writing of the output compressed bitstream</td> </tr> <tr> <td>1h</td> <td>Disable</td> <td>disable the writing of the output compressed bitstream</td> </tr> </tbody> </table>			Value	Name	Description	0h	Enable	enable the writing of the output compressed bitstream	1h	Disable	disable the writing of the output compressed bitstream			
Value	Name	Description													
0h	Enable	enable the writing of the output compressed bitstream													
1h	Disable	disable the writing of the output compressed bitstream													
17	<p><b>HeaderPresentFlag - Header Insertion Present in Bitstream (Encoder-only)</b></p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disable</td> <td>no header insertion into the output bitstream buffer, in front of the current slice encoded bits</td> <td>All</td> </tr> <tr> <td>1h</td> <td>Enable</td> <td>header insertion into the output bitstream buffer is present, and is in front of the current slice encoded bits.</td> <td>All</td> </tr> </tbody> </table>			Value	Name	Description	Project	0h	Disable	no header insertion into the output bitstream buffer, in front of the current slice encoded bits	All	1h	Enable	header insertion into the output bitstream buffer is present, and is in front of the current slice encoded bits.	All
Value	Name	Description	Project												
0h	Disable	no header insertion into the output bitstream buffer, in front of the current slice encoded bits	All												
1h	Enable	header insertion into the output bitstream buffer is present, and is in front of the current slice encoded bits.	All												
16	<p><b>SliceData PresentFlag - SliceData Insertion Present in Bitstream (Encoder-only)</b></p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disable</td> <td>no Slice Data insertion into the output bitstream buffer</td> <td>All</td> </tr> <tr> <td>1h</td> <td>Enable</td> <td>Slice Data insertion into the output bitstream buffer is present.</td> <td>All</td> </tr> </tbody> </table>			Value	Name	Description	Project	0h	Disable	no Slice Data insertion into the output bitstream buffer	All	1h	Enable	Slice Data insertion into the output bitstream buffer is present.	All
Value	Name	Description	Project												
0h	Disable	no Slice Data insertion into the output bitstream buffer	All												
1h	Enable	Slice Data insertion into the output bitstream buffer is present.	All												
15	<p><b>TailPresentFlag - Tail Insertion Present in bitstream (Encoder-only)</b></p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td></td> <td>no tail insertion into the output bitstream buffer, after the current slice encoded bits</td> </tr> <tr> <td>1h</td> <td></td> <td>tail insertion into the output bitstream buffer is present, and is after the current slice encoded bits.</td> </tr> </tbody> </table>			Value	Name	Description	0h		no tail insertion into the output bitstream buffer, after the current slice encoded bits	1h		tail insertion into the output bitstream buffer is present, and is after the current slice encoded bits.			
Value	Name	Description													
0h		no tail insertion into the output bitstream buffer, after the current slice encoded bits													
1h		tail insertion into the output bitstream buffer is present, and is after the current slice encoded bits.													
14	<p><b>FirstSliceHdrDisabled</b>                      when this is on, the first slice header of the slice group is expected to be provided by the user via insertion command. PAK HW will skip it.</p>														
13	<p><b>IntraSlice</b>                      intra slice value included in slice headers, when IntraSliceFlag = 1.</p>														
12	<p><b>IntraSliceFlag</b>                      intra slice flag included in slice headers</p>														
11:8	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ for SliceID extension</td> </tr> </table>			Format:	MBZ for SliceID extension										
Format:	MBZ for SliceID extension														

<b>MFC_MPEG2_SLICEGROUP_STATE</b>		
	7:4	<b>SliceID[3:0] (Encoder-only)</b> To identify the output data (coding information record) returned for rate control from PAK to ENC and VPP
	3:2	<b>Reserved</b> Format: MBZ for StreamID extension
	1:0	<b>StreamID[1:0] (Encoder-only)</b> To identify the output data (coding information record) returned for rate control from PAK to ENC and VPP
2	31:24	<b>NextSgMbYcnt - also NextStartVertPos</b> Vertical count of the first MB in the next slice group (Encoder-only)Note: This field restricts total number of MB in the Y direction to 255 or less.
	23:16	<b>NextSgMbXcnt - also NextStartHorzPos</b> BitFieldDesc
	15:8	<b>FirstMbYcnt - also CurrStartVertPos</b> Project: All Format: U8 also CurrStartVertPos, Vertical count of the first MB in the current slice group (Encoder-only)
	7:0	<b>FirstMbXcnt - also CurrStartHorzPos</b> Project: All Format: U8 Horizontal count of the first MB in the current slice group (Encoder-only)
	31:9	<b>Reserved</b> Format: MBZ
3	8	<b>SliceGroupSkip</b> Project: All Exists If: //Encoder Only Format: U1 All macroblocks are skipped
	7:6	<b>Reserved</b> Format: MBZ
	5:0	<b>SliceGroupQp</b> Project: All Exists If: //Encoder Only Format: U6 Initial slice quality parameter

<b>MFC_MPEG2_SLICEGROUP_STATE</b>						
4	31:29	<b>Reserved</b> Format: MBZ				
	28:0	<b>BitstreamOffset - Indirect PAK-BSE Data Start Address (Write)</b> Exists If: //Encoder Only This field specifies the memory starting address (offset) to write out the compressed bitstream data from the BSE processing. This pointer is relative to the MFC Indirect PAK-BSE Object Base Address. It is a byte-aligned address for the AVC bitstream data in both CABAC/CAVLC Modes. For Write, there is no need to have a data length field. It is assumed the global memory bound check specified in the IND_OBJ_BASE_ADDRESS command (Indirect PAK-BSE Object Access Upper Bound) will take care of any illegal write access. This field is only valid for AVC encode mode. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>[0, 512MB)</td> <td></td> </tr> </tbody> </table>	Value	Name	[0, 512MB)	
Value	Name					
[0, 512MB)						
5	31:24	<b>MaxQpNegModifier - Magnitude of QP Max Negative Modifier (Encoder-only)</b> Format: U8 This field specifies the lower limit of the QP modifier. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>[0, 51]</td> <td></td> </tr> </tbody> </table>	Value	Name	[0, 51]	
	Value	Name				
	[0, 51]					
	23:16	<b>MaxQpPosModifier - Magnitude of QP Max Positive Modifier (Encoder-only)</b> Format: U8 This field specifies the upper limit of the QP modifier. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>[0, 51]</td> <td></td> </tr> </tbody> </table>	Value	Name	[0, 51]	
	Value	Name				
	[0, 51]					
	15:12	<b>ShrinkParam - Shrink Resistance (Encoder-only)</b> Format: U4 This field specifies the additional points added each time decreased correction is invoked. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>[0, 15]</td> <td></td> </tr> </tbody> </table>	Value	Name	[0, 15]	
	Value	Name				
	[0, 15]					
	11:8	<b>Shrinkaram - Shrink Init (Encoder-only)</b> Format: U4 This field specifies the initial points required to trip decreased control. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>[0, 15]</td> <td></td> </tr> </tbody> </table>	Value	Name	[0, 15]	
	Value	Name				
	[0, 15]					
7:4	<b>GrowParam - Grow Resistance (Encoder-only)</b> Format: U4 This field specifies the additional points added each time increased correction is invoked. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>[0, 15]</td> <td></td> </tr> </tbody> </table>	Value	Name	[0, 15]		
Value	Name					
[0, 15]						

<b>MFC_MPEG2_SLICEGROUP_STATE</b>						
	3:0	<b>GrowParam - Grow Init (Encoder-only)</b>				
	Format: U4 This field specifies the initial points required to trip increased control.					
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>[0, 15]</td> <td></td> </tr> </tbody> </table>	Value	Name	[0, 15]	
Value	Name					
[0, 15]						
6	31:24	<b>Reserved</b>				
	Format: MBZ					
	23:20	<b>CorrectPoints - Correct 6 (Encoder-only)</b>				
	Format: U4					
	This field specifies the points used in the lowermost RC region when $sum\_act \leq sum\_min$ .					
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>[0, 15]</td> <td></td> </tr> </tbody> </table>		Value	Name	[0, 15]	
	Value	Name				
	[0, 15]					
	19:16	<b>CorrectPoints - Correct 5 (Encoder-only)</b>				
	Format: U4					
This field specifies the points used in the fifth RC region when $sum\_act > sum\_min$ but $\leq lower\_midpt$ .						
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>[0, 15]</td> <td></td> </tr> </tbody> </table>		Value	Name	[0, 15]		
Value	Name					
[0, 15]						
15:12	<b>CorrectPoints - Correct 4 (Encoder-only)</b>					
Format: U4						
This field specifies the points used in the fourth RC region when $sum\_act > lower\_midpt$ but $\leq sum\_target$ .						
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>[0, 15]</td> <td></td> </tr> </tbody> </table>		Value	Name	[0, 15]		
Value	Name					
[0, 15]						
11:8	<b>CorrectPoints - Correct 3 (Encoder-only)</b>					
Format: U4						
This field specifies the points used in the third RC region when $sum\_act > sum\_target$ but $\leq upper\_midpt$ .						
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>[0, 15]</td> <td></td> </tr> </tbody> </table>		Value	Name	[0, 15]		
Value	Name					
[0, 15]						
7:4	<b>CorrectPoints - Correct 2 (Encoder-only)</b>					
Format: U4						
This field specifies the points used in the second RC region when $sum\_act > upper\_midpt$ but $\leq sum\_max$ .						
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>[0, 15]</td> <td></td> </tr> </tbody> </table>		Value	Name	[0, 15]		
Value	Name					
[0, 15]						
3:0	<b>CorrectPoints - Correct 1 (Encoder-only)</b>					
Format: U4						

		<b>MFC_MPEG2_SLICEGROUP_STATE</b>	
		This field specifies the points used in the topmost RC region when sum_act > sum_max	
		<b>Value</b>	<b>Name</b>
		[0, 15]	
7	31:28	<b>CV7 - Clamp Value 7 (Encoder-only)</b>	
		Exists If:	//Encoder Only
	27:24	<b>CV6 - Clamp Value 6 (Encoder-only)</b>	
		Project:	All
		Exists If:	//Encoder Only
		Format:	U4
	23:20	<b>CV5 - Clamp Value 5 (Encoder-only)</b>	
		Project:	All
		Exists If:	//Encoder Only
		Format:	U4
19:16	<b>CV4 - Clamp Value 4 (Encoder-only)</b>		
	Project:	All	
	Exists If:	//Encoder Only	
	Format:	U4	
15:12	<b>CV3 - Clamp Value 3 (Encoder-only)</b>		
	Project:	All	
	Exists If:	//Encoder Only	
	Format:	U4	
11:8	<b>CV2 - Clamp Value 2 (Encoder-only)</b>		
	Project:	All	
	Exists If:	//Encoder Only	
	Format:	U4	
7:4	<b>CV1 - Clamp Value 1 (Encoder-only)</b>		
	Project:	All	
	Exists If:	//Encoder Only	
	Format:	U4	
3:0	<b>CV0 - Clamp Value 0 (Encoder-only)</b>		
	<p>If the magnitude of coefficients at locations assigned with CV0 (mapping shown below) exceeds 2CV0-1, they are replaced with 2CV0-1. For coefficients at locations marked as 'none', no clamping is performed. The following mappings are only applied to luma and chroma blocks\subblocks containing AC coefficients (blocks\subblocks with only DC coeffs will not be clamped).</p> <p>For 8x8 frame block, each coefficient is mapped to one of the eight CV values as following:</p>		
	none	none	CV7 CV6 CV5 CV4 CV3 CV3

### MFC\_MPEG2\_SLICEGROUP\_STATE

none	CV7	CV6	CV5	CV4	CV3	CV3	CV2
CV7	CV6	CV5	CV4	CV3	CV3	CV2	CV2
CV6	CV5	CV4	CV3	CV3	CV2	CV2	CV1
CV5	CV4	CV3	CV3	CV2	CV2	CV1	CV1
CV4	CV3	CV3	CV2	CV2	CV1	CV1	CV0
CV3	CV3	CV2	CV2	CV1	CV1	CV0	CV0
CV3	CV2	CV2	CV1	CV1	CV0	CV0	CV0

For 8x8 field block, each coefficient is mapped to one of the eight CV values as following:

none	none	CV6	CV5	CV4	CV3	CV2	CV1
none	CV7	CV6	CV5	CV4	CV3	CV2	CV1
CV7	CV6	CV5	CV4	CV3	CV3	CV2	CV1
CV7	CV6	CV5	CV4	CV3	CV2	CV2	CV1
CV6	CV5	CV4	CV4	CV3	CV2	CV1	CV0
CV6	CV5	CV4	CV3	CV2	CV2	CV1	CV0
CV5	CV5	CV4	CV3	CV2	CV1	CV1	CV0
CV5	CV5	CV4	CV3	CV2	CV1	CV1	CV0

## MFD\_AVC\_BSD\_OBJECT

MFD_AVC_BSD_OBJECT			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
Description			
<p>The MFD_AVC_BSD_OBJECT command is the only primitive command for the AVC Decoding Pipeline. The same command is used for both CABAC and CAVLD modes. The Slice Data portion of the bitstream is loaded as indirect data object. Before issuing a MFD_AVC_BSD_OBJECT command, all AVC states of the MFD Engine need to be valid. Therefore the commands used to set these states need to have been issued prior to the issue of a MFD_AVC_BSD_OBJECT command.</p>			
Context switch interrupt is not supported by this command.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h MFD_AVC_BSD_OBJECT
		Format:	OpCode
	26:24	<b>Media Command Opcode</b>	
		Default Value:	1h AVC_DEC
		Format:	OpCode
	23:21	<b>SubOpcode A</b>	
		Default Value:	1h
		Format:	OpCode
	20:16	<b>SubOpcode B</b>	
		Default Value:	8h
Format:		OpCode	
15:12	<b>Reserved</b>		
	Format:	MBZ	
11:0	<b>DWord Length</b>	Format:	=n Total Length - 2
	<b>Value</b>	<b>Name</b>	<b>Project</b>
	4h	Excludes DWord (0,1) = 0004 <b>[Default]</b>	CHV, BSW



<b>MFD_AVC_BSD_OBJECT</b>									
1	31:0	<p><b>Indirect BSD Data Length</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>U32</td> </tr> </table> <p>This field provides the length in bytes of the indirect data. A value zero indicates that indirect data fetching is disabled - subsequently, the Indirect Data Start Address field is ignored. This field must have the same alignment as the Indirect Object Data Start Address. AVC Short Format : It is the length in bytes of the bitstream data for the current slice, including Slice Header + Slice Data + Emulation Prevention Bytes + any filling trailing zeros after the last MB. Hardware ignores the contents after the last non-zero byte. Trailing zero is allowed and handled correctly in both CABAC and CAVLC modes.</p>	Format:	U32					
Format:	U32								
2	31:29	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ					
	Format:	MBZ							
28:0	<p><b>Indirect BSD Data Start Address</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 40%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U29</td> </tr> </table> <p>This field specifies the Graphics Memory starting address of the data to be fetched into BSD Unit for processing. This pointer is relative to the <b>MFD Indirect Object Base Address</b>. Hardware ignores this field if indirect data is not present. It is a byte-aligned address for the AVC bitstream data in both CABAC/CAVLD Modes. In implementing a phantom slice at the end of a picture for automatic error concealment, this field should set to 0. It includes the NAL Header (the NAL Header does not need to perform EMU detection). For AVC, it is a single byte. But for MVC, the NAL Header is 4 Bytes long. These NAL Header Unit must be passed to HW in the compressed bitstream buffer.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 60%; text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>[0,512MB)</td> <td></td> </tr> </tbody> </table>	Project:	CHV, BSW	Format:	U29	Value	Name	[0,512MB)	
Project:	CHV, BSW								
Format:	U29								
Value	Name								
[0,512MB)									
3..5	31:0	<p><b>Inline Data</b></p> <p>All the required Slice Header parameters and error handling settings are captured as InLine Data of the AVC_BSD_OBJECT command. It has a fixed size of 4 DWs. Its definition is described in the following section: Inline Data Description [CHV, BSW].</p>							

## MFD\_AVC\_DPB\_STATE

MFD_AVC_DPB_STATE						
Project:	CHV, BSW					
Source:	VideoCS					
Length Bias:	2					
<p>This is a frame level state command used only in DXVA2 AVC Short Slice Bitstream Format VLD mode. RefFrameList[16] of DXVA2 interface is replaced with intel Reference Picture Addresses[16] of MFX_PIPE_BUF_ADDR_STATE command. The LongTerm Picture flag indicator of all reference pictures are collected into LongTermPic_Flag[16]. FieldOrderCntList[16][2] and CurrFieldOrderCnt[2] of DXVA2 interface are replaced with intel POCList[34] of MFX_AVC_DIRECTMODE_STATE command.</p>						
DWord	Bit	Description				
0	31:29	<b>Command Type</b>				
		Default Value: 3h PARALLEL_VIDEO_PIPE Format: OpCode				
	28:27	<b>Pipeline</b>				
		Default Value: 2h MFX_MULTI_DW Format: OpCode				
	26:24	<b>Media Command Opcode</b>				
		Default Value: 1h AVC_DEC Format: OpCode				
	23:21	<b>SubOpcode A</b>				
		Default Value: 1h Format: OpCode				
20:16	<b>SubOpcode B</b>					
	Default Value: 6h Format: OpCode					
15:12	<b>Reserved</b>					
	Format: MBZ					
11:0	<b>DWord Length</b>					
	Format: =n Total Length - 2					
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>9h</td> <td>Excludes DWord (0,1) <b>[Default]</b></td> <td>CHV, BSW</td> </tr> </tbody> </table>	Value	Name	Project	9h	Excludes DWord (0,1) <b>[Default]</b>
Value	Name	Project				
9h	Excludes DWord (0,1) <b>[Default]</b>	CHV, BSW				

<b>MFD_AVC_DPB_STATE</b>																	
1	31:16	<p><b>LongTermFrame_Flag[16][1 bit]</b> One-to-one correspondence with the entries of the Intel RefFrameList[16]. 1 bit per reference frame.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">1</td> <td>the picture is a long term reference picture</td> </tr> <tr> <td style="text-align: center;">0</td> <td>the picture is a short term reference picture</td> </tr> </tbody> </table>	Value	Name	1	the picture is a long term reference picture	0	the picture is a short term reference picture									
	Value	Name															
1	the picture is a long term reference picture																
0	the picture is a short term reference picture																
	15:0	<p><b>Non-ExistingFrame_Flag[16][1 bit]</b> One-to-one correspondence with the entries of the Intel RefFrameList[16]. 1 bit per reference frame.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">1</td> <td>INVALID</td> <td>the reference picture in that entry of RefFrameList[] does not exist anymore.</td> </tr> <tr> <td style="text-align: center;">0</td> <td>VALID</td> <td>the reference picture in that entry of RefFrameList[] is a valid reference</td> </tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>When an element of the list of frames is not relevant (e.g., due to the corresponding reference entry being empty or being marked as "not used for reference"), the value of the corresponding bit of NonExistingFrameFlags shall be set to 0.</p>	Value	Name	Description	1	INVALID	the reference picture in that entry of RefFrameList[] does not exist anymore.	0	VALID	the reference picture in that entry of RefFrameList[] is a valid reference						
Value	Name	Description															
1	INVALID	the reference picture in that entry of RefFrameList[] does not exist anymore.															
0	VALID	the reference picture in that entry of RefFrameList[] is a valid reference															
2	31:0	<p><b>UsedForReference_Flag[16][2 bits]</b> One-to-one correspondence with the entries of the Intel RefFrameList[16]. 2 bits per reference frame.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>NOT_REFERENCE</td> <td>indicates a frame is "not used for reference".</td> </tr> <tr> <td style="text-align: center;">1</td> <td>TOP_FIELD</td> <td>bit[0] indicates that the top field of a frame is marked as "used for reference".</td> </tr> <tr> <td style="text-align: center;">2</td> <td>BOTTOM_FIELD</td> <td>bit[1] indicates that the bottom field of a frame is marked as "used for reference".</td> </tr> <tr> <td style="text-align: center;">3</td> <td>FRAME</td> <td>bit[1:0] indicates that a frame (or field pair) is marked as "used for reference".</td> </tr> </tbody> </table>	Value	Name	Description	0	NOT_REFERENCE	indicates a frame is "not used for reference".	1	TOP_FIELD	bit[0] indicates that the top field of a frame is marked as "used for reference".	2	BOTTOM_FIELD	bit[1] indicates that the bottom field of a frame is marked as "used for reference".	3	FRAME	bit[1:0] indicates that a frame (or field pair) is marked as "used for reference".
Value	Name	Description															
0	NOT_REFERENCE	indicates a frame is "not used for reference".															
1	TOP_FIELD	bit[0] indicates that the top field of a frame is marked as "used for reference".															
2	BOTTOM_FIELD	bit[1] indicates that the bottom field of a frame is marked as "used for reference".															
3	FRAME	bit[1:0] indicates that a frame (or field pair) is marked as "used for reference".															
3..10	31:0	<p><b>LTSTFrameNumList[16][16 bits]</b> One-to-one correspondence with the entries of the Intel RefFrameList[16]. 16 bits per reference frame. Depending on the corresponding LongTermFrame_Flag[], the content of this field is interpreted differently.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">1</td> <td>LongTermFrame_Flag[i]</td> <td>LTSTFrameNumList[i] represent LongTermFrameIdx.</td> </tr> <tr> <td style="text-align: center;">0</td> <td>ShortTermFrame_Flag[i]</td> <td>LTSTFrameNumList[i] represent Short Term Picture FrameNum.</td> </tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>When an element of the list of frames is not relevant (e.g., due to the corresponding reference entry being empty or being marked as "not used for reference"), the value of the LTSTFrameNumList entry shall be set to 0.</p>	Value	Name	Description	1	LongTermFrame_Flag[i]	LTSTFrameNumList[i] represent LongTermFrameIdx.	0	ShortTermFrame_Flag[i]	LTSTFrameNumList[i] represent Short Term Picture FrameNum.						
Value	Name	Description															
1	LongTermFrame_Flag[i]	LTSTFrameNumList[i] represent LongTermFrameIdx.															
0	ShortTermFrame_Flag[i]	LTSTFrameNumList[i] represent Short Term Picture FrameNum.															

<b>MFD_AVC_DPB_STATE</b>						
11..18 <b>Project:</b> CHV, BSW	31:0 <b>ViewIDList[16][16 bits]</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table> One-to-one correspondence with the entries of the Intel RefFrameList[16]. 16 bits per reference frame. The view ids are 10-bits, the upper 6 bits are ignored."000000" & ViewId1[9:0] & "000000" & ViewId0[9:0] <table border="1" style="width: 100%; border-collapse: collapse; background-color: #e6f2ff;"> <tr> <th style="text-align: center; padding: 5px;">Programming Notes</th> </tr> <tr> <td style="padding: 5px;">When an Intel RefFrameList[i] is not an valid entries, Viewid should be set to 0x00</td> </tr> </table>	Project:	CHV, BSW	Programming Notes	When an Intel RefFrameList[i] is not an valid entries, Viewid should be set to 0x00	
Project:	CHV, BSW					
Programming Notes						
When an Intel RefFrameList[i] is not an valid entries, Viewid should be set to 0x00						
19..22 <b>Project:</b> CHV, BSW	31:0 <b>ViewOrderListL0[16][8 bits]</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table> One-to-one correspondence with the entries of the Intel RefFrameList[16]. 8 bits per reference frame. The view order need 4-bits, the upper 4 bits are ignored. 0000 & ViewOrder3[3:0] & 0000 & ViewOrder2[3:0] & 0000 & ViewOrder1[3:0] & 0000 & ViewOrder0[3:0] <table border="1" style="width: 100%; border-collapse: collapse; background-color: #e6f2ff;"> <tr> <th style="text-align: center; padding: 5px;">Programming Notes</th> </tr> <tr> <td style="padding: 5px;">When the ViewOrderListL0[i] is not an valid inter-view reference, its corresponding ViewOrder should be set to 0xF</td> </tr> <tr> <td style="padding: 5px;">Since only interview with the same polarity will be used, there is no need to have field bit in this list. Hardware is going to append correct polarity bit as needed.</td> </tr> </table>	Project:	CHV, BSW	Programming Notes	When the ViewOrderListL0[i] is not an valid inter-view reference, its corresponding ViewOrder should be set to 0xF	Since only interview with the same polarity will be used, there is no need to have field bit in this list. Hardware is going to append correct polarity bit as needed.
Project:	CHV, BSW					
Programming Notes						
When the ViewOrderListL0[i] is not an valid inter-view reference, its corresponding ViewOrder should be set to 0xF						
Since only interview with the same polarity will be used, there is no need to have field bit in this list. Hardware is going to append correct polarity bit as needed.						
23..26 <b>Project:</b> CHV, BSW	31:0 <b>ViewOrderListL1[16][8 bits]</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table> One-to-one correspondence with the entries of the Intel RefFrameList[16]. 8 bits per reference frame. The view order need 4-bits, the upper 4 bits are ignored. 0000 & ViewOrder3[3:0] & 0000 & ViewOrder2[3:0] & 0000 & ViewOrder1[3:0] & 0000 & ViewOrder0[3:0] <table border="1" style="width: 100%; border-collapse: collapse; background-color: #e6f2ff;"> <tr> <th style="text-align: center; padding: 5px;">Programming Notes</th> </tr> <tr> <td style="padding: 5px;">When the ViewOrderListL1[i] is not an valid inter-view reference, its corresponding ViewOrder should be set to 0xF</td> </tr> <tr> <td style="padding: 5px;">Since only interview with the same polarity will be used, there is no need to have field bit in this list. Hardware is going to append correct polarity bit as needed.</td> </tr> </table>	Project:	CHV, BSW	Programming Notes	When the ViewOrderListL1[i] is not an valid inter-view reference, its corresponding ViewOrder should be set to 0xF	Since only interview with the same polarity will be used, there is no need to have field bit in this list. Hardware is going to append correct polarity bit as needed.
Project:	CHV, BSW					
Programming Notes						
When the ViewOrderListL1[i] is not an valid inter-view reference, its corresponding ViewOrder should be set to 0xF						
Since only interview with the same polarity will be used, there is no need to have field bit in this list. Hardware is going to append correct polarity bit as needed.						

## MFD\_AVC\_PICID\_STATE

MFD_AVC_PICID_STATE			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>This is a frame level state command used for both AVC Long and Short Format in VLD mode. PictureID[16] contains the pictureID of each reference picture (16 maximum) so hardware can uniquely identify the reference picture across frames (this will be used for DMV operation). This command will be needed for both short and long format.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h MFX_MULTI_DW
		Format:	OpCode
	26:24	<b>Media Command Opcode</b>	
		Default Value:	1h MFD_AVC_DPB_STATE
		Format:	OpCode
	23:21	<b>SubOpcode A</b>	
Default Value:		1h DEC	
Format:		OpCode	
20:16	<b>SubOpcode B</b>		
	Default Value:	5h MEDIA_	
	Format:	OpCode	
15:12	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
11:0	<b>DWord Length</b>		
	Default Value:	0008h Excludes DWord (0,1)	
	Project:	CHV, BSW	
	Format:	=n Total Length - 2	
1	31:1	<b>Reserved</b>	
		Project:	All
		Format:	MBZ

<b>MFD_AVC_PICID_STATE</b>				
	0	<b>PictureID Remapping Disable</b>		
	Project:		CHV, BSW	
	<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>
	0h	AVC decoder will use 16 bits Picture ID to handle DMV and identify the reference picture	Desc	All
	1h	AVC decoder will use 4 bits FrameStoreID (index to RefFrameList) to handle DMV and identify the reference picture	Desc	All
<b>Programming Notes</b>				
If Picture ID Remapping Disable is "1", PictureIDList will not be used.				
2..9	31:0	<b>PictureIDList[16][16 bits]</b>		
Project:		CHV, BSW		
<p>One-to-one correspondence with the entries of the Intel RefFrameList[16]. 16 bits per reference frame. PictureID of each Frame uniquely identifies the reference picture across frames. The same number cannot be reused until the reference picture is completely retired (no longer used for reference). When an element of the list of frames is not relevant (e.g., due to the corresponding reference entry being empty or being marked as "not used for reference"), the value of the LTSTFrameNumList entry shall be set to 0.</p>				

## MFD\_AVC\_SLICEADDR

<b>MFD_AVC_SLICEADDR</b>			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>This is a Slice level command used only for DXVA2 AVC Short Slice Bitstream Format VLD mode. When decoding a slice, H/W needs to know the last MB of the slice has reached in order to start decoding the next slice. It also needs to know if a slice is terminated but the last MB has not reached, error concealment should be invoked to generate those missing MBs. For AVC DXVA2 Short Format, the only way to know the last MB position of the current slice, H/W needs to snoop into the next slice's start MB address (a linear address encoded in the Slice Header). Since each BSD Object command can have only one indirect bitstream buffer address, this command is added to help H/W to snoop into the next slice's slice header and retrieve its Start MB Address. This command will take the next slice's bitstream buffer address as input (exactly the same way as a BSD Object command), and parse only the first_mb_in_slice syntax element. The result will be stored inside the H/W, and will be used to decode the current slice specified in the BSD Object command. Only the very first few bytes (max 5 bytes for a max 4K picture) of the Slice Header will be decoded, the rest of the bitstream are don't care. This is because the first_mb_in_slice is encoded in Exponential Golomb, and will take 33 bits to represent the max <math>256 \times 256 = 64K-1</math> value. The indirect data of MFD_AVC_SLICEADDR is a valid BSD object and is decoded as in BSD OBJECT command. The next Slice Start MB Address is also exposed to the MMIO interface. The Slice Start MB Address (first_mb_in_slice) is a linear MB address count; but it is translated into the corresponding 2D MB X and Y raster position, and are stored internally as NextSliceMbY and NextSliceMbX.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h MFD_AVC_SLICEADDR
		Format:	OpCode
	26:24	<b>Media Command Opcode</b>	
		Default Value:	1h AVC_DEC
		Format:	OpCode
	23:21	<b>SubOpcode A</b>	
		Default Value:	1h
		Format:	OpCode
	20:16	<b>SubOpcode B</b>	
		Default Value:	7h
		Format:	OpCode
15:12	<b>Reserved</b>		
	Format:	MBZ	

<b>MFD_AVC_SLICEADDR</b>								
	11:0	<b>DWord Length</b> Format: =n Total Length - 2						
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 20%;">Value</th> <th style="width: 60%;">Name</th> <th style="width: 20%;">Project</th> </tr> </thead> <tbody> <tr> <td>1h</td> <td>Excludes DWord (0,1) <b>[Default]</b></td> <td>CHV, BSW</td> </tr> </tbody> </table>	Value	Name	Project	1h	Excludes DWord (0,1) <b>[Default]</b>	CHV, BSW
		Value	Name	Project				
1h	Excludes DWord (0,1) <b>[Default]</b>	CHV, BSW						
1	31:0	<b>Indirect BSD Data Length</b> Project: CHV, BSW Format: U32 <p>This field provides the length in bytes of the indirect data. A value zero indicates that indirect data fetching is disabled - subsequently, the Indirect Data Start Address field is ignored. Driver always programs this up to 5 bytes; for bitstream less than 5 bytes, driver program the lesser value. (Emulation Prevention Byte should never happen for the first 5 bytes when the max picture size can only be 4Kx4K)It is the length in bytes of the bitstream data for the current slice, including Slice Header + Slice Data + Emulation Prevention Bytes + any filling trailing zeros after the last MB. Hardware ignores the contents after the last non-zero byte. Trailing zero is allowed and handled correctly in both CABAC and CAVLC modes.</p>						
2	31:29	<b>Reserved</b> Format: MBZ						
	28:0	<b>Indirect BSD Data Start Address</b> This field specifies the Graphics Memory starting address of the data to be fetched into BSD Unit for processing. This pointer is relative to the MFD Indirect Object Base Address.Hardware ignores this field if indirect data is not present. It is a byte-aligned address for the AVC bitstream data in both CABAC/CAVLD Modes.In implementing a phantom slice at the end of a picture for automatic error concealment, this field should set to 0.It includes the NAL Header Byte. (but does not perform EMU detection).Must provide a valid MB address, even if error. MB must be clamped to within a pic boundary. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 60%;">Value</th> <th style="width: 40%;">Name</th> </tr> </thead> <tbody> <tr> <td>[0,512MB)</td> <td></td> </tr> </tbody> </table>	Value	Name	[0,512MB)			
Value	Name							
[0,512MB)								



## MFD\_IT\_OBJECT

<b>MFD_IT_OBJECT</b>			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
All weight mode (default and implicit) are mapped to explicit mode. But the weights come in either as explicit or implicit.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h MFD_IT_OBJECT
		Format:	OpCode
	26:24	<b>Media Command Opcode</b>	
		Default Value:	0h MFX_COMMON_DEC
		Format:	OpCode
	23:21	<b>SubOpcode A</b>	
Default Value:		1h	
Format:		OpCode	
20:16	<b>SubOpcode B</b>		
	Default Value:	9h	
	Format:	OpCode	
15:12	<b>Reserved</b>		
	Format:	MBZ	
11:0	<b>DWord Length</b>		
	Default Value:	06h Excludes DWord (0,1) For AVC = Ch	
	Format:	=n Total Length - 2 Note: Regardless of the mode, inline data must be present in this command.	
1	31:10	<b>Reserved</b>	
		Format:	MBZ
	9:0	<b>Indirect IT-MV Data Length</b>	
Format:		U10 FormatDesc: In bytes	
This field provides the length in bytes of the indirect data, which contains all the MVs for the current MB (in any partitioning and subpartitioning form). A value zero indicates that indirect data fetching is disabled - subsequently, the Indirect IT-MV Data Start Address field is ignored.			

<b>MFD_IT_OBJECT</b>							
		This field must have the same alignment as the Indirect Object Data Start Address.AVC-IT Mode: It must be DWord aligned (since each MV is 4bytes in size)Driver has to derived this field from MVsize (MVquantity in DXVA, exact size) *4 bytes per MV.This field is only valid in AVC decoder IT mode (VC1 and MPEG uses inline MV data).					
2	31:29	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ			
	Format:	MBZ					
28:0	<p><b>Indirect IT-MV Data Start Address Offset</b></p> <p>This field specifies the memory starting address (offset) of the MV data to be fetched into the IT pipeline for processing. This pointer is relative to the Indirect IT-MV Object Base Address.Hardware ignores this field if indirect data is not present, i.e. the Indirect MV Data Length is set to 0. Alignment of this address depends on the mode of operation.AVC-IT Mode: It must be DWord aligned (since each MV is 4 bytes in size). This field is only valid in AVC decoder IT mode (VC1 and MPEG uses inline MV data).</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>[0,512MB)</td> <td></td> </tr> </tbody> </table>	Value	Name	[0,512MB)			
Value	Name						
[0,512MB)							
3	31:12	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ			
	Format:	MBZ					
11:0	<p><b>Indirect IT-COEFF Data Length</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> </table> <p>This field provides the length in bytes of the indirect data, which contains all the non-zero coefficients for the current MB. A value zero indicates that indirect data fetching is disabled - subsequently, the Indirect IT-COEFF Data Start Address field is ignored. Since each IT-COEFF data is 1 DW in size, with 12 bits, this field can be extended to support up to 4:4:4 format.(256 pixel * 3 byte pixel components * 4 bytes per coeff).This field must be integer multiple of 16-bytes for AVC (since each coefficient is 4 bytes in size).This field is only valid in AVC, VC1, MPEG2 decoder IT mode.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 40%;">Value</th> <th style="width: 60%;">Name</th> </tr> </thead> <tbody> <tr> <td>[0,3072]</td> <td>In bytes [0, 256*3*4]</td> </tr> </tbody> </table>	Project:	All	Value	Name	[0,3072]	In bytes [0, 256*3*4]
Project:	All						
Value	Name						
[0,3072]	In bytes [0, 256*3*4]						
4	31:29	<p><b>Reserved</b></p>					
	28:0	<p><b>Indirect IT-COEFF Data Start Address Offset</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> </table> <p>This field specifies the memory starting address (offset) of the coeff data to be loaded into the IT pipeline for processing. This pointer is relative to the Indirect IT-COEFF Object Base Address.Hardware ignores this field if indirect IT-COEFF data is not present, i.e. the Indirect IT-COEFF Data Length is set to 0.This field must be DW aligned, since each coefficient is 4 bytes in size.Driver will determine the Num of EOB 4x4/8x8 must match the block cbp flags, if not match, hardware cannot hang - add error handling.This field is only valid in AVC, VC1, MPEG2 decoder IT mode.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>[0,512MB)</td> <td></td> </tr> </tbody> </table>	Project:	All	Value	Name	[0,512MB)
Project:	All						
Value	Name						
[0,512MB)							

<b>MFD_IT_OBJECT</b>							
5	31:6	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ			
	Format:	MBZ					
5:0	<p><b>Indirect IT-DBLK Control Data Length</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U6</td> </tr> </table> <p>This field provides the length in bytes of the indirect data, which contains all the deblocker control information for the current MB (in 4x4 sub-block partitioning). A value zero indicates that indirect data fetching is disabled - subsequently, the Indirect IT-DBLK Data Start Address field is ignored. This field must have the same alignment as the Indirect IT-DBLK Data Start Address. It must be DWord aligned. Each Deblock Control Data record is 48 bytes or 12 DWords in size. This field is only valid in AVC decoder IT mode.</p>	Project:	All	Format:	U6		
Project:	All						
Format:	U6						
6	31:29	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ			
	Format:	MBZ					
28:0	<p><b>Indirect IT-DBLK Control Data Start Address Offset</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 20%;">Format:</td> <td>IndirectObjectBaseAddress[28:0]</td> </tr> </table> <p>This field specifies the memory starting address (offset) of the Deblocker control data to be fetched into the IT Pipeline for processing. This pointer is relative to the Indirect IT-DBLK Object Base Address. Hardware ignores this field if indirect data is not present, ie. The indirect IT-DBLK Control Data Length is set to 0. It must be DWord aligned. Each Deblock Control Data record is 48 bytes or 12 DWords in size. This field is only valid in AVC decoder IT mode.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 60%; text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>[0,512MB)</td> <td></td> </tr> </tbody> </table>	Format:	IndirectObjectBaseAddress[28:0]	Value	Name	[0,512MB)	
Format:	IndirectObjectBaseAddress[28:0]						
Value	Name						
[0,512MB)							
7..n	31:0	<p><b>Inline Data</b></p> <p>Union for all 3 codecs Includes IT, MC, IntraPred inline data as well as Deblocker control information AVC-IT Modes: Hardware interprets this data in the specified format. VC1-IT Modes: Hardware interprets this data in the specified format. MV inline MPEG2-IT Modes: Hardware interprets this data in the specified format. (IS mode) MV inline For AVC there 7 DWords of inline data, hence N is equal to 13.</p>					

## MFD\_JPEG\_BSD\_OBJECT

<b>MFD_JPEG_BSD_OBJECT</b>				
Project:	CHV, BSW			
Source:	VideoCS			
Length Bias:	2			
Exists If:	//Decoder			
DWord	Bit	Description		
0	31:29	<b>Command Type</b>		
		Default Value:	3h PARALLEL_VIDEO_PIPE	
		Format:	OpCode	
	28:27	28:27	<b>Pipeline</b>	
			Default Value:	2h MFD_JPEG_BSD_OBJECT
			Format:	OpCode
	26:24	26:24	<b>Media Command Opcode</b>	
			Default Value:	7h JPEG_DEC
			Format:	OpCode
	23:21	23:21	<b>SubOpcode A</b>	
Default Value:			1h	
Format:			OpCode	
20:16	20:16	<b>SubOpcode B</b>		
		Default Value:	8h	
		Format:	OpCode	
15:12	15:12	<b>Reserved</b>		
		Project:	All	
		Format:	MBZ	
11:0	11:0	<b>DWord Length</b>		
		Default Value:	004h Excludes DWord (0,1)	
		Project:	All	
		Format:	=n Total Length - 2	
1	31:0	<b>Indirect Data Length</b>		
		Project:	All	
<p>. It is the length in bytes of the bitstream data for the current Scan. It includes the first byte of the first MCU and the last non-zero byte of the last MCU in the Scan. Specifically, the zero-padding bytes (if present) are excluded. Hardware ignores the contents after the last non-zero byte.</p>				

<b>MFD_JPEG_BSD_OBJECT</b>											
2	31:29	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ					
	Project:	All									
Format:	MBZ										
28:0	<p><b>Indirect Data Start Address</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>IndirectObjectOffset[28:0]</td> </tr> </table> <p>This field specifies the Graphics Memory starting address of the data to be fetched into BSD Unit for processing. This pointer is relative to the BSD Indirect Object Base Address. Hardware ignores this field if indirect data is not present. It is a byte-aligned address for the JPEG bitstream data</p>	Project:	All	Format:	IndirectObjectOffset[28:0]						
Project:	All										
Format:	IndirectObjectOffset[28:0]										
3	31:29	<p><b>Reserved</b></p>									
	28:16	<p><b>Scan Horizontal Position</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U13 bits in blocks</td> </tr> </table> <p>This field indicates the horizontal position (in block units) of the first MCU in the Scan.</p>	Project:	All	Format:	U13 bits in blocks					
	Project:	All									
	Format:	U13 bits in blocks									
15:13	<p><b>Reserved</b></p>										
12:0	<p><b>Scan Vertical Position</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U13 bits in blocks</td> </tr> </table> <p>This field indicates the vertical position (in block units) of the first MCU in the Scan.</p>	Project:	All	Format:	U13 bits in blocks						
Project:	All										
Format:	U13 bits in blocks										
4	31	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ							
	Format:	MBZ									
	30	<p><b>Interleaved</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #e1eef6;"> <th style="width: 15%;">Value</th> <th style="width: 35%;">Name</th> <th style="width: 50%;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Non-Interleaved</td> <td>one component in the Scan</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Interleaved</td> <td>multiple components in the Scan</td> </tr> </tbody> </table>	Value	Name	Description	0	Non-Interleaved	one component in the Scan	1	Interleaved	multiple components in the Scan
	Value	Name	Description								
	0	Non-Interleaved	one component in the Scan								
	1	Interleaved	multiple components in the Scan								
29:27	<p><b>Scan Components</b></p> <p>Bit0: Y Bit1: U Bit2: V For example, if non-interleaved Y, then it will be set to 001b. If interleaved Y, U, and V, it will be set to 111b.</p>										
26	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ								
Format:	MBZ										
25:0	<p><b>MCU Count</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U26</td> </tr> </table> <p>This field indicates the number of MCUs in the Scan.</p>	Project:	All	Format:	U26						
Project:	All										
Format:	U26										

<b>MFD_JPEG_BSD_OBJECT</b>					
5	31:16	<b>Reserved</b>			
		<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:
	Project:	All			
	Format:	MBZ			
	15:0	<b>RestartInterval(16 bit)</b>			
		<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U16</td> </tr> </table>	Project:	All	Format:
Project:		All			
Format:		U16			
<p>Specifies the number of MCU in restart interval. Valid values are 1-&gt;0xFFFF Value of 0 implies that all the SCAN have only one ECS.</p>					

## MFD\_MPEG2\_BSD\_OBJECT

<b>MFD_MPEG2_BSD_OBJECT</b>			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>Different from AVC and VC1, MFD_MPEG2_BSD_OBJECT command is pipelinable. This is for performance purpose as in MPEG2 a slice is defined as a group of MBs of any size that must be within a macroblock row. Slice header parameters are passed in as inline data and the bitstream data for the slice is passed in as indirect data. Of the inline data, slice_horizontal_position and slice_vertical_position determines the location within the destination picture of the first macroblock in the slice. The content in this command is identical to that in the MEDIA_OBJECT command in VLD mode described in the Media Chapter.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h MFD_MPEG2_BSD_OBJECT
		Format:	OpCode
	26:24	<b>Media Command Opcode</b>	
		Default Value:	3h MPEG2_DEC
		Format:	OpCode
	23:21	<b>SubOpcode A</b>	
		Default Value:	1h
		Format:	OpCode
	20:16	<b>SubOpcode B</b>	
		Default Value:	8h
		Format:	OpCode
	15:12	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
11:0	<b>DWord Length</b>		
	Default Value:	0003h Excludes DWord (0,1)	
	Project:	All	
	Format:	=n Total Length - 2	

<b>MFD_MPEG2_BSD_OBJECT</b>												
1	31:0	<p><b>Indirect BSD Data Length</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>It is the length in bytes of the bitstream data for the current slice. It includes the first byte of the first macroblock and the last non-zero byte of the last macroblock in the slice. Specifically, the zero-padding bytes (if present) and the next start-code are excluded. This field is sized to support beyond MPEG-2 MP@HL bitstream (&lt;4K). According to Table 8-6 of ISO/IEC 13818-2, the maximum number of bits per macroblock for 4:2:0 is 4608. So the maximum slice size for 4K x 4K is <math>4608 * 256 / 8 = 147,456</math> bytes (0x24000), which requires 18 bits.</p> <table border="1" style="width: 100%;"> <tr> <th style="text-align: center; background-color: #e1eef6;">Programming Notes</th> <th style="text-align: center;">Project</th> </tr> <tr> <td style="width: 80%;">As MPEG-2 spec does not post any limitation of the size of zero-padding bytes, it is possible to have a slice data with large length (including zero-padding bytes). As the data beyond 0x10E00 would only be zero bytes for a valid slice data</td> <td></td> </tr> <tr> <td>zero-padding restriction is removed</td> <td style="text-align: center;">CHV, BSW</td> </tr> </table>	Project:	All	Format:	U32	Programming Notes	Project	As MPEG-2 spec does not post any limitation of the size of zero-padding bytes, it is possible to have a slice data with large length (including zero-padding bytes). As the data beyond 0x10E00 would only be zero bytes for a valid slice data		zero-padding restriction is removed	CHV, BSW
		Project:	All									
		Format:	U32									
		Programming Notes	Project									
As MPEG-2 spec does not post any limitation of the size of zero-padding bytes, it is possible to have a slice data with large length (including zero-padding bytes). As the data beyond 0x10E00 would only be zero bytes for a valid slice data												
zero-padding restriction is removed	CHV, BSW											
2	31:29	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ						
		Project:	All									
Format:	MBZ											
28:0	<p><b>Indirect Data Start Address</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>IndirectObjectOffset[28:0]</td> </tr> </table> <p>This field specifies the Graphics Memory starting address of the data to be fetched into BSD Unit for processing. This pointer is relative to the BSD Indirect Object Base Address. Hardware ignores this field if indirect data is not present. It is a byte-aligned address for the MPEG2 VLD bitstream data This address points to the first byte of the MB layer data, i.e. not including slice header.</p>	Format:	IndirectObjectOffset[28:0]									
Format:	IndirectObjectOffset[28:0]											
3..4	31:0	<p><b>Inline Data</b></p> <p>All the required Slice Header parameters and error handling settings are captured as MPEG2_BSD_OBJECT Inline Data Descriptor structures. It has a fixed size of 2 DWs. Its definition is described in the next section.</p>										



## MFD\_VC1\_BSD\_OBJECT

<b>MFD_VC1_BSD_OBJECT</b>			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>The MFD_VC1_BSD_OBJECT command is the only primitive command for the VC1 Decoding Pipeline. The macroblock data portion of the bitstream is loaded as indirect data object. Before issuing a MFD_VC1_BSD_OBJECT command, all VC1 states of the MFD Engine need to be valid. Therefore the commands used to set these states need to have been issued prior to the issue of a MFD_VC1_BSD_OBJECT command. VC1 deblock filter kernel cross the slice boundary if in the last MB row of a slice, so need to know the last MB row of a slice to disable the edge mask. There is why VC1 BSD hardware need to know the end of MB address for the current slice. As such no more phantom slice is needed for VC1, as long as the driver will program both start MB address in the current slice and the start MB address of the next slice. As a result, we can also support multiple picture state commands in between slices.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h MFX_MULTI_DW
		Format:	OpCode
	26:24	<b>Media Command Opcode</b>	
		Default Value:	2h VC1_DEC
		Format:	OpCode
	23:21	<b>SubOpcode A</b>	
		Default Value:	1h
		Format:	OpCode
	20:16	<b>SubOpcode B</b>	
		Default Value:	8h
		Format:	OpCode
	15:12	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	11:0	<b>DWord Length</b>	
		Default Value:	0003h Excludes DWord (0,1)
		Project:	All
		Format:	=n Total Length - 2

<b>MFD_VC1_BSD_OBJECT</b>									
1	31:24	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ			
	Project:	All							
	Format:	MBZ							
	23:0	<p><b>Indirect BSD Data Length</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U24</td> </tr> </table> <p>This field provides the length in bytes of the indirect data. A value zero indicates that indirect data fetching is disabled - subsequently, the Indirect Data Start Address field is ignored. This field must have the same alignment as the Indirect Object Data Start Address. GEN6 Long Format : It is the length in bytes of the bitstream data for the current slice/picture. It includes the first byte of the first macroblock and the last byte of the last macroblock in the slice/picture. Specifically, the zero-padding bytes (if present) and the next start-code are excluded. Hardware ignores the contents after the last non-zero byte (trailing zeros). This field is sized to support VC1 AP@L4 Level bitstream. It includes the byte that contains the First MB Bit Offset. GEN7 Short Format : It is the length in bytes of the bitstream data for the current slice, including Picture/Slice Header + Emulation Prevention Bytes + any filling trailing zeros after the last MB. Hardware ignores the contents after the last non-zero byte. Trailing zero is allowed and handled correctly.</p>	Project:	All	Format:	U24			
Project:	All								
Format:	U24								
31:29	<p><b>Reserved</b></p>								
28:0	<p><b>Indirect Data Start Address</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>IndirectObjectOffset[28:0]</td> </tr> </table> <p>This field specifies the Graphics Memory starting address of the data to be fetched into BSD Unit for processing. This pointer is relative to the MFD Indirect Object Base Address. Hardware ignores this field if indirect data is not present. It is a byte-aligned address for the VC1 bitstream data.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 60%; text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>[0,512MB)</td> <td></td> </tr> </tbody> </table>	Project:	All	Format:	IndirectObjectOffset[28:0]	Value	Name	[0,512MB)	
Project:	All								
Format:	IndirectObjectOffset[28:0]								
Value	Name								
[0,512MB)									
3	31:24	<p><b>Reserved</b></p>							
	23:16	<p><b>Slice Start Vertical Position</b></p> <p>This field specifies the position in y-direction of the first macroblock in the Slice in unit of macroblocks. For SecondField this value is reset to zero as opposed to the VC1 spec Ref: 9.1.2 Slice Layer. This field is for both Long and Short VC1 Interface Format.</p>							
	15:9	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ			
	Project:	All							
Format:	MBZ								
8:0	<p><b>Next Slice Vertical Position</b></p> <p>This field specifies the position in y-direction of the first macroblock in the next Slice in unit of macroblocks. This field is primarily used for error concealment. In the case that current slice is the last slice, this field should set to the height of picture (since y-direction is zero-based numbering) This field is maintained and provided by the driver for both Long and Short VC1 Interface Format.</p>								

<b>MFD_VC1_BSD_OBJECT</b>															
4	31:16	<b>First_MB_Byte_Offset of Slice Data or Slice Header</b> For DXVA2 VC1 Short Format onlyIt gives the byte offset to locate the first MB data in the bitstream for a slice, relative to the Indirect BSD Data Start Address.													
	15:5	<b>Reserved</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>		Project:	All	Format:	MBZ								
	Project:	All													
	Format:	MBZ													
	4	<b>Emulation Prevention Byte Present</b> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 10%;">Name</th> <th style="width: 60%;">Description</th> <th style="width: 10%;">Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td></td> <td>H/W needs to perform Emulation Byte Removal</td> <td>All</td> </tr> <tr> <td>1h</td> <td></td> <td>H/W does not need to perform Emulation Byte Removal</td> <td>All</td> </tr> </tbody> </table>			Value	Name	Description	Project	0h		H/W needs to perform Emulation Byte Removal	All	1h		H/W does not need to perform Emulation Byte Removal
Value	Name	Description	Project												
0h		H/W needs to perform Emulation Byte Removal	All												
1h		H/W does not need to perform Emulation Byte Removal	All												
3	<b>Reserved</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>			Project:	All	Format:	MBZ								
Project:	All														
Format:	MBZ														
2:0	<b>FirstMbBitOffset (First Macroblock Bit Offset )</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td>U3</td> </tr> </table> <p>This field provides the bit offset of the first macroblock of the Slice in the first byte of the input compressed bitstream.It is used with First_MB_Byte_Offset for non-byte aligned position.</p>			Format:	U3										
Format:	U3														

## MFD\_VC1\_LONG\_PIC\_STATE

<b>MFD_VC1_LONG_PIC_STATE</b>			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>MFX_VC1_LONG_PIC_STATE command encapsulates the decoding parameters that are read or derived from bitstream syntax elements above (inclusive) picture header layer. These parameters are static for a picture and when slice structure is present, these parameters are not changed from slice to slice of the same picture. Hence, this command is only issued at the beginning of processing a new picture and prior to the VC1_*_OBJECT command. The values set for these state variables are retained internally across slices. Only the parameters needed by hardware (BSD unit) to decode bit sequence for the macroblocks in a picture layer or a slice layer are presented in this command. Other parameters such as the ones used for inverse transform or motion compensation are provided in MFX_VC1_PRED_PIPE_STATE command. This Long interface format is intel proprietary interface. Driver will need to perform addition operations to generate all the fields in this command.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h MFD_VC1_LONG_PIC_STATE
		Format:	OpCode
	26:24	<b>Media Command Opcode</b>	
		Default Value:	2h VC1_DEC
		Format:	OpCode
	23:21	<b>SubOpcode A</b>	
		Default Value:	1h
		Format:	OpCode
	20:16	<b>SubOpcode B</b>	
		Default Value:	1h
		Format:	OpCode
	15:12	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	11:0	<b>DWord Length</b>	
		Default Value:	0004h Excludes DWord (0,1)
		Project:	All
		Format:	=n Total Length - 2

<b>MFD_VC1_LONG_PIC_STATE</b>											
1	31:24	<b>Reserved</b>									
		Project:	CHV, BSW								
		Format:	MBZ								
	23:16	<b>PictureHeightInMBsMinus1 (Picture Height Minus 1 in Macroblocks)</b>									
		Project:	CHV, BSW								
	Format:	U8									
<p>This field indicates the height of the picture in unit of macroblocks. For example, for a 1920x1080 frame picture, PictureHeightInMBs equals 68 (1080 divided by 16, and rounded up, i.e. effectively specified as 1088 instead). This field is used in VLD and IT modes.</p>											
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 25%;">Name</th> <th style="width: 45%;">Description</th> <th style="width: 15%;">Project</th> </tr> </thead> <tbody> <tr> <td>[0,254]</td> <td>Value_0_to_254</td> <td>a valid range of [0,254] [1, 255] MB</td> <td>CHV, BSW</td> </tr> </tbody> </table>				Value	Name	Description	Project	[0,254]	Value_0_to_254	a valid range of [0,254] [1, 255] MB	CHV, BSW
Value	Name	Description	Project								
[0,254]	Value_0_to_254	a valid range of [0,254] [1, 255] MB	CHV, BSW								
<b>Programming Notes</b>											
<p>Note: Even though the Advanced Profile allows frame dimensions (width, height) to not be aligned to macroblock boundary, it doesn't affect the bitstream decoding. And it is preferable to use 'intermediate buffer' that is macroblock aligned for decoding. In order to simplify the out-of-bound reference pixel access, the out-of-bound extrapolation rule in VC1 spec can be used to expand the expected decoded frame to the intermediate buffer dimension.</p>											
15:8	<b>Reserved</b>										
		Project:	CHV, BSW								
		Format:	MBZ								
	7:0	<b>PictureWidthInMBsMinus1 (Picture Width Minus 1 in Macroblocks)</b>									
		Project:	CHV, BSW								
	Format:	U8-1									
<p>This field indicates the width of the picture in unit of macroblocks. For example, for a 1920x1080 frame picture, PictureWidthInMBs equals 120 (1920 divided by 16). This field is used in VLD and IT modes</p>											
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 25%;">Name</th> <th style="width: 45%;">Description</th> <th style="width: 15%;">Project</th> </tr> </thead> <tbody> <tr> <td>[0,254]</td> <td>Value_0_to_254</td> <td>[1,255] MB</td> <td>CHV, BSW</td> </tr> </tbody> </table>				Value	Name	Description	Project	[0,254]	Value_0_to_254	[1,255] MB	CHV, BSW
Value	Name	Description	Project								
[0,254]	Value_0_to_254	[1,255] MB	CHV, BSW								
2	31:24	<b>Bitplane Buffer Pitch Minus 1</b>									
		Project:	CHV, BSW								
		Format:	U7-1 Pitch in (Bytes - 1).								
	<p>Specifies the bitplane buffer pitch in (#Bytes - 1). Bitplane buffer is a linear buffer. It is needed only when the bitplane is not encoded as raw, and therefore is present in the header explicitly. In VC1 Long Format (Gen6 and Gen7), it is written by an application and later read by the HW. But in VC1 Short Format (Gen7 only), it is written and read by H/W only. This field is specified for better performance</p>										
	<b>Value</b>		<b>Name</b>								
[0, FFFFFFFFh]											

<b>MFD_VC1_LONG_PIC_STATE</b>				
<b>Programming Notes</b>				
<p>For Gen6 : The pitch must be equal to PictureWidthInMBs/2.For Gen7 VC1 Long Format : The pitch must be equal to PictureWidthInMBs/2.For Gen7 VC1 Short Format : If Pic Width is less than or equal to 2K pixels, bitplane pitch is set to 64 (one cacheline; programmed as 63) bytes per MB row. If Pic Width is greater than 2K pixels, bitplane pitch is set to 128 (two cachelines; programmed as 127) bytes per MB row.This field is not used in IT mode, used in VLD mode only.For VC1 DXVA2 Short Format, the bitplane specification is between H/W and Driver only. For Long Format, application is responsible for allocation with the driver.</p>				
23:16	<b>Reserved</b>			
	Project:	CHV, BSW		
	Format:	MBZ		
15	<b>DmvSurfaceValid</b>			
	Project:	CHV, BSW		
<p>Indicated when the DMV read surface is valid. This surface stored the direct motion vectors and Mb type.This field is set for B pictures that can refer to a previous P picture for DMV. If there is an I-picture before a B (in decoding order) then this field is not set (as a result, zero's DMV's will be assumed while decoding the B picture. That is, there is no explicit DMV buffer for an I-picture).Whne the current picture being decoded is an I, P or BI, this bit is set to 0, since there is no DMV read in these picture decoding process.This field is not used in IT mode, used in VLD mode only.</p>				
14	<b>ImplicitQuantizer</b>			
	Project:	CHV, BSW		
<p>Derived by driver from QUANTIZER.This field is used in intel VC1 VLD Long Format only, not used in IT and DXVA2 VC1.This bit is set to 1 when syntax element QUANTIZER=0, else its set to 0</p>				
13	<b>Interpolation Rounder Contro</b>			
	Project:	CHV, BSW		
<p>Used only in MC operation. This field specifies the rounding control value used in interpolation operation of motion prediction process.This field is used in VLD and IT modes.</p>				
<b>Programming Notes</b>				
<p>This bit field is taken from bRcontrol in DXVA_PictureParameters data structure</p>				
12	<b>SyncMarker</b>			
	Project:	CHV, BSW		
<p>Indicates whether sync markers are enabled/disabled. If enable, sync markers "may be" present in the current video sequence being decoded. It is a sequence level syntax element and is valid only for Simple and Main Profiles.</p>				
	<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>
	0h	Not Present	Sync Marker is not present in the bitstream	CHV, BSW
	1h	Maybe present	Sync Marker maybe present in the bitstream	CHV, BSW

## MFD\_VC1\_LONG\_PIC\_STATE

		<b>Programming Notes</b>	
		This field is only valid in VLD mode. For Simple Profile, SyncMarker must set to 0. For Main Profile, SyncMarker can be set to 0 or 1. This field is used in both intel and MS DXVA2 VLD interface, but not used in IT mode.	
11:8	<b>Motion Vector Mode</b>		
	Project:	CHV, BSW	
	This field indicates one of the following motion compensation interpolation modes for P and B pictures. The MC interpolation modes apply to prediction values of luminance blocks and are always in quarter-sample. For chrominance blocks, it always performs bilinear interpolation with either half-pel or quarter-pel precision. Before the polarity of Chroma Half-pel or Q-pel is reversed from DXVA2 Spec, now I have fixed it to match with DXVA2 VC1 Spec.		
	Value	Name	Description
	0XX0b		Chroma Quarter -pel + Luma bicubic. (can only be 1MV)
	0XX1b		Chroma Half-pel + Luma bicubic. (can be 1MV or 4MV)
	1XX0b		Chroma Quarter -pel + Luma bilinear. (can only be 1MV)
	1XX1b		Chroma Half-pel + Luma bilinear
		Project	
		CHV, BSW	
		CHV, BSW	
		CHV, BSW	
		CHV, BSW	
		<b>Programming Notes</b>	
	Bits 11:8 are taken from bMVprecisionAndChromaRelation in DXVA_PictureParameters data structure. Bit 11 of Motion Vector Mode = 1 for Luma Bilinear MC; = 0 for Luma Bicubic MC. Bit 8 of Motion Vector Mode = 1 for half-sample Chroma motion = 0 for quarter-sample Chroma motion. This field is used in both VLD and IT modes.		
7	<b>RangeReductionScale</b>		
	Project:	CHV, BSW	
	This field specifies whether the reference picture pixel values should be scaled up or scaled down on-the-fly, if RangeReduction is Enabled.		
	Value	Name	Description
	0h		Scale down reference picture by factor of 2
	1h		Scale up reference picture by factor of 2
		Project	
		CHV, BSW	
		CHV, BSW	
		<b>Programming Notes</b>	
	This bit is derived by driver for Main Profile only. Ignored in Simple and Advanced Profiles. This field is used in both VLD and IT modes. This is derived by driver from the history of RANGERED and RANGEREDFRM syntax elements (i.e. of forward/preceding reference picture) and those of the current picture. RANGERED is the same as (bPicOverflowBlocks » 3) & 1. RANGEREDFRM is the same as (bPicDeblocked » 5) & 1. For the current picture is a B picture, this field represents the state of the forward/preceding reference picture only. Driver is responsible to keep RangeReductionScale, RangeReduction Enable and RANGERED Present Flag of current picture coherent.		

## MFD\_VC1\_LONG\_PIC\_STATE

6	<b>RangeReduction Enable</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This field specifies whether on-the-fly pixel value range reduction should be performed for the preceding (or forward) reference picture. Along with RangeReductionScale to specify whether scale up or down should be performed. It is not the same value as RANGEREDFRM Syntax Element (DXVA_PictureParameters bPicDeblocked bit 5) in the Picture Header.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 50%;">Description</th> <th style="width: 15%;">Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disable</td> <td>Range reduction is not performed</td> <td>All</td> </tr> <tr> <td>1h</td> <td>Enable</td> <td>Range reduction is performed</td> <td>All</td> </tr> </tbody> </table> <div style="border: 1px solid black; padding: 5px; margin-top: 5px;"> <p style="text-align: center; color: blue; font-weight: bold;">Programming Notes</p> <p>This field is for Main Profile only. Simple Profile is always disable, and not applicable to Advanced Profile. This field is used in both VLD and IT modes. This is derived by driver from the history of RANGERED and RANGEREDFRM syntax elements (i.e. of forward/preceding reference picture) and those of the current picture. RANGERED is the same as (bPicOverflowBlocks » 3) &amp; 1. RANGEREDFRM is the same as (bPicDeblocked » 5) &amp; 1. For the current picture is a B picture, this field represents the state of the forward/preceding reference picture only. Driver is responsible to keep RangeReductionScale, RangeReduction Enable and RANGERED Present Flag of current picture coherent.</p> </div>			Project:	CHV, BSW	Value	Name	Description	Project	0h	Disable	Range reduction is not performed	All	1h	Enable	Range reduction is performed	All
Project:	CHV, BSW																	
Value	Name	Description	Project															
0h	Disable	Range reduction is not performed	All															
1h	Enable	Range reduction is performed	All															
5	<b>LOOPFILTER Enable Flag</b>	<p>This field is the decoded syntax element LOOPFILTER in bitstream. It indicates if In-loop Deblocking is ON according to picture level bitstream syntax control. This bit affects BSD unit and also the loop filter unit. When this bit is set to 1, PostDeblockOutEnable field in MFX_PIPE_MODE_SELECT command must also be set to 1. In this case, in-loop deblocking operation follows the VC1 standard - deblocking doesn't cross slice boundary. When this bit is set to 0, but PostDeblockOutEnable field in MFX_PIPE_MODE_SELECT command is set to 1. It indicates the loop filter unit is used for out-of-loop deblocking. In this case, deblocking operation does cross slice boundary. This field is used in VLD mode only, not in IT mode.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 50%;">Description</th> <th style="width: 15%;">Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disable</td> <td>Disables loop filter</td> <td>All</td> </tr> <tr> <td>1h</td> <td>Enable</td> <td>Enables loop filter</td> <td>All</td> </tr> </tbody> </table>			Value	Name	Description	Project	0h	Disable	Disables loop filter	All	1h	Enable	Enables loop filter	All		
Value	Name	Description	Project															
0h	Disable	Disables loop filter	All															
1h	Enable	Enables loop filter	All															
4	<b>Overlap Smoothing Enable Flag</b>	<p>This field is the decoded syntax element OVERLAP in bitstream. Indicates if Overlap smoothing is ON at the picture level. This field is used in both VLD and IT modes.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 50%;">Description</th> <th style="width: 15%;">Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disable</td> <td>to disable overlap smoothing filter</td> <td>All</td> </tr> <tr> <td>1h</td> <td>Enable</td> <td>to enable overlap smoothing filter</td> <td>All</td> </tr> </tbody> </table>			Value	Name	Description	Project	0h	Disable	to disable overlap smoothing filter	All	1h	Enable	to enable overlap smoothing filter	All		
Value	Name	Description	Project															
0h	Disable	to disable overlap smoothing filter	All															
1h	Enable	to enable overlap smoothing filter	All															
3	<b>Secondfield</b>	<p>This flag is set for the second field in field pictures. This field is used in both VLD and IT modes.</p>																
2:1	<b>Reserved</b>																	



<b>MFD_VC1_LONG_PIC_STATE</b>			
0	<b>VC1 Profile</b> specifies the bitstream profile. This field is used in both VLD and IT modes.		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0h	Disable	current picture is in Simple or Main Profile (No need to distinguish Simple and Main Profile)
	1h	Enable	current picture is in Advanced Profile
	<b>Programming Notes</b>		
This is required because 128 is added for intra blocks post inverse transform in advanced profile and also to find out if Motion vectors are adjusted or not.			
3	31	<b>Reserved</b>	
	30:29	<b>CondOver</b> This field is the decoded syntax element CONDOVER in a bitstream of advanced profile. It controls the overlap smoothing filter operation for an I frame or an BI frame when the picture level qualization step size PQUANT is 8 or lower. This field is used in intel VC1 VLD mode only, not in DXVA2 VC1 and IT modes.	
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	00b		No overlap smoothing
	01b		Reserved
10b		Always perform overlap smoothing filter	
11b		Overlap smoothing on a per macroblock basis based on OVERFLAGS	
28:26	<b>PicType (Picture Type)</b> This field specifies the coding type of the picture according to the Frame Coding Mode. When FCM = 00   01 (a Progressive or Interlaced Frame Picture): 000 = I001 = P010 = B011 = BI100 = Skipped Other encodings are reserved When FCM = 10   11 (a Field Picture) 000 = I/I001 = I/P010 = P/I011 = P/P100 = B/B101 = B/BI110 = BI/B111 = BI/BIA Although, for a field picture, it is set for a field-pair, but HW will only look at one field state only, and the other field state is don't care. This field is read and qualified with the SecondField flag internally. This field is unique to intel VC1 VLD Long format, and is used in IT mode as well. For DXVA2 VC1 IT mode, driver needs to convert the DXVA2 interface to intel HW VLD Long Format interface.		
25:24	<b>FCM (Frame Coding Mode)</b> This is the same as the variable FCM defined in VC1. This field must be set to 0 for Simple and Main Profiles This field is unique to intel VC1 VLD Long format, and is used in IT mode as well. For DXVA2 VC1 IT mode, driver needs to convert the DXVA2 interface to intel HW VLD Long Format interface.		
<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>
00b	Disable	Progressive Frame Picture	All
01b	Enable	Interlaced Frame Picture	All
10b		Field Picture with Top Field First	
11b		Field Picture with Bottom Field First	

<b>MFD_VC1_LONG_PIC_STATE</b>						
4	23:21	<b>Reserved</b>				
		<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ
	Project:	All				
	Format:	MBZ				
	20:16	<p><b>AltPQuant (Alternative Picture Quantization Value)</b></p> <p>This field is identical to the variable ALTPQUANT which is derived from VOPDQUANT configuration in the VC1 standard. This field must be set to 0 for Simple/Main I and BI pictures as VOPDQUANT is not present. This field is used in intel VC1 VLD Long Format mode only, not used in DXVA2 VC1 VLD and IT modes.</p>				
15:13	<b>Reserved</b>					
	<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ	
Project:	All					
Format:	MBZ					
	12:8	<p><b>PQuant (Picture Quantization Value)</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U5</td> </tr> </table> <p>This is the same as the calculated variable PQUANT in VC1 standard where PQuant = PQINDEX, except when QUANTIZER = 0 and PQINDEX &gt; 8, it is given as PQuant = (PQINDEX &lt; 29) ? PQINDEX - 3 : PQINDEX*2 - 31. This field is used in all picture types (I, P, B and BI) and all operating modes (IT mode and intel and DXVA2 VLD modes).</p>	Project:	All	Format:	U5
	Project:	All				
Format:	U5					
7:0	<p><b>BScaleFactor</b></p> <p>BScaleFactor This field is the scale factor for computing Direct-mode motion vectors. It is derived from the variable BFRACTION in the VC1 standard, section 8.4.5.4. There are only 21 valid values corresponding to the 21 encodings of BFRACTION as shown in the table here. Other values are reserved. MSB of this field can be used to determine if BFRACTION is greater than or equal to 1/2, which is used to determine Motion Prediction Type for B pictures. Effectively, condition "BFRACTION &gt;= 1/2" is equivalent to condition "BScaleFactor &gt;= 128". This field is only valid for B pictures. This field is used only in intel VC1 VLD Long format mode, it is not used in DXVA2 VC1 VLD and IT modes. BFRACTION</p> <p>VLCBFRACTIONBScaleFactor  0001/21280011/3850102/31700111/4641003/41921011/5511102/  510211100003/515311100014/520411100101/64311100115/621511101001/73711101012/  77411101103/711111101114/714811110005/718511110016/722211110101/83211110113/  89611111005/816011111017/8224</p>					
	31:30	<b>Reserved</b>				
		<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ					
	29:28	<p><b>UnifiedMvMode (Unified Motion Vector Mode)</b></p> <p>This field is a combination of the variables MVMODE and MVMODE2 in the VC1 standard, for parsing Luma MVD from the bitstream. This field is used to signal 1MV vs 4MV allowed (Mixed Mode). This field is also used to signal Q-pel or Half-pel MVD read from the bitstream. The bicubic or bilinear Luma MC interpolation mode is duplicate information from Motion Vector Mode field, and is ignored here. This field is used in intel VC1 VLD Long Format mode only, it is not used in DXVA2 VC1 VLD and IT modes.</p>				

<b>MFD_VC1_LONG_PIC_STATE</b>					
		<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>
		00b		Mixed MV, Q-pel bicubic	All
		01b		1-MV, Q-pel bicubic	All
		10b		1-MV half-pel bicubic	
		11b		1-MV half-pel bilinear	
27	<p><b>FourMvSwitch (Four Motion Vector Switch)</b>                      This field indicates if 4-MV is present for an interlaced frame P picture. It is identical to the variable 4MVSWITCH (4 Motion Vector Switch) in VC1 standard. This field is used in intel VC1 VLD Long Format mode only, it is not used in DXVA2 VC1 VLD and IT modes.</p>				
		Value	Name	Description	Project
		0h	Disable	only 1-MV	All
		1h	Enable	1, 2, or 4 MVs	All
26	<p><b>FastUVMCFlag (Fast UV Motion Compensation Flag)</b>                      This field specifies whether the motion vectors for UV is rounded to half or full pel position. It is identical to the variable FASTUVMC in VC1 standard. This field is used in both VLD and IT modes. It is derived from FASTUVMC = (bPicSpatialResid8 » 4) &amp; 1 in both VLD and IT modes, and should have the same value as Motion Vector Mode LSBit.</p>				
		Value	Name	Description	
		0h		no rounding	
		1h		quarter-pel offsets to half/full pel positions	
25	<p><b>RefFieldPicPolarity (Reference Field Picture Polarity)</b>                      This field specifies the polarity of the one reference field picture used for a field P picture. It is derived from the variable REFFIELD defined in VC1 standard and is only valid when one field is referenced (NUMREF = 0) for a field P picture. When NUMREF = 0 and REFFIELD = 0, this field is the polarity of the reference I/P field that is temporally closest; When NUMREF = 0 and REFFIELD = 1, this field is the polarity of the reference I/P field that is the second most temporally closest. The distance is measured based on display order but ignoring the repeated field if present (due to RFF = 1). This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.</p>				
		Value	Name	Description	Project
		0h		Top (even) field	All
		1h		Bottom (odd) field	All
24	<p><b>NumRef (Number of References)</b>                      This field indicates how many reference fields are referenced by the current (field) picture. It is identical to the variable NUMREF in the VC1 standard. This field is only valid for field P picture (FCM = 10   11). This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.</p>				
		Value	Name	Description	
		0h		One field referenced	
		1h		Two fields referenced	

<b>MFD_VC1_LONG_PIC_STATE</b>																	
23:20	<p><b>BwdRefDist (Reference Distance)</b>            This field is valid only in B field pictures giving the value of BRFD. The field is ignored in P Picture. This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.</p>																
19:16	<p><b>FwdRefDist (Reference Distance)</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U4</td> </tr> </table> <p>This field is the number of frames between the current frame and its reference frame. It is derived from the syntax element REFDIST (P Reference Distance) in the VC1 standard. 0 means that the previous frame is the reference frame. It has the same value as of FRFD for both P and B field pictures. This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>[0, 15]</td> <td></td> </tr> </tbody> </table>		Format:	U4	Value	Name	[0, 15]										
Format:	U4																
Value	Name																
[0, 15]																	
15:12	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">MBZ</td> </tr> </table>		Format:	MBZ													
Format:	MBZ																
11:10	<p><b>ExtendedDMVRange (Extended Differential Motion Vector Range Flag)</b>            This field specifies the differential motion vector range in interlaced pictures. It is equivalent to the variable DMVRANGE in the VC1 standard. This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 20%;">Value</th> <th style="width: 20%;">Name</th> <th style="width: 60%;">Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td></td> <td>No extended range</td> </tr> <tr> <td>01b</td> <td></td> <td>Extended horizontally</td> </tr> <tr> <td>10b</td> <td></td> <td>Extended vertically</td> </tr> <tr> <td>11b</td> <td></td> <td>Extended in both directions</td> </tr> </tbody> </table>		Value	Name	Description	00b		No extended range	01b		Extended horizontally	10b		Extended vertically	11b		Extended in both directions
Value	Name	Description															
00b		No extended range															
01b		Extended horizontally															
10b		Extended vertically															
11b		Extended in both directions															
9:8	<p><b>ExtendedMVRRange (Extended Motion Vector Range Flag)</b>            This field specifies the motion vector range in quarter-pel or half-pel modes. It is equivalent to the variable MVRANGE in the VC1 standard. This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 20%;">Value</th> <th style="width: 20%;">Name</th> <th style="width: 60%;">Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td></td> <td>[-256, 255] x [-128, 127]</td> </tr> <tr> <td>01b</td> <td></td> <td>512, 511] x [-256, 255]</td> </tr> <tr> <td>10b</td> <td></td> <td>[-2048, 2047] x [-1024, 1023]</td> </tr> <tr> <td>11b</td> <td></td> <td>[-4096, 4095] x [-2048, 2047]</td> </tr> </tbody> </table>		Value	Name	Description	00b		[-256, 255] x [-128, 127]	01b		512, 511] x [-256, 255]	10b		[-2048, 2047] x [-1024, 1023]	11b		[-4096, 4095] x [-2048, 2047]
Value	Name	Description															
00b		[-256, 255] x [-128, 127]															
01b		512, 511] x [-256, 255]															
10b		[-2048, 2047] x [-1024, 1023]															
11b		[-4096, 4095] x [-2048, 2047]															
7:4	<p><b>AltPQuantEdgeMask (Alternative Picture Quantization Edge Mask)</b>            This field is a bit mask for the four edges in clock-wise order, indicating whether AltPQuant is used for the edge macroblocks. It is derived based on the following variables DQUANT, DQUANTFRM, DQPROFILE, DQSBEDGE, DQDBEDGE, and DQBILEVEL defined in the VC1 standard, as shown in Error! Reference source not found.. This field is valid only if AltPQuantConfig is 01. Bit 0: Left picture edge macroblocks Bit 1: Top picture edge macroblocks Bit 2: Right picture edge macroblocks Bit 3: Bottom picture edge macroblocks This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.</p>																

<b>MFD_VC1_LONG_PIC_STATE</b>																					
3:2	<p><b>AltPQuantConfig (Alternative Picture Quantization Configuration)</b></p> <p>This field specifies the way AltPQuant is used in the picture. It determines how to compute the macroblock quantizer step size, MQANT. It is derived based on the following variables DQUANT, DQUANTFRM, DQPROFILE, DQSBEDGE, DQDBEDGE, and DQBILEVEL defined in the VC1 standard, as shown in Error! Reference source not found..This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 10%;">Name</th> <th style="width: 60%;">Description</th> <th style="width: 10%;">Project</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td></td> <td>AltPQuant not used</td> <td>All</td> </tr> <tr> <td>01b</td> <td></td> <td>AltPQuant is used and applied to edge macroblocks only</td> <td>All</td> </tr> <tr> <td>10b</td> <td></td> <td>MQANT is encoded in macroblock layer</td> <td></td> </tr> <tr> <td>11b</td> <td></td> <td>AltPQuant and PQuant are selected on macroblock basis</td> <td></td> </tr> </tbody> </table>	Value	Name	Description	Project	00b		AltPQuant not used	All	01b		AltPQuant is used and applied to edge macroblocks only	All	10b		MQANT is encoded in macroblock layer		11b		AltPQuant and PQuant are selected on macroblock basis	
	Value	Name	Description	Project																	
	00b		AltPQuant not used	All																	
	01b		AltPQuant is used and applied to edge macroblocks only	All																	
	10b		MQANT is encoded in macroblock layer																		
11b		AltPQuant and PQuant are selected on macroblock basis																			
1	<p><b>HalfQP</b></p> <p>This field is used for inverse quantization of AC coefficients. It is valid only when PQuant is used.This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.</p>																				
0	<p><b>PQuantUniform</b></p> <p>Indicating if uniform quantization applies to the picture. It is used for inverse quantization of the AC coefficients.QUANTIZER 001123PQUANTIZER - 01--PQINDEX&gt;=9&lt;=8----</p> <p>PQuantUniform010201ImplicitQuantizer = 0, and PQuantUniform = 0 is used to represent 2 cases : 1) QUANTIZER=01 and PQUANTIZER=0; and 2) QUANTIZER = 10b.ImplicitQuantizer = 0, and PQuantUniform = 1 is used to represent 2 cases : 1) QUANTIZER=01 and PQUANTIZER=1; and 2) QUANTIZER = 11bThis field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 10%;">Name</th> <th style="width: 60%;">Description</th> <th style="width: 10%;">Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td></td> <td>Non-uniform</td> <td>All</td> </tr> <tr> <td>1h</td> <td></td> <td>Uniform</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	0h		Non-uniform	All	1h		Uniform	All								
Value	Name	Description	Project																		
0h		Non-uniform	All																		
1h		Uniform	All																		
5	31	<p><b>BitplanePresentFlag (Bitplane Buffer Present Flag)</b></p> <p>This field indicates whether the bitplane buffer is present for the picture. If set, at least one of the fields listed in bits 22:16 is coded in non-raw mode, and Bitplane Buffer Base Address field in the VC1_BSD_BUF_BASE_STATE command points to the bitplane buffer. Otherwise, all the fields that are applicable for the current picture in bits 22:16 must be coded in raw mode.This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 10%;">Name</th> <th style="width: 60%;">Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td></td> <td>bitplane buffer is not present</td> </tr> <tr> <td>1h</td> <td></td> <td>bitplane buffer is present</td> </tr> </tbody> </table>	Value	Name	Description	0h		bitplane buffer is not present	1h		bitplane buffer is present										
	Value	Name	Description																		
	0h		bitplane buffer is not present																		
1h		bitplane buffer is present																			
30	<p><b>ForwardMbRaw</b></p> <p>This field indicates whether the FORWARDMB field is coded in raw or non-raw mode.This field is only valid when PictureType is B.This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.</p>																				

## MFD\_VC1\_LONG\_PIC\_STATE

		Value	Name	Description
		0h		non-raw mode
		1h		raw mode
29	<b>MvTypeMbRaw</b> This field indicates whether the MVTYPREMB field is coded in raw or non-raw mode. This field is only valid when PictureType is P. This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.			
		Value	Name	Description
		0h		Non-Raw Mode
		1h		Raw Mode
28	<b>SkipMbRaw</b> This field indicates whether the SKIPMB field is coded in raw or non-raw mode. This field is only valid when PictureType is P or B. 0 = non-raw mode 1 = raw mode This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.			
		Value	Name	Description
		0h	Disable	Non-Raw Mode
		1h	Enable	Raw Mode
27	<b>DirectMbRaw</b> This field indicates whether the DIRECTMB field is coded in raw or non-raw mode. This field is only valid when PictureType is P or B. This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.			
		Value	Name	Description
		0h		Non-Raw Mode
		1h		Raw Mode
26	<b>OverflagsRaw</b> This field indicates whether the OVERFLAGS field is coded in raw or non-raw mode. This field is only valid when PictureType is I or BI. This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.			
		Value	Name	Description
		0h		Non-Raw Mode
		1h		Raw Mode
25	<b>AcPredRaw</b> This field indicates whether the ACPRED field is coded in raw or non-raw mode. This field is only valid when PictureType is I or BI. This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.			
		Value	Name	Description
		0h	Disable	Non-Raw Mode
		1h	Enable	Raw Mode

## MFD\_VC1\_LONG\_PIC\_STATE

24	<b>FieldTxRaw</b>	<p>This field indicates whether the FIELDTX field is coded in raw or non-raw mode. This field is only valid when PictureType is I or BI. This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 25%;">Value</th> <th style="width: 30%;">Name</th> <th style="width: 45%;">Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disable</td> <td>Non-Raw Mode</td> </tr> <tr> <td>1h</td> <td>Enable</td> <td>Raw Mode</td> </tr> </tbody> </table>	Value	Name	Description	0h	Disable	Non-Raw Mode	1h	Enable	Raw Mode
Value	Name	Description									
0h	Disable	Non-Raw Mode									
1h	Enable	Raw Mode									
23	<b>Reserved</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ					
Project:	All										
Format:	MBZ										
22:20	<b>MvTab (Motion Vector Table)</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U3</td> </tr> </table> <p>This field specifies which motion vector table(s) is (are) used for motion vector (differential) decoding in a P or B picture. This field is the combination of the variables MVTAB and IMVTAB in the VC1 standard. Two bits are defined for progressive frame pictures; And two or three bits are defined for interlaced field/frame pictures depending on NUMREF and P or B picture types. This field is valid for P and B pictures. It is not valid for I pictures. For P or B progressive frame pictures 0 = Motion Vector Differential VLD Table 01 = Motion Vector Differential VLD Table 12 = Motion Vector Differential VLD Table 23 = Motion Vector Differential VLD Table 3 The other encodings are reserved For P interlace field pictures with NUMREF = 0 or P/B interlace frame pictures 0 = 1-Reference Table 01 = 1-Reference Table 12 = 1-Reference Table 23 = 1-Reference Table 3 The other encodings are reserved For P interlace field picture with NUMREF = 1 or B interlaced field pictures 0 = 2-Reference Table 01 = 2-Reference Table 12 = 2-Reference Table 23 = 2-Reference Table 34 = 2-Reference Table 45 = 2-Reference Table 56 = 2-Reference Table 67 = 2-Reference Table 7 The other encodings are reserved This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.</p>	Project:	All	Format:	U3					
Project:	All										
Format:	U3										
19:18	<b>FourMvBpTab (4-MV Block Pattern Table)</b>	<p>This field specifies which table is used to decode the 4-MV block pattern (4MVBP) syntax element in 4-MV macroblocks. It is identical to the variables 4MVBPTAB in the VC1 standard, section 9.1.1.37. This field is valid only in interlace frame P, B pictures, or interlace field P, B pictures. It is not valid for I picture. For interlace field P and B pictures, it is only valid if UnifiedMvMode is equal to Mixed-MV Type. For interlace frame P picture, it is only valid if FourMvSwitch is 1. For interlace frame B picture, it is always valid. 0 = 4MVBP Table 01 = 4MVBP Table 12 = 4MVBP Table 23 = 4MVBP Table 3 This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.</p>									
17:16	<b>TwoMvBpTab (2MV Block Pattern Table)</b>	<p>This field specifies which table is used to decode the 2MV block pattern (2MVBP) syntax element in 2MV field macroblocks. It is identical to the variables 2MVBPTAB in the VC1 standard, section 9.1.1.36. This field is valid only in interlace frame P/B pictures. It is not valid for I picture, nor for interlace field P or B pictures. 0 = 2MVBP Table 01 = 2MVBP Table 12 = 2MVBP Table 23 = 2MVBP Table 3 This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.</p>									

<b>MFD_VC1_LONG_PIC_STATE</b>											
15:14	<b>Reserved</b>										
	Project:	All									
	Format:	MBZ									
13:12	<b>TransType (Picture-level Transform Type)</b>										
	Project:	All									
	Format:	U2									
<p>This field specifies the Transform Type at picture level. It is identical to the variable TTFRM in the VC1 standard, section 7.1.1.41. This field is only valid when TransTypeMbFlag is 1. Otherwise, it is reserved and MBZ. This field is set to 00 when VSTRANSFORM is 0 in the entry point layer. 00 = 8x8 Transform 01 = 8x4 Transform 10 = 4x8 Transform 11 = 4x4 Transform This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.</p>											
11	<b>TransTypeMbFlag (Macroblock Transform Type Flag)</b>										
	<p>This field indicates whether Transform Type is fixed at picture level or variable at macroblock level. It is identical to the variable TTMBF in the VC1 standard, section 7.1.1.40. This field is set to 1 when VSTRANSFORM is 0 in the entry point layer. This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.</p>										
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td></td> <td>variable transform type in macroblock layer</td> </tr> <tr> <td>1h</td> <td></td> <td>use picture level transform type TransType</td> </tr> </tbody> </table>	Value	Name	Description	0h		variable transform type in macroblock layer	1h		use picture level transform type TransType	
Value	Name	Description									
0h		variable transform type in macroblock layer									
1h		use picture level transform type TransType									
10:8	<b>MbModeTab (Macroblock Mode Table)</b>										
	<p>This field signals which code table is used to decode the macroblock mode syntax element (MBMODE) in the macroblock layer in a P or B picture. This field is identical to the variables MBMODETAB in the VC1 standard, section 9.1.1.33. This field is valid for interlace frame P, B picture and interlace field P, B picture. It is not valid for I picture, nor progressive frame P, B pictures. Two bits are defined for interlace frame P, B pictures; And three bits are defined for interlaced field P, B pictures. Two bits are defined for interlace frame P, B pictures. There are two set of code tables selected based on if UnifiedMvMode is equal to 4-MV Type or not. 0 = Code Table 01 = Code Table 12 = Code Table 23 = Code Table 30 Other encodings are invalid Three bits are defined for interlace field P, B pictures. There are two set of code tables selected based on if UnifiedMvMode is equal to Mixed-MV Type or not. 0 = Code Table 01 = Code Table 12 = Code Table 23 = Code Table 34 = Code Table 45 = Code Table 56 = Code Table 67 = Code Table 7 This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.</p>										
7:6	<b>TransAcY (Picture-level Transform Luma AC Coding Set Index, TRANSACTABLE2)</b>										
	BitFieldDesc										
5:4	<b>TransAcUV (Picture-level Transform Chroma AC Coding Set Index, TRANSACTABLE)</b>										
	<p>This field, together with PQINDEX, specifies which intra AC coding set to be used for decoding the non-zero AC coefficients in a coded luma (Y) block. This field is the combination of the variables TRANSACFRM and TRANSACFRM2 in the VC1 standard. For I pictures, TransAcY is the same as TRANSACFRM2. For other pictures, it is the same as TRANSACFRM, and therefore must be programmed to be the same as TransAcUV. This field is valid for all picture types. 0 = Coding set index 01 = Coding set index 12 = Coding set index 23 is invalid This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.</p>										



<b>MFD_VC1_LONG_PIC_STATE</b>															
3	<p><b>TransDcTab (Intra Transform DC Table)</b></p> <p>This field specifies whether the low motion tables or the high motion tables are used to decode the Transform DC coefficients in intra-coded blocks. This field is identical to the variable TRANSDCTAB in the VC1 standard, section 8.1.1.2. This field is valid for all picture types. This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> <th style="text-align: center;">Project</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0h</td> <td></td> <td>The high motion tables</td> <td style="text-align: center;">All</td> </tr> <tr> <td style="text-align: center;">1h</td> <td></td> <td>The low motion tables</td> <td style="text-align: center;">All</td> </tr> </tbody> </table>	Value	Name	Description	Project	0h		The high motion tables	All	1h		The low motion tables	All		
Value	Name	Description	Project												
0h		The high motion tables	All												
1h		The low motion tables	All												
2:0	<p><b>CbpTab (Coded Block Pattern Table)</b></p> <p>This field specifies the table used to decode the CBPCY syntax element for each coded macroblock in P and B pictures. This field is combination of the variable CBPTAB for P and B frame pictures and the variable ICBPTAB in interlace field P, B pictures and interlace frame P, B pictures in the VC1 standard (Table 52 and Table 102). This field is reserved and MBZ for I or BI pictures as I only has a fixed table. 000 = Table 0 (Table 169 for P, B frames or Table 124 otherwise) 001 = Table 1 (Table 170 for P, B frames or Table 125 otherwise) 010 = Table 2 (Table 171 for P, B frames or Table 126 otherwise) 011 = Table 3 (Table 172 for P, B frames or Table 127 otherwise) 100 = Table 4 (Table 128 for interlace field/frame P, B pictures) 101 = Table 5 (Table 129 for interlace field/frame P, B pictures) 110 = Table 6 (Table 130 for interlace field/frame P, B pictures) 111 = Table 7 (Table 131 for interlace field/frame P, B pictures) This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.</p>														

## MFD\_VC1\_SHORT\_PIC\_STATE

<b>MFD_VC1_SHORT_PIC_STATE</b>			
Project:		CHV, BSW	
Source:		VideoCS	
Length Bias:		2	
D Wo rd	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h MFD_VC1_SHORT_PIC_STATE
		Format:	OpCode
	26:24	<b>Media Command Opcode</b>	
		Default Value:	2h VC1_DEC
		Format:	OpCode
	23:21	<b>SubOpcode A</b>	
Default Value:		1h	
Format:		OpCode	
20:16	<b>SubOpcode B</b>		
	Default Value:	0h	
	Format:	OpCode	
15:12	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
11:0	<b>DWord Length</b>		
	Default Value:	0003h Excludes DWord (0,1)	
	Project:	All	
	Format:	=n Total Length - 2	
1	31:24	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	23:16	<b>Picture Height</b>	
Format:	U8-1 Picture Height in Macroblocks		
This field indicates the height of the picture in unit of macroblocks. For example, for a 1920x1080			

<b>MFD_VC1_SHORT_PIC_STATE</b>											
	<p>frame picture, PictureHeightInMBs equals 68 (1080 divided by 16, and rounded up, i.e. effectively specified as 1088 instead).This field is used in VLD and IT modes.Note: Even though the Advanced Profile allows frame dimensions (width, height) to not be aligned to macroblock boundary, it doesn't affect the bitstream decoding. And it is preferable to use 'intermediate buffer' that is macroblock aligned for decoding. In order to simplify the out-of-bound reference pixel access, the out-of-bound extrapolation rule in VC1 spec can be used to expand the expected decoded frame to the intermediate buffer dimension.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>[0,127]</td> <td>Value_0_to_127</td> <td>[1, 128] MB</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Value	Name	Description	Project	[0,127]	Value_0_to_127	[1, 128] MB	CHV, BSW		
Value	Name	Description	Project								
[0,127]	Value_0_to_127	[1, 128] MB	CHV, BSW								
15:8	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ						
Project:	All										
Format:	MBZ										
7:0	<p><b>Picture Width</b></p> <table border="1"> <tr> <td>Format:</td> <td>U8-1 Picture Width in Macroblocks</td> </tr> </table> <p>This field indicates the width of the picture in unit of macroblocks. For example, for a 1920x1080 frame picture, PictureWidthInMBs equals 120 (1920 divided by 16).This field is used in VLD and IT modes.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>[0,127]</td> <td>Value_0_to_127</td> <td>[1, 128] MB</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Format:	U8-1 Picture Width in Macroblocks	Value	Name	Description	Project	[0,127]	Value_0_to_127	[1, 128] MB	CHV, BSW
Format:	U8-1 Picture Width in Macroblocks										
Value	Name	Description	Project								
[0,127]	Value_0_to_127	[1, 128] MB	CHV, BSW								
2	<p>31:24 <b>Bitplane Buffer Pitch Minus 1</b></p> <table border="1"> <tr> <td>Format:</td> <td>U7-1 Pitch in Bytes</td> </tr> </table> <p>Specifies the bitplane buffer pitch in (#Bytes - 1). Bitplane buffer is a linear buffer. It is needed only when the bitplane is not encoded as raw, and therefore is present in the header explicitly. In VC1 Long Format (Gen6 and Gen7), it is written by an application and later read by the HW. In VC1 Long Format (Gen6 and Gen7), it is written by an application, and later read by the HW. But in VC1 Short Format (Gen7 only), it is written and read by H/W only.This field is specified for better performanceFor Gen6 : The pitch must be equal to PictureWidthInMBs/2.For Gen7 VC1 Long Format : The pitch must be equal to PictureWidthInMBs/2.For Gen7 VC1 Short Format : If Pic Width is less than or equal to 2K pixels, bitplane pitch is set to 64 (one cacheline; programmed as 63) bytes per MB row. If Pic Width is greater than 2K pixels, bitplane pitch is set to 128 (two cachelines; programmed as 127) bytes per MB row.This field is not used in IT mode, used in VLD mode only.For VC1 DXVA2 Short Format, the bitplane specification is between H/W and Driver only. For Long Format, application is responsible for allocation with the driver.</p>	Format:	U7-1 Pitch in Bytes								
Format:	U7-1 Pitch in Bytes										
	<p>23 <b>Interpolation Rounder Control</b></p> <p>Used only in MC operation. This field specifies the rounding control value used in interpolation operation of motion prediction process. Note: This bit field is taken from bRcontrol in DXVA_PictureParameters data structure This field is used in VLD and IT modes.</p>										
	<p>22:20 <b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ						
Project:	All										
Format:	MBZ										

## MFD\_VC1\_SHORT\_PIC\_STATE

19:16	<b>Motion Vector Mode</b>	<p>This field indicates one of the following motion compensation interpolation modes for P and B pictures. The MC interpolation modes apply to prediction values of luminance blocks and are always in quarter-sample. For chrominance blocks, it always performs bilinear interpolation with either half-pel or quarter-pel precision. 0XX0 = Chroma Quarter -pel + Luma bicubic. (can only be 1MV) 0XX1 = Chroma Half-pel + Luma bicubic. (can be 1MV or 4MV) 1XX0 = Chroma Quarter -pel + Luma bilinear. (can only be 1MV) 1XX1 = Chroma Half-pel + Luma bilinear. Note: Bits 19:16 are taken from bMVprecisionAndChromaRelation in DXVA_PictureParameters data structure. Bit 19 of Motion Vector Mode = 1 for Luma Bilinear MC; = 0 for Luma Bicubic MC. Bit 16 of Motion Vector Mode = 1 for half-sample Chroma motion = 0 for quarter-sample Chroma motion. This field is used in both VLD and IT modes.</p>												
15	<b>DmvSurfaceValid</b>	<p>Indicated when the DMV read surface is valid. This surface stored the direct motion vectors. This field is set fo B pictures that can refer to a previous P picture for DMV. If there is an I-picture before a B (in decoding order) then this field is not set (as a result, zero's DMV's will be assumed while decoding the B picture. That is, there is no explicit DMV buffer for an I-picture). This field is not used in IT mode, used in VLD mode only.</p>												
14:12	<b>Reserved</b>													
11	<b>VC1 Profile</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Project:</td> <td style="width: 30%;">All</td> </tr> </table> <p>specifies the bitstream profile. Note: This is required because 128 is added for intra blocks post inverse transform in advanced profile and also to find out if Motion vectors are adjusted or not. This field is used in both VLD and IT modes.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #e1eef6;"> <th style="width: 10%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 75%;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0h</td> <td style="text-align: center;"><b>[Default]</b></td> <td>current picture is in Simple or Main Profile (No need to distinguish Simple and Main Profile)</td> </tr> <tr> <td style="text-align: center;">1h</td> <td></td> <td>current picture is in Advanced Profile</td> </tr> </tbody> </table>		Project:	All	Value	Name	Description	0h	<b>[Default]</b>	current picture is in Simple or Main Profile (No need to distinguish Simple and Main Profile)	1h		current picture is in Advanced Profile
Project:	All													
Value	Name	Description												
0h	<b>[Default]</b>	current picture is in Simple or Main Profile (No need to distinguish Simple and Main Profile)												
1h		current picture is in Advanced Profile												
10:6	<b>Reserved</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Project:</td> <td style="width: 30%;">All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>		Project:	All	Format:	MBZ							
Project:	All													
Format:	MBZ													
5	<b>Backward Prediction Present Flag</b>	<p>Note : a B picture that only uses forward prediction may have this flag set to 1 as well. Driver may still need to provide a valid reference picture index. This field is used in both DXVA2 VC1 VLD mode and IT mode. It is the same parameter as bPicBackwardPrediction in DXVA2 VC1 spec. The Intra Picture Flag, Backward Prediction Present Flag and RefPicFlag are used to derive the picture type, as specified in PTYPE for a frame, and in FPTYPE for a field, in DXVA2 VC1 VLD and IT mode.</p>												
4	<b>Intra Picture Flag</b>	<p>This field is used in both DXVA2 VC1 VLD mode and IT mode. It is the same parameter as bPicIntra in DXVA2 VC1 spec. The Intra Picture Flag, Backward Prediction Present Flag and RefPicFlag are used to derive the picture type, as specified in PTYPE for a frame, and in FPTYPE for a field, in DXVA2 VC1 VLD and IT mode.</p>												

<b>MFD_VC1_SHORT_PIC_STATE</b>				
	<b>Value</b>	<b>Name</b>	<b>Description</b>	
	0h		entire picture can have a mixture of intra and inter MB type or just inter MB type.	
	1h		entire picture is coded in intra MB type	
3	<b>SecondField</b> This flag is set for the second field in field pictures. This field is used in both VLD and IT modes.			
2	<b>Reserved</b>			
	Project:		All	
	Format:		MBZ	
1:0	<b>Picture Structure</b> This field is used in both DXVA2 VC1 VLD mode and IT mode. It is the same parameter as bPicStructure in DXVA2 VC1 spec. The Picture Structure and Progressive Pic Type are used to derive the picture structure as specified in FCM, in DXVA2 VC1 VLD and IT mode.			
	<b>Value</b>	<b>Name</b>	<b>Description</b>	
	01b		top field (bit 0)	
	10b		bottom field (bit 1)	
	11b		frame (both fields are present)	
	00b		illegal	
3	31	<b>Reserved</b>		
	Project:		All	
	Format:		MBZ	
	30	<b>Overlap Smoothing Enable Flag</b> This field is the decoded syntax element OVERLAP in bitstream. Indicates if Overlap smoothing is ON at the picture level. This field is used in both VLD and IT modes.		
	<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>
	0h	Disable	to disable overlap smoothing filter	All
	1h	Enable	to enable overlap smoothing filter	All
	29	<b>Range Reduction Scale</b>		
	Project:		All	
	Access:		None	
	This field specifies whether the reference picture pixel values should be scaled up or scaled down on-the-fly, if RangeReduction is Enabled. NOTE: This bit is derived by driver for Main Profile only. Ignored in Simple and Advanced Profiles. This field is used in both VLD and IT modes. This is derived by driver from the history of RANGERED and RANGEREDFRM syntax elements (i.e. of forward/preceding reference picture) and those of the current picture. RANGERED is the same as (bPicOverflowBlocks » 3) & 1. RANGEREDFRM is the same as (bPicDeblocked » 5) & 1. For the current picture is a B picture, this field represents the state of the forward/preceding reference picture only. Driver is responsible to keep RangeReductionScale, RangeReduction Enable and RANGERED Present Flag of current picture coherent.			

<b>MFD_VC1_SHORT_PIC_STATE</b>																								
	<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>																				
	0h	Disable <b>[Default]</b>	Scale down reference picture by factor of 2	All																				
	1h	Enable	Scale up reference picture by factor of 2	All																				
28	<p><b>Range Reduction Enable</b></p> <p>This field specifies whether on-the-fly pixel value range reduction should be performed for the preceding (or forward) reference picture. Along with RangeReductionScale to specify whether scale up or down should be performed. It is not the same value as RANGEREDFRM Syntax Element (DXVA_PictureParameters bPicDeblocked bit 5) in the Picture Header. This field is for Main Profile only. Simple Profile is always disable, and not applicable to Advanced Profile. This field is used in both VLD and IT modes. This is derived by driver from the history of RANGERED and RANGEREDFRM syntax elements (i.e. of forward/preceding reference picture) and those of the current picture. RANGERED is the same as (bPicOverflowBlocks » 3) &amp; 1. RANGEREDFRM is the same as (bPicDeblocked » 5) &amp; 1. For the current picture is a B picture, this field represents the state of the forward/preceding reference picture only. Driver is responsible to keep RangeReductionScale, RangeReduction Enable and RANGERED Present Flag of current picture coherent.</p> <table border="1"> <thead> <tr> <th><b>Value</b></th> <th><b>Name</b></th> <th><b>Description</b></th> <th><b>Project</b></th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disable <b>[Default]</b></td> <td>Range reduction is not performed</td> <td>All</td> </tr> <tr> <td>1h</td> <td>Enable</td> <td>Range reduction is performed</td> <td>All</td> </tr> </tbody> </table>				<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>	0h	Disable <b>[Default]</b>	Range reduction is not performed	All	1h	Enable	Range reduction is performed	All								
<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>																					
0h	Disable <b>[Default]</b>	Range reduction is not performed	All																					
1h	Enable	Range reduction is performed	All																					
27:24	<b>Reserved</b>																							
23:22	<p><b>Progressive Pic Type</b></p> <p>This field is used in both DXVA2 VC1 VLD mode and IT mode. It is the same parameter as bPicExtrapolation in DXVA2 VC1 spec. The Picture Structure and Progressive Pic Type are used to derive the picture structure as specified in FCM, in DXVA2 VC1 VLD and IT mode.</p> <table border="1"> <thead> <tr> <th><b>Value</b></th> <th><b>Name</b></th> <th><b>Description</b></th> <th><b>Project</b></th> </tr> </thead> <tbody> <tr> <td>0</td> <td></td> <td>progressive only picture</td> <td>All</td> </tr> <tr> <td>1</td> <td></td> <td>progressive only picture</td> <td>All</td> </tr> <tr> <td>2</td> <td></td> <td>interlace picture (frame-interlace or field-interlace)</td> <td></td> </tr> <tr> <td>3</td> <td></td> <td>illegal</td> <td></td> </tr> </tbody> </table>				<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>	0		progressive only picture	All	1		progressive only picture	All	2		interlace picture (frame-interlace or field-interlace)		3		illegal	
<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>																					
0		progressive only picture	All																					
1		progressive only picture	All																					
2		interlace picture (frame-interlace or field-interlace)																						
3		illegal																						
21	<b>Reserved</b>																							
20:16	<p><b>P-Pic Ref Distance</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Access:</td> <td>None</td> </tr> </table> <p>This element defines the number of frames between the current frame and the reference frame. It is the same as the REFDIST SE in VC1 interlaced field picture header. It is present if the entry-level flag REFDIST_FLAG == 1, and if the picture type is not one of the following types: B/B, B/BI, BI/B, BI/BI. If the entry level flag REFDIST_FLAG == 0, REFDIST shall be set to the default value of 0. This field is used in DXVA2 VC1 VLD mode only, not used in IT and intel VC1 VLD Long Format modes.</p> <table border="1"> <thead> <tr> <th><b>Value</b></th> <th><b>Name</b></th> </tr> </thead> <tbody> <tr> <td>0-16</td> <td>unsigned integer</td> </tr> <tr> <td>0h</td> <td><b>[Default]</b></td> </tr> </tbody> </table>				Project:	All	Access:	None	<b>Value</b>	<b>Name</b>	0-16	unsigned integer	0h	<b>[Default]</b>										
Project:	All																							
Access:	None																							
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0-16	unsigned integer																							
0h	<b>[Default]</b>																							

<b>MFD_VC1_SHORT_PIC_STATE</b>			
15:14	<b>QUANTIZER</b>		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	00b		implicit quantizer at frame leve
	01b		explicit quantizer at frame level, and use PQUANTIZER SE to specify uniform or non-uniform
	10b		explicit quantizer, and non-uniform quantizer for all frames
11b		explicit quantizer, and uniform quantizer for all frames	
13	<b>MULTIRES Present Flag (for Simple/Main Profile only)</b>		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0h		RESPIC Parameter is present in the picture header
1h		RESPIC Parameter is present in the picture header	
12	<b>SYNCMARKER Present Flag (for Simple/Main Profile only)</b>		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0		Bitstream for Simple and Main Profile has no sync marker
1		Bitstream for Simple and Main Profile may have sync marker(s)	
11	<b>RANGERED Present Flag (for Simple/Main Profile only)</b>		
	It is needed for Picture Header Parsing.Driver is responsible to keep RangeReductionScale, RangeReduction Enable and RANGERED Present Flag of current picture coherent.		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
0		Range Reduction Parameter (RANGEREDFRM) is not present in the picture header	
1		Range Reduction Parameter (RANGEREDFRM) is present in the picture header.	
10:8	<b>MAXBFRAMES</b>		
Number of consecutive B Frames.			
7	<b>PANSCAN Present Flag</b>		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0		Pan Scan Parameters are not present in the picture header
1		Pan Scan Parameters are present in the picture header	
6	<b>REFDIST_FLAG</b>		
For header parsing REFDIST.This is used in DXVA2 VC1 VLD mode only, not used in IT and intel VC1 VLD modes.			
5	<b>LOOPFILTER Enable Flag</b>		
This filed is the decoded syntax element LOOPFILTER in bitstream. It indicates if In-loop Deblocking is ON according to picture level bitstream syntax control. This bit affects BSD unit and also the loop filter unit.When this bit is set to 1, PostDeblockOutEnable field in MFX_PIPE_MODE_SELECT command must also be set to 1. In this case, in-loop deblocking operation follows the VC1 standard - deblocking doesn't cross slice boundary.When this bit is set to 0, but PostDeblockOutEnable field in MFX_PIPE_MODE_SELECT command is set to 1. It indicates the loop filter unit is used for out-of-loop deblocking. In this case, deblocking operation does cross slice boundary.This field is used in VLD mode only, not in IT mode.			

<b>MFD_VC1_SHORT_PIC_STATE</b>																											
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td></td> <td>In-Loop-Deblocking-Filter is disabled</td> </tr> <tr> <td>1</td> <td></td> <td>In-Loop-Deblocking-Filter is enabled</td> </tr> </tbody> </table>	Value	Name	Description	0		In-Loop-Deblocking-Filter is disabled	1		In-Loop-Deblocking-Filter is enabled																
Value	Name	Description																									
0		In-Loop-Deblocking-Filter is disabled																									
1		In-Loop-Deblocking-Filter is enabled																									
4		<p><b>FastUVMCFlag (Fast UV Motion Compensation Flag)</b>            This field specifies whether the motion vectors for UV is rounded to half or full pel position. It is identical to the variable FASTUVMC in VC1 standard. This field is used in both VLD and IT modes. It is derived from <math>FASTUVMC = (bPicSpatialResid8 \gg 4) \&amp; 1</math> in both VLD and IT modes, and should have the same value as Motion Vector Mode LSBit.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td></td> <td>no rounding</td> <td>All</td> </tr> <tr> <td>1h</td> <td></td> <td>quarter-pel offsets to half/full pel positions</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	0h		no rounding	All	1h		quarter-pel offsets to half/full pel positions	All													
Value	Name	Description	Project																								
0h		no rounding	All																								
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3		<p><b>EXTENDED_MV Present Flag</b>            BitFieldDesc</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td></td> <td>Extended_MV is not present in the picture header</td> <td>All</td> </tr> <tr> <td>1h</td> <td></td> <td>Extended_MV is present in the picture header</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	0h		Extended_MV is not present in the picture header	All	1h		Extended_MV is present in the picture header	All													
Value	Name	Description	Project																								
0h		Extended_MV is not present in the picture header	All																								
1h		Extended_MV is present in the picture header	All																								
2:1		<p><b>DQUANT</b></p> <table border="1"> <tbody> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Access:</td> <td>None</td> </tr> <tr> <td>Format:</td> <td>U2</td> </tr> </tbody> </table> <p>Use for Picture Header Parsing of VOPDUANT elements</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>[Default]</td> <td></td> </tr> <tr> <td>00b</td> <td></td> <td>no VOPDQUANT elements; Quantizer cannot vary in frame, same quantization step size PQUANT is used for all MBs in the frame</td> </tr> <tr> <td>01b</td> <td></td> <td>refer to VC1 Spec. for all the MB position dependent quantizer selection</td> </tr> <tr> <td>10b</td> <td></td> <td>The macroblocks located on the picture edge boundary shall be quantized with ALTPQUANT while the rest of the macroblocks shall be quantized with PQUANT.</td> </tr> <tr> <td>11b</td> <td>Reserved</td> <td></td> </tr> </tbody> </table>	Project:	All	Access:	None	Format:	U2	Value	Name	Description	0h	[Default]		00b		no VOPDQUANT elements; Quantizer cannot vary in frame, same quantization step size PQUANT is used for all MBs in the frame	01b		refer to VC1 Spec. for all the MB position dependent quantizer selection	10b		The macroblocks located on the picture edge boundary shall be quantized with ALTPQUANT while the rest of the macroblocks shall be quantized with PQUANT.	11b	Reserved		
Project:	All																										
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0		<p><b>VSTRANSFORM flag</b></p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disable</td> <td>variable-sized transform coding is not enabled</td> </tr> <tr> <td>1h</td> <td>Enable</td> <td>variable-sized transform coding is enabled</td> </tr> </tbody> </table>	Value	Name	Description	0h	Disable	variable-sized transform coding is not enabled	1h	Enable	variable-sized transform coding is enabled																
Value	Name	Description																									
0h	Disable	variable-sized transform coding is not enabled																									
1h	Enable	variable-sized transform coding is enabled																									
4	31:29	<p><b>Reserved</b></p> <table border="1"> <tbody> <tr> <td>Format:</td> <td>MBZ (for possible future change to BFraction Enumeration)</td> </tr> </tbody> </table>	Format:	MBZ (for possible future change to BFraction Enumeration)																							
Format:	MBZ (for possible future change to BFraction Enumeration)																										
	28:24	<b>BFraction Enumeration</b>																									



## MFD\_VC1\_SHORT\_PIC\_STATE

	<p>This field is the scale factor for computing Direct-mode motion vectors. It is derived from the variable BFACTION in the VC1 standard, section 8.4.5.4. There are only 21 valid values corresponding to the 21 encodings of BFACTION as shown in the table here. Other values are reserved. The VLD decoded value of BFACTION (from the picture header) is mapped into an enum value from 0 to 20. MSB of this field can be used to determine if BFACTION is greater than or equal to 1/2, which is used to determine Motion Prediction Type for B pictures. Effectively, condition "BFACTION &gt;= 1/2" is equivalent to condition "ScaleFactor &gt;= 128". This field is only valid for B pictures. This field is used only in DXVA2 VC1 VLD mode, it is not used in Intel VC1 VLD Long Format mode and IT mode.</p>				
23	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ Advanced Profile only; RANGE_MAPY_FLAG Range Mapping not supported</td> </tr> </table>	Project:	All	Format:	MBZ Advanced Profile only; RANGE_MAPY_FLAG Range Mapping not supported
Project:	All				
Format:	MBZ Advanced Profile only; RANGE_MAPY_FLAG Range Mapping not supported				
22:20	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ Advanced Profile only; RANGE_MAPY Range Mapping not supported</td> </tr> </table>	Project:	All	Format:	MBZ Advanced Profile only; RANGE_MAPY Range Mapping not supported
Project:	All				
Format:	MBZ Advanced Profile only; RANGE_MAPY Range Mapping not supported				
19	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ Advanced Profile only; RANGE_MAPUV_FLAG Range Mapping not supported</td> </tr> </table>	Project:	All	Format:	MBZ Advanced Profile only; RANGE_MAPUV_FLAG Range Mapping not supported
Project:	All				
Format:	MBZ Advanced Profile only; RANGE_MAPUV_FLAG Range Mapping not supported				
18:16	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ Advanced Profile only; RANGE_MAPUV Range Mapping not supported</td> </tr> </table>	Project:	All	Format:	MBZ Advanced Profile only; RANGE_MAPUV Range Mapping not supported
Project:	All				
Format:	MBZ Advanced Profile only; RANGE_MAPUV Range Mapping not supported				
15:9	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ
Project:	All				
Format:	MBZ				
8	<b>4MV Allowed Flag</b>				
7	<b>POSTPROC Flag</b>				
6	<b>PULLDOWN</b>				
5	<b>INTERLACE</b>				
4	<b>TFCNTRFLAG</b>				
3	<b>FINTERFLAG</b>				
2	<p><b>REFPIC Flag</b></p> <p>For a BI picture, REFPIC flag must set to 0. For I and P picture, REFPIC flag must set to 0. For a B picture, REFPIC flag must set to 0, except for a B-field in interlaced field mode which can be 0 or 1 (e.g. the top B field can be used as a reference for decoding its corresponding bottom B-field in a field pair). In VLD mode, this flag cannot be used as an optimization signaling for an I or P picture that is not used as a reference picture. This field is used in both DXVA2 VC1 VLD mode and IT mode. It is the same parameter as bPicDeblockConfined[bit2] in DXVA2 VC1 spec. The Intra Picture Flag, Backward Prediction Present Flag and RefPicFlag are used to derive the picture type, as specified in PTYPE for a frame, and in FPTYPE for a field, in DXVA2 VC1 VLD and IT mode.</p>				

<b>MFD_VC1_SHORT_PIC_STATE</b>			
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0h		the current picture after decoded, will never used as a reference picture
	1h		the current picture after decoded, will be used as a reference picture later
1	<b>PSF</b>		
0	<b>EXTENDED_DMV Present Flag</b>		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0h	<b>[Default]</b>	Extended_DMV is not present in the picture header
	1h		Extended_DMV is present in the picture header

## MFD\_VP8\_BSD\_OBJECT

<b>MFD_VP8_BSD_OBJECT</b>				
Project:	CHV, BSW			
Source:	VideoCS			
Length Bias:	2			
<p>The MFD_VP8_BSD_OBJECT command is the only primitive command for the VP8 Decoding Pipeline. The Partitions of the bitstream is loaded as indirect data object. Before issuing a MFD_VP8_BSD_OBJECT command, all VP8 frame level states of the MFD Engine need to be valid. Therefore the commands used to set these states need to have been issued prior to the issue of a MFD_VP8_BSD_OBJECT command. Context switch interrupt is not supported by this command.</p>				
DWord	Bit	Description		
0	31:29	<b>Command Type</b>		
		Default Value:	3h PARALLEL_VIDEO_PIPE	
		Format:	OpCode	
	28:27	<b>Pipeline</b>	Default Value:	2h MFD_VP8_BSD_OBJECT
			Format:	OpCode
			<b>Media Command OpCode</b>	
	26:24	<b>Media Command OpCode</b>	Default Value:	4h VP8_DEC
			Format:	OpCode
			<b>subOpcodeA</b>	
	23:21	<b>subOpcodeA</b>	Default Value:	1h
Format:			OpCode	
<b>subOpcodeB</b>				
20:16	<b>subOpcodeB</b>	Default Value:	8h	
		Format:	OpCode	
		<b>Reserved</b>		
15:12	<b>Reserved</b>	Format:	MBZ	
		<b>DWord Length</b>		
		11:0	Default Value:	14h Excludes DWord (0,1)
Format:	=n Total Length - 2			
1	31:21	<b>Reserved</b>		
		Format:	MBZ	
		<b>Partition0 CPBAC Entropy Count</b> Pass the Partition0 CPBAC State to HW. Max value is 24.		
15:8	<b>Partition0 CPBAC Entropy Range</b> Pass the Partition0 CPBAC State to HW.			

<b>MFD_VP8_BSD_OBJECT</b>		
	7:6	<b>Reserved</b> Format: MBZ
	5:4	<b>Coded Num of Coeff Token Partitions</b> Num of Partitions = 2^CodedNumCoeffTokenPartitions. 0 = 1 Partition only 1 = 2 Partitions 2 = 4 Partitions 3 = 8 Partitions are present in the bitstream.
	3	<b>Reserved</b> Format: MBZ
	2:0	<b>Partition0 FirstMBBitOffset from Frame Header</b> Allow HW to jump to the location in the bitstream where per MB information starts in the Partition0.
2	31:24	<b>Partition0 CPBAC Entropy Value</b> Pass the Partition0 CPBAC State to HW.
	23:0	<b>Reserved</b> Format: MBZ
3	31:24	<b>Reserved</b> Format: MBZ
	23:0	<b>Indirect Partition0 Data Length</b> This field provides the length in bytes of the indirect data. A value zero indicates that indirect data fetching is disabled - subsequently, the Indirect Partition Start Offset field is ignored. The Partition is byte aligned in both ends. It is the length in bytes of the bitstream data for the current partition. It includes the first byte of the first macroblock and the last byte of the last macroblock in the partition.
4	31:0	<b>Indirect Partition0 Data Start Offset</b> This field specifies the Graphics Memory starting address of the data to be fetched into BSD Unit for processing. This offset is relative to the MFD Indirect Object Base Address. Hardware ignores this field if indirect data is not present. It is a byte-aligned address for the VP8 bitstream data in each partition.
5	31:24	<b>Reserved</b> Format: MBZ
	23:0	<b>Indirect Partition1 Data Length</b> This field provides the length in bytes of the indirect data. A value zero indicates that indirect data fetching is disabled - subsequently, the Indirect Partition Start Offset field is ignored. The Partition is byte aligned in both ends. It is the length in bytes of the bitstream data for the current partition. It includes the first byte of the first macroblock and the last byte of the last macroblock in the partition.
6	31:0	<b>Indirect Partition1 Data Start Offset</b> This field specifies the Graphics Memory starting address of the data to be fetched into BSD Unit for processing. This offset is relative to the MFD Indirect Object Base Address. Hardware ignores this field if indirect data is not present. It is a byte-aligned address for the VP8 bitstream data in each partition.
7	31:24	<b>Reserved</b>

<b>MFD_VP8_BSD_OBJECT</b>				
	23:0	<p><b>Indirect Partition2 Data Length</b></p> <p>This field provides the length in bytes of the indirect data. A value zero indicates that indirect data fetching is disabled - subsequently, the Indirect Partition Start Offset field is ignored. The Partition is byte aligned in both ends. It is the length in bytes of the bitstream data for the current partition. It includes the first byte of the first macroblock and the last byte of the last macroblock in the partition.</p>		
8	31:0	<p><b>Indirect Partition2 Data Start Offset</b></p> <p>This field specifies the Graphics Memory starting address of the data to be fetched into BSD Unit for processing. This offset is relative to the MFD Indirect Object Base Address. Hardware ignores this field if indirect data is not present. It is a byte-aligned address for the VP8 bitstream data in each partition.</p>		
9	31:24	<p><b>Reserved</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
23:0	<p><b>Indirect Partition3 Data Length</b></p> <p>This field provides the length in bytes of the indirect data. A value zero indicates that indirect data fetching is disabled - subsequently, the Indirect Partition Start Offset field is ignored. The Partition is byte aligned in both ends. It is the length in bytes of the bitstream data for the current partition. It includes the first byte of the first macroblock and the last byte of the last macroblock in the partition.</p>			
10	31:0	<p><b>Indirect Partition3 Data Start Offset</b></p> <p>This field specifies the Graphics Memory starting address of the data to be fetched into BSD Unit for processing. This offset is relative to the MFD Indirect Object Base Address. Hardware ignores this field if indirect data is not present. It is a byte-aligned address for the VP8 bitstream data in each partition.</p>		
11	31:24	<p><b>Reserved</b></p>		
	23:0	<p><b>Indirect Partition4 Data Length</b></p> <p>This field provides the length in bytes of the indirect data. A value zero indicates that indirect data fetching is disabled - subsequently, the Indirect Partition Start Offset field is ignored. The Partition is byte aligned in both ends. It is the length in bytes of the bitstream data for the current partition. It includes the first byte of the first macroblock and the last byte of the last macroblock in the partition.</p>		
12	31:0	<p><b>Indirect Partition4 Data Start Offset</b></p> <p>This field specifies the Graphics Memory starting address of the data to be fetched into BSD Unit for processing. This offset is relative to the MFD Indirect Object Base Address. Hardware ignores this field if indirect data is not present. It is a byte-aligned address for the VP8 bitstream data in each partition.</p>		
13	31:24	<p><b>Reserved</b></p>		
	23:0	<p><b>Indirect Partition5 Data Length</b></p> <p>This field provides the length in bytes of the indirect data. A value zero indicates that indirect data fetching is disabled - subsequently, the Indirect Partition Start Offset field is ignored. The Partition is byte aligned in both ends. It is the length in bytes of the bitstream data for the current partition. It includes the first byte of the first macroblock and the last byte of the last macroblock in the partition.</p>		

<b>MFD_VP8_BSD_OBJECT</b>				
14	31:0	<p><b>Indirect Partition5 Data Start Offset</b></p> <p>This field specifies the Graphics Memory starting address of the data to be fetched into BSD Unit for processing. This offset is relative to the MFD Indirect Object Base Address. Hardware ignores this field if indirect data is not present. It is a byte-aligned address for the VP8 bitstream data in each partition.</p>		
15	31:24	<p><b>Reserved</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">MBZ</td> </tr> </table>	Format:	MBZ
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23:0	<p><b>Indirect Partition6 Data Length</b></p> <p>This field provides the length in bytes of the indirect data. A value zero indicates that indirect data fetching is disabled - subsequently, the Indirect Partition Start Offset field is ignored. The Partition is byte aligned in both ends. It is the length in bytes of the bitstream data for the current partition. It includes the first byte of the first macroblock and the last byte of the last macroblock in the partition.</p>			
16	31:0	<p><b>Indirect Partition6 Data Start Offset</b></p> <p>This field specifies the Graphics Memory starting address of the data to be fetched into BSD Unit for processing. This offset is relative to the MFD Indirect Object Base Address. Hardware ignores this field if indirect data is not present. It is a byte-aligned address for the VP8 bitstream data in each partition.</p>		
17	31:24	<p><b>Reserved</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
23:0	<p><b>Indirect Partition7 Data Length</b></p> <p>This field provides the length in bytes of the indirect data. A value zero indicates that indirect data fetching is disabled - subsequently, the Indirect Partition Start Offset field is ignored. The Partition is byte aligned in both ends. It is the length in bytes of the bitstream data for the current partition. It includes the first byte of the first macroblock and the last byte of the last macroblock in the partition.</p>			
18	31:0	<p><b>Indirect Partition7 Data Start Offset</b></p> <p>This field specifies the Graphics Memory starting address of the data to be fetched into BSD Unit for processing. This offset is relative to the MFD Indirect Object Base Address. Hardware ignores this field if indirect data is not present. It is a byte-aligned address for the VP8 bitstream data in each partition.</p>		
19	31:24	<p><b>Reserved</b></p>		
	23:0	<p><b>Indirect Partition8 Data Length</b></p> <p>This field provides the length in bytes of the indirect data. A value zero indicates that indirect data fetching is disabled - subsequently, the Indirect Partition Start Offset field is ignored. The Partition is byte aligned in both ends. It is the length in bytes of the bitstream data for the current partition. It includes the first byte of the first macroblock and the last byte of the last macroblock in the partition.</p>		
20	31:0	<p><b>Indirect Partition8 Data Start Offset</b></p> <p>This field specifies the Graphics Memory starting address of the data to be fetched into BSD Unit for processing. This offset is relative to the MFD Indirect Object Base Address. Hardware ignores this field if indirect data is not present. It is a byte-aligned address for the VP8 bitstream data in each partition.</p>		

<b>MFD_VP8_BSD_OBJECT</b>											
21	31	<p><b>Concealment Method</b> This field specifies the method used for concealment when error is detected.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Intra 16x16 Prediction</td> <td>A copy from the current picture is performed using Intra 16x16 Prediction method.</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Inter P Copy</td> <td>A copy from collocated macroblock location is performed from the concealment reference indicated by the ConCeal_Pic_Id field.</td> </tr> </tbody> </table>	Value	Name	Description	0	Intra 16x16 Prediction	A copy from the current picture is performed using Intra 16x16 Prediction method.	1	Inter P Copy	A copy from collocated macroblock location is performed from the concealment reference indicated by the ConCeal_Pic_Id field.
	Value	Name	Description								
	0	Intra 16x16 Prediction	A copy from the current picture is performed using Intra 16x16 Prediction method.								
	1	Inter P Copy	A copy from collocated macroblock location is performed from the concealment reference indicated by the ConCeal_Pic_Id field.								
	30:18	<p><b>Reserved</b></p> <table border="1"> <tr> <td style="width: 60%;">Format:</td> <td style="text-align: center;">MBZ</td> </tr> </table>	Format:	MBZ							
	Format:	MBZ									
	17:16	<p><b>Conceal_Pic_Id (Concealment Picture ID)</b></p> <table border="1"> <tr> <td style="width: 30%;">Exists If:</td> <td>[Concealment Method] == 1</td> </tr> </table> <p>This field identifies the picture in the reference list to be used for concealment. This field is only valid if Concealment Method is Inter P Copy. 00 - Last Decoded Picture 01 - Golden Reference Picture 02 - Alternate Reference Picture 03 - User provided Reference Picture</p>	Exists If:	[Concealment Method] == 1							
	Exists If:	[Concealment Method] == 1									
	15	<p><b>Reserved</b></p> <table border="1"> <tr> <td style="width: 60%;">Format:</td> <td style="text-align: center;">MBZ</td> </tr> </table>	Format:	MBZ							
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14	<p><b>BSDPrematureComplete Error Handling</b> It occurs in situation where the decode is completed but there are still data in the bitstream.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Ignore the error and continue (masked the interrupt), assume the hardware automatically perform the error handling</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Set the interrupt to the driver (provide MMIO registers for MB address R/W)</td> </tr> </tbody> </table>	Value	Name	0	Ignore the error and continue (masked the interrupt), assume the hardware automatically perform the error handling	1	Set the interrupt to the driver (provide MMIO registers for MB address R/W)				
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12	<p><b>MPR Error (MV out of range) Handling</b></p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Ignore the error and continue (masked the interrupt), assume the hardware automatically perform the error handling</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Set the interrupt to the driver (provide MMIO registers for MB address R/W)</td> </tr> </tbody> </table>	Value	Name	0	Ignore the error and continue (masked the interrupt), assume the hardware automatically perform the error handling	1	Set the interrupt to the driver (provide MMIO registers for MB address R/W)				
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11	<p><b>Reserved</b></p>										
10	<p><b>Entropy Error Handling</b></p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Ignore the error and continue (masked the interrupt), assume the hardware automatically perform the error handling</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Set the interrupt to the driver (provide MMIO registers for MB address R/W)</td> </tr> </tbody> </table>	Value	Name	0	Ignore the error and continue (masked the interrupt), assume the hardware automatically perform the error handling	1	Set the interrupt to the driver (provide MMIO registers for MB address R/W)				
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Format:	MBZ										

<b>MFD_VP8_BSD_OBJECT</b>		
	8	<b>MB Header Error Handling</b>
	<b>Value</b>	<b>Name</b>
	0	Ignore the error and continue (masked the interrupt), assume the hardware automatically performs the error handling.
	1	Set the interrupt to the driver (provide MMIO registers for MB address R/W)
	7:0	<b>Reserved</b>
		Format: <span style="float: right;">MBZ</span>



## MFX\_AVC\_DIRECTMODE\_STATE

MFX_AVC_DIRECTMODE_STATE			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>This is a picture level command and is issued once per picture. All DMV buffers are treated as standard media surfaces, in which the lower 6 bits are used for conveying surface states. Current Pic POC number is assumed to be available in POCList[32 and 33] of the MFX_AVC_DIRECTMODE_STATE Command. This command is only valid in the AVC decoding in VLD and IT modes, and AVC encoder mode. The same command supports both Long and Short DXVA2 AVC Interface. The DMV buffers are not required to be programmed for encoder mode.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h MFX_SINGLE_DW
		Format:	OpCode
	26:24	<b>Media Command Opcode</b>	
		Default Value:	1h AVC_COMMON
		Format:	OpCode
	23:21	<b>SubOpcodeA</b>	
Default Value:		0h	
Format:		OpCode	
20:16	<b>SubOpcodeB</b>		
	Default Value:	2h	
	Format:	OpCode	
15:12	<b>Reserved</b>		
	Format:	MBZ	
11:0	<b>DWord Length</b>		
	Default Value:	0045h Excludes DWord (0,1)	
	Format:	=n Total Length - 2	
1	31:6	<b>Direct MV Buffer Base Address for Picture 0 (In Frame)</b>	
		Format:	GraphicsAddress[31:6]
		<b>Note:</b> This field is changed to one per frame (both top and bottom field share the same Direct MV Buffer Base Address).	
		This field provides the base address of the DMV write buffer to store motion vectors	

<b>MFX_AVC_DIRECTMODE_STATE</b>													
	<p>decoded in the current picture (top field), which may be used later as a collocated motion information read buffer of the associated reference picture in decoding subsequent B-pictures that have MB coded in direct mode. It is a private buffer used by the MPR hardware only. Its content is not accessed by software. This buffer must be 64-byte cacheline aligned. The write buffer size is 557,056 bytes for 1 frame. Scalable with frame height, but do not scale with frame width as the hardware assumes frame width (in MBs) fixed at 128 (smallest power of 2 value larger than 120 - 1920x1088 screen resolution) It is only valid if the current picture is a progressive frame, MbAff frame, or a top field. There are a total of 32 reference picture (previously decoded) Direct MV Buffers (0 to 31, not including the DMV write buffer 32 and 33 of the current picture) to read in the corresponding collocated DMV and motion information. For reference picture, these 32 DMV read Buffers can be indexed by the frame_store_ID[4:0], which is obtained from RefPicList L0/L1[RefPicIdx]. frame_Store_IDbit[0] (indicator for Top/Bottom Field). For writing out motion information during the decoding of the current picture, all 34 DMV buffers can be addressed by [ img_dec_fs_idc[4:0] &lt; 1 + img_structure[1] ].</p>												
	<p>5:0 <b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ								
Project:	CHV, BSW												
Format:	MBZ												
2	<p>31:16 <b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>Reserved for 64-bit address extension.</p> <p>15:0 <b>Direct MV Buffer Base Address for Picture 0 - Read/Write [47:32]</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table> <table border="1"> <thead> <tr> <th style="text-align: center;">Description</th> <th style="text-align: center;">Project</th> </tr> </thead> <tbody> <tr> <td>This field is for the upper range of AACs Bit Vector Surface Starting Byte Address.</td> <td></td> </tr> <tr> <td>This field is used for 48-bit addressing.</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Project:	CHV, BSW	Format:	MBZ	Project:	CHV, BSW	Description	Project	This field is for the upper range of AACs Bit Vector Surface Starting Byte Address.		This field is used for 48-bit addressing.	CHV, BSW
Project:	CHV, BSW												
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3..32	<p>63:48 <b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>47:32 <b>Direct MV Buffer Base Address for Reference Frame 1 to 15 (In Frame) High</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>This field is for the upper range of Pre-Deblocking Destination Address. This field is ignored if PreDeblockOutEnable is set to 0 (disable). This field is used for 48-bit addressing.</p> <p>31:6 <b>Direct MV Buffer Base Address for Reference Frame 1 to 15 (In Frame)</b></p> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[31:6]</td> </tr> </table>	Format:	MBZ	Project:	CHV, BSW	Format:	GraphicsAddress[47:32]	Format:	GraphicsAddress[31:6]				
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Project:	CHV, BSW												
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Format:	GraphicsAddress[31:6]												

<b>MFX_AVC_DIRECTMODE_STATE</b>														
	<p><b>Note:</b>This field is changed to one per frame (both top and bottom field shared the same Direct MV Buffer Base Address)</p> <p>This field provides the base address of the DMV buffer for reference frame 2 to 31. They are needed if the current B-Picture has MBs coded in direct mode. It is a private buffer used by the MPR hardware only. Its content is not accessed by software. All these buffers must be 64-byte cacheline aligned. There are a total of 32 possible Direct MV Read Buffers (not including the current write buffer of the current picture) to read in the corresponding DMV. Each read buffer size is 557,056 bytes for 1 frame (the selected colPic). Scalable with frame height, but do not scale with frame width as the hardware assumes frame width (in MBs) fixed at 128 (smallest power of 2 value larger than 120 - 1920x1088 screen resolution). The adjacent DMV buffers are paired ([2 and 3], [4 and 5], [N and N+1], ..[30 and 31]).</p>													
	<p>5:0 <b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">MBZ</td> </tr> </table> <p>Reserved for 64-bit address extension.</p>	Format:	MBZ											
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33	<p>31:15 <b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td style="width: 50%;">CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ									
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<p>8:7 <b>Direct MV Buffer Base Address for Reference Frame - Arbitration Priority Control</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td style="width: 50%;">CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U2</td> </tr> </table> <p>This field controls the priority of arbitration used in the GAC/GAM pipeline for this surface.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 30%; text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">00b</td> <td>Highest priority</td> </tr> <tr> <td style="text-align: center;">01b</td> <td>Second highest priority</td> </tr> <tr> <td style="text-align: center;">10b</td> <td>Third highest priority</td> </tr> <tr> <td style="text-align: center;">11b</td> <td>Lowest priority</td> </tr> </tbody> </table>	Project:	CHV, BSW	Format:	U2	Value	Name	00b	Highest priority	01b	Second highest priority	10b	Third highest priority	11b	Lowest priority
Project:	CHV, BSW													
Format:	U2													
Value	Name													
00b	Highest priority													
01b	Second highest priority													
10b	Third highest priority													
11b	Lowest priority													
<p>6:5 <b>Memory Type: LLC/eLLC Cacheability Control (LeLLCCC) for Direct MV Buffer for Reference Picture 0 to 15</b></p>														

<b>MFX_AVC_DIRECTMODE_STATE</b>															
	<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td colspan="2">This is the field used in GT interface block to determine what type of access need to be generated to uncore. For the cases where the LeLLCCC is set, cacheable transaction are generated to enable LLC usage for particular stream.</td> </tr> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> <tr> <td>00b</td> <td>Use Cacheability Controls from page table</td> </tr> <tr> <td>01b</td> <td>Uncacheable (UC) - non-cacheable</td> </tr> <tr> <td>10b</td> <td>Writethrough (WT)</td> </tr> <tr> <td>11b</td> <td>Writeback (WB)</td> </tr> </table>	Project:	CHV, BSW	This is the field used in GT interface block to determine what type of access need to be generated to uncore. For the cases where the LeLLCCC is set, cacheable transaction are generated to enable LLC usage for particular stream.		Value	Name	00b	Use Cacheability Controls from page table	01b	Uncacheable (UC) - non-cacheable	10b	Writethrough (WT)	11b	Writeback (WB)
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4:3	<p><b>Target Cache (TC) for Direct MV Buffer for Reference Picture 0 to 15</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td colspan="2">This field allows the choice of LLC vs eLLC for caching</td> </tr> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> <tr> <td>00b</td> <td>eLLC Only - not snooped in GT</td> </tr> <tr> <td>01b</td> <td>LLC Only</td> </tr> <tr> <td>10b</td> <td>LLC/eLLC Allowed</td> </tr> <tr> <td>11b</td> <td>L3, LLC, eLLC Allowed</td> </tr> </table>	Project:	CHV, BSW	This field allows the choice of LLC vs eLLC for caching		Value	Name	00b	eLLC Only - not snooped in GT	01b	LLC Only	10b	LLC/eLLC Allowed	11b	L3, LLC, eLLC Allowed
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34	<p>31:6 <b>Direct MV Buffer Base Address for Write (Write-Only Buffer)(in frame)</b></p> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[31:6]</td> </tr> <tr> <td colspan="2"> <p>This field provides the base address of the DMV write-only buffer for the current decoding frame/field. It is a private buffer used by the MPR hardware only. Its content is not accessed by software. All these buffers must be 64-byte cacheline aligned, i.e. the same as the above DMV read/write buffers. These 2 buffers can only be addressed by [img_dec_fs_idc[4:0]«1 + img_structure[1]] for the current picture being decoded.</p> <p>Each write buffer size is 557,056 bytes for 1 frame (the selected colPic). Scalable with frame height, but do not scale with frame width as the hardware assumes frame width (in MBs) fixed at 128 (smallest power of 2 value larger than 120 - 1920x1088 screen resolution).</p> <p>DMV write buffer 32 is valid only if the current picture is a progressive frame, MbAff frame, or a top field. DMV write buffer 33 is valid only if the current picture is a bottom field.</p> </td> </tr> </table>	Format:	GraphicsAddress[31:6]	<p>This field provides the base address of the DMV write-only buffer for the current decoding frame/field. It is a private buffer used by the MPR hardware only. Its content is not accessed by software. All these buffers must be 64-byte cacheline aligned, i.e. the same as the above DMV read/write buffers. These 2 buffers can only be addressed by [img_dec_fs_idc[4:0]«1 + img_structure[1]] for the current picture being decoded.</p> <p>Each write buffer size is 557,056 bytes for 1 frame (the selected colPic). Scalable with frame height, but do not scale with frame width as the hardware assumes frame width (in MBs) fixed at 128 (smallest power of 2 value larger than 120 - 1920x1088 screen resolution).</p> <p>DMV write buffer 32 is valid only if the current picture is a progressive frame, MbAff frame, or a top field. DMV write buffer 33 is valid only if the current picture is a bottom field.</p>											
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<b>MFX_AVC_DIRECTMODE_STATE</b>			
	5:0	<b>Reserved</b>	
		Project: CHV, BSW	
		Format: MBZ	
35	31:16	<b>Reserved</b>	
		Project: CHV, BSW	
		Format: MBZ	
	Reserved for 64-bit address extension.		
	15:0	<b>Direct MV Buffer Base Address for Write (Write-Only Buffer)(in frame) High</b>	
		Project: CHV, BSW	
		Format: GraphicsAddress[47:32]	
	This field is for the upper range of Direct MV Buffer Base Address. This field is ignored if PreDeblockOutEnable is set to 0 (disable). This field is used for 48-bit addressing.		
	36	31:15	<b>Reserved</b>
			Project: CHV, BSW
Format: MBZ			
14:13		<b>Reserved</b>	
		Project: CHV, BSW	
		Format: MBZ	
12:11		<b>Reserved</b>	
10:9		<b>Reserved</b>	
		Project: CHV, BSW	
		Format: MBZ	
8:7		<b>Direct MV Buffer Base Address for Write - Arbitration Priority Control</b>	
		Project: CHV, BSW	
		This field controls the priority of arbitration used in the GAC/GAM pipeline for this surface.	
		<b>Value</b>	<b>Name</b>
		00b	Highest priority
		01b	Second highest priority
		10b	Third highest priority
11b		Lowest priority	
6:5	<b>Memory Type: LLC/eLLC Cacheability Control (LeLLCCC) for Direct MV Buffer for Write</b>		
	Project: CHV, BSW		
	This is the field used in GT interface block to determine what type of access need to be generated to uncore. For the cases where the LeLLCCC is set, cacheable transaction are generated to enable LLC usage for particular stream.		
	<b>Value</b>	<b>Name</b>	

<b>MFX_AVC_DIRECTMODE_STATE</b>													
	<table border="1"> <tr> <td>00b</td> <td>Use Cacheability Controls from page table</td> </tr> <tr> <td>01b</td> <td>Uncacheable (UC) - non-cacheable</td> </tr> <tr> <td>10b</td> <td>Writethrough (WT)</td> </tr> <tr> <td>11b</td> <td>Writeback (WB)</td> </tr> </table>	00b	Use Cacheability Controls from page table	01b	Uncacheable (UC) - non-cacheable	10b	Writethrough (WT)	11b	Writeback (WB)				
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4:3	<p><b>Target Cache (TC) for Direct MV Buffer for Write</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This field controls the L3\$, LLC and eLLC (eDRAM) cacheability for a given surface. Setting of "00" points to PTE settings which defaults to eDRAM (when present). If no eDRAM, the access will be allocated to LLC. Setting of "01", allocates into LLC and victimizes the line to eDRAM. Setting of "10" allows the line to be allocated in either LLC or eDRAM. Setting of "11" is the only option for a memory access to be allocated in L3\$ as well as LLC/eLLC</p> <p>00b: eLLC Only ("00" setting points TC selection to PTE which defaults to eLLC)            01b: LLC Only (Works at the allocation time, later victimization from LLC downgrades the line to eLLC if present).            10b: LLC/eLLC Allowed.            11b: L3, LLC, eLLC Allowed.</p> <p><b>Errata CHV:A-E (FIXED BY:G0 Stepping):</b>            For all system that does NOT use SVM (i.e. coherent L3\$ surfaces), back snoops from LLC has to be disabled (<b>Dis_GtCvUpdtOnRd = "1"</b>). Than target Cache settings can be programmed as POR requirements of L3/LLC/eDRAM caching.            For all systems that does use SVM (i.e. coherent L3\$ surfaces), the recommended setting would be "00" in target cache settings. In case of L3 surfaces, the performance has to be tuned between "00" and "11" setting based on the benefits of L3 caching outweighing the degradation of backsnoops.            Post G0-stepping, the above w/a for coherent L3\$ surfaces is not needed.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>eLLC Only - not snooped in GT</td> </tr> <tr> <td>01b</td> <td>LLC Only</td> </tr> <tr> <td>10b</td> <td>LLC/eLLC Allowed</td> </tr> <tr> <td>11b</td> <td>L3, LLC, eLLC Allowed</td> </tr> </tbody> </table>	Project:	CHV, BSW	Value	Name	00b	eLLC Only - not snooped in GT	01b	LLC Only	10b	LLC/eLLC Allowed	11b	L3, LLC, eLLC Allowed
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1:0	<p><b>Age for QUADLRU (AGE) for Direct MV Buffer for Write</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This field allows the selection of AGE parameter for a given surface in LLC or eLLC. If a particular allocation is done at youngest age ("0,1,2") it tends to stay longer in the cache. This option is given to GFX software to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>11b</td> <td>Good chance of generating hits.</td> </tr> <tr> <td>10b</td> <td>Next good chance of generating hits</td> </tr> <tr> <td>01b</td> <td>Decent chance of generating hits</td> </tr> </tbody> </table>	Project:	CHV, BSW	Value	Name	11b	Good chance of generating hits.	10b	Next good chance of generating hits	01b	Decent chance of generating hits		
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<b>MFX_AVC_DIRECTMODE_STATE</b>				
		<table border="1" style="width: 100%;"> <tr> <td style="width: 25%;">00b</td> <td>Poor chance of generating hits</td> </tr> </table>	00b	Poor chance of generating hits
00b	Poor chance of generating hits			
37..70	31:0	<p><b>POC List, POCList[34][31:0]</b></p> <p>Each POC value is a signed 32-bit number. One-to-one correspondence with the 34 Direct MV Buffer Address for Reference and Current Frames/Fields There are 34 POC entries in the list. For reference picture, only the lower 32 POC [0-31] entries can be used, and POCList[ ] is indexed by the frame_store_ID[4:0], which is obtained from RefPicList L0/L1[RefPicIdx]. frame_Store_IDbit[0] (indicator for Top/Bottom Field). For current picture, all 34 POC entries [0-33] can be addressed by POCList[ img_dec_fs_idc[4:0]«1 + img_structure[1] ]. For frame-only mode, every other entry is skipped. For MBAFF and field-only picture, each entry is a field POC, and every two entries are paired.</p>		

## MFV\_AVC\_IMG\_STATE

<b>MFV_AVC_IMG_STATE</b>		
Project:	CHV, BSW	
Source:	VideoCS	
Length Bias:	2	
<p>This must be the very first command to issue after the surface state, the pipe select and base address setting commands. This command supports both Long and Short VLD and IT DXVA2 AVC Decoding Interface.</p>		
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 3h PARALLEL_VIDEO_PIPE
		Format: OpCode
	28:27	<b>Pipeline</b>
		Default Value: 2h MFV_AVC_IMG_STATE
		Format: OpCode
	26:24	<b>Media Command Opcode</b>
		Default Value: 1h AVC_COMMON
		Format: OpCode
	23:21	<b>SubOpcode A</b>
		Default Value: 0h
		Format: OpCode
	20:16	<b>SubOpcode B</b>
Default Value: 0h		
Format: OpCode		
15:12	<b>Reserved</b>	
	Format: MBZ	
11:0	<b>DWord Length</b>	
	Default Value: 0Ch Excludes DWord (0,1)	
	Format: =n 00Eh, used for normal decode and encode mode 000h, a special case to provide a dummy image state for stitch mode operation. In this case, fields in DW1 which is part of the dummy image state command are ignored by hardware.	
1	31:16	<b>Reserved</b>
		Format: MBZ
	15:0	<b>Frame Size</b>
		Format: U16-1 in MB unit



<b>MFX_AVC_IMG_STATE</b>									
		<p>The value for FrameSizeInMBs must match the product of FrameWidthInMBs and FrameHeightInMBs.Max. Screen resolution is therefore limited to 256 x 256 in MB unit. It is enough to cover all the Profile-Level specified in the current HD-DVD specification. E.g., for 1920x1080, FrameSizeInMBs[15:0] = 8160 (1920/16 * 1088/16; rounded up 1080). This parameter is specified for Intel interface only, not present in the DXVA.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 20%;">Value</th> <th style="width: 20%;">Name</th> <th style="width: 60%;">Description</th> </tr> </thead> <tbody> <tr> <td>[0,16383]</td> <td></td> <td>representing Number of MBs [1,16384]</td> </tr> </tbody> </table>	Value	Name	Description	[0,16383]		representing Number of MBs [1,16384]	
Value	Name	Description							
[0,16383]		representing Number of MBs [1,16384]							
2	31:24	<p><b>Reserved</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">MBZ</td> </tr> </table> <p>(bit[31:24] must be zero to match the DXVA 16-bit definition for FrameHeightInMBsMinus1)</p>	Format:	MBZ					
	Format:	MBZ							
23:16	<p><b>Frame Height</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">U8-1 in MB unit</td> </tr> </table> <p>It is set to the value of (FrameHeightInMBsMinus1+ 1). Since the max value for FrameHeightInMBs is 255, the max allowed value for FrameHeightInMBsMinus1 is only 254. The min value for FrameHeightInMBs is 1.Although the max. value that can be specified for FrameHeightInMBs is 255 (in the current implementation), FrameWidthInMBs * FrameHeightInMBs must not exceed the max value of FrameSizeInMBs[14:0].e.g. for 1920x1080, FrameHeightInMBs[7:0] is equal to 68 (1080 divided by 16, and rounded up, i.e. effectively specified as 1088 instead).It is derived from FrameHeightInMbs = ( 2 - frame_mbs_only_flag ) * PicHeightInMapUnits and PicHeightInMbs = FrameHeightInMbs / ( 1 + field_pic_flag ) internally done. For MBAFF, PicHeightInMapUnits is in MB pair unit, so the bitstream sends only half frame height.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 20%;">Value</th> <th style="width: 20%;">Name</th> <th style="width: 60%;">Description</th> </tr> </thead> <tbody> <tr> <td>[0,255]</td> <td></td> <td>representing height [1,256]</td> </tr> </tbody> </table>	Format:	U8-1 in MB unit	Value	Name	Description	[0,255]		representing height [1,256]
Format:	U8-1 in MB unit								
Value	Name	Description							
[0,255]		representing height [1,256]							
	15:8	<p><b>Reserved</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">MBZ</td> </tr> </table> <p>(bit[15:8] must be zero to match the DXVA 16-bit definition for FrameWidthInMBsMinus1)</p>	Format:	MBZ					
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	7:0	<p><b>Frame Width</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">U8-1 in MB unit</td> </tr> </table> <p>It is set to the value of (FrameWidthInMBsMinus1+ 1). Since the max value for FrameWidthInMBs is 255, the max allowed value for FrameWidthInMBsMinus1 is only 254. The min value for FrameWidthInMBs is 1.Although the max. value that can be specified for FrameWidthInMBs is 255 (in the current implementation), FrameWidthInMBs * FrameWidthInMBs must not exceed the max value of FrameSizeInMBs[14:0].e.g. for 1920x1080, FrameHeightInMBs[7:0] is equal to 68 (1080 divided by 16, and rounded up, i.e. effectively specified as 1088 instead).It is derived from FrameWidthInMbs = ( 2 - frame_mbs_only_flag ) * PicWidthInMapUnits and PicWidthInMbs = FrameWidthInMbs / ( 1 + field_pic_flag ) internally done. For MBAFF, PicWidthInMapUnits is in MB pair unit, so the bitstream sends only half frame width.</p>	Format:	U8-1 in MB unit					
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<b>MFX_AVC_IMG_STATE</b>												
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	Format:	MBZ										
	28:24	<p><b>Second Chroma QP Offset</b></p> <p>Signed integer value. It should be in the range of -12 to +12 (according to AVC spec).It specifies the offset for determining QP Cr from QP Y. It is set to the upper 5 bits of the value of the syntax element (Chroma_qp_offset[9:0]) read from the current active PPS.Chroma_qp_offset [4:0] - chroma_qp_offset_bits (from the current active PPS)Chroma_qp_offset [9:5] - second_chroma_qp_offset_bits</p>										
	23:21	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>(bit[23:21] must be zero to match the DXVA2 8-bit definition for InitQpChroma[1])</p>	Format:	MBZ								
	Format:	MBZ										
	20:16	<p><b>First Chroma QP Offset</b></p> <p>Signed integer value. It should be in the range of -12 to +12 (according to AVC spec).It specifies the offset for determining QP Cb from QP Y. It is set to the lower 5 bits of the value of the syntax element (Chroma_qp_offset[9:0]) read from the current active PPS.Chroma_qp_offset [4:0] - chroma_qp_offset_bits (from the current active PPS)Chroma_qp_offset [9:5] - second_chroma_qp_offset_bits</p>										
	15:14	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ								
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	13	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ						
	Project:	CHV, BSW										
Format:	MBZ											
12	<p><b>Weighted_Pred_Flag</b></p> <table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>(This field is defined differently from Gen6, Gen7 follows strictly DXVA2 AVC interface.)</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Disable <b>[Default]</b></td> <td>specifies that weighted prediction is not used for P and SP slices</td> </tr> <tr> <td>1</td> <td>Enable</td> <td>specifies that weighted prediction is used for P and SP slices</td> </tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>This field must set to '0' for B and I pictures.</p>	Format:	Enable	Value	Name	Description	0	Disable <b>[Default]</b>	specifies that weighted prediction is not used for P and SP slices	1	Enable	specifies that weighted prediction is used for P and SP slices
Format:	Enable											
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1	Enable	specifies that weighted prediction is used for P and SP slices										
11:10	<p><b>Weighted_BiPred_Idc</b></p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> </tbody> </table>	Value	Name	Description								
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0	DEFAULT <b>[Default]</b>	Specifies that the default weighted prediction is used for B slices												
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	9:8	<p><b>ImgStruct - Image Structure, img_structure[1:0]</b> The current encoding picture structure can only takes on 3 possible values</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">00b</td> <td>Frame Picture</td> </tr> <tr> <td style="text-align: center;">01b</td> <td>Top Field Picture</td> </tr> <tr> <td style="text-align: center;">11b</td> <td>Bottom Field Picture</td> </tr> <tr> <td style="text-align: center;">10b</td> <td>Invalid, not allowed.</td> </tr> </tbody> </table>	Value	Name	00b	Frame Picture	01b	Top Field Picture	11b	Bottom Field Picture	10b	Invalid, not allowed.		
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00b	Frame Picture													
01b	Top Field Picture													
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		<b>Programming Notes</b>												
		img_structure[0] can be used as a flag to distinguish between frame and field structure. It must be consistent with the field_pic_flag setting in the Slice Header. This parameter is specified for Intel interface only, not present in the DXVA as a separate state (instead the img_structure[1] is embedded inside the DXVA picture definition).												
	7:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td style="width: 150px;">Format:</td> <td style="text-align: center;">MBZ</td> </tr> </table>	Format:	MBZ										
Format:	MBZ													
4	31:16	<p><b>MinFrameWSize</b></p> <table border="1"> <tr> <td style="width: 150px;">Default Value:</td> <td style="text-align: center;">0h</td> </tr> <tr> <td>Format:</td> <td style="text-align: center;">U16</td> </tr> </table> <p><b>Minimum Frame Size [15:0] (in Word, 16-bit)(Encoder Only)</b> Minimum Frame Size is specified to compensate for intel Rate Control Currently zero fill (no need to perform emulation byte insertion) is done only to the end of the CABAC_ZERO_WORD insertion (if any) at the last slice of a picture. Intel encoder parameter, not part of DXVA. The caller should always make sure that the value, represented by Minimum Frame Size, is always less than maximum frame size <b>FrameBitRateMax (DWORD 10 bits 29:16)</b>. This field is reserved in Decode mode.</p> <p>The programmable range <math>0 \dots 2^{18} - 1</math> When MinFrameWSizeUnits is 00.</p> <p>Programmable range is <math>0 \dots 2^{20} - 1</math> when MinFrameWSizeUnits is 01.</p> <p>Programmable range is <math>0 \dots 2^{26} - 1</math> when MinFrameWSizeUnits is 10.</p> <p>Programmable range is <math>0 \dots 2^{32} - 1</math> when MinFrameWSizeUnits is 11.</p>	Default Value:	0h	Format:	U16								
Default Value:	0h													
Format:	U16													

<b>MFX_AVC_IMG_STATE</b>			
15	<b>MbStatEnabled</b>		
	Format: Enable		
	Enable reading in MB status buffer (a.k.a. encoding stream-out buffer) Note: For multi-pass encoder, all passes except the first one need to set this value to 1. By setting the first pass to 0, it does save some memory bandwidth. In VDenc mode this must be set to zero as no MB level rate control is used.		
	<b>Value</b>	<b>Name</b>	
	0	Disable	
	<b>Description</b>		
	Disable Reading of Macroblock Status Buffer		
	1	Enable	
	Enable Reading of Macroblock Status Buffer		
	14	<b>LoadSlicePointerFlag</b>	
		Format: Enable	
		LoadBitStreamPointerPerSlice (Encoder-only)To support multiple slice picture and additional header/data insertion before and after an encoded slice.When this field is set to 0, bitstream pointer is only loaded once for the first slice of a frame. For subsequent slices in the frame, bitstream data are stitched together to form a single output data stream.When this field is set to 1, bitstream pointer is loaded for each slice of a frame. Basically bitstream data for different slices of a frame will be written to different memory locations.	
		<b>Value</b>	<b>Name</b>
		0	Disable
		<b>Description</b>	
Load BitStream Pointer only once for the first slice of a frame			
1		Enable	
Load/reload BitStream Pointer only once for the each slice, reload the start location of the bitstream buffer from the Indirect PAK-BSE Object Data Start Address field			
13		<b>Reserved</b>	
12	<b>MvUnpackedFlag</b>		
	MVUnpackedEnable (Encoder Only)This field is reserved in Decode mode.		
	<b>Value</b>	<b>Name</b>	
	0	PACKED	
<b>Description</b>			
use packed MV format (compliant to DXVA)			
1	UNPACKED		
use unpacked 8MV/32MV format only			
11:10	<b>ChromaFormatIdc</b>		
	Chroma Format IDC, ChromaFormatIdc[1:0]It specifies the sampling of chroma component (Cb, Cr) in the current picture as follows :		
	<b>Value</b>	<b>Name</b>	
	00b	monochrome picture	
	<b>Description</b>		
	Desc		
	01b	4:2:0 picture	
	Desc		
	10b	4:2:2 picture (not supported)	
	Desc		
11b	4:4:4 picture (not supported)		
Desc			
<b>Programming Notes</b>			
It is set to the value of the syntax element read from the current active SPS.The			

<b>MFX_AVC_IMG_STATE</b>		
		corresponding Monochrome Flag (monochrome_flag) can be derived from this field.
9	<b>Reserved</b>	
8	<b>MbMvFormatFlag</b> Use MB level MvFormat flag (Encoder Only)	
	<b>Value</b>	<b>Name</b>
	<b>Description</b>	
0	IGNORE	HW PAK ignore MvFormat in the MB data. When bit 12 == 0, all MBs use packed MV format When bit 12 == 1, each MB data must use unpacked MV format, 8MV when there is no minor MV involved, and 32MV if there are some minor MVs.
1	FOLLOW	HW PAK will follow MvFormat value set within each MB data.
<b>Programming Notes</b>		
They must take one of the two values: the 8MV unpacked format (MvFormat = 101b), and the 32MV unpacked format (MvFormat = 110b). This bit can be set only when MvUnpackedFlag (bit 12 of this register) is set otherwise system could hang.		
7	<b>EntropyCodingFlag</b> Entropy Coding Flag, entropy_coding_flag	
	<b>Value</b>	<b>Name</b>
	<b>Description</b>	
0	CAVLC bit-serial encoding mode	Desc
1	CABAC bit-serial encoding mode.	Desc
<b>Programming Notes</b>		
It specifies one of the two possible bit stream encoding modes in the AVC. It is set to the value of the syntax element read from the current active PPS.		
6	<b>ImgDisposableFlag</b> Current Img Disposable Flag or Non-Reference Picture Flag	
	<b>Value</b>	<b>Name</b>
	<b>Description</b>	
0	REFERENCE	the current decoding picture may be used as a reference picture for others
1	DISPOSABLE	the current decoding picture is not used as a reference picture (e.g. a B-picture cannot be a reference picture for any subsequent decoding)
<b>Programming Notes</b>		
It is derived from ImgDisposableFlag = (nal_ref_idc == 0). nal_ref_idc is a syntax element from a NAL unit. When this flag is set, no reference picture and DMV are written out. This field is only valid for VLD decoding mode.		
5	<b>ConstrainedIPredFlag</b> Constrained Intra Prediction Flag, constrained_ipred_flag It is set to the value of the syntax element in the current active PPS.	

<b>MFX_AVC_IMG_STATE</b>												
	<b>Value</b>	<b>Name</b>	<b>Description</b>									
	0	INTRA_AND_INTER	allows both intra and inter neighboring MB to be used in the intra-prediction encoding of the current MB.									
	1	INTRA_ONLY	allows only to use neighboring Intra MBs in the intra-prediction encoding of the current MB. If the neighbor is an inter MB, it is considered as not available.									
4	<p><b>Direct8x8InfFlag</b>            Direct 8x8 Inference Flag, direct_8x8_inference_flagIt is set to the value of the syntax element in the current active SPS.It specifies the derivation process for luma motion vectors in the Direct MV coding modes (B_Skip, B_Direct_16x16 and B_Direct_8x8). When frame_mbs_only_flag is equal to 0, direct_8x8_inference_flag shall be equal to 1.It must be consistent with the frame_mbs_only_flag and transform_8x8_mode_flag settings.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>SUBBLOCK</td> <td>allows subpartitioning to go below 8x8 block size (i.e. 4x4, 8x4 or 4x8)</td> </tr> <tr> <td>1</td> <td>BLOCK</td> <td>allows processing only at 8x8 block size. MB Info is stored for 8x8 block size.</td> </tr> </tbody> </table>			Value	Name	Description	0	SUBBLOCK	allows subpartitioning to go below 8x8 block size (i.e. 4x4, 8x4 or 4x8)	1	BLOCK	allows processing only at 8x8 block size. MB Info is stored for 8x8 block size.
Value	Name	Description										
0	SUBBLOCK	allows subpartitioning to go below 8x8 block size (i.e. 4x4, 8x4 or 4x8)										
1	BLOCK	allows processing only at 8x8 block size. MB Info is stored for 8x8 block size.										
3	<p><b>Transform8x8Flag</b>            8x8 IDCT Transform Mode Flag, trans8x8_mode_flagSpecifies 8x8 IDCT transform may be used in this pictureIt is set to the value of the syntax element in the current active PPS.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>4x4</td> <td>no 8x8 IDCT Transform, only 4x4 IDCT transform blocks are present</td> </tr> <tr> <td>1</td> <td>8x8</td> <td>8x8 Transform is allowed</td> </tr> </tbody> </table>			Value	Name	Description	0	4x4	no 8x8 IDCT Transform, only 4x4 IDCT transform blocks are present	1	8x8	8x8 Transform is allowed
Value	Name	Description										
0	4x4	no 8x8 IDCT Transform, only 4x4 IDCT transform blocks are present										
1	8x8	8x8 Transform is allowed										
2	<p><b>FrameMbOnlyFlag</b>            Frame MB only flag, frame_mbs_only_flagIt is set to the value of the syntax element in the current active SPS.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>FALSE</td> <td>not true ; effectively enables the possibility of MBAFF mode.</td> </tr> <tr> <td>1</td> <td>TRUE</td> <td>true, only frame MBs can occur in this sequence, hence disallows the MBAFF mode and field picture.</td> </tr> </tbody> </table>			Value	Name	Description	0	FALSE	not true ; effectively enables the possibility of MBAFF mode.	1	TRUE	true, only frame MBs can occur in this sequence, hence disallows the MBAFF mode and field picture.
Value	Name	Description										
0	FALSE	not true ; effectively enables the possibility of MBAFF mode.										
1	TRUE	true, only frame MBs can occur in this sequence, hence disallows the MBAFF mode and field picture.										
1	<p><b>MbaffFlameFlag</b>            MBAFF mode is active, mbaff_frame_flag.It is derived from MbaffFrameFlag = (mb_adaptive_frame_field_flag &amp;&amp; ! field_pic_flag ). mb_adaptive_frame_field_flag is a syntax element in the current active SPS and field_pic_flag is a syntax element in the current Slice Header. They both are present only if frame_mbs_only_flag is 0. Although mbaff_frame_flag is a Slice Header parameter, its value is expected to be the same for all the slices of a picture.It must be consistent with the mb_adaptive_frame_field_flag, the field_pic_flag and the frame_mbs_only_flag settings.This bit is valid only when the img_structure[1:0] indicates the current picture is a frame.</p>											

<b>MFX_AVC_IMG_STATE</b>							
		<b>Value</b>	<b>Name</b>	<b>Description</b>			
		0	FALSE	not in MBAFF mode			
		1	TRUE	in MBAFF mode			
	0	<b>FieldPicFlag</b>					
		Field picture flag, field_pic_flag, specifies the current slice is a coded field or not. It is set to the same value as the syntax element in the Slice Header. It must be consistent with the img_structure[1:0] and the frame_mbs_only_flag settings. Although field_pic_flag is a Slice Header parameter, its value is expected to be the same for all the slices of a picture.					
		<b>Value</b>	<b>Name</b>	<b>Description</b>			
		0h	FRAME	a slice of a coded frame			
		1h	FIELD	a slice of a coded field			
5	31	<b>Trellis Quantization Enabled (TQEnb)</b>					
		Format:		Enable			
		The TQ improves output video quality of AVC CABAC encoder by selecting quantized values for each non-zero coefficient so as to minimize the total R-D cost. This flag is only valid AVC CABAC mode. Otherwise, this flag should be disabled.					
		<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>		
		0h	Disable	Use Normal			
		1h	Enable	Use Trellis quantization	CHV, BSW		
		30:28		<b>Trellis Quantization Rounding (TQR)</b>			
				This rounding scheme is only applied to the quantized coefficients ranging from 0 to 1 when TQEnb is set to 1 in AVC CABAC mode. One of the following values is added to quantized coefficients before truncating fractional part.			
				<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>
				000b		Add 1/8	CHV, BSW
001b				Add 2/8	CHV, BSW		
010b				Add 3/8	CHV, BSW		
011b				Add 4/8 (rounding 0.5)	CHV, BSW		
100b				Add 5/8	CHV, BSW		
101b				Add 6/8	CHV, BSW		
110b	Default			Add 7/8 (Default rounding 0.875)	CHV, BSW		
[ExistsIf]Encode Only	27	<b>Trellis Quantization Chroma Disable (TQChromaDisable)</b>					
		This signal is used to disable chroma TQ. To enable TQ for both luma and chroma, TQEnb=1, TQChromaDisable=0. To enable TQ only for luma, TQEnb=1, TQChromaDisable=1.					
		<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>		
		0h		Enable Trellis Quantization chroma	CHV, BSW		
	1h	Default	Disable Trellis Quantization chroma	CHV, BSW			

<b>MFX_AVC_IMG_STATE</b>		
26:21	<b>Reserved</b>	
	Project:	CHV, BSW
	Format:	MBZ
20:17	<b>Reserved</b>	
	Format:	MBZ
16	<b>NonFirstPassFlag</b>	
	This signals the current pass is not the first pass. It will imply designate HW behavior: e.g	
	<b>Value</b>	<b>Name</b> <b>Description</b>
	0h	Disable      Always use the MbQpY from initial PAK inline object for all passes of PAK
	1h	Enable      Use MbQpY from stream-out buffer if MbRateCtrlFlag is set to 1
15:13	<b>Reserved</b>	
	Format:	MBZ
12	<b>Reserved</b>	
	Project:	CHV, BSW
	Format:	MBZ
11:10	<b>MinFrameWSizeUnits</b>	
	This field is the Minimum Frame Size Units	
	<b>Value</b>	<b>Name</b> <b>Description</b>
	00b	compatibility mode      Minimum Frame Size is in old mode (words, 2bytes)
	01b	16 byte      Minimum Frame Size is in 16bytes
	10b	4Kb      Minimum Frame Size is in 4Kbytes
	11b	16Kb      Minimum Frame Size is in 16Kbytes
9	<b>MbRateCtrlFlag - MB level Rate Control Enabling Flag</b>	
	MB Rate Control conformance mask	
	In VDenc mode, this field must be zero as frame level rate control is used.	
	<b>Value</b>	<b>Name</b> <b>Description</b>
	0h	Disable      Apply accumulative delta QP for consecutive passes on top of the macroblock QP values in inline data
	1h	Enable      Apply RC QP delta to suggested QP values in Macroblock Status Buffer except the first pass.
	<b>Programming Notes</b>	
	This field is ignored when MacroblockStatEnable is disabled or MB level Rate control flag for the current MB is disable in Macroblock Status Buffer.	
8	<b>Reserved</b>	
	Format:	MBZ



<b>MFX_AVC_IMG_STATE</b>			
7	<b>Intra/InterMblpcmFlag - ForcelPCMControlMask</b>		
	This field is to Force <b>IPCM</b> for Intra or Inter Macroblock size conformance mask.		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0h	Disable	Do not change intra or Inter macroblocks even
	1h	Enable	Change intra or Inter macroblocks MB_type to IPCM
<b>Project</b>			
CHV, BSW			
CHV, BSW			
<b>Programming Notes</b>			
This field is ignored when MacroblockStatEnable is disabled or MB level Intra MB conformance flag for the current MB is disable in Macroblock Status Buffer.			
6:4	<b>Reserved</b>		
	Format:	MBZ	
3	<b>FrameSzUnderFlag - FrameBitRateMinReportMask</b>		
	This is a mask bit controlling if the condition of frame level bit count is less than FrameBitRateMin		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0h	Disable	Do not update bit0 of MFC_IMAGE_STATUS control register.
	1h	Enable	set bit0 and bit 1of MFC_IMAGE_STATUS control register if the total frame level bit counter is less than or equal to Frame Bit rate Minimum limit.
2	<b>FrameSzOverFlag - FrameBitRateMaxReportMask</b>		
	This is a mask bit controlling if the condition of frame level bit count exceeds FrameBitRateMax.		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0	Disable	Do not update bit0 of MFC_IMAGE_STATUS control register.
	1	Enable	Set bit0 and bit 1 of MFC_IMAGE_STATUS control register if the total frame level bit counter is greater than or equal to Frame Bit rate Maximum limit.
1	<b>InterMbMaxBitFlag - InterMBMaxSizeReportMask</b>		
	This is a mask bit controlling if the condition of any inter MB in the frame exceeds InterMBMaxSize.		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0	Disable	Do not update bit0 of MFC_IMAGE_STATUS control register.
	1	Enable	Set bit0 of MFC_IMAGE_STATUS control register if the total bit counter for the current MB is greater than the Inter MB Conformance Max size limit.
0	<b>IntraMbMaxBitFlag - IntraMBMaxSizeReportMask</b>		
	This is a mask bit controlling if the condition of any intra MB in the frame exceeds IntraMBMaxSize.		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
0h	Disable	Do not update bit0 of MFC_IMAGE_STATUS control register.	

<b>MFX_AVC_IMG_STATE</b>													
		<table border="1"> <tr> <td style="width: 50px; text-align: center;">1</td> <td style="width: 100px;">Enable</td> <td>set bit0 of MFC_IMAGE_STATUS control register if the total bit counter for the current MB is greater than the Intra MB Conformance Max size limit.</td> </tr> </table>	1	Enable	set bit0 of MFC_IMAGE_STATUS control register if the total bit counter for the current MB is greater than the Intra MB Conformance Max size limit.								
1	Enable	set bit0 of MFC_IMAGE_STATUS control register if the total bit counter for the current MB is greater than the Intra MB Conformance Max size limit.											
6	31:28	<b>Reserved</b>											
	27:16	<b>InterMbMaxSz</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U12</td> </tr> </table> <p>This field, Inter MB Conformance Max size limit, indicates the allowed max bit count size for Inter MB</p>	Format:	U12									
	Format:	U12											
	15:12	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">MBZ</td> </tr> </table>	Format:	MBZ									
Format:	MBZ												
11:0	<b>IntraMbMaxSz</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Exists If:</td> <td style="width: 50%;">//Intra Only</td> </tr> <tr> <td>Format:</td> <td>U12</td> </tr> </table> <p>This field, Intra MB Conformance Max size limit, indicates the allowed max bit count size for Intra MB</p> <p>All IPCM MBs should ignore this Max size limit.</p>	Exists If:	//Intra Only	Format:	U12								
Exists If:	//Intra Only												
Format:	U12												
7	31:1	<b>Reserved</b>											
	0	<b>VSL Top MB Trans8x8flag</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td style="width: 50%;">CHV, BSW</td> </tr> </table> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #e1eef6;"> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 70%;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Disable <b>[Default]</b></td> <td>VSL will only fetch the current MB data.</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Enable</td> <td>When this bit is set VSL will make extra fetch to memory to fetch the MB data for top MB.</td> </tr> </tbody> </table>	Project:	CHV, BSW	Value	Name	Description	0	Disable <b>[Default]</b>	VSL will only fetch the current MB data.	1	Enable	When this bit is set VSL will make extra fetch to memory to fetch the MB data for top MB.
	Project:	CHV, BSW											
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1	Enable	When this bit is set VSL will make extra fetch to memory to fetch the MB data for top MB.											
[ExistsIf]Encode Only													
8	31:24	<b>SliceDeltaQpMax[3]</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">S7</td> </tr> </table> <p>Range: [0:MAX_QP_DELTA]</p> <p>This field is the Slice level delta QP for total bit-count above FrameBitRateMax - first 1/8 region. This field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame exceeds FrameBitRateMax but is within 1/8 of FrameBitRateMaxDelta above FrameBitRateMax, i.e., in the range of (FrameBitRateMax, (FrameBitRateMax+ FrameBitRateMaxDelta»3).</p>	Format:	S7									
	Format:	S7											
23:16	<b>SliceDeltaQpMax[2]</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U8</td> </tr> </table>	Format:	U8										
Format:	U8												
[ExistsIf]Encode Only													

<b>MFX_AVC_IMG_STATE</b>			
	<p>Range: [0:MAX_QP_DELTA]</p> <p>This field is the Slice level delta QP for bit-count above FrameBitRateMax - above 1/8 and below 1/4 This field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame is between 1/8 and 1/4 of FrameBitRateMaxDelta above FrameBitRateMax, i.e., in the range of ((FrameBitRateMax+ FrameBitRateMaxDelta»3), (FrameBitRateMax+ FrameBitRateMaxDelta»2).</p>		
	<p><b>15:8 SliceDeltaQpMax[1]</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">S7</td> </tr> </table> <p>Range: [0:MAX_QP_DELTA]</p> <p>This field is the Slice level delta QP for bit-count above FrameBitRateMax - above 1/4 and below 1/2 This field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame is between 1/4 and 1/2 of FrameBitRateMaxDelta above FrameBitRateMax, i.e., in the range of ((FrameBitRateMax+ FrameBitRateMaxDelta»2), (FrameBitRateMax+ FrameBitRateMaxDelta»1).</p>	Format:	S7
Format:	S7		
	<p><b>7:0 SliceDeltaQpPMax[0]</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">S7</td> </tr> </table> <p>Range: [0:MAX_QP_DELTA]</p> <p>This field is the Slice level delta QP for bit-count above FrameBitRateMax - above 1/2 This field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame is above FrameBitRateMax by more than half the distance of FrameBitRateMaxDelta , i.e., in the range of ((FrameBitRateMax+ FrameBitRateMaxDelta»1), infinite).</p>	Format:	S7
Format:	S7		
9	<p><b>31:24 SliceDeltaQpMin[3]</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">S7</td> </tr> </table> <p>Range: [0:MAX_QP_DELTA]</p> <p>This field is the Slice level delta QP for total bit-count below FrameBitRateMin - first 1/8 region This field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame is less than FrameBitRateMin and greater than or equal to 1/8 the distance of FrameBitRateMinDelta from FrameBitRateMin, i.e., in the range of [(FrameBitRateMin- FrameBitRateMinDelta»3), FrameBitRateMin).</p>	Format:	S7
Format:	S7		
[ExistsIf]Encode Only	<p><b>23:16 SliceDeltaQpMin[2]</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">S7</td> </tr> </table> <p>Range: [0:MAX_QP_DELTA]</p> <p>This field is the Slice level delta QP for bit-count below FrameBitRateMin - below 1/8</p>	Format:	S7
Format:	S7		

<b>MFX_AVC_IMG_STATE</b>											
		and above 1/ 4This field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame is between one-eighth and quarter the distance of FrameBitRateMinDelta from FrameBitRateMin, i.e., in the range of [(FrameBitRateMin- FrameBitRateMinDelta»2), (FrameBitRateMin- FrameBitRateMinDelta»3)).									
	15:8	<p><b>SliceDeltaQpMin[1]</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">S7</td> </tr> </table> <p>Range: [0:MAX_QP_DELTA]</p> <p>This field is the Slice level delta QP for bit-count below FrameBitRateMin- below 1/4 and above 1/ 2This field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame is between quarter and half the distance of FrameBitRateMinDelta from FrameBitRateMin, i.e., in the range of [(FrameBitRateMin- FrameBitRateMinDelta»1), (FrameBitRateMin- FrameBitRateMinDelta»2)).</p>	Format:	S7							
Format:	S7										
	7:0	<p><b>SliceDeltaQpMin[0]</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">S7</td> </tr> </table> <p>Range: [0:MAX_QP_DELTA]</p> <p>This field is the Slice Level Delta QP for bit-count below FrameBitRateMin - below 1/ 2This field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame is below FrameBitRateMin by more than half the distance of FrameBitRateMinDelta , i.e., in the range of [0, (FrameBitRateMin- FrameBitRateMinDelta»1).</p>	Format:	S7							
Format:	S7										
10  [ExistsIf]Encode Only	31	<p><b>FrameBitrateMaxUnit</b></p> <p>This field is the Frame Bitrate Maximum Limit Units.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 10%;">Name</th> <th style="width: 80%;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Byte</td> <td>FrameBitRateMax is in units of 32 Bytes when FrameBitrateMaxUnitMode is 1 and in units of 128 Bytes if FrameBitrateMaxUnitMode is 0</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Kilo Byte</td> <td>FrameBitRateMax is in units of 4KBytes Bytes when FrameBitrateMaxUnitMode is 1 and in units of 16KBytes if FrameBitrateMaxUnitMode is 0</td> </tr> </tbody> </table>	Value	Name	Description	0	Byte	FrameBitRateMax is in units of 32 Bytes when FrameBitrateMaxUnitMode is 1 and in units of 128 Bytes if FrameBitrateMaxUnitMode is 0	1	Kilo Byte	FrameBitRateMax is in units of 4KBytes Bytes when FrameBitrateMaxUnitMode is 1 and in units of 16KBytes if FrameBitrateMaxUnitMode is 0
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		0	Byte	FrameBitRateMax is in units of 32 Bytes when FrameBitrateMaxUnitMode is 1 and in units of 128 Bytes if FrameBitrateMaxUnitMode is 0							
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30	<p><b>FrameBitrateMaxUnitMode</b></p> <p>This field is the Frame Bitrate Maximum Limit Units.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 10%;">Name</th> <th style="width: 80%;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0h</td> <td>compatibility mode</td> <td>FrameBitRateMaxUnit is in old mode (128b/16Kb)</td> </tr> <tr> <td style="text-align: center;">1h</td> <td>New mode</td> <td>FrameBitRateMaxUnit is in new mode (32byte/4Kb)</td> </tr> </tbody> </table>	Value	Name	Description	0h	compatibility mode	FrameBitRateMaxUnit is in old mode (128b/16Kb)	1h	New mode	FrameBitRateMaxUnit is in new mode (32byte/4Kb)	
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	0h	compatibility mode	FrameBitRateMaxUnit is in old mode (128b/16Kb)								
1h	New mode	FrameBitRateMaxUnit is in new mode (32byte/4Kb)									
29:16	<p><b>FrameBitRateMax</b></p> <p>This field is the Frame Bitrate Maximum Limit. This field along with FrameBitrateMaxUnit determines maximum allowed bits in a frame before multi-pass gets triggered (when</p>										

<b>MFX_AVC_IMG_STATE</b>															
		<p>enabled). In other words, multi-pass is triggered when the actual frame byte count exceeds this value. When FrameBitrateMaxUnitMode is 0(compatibility mode) bits 16:27 should be used, bits 28 and 29 should be 0..</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0-512KB</td> <td></td> <td>The programmable range is 0-512KB when FrameBitrateMaxUnit is 0.</td> </tr> <tr> <td>0-8190KB</td> <td></td> <td>The programmable range is 0-8190KB when FrameBitrateMaxUnit is 1.</td> </tr> </tbody> </table>	Value	Name	Description	0-512KB		The programmable range is 0-512KB when FrameBitrateMaxUnit is 0.	0-8190KB		The programmable range is 0-8190KB when FrameBitrateMaxUnit is 1.				
Value	Name	Description													
0-512KB		The programmable range is 0-512KB when FrameBitrateMaxUnit is 0.													
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	15	<p><b>FrameBitrateMinUnit</b> This field is the Frame Bitrate Minimum Limit Units.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Byte</td> <td>FrameBitRateMax is in units of 32 Bytes when FrameBitrateMinUnitMode is 1 and in units of 128 Bytes if FrameBitrateMinUnitMode is 0</td> </tr> <tr> <td>1</td> <td>Kilo Byte</td> <td>FrameBitRateMax is in units of 4KBytes Bytes when FrameBitrateMaxUnitMode is 1 and in units of 16KBytes if FrameBitrateMaxUnitMode is 0</td> </tr> </tbody> </table>	Value	Name	Description	0	Byte	FrameBitRateMax is in units of 32 Bytes when FrameBitrateMinUnitMode is 1 and in units of 128 Bytes if FrameBitrateMinUnitMode is 0	1	Kilo Byte	FrameBitRateMax is in units of 4KBytes Bytes when FrameBitrateMaxUnitMode is 1 and in units of 16KBytes if FrameBitrateMaxUnitMode is 0				
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	14	<p><b>FrameBitrateMinUnitMode</b> This field is the Frame Bitrate Minimum Limit Units.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Compatibility mode</td> <td>FrameBitRateMaxUnit is in old mode (128b/16Kb)</td> </tr> <tr> <td>1h</td> <td>New mode</td> <td>FrameBitRateMaxUnit is in new mode (32byte/4Kb)</td> </tr> </tbody> </table>	Value	Name	Description	0h	Compatibility mode	FrameBitRateMaxUnit is in old mode (128b/16Kb)	1h	New mode	FrameBitRateMaxUnit is in new mode (32byte/4Kb)				
Value	Name	Description													
0h	Compatibility mode	FrameBitRateMaxUnit is in old mode (128b/16Kb)													
1h	New mode	FrameBitRateMaxUnit is in new mode (32byte/4Kb)													
	13:0	<p><b>FrameBitRateMin</b> RangeThe programmable range 0-512KB When FrameBitrateMinUnit is in 0.Programmable range is 0-8190 KB when FrameBitrateMinUnit is in 1.This field is the Frame Bitrate Minimum Limit ( )This field along with FrameBitrateMinUnit determines minimum allowed bits in a Frame before Multi-Pass gets triggered (when enabled). In other words, multi-pass is triggered when the actual frame byte count is less than this value. When FrameBitrateMinUnitMode is 0 (compatibility mode) bits 0:11 should be used, bits 12 and 13 should be 0.</p>													
11	31	<b>Slice Stats Streamout Enable</b>													
	30:16	<p><b>FrameBitRateMaxDelta</b></p> <table border="1"> <tr> <td>Format:</td> <td>U15</td> </tr> </table> <p>This field is used to select the slice delta QP when FrameBitRateMax Is exceeded. It shares the same FrameBitrateMaxUnit. When FrameBitrateMaxUnitMode is 0(compatibility mode) bits 16:27 should be used, bits 28, 29 and 30 should be 0.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0-1024KB</td> <td></td> <td>The Programmable range 0-1024KB when FrameBitRateMaxUnit is 0.</td> </tr> <tr> <td>0-16380KB</td> <td></td> <td>The Programmable range is 0-16380KB when FrameBitRateMaxUnit is 1.</td> </tr> <tr> <td>0h</td> <td><b>[Default]</b></td> <td></td> </tr> </tbody> </table>	Format:	U15	Value	Name	Description	0-1024KB		The Programmable range 0-1024KB when FrameBitRateMaxUnit is 0.	0-16380KB		The Programmable range is 0-16380KB when FrameBitRateMaxUnit is 1.	0h	<b>[Default]</b>
Format:	U15														
Value	Name	Description													
0-1024KB		The Programmable range 0-1024KB when FrameBitRateMaxUnit is 0.													
0-16380KB		The Programmable range is 0-16380KB when FrameBitRateMaxUnit is 1.													
0h	<b>[Default]</b>														
[ExistsIf]Encode Only															

<b>MFX_AVC_IMG_STATE</b>													
	15	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ									
	Format:	MBZ											
14:0	<b>FrameBitRateMinDelta</b> Range: The programmable range 0-1024KB When FrameBitrateMinUnit is in 32Bytes. Programmable range is 0-16380KB when FrameBitrateMinUnit is in 4Kbytes. This field is used to select the slice delta QP when FrameBitRateMin Is exceeded. It shares the same FrameBitrateMinUnit. When FrameBitrateMinUnitMode is 0(compatibility mode) bits 0:11 should be used, bits 12, 13 and 14 should be 0. Note: HW requires the following condition $FrameBitRateMinDelta \leq 2 * FrameBitRateMinMust$ be true, otherwise it may cause unpredicted behavior.												
12	31:21	<b>Reserved</b>											
	20	<b>VMD Error Logic</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>CHV, BSW</td> </tr> </table> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 45%;">Name</th> <th style="width: 40%;">Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Disable <b>[Default]</b></td> <td></td> </tr> <tr> <td>1</td> <td>Enable</td> <td>Error Handling</td> </tr> </tbody> </table>	Project:	CHV, BSW	Value	Name	Description	0	Disable <b>[Default]</b>		1	Enable	Error Handling
	Project:	CHV, BSW											
	Value	Name	Description										
	0	Disable <b>[Default]</b>											
	1	Enable	Error Handling										
	19	<b>Reserved</b>											
	18	<b>VAD Error Logic</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>CHV, BSW</td> </tr> </table> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 20%;">Name</th> <th style="width: 65%;">Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Enable <b>[Default]</b></td> <td>Error reporting ON in case of premature Slice done</td> </tr> <tr> <td>1</td> <td>Disable</td> <td>CABAC Engine will auto decode the bitstream in case of premature slice done.</td> </tr> </tbody> </table>	Project:	CHV, BSW	Value	Name	Description	0	Enable <b>[Default]</b>	Error reporting ON in case of premature Slice done	1	Disable	CABAC Engine will auto decode the bitstream in case of premature slice done.
	Project:	CHV, BSW											
	Value	Name	Description										
0	Enable <b>[Default]</b>	Error reporting ON in case of premature Slice done											
1	Disable	CABAC Engine will auto decode the bitstream in case of premature slice done.											
17	<b>Reserved</b>												
16	<b>Reserved</b>												
15:0	<b>Reserved</b>												
13	31:30	<b>Reserved</b>											
	29	<b>Current Picture Has Performed MMC05</b> Set to 1 if the current Pic has performed the memory_management_control_operation = 5.											
	28:24	<b>Number of Reference Frames</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>U5</td> </tr> </table> <p>Range: Range 0 to MaxDpbSize (= 16 for Level 4.1)</p> Specifies the maximum number of reference frames (frames, field pairs, unpaired field) existed in the current DBP for decoding the current picture.	Format:	U5									
Format:	U5												

<b>MFX_AVC_IMG_STATE</b>							
	<p>23:22 <b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ				
Format:	MBZ						
	<p>21:16 <b>Number of Active Reference Pictures from L1</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>U6-1</td> </tr> </table> <p>Specifies the initial maximum reference index value minus 1 to access the L1 Reference List. It is extracted from PPS. It corresponds to the number of active reference pictures from L1 to decode the current picture. It can be modified by the slice header if num_ref_idx_active_override_flag is set. Only valid for B picture.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>[0,31]</td> <td></td> </tr> </tbody> </table>	Format:	U6-1	Value	Name	[0,31]	
Format:	U6-1						
Value	Name						
[0,31]							
	<p>15:14 <b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ				
Format:	MBZ						
	<p>13:8 <b>Number of Active Reference Pictures from L0</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>U6-1</td> </tr> </table> <p>Specifies the initial maximum reference index value minus 1 to access the L0 Reference List. It is extracted from PPS. It corresponds to the number of active reference pictures from L0 to decode the current picture. It can be modified by the slice header if num_ref_idx_active_override_flag is set. Valid for both P and B pictures.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>[0,31]</td> <td></td> </tr> </tbody> </table>	Format:	U6-1	Value	Name	[0,31]	
Format:	U6-1						
Value	Name						
[0,31]							
	<p>7:0 <b>Initial QP Value</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>S7</td> </tr> </table> <p>Range: [-26,25]</p> <p>Initial QP value for a Slice, extracted from PPS. It may further get modified by slice_qp_delta in slice header and mb_qp_delta in MB header.</p>	Format:	S7				
Format:	S7						
14	<p>31:24 <b>Log2_max_pic_order_cnt_lsb_minus4</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 40%;">Exists If:</td> <td>//Short Format Only</td> </tr> </table> <p>It is a SPS syntax element, used to determine how many bits in the bitstream are used to represent pic_order_cnt_lsb syntax element in the slice header. Unsigned</p>	Exists If:	//Short Format Only				
Exists If:	//Short Format Only						
[ExistsIf] Short Format only	<p>23:16 <b>Log2_max_frame_num_minus4</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 40%;">Exists If:</td> <td>//Short Format Only</td> </tr> </table> <p>It is a SPS syntax element, used to determine how many bits in the bitstream are used to represent frame_num syntax element in the slice header. Unsigned.</p>	Exists If:	//Short Format Only				
Exists If:	//Short Format Only						
	<p>15 <b>deblocking_filter_control_present_flag</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 40%;">Exists If:</td> <td>//Short Format Only</td> </tr> </table> <p>It is a PPS syntax element, indicates if more deblocking filter control syntax elements are present in the slice header.</p>	Exists If:	//Short Format Only				
Exists If:	//Short Format Only						

<b>MFX_AVC_IMG_STATE</b>		
	14:12	<b>num_slice_groups_minus1</b> Exists If: //Short Format Only BitField It is a PPS syntax element. Use for Slice Header parsing only, to read in slice_group_change_cycle, if any, but is not used by H/W, i.e. no slice group support. Desc
	11	<b>redundant_pic_cnt_present_flag</b> Exists If: //Short Format Only It is a PPS syntax element. Use for Slice Header parsing only, to read-in redundant_pic_cnt, if any, but is not used by H/W, i.e. no support for redundant slice processing.
	10:8	<b>slice_group_map_type</b> Exists If: //Short Format Only It is a PPS syntax element. Use for Slice Header parsing only, to read in slice_group_change_cycle, if any, but is not used by H/W, i.e. no slice group support.
	7:4	<b>Reserved</b>
	3:2	<b>Pic_order_cnt_type</b> Exists If: //Short Format Only It is a SPS syntax element. Use for Slice Header parsing only.
	1	<b>Delta_pic_order_always_zero_flag</b> Exists If: //Short Format Only It is a SPS syntax element. Use for Slice Header parsing only.
	0	<b>Pic_order_present_flag</b> Exists If: //Short Format Only It is a PPS syntax element. Use for Slice Header parsing only.
15 [ExistsIf] Short Format only	31:16	<b>Curr Pic Frame Num</b> Exists If: //Short Format Only Format: U16 Derived from Slice Header syntax element
	15:0	<b>Slice Group Change Rate</b> Exists If: //Short Format Only Format: U16-1 It is a PPS syntax element Use for Slice Header parsing only, to read in slice_group_change_cycle, if any, but is not used by H/W, i.e. no slice group support.



		<b>MFX_AVC_IMG_STATE</b>			
16	31	<b>Inter View Order Disable</b>			
		Project:	CHV, BSW		
		Exists If:	//Short Format Only		
		It indicates how to append inter-view picture into initial sorted reference list. (due to ambiguity in the MVC Spec)			
			<b>Value</b>	<b>Name</b>	<b>Description</b>
			0h	Default <b>[Default]</b>	View Order Ascending
			1h	Disable	View ID Ascending
	30:22	<b>Reserved</b>			
		Project:	CHV, BSW		
	21:18	Format:	MBZ		
<b>Max View IDXL1</b>					
		Project:	CHV, BSW		
		Exists If:	//Short Format Only		
		It is a PPS syntax element corresponding to Anchor/Non-Anchor Reference ListL1 It indicates the maximum number of inter-view picture for Reference List L1			
17:16	<b>Reserved</b>				
	Project:	CHV, BSW			
15:12	Format:	MBZ			
	<b>Max View IDXLO</b>				
		Project:	CHV, BSW		
		Exists If:	//Short Format Only		
		Reference ListL0 It indicates the maximum number of inter-view picture for Reference List L0			
11:10	<b>Reserved</b>				
	Project:	CHV, BSW			
9:0	Format:	MBZ			
	<b>Current Frame View ID</b>				
		Project:	CHV, BSW		
		Exists If:	//Short Format Only		
		It indicates the View ID of the current decoding frame			

## MFX\_AVC\_REF\_IDX\_STATE

<b>MFX_AVC_REF_IDX_STATE</b>				
Project:	CHV, BSW			
Source:	VideoCS			
Length Bias:	2			
<p>This is a slice level command and can be issued multiple times within a picture that is comprised of multiple slices. The same command is used for AVC encoder (PAK mode) and decoder (VLD mode); it is not need in decoder IT mode.</p> <p>The inline data of this command is interpreted differently for encoder as for decoder. For decoder, it is interpreted as RefIdx List L0/L1 as in AVC spec., and it matches with the DXVA2 AVC API data structure for decoder in VLD mode : RefPicList[2][32] (L0:L1, 0:31 RefPic). But for encoder, it is interpreted as a Reference Index Mapping Table for L0 and L1 reference pictures. For packing the bits at the output of PAK, the syntax elements must follow the definition of RefIdxL0/L1 list according to the AVC spec. However, the decoder pipeline was designed to use a variation of that standard definition, as such a conversion (mapping) is needed to support the hardware design.</p> <p>The Reference lists are needed in processing both P and B slice in AVC codec. For P-MB, only L0 list is used; for B-MB both L0 and L1 lists are needed. For a B-MB that is coded in L1-only Prediction, only L1 list is used.</p>				
<b>Programming Notes</b>				
<p>DXVA2 specifies that an application will create the RefPicList L0 and L1 and pass onto the driver. The content of each entry of RefPicList L0/L1[ ] is a 7-bit picture index. This picture index is the same as that of RefFrameList[ ] content. This picture index, however, is not defined the same as the frame store ID (0 to 16, 5-bits) we have implemented in H/W. Hence, driver is required to manage a table to convert between DXVA2 picture index and intel frame store ID. As such, the final RefPicList L0/L1[ ] that the driver passes onto the H/W is not the same as that defined in the DXVA2.</p>				
DWord	Bit	Description		
0	31:29	<b>Command Type</b>		
		Default Value:	3h PARALLEL_VIDEO_PIPE	
		Format:	OpCode	
	28:27	28:27	<b>Pipeline</b>	
			Default Value:	2h MFX_AVC_REF_IDX_STATE
			Format:	OpCode
	26:24	26:24	<b>Command Opcode</b>	
			Default Value:	1h AVC
			Format:	OpCode
	23:21	23:21	<b>SubOpcodeA</b>	
			Default Value:	0h MFX_AVC_REF_IDX_STATE
			Format:	OpCode

<b>MFX_AVC_REF_IDX_STATE</b>										
	20:16	<b>SubOpcodeB</b> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>4h MFX_AVC_REF_IDX_STATE</td> </tr> <tr> <td>Format:</td> <td>OpCode</td> </tr> </table>	Default Value:	4h MFX_AVC_REF_IDX_STATE	Format:	OpCode				
	Default Value:	4h MFX_AVC_REF_IDX_STATE								
	Format:	OpCode								
	15:12	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ						
Format:	MBZ									
11:0	<b>DWord Length</b> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>0008h</td> </tr> <tr> <td>Format:</td> <td>=n</td> </tr> </table> Excludes DWords 0,1	Default Value:	0008h	Format:	=n					
Default Value:	0008h									
Format:	=n									
1	31:1	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ						
	Format:	MBZ								
0	<b>RefPicList Select</b> Num_ref_idx_l1_active is resulted from the specifications in both PPS and Slice Header for the current slice. However, since the full reference list L0 and/or L1 are always sent, only present flags are specified instead. This parameter is specified for Intel interface only, not present in the DXVA. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 75%;">Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>RefPicList 0</td> <td>The list that followed represents RefList L0 (Decoder VLD mode) or Ref Idx Mapping Table L0 (Encoder PAK mode)</td> </tr> <tr> <td>1</td> <td>RefPicList1</td> <td>The list that followed represents RefList L1 (Decoder VLD mode) or Ref Idx Mapping Table L1 (Encoder PAK mode)</td> </tr> </tbody> </table>	Value	Name	Description	0	RefPicList 0	The list that followed represents RefList L0 (Decoder VLD mode) or Ref Idx Mapping Table L0 (Encoder PAK mode)	1	RefPicList1	The list that followed represents RefList L1 (Decoder VLD mode) or Ref Idx Mapping Table L1 (Encoder PAK mode)
Value	Name	Description								
0	RefPicList 0	The list that followed represents RefList L0 (Decoder VLD mode) or Ref Idx Mapping Table L0 (Encoder PAK mode)								
1	RefPicList1	The list that followed represents RefList L1 (Decoder VLD mode) or Ref Idx Mapping Table L1 (Encoder PAK mode)								
2..9	31:0	<b>Reference List Entry</b> This set of fields is always present whenever this command is issued. It always specifies the full 32 reference pictures in the selected list, regardless they are "existing picture" or not. If a picture is non-existing, the corresponding entry should be set to all ones. Each list entry is 1 byte. A 32-bit DW can hold 4 list entries in the following format <ul style="list-style-type: none"> <li>• 31:24 entry X+3 (e.g. listY_3)</li> <li>• 23:16 entry X+2 (e.g. listY_2)</li> <li>• 15:8 entry X+1 (e.g. listY_1)</li> <li>• 7:0 entry X (e.g. listY_0)</li> </ul> X is replaced by the paddr[2:0] * 4 ; paddr[5:0] with 0x20 and 0x27, and Y is replaced by 0 or 1. The byte definition for a reference picture : <ul style="list-style-type: none"> <li>• Bit 7 : Non-Existing - indicates that frame store index that should have been at this entry did not exist and was replaced by an index 0 (a valid entry) for error concealment</li> <li>• Bit 6 : Long term bit - set this reference picture to be used as long term reference</li> <li>• Bit 5 : Field picture flag - indicates frame/field</li> <li>• Bit 4:0 : Frame store index or Frame Store ID (Bit 4:1 is used to form the binding table index in intel implementation)</li> </ul>								

## MFX\_AVC\_REF\_IDX\_STATE

	<p>This is the final Reference List L0 or L1 after any reordering specified in the Slice Header as well as modified by the driver, and its indices values are all translated to the intel specification. If the reference picture is a frame (Bit5 = 1), frame store ID is always an even number. This list is used in outputting MV information by the BSD unit in VLD mode. DMV access also reads and writes Mvlist0 using this frame store ID. If this set of fields is interpreted as Reference Index Mapping Table L0/L1, the same field alignment is followed, i.e. 4 mapping entries per DW. Each mapping entry is one byte in size, but only the least significant 5 bits [4:0] is relevant. Driver should zero all the upper bits [7:5] for each entry.</p>
--	--

## MFX\_AVC\_SLICE\_STATE

<b>MFX_AVC_SLICE_STATE</b>			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>This is a slice level command and can be issued multiple times within a picture that is comprised of multiple slices. The same command is used for AVC encoder (PAK mode) and decoder (VLD and IT modes).</p>			
<b>Programming Notes</b>			
<p>MFX_AVC_SLICE_STATE command is not issued for AVC DXVA2 Short Format Bitstream decode, instead MFD_AVC_SLICEADDR command is executed to retrieve the next slice MB Start Address X and Y by H/W itself.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h MFX_AVC_SLICE_STATE
		Format:	OpCode
	26:24	<b>Command Opcode</b>	
		Default Value:	1h AVC
		Format:	OpCode
	23:21	<b>SubOpcodeA</b>	
Default Value:		0h MFX_AVC_SLICE_STATE	
Format:		OpCode	
20:16	<b>Command SubOpcodeB</b>		
	Default Value:	3h MFX_AVC_SLICE_STATE	
	Format:	OpCode	
15:12	<b>Reserved</b>		
	Format:	MBZ	
11:0	<b>DWord Length</b>	Default Value:	8h DWORD_COUNT_n
		Format:	=n
	Excludes DWords 0,1		
	1	31:4	<b>Reserved</b>
Format:			MBZ

<b>MFX_AVC_SLICE_STATE</b>											
3:0	<p><b>Slice Type</b> It is set to the value of the syntax element read from the Slice Header.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 60%;">Value</th> <th style="width: 40%;">Name</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>P Slice</td> </tr> <tr> <td>0001b</td> <td>B Slice</td> </tr> <tr> <td>0010b</td> <td>I Slice</td> </tr> <tr> <td>0011b-1111b</td> <td>Reserved</td> </tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>Bits[3:2] must be 0</p>	Value	Name	0000b	P Slice	0001b	B Slice	0010b	I Slice	0011b-1111b	Reserved
	Value	Name									
	0000b	P Slice									
	0001b	B Slice									
	0010b	I Slice									
	0011b-1111b	Reserved									
	2	<p>31:30 <b>Reserved</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">MBZ</td> </tr> </table>	Format:	MBZ							
Format:		MBZ									
<p>29:24 <b>Number of Reference Pictures in Inter-prediction List 1</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">U6</td> </tr> </table> <p>This field is valid only for encoding a B Slice, for which it is expected to have at least one entry in the reference list L1; otherwise (if Slice Type is not a B Slice ), this field must be set to 0. This field can be derived for a B Slice from the Slice Header syntax element NumRefIdxActiveMinus1 as, Num_Ref_Idx_L1 = NumRefIdxActiveMinus1[1] + 1.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 60%;">Value</th> <th style="width: 40%;">Name</th> </tr> </thead> <tbody> <tr> <td>0-32</td> <td></td> </tr> </tbody> </table>		Format:	U6	Value	Name	0-32					
Format:		U6									
Value		Name									
0-32											
<p>23:22 <b>Reserved</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">MBZ</td> </tr> </table>	Format:	MBZ									
Format:	MBZ										
<p>21:16 <b>Number of Reference Pictures in Inter-prediction List 0</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">U6</td> </tr> </table> <p>This field is valid for encoding a P or B Slice, for which it is expected to have at least one entry in the reference list L0; otherwise (if Slice Type is not a P or B Slice ), this field must be set to 0. This field can be derived for a P or B Slice from the Slice Header syntax element NumRefIdxActiveMinus1 as, Num_Ref_Idx_L0 = NumRefIdxActiveMinus1[0] + 1.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 60%;">Value</th> <th style="width: 40%;">Name</th> </tr> </thead> <tbody> <tr> <td>0-32</td> <td></td> </tr> </tbody> </table>	Format:	U6	Value	Name	0-32						
Format:	U6										
Value	Name										
0-32											
<p>15:11 <b>Reserved</b></p>											
<p>10:8 <b>Log 2 Weight Denom Chroma</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">U3</td> </tr> </table> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 60%;">Value</th> <th style="width: 40%;">Name</th> </tr> </thead> <tbody> <tr> <td>0-7</td> <td></td> </tr> </tbody> </table>	Format:	U3	Value	Name	0-7						
Format:	U3										
Value	Name										
0-7											
<p>7:3 <b>Reserved</b></p>											

<b>MFX_AVC_SLICE_STATE</b>														
	2:0	<p><b>Log 2 Weight Denom Luma</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U3</td> </tr> </table> <p>It is the base 2 logarithm of the denominator for all Luma weighting factors. It is set to the value of the syntax element read from the Slice Header Pred_Weight_Table().</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>0-7</td> <td></td> </tr> </tbody> </table>	Format:	U3	Value	Name	0-7							
		Format:	U3											
		Value	Name											
		0-7												
3	31:30	<p><b>Weighted Prediction Indicator</b></p> <p>This field indicates the Weighted Prediction mode for a P or B Slice. It is a combined field corresponding to the syntax element WeightedBiPredIdc or WeightedPredFlag read from the current active PPS.</p> <ul style="list-style-type: none"> <li>If it is a B-Slice, these bits are interpreted as:                             <ul style="list-style-type: none"> <li>00b - Specifies the default weighted inter-prediction to be applied</li> <li>01b - Specifies the explicit weighted inter-prediction to be applied</li> <li>10b - Specifies the implicit weighted inter-prediction to be applied</li> <li>11b - Reserved (not allowed)</li> </ul> </li> <li>If it is a P Slice, these bits are interpreted as:                             <ul style="list-style-type: none"> <li>00b - Disables weighted inter-prediction (Default weighted)</li> <li>01b - Enables weighted inter-prediction (Explicit weighted)</li> <li>10b - 11b - Reserved</li> </ul> </li> </ul> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th colspan="2"><b>Programming Notes</b></th> </tr> </thead> <tbody> <tr> <td colspan="2">Only when in B Slice with Weighted_Pred_Idc = 1 (explicit weighted prediction), will there be a L1 and/or a L0 weight+offset tables being sent to the BSD unit through the Slice_State command. Only when in P Slice with Weighted_Pred_Idc = 1, will there be a L0 weight+offset table being sent to the BSD.</td> </tr> <tr> <td colspan="2">If Weighted_Pred_Idc != 1 for B Slice or Weighted_Pred_Idc =0 for P Slice, no Slice_State command should be issued to send these tables. If still being issued, the data is read but ignored.</td> </tr> <tr> <td colspan="2">DXVA specifies Weighted_Bipred and Weighted_Pred in frame-level state. However, these two flags are combined and specified in slice level for both P and B slice type.</td> </tr> </tbody> </table>	<b>Programming Notes</b>		Only when in B Slice with Weighted_Pred_Idc = 1 (explicit weighted prediction), will there be a L1 and/or a L0 weight+offset tables being sent to the BSD unit through the Slice_State command. Only when in P Slice with Weighted_Pred_Idc = 1, will there be a L0 weight+offset table being sent to the BSD.		If Weighted_Pred_Idc != 1 for B Slice or Weighted_Pred_Idc =0 for P Slice, no Slice_State command should be issued to send these tables. If still being issued, the data is read but ignored.		DXVA specifies Weighted_Bipred and Weighted_Pred in frame-level state. However, these two flags are combined and specified in slice level for both P and B slice type.					
		<b>Programming Notes</b>												
		Only when in B Slice with Weighted_Pred_Idc = 1 (explicit weighted prediction), will there be a L1 and/or a L0 weight+offset tables being sent to the BSD unit through the Slice_State command. Only when in P Slice with Weighted_Pred_Idc = 1, will there be a L0 weight+offset table being sent to the BSD.												
		If Weighted_Pred_Idc != 1 for B Slice or Weighted_Pred_Idc =0 for P Slice, no Slice_State command should be issued to send these tables. If still being issued, the data is read but ignored.												
		DXVA specifies Weighted_Bipred and Weighted_Pred in frame-level state. However, these two flags are combined and specified in slice level for both P and B slice type.												
29	<b>Direct Prediction Type</b>	Type of direct prediction used for B Slices. This field is valid only for Slice_Type = B Slice; otherwise, it must be set to 0.												
		<table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Temporal</td> </tr> <tr> <td>1</td> <td>Spatial</td> </tr> </tbody> </table>	Value	Name	0	Temporal	1	Spatial						
		Value	Name											
0	Temporal													
1	Spatial													
28:27	<b>Disable Deblocking Filter Indicator</b>	<table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 70%;">Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td></td> <td>FilterInternalEdgesFlag is set equal to 1</td> </tr> <tr> <td>01b</td> <td></td> <td>Disable all deblocking operation, no deblocking parameter syntax element is read; filterInternalEdgesFlag is set equal to 0</td> </tr> <tr> <td>10b</td> <td></td> <td>Macroblocks in different slices are considered not available;</td> </tr> </tbody> </table>	Value	Name	Description	00b		FilterInternalEdgesFlag is set equal to 1	01b		Disable all deblocking operation, no deblocking parameter syntax element is read; filterInternalEdgesFlag is set equal to 0	10b		Macroblocks in different slices are considered not available;
		Value	Name	Description										
		00b		FilterInternalEdgesFlag is set equal to 1										
		01b		Disable all deblocking operation, no deblocking parameter syntax element is read; filterInternalEdgesFlag is set equal to 0										
10b		Macroblocks in different slices are considered not available;												

<b>MFV_AVC_SLICE_STATE</b>			
			filterInternalEdgesFlag is set equal to 1
	11b	Reserved	Not defined in AVC
26	<b>Reserved</b>		
	Format:		MBZ
25:24	<b>Cabac Init Idc[1:0]</b>		
	Specifies the index for determining the initialization table used in the context variable initialization process.		
	<b>Value</b>	<b>Name</b>	
	0-2		
	<b>Programming Notes</b>		
	Cabac initialization is also dependent on the field/frame picture type, Slice type, and the current SliceQP value.		
23:22	<b>Reserved</b>		
	Format:		MBZ
21:16	<b>Slice Quantization Parameter</b>		
	Quantization Parameter for current slice. Derived from PPS and slice_delta_qp syntax element in Slice Header. It is needed for CABAC context initialization and deblocking filter control. And it is also used as the starting QP value in the very first MB of a slice. It is in the range of unsigned integer 0 to 51, for 8-bit pixel bit-depth.		
15:12	<b>Reserved</b>		
	Format:		MBZ
11:8	<b>Slice Beta Offset Div2</b>		
	Format:		S3 2's Complement
	Range: [-6, 6] Inclusive		
	Specifies the offset used in accessing the deblocking filter strength tables.		
7:4	<b>Reserved</b>		
	Format:		MBZ
3:0	<b>Slice Alpha C0 Offset Div2</b>		
	Format:		S3 2's Complement
	Range: [-6, 6] Inclusive		
	Specifies the offset used in accessing the deblocking filter strength tables.		
4	31:24	<b>Slice Vertical Position</b>	
	This field specifies the position in y-direction of the first macroblock in the Slice in unit of macroblocks. The fields (Slice_MB_Start_Hor_Pos, Slice_MB_Start_Vert_Pos) are valid in VLD (decoding) mode only. They are ignored by hardware in decoding IT mode and encoding mode (whereas the position is provided by the per-macroblock object command). Derived		



		<b>MFX_AVC_SLICE_STATE</b>			
		<b>Programming Notes</b>			
		Error Handling: Driver needs to check if FirstMbY starts at 0 on the first slice of frame. If not, driver needs to add a phantom slice with FirstMbX and FirstMbY set to 0.			
	23:16	<b>Slice Horizontal Position</b> This field specifies the position in x-direction of the first macroblock in the Slice in unit of macroblocks. Derived			
		<b>Programming Notes</b>			
		Error Handling: Driver needs to check if FirstMbY starts at 0 on the first slice of frame. If not, driver needs to add a phantom slice with FirstMbX and FirstMbY set to 0.			
	15	<b>Reserved</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;"></td><td style="width: 50px;">MBZ</td></tr></table>			MBZ
	MBZ				
	14:0	<b>Slice Start Mb Num</b> Exists If: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;"></td><td>//Decoder Only</td></tr></table> The MB number (linear MB address in a picture) at the start of a Slice, it must match with the Slice Horizontal Position (Slice_MB_Start_Hor_Pos) and Vertical Position (Slice_MB_Start_Vert_Pos) in the picture.			//Decoder Only
	//Decoder Only				
		<b>Programming Notes</b>			
		In creating the Phantom Slice for error concealment, this field should set to the total number of MB in the current picture + 1.			
5	31:24	<b>Reserved</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;"></td><td style="width: 50px;">MBZ</td></tr></table>			MBZ
		MBZ			
	23:16	<b>Next Slice Vertical Position</b> This field specifies the position in y-direction of the first macroblock in the next Slice in unit of macroblocks. This field is primarily used for error concealment. In the case that current slice is the last slice, this field should set to the height of picture (since y-direction is zero-based numbering).			
	15:8	<b>Reserved</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;"></td><td style="width: 50px;">MBZ</td></tr></table>			MBZ
	MBZ				
7:0	<b>Next Slice Horizontal Position</b> This field specifies the position in x-direction of the first macroblock in the next Slice in unit of macroblocks. This field is primarily used for error concealment. In the case that current slice is the last slice, this field should set to 0.				
6 Encoder Only	31	<b>Rate Control Counter Enable</b> To enable the accumulation of bit allocation for rate control This field enables hardware Rate Control logic. The rest of the RC control fields are only valid when this field is set to 1. Otherwise, hardware ignores these fields.			
		<b>Value</b>	<b>Name</b>		
		0	Disable		
	1	Enable			

<b>MFX_AVC_SLICE_STATE</b>		
30	<b>ResetRateControlCounter</b>	
	To reset the bit allocation accumulation counter to 0 to restart the rate control.	
	<b>Value</b>	<b>Name</b>
	0	Not Reset
	1	Reset
29:28	<b>RC Triggler Mode</b>	
	<b>Value</b>	<b>Name</b>
	00b	Always Rate Control
	01b	Gentle Rate Control
	10b	Loose Rate Control
11b	Reserved	
27:24	<b>RC Stable Tolerance</b>	
	Format:	U4
	This field specifies the tolerance required to deactivate RC once it has been triggered.	
	<b>Value</b>	<b>Name</b>
	0-15	
23	<b>RC Panic Enable</b>	
	If this field is set to 1, RC enters panic mode when sum_act > sum_max. RC Panic Type field controls what type of panic behavior is invoked.	
	<b>Value</b>	<b>Name</b>
	0	Disable
	1	Enable
22	<b>RC Panic Type</b>	
	This field selects between two RC Panic methods	
	<b>Value</b>	<b>Name</b>
	0	QP Panic
	1	CBP Panic
<b>Programming Notes</b>		
If it is set to 0, in panic mode, the macroblock QP is maxed out, setting to requested QP + QP_max_pos_mod. If it is set to 1, for an intra macroblock, AC CBPs are set to zero (note that DC CBPs are not modified). For inter macroblocks, AC and DC CBPs are forced to zero.		
21	<b>MB Type Direct Conversion Disable</b>	
	Exists If:	//B-Slice
For all Macroblock type conversions in different slices, refer to Section "Macroblock Type Conversion Rules" in the same volume.		

<b>MFX_AVC_SLICE_STATE</b>											
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Enable direct mode conversion</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Disable direct mode conversion</td> </tr> </tbody> </table>	Value	Name	0	Enable direct mode conversion	1	Disable direct mode conversion				
Value	Name										
0	Enable direct mode conversion										
1	Disable direct mode conversion										
	<b>Programming Notes</b>										
	This field is zero for all other slices other than B-Slice.										
20	<b>MB Type Skip Conversion Disable</b> Exists If: //P-Slice or B-Slice For all Macroblock type conversions in different slices, refer to Section "Macroblock Type Conversion Rules" in the same volume.										
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Enable skip type conversion</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Disable skip type conversion</td> </tr> </tbody> </table>	Value	Name	0	Enable skip type conversion	1	Disable skip type conversion				
Value	Name										
0	Enable skip type conversion										
1	Disable skip type conversion										
	<b>Programming Notes</b>										
	This field is zero for all other slices other than P_Slice or B-Slice. \										
19	<b>Is Last Slice</b> It is used by the zero filling in the Minimum Frame Size test.										
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">1</td> <td></td> <td>Current slice is the last slice of a picture</td> </tr> <tr> <td style="text-align: center;">0</td> <td></td> <td>Current slice is NOT the last slice of a picture</td> </tr> </tbody> </table>	Value	Name	Description	1		Current slice is the last slice of a picture	0		Current slice is NOT the last slice of a picture	
Value	Name	Description									
1		Current slice is the last slice of a picture									
0		Current slice is NOT the last slice of a picture									
18	<b>Reserved</b>										
17	<b>Header Insertion Present in Bitstream</b>										
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td></td> <td>No header insertion into the output bitstream buffer, in front of the current slice encoded bits.</td> </tr> <tr> <td style="text-align: center;">1</td> <td></td> <td>Header insertion into the output bitstream buffer is present, and is in front of the current slice encoded bits.</td> </tr> </tbody> </table>	Value	Name	Description	0		No header insertion into the output bitstream buffer, in front of the current slice encoded bits.	1		Header insertion into the output bitstream buffer is present, and is in front of the current slice encoded bits.	
Value	Name	Description									
0		No header insertion into the output bitstream buffer, in front of the current slice encoded bits.									
1		Header insertion into the output bitstream buffer is present, and is in front of the current slice encoded bits.									
	<b>Programming Notes</b>										
	Note: In VDEnc mode, the slice header PAK object maximum size is 25 DWs.										
16	<b>SliceData Insertion Present in Bitstream</b>										
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td></td> <td>No Slice Data insertion into the output bitstream buffer</td> </tr> <tr> <td style="text-align: center;">1</td> <td></td> <td>Slice Data insertion into the output bitstream buffer is present.</td> </tr> </tbody> </table>	Value	Name	Description	0		No Slice Data insertion into the output bitstream buffer	1		Slice Data insertion into the output bitstream buffer is present.	
Value	Name	Description									
0		No Slice Data insertion into the output bitstream buffer									
1		Slice Data insertion into the output bitstream buffer is present.									
15	<b>Tail Insertion Present in bitstream</b>										
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td></td> <td>No tail insertion into the output bitstream buffer, after the current slice</td> </tr> </tbody> </table>	Value	Name	Description	0		No tail insertion into the output bitstream buffer, after the current slice				
Value	Name	Description									
0		No tail insertion into the output bitstream buffer, after the current slice									

<b>MFX_AVC_SLICE_STATE</b>			
			encoded bits
	1		Tail insertion into the output bitstream buffer is present, and is after the current slice encoded bits.
	14	<b>Reserved</b>	
		Format:	MBZ
	13	<b>EmulationByteSliceInsertEnable</b> To have PAK outputting SODB or EBSP to the output bitstream buffer	
		<b>Value</b>	<b>Name</b> <b>Description</b>
		0	outputting RBSP
		1	outputting EBSP
	12	<b>CabacZeroWordInsertionEnable</b> To pad the end of a SliceLayer RBSP to meet the encoded size requirement.	
		<b>Value</b>	<b>Name</b> <b>Description</b>
		0	No Cabac_Zero_Word Insertion
		1	Allow internal Cabac_Zero_Word generation and append to the end of RBSP (effectively can be used as an indicator for last slice of a picture, if the assumption is only the last slice of a picture needs to insert CABAC_ZERO_WORDS.
	11:8	<b>Reserved</b>	
		Format:	MBZ
	7:4	<b>Slice ID [3:0]</b> To identify the output data (coding information record) returned for rate control from PAK to ENC and VPP.	
	3:2	<b>Reserved</b>	
		Format:	MBZ
	1:0	<b>Stream ID [1:0]</b> To identify the output data (coding information record) returned for rate control from PAK to ENC and VPP.	
Encoder Only	7	31:29	<b>Reserved</b>
			Format:      MBZ
		28:0	<b>Indirect PAK-BSE Data Start Address (Write)</b>
		Exists If:	//AVC Encode Mode
		This field specifies the memory starting address (offset) to write out the compressed bitstream data from the BSE processing. This pointer is relative to the MFC Indirect PAK-BSE Object Base Address. It is a byte-aligned address for the AVC bitstream data in both CABAC/CAVLC Modes. For Write, there is no need to have a data length field. It is assumed the global memory bound check specified in the IND_OBJ_BASE_ADDRESS command (Indirect PAK-BSE Object Access Upper Bound) will take care of any illegal write access.	

<b>MFX_AVC_SLICE_STATE</b>						
		<table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 60%;">Value</th> <th style="width: 40%;">Name</th> </tr> </thead> <tbody> <tr> <td>0 - 512MB</td> <td></td> </tr> </tbody> </table>	Value	Name	0 - 512MB	
Value	Name					
0 - 512MB						
8  Encoder Only	31:24	<b>Magnitude of QP Max Negative Modifier</b> Format: _____ U8 This field specifies the lower limit of the QP modifier.				
		<table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 60%;">Value</th> <th style="width: 40%;">Name</th> </tr> </thead> <tbody> <tr> <td>0-51</td> <td></td> </tr> </tbody> </table>	Value	Name	0-51	
		Value	Name			
		0-51				
	23:16	<b>Magnitude of QP Max Positive Modifier</b> Format: _____ U8 This field specifies the upper limit of the QP modifier.				
		<table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 60%;">Value</th> <th style="width: 40%;">Name</th> </tr> </thead> <tbody> <tr> <td>0 - 15</td> <td></td> </tr> </tbody> </table>	Value	Name	0 - 15	
	Value	Name				
	0 - 15					
	15:12	<b>Shrink Param - Shrink Resistance</b> Format: _____ U4 This field specifies the additional points added each time decreased correction is invoked.				
		<table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 60%;">Value</th> <th style="width: 40%;">Name</th> </tr> </thead> <tbody> <tr> <td>0 - 15</td> <td></td> </tr> </tbody> </table>	Value	Name	0 - 15	
Value	Name					
0 - 15						
11:8	<b>Shrink Param - Shrink Init</b> Format: _____ U4 This field specifies the initial points required to trip decreased control.					
	<table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 60%;">Value</th> <th style="width: 40%;">Name</th> </tr> </thead> <tbody> <tr> <td>0 - 15</td> <td></td> </tr> </tbody> </table>	Value	Name	0 - 15		
Value	Name					
0 - 15						
7:4	<b>Grow Param - Grow Resistance</b> Format: _____ U4 This field specifies the additional points added each time increased correction is invoked.					
	<table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 60%;">Value</th> <th style="width: 40%;">Name</th> </tr> </thead> <tbody> <tr> <td>0 - 15</td> <td></td> </tr> </tbody> </table>	Value	Name	0 - 15		
Value	Name					
0 - 15						
3:0	<b>Grow Param - Grow Init</b> Format: _____ U4 This field specifies the initial points required to trip increased control.					
	<table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 60%;">Value</th> <th style="width: 40%;">Name</th> </tr> </thead> <tbody> <tr> <td>0 - 15</td> <td></td> </tr> </tbody> </table>	Value	Name	0 - 15		
Value	Name					
0 - 15						
9  Encoder Only	31	<b>RoundInterEnable</b> Format: _____ Enable When this bit is not set, RoundInter defaults to 2.				

<b>MFX_AVC_SLICE_STATE</b>																			
30:28	<b>RoundInter</b> Format: <span style="float: right;">U3</span> Rounding precision for Inter quantized coefficients <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 30%;">Value</th> <th>Name</th> </tr> </thead> <tbody> <tr><td>000b</td><td>+1/16 <b>[Default]</b></td></tr> <tr><td>001b</td><td>+2/16</td></tr> <tr><td>010b</td><td>+3/16</td></tr> <tr><td>011b</td><td>+4/16</td></tr> <tr><td>100b</td><td>+5/16</td></tr> <tr><td>101b</td><td>+6/16</td></tr> <tr><td>110b</td><td>+7/16</td></tr> <tr><td>111b</td><td>+8/16</td></tr> </tbody> </table>	Value	Name	000b	+1/16 <b>[Default]</b>	001b	+2/16	010b	+3/16	011b	+4/16	100b	+5/16	101b	+6/16	110b	+7/16	111b	+8/16
	Value	Name																	
	000b	+1/16 <b>[Default]</b>																	
	001b	+2/16																	
	010b	+3/16																	
	011b	+4/16																	
	100b	+5/16																	
	101b	+6/16																	
	110b	+7/16																	
	111b	+8/16																	
27	<b>RoundIntraEnable</b> Format: <span style="float: right;">Enable</span> When this bit is not set, RoundIntra defaults to 4.																		
	<b>RoundIntra</b> Format: <span style="float: right;">U3</span> Rounding precision for Intra quantized coefficients <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 30%;">Value</th> <th>Name</th> </tr> </thead> <tbody> <tr><td>000b</td><td>+1/16 <b>[Default]</b></td></tr> <tr><td>001b</td><td>+2/16</td></tr> <tr><td>010b</td><td>+3/16</td></tr> <tr><td>011b</td><td>+4/16</td></tr> <tr><td>100b</td><td>+5/16</td></tr> <tr><td>101b</td><td>+6/16</td></tr> <tr><td>110b</td><td>+7/16</td></tr> <tr><td>111b</td><td>+8/16</td></tr> </tbody> </table>	Value	Name	000b	+1/16 <b>[Default]</b>	001b	+2/16	010b	+3/16	011b	+4/16	100b	+5/16	101b	+6/16	110b	+7/16	111b	+8/16
Value	Name																		
000b	+1/16 <b>[Default]</b>																		
001b	+2/16																		
010b	+3/16																		
011b	+4/16																		
100b	+5/16																		
101b	+6/16																		
110b	+7/16																		
111b	+8/16																		
23:20	<b>Correct 6</b> Format: <span style="float: right;">U4</span> This field specifies the points used in the lowermost RC region when $sum\_act \leq sum\_min$ . <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Value</th> <th>Name</th> </tr> </thead> <tbody> <tr><td>0 - 15</td><td></td></tr> </tbody> </table>	Value	Name	0 - 15															
	Value	Name																	
0 - 15																			
19:16	<b>Correct 5</b> Format: <span style="float: right;">U4</span> This field specifies the points used in the fifth RC region when $sum\_act > sum\_min$ but $\leq lower\_midpt$ .																		

<b>MFX_AVC_SLICE_STATE</b>								
		<table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>0 - 15</td> <td></td> </tr> </tbody> </table>	Value	Name	0 - 15			
Value	Name							
0 - 15								
	15:12	<p><b>Correct 4</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U4</td> </tr> </table> <p>This field specifies the points used in the fourth RC region when <math>\text{sum\_act} &gt; \text{lower\_midpt}</math> but <math>\leq \text{sum\_target}</math>.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>0 - 15</td> <td></td> </tr> </tbody> </table>	Format:	U4	Value	Name	0 - 15	
Format:	U4							
Value	Name							
0 - 15								
	11:8	<p><b>Correct 3</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U4</td> </tr> </table> <p>This field specifies the points used in the third RC region when <math>\text{sum\_act} &gt; \text{sum\_target}</math> but <math>\leq \text{upper\_midpt}</math>.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>0 - 15</td> <td></td> </tr> </tbody> </table>	Format:	U4	Value	Name	0 - 15	
Format:	U4							
Value	Name							
0 - 15								
	7:4	<p><b>Correct 2</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U4</td> </tr> </table> <p>This field specifies the points used in the second RC region when <math>\text{sum\_act} &gt; \text{upper\_midpt}</math> but <math>\leq \text{sum\_max}</math>.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>0 - 15</td> <td></td> </tr> </tbody> </table>	Format:	U4	Value	Name	0 - 15	
Format:	U4							
Value	Name							
0 - 15								
	3:0	<p><b>Correct 1</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U4</td> </tr> </table> <p>This field specifies the points used in the topmost RC region when <math>\text{sum\_act} &gt; \text{sum\_max}</math>.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>0 - 15</td> <td></td> </tr> </tbody> </table>	Format:	U4	Value	Name	0 - 15	
Format:	U4							
Value	Name							
0 - 15								
10 Encoder Only	31:28	<b>ClampValues - CV7</b>						
	27:24	<b>CV6</b>						
	23:20	<b>CV5</b>						
	19:16	<b>CV4</b>						
	15:12	<b>CV3</b>						
	11:8	<b>CV2</b>						
	7:4	<b>CV1</b>						
	3:0	<p><b>CV0 - Clamp Value 0</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U4</td> </tr> </table> <p>If the magnitude of coefficients at locations assigned with CV0 (mapping shown below) exceeds <math>2^{\text{CV0}-1}</math>, they are replaced with <math>2^{\text{CV0}-1}</math>. For coefficients at locations marked as 'none', no clamping is performed. The following mappings are only applied to luma and chroma blocks\subblocks containing AC coefficients (blocks\subblocks with only DC coeffs will not be clamped).</p>	Format:	U4				
Format:	U4							

## MFX\_AVC\_SLICE\_STATE

**For 4x4 frame block, each coefficient is mapped to one of the eight CV values as following:**

none	CV7	CV5	CV4
CV7	CV6	CV4	CV3
CV5	CV4	CV2	CV1
CV4	CV3	CV1	CV0

**For 8x8 frame block, each coefficient is mapped to one of the eight CV values as following:**

none	none	CV7	CV6	CV5	CV4	CV3	CV3
none	CV7	CV6	CV5	CV4	CV3	CV3	CV2
CV7	CV6	CV5	CV4	CV3	CV3	CV2	CV2
CV6	CV5	CV4	CV3	CV3	CV2	CV2	CV1
CV5	CV4	CV3	CV3	CV2	CV2	CV1	CV1
CV4	CV3	CV3	CV2	CV2	CV1	CV1	CV0
CV3	CV3	CV2	CV2	CV1	CV1	CV0	CV0
CV3	CV2	CV2	CV1	CV1	CV0	CV0	CV0

**For 4x4 field block, each coefficient is mapped to one of the eight CV values as following:**

none	CV6	CV3	CV1
CV7	CV6	CV3	CV1
CV5	CV4	CV2	CV0
CV5	CV4	CV2	CV0

**For 8x8 field block, each coefficient is mapped to one of the eight CV values as following:**

none	none	CV6	CV5	CV4	CV3	CV2	CV1
none	CV7	CV6	CV5	CV4	CV3	CV2	CV1
CV7	CV6	CV5	CV4	CV3	CV3	CV2	CV1
CV7	CV6	CV5	CV4	CV3	CV2	CV2	CV1
CV6	CV5	CV4	CV4	CV3	CV2	CV1	CV0
CV6	CV5	CV4	CV3	CV2	CV2	CV1	CV0
CV5	CV5	CV4	CV3	CV2	CV1	CV1	CV0
CV5	CV5	CV4	CV3	CV2	CV1	CV1	CV0

Value	Name
0 - 15	



## MFX\_AVC\_WEIGHTOFFSET\_STATE

MFX_AVC_WEIGHTOFFSET_STATE			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>This is a slice level command and can be issued multiple times within a picture that is comprised of multiple slices. The same command is used for AVC encoder (PAK mode) and decoder (VLD and IT modes). However, since for AVC decoder VLD and IT modes, and AVC encoder mode, the implicit weights are computed in hardware, this command is not issued. For encoder, regardless of the type of weight calculation is active for the current slice (default, implicit or explicit), they are all sent to the PAK as if they were all in explicit mode. However, for implicit weight and offset, each entry contains only a 16-bit weight and no offset (offset = 0 always in implicit mode and can be hard-coded inside the hardware).The weights (and offsets) are needed in processing both P and B slice in AVC codec. For P-MB, at most only L0 list is used; for B-MB both L0 and L1 lists may be needed. For a B-MB that is coded in L1-only Prediction, only L1 list is sent.The content of this command matches with the DXVA2 AVC API data structure for explicit prediction mode only : Weights[2][32][3][2] (L0:L1, 0:31 RefPic, Y:Cb:Cr, W:0)</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h MFX_AVC_WEIGHTOFFSET_STATE
		Format:	OpCode
	26:24	<b>Media Command Opcode</b>	
		Default Value:	1h AVC_COMMON
		Format:	OpCode
	23:21	<b>SubOpcode A</b>	
		Default Value:	0h
		Format:	OpCode
	20:16	<b>SubOpcode B</b>	
		Default Value:	5h
Format:		OpCode	
15:12	<b>Reserved</b>		
	Format:	MBZ	
11:0	<b>DWord Length</b>		
	Default Value:	60h Excludes DWord (0,1)	
	Format:	=n Total Length - 2	

<b>MFV_AVC_WEIGHTOFFSET_STATE</b>											
1	31:1	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">MBZ</td> </tr> </table>	Format:	MBZ							
	Format:	MBZ									
0	<p><b>Weight and Offset Select</b></p> <p>It must be set in consistent with the WeightedPredFlag and WeightedBiPredIdc in the Img_State command. This parameter is specified for Intel interface only, not present in the DXVA. For implicit even though only one entry may be used, still loading the whole 32-entry table.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 30%;">Name</th> <th style="width: 60%;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Weight and Offset L0 table</td> <td>The list that followed is associated with the weight and offset for RefPicList L0</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Weight and Offset L1 table</td> <td>The list that followed is associated with the weight and offset for RefPicList L1</td> </tr> </tbody> </table>		Value	Name	Description	0	Weight and Offset L0 table	The list that followed is associated with the weight and offset for RefPicList L0	1	Weight and Offset L1 table	The list that followed is associated with the weight and offset for RefPicList L1
Value	Name	Description									
0	Weight and Offset L0 table	The list that followed is associated with the weight and offset for RefPicList L0									
1	Weight and Offset L1 table	The list that followed is associated with the weight and offset for RefPicList L1									
2..97	31:0	<p><b>WeightOffset</b></p> <p>WeightOffset[L=L0=0 or L1=1][i=0 to 31][Y=0/Cb=1/Cr=2][weight=0/offset=1]            WeightOffset[L][ i=0][Y=0][Weight=0], WeightOffset[L][i=0][Y=0][Offset=1] WeightOffset[L][ i=0][Cb=1][Weight=0], WeightOffset[L][ i=0][Cb=1][Offset=1] WeightOffset[L][ i=0][Cr=2][Weight=0], WeightOffset[L][ i=0][Cr=2][Offset=1]: WeightOffset[L][ i=31][Y=0][Weight=0], WeightOffset[L][ i=31][Y=0][Offset=1] WeightOffset[L][ i=31][Cb=1][Weight=0], WeightOffset[L][ i=31][Cb=1][Offset=1] WeightOffset[L][ i=31][Cr=2][Weight=0], WeightOffset[L][ i=31][Cr=2][Offset=1]</p> <p>Format for explicit: Both Weight and Offset are S15 in two's compliment, with a valid range from -128 to 128 Format for implicit: S15</p>									

## MFX\_AVC\_WEIGHTOFFSET\_STATE

This set of fields is always present whenever this command is issued. The full table, one entry for each reference picture, is always specified. Any reference list L0/L1[i] that does not exist, the corresponding weight and offset are set to 0. Weight and Offset are 2 byte each. A pair of Weight and Offset forms a dword, with Weight in the LOWER word and Offset in the HIGHER word. WeightOffset[L0=0][i=0 to 31][Y=0] (i.e. luma\_weight\_I0[ i ]) are specified for the weighting and offset factors applied to the luma prediction value for list 0 prediction using RefPicList0[ i ] (one-to-one correspondence in i). When luma\_weight\_I0\_flag (Slice Header syntax element) is equal to 1, the value of luma\_weight\_I0[ i ] shall be in the range of -128 to 127. When luma\_weight\_I0\_flag is equal to 0, luma\_weight\_I0[ i ] shall be inferred to be equal to 2luma\_log2\_weight\_denom for RefPicList0[ i ]. luma\_log2\_weight\_denom is a Slice Header syntax element. WeightOffset[L0=0][i=0 to 31][Cb=1] (i.e. chromaCb\_weight\_I0[ i ]) are specified for the weighting and offset factors applied to the chroma Cb prediction values for list 0 prediction using RefPicList0[ i ] (one-to-one correspondence in i). When chroma\_weight\_I0\_flag (Slice Header syntax element) is equal to 1, the value of chromaCb\_weight\_I0[ i ] shall be in the range of -128 to 127. When chroma\_weight\_I0\_flag is equal to 0, chromaCb\_weight\_I0[ i ] shall be inferred to be equal to 2chroma\_log2\_weight\_denom for RefPicList0[ i ]. chroma\_log2\_weight\_denom is a Slice Header syntax element. WeightOffset[L0=0][i=0 to 31][Cr=2] (i.e. chromaCr\_weight\_I0[ i ]) are specified for the weighting and offset factors applied to the chroma Cr prediction values for list 0 prediction using RefPicList0[ i ] (one-to-one correspondence in i). When chroma\_weight\_I0\_flag (Slice Header syntax element) is equal to 1, the value of chromaCr\_weight\_I0[ i ] shall be in the range of -128 to 127. When chroma\_weight\_I0\_flag is equal to 0, chromaCr\_weight\_I0[ i ] shall be inferred to be equal to 2chroma\_log2\_weight\_denom for RefPicList0[ i ].

## MFX\_BSP\_BUF\_BASE\_ADDR\_STATE

MFX_BSP_BUF_BASE_ADDR_STATE			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>This frame-level state command is used to specify all the buffer base addresses needed for the operation of the AVC Bit Stream Processing Units (for decoder, it is BSD Unit; for encoder, it is BSE Unit) For both encoder and decoder, currently it is assumed that all codec standards can share the same BSP_BUF_BASE_STATE. The simplicity of this command is the result of moving all the direct MV related processing into the ENC Subsystem. Since all implicit weight calculations and directMV calculations are done in ENC and all picture buffer management are done in the Host, there is no need to provide POC (POC List - FieldOrderCntList, CurrPic POC - CurrFieldOrderCnt) information to PAK. For decoder, all the direct mode information are sent in a separate slice-level command (AVC_DIRECTMODE_STATE command). In addition, in Encoder, the row stores for CABAC encoding and MB Parameters Construction (MPC) are combined into one single row store. The row stores specified in this command do not combine with those specified in the MFC_PIPE_BUF_ADDR_STATE command for hardware simplification reason.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h Pipeline
		Format:	OpCode
	26:24	<b>Media Command Opcode</b>	
		Default Value:	0h MFX_COMMON_STATE
		Format:	OpCode
	23:21	<b>SubOpcode A</b>	
		Default Value:	0h
		Format:	OpCode
	20:16	<b>SubOpcode B</b>	
		Default Value:	4h
		Format:	OpCode
	15:12	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	11:0	<b>DWord Length</b>	
		Default Value:	8h Excludes DWord (0,1)

<b>MFX_BSP_BUF_BASE_ADDR_STATE</b>						
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>=n Total Length - 2</td> </tr> </table>	Project:	All	Format:	=n Total Length - 2
Project:	All					
Format:	=n Total Length - 2					
1	31:6	<p><b>BSD/MPC Row Store Scratch Buffer Base Address - Read/Write</b></p> <p>This field provides the base address of the scratch buffer used by BSD (decoder) and MPC (encoder) unit to store MB information of the previous row for coding each macroblock in the current row. It is a private buffer used by the BSD (decoder) and MPC (encoder) hardware only. Its content is not accessible by software. This Row Store buffer must be 64-byte cacheline aligned. Hardware uses the horizontal address of the current macroblock to address this Row Store.</p> <p>For AVC BSD, 2 cacheline (CL) per MB when in MBAFF mode (row of MB pair); 1 CL per MB for non-MBAFF. So, to support 256 MBs per row (4K screen resolution), 2 * 256 * 64 bytes = 32,768 bytes are required. Cacheline alignment should be followed. For AVC MPC, 1 cacheline for non-MBAFF, 2 cachelines for MBAFF per MB. For VC1, the BSD row store is 512-bit (one cacheline) per MB, times the number of MBs per picture MB row.</p> <p style="text-align: center;"><b>Programming Notes</b></p> <p>This is one of the four RowStore Scratch Buffers which can programmed to use the internal Media Storage (total size 640 CacheLine). When Deblocking Filter Row Store Scratch Buffer Cache Select is programmed to "1", this will be stored inside MFX Media Internal Storage. Driver then needs to program this Base Address between 0 to 639, indicating starting cacheline address location for this buffer. Driver needs to make sure the whole buffer fits into Media Internal Storage.</p> <p><i>(Notes: 1 cachelines per MB for non-mbaff; 2 cachelines per MB pair for mbaff, and the buffer needs to have enough space for 1 MB (pair) row).</i></p>				
	5:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ
Project:	CHV, BSW					
Format:	MBZ					
2	31:16	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>Reserved for 64-bit address extension.</p>	Project:	CHV, BSW	Format:	MBZ
Project:	CHV, BSW					
Format:	MBZ					
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3	14:13	<p><b>Reserved</b></p>				

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01b	Uncacheable (UC) - non-cacheable																

<b>MFX_BSP_BUF_BASE_ADDR_STATE</b>															
	<table border="1"> <tr> <td>10b</td> <td>Writethrough (WT)</td> </tr> <tr> <td>11b</td> <td>Writeback (WB)</td> </tr> </table>	10b	Writethrough (WT)	11b	Writeback (WB)										
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4:3	<p><b>Target Cache (TC) Bitplane Read Buffer Base Address</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This field controls the L3\$, LLC and eLLC (eDRAM) cacheability for a given surface. Setting of "00" points to PTE settings which defaults to eDRAM (when present). If no eDRAM, the access will be allocated to LLC. Setting of "01", allocates into LLC and victimizes the line to eDRAM. Setting of "10" allows the line to be allocated in either LLC or eDRAM. Setting of "11" is the only option for a memory access to be allocated in L3\$ as well as LLC/eLLC</p> <p>00b: eLLC Only ("00" setting points TC selection to PTE which defaults to eLLC)                      01b: LLC Only (Works at the allocation time, later victimization from LLC downgrades the line to eLLC if present).                      10b: LLC/eLLC Allowed.                      11b: L3, LLC, eLLC Allowed.</p> <p><b>Errata CHV:A-E (FIXED BY:G0 Stepping):</b>                      For all system that does NOT use SVM (i.e. coherent L3\$ surfaces), back snoops from LLC has to be disabled (<b>Dis_GtCvUpdtOnRd = "1"</b>). Than target Cache settings can be programmed as POR requirements of L3/LLC/eDRAM caching.                      For all systems that does use SVM (i.e. coherent L3\$ surfaces), the recommended setting would be "00" in target cache settings. In case of L3 surfaces, the performance has to be tuned between "00" and "11" setting based on the benefits of L3 caching outweighing the degradation of backsnoops.                      Post G0-stepping, the above w/a for coherent L3\$ surfaces is not needed.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>eLLC Only - not snooped in GT</td> </tr> <tr> <td>01b</td> <td>LLC Only</td> </tr> <tr> <td>10b</td> <td>LLC/eLLC Allowed</td> </tr> <tr> <td>11b</td> <td>L3, LLC, eLLC Allowed</td> </tr> </tbody> </table>	Project:	CHV, BSW	Value	Name	00b	eLLC Only - not snooped in GT	01b	LLC Only	10b	LLC/eLLC Allowed	11b	L3, LLC, eLLC Allowed		
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## MFX\_DBK\_OBJECT

<b>MFX_DBK_OBJECT</b>			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h MFX_DBK_OBJECT
		Format:	OpCode
	26:24	<b>Media Command Opcode</b>	
		Default Value:	0h Common
		Format:	OpCode
	23:21	<b>SubOpcode A</b>	
Default Value:		0h	
Format:		OpCode	
20:16	<b>SubOpcode B</b>		
	Default Value:	9h	
	Format:	OpCode	
15:12	<b>Reserved</b>		
	Format:	MBZ	
11:0	<b>DWord Length</b>	Default Value:	0Bh Excludes DWord (0,1)
		Format:	=n
		Note: Regardless of the mode, inline data must be present in this command	
	31:6	<b>Pre Deblocking Source Address</b>	
Format:		GraphicsAddress[31:6]	
Specifies the 4K byte aligned frame buffer address for outputting the non-filtered reconstructed YUV picture (i.e. output of final adder in each codec standard, and prior to the deblocking filter unit).			
1	5:0	<b>Reserved</b>	
		Project:	CHV, BSW
		Format:	MBZ

<b>MFX_DBK_OBJECT</b>													
2 <b>Project:</b> CHV, BSW	31:16	<b>Reserved</b>											
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	Format:	MBZ											
	10:9	<b>Reserved</b>											
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4	31:6	<p><b>Deblocking Control Address</b></p> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[31:6]</td> </tr> </table> <p>Specifies the 4K byte aligned frame buffer address as input MB-level deblocking parameters to control the way hardware deblock the each micro-block. One 512-bit cacheline is allocated for each Macroblock in raster scan order.</p>	Format:	GraphicsAddress[31:6]												
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2	<b>Reserved</b>														
1:0	<p><b>Age for QUADLRU (AGE) for Deblocking Destination Address</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field allows the selection of AGE parameter for a given surface in LLC or eLLC.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>11b</td> <td>Good chance of generating hits</td> </tr> <tr> <td>10b</td> <td>Next good chance of generating hits</td> </tr> <tr> <td>01b</td> <td>Decent chance of generating hits</td> </tr> <tr> <td>00b</td> <td>Poor chance of generating hits</td> </tr> </tbody> </table>	Project:	CHV, BSW	Format:	Enable	Value	Name	11b	Good chance of generating hits	10b	Next good chance of generating hits	01b	Decent chance of generating hits	00b	Poor chance of generating hits
Project:	CHV, BSW														
Format:	Enable														
Value	Name														
11b	Good chance of generating hits														
10b	Next good chance of generating hits														
01b	Decent chance of generating hits														
00b	Poor chance of generating hits														
10	<p>31:6 <b>Deblock Row Store Address</b></p> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[31:6]</td> </tr> </table> <p>This field provides the base address of the scratch buffer (read and write) used by the deblocking filter unit to store MB information of the previous row for filtering of each macroblock in the current row. The Deblocking Filter Row Store buffer must be 64-byte cacheline aligned. Hardware uses the horizontal address of the current macroblock to address the Deblocking Filter Row Store.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Programming Notes</th> </tr> </thead> <tbody> <tr> <td> <p>This is one of the four RowStore Scratch Buffers which can be programmed to use the internal Media Cache (total size 640 CacheLine). When Deblocking Row Store Cache Select is programmed to 1, this will be stored inside MFX Media Internal Storage. Driver then needs to program this Base Address between 0 to 639, indicating starting cachelines address location for this buffer. Driver needs to make sure the whole buffer fits into Media Internal Storage. Also, this command is only for Standalone Deblocker Mode. During Standalone Deblocker Mode, only this Deblock Row Store will be active. There is no other row store active so it can use the whole internal Media Cache. (Notes: 2 cachelines per MB for non-mbaff; 4 cachelines per MB pair for mbaff, and the buffer needs to have enough space for 1</p> </td> </tr> </tbody> </table>	Format:	GraphicsAddress[31:6]	Programming Notes	<p>This is one of the four RowStore Scratch Buffers which can be programmed to use the internal Media Cache (total size 640 CacheLine). When Deblocking Row Store Cache Select is programmed to 1, this will be stored inside MFX Media Internal Storage. Driver then needs to program this Base Address between 0 to 639, indicating starting cachelines address location for this buffer. Driver needs to make sure the whole buffer fits into Media Internal Storage. Also, this command is only for Standalone Deblocker Mode. During Standalone Deblocker Mode, only this Deblock Row Store will be active. There is no other row store active so it can use the whole internal Media Cache. (Notes: 2 cachelines per MB for non-mbaff; 4 cachelines per MB pair for mbaff, and the buffer needs to have enough space for 1</p>										
Format:	GraphicsAddress[31:6]														
Programming Notes															
<p>This is one of the four RowStore Scratch Buffers which can be programmed to use the internal Media Cache (total size 640 CacheLine). When Deblocking Row Store Cache Select is programmed to 1, this will be stored inside MFX Media Internal Storage. Driver then needs to program this Base Address between 0 to 639, indicating starting cachelines address location for this buffer. Driver needs to make sure the whole buffer fits into Media Internal Storage. Also, this command is only for Standalone Deblocker Mode. During Standalone Deblocker Mode, only this Deblock Row Store will be active. There is no other row store active so it can use the whole internal Media Cache. (Notes: 2 cachelines per MB for non-mbaff; 4 cachelines per MB pair for mbaff, and the buffer needs to have enough space for 1</p>															

<b>MFX_DBK_OBJECT</b>									
		MB (pair) row).							
	5:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ			
Project:	CHV, BSW								
Format:	MBZ								
11 <b>Project:</b> CHV, BSW	31:16	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>Reserved for 64-bit address extension.</p>	Project:	CHV, BSW	Format:	MBZ			
	Project:	CHV, BSW							
Format:	MBZ								
	15:0	<p><b>Deblock Row Store Address High</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>This field is for the upper range of Deblock Row Store Address (DeblockRowStoreAddr). This field is used for 48-bit addressing.</p>	Project:	CHV, BSW	Format:	GraphicsAddress[47:32]			
Project:	CHV, BSW								
Format:	GraphicsAddress[47:32]								
12 <b>Project:</b> CHV, BSW	31:15	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ			
	Project:	CHV, BSW							
	Format:	MBZ							
	14:13	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ			
	Project:	CHV, BSW							
	Format:	MBZ							
12	<p><b>Deblock Row Store - Cache Select</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This field controls if Deblock Row Store is going to store inside Media Cache or to LLC.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Buffer going to LLC.</td> </tr> <tr> <td>1</td> <td>Buffer going to Internal Media Storage</td> </tr> </tbody> </table>	Project:	CHV, BSW	Value	Name	0	Buffer going to LLC.	1	Buffer going to Internal Media Storage
Project:	CHV, BSW								
Value	Name								
0	Buffer going to LLC.								
1	Buffer going to Internal Media Storage								
11	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ				
Project:	CHV, BSW								
Format:	MBZ								
10:9	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ				
Project:	CHV, BSW								
Format:	MBZ								
8:7	<p><b>Deblock Row Store - Arbitration Priority Control</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This field controls the priority of arbitration used in the GAC/GAM pipeline for this surface.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> </tbody> </table>	Project:	CHV, BSW	Value	Name				
Project:	CHV, BSW								
Value	Name								

<b>MFX_DBK_OBJECT</b>													
	<table border="1"> <tr> <td>00b</td> <td>Highest priority</td> </tr> <tr> <td>01b</td> <td>Second highest priority</td> </tr> <tr> <td>10b</td> <td>Third highest priority</td> </tr> <tr> <td>11b</td> <td>Lowest priority</td> </tr> </table>	00b	Highest priority	01b	Second highest priority	10b	Third highest priority	11b	Lowest priority				
00b	Highest priority												
01b	Second highest priority												
10b	Third highest priority												
11b	Lowest priority												
6:5	<p><b>Memory Type: LLC/eLLC Cacheability Control (LeLLCCC) for Deblock Row Store Address</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This is the field used in GT interface block to determine what type of access need to be generated to uncore. For the cases where the LeLLCCC is set, cacheable transaction are generated to enable LLC usage for particular stream.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Use Cacheability Controls from page table</td> </tr> <tr> <td>01b</td> <td>Uncacheable (UC) - non-cacheable</td> </tr> <tr> <td>10b</td> <td>Writethrough (WT)</td> </tr> <tr> <td>11b</td> <td>Writeback (WB)</td> </tr> </tbody> </table>	Project:	CHV, BSW	Value	Name	00b	Use Cacheability Controls from page table	01b	Uncacheable (UC) - non-cacheable	10b	Writethrough (WT)	11b	Writeback (WB)
Project:	CHV, BSW												
Value	Name												
00b	Use Cacheability Controls from page table												
01b	Uncacheable (UC) - non-cacheable												
10b	Writethrough (WT)												
11b	Writeback (WB)												
4:3	<p><b>Target Cache (TC) for Deblock Row Store Address</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This field controls the L3\$, LLC and eLLC (eDRAM) cacheability for a given surface. Setting of "00" points to PTE settings which defaults to eDRAM (when present). If no eDRAM, the access will be allocated to LLC. Setting of "01", allocates into LLC and victimizes the line to eDRAM. Setting of "10" allows the line to be allocated in either LLC or eDRAM. Setting of "11" is the only option for a memory access to be allocated in L3\$ as well as LLC/eLLC</p> <p>00b: eLLC Only (<i>"00" setting points TC selection to PTE which defaults to eLLC</i>)          01b: LLC Only (<i>Works at the allocation time, later victimization from LLC downgrades the line to eLLC if present</i>).          10b: LLC/eLLC Allowed.          11b: L3, LLC, eLLC Allowed.</p> <p><b>Errata CHV:A-E (FIXED BY:G0 Stepping):</b>          For all system that does NOT use SVM (i.e. coherent L3\$ surfaces), back snoops from LLC has to be disabled (<b>Dis_GtCvUpdtOnRd = "1"</b>). Than target Cache settings can be programmed as POR requirements of L3/LLC/eDRAM caching.          For all systems that does use SVM (i.e. coherent L3\$ surfaces), the recomend setting would be "00" in target cache settings. In case of L3 surfaces, the performance has to be tuned between "00" and "11" setting based on the benefits of L3 caching outweighing the degradation of backsnoops.          Post G0-stepping, the above w/a for coherent L3\$ surfaces is not needed.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>eLLC Only - not snooped in GT</td> </tr> <tr> <td>01b</td> <td>LLC Only</td> </tr> <tr> <td>10b</td> <td>LLC/eLLC Allowed</td> </tr> <tr> <td>11b</td> <td>L3, LLC, eLLC Allowed</td> </tr> </tbody> </table>	Project:	CHV, BSW	Value	Name	00b	eLLC Only - not snooped in GT	01b	LLC Only	10b	LLC/eLLC Allowed	11b	L3, LLC, eLLC Allowed
Project:	CHV, BSW												
Value	Name												
00b	eLLC Only - not snooped in GT												
01b	LLC Only												
10b	LLC/eLLC Allowed												
11b	L3, LLC, eLLC Allowed												
2	<b>Reserved</b>												

<b>MFX_DBK_OBJECT</b>		
1:0	<b>Age for QUADLRU (AGE) for Deblock Row Store Address</b>	
	Project: CHV, BSW	
	Format: Enable	
	<p>This field allows the selection of AGE parameter for a given surface in LLC or eLLC. If a particular allocation is done at youngest age ("0,1,2") it tends to stay longer in the cache. This option is given to GFX software to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches.</p>	
	<b>Value</b>	<b>Name</b>
	11b	Good chance of generating hits
10b	Next good chance of generating hits	
01b	Decent chance of generating hits	
00b	Poor chance of generating hits	

## MFX\_FQM\_STATE

MFX_FQM_STATE			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>This is a common state command for AVC encoder modes. For encoder, it represents both the forward QM matrices as well as the decoding QM matrices. This is a Frame-level state. Only Scaling Lists specified by an application are being sent to the hardware. The driver is responsible for determining the final set of scaling lists to be used for decoding the current slice, based on the AVC Spec Table 7-2 (Fall-Back Rules A and B). In MFX AVC PAK mode, PAK needs both forward Q scaling lists and IQ scaling lists. The IQ scaling lists are sent as in MFD in raster scan order. But the Forward Q scaling lists are sent in column-wise raster order (column-by-column) to simplify the H/W. Driver will perform all the scan order conversion for both ForwardQ and IQ.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h MFX_MULTI_DW
		Format:	OpCode
	26:24	<b>Media Command Opcode</b>	
		Default Value:	0h MFX_COMMON_STATE
		Format:	OpCode
	23:21	<b>SubOpcode A</b>	
Default Value:		0h	
Format:		OpCode	
20:16	<b>SubOpcode B</b>		
	Default Value:	8h	
	Format:	OpCode	
15:12	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
11:0	<b>DWord Length</b>		
	Default Value:	20h Excludes DWord (0,1)	
	Project:	All	
	Format:	=n Total Length - 2	
1	31:2	<b>Reserved</b>	
		Format:	MBZ

<b>MFX_FQM_STATE</b>													
1:0	<p><b>AVC</b></p> <table border="1"> <tr> <td>Exists If:</td> <td>//AVC- Decoder Only</td> </tr> </table> <p><b>For AVC QM Type:</b> This field specifies which Quantizer Matrix is loaded.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>AVC_4x4_Intra_MATRIX, (Y-4DWs, Cb-4DWs, Cr-4DWs, reserved-4DWs)</td> </tr> <tr> <td>1</td> <td>AVC_4x4_Inter_MATRIX, (Y-4DWs, Cb-4DWs, Cr-4DWs, reserved-4DWs)</td> </tr> <tr> <td>2</td> <td>AVC_8x8_Intra_MATRIX</td> </tr> <tr> <td>3</td> <td>AVC_8x8_Inter_MATRIX</td> </tr> </tbody> </table>	Exists If:	//AVC- Decoder Only	Value	Name	0	AVC_4x4_Intra_MATRIX, (Y-4DWs, Cb-4DWs, Cr-4DWs, reserved-4DWs)	1	AVC_4x4_Inter_MATRIX, (Y-4DWs, Cb-4DWs, Cr-4DWs, reserved-4DWs)	2	AVC_8x8_Intra_MATRIX	3	AVC_8x8_Inter_MATRIX
	Exists If:	//AVC- Decoder Only											
	Value	Name											
	0	AVC_4x4_Intra_MATRIX, (Y-4DWs, Cb-4DWs, Cr-4DWs, reserved-4DWs)											
	1	AVC_4x4_Inter_MATRIX, (Y-4DWs, Cb-4DWs, Cr-4DWs, reserved-4DWs)											
	2	AVC_8x8_Intra_MATRIX											
	3	AVC_8x8_Inter_MATRIX											
	1:0	<p><b>MPEG2</b></p> <table border="1"> <tr> <td>Exists If:</td> <td>//MPEG2- Decoder Only</td> </tr> </table> <p><b>For MPEG2 QM Type:</b> This field specifies which Quantizer Matrix is loaded.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>MPEG_INTRA_QUANTIZER_MATRIX</td> </tr> <tr> <td>1</td> <td>MPEG_NON_INTRA_QUANTIZER_MATRIX</td> </tr> <tr> <td>2-3</td> <td>Reserved</td> </tr> </tbody> </table>	Exists If:	//MPEG2- Decoder Only	Value	Name	0	MPEG_INTRA_QUANTIZER_MATRIX	1	MPEG_NON_INTRA_QUANTIZER_MATRIX	2-3	Reserved	
		Exists If:	//MPEG2- Decoder Only										
		Value	Name										
		0	MPEG_INTRA_QUANTIZER_MATRIX										
		1	MPEG_NON_INTRA_QUANTIZER_MATRIX										
2-3	Reserved												
1:0	<p><b>JPEG</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table> <table border="1"> <tr> <td>Exists If:</td> <td>//JPEG- Encoder Only</td> </tr> </table> <p><b>For JPEG QM Type:</b> This field specifies which Quantizer Matrix is loaded.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>JPEG_Luma_Y_QUANTIZER_MATRIX (or R)</td> </tr> <tr> <td>1</td> <td>JPEG_Chroma_Cb_QUANTIZER_MATRIX (or G)</td> </tr> <tr> <td>2</td> <td>JPEG_Chroma_Cr_QUANTIZER_MATRIX (or B)</td> </tr> </tbody> </table>	Project:	CHV, BSW	Exists If:	//JPEG- Encoder Only	Value	Name	0	JPEG_Luma_Y_QUANTIZER_MATRIX (or R)	1	JPEG_Chroma_Cb_QUANTIZER_MATRIX (or G)	2	JPEG_Chroma_Cr_QUANTIZER_MATRIX (or B)
	Project:	CHV, BSW											
	Exists If:	//JPEG- Encoder Only											
	Value	Name											
	0	JPEG_Luma_Y_QUANTIZER_MATRIX (or R)											
	1	JPEG_Chroma_Cb_QUANTIZER_MATRIX (or G)											
	2	JPEG_Chroma_Cr_QUANTIZER_MATRIX (or B)											
<b>Programming Notes</b>													
For JPEG encoder, each quantization element presents 16-bit $1/QM[i][j]$ . In RGB encoding, because the order input image components can be RGB, GBR, BGR, YUV, the value 0 is used for the first image component, the value 1 is used for the second image component, and the value 2 is used for the third image component.													
2..33	31:0	<p><b>Forward Quantizer Matrix</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>The format of a Quantizer Matrix is an 8x8 matrix in raster order. Each element is an unsigned byte.</p>	Project:	All	Format:	U32							
		Project:	All										
		Format:	U32										

## MFX\_IND\_OBJ\_BASE\_ADDR\_STATE

<b>MFX_IND_OBJ_BASE_ADDR_STATE</b>								
Project:	CHV, BSW							
Source:	VideoCS							
Length Bias:	2							
<p>This state command provides the memory base addresses for all row stores, StreamOut buffer and reconstructed picture output buffers required by the MFD or MFC Engine (that are in addition to the row stores of the Bit Stream Decoding/Encoding Unit (BSD/BSE) and the reference picture buffers). This is a picture level state command and is common among all codec standards and for both encoder and decoder operating modes. However, some fields may only applicable to a specific codec standard. All Pixel Surfaces (original, reference frame and reconstructed frame) in the Encoder are programmed with the same surface state (NV12 and TileY format), except each has its own frame buffer base address. In the tile format, there is no need to provide buffer offset for each slice; since from each MB address, the hardware can calculated the corresponding memory location within the frame buffer directly.</p> <p>The MFX_IND_OBJ_BASE_ADDR command sets the memory base address pointers for the corresponding Indirect Object Data Start Addresses (Offsets) specified in each OBJECT commands. The characteristic of these indirect object data is their variable size (per MB or per Slice). Hence, each OBJECT command must specify the indirect object data offset from the base address to start fetching or writing object data.</p> <p>While the use of base address is unconditional, the indirection can be effectively disabled by setting the base address to zero.</p> <p>For decoder, there are:</p> <ul style="list-style-type: none"> <li>• 1 read-only per-slice indirect object in the BSD_OBJECT Command, and</li> <li>• 2 read-only per-MB indirect objects in the IT_OBJECT Command.</li> </ul> <p>For decoder: the Video Command Streamer (VCS) will perform the memory access bound check automatically using the corresponding MFC Indirect Object Access Upper Bound specification. If any access is at or beyond the upper bound, zero value is returned. The request to memory is still being sent, but the corresponding codec's BSD unit will detect this condition and perform the zeroing return. If the Upper Bound is turned off, the beyond bound request will return whatever on the bus (invalid data).</p> <p>For encoder, there are:</p> <ul style="list-style-type: none"> <li>• 1 read-only per-MB indirect object in the PAK_OBJECT Command, and</li> <li>• 1 write-only per-slice indirect object in the PAK Slice_State Command</li> </ul> <p>For encoder: whenever an out of bound address accessing request is generated, VMX will detect such requests and snap the address to the corresponding [indirect object base address + indirect data start address]. VMX will return all 0s as the data to the requestor. NotationDefinitionPhysicalAddress[n:m] Corresponding bits of a physical graphics memory byte address (not mapped by a GTT) GraphicsAddress[n:m] Corresponding bits of an absolute, virtual graphics memory byte address (mapped by a GTT).</p>								
DWord	Bit	Description						
0	31:29	<table border="1"> <tr> <td colspan="2"><b>Command Type</b></td> </tr> <tr> <td>Default Value:</td> <td>3h PARALLEL_VIDEO_PIPE</td> </tr> <tr> <td>Format:</td> <td>OpCode</td> </tr> </table>	<b>Command Type</b>		Default Value:	3h PARALLEL_VIDEO_PIPE	Format:	OpCode
<b>Command Type</b>								
Default Value:	3h PARALLEL_VIDEO_PIPE							
Format:	OpCode							

<b>MFX_IND_OBJ_BASE_ADDR_STATE</b>						
	28:27	<b>Pipeline</b> <table border="1"> <tr> <td>Default Value:</td> <td>2h MFX_IND_OBJ_BASE_ADDR_STATE</td> </tr> <tr> <td>Format:</td> <td>OpCode</td> </tr> </table>	Default Value:	2h MFX_IND_OBJ_BASE_ADDR_STATE	Format:	OpCode
	Default Value:	2h MFX_IND_OBJ_BASE_ADDR_STATE				
	Format:	OpCode				
	26:24	<b>Common Opcode</b> <table border="1"> <tr> <td>Default Value:</td> <td>0h MFX_IND_OBJ_BASE_ADDR_STATE</td> </tr> <tr> <td>Format:</td> <td>OpCode</td> </tr> </table>	Default Value:	0h MFX_IND_OBJ_BASE_ADDR_STATE	Format:	OpCode
	Default Value:	0h MFX_IND_OBJ_BASE_ADDR_STATE				
	Format:	OpCode				
	23:21	<b>Sub OpcodeA</b> <table border="1"> <tr> <td>Default Value:</td> <td>0h MFX_IND_OBJ_BASE_ADDR_STATE</td> </tr> <tr> <td>Format:</td> <td>OpCode</td> </tr> </table>	Default Value:	0h MFX_IND_OBJ_BASE_ADDR_STATE	Format:	OpCode
	Default Value:	0h MFX_IND_OBJ_BASE_ADDR_STATE				
	Format:	OpCode				
	20:16	<b>SubOpcodeB</b> <table border="1"> <tr> <td>Default Value:</td> <td>3h MFX_IND_OBJ_BASE_ADDR_STATE</td> </tr> <tr> <td>Format:</td> <td>OpCode</td> </tr> </table>	Default Value:	3h MFX_IND_OBJ_BASE_ADDR_STATE	Format:	OpCode
Default Value:	3h MFX_IND_OBJ_BASE_ADDR_STATE					
Format:	OpCode					
15:12	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ			
Format:	MBZ					
11:0	<b>DWord Length</b> <table border="1"> <tr> <td>Default Value:</td> <td>0018h Excludes DWord (0,1)</td> </tr> <tr> <td>Format:</td> <td>=n Total Length - 2</td> </tr> </table>	Default Value:	0018h Excludes DWord (0,1)	Format:	=n Total Length - 2	
Default Value:	0018h Excludes DWord (0,1)					
Format:	=n Total Length - 2					
1	31:12	<b>MFX Indirect Bitstream Object - Base Address (Decoder and Stitch Modes)</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[31:12]</td> </tr> </table> <p>Specifies the 4K-byte aligned memory base address for the read-only indirect data object pointed in the MFD_XXX_BSD_OBJECT command for fetching (reading) the compressed Slice Data. This field is only valid in MPEG2, AVC and VC1 decoder VLD mode.</p>	Project:	All	Format:	GraphicsAddress[31:12]
	Project:	All				
	Format:	GraphicsAddress[31:12]				
11:6	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ			
Format:	MBZ					
5:0	<b>Reserved</b> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ	
Project:	CHV, BSW					
Format:	MBZ					
2	31:16	<b>Reserved</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>Reserved for 64-bit address extension.</p>	Project:	All	Format:	MBZ
	Project:	All				
Format:	MBZ					
15:0	<b>MFX Indirect Bitstream Object - Destination Address (Decoder and Stitch Modes)[47:32]</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> </table>	Project:	All			
Project:	All					



		<b>MFX_IND_OBJ_BASE_ADDR_STATE</b>		
		<b>Description</b>		
		This field is for the upper range of MFX Indirect Bitstream Object Base Address.		
		This field is used for 48-bit addressing.		
3	31:15	<b>Reserved</b>		
		Project:	CHV, BSW	
		Format:	MBZ	
	14:13	<b>Reserved</b>		
		Project:	CHV, BSW	
		Format:	MBZ	
	12:11	<b>Reserved</b>		
		Project:	CHV, BSW	
		Format:	MBZ	
	10:9	<b>Reserved</b>		
		Project:	CHV, BSW	
		Format:	MBZ	
	8:7	<b>MFX Indirect Bitstream ObjectBase - Arbitration Priority Control</b>		
		Project:	CHV, BSW	
		Format:	U2	
		This field controls the priority of arbitration used in the GAC/GAM pipeline for this surface.		
		<b>Value</b>	<b>Name</b>	
00b		Highest priority		
01b		Second highest priority		
10b		Third highest priority		
11b		Lowest priority		
6:5		<b>Memory Type: LLC/eLLC Cacheability Control (LeLLCCC) for MFX Indirect Bitstream ObjectBase Address</b>		
	Project:	CHV, BSW		
	This is the field used in GT interface block to determine what type of access need to be generated to uncore. For the cases where the LeLLCCC is set, cacheable transaction are generated to enable LLC usage for particular stream.			
	<b>Value</b>	<b>Name</b>		
	00b	Use Cacheability Controls from page table		
	01b	Uncacheable (UC) - non-cacheable		
	10b	Writethrough (WT)		
	11b	Writeback (WB)		
	4:3	<b>Target Cache (TC) MFX Indirect Bitstream ObjectBase Address</b>		
		Project:	CHV, BSW	

<b>MFX_IND_OBJ_BASE_ADDR_STATE</b>												
		This field allows the choice of LLC vs eLLC for caching										
		<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>eLLC Only - not snooped in GT</td> </tr> <tr> <td>01b</td> <td>LLC Only</td> </tr> <tr> <td>10b</td> <td>LLC/eLLC Allowed</td> </tr> <tr> <td>11b</td> <td>L3, LLC, eLLC Allowed</td> </tr> </tbody> </table>	Value	Name	00b	eLLC Only - not snooped in GT	01b	LLC Only	10b	LLC/eLLC Allowed	11b	L3, LLC, eLLC Allowed
	Value	Name										
	00b	eLLC Only - not snooped in GT										
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	10b	LLC/eLLC Allowed										
	11b	L3, LLC, eLLC Allowed										
	2	<b>Reserved</b>										
	1:0	<b>Age for QUADLRU (AGE) MFX Indirect Bitstream ObjectBase Address</b>										
		<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table>	Project:	CHV, BSW	Format:	Enable						
Project:	CHV, BSW											
Format:	Enable											
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC.											
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>11b</td> <td>Good chance of generating hits.</td> </tr> <tr> <td>10b</td> <td>Next good chance of generating hits</td> </tr> <tr> <td>01b</td> <td>Decent chance of generating hits</td> </tr> <tr> <td>00b</td> <td>Poor chance of generating hits</td> </tr> </tbody> </table>	Value	Name	11b	Good chance of generating hits.	10b	Next good chance of generating hits	01b	Decent chance of generating hits	00b	Poor chance of generating hits	
Value	Name											
11b	Good chance of generating hits.											
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00b	Poor chance of generating hits											
4	31:12	<b>MFX Indirect Bitstream Object - Access Upper Bound (Decoder and Stitch Modes)</b> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[31:12]</td> </tr> </table> <p>This field specifies the 4K-byte aligned (exclusive) maximum Graphics Memory address access by the indirect data object in the MFD_XXX_BSD_OBJECT command for the compressed Slice Data. Indirect data accessed at this address and beyond will return as 0 by the hardware. Setting this field to 0 will cause this range check to be ignored. If non-zero, this address must be greater than the MFX Indirect Bitstream ObjectBase Address state. Hardware ignores this field if indirect data is not present, i.e. the Indirect Data Length field of the MFD_XXX_BSD_OBJECT command is set to 0. This field is only valid in MPEG2, AVC, VP8, and VC1 decoder VLD mode.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Programming Notes</th> <th style="text-align: center;">Project</th> </tr> </thead> <tbody> <tr> <td>For <b>VP8 Encoder</b>, this field is corresponding to <b>MFC Indirect PAK-BSE Object - Access Upper Bound in DW24, DW25</b>. Please program Indirect bitstream upperbound in this field the same as DW24, DW25.</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Format:	GraphicsAddress[31:12]	Programming Notes	Project	For <b>VP8 Encoder</b> , this field is corresponding to <b>MFC Indirect PAK-BSE Object - Access Upper Bound in DW24, DW25</b> . Please program Indirect bitstream upperbound in this field the same as DW24, DW25.	CHV, BSW				
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Format:	MBZ											
5 <b>Project:</b> CHV, BSW	31:16	<b>Reserved</b>										
		<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ						
		Project:	CHV, BSW									
Format:	MBZ											
Reserved for 64-bit address extension.												
	15:0	<b>MFX Indirect Bitstream Object UpperBound (Decoder and Stitch Modes)[47:32]</b> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table>	Project:	CHV, BSW								
Project:	CHV, BSW											

<b>MFX_IND_OBJ_BASE_ADDR_STATE</b>												
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6	31:12	<p><b>MFX Indirect MV Object - Base Address</b></p> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>GraphicsAddress[31:12]</td> </tr> </table> <p>Specifies the 4K-byte aligned memory base address for the read-only indirect data object pointed in the encoder MFC_AVC_PAK_OBJECT command or the decoder MFD_IT_OBJECT command for fetching the per-MB MV data. This field is only valid in AVC encoder mode or in AVC decoder IT mode</p>	Format:	GraphicsAddress[31:12]								
	Format:	GraphicsAddress[31:12]										
	11:6	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ								
Format:	MBZ											
5:0	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ							
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7 <b>Project:</b> CHV, BSW	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>Reserved for 64-bit address extension.</p>	Project:	CHV, BSW	Format:	MBZ						
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15:0	<p><b>MFX Indirect MV Object Base Address [47:32]</b></p> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> </table> <table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">Description</th> <th style="text-align: center;">Project</th> </tr> </thead> <tbody> <tr> <td>This field is for the upper range of MFX Indirect MV Object Base Address.</td> <td></td> </tr> <tr> <td>This field is used for 48-bit addressing.</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Project:	All	Description	Project	This field is for the upper range of MFX Indirect MV Object Base Address.		This field is used for 48-bit addressing.	CHV, BSW			
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<b>MFX_IND_OBJ_BASE_ADDR_STATE</b>					
12:11	<b>Reserved</b>				
	<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ
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10:9	<b>Reserved</b>				
	<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ
Project:	CHV, BSW				
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8:7	<b>MFX Indirect MV Object - Arbitration Priority Control</b>				
	<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U2</td> </tr> </table>	Project:	CHV, BSW	Format:	U2
	Project:	CHV, BSW			
	Format:	U2			
	This field controls the priority of arbitration used in the GAC/GAM pipeline for this surface.				
	<b>Value</b>	<b>Name</b>			
	00b	Highest priority			
01b	Second highest priority				
10b	Third highest priority				
11b	Lowest priority				
6:5	<b>Memory Type: LLC/eLLC Cacheability Control (LeLLCCC) for MFX Indirect MV ObjectBase Address</b>				
	<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table>	Project:	CHV, BSW		
	Project:	CHV, BSW			
	This is the field used in GT interface block to determine what type of access need to be generated to uncore. For the cases where the LeLLCCC is set, cacheable transaction are generated to enable LLC usage for particular stream.				
	<b>Value</b>	<b>Name</b>			
	00b	Use Cacheability Controls from page table			
	01b	Uncacheable (UC) - non-cacheable			
10b	Writethrough (WT)				
11b	Writeback (WB)				
4:3	<b>Target Cache (TC) MFX Indirect MV ObjectBase Address</b>				
	<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table>	Project:	CHV, BSW		
	Project:	CHV, BSW			
	This field allows the choice of LLC vs eLLC for caching				
	<b>Value</b>	<b>Name</b>			
	00b	eLLC Only - not snooped in GT			
01b	LLC Only				
10b	LLC/eLLC Allowed				
11b	L3, LLC, eLLC Allowed				
2	<b>Reserved</b>				
1:0	<b>Age for QUADLRU (AGE) MFX Indirect MV ObjectBase Address</b>				
	<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table>	Project:	CHV, BSW		
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<b>MFX_IND_OBJ_BASE_ADDR_STATE</b>																
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9	31:12	<p><b>MFX Indirect MV Object Access Upper Bound</b></p> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[31:12]</td> </tr> </table> <p>This field specifies the 4K-byte aligned (exclusive) maximum Graphics Memory address access by the indirect data object in the MFC_AVC_PAK_OBJECT / MFD_IT_OBJECT command for the per-MB MV data. Indirect data accessed at this address and beyond will return as 0 by the hardware. Setting this field to 0 will cause this range check to be ignored. If non-zero, this address must be greater than the MFX Indirect MV Object Base Address state. Hardware ignores this field if indirect data is not present, i.e. the Indirect Data Length field of the MFC_AVC_PAK_OBJECT / MFD_IT_OBJECT command is set to 0. This field is only valid in AVC encoder mode or in AVC decoder IT mode.</p>	Format:	GraphicsAddress[31:12]												
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11:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ													
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10 <b>Project:</b> CHV, BSW	31:16	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>Reserved for 64-bit address extension.</p>	Project:	All	Format:	MBZ										
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This field is for the upper range of MFX Indirect MV Object Base Address.																
This field is used for 48-bit addressing.	CHV, BSW															
11	31:12	<p><b>MFD Indirect IT-COEFF Object - Base Address (Decoder Only)</b></p> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[31:12]</td> </tr> </table> <p>Specifies the 4K-byte aligned memory base address for the read-only indirect data object pointed in the MFD_IT_OBJECT command for fetching (reading) the per-MB non-scaled coefficient data (all inverse scaling and quantization are done in hardware). This field is only valid in MPEG2, AVC and VC1 decoder IT mode.</p>	Format:	GraphicsAddress[31:12]												
	Format:	GraphicsAddress[31:12]														
11:6	<p><b>Reserved</b></p>															

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8:7	<table border="1"> <tr> <td colspan="2"><b>MFC Indirect PAK-BSE Object Desitnation - Arbitration Priority Control</b></td> </tr> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U2</td> </tr> <tr> <td colspan="2">This field controls the priority of arbitration used in the GAC/GAM pipeline for this surface.</td> </tr> <tr> <td style="text-align: center;"><b>Value</b></td> <td style="text-align: center;"><b>Name</b></td> </tr> <tr> <td>00b</td> <td>Highest priority</td> </tr> <tr> <td>01b</td> <td>Second highest priority</td> </tr> <tr> <td>10b</td> <td>Third highest priority</td> </tr> <tr> <td>11b</td> <td>Lowest priority</td> </tr> </table>	<b>MFC Indirect PAK-BSE Object Desitnation - Arbitration Priority Control</b>		Project:	CHV, BSW	Format:	U2	This field controls the priority of arbitration used in the GAC/GAM pipeline for this surface.		<b>Value</b>	<b>Name</b>	00b	Highest priority	01b	Second highest priority	10b	Third highest priority	11b	Lowest priority
<b>MFC Indirect PAK-BSE Object Desitnation - Arbitration Priority Control</b>																			
Project:	CHV, BSW																		
Format:	U2																		
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<b>Value</b>	<b>Name</b>																		
00b	Highest priority																		
01b	Second highest priority																		
10b	Third highest priority																		
11b	Lowest priority																		
6:5	<b>Memory Type: LLC/eLLC Cacheability Control (LeLLCCC) for MFC Indirect PAK-BSE</b>																		

<b>MFX_IND_OBJ_BASE_ADDR_STATE</b>													
	<p><b>ObjectBase Address</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This is the field used in GT interface block to determine what type of access need to be generated to uncore. For the cases where the LeLLCCC is set, cacheable transaction are generated to enable LLC usage for particular stream.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Use Cacheability Controls from page table</td> </tr> <tr> <td>01b</td> <td>Uncacheable (UC) - non-cacheable</td> </tr> <tr> <td>10b</td> <td>Writethrough (WT)</td> </tr> <tr> <td>11b</td> <td>Writeback (WB)</td> </tr> </tbody> </table>	Project:	CHV, BSW	Value	Name	00b	Use Cacheability Controls from page table	01b	Uncacheable (UC) - non-cacheable	10b	Writethrough (WT)	11b	Writeback (WB)
Project:	CHV, BSW												
Value	Name												
00b	Use Cacheability Controls from page table												
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10b	Writethrough (WT)												
11b	Writeback (WB)												
4:3	<p><b>Target Cache (TC) MFC Indirect PAK-BSE ObjectBase Address</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This field controls the L3\$, LLC and eLLC (eDRAM) cacheability for a given surface. Setting of "00" points to PTE settings which defaults to eDRAM (when present). If no eDRAM, the access will be allocated to LLC. Setting of "01", allocates into LLC and victimizes the line to eDRAM. Setting of "10" allows the line to be allocated in either LLC or eDRAM. Setting of "11" is the only option for a memory access to be allocated in L3\$ as well as LLC/eLLC</p> <p>00b: eLLC Only ("00" setting points TC selection to PTE which defaults to eLLC)</p> <p>01b: LLC Only (Works at the allocation time, later victimization from LLC downgrades the line to eLLC if present).</p> <p>10b: LLC/eLLC Allowed.</p> <p>11b: L3, LLC, eLLC Allowed.</p> <p><b>Errata CHV:A-E (FIXED BY:G0 Stepping):</b></p> <p>For all system that does NOT use SVM (i.e. coherent L3\$ surfaces), back snoops from LLC has to be disabled (<b>Dis_GtCvUpdtOnRd = "1"</b>). Than target Cache settings can be programmed as POR requirements of L3/LLC/eDRAM caching.</p> <p>For all systems that does use SVM (i.e. coherent L3\$ surfaces), the recomended setting would be "00" in target cache settings. In case of L3 surfaces, the performance has to be tuned between "00" and "11" setting based on the benefits of L3 caching outweighing the degradation of backsnoops.</p> <p>Post G0-stepping, the above w/a for coherent L3\$ surfaces is not needed.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>eLLC Only - not snooped in GT</td> </tr> <tr> <td>01b</td> <td>LLC Only</td> </tr> <tr> <td>10b</td> <td>LLC/eLLC Allowed</td> </tr> <tr> <td>11b</td> <td>L3, LLC, eLLC Allowed</td> </tr> </tbody> </table>	Project:	CHV, BSW	Value	Name	00b	eLLC Only - not snooped in GT	01b	LLC Only	10b	LLC/eLLC Allowed	11b	L3, LLC, eLLC Allowed
Project:	CHV, BSW												
Value	Name												
00b	eLLC Only - not snooped in GT												
01b	LLC Only												
10b	LLC/eLLC Allowed												
11b	L3, LLC, eLLC Allowed												
2	<b>Reserved</b>												
1:0	<p><b>Age for QUADLRU (AGE) MFC Indirect PAK-BSE ObjectBase Address</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field allows the selection of AGE parameter for a given surface in LLC or eLLC. If a</p>	Project:	CHV, BSW	Format:	Enable								
Project:	CHV, BSW												
Format:	Enable												

<b>MFX_IND_OBJ_BASE_ADDR_STATE</b>													
	<p>particular allocation is done at youngest age (“0,1,2”) it tends to stay longer in the cache. This option is given to GFX software to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>11b</td> <td>Good chance of generating hits</td> </tr> <tr> <td>10b</td> <td>Next good chance of generating hits</td> </tr> <tr> <td>01b</td> <td>Decent chance of generating hits</td> </tr> <tr> <td>00b</td> <td>Poor chance of generating hits</td> </tr> </tbody> </table>	Value	Name	11b	Good chance of generating hits	10b	Next good chance of generating hits	01b	Decent chance of generating hits	00b	Poor chance of generating hits		
Value	Name												
11b	Good chance of generating hits												
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24 <b>Project:</b> CHV, BSW	31:12 <b>MFC Indirect PAK-BSE Object - Access Upper Bound (Eecoder Only)</b> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[31:12]</td> </tr> </table> <p>This field specifies the 4K-byte aligned (exclusive) maximum Graphics Memory address access by the indirect data object in the PAK_SLICE_STATE command for the per-slice output bitstream. Indirect data accessed at this address and beyond will be blocked by the hardware and ignored. Setting this field to 0 will cause this range check to be ignored. If non-zero, this address must be greater than the MFC Indirect PAK-BSE Object Base Address state. This field is only valid in AVC encoder mode.</p> <table border="1"> <thead> <tr> <th>Programming Notes</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>For VP8 Encoder, this field should be programmed the same at both DW4, DW5 <b>MFX Indirect Bitstream Object - Access Upper Bound</b> as well as DW24, DW25.</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Project:	CHV, BSW	Format:	GraphicsAddress[31:12]	Programming Notes	Project	For VP8 Encoder, this field should be programmed the same at both DW4, DW5 <b>MFX Indirect Bitstream Object - Access Upper Bound</b> as well as DW24, DW25.	CHV, BSW				
	Project:	CHV, BSW											
Format:	GraphicsAddress[31:12]												
Programming Notes	Project												
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	11:0 <b>Reserved</b>												
25 <b>Project:</b> CHV, BSW	31:16 <b>Reserved</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>Reserved for 64-bit address extension.</p>	Project:	All	Format:	MBZ								
	Project:	All											
Format:	MBZ												
	15:0 <b>MFC Indirect PAK-BSE Object UpperBound [47:32]</b> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table> <table border="1"> <thead> <tr> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>This field is for the upper range of MFC Indirect PAK-BSE Object UpperBound</td> <td></td> </tr> <tr> <td>This field is used for 48-bit addressing.</td> <td>CHV, BSW</td> </tr> </tbody> </table> <table border="1"> <thead> <tr> <th>Programming Notes</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>For VP8 Encoder, this field should be programmed the same at both DW4, DW5 <b>MFX Indirect Bitstream Object - Access Upper Bound</b> as well as DW24, DW25.</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Project:	CHV, BSW	Description	Project	This field is for the upper range of MFC Indirect PAK-BSE Object UpperBound		This field is used for 48-bit addressing.	CHV, BSW	Programming Notes	Project	For VP8 Encoder, this field should be programmed the same at both DW4, DW5 <b>MFX Indirect Bitstream Object - Access Upper Bound</b> as well as DW24, DW25.	CHV, BSW
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## MFX\_JPEG\_HUFF\_TABLE\_STATE

MFX_JPEG_HUFF_TABLE_STATE								
Project:	CHV, BSW							
Source:	VideoCS							
Length Bias:	2							
<p>This Huffman table commands contains both DC and AC tables for either luma or chroma. Once a Huffman table has been defined for a particular destination, it replaces the previous tables stored in that destination and shall be used in the remaining Scans of the current image. A Huffman table will be sent to H/W only when it is loaded from bitstream.</p>								
DWord	Bit	Description						
0	31:29	<b>Command Type</b>						
		Default Value:	3h PARALLEL_VIDEO_PIPE					
		Format:	OpCode					
	28:27	<b>Pipeline</b>						
		Default Value:	2h MFX_MULTI_DW					
	26:24	<b>Media Command Opcode</b>						
		Default Value:	7h JPEG_COMMON					
	23:21	<b>SubOpcode A</b>						
		Default Value:	0h					
	20:16	<b>SubOpcode B</b>						
Default Value:		2h						
15:12	<b>Reserved</b>							
11:0	<b>DWord Length</b>							
	Default Value:	033Dh Excludes DWord (0,1)						
	Format:	=n Total Length - 2						
1	31:1	<b>Reserved</b>						
	0	<b>HuffTableID (1-bit)</b> Identifies the huffman table.						
<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Y</td> <td>Huffman table for Y</td> </tr> </tbody> </table>			Value	Name	Description	0	Y	Huffman table for Y
Value	Name	Description						
0	Y	Huffman table for Y						

<b>MFX_JPEG_HUFF_TABLE_STATE</b>		
2..4	31:0	<b>DC_BITS (12 8-bit array)</b> The number of DC Huffman codes of length i, where i is 1~12
5..7	31:0	<b>DC_HUFFVAL (12 8-bit array)</b> The value associated with each DC Huffman code of length i.
8..11	31:0	<b>AC_BITS (16 8-bit array)</b> the list of Li, number of Huffman codes of length i, where i is 1~16
12..51	31:0	<b>AC_HUFFVAL (160 8-bit array)</b> the list of Vi,j, the value associated with each Huffman code of length i
52	31:16	<b>Reserved</b>
		Project: All
		Format: MBZ
	15:0	<b>AC_HUFFVAL(2-8 bit array)</b> In AC table, BITS can have up to 16-bit codeword. Li can be 0 ~ 162. HUFFVAL will have a list of likely random distributed values

## MFX\_JPEG\_PIC\_STATE

<b>MFX_JPEG_PIC_STATE</b>			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h MFX_MULTI_DW
		Format:	OpCode
	26:24	<b>Media Command Opcode</b>	
		Default Value:	7h JPEG
		Format:	OpCode
	23:21	<b>SubOpcode A</b>	
Default Value:		0h Common	
Format:		OpCode	
20:16	<b>SubOpcode B</b>		
	Default Value:	0h MEDIA_	
	Format:	OpCode	
15:12	<b>Reserved</b>		
	Format:	MBZ	
11:0	<b>DWord Length</b>	Project:	All
		Format:	=n Total Length - 2
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0001h	[Default]	Excludes DWord (0,1)
1	31	<b>Reserved</b>	
	30:26	<b>Pixels In Horizontal Last MCU</b>	
		Project:	CHV, BSW
		Exists If:	//Encoder Only
		The number of pixels in the last MCU in a row MCUs. This information is used for completion of partial MCU.	



<b>MFX_JPEG_PIC_STATE</b>		
31:21	<b>Reserved</b>	
	Exists If:	//Decoder Only
	Format:	MBZ
25:21	<b>Pixels In Vertical Last MCU</b>	
	Project:	CHV, BSW
	Exists If:	//Encoder Only
The number of pixels in the last MCU in a column MCUs. This information is used for completion of partial MCU.		
20	<b>Vertical Up-Sampling Enable</b>	
	Project:	CHV, BSW
	Exists If:	//Decoder Only
Only applied to chroma blocks. This flag is used for 2:1 vertical up-sampling for chroma 420 and outputting chroma422 YUY2 or UYVY format. To enable this flag, the input should be interleaved Scan, <b>InputFormatYUV</b> should be set to YUV420, and <b>OutputFormatYUV</b> should be set to YUY2 or UYVY.		
	<b>Value</b>	<b>Name</b> <b>Description</b>
	0b	no up-sampling
	1b	2:1 vertical up-sampling
19	<b>Reserved</b>	
	Project:	CHV, BSW
	Exists If:	//Decoder Only
18	<b>Horizontal Down-Sampling Enable</b>	
	Project:	CHV, BSW
	Exists If:	//Decoder Only
Only applied to chroma blocks. This flag is used for 2:1 horizontal down-sampling for chroma 422 and outputting chroma420 NV21 format. To enable this flag, the input should be interleaved Scan, <b>InputFormatYUV</b> should be set to YUV422V_2Y or YUV422V_4Y, and <b>OutputFormatYUV</b> should be set to NV12.		
	<b>Value</b>	<b>Name</b> <b>Description</b>
	0b	no down-sampling
	1b	2:1 horizontal down-sampling
17	<b>Vertical Down-Sampling Enable</b>	
	Project:	CHV, BSW
	Exists If:	//Decoder Only
Only applied to chroma blocks. This flag is used for 2:1 vertical down-sampling for chroma 422 and outputting chroma420 NV21 format. To enable this flag, the input should be interleaved Scan, <b>InputFormatYUV</b> should be set to YUV422H_2Y or YUV422H_4Y, and <b>OutputFormatYUV</b> should be set to NV12.		

<b>MFX_JPEG_PIC_STATE</b>			
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0b		no down-sampling
	1b		2:1 vertical down-sampling
16	<b>Average Down Sampling</b>		
	Project:		CHV, BSW
	Exists If:		//Decoder Only
	This flag is used to select a down-sampling method when <b>VertDownSamplingEnb</b> or <b>HoriDownSamplingEnb</b> is set to 1.		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0b		Drop every other line (or column) pixels
	1b		Average neighboring two pixels
20:12	<b>Reserved</b>		
	Project:		CHV, BSW
	Exists If:		//Encoder Only
	Format:		MBZ
15:12	<b>Reserved</b>		
	Exists If:		//Decoder Only
	Format:		MBZ
11:8	<b>Output Format YUV</b>		
	Project:		CHV, BSW
	Exists If:		//Decoder Only
	This field specifies the surface format to write the decoded JPEG image. Note that any non-interleaved JPEG input should be set to "0000". For the interleaved input Scan data, it can be set either "0000" or the corresponding format.		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0000b		3 separate plane for Y, U, and V respectively
	0001b		NV12 for chroma 4:2:0
	0010b		UYVY for chroma 4:2:2
	0011b		YUY2 for chroma 4:2:2
	<b>Programming Notes</b>		
	The <b>MFX_SURFACE_STATE</b> command should be set accordingly for each <b>OutputFormatYUV</b> . For NV12, <b>Surface Format</b> = 4 (PLANAR_420_8) For YUY2, <b>Surface Format</b> = 0 (YCRCB_NORMAL) For UYVY, <b>Surface Format</b> = 3 (YCRCB_SWAPY) NV12 (0001b) can be set only when Y, U, V are interleaved in a single Scan data with the following cases		
	<ul style="list-style-type: none"> <li><b>InputFormatYUV</b> is YUV420 and <b>VertDownSamplingEnb</b> is disabled</li> </ul>		

## MFX\_JPEG\_PIC\_STATE

- **InputFormatYUV** is YUV422H\_2Y or YUV422H\_4Y, and **VertDownSamplingEnb** is enabled

UYVY (0010b) and YUY2 (0011b) can be set only when Y, U, V are interleaved in a single Scan data with the following cases

- **InputFormatYUV** is YUV420 and **VertUpSamplingEnb** is enabled
- **InputFormatYUV** is YUV422H\_2Y or YUV422H\_4Y and **VertUpSamplingEnb** is disabled

11:8 **Input Surface Format YUV**

Project:	CHV, BSW
Exists If:	//Encoder Only

This field specifies the surface format to read a YUV image data

Value	Name	Description
0000b		Reserved
0001b	NV12	NV12 for chroma 4:2:0
0010b	UYVY	UYVY for chroma 4:2:2
0011b	YUY2	YUY2 for chroma 4:2:2
0100b	Y8	Y8 for chroma400 Y-only image
0101b	RGB	RGB or YUV for chroma 4:4:4

**Programming Notes**

This field should be set accordingly for **SurfaceFormat** in MFX\_SURFACE\_STATE command.

R8G8B8A8\_UNORM in this field is used for encoding RGB and YUV chroma 4:4:4. For RGB input, any order of image components R, G, B (e.g., RGB, GBR, BGR, YUV) will be acceptable as far as the order of Quantization tables and Huffman tables match the order of image components.

7:6 **Reserved**

Exists If:	//Decoder Only
Format:	MBZ

7:6 **Reserved**

Project:	CHV, BSW
Exists If:	//Encoder Only
Format:	MBZ

5:4 **Rotation**

Exists If:	//Decoder Only
------------	----------------

Value	Name	Description
00b		no rotation
01b		rotate clockwise 90 degree
10b		rotate counter-clockwise 90 degree (same as rotating 270 degree clockwise)

<b>MFX_JPEG_PIC_STATE</b>		
	11b	rotate 180 degree (NOT the same as flipped on the x-axis)
	<b>Programming Notes</b>	
	Rotation can be set to 01b, 10b, or 11b when OutputFormatYUV is set to 0000b. For other OutputFormatYUV, Rotation is not allowed.	<b>Project</b> CHV, BSW
5:3	<b>Reserved</b>	
	Project:	CHV, BSW
	Exists If:	//Encoder Only
	Format:	MBZ
3	<b>Reserved</b>	
	Exists If:	//Decoder Only
	Format:	MBZ
2:0	<b>Input Format YUV</b>	
	Exists If:	//Decoder Only
	Format:	U3
	<b>Value</b>	<b>Name</b> <b>Description</b>
	0	<b>[Default]</b> YUV400 (grayscale image)
	1	YUV420
	2	YUV422H_2Y (Horizontally chroma 2:1 subsampled) - horizontal 2 Y-block, 1U and 1V
	3	YUV444
	4	YUV411
	5	YUV422V_2Y (Vertically chroma 2:1 subsampled) - vertical 2 Y-blocks, 1U and 1V
	6	YUV422H_4Y - 2x2 Y-blocks, vertical 2U and 2V
	7	YUV422V_4Y - 2x2 Y-blocks, horizontal 2U and 2V
2:0	<b>Output MCU Structure</b>	
	Project:	CHV, BSW
	Exists If:	//Encoder Only
	Output MCU Structure( <b>OutputMcuStructure</b> ) should be set accordingly for each Input Surface Format YUV( <b>InputSurfaceFormatYUV</b> ):	
	<ul style="list-style-type: none"> <li>• If <b>InputSurfaceFormatYUV</b> is set to NV12, <b>OutputMCUStructure</b> is set to YUV420.</li> <li>• If <b>InputSurfaceFormatYUV</b> is set to UYVY or YUY2, <b>OutputMCUStructure</b> is set to YUV422H_2Y.</li> <li>• If <b>InputSurfaceFormatYUV</b> is set to Y8, <b>OutputMCuStructure</b> is set to YUV400.</li> <li>• If <b>InputSurfaceFormatYUV</b> is set to RGB (or GBR, BGR, YUV), <b>OutputMCuStructure</b> is set to RGB.</li> </ul>	

<b>MFX_JPEG_PIC_STATE</b>																													
		<ul style="list-style-type: none"> <li>If <b>InputSurfaceFormatYUV</b> is set to RGB, the order of encoded blocks in MCU will be same as the order of input image components. If the order of input image components is RGB (or GBR, BGR, YUV), then the order of blocks will be RGB (or GBR, BGR, YUV respectively).</li> </ul> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 75%;">Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>YUV400</td> <td>Grayscale Image</td> </tr> <tr> <td>1</td> <td>YUV420</td> <td>Both horizontally and vertically chroma 2:1 subsampled</td> </tr> <tr> <td>2</td> <td>YUV422H_2Y</td> <td>Horizontally chroma 2:1 subsampled - horizontal 2 Y-blocks, 1 U and 1 V block</td> </tr> <tr> <td>3</td> <td>RGB</td> <td>RGB or YUV444: No subsample</td> </tr> <tr> <td>4</td> <td></td> <td></td> </tr> <tr> <td>5</td> <td></td> <td></td> </tr> <tr> <td>6</td> <td></td> <td></td> </tr> <tr> <td>7</td> <td></td> <td></td> </tr> </tbody> </table>	Value	Name	Description	0	YUV400	Grayscale Image	1	YUV420	Both horizontally and vertically chroma 2:1 subsampled	2	YUV422H_2Y	Horizontally chroma 2:1 subsampled - horizontal 2 Y-blocks, 1 U and 1 V block	3	RGB	RGB or YUV444: No subsample	4			5			6			7		
Value	Name	Description																											
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3	RGB	RGB or YUV444: No subsample																											
4																													
5																													
6																													
7																													
2	31:30	<b>Reserved</b>																											
		Exists If: //Decoder Only																											
		Format: MBZ																											
	31:29	<b>Reserved</b>																											
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		Format: MBZ																											
	29	<b>Reserved</b>																											
		Exists If: //Decoder Only																											
		Format: MBZ																											
	28:16	<b>Frame Height In Blocks Minus 1</b>																											
		Exists If: //Decoder Only																											
Format: U13-1																													
<b>Description</b>																													
(The number of blocks in height) - 1. This value is calculated using the number of lines Y and vertical sampling factor of the first component V <sub>1</sub> in Frame header. See the note following this table. For interleaved components, $((Y + (V_1 * 8 - 1)) / (V_1 * 8)) * V_1 - 1$ , where "/" is integer division. For non-interleaved components, $((Y + 7) / 8) - 1$ .  Workaround: For interleaved components, when <b>Input Format YUV</b> is set to <b>YUV422H_2Y</b> , <b>OutputFormatYUV</b> is set to <b>NV12</b> , If $(((((Y + (V_1 * 8 - 1)) / (V_1 * 8)) * V_1) - 1) \% 2) == 0$ , then <b>Frame Height In Blocks Minus 1</b> = $((Y + (V_1 * 8 - 1)) / (V_1 * 8)) * V_1$ else																													

<b>MFX_JPEG_PIC_STATE</b>			
		then <b>Frame Height In Blocks Minus 1</b> = $((Y + (V1*8 - 1)) / (V1*8)) * V1) - 1$	
28:16	<b>Frame Height In Blks Minus 1</b>		
	Project:	CHV, BSW	
	Exists If:	//Encoder Only	
	Format:	U13-1	
	<p>(The number of blocks in height) - 1. This value is calculated using the number of lines Y and vertical sampling factor of the first component V1 in Frame header. See the note following this table.</p> <p>For interleaved components: <math>((Y + (V1*8 - 1)) / (V1*8)) * V1) - 1</math> For non-interleaved components: <math>(Y + 7) / 8) - 1</math></p>		
15:13	<b>Reserved</b>		
	Exists If:	//Decoder Only	
	Format:	MBZ	
15:13	<b>RoundingQuant</b>		
	Project:	CHV, BSW	
	Exists If:	//Encoder Only	
	Rounding value applied to quantization output		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	000b	<b>[Default]</b>	1/2
	001b		(1/2 - 1/128)
	010b		(1/2 + 1/128)
	011b		(1/2 - 1/64)
	100b		(1/2 + 1/64)
101b		(1/2 - 1/32)	
110b		(1/2 - 1/16)	
111b		(1/2 - 1/8)	
12:0	<b>Frame Width In Blocks Minus 1</b>		
	Exists If:	//Decoder Only	
	Format:	U13-1	
	<p>(The number of blocks in width) - 1. This value is calculated using the number of samples per line X and horizontal sampling factor of the first component H<sub>1</sub> in Frame header. See the note following this table. For interleaved components, <math>((X + (H_1 * 8 - 1)) / (H_1 * 8)) * H_1) - 1</math>. For non-interleaved components, <math>(X + 7) / 8) - 1</math>.</p>		
12:0	<b>Frame Width In Blks Minus 1</b>		
	Project:	CHV, BSW	
	Exists If:	//Encoder Only	
	Format:	U13-1	

### MFX\_JPEG\_PIC\_STATE

(The number of blocks in width) - 1. This value is calculated using the number of samples per line X and horizontal sampling factor of the first component H1 in Frame header. See the note following this table.

For interleaved components:  $((X + (H1 * 8 - 1)) / (H1 * 8)) * H1 - 1$  For non-interleaved components:  $(X + 7) / 8 - 1$

## MFX\_MPEG2\_PIC\_STATE

MFX_MPEG2_PIC_STATE		
Project:	CHV, BSW	
Source:	VideoCS	
Length Bias:	2	
<p>This must be the very first command to issue after the surface state, the pipe select and base address setting commands. For MPEG-2 the encoder is called per slice-group, however the picture state is called per picture. Notice that a slice-group is a group of consecutive slices that no non-trivial slice headers are inserted in between.</p>		
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 3h PARALLEL_VIDEO_PIPE
	Format: OpCode	
	28:27	<b>Pipeline</b>
		Default Value: 2h MFX_MPEG2_PIC_STATE
	Format: OpCode	
	26:24	<b>Media Command Opcode</b>
		Default Value: 3h MPEG2_COMMON
Format: OpCode		
23:21	<b>SubOpcode A</b>	
	Default Value: 0h	
Format: OpCode		
20:16	<b>SubOpcode B</b>	
	Default Value: 0h	
Format: OpCode		
15:12	<b>Reserved</b>	
	Format: MBZ	
11:0	<b>DWord Length</b>	
	Default Value: 0h Excludes DWord (0,1)= 00Bh, used for normal decode and encode mode000h, a special case to provide a dummy image state for stitch mode operation. In this case, fields in DW1 which is part of the dummy image state command are ignored by hardware.	
Format: =n Total Length - 2		
1	31:28	<b>f_code[1][1].</b> Used for backward motion vector prediction. See ISO/IEC 13818-2 7.6.3.1 for details
	27:24	<b>f_code[1][0].</b> Used for backward motion vector prediction. See ISO/IEC 13818-2 7.6.3.1 for details



<b>MFX_MPEG2_PIC_STATE</b>												
23:20	<p><b>f_code[0][1]</b> Used for forward motion vector prediction. See ISO/IEC 13818-2 7.6.3.1 for details</p>											
19:16	<p><b>f_code[0][0]</b> Used for forward motion vector prediction. See ISO/IEC 13818-2 7.6.3.1 for details</p>											
15:14	<p><b>Intra DC Precision</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U2</td> </tr> </table> <p>See ISO/IEC 13818-2 6.3.10 for details.</p>	Project:	All	Format:	U2							
Project:	All											
Format:	U2											
13:12	<p><b>Picture Structure</b> This field specifies whether the picture is encoded in the form of a frame picture or one field (top or bottom) picture. See ISO/IEC 13818-2 6.3.10 for details.Format = MPEG_PICTURE_STRUCTURE00 = Reserved01 = MPEG_TOP_FIELD10 = MPEG_BOTTOM_FIELD11 = MPEG_FRAME</p>											
11	<p><b>TFF (Top Field First)</b> When two fields are stored in a picture, this bit indicates if the top field is the first field.For a frame P picture, the value 1 indicates that the top field of the reconstructed frame is the first field output by the decoding process, the same as defined in ISO/IEC 13818-2 6.3.10. Particularly, it is used by the hardware to calculate derivative motion vectors from the dual-prime motion vectors.For a field P picture, hardware uses this bit together with the Picture Structure to determine if the current picture is the Second Field. In this case, the definition of this bit differs from ISO/IEC 13818-2 6.3.10 - software must derive the value for this bit according to the following relation:Picture Structure = top fieldPicture Structure = bottom fieldSecond Field = 0TFF = 1TFF = 0Second Field = 1TFF = 0TFF = 1</p>											
10	<p><b>Frame Prediction Frame DCT</b> This field provides constraints on the DCT type and prediction type. It affects the syntax of the bitstream.</p>											
9	<p><b>Concealment Motion Vector Flag</b> This field indicates if the concealment motion vectors are coded in intra macroblocks. It affects the syntax of the bitstream.</p>											
8	<p><b>Quantizer Scale Type</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 40%;">Format:</td> <td>MPEG_Q_SCALE_TYPE</td> </tr> </table> <p>This field specifies the quantizer scaling type.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 20%;">Value</th> <th style="width: 20%;">Name</th> <th style="width: 60%;">Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td></td> <td>MPEG_QSCALE_LINEAR</td> </tr> <tr> <td>1h</td> <td></td> <td>D MPEG_QSCALE_NONLINEAR esc</td> </tr> </tbody> </table>	Format:	MPEG_Q_SCALE_TYPE	Value	Name	Description	0h		MPEG_QSCALE_LINEAR	1h		D MPEG_QSCALE_NONLINEAR esc
Format:	MPEG_Q_SCALE_TYPE											
Value	Name	Description										
0h		MPEG_QSCALE_LINEAR										
1h		D MPEG_QSCALE_NONLINEAR esc										
7	<p><b>Intra VLC Format</b> This field is used by VLD</p>											
6	<p><b>Scan Order</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 40%;">Format:</td> <td>MPEG_INVERSESCAN_TYPE</td> </tr> </table>	Format:	MPEG_INVERSESCAN_TYPE									
Format:	MPEG_INVERSESCAN_TYPE											

<b>MFX_MPEG2_PIC_STATE</b>																					
		<p>This field specifies the Inverse Scan method for the DCT-domain coefficients in the blocks of the current picture.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td></td> <td>MPEG_ZIGZAG_SCAN</td> </tr> <tr> <td>1h</td> <td></td> <td>MPEG_ALTERNATE_VERTICAL_SCAN</td> </tr> </tbody> </table>	Value	Name	Description	0h		MPEG_ZIGZAG_SCAN	1h		MPEG_ALTERNATE_VERTICAL_SCAN										
Value	Name	Description																			
0h		MPEG_ZIGZAG_SCAN																			
1h		MPEG_ALTERNATE_VERTICAL_SCAN																			
	5:0	<b>Reserved</b>																			
2	31	<p><b>I Slice Concealment Mode</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Decoder</td> </tr> </table> <p>This field controls how MPEG decoder handles MB concealment in I Slice</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Intra Concealment</td> <td>Using Coefficient values to handle MB concealment</td> </tr> <tr> <td>1h</td> <td>Inter Concealment</td> <td>Using Motion Vectors to handle MB concealment</td> </tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>If this field is set to "1", driver must provide a valid forward reference picture (both top and bottom Field must be valid)</p>	Project:	CHV, BSW	Exists If:	//Decoder	Value	Name	Description	0h	Intra Concealment	Using Coefficient values to handle MB concealment	1h	Inter Concealment	Using Motion Vectors to handle MB concealment						
		Project:	CHV, BSW																		
Exists If:	//Decoder																				
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	30	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ															
Project:	CHV, BSW																				
Format:	MBZ																				
	29:28	<p><b>P/B Slice Concealment Mode</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Decoder</td> </tr> </table> <p>This field controls how MPEG decoder handles MB concealment in P/B Slice.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>INTER</td> <td>If left MB is NOT Intra MB type (including skipMB), use left MB inter prediction mode [frame/field or forward/backward/bi] and MV final values as concealment. Otherwise (left MB is Intra MB), use forward reference (same polarity for field pic) with MV final values set to 0.</td> </tr> <tr> <td>01b</td> <td>LEFT</td> <td>If left MB is NOT Intra MB type (including skipMB), use left MB inter prediction mode [frame/field or forward/backward/bi] and MV final values as concealment. Otherwise (left MB is Intra MB), use left MB dct_dc_pred[cc] values for concealment (Macroblock is concealed as INTRA MB and dct_dc_pred[cc] are DC predictor for Luma, Cr, Cb data)</td> </tr> <tr> <td>10b</td> <td>ZERO</td> <td>Always use forward reference (same polarity for field pic) with MV final values set to 0 (Macroblock is concealed as INTER coded)</td> </tr> <tr> <td>11b</td> <td>INTRA</td> <td>Use left MB dct_dc_pred[cc] values for concealment (Macroblock is concealed as INTRA MB and dct_dc_pred[cc] are DC predictor for Luma, Cr, Cb data)</td> </tr> </tbody> </table>	Project:	CHV, BSW	Exists If:	//Decoder	Value	Name	Description	00b	INTER	If left MB is NOT Intra MB type (including skipMB), use left MB inter prediction mode [frame/field or forward/backward/bi] and MV final values as concealment. Otherwise (left MB is Intra MB), use forward reference (same polarity for field pic) with MV final values set to 0.	01b	LEFT	If left MB is NOT Intra MB type (including skipMB), use left MB inter prediction mode [frame/field or forward/backward/bi] and MV final values as concealment. Otherwise (left MB is Intra MB), use left MB dct_dc_pred[cc] values for concealment (Macroblock is concealed as INTRA MB and dct_dc_pred[cc] are DC predictor for Luma, Cr, Cb data)	10b	ZERO	Always use forward reference (same polarity for field pic) with MV final values set to 0 (Macroblock is concealed as INTER coded)	11b	INTRA	Use left MB dct_dc_pred[cc] values for concealment (Macroblock is concealed as INTRA MB and dct_dc_pred[cc] are DC predictor for Luma, Cr, Cb data)
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<b>MFX_MPEG2_PIC_STATE</b>				
27	<b>Reserved</b>			
	Project:	CHV, BSW		
	Format:	MBZ		
	26:25	<b>P/B Slice Predicted BiDir Motion Type Override - Bi-direction MV Type Override</b>		
		Project:	CHV, BSW	
		Exists If:	//Decoder	
		This field is only applicable if the Concealment Motion Type is predicted to be Bi-directional. (It is only possible if "P/B Slice Concealment Mode" is set to "00" or "01" and left MB is a bi-directional MB).		
		<b>Value</b>	<b>Name</b>	<b>Description</b>
		0h	BID	Keep Bi-direction Prediction
		1h	RESERVED	
2h		FWD	Only use Forward Prediction (Backward MV is forced to invalid)	
3h		BWD	Only use Backward Prediction (Forward MV is forced to invalid)	
24		<b>P/B Slice Predicted Motion Vector Override Final MV value Override</b>		
	Project:	CHV, BSW		
	Exists If:	//Decoder		
	This field is only applicable if the Concealment Motion Vectors are non-zero. It is only possible if "P/B Slice Concealment Mode" is set to "00" or "01" and left MB has non-zero motion vectors).			
	<b>Value</b>	<b>Name</b>	<b>Description</b>	
	0h	Predicted	Motion Vectors use predicted values	
	1h	ZERO	Motion Vectors force to 0	
	23:15	<b>Reserved</b>		
		Format:	MBZ	
	14	<b>LoadSlicePointerFlag - LoadBitStreamPointerPerSlice</b>		
Exists If:		//Encoder		
To support multiple slice picture and additional header/data insertion before and after an encoded slice. When this field is set to 0, bitstream pointer is only loaded once for the first slice of a frame. For subsequent slices in the frame, bitstream data are stitched together to form a single output data stream. When this field is set to 1, bitstream pointer is loaded for each slice of a frame. Basically bitstream data for different slices of a frame will be written to different memory locations.				
<b>Value</b>		<b>Name</b>	<b>Description</b>	
0h			Load BitStream Pointer only once for the first slice of a frame	
1h			Load/reload BitStream Pointer only once for the each slice, reload the start location of the bitstream buffer from the Indirect PAK-BSE Object Data Start Address field	
13		<b>Reserved</b>		

<b>MFX_MPEG2_PIC_STATE</b>																
	12	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ												
	Format:	MBZ														
	11	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ												
	Format:	MBZ														
	10:9	<b>Picture Coding Type</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 20%;">Format:</td> <td>MPEG_PICTURE_CODING_TYPE</td> </tr> </table> <p>This field identifies whether the picture is an intra-coded picture (I), predictive-coded picture (P) or bi-directionally predictive-coded picture (B). See ISO/IEC 13818-2 6.3.9 for details.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 20%;">Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Reserved</td> </tr> <tr> <td>01b</td> <td>MPEG_I_PICTURE</td> </tr> <tr> <td>10b</td> <td>10 = MPEG_P_PICTURE</td> </tr> <tr> <td>11b</td> <td>MPEG_B_PICTURE</td> </tr> </tbody> </table>	Format:	MPEG_PICTURE_CODING_TYPE	Value	Name	00b	Reserved	01b	MPEG_I_PICTURE	10b	10 = MPEG_P_PICTURE	11b	MPEG_B_PICTURE		
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8:2	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ													
Format:	MBZ															
1	<b>MismatchControlDisabled</b> These 2 bits flag disables mismatch control of the inverse transformation for some specific cases during reference reconstruction. <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td></td> <td>Mismatch control applies to all MBs</td> </tr> <tr> <td>01b</td> <td></td> <td>Disable mismatch control to all intra MBs whose all AC-coefficients are zero.</td> </tr> <tr> <td>10b</td> <td></td> <td>Disable mismatch control to all MBs whose all AC-coefficients are zero.</td> </tr> <tr> <td>11b</td> <td></td> <td>Disable mismatch control to all MBs.</td> </tr> </tbody> </table>	Value	Name	Description	00b		Mismatch control applies to all MBs	01b		Disable mismatch control to all intra MBs whose all AC-coefficients are zero.	10b		Disable mismatch control to all MBs whose all AC-coefficients are zero.	11b		Disable mismatch control to all MBs.
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11b		Disable mismatch control to all MBs.														
0	<b>Disable Mismatch</b> To disable MPEG2 IDCT fixed point arithmetic correction															
3	31 <b>Slice Concealment Disable Bit</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Decode</td> </tr> </table> <p>If VINunit detects the next slice starting position is either out-of-bound or smaller than or equal to the current slice starting position, VIN will set the current slice to be 1 MB and force VMDunit to do slice concealment on the next slice. This bit will disable this feature and the MB data from the next slice will be decoded from bitstream.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Enable <b>[Default]</b></td> <td>VIN will force next slice to be concealment if detects slice boundary error</td> </tr> <tr> <td>1h</td> <td>Disable</td> <td>VIN will not force next slice to be in concealment</td> </tr> </tbody> </table>	Project:	CHV, BSW	Exists If:	//Decode	Value	Name	Description	0h	Enable <b>[Default]</b>	VIN will force next slice to be concealment if detects slice boundary error	1h	Disable	VIN will not force next slice to be in concealment		
Project:	CHV, BSW															
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<b>MFX_MPEG2_PIC_STATE</b>																				
		<b>Programming Notes</b>																		
		Driver has an option to detect the scenario given in description (above) and remove the second (out-of-order) slice. In this case, hardware will decode the first slice in completion and do concealment till the third slice. It should yield a picture with better quality this way.																		
	30:29	<b>Reserved</b>																		
		Format: MBZ																		
	28:24	<b>Reserved</b>																		
	23:16	<b>FrameHeightInMBsMinus1[7:0] (Picture Height in Macroblocks)</b>																		
		Format: U8																		
	15:8	<b>Reserved</b>																		
		Format: MBZ for future supporting width > 4K																		
	7:0	<b>FrameWidthInMBsMinus1[7:0] (Picture Width in Macroblocks)</b>																		
		Project: All																		
		Format: U8																		
4	31:16	<b>MinFrameWSize</b>																		
		Project: All																		
		Format: U16																		
		- Minimum Frame Size [15:0] (16-bit) (Encoder Only) Minimum Frame Size is specified to compensate for intel Rate Control Currently zero fill (no need to perform emulation byte insertion) is done only to the end of the CABAC_ZERO_WORD insertion (if any) at the last slice of a picture. Intel encoder parameter, not part of DXVA. The caller should always make sure that the value, represented by Minimum Frame Size, is always less than maximum frame size FrameBitRateMax (DWORD 10 bits 29:16). This field is reserved in Decode mode.																		
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[0,0003FFFFh]</td> <td></td> <td>The programmable range when MinFrameWSizeUnits is 00.</td> </tr> <tr> <td>[0,000FFFFFFh]</td> <td></td> <td>The Programmable range when MinFrameWSizeUnits is 01.</td> </tr> <tr> <td>[0,03FFFFFFh]</td> <td></td> <td>The Programmable range when MinFrameWSizeUnits is 10.</td> </tr> <tr> <td>[0, FFFFFFFFh]</td> <td></td> <td>The Programmable range when MinFrameWSizeUnits is 11.</td> </tr> <tr> <td>0h</td> <td><b>[Default]</b></td> <td></td> </tr> </tbody> </table>	Value	Name	Description	[0,0003FFFFh]		The programmable range when MinFrameWSizeUnits is 00.	[0,000FFFFFFh]		The Programmable range when MinFrameWSizeUnits is 01.	[0,03FFFFFFh]		The Programmable range when MinFrameWSizeUnits is 10.	[0, FFFFFFFFh]		The Programmable range when MinFrameWSizeUnits is 11.	0h	<b>[Default]</b>	
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	15	<b>Reserved</b>																		
		Project: All																		
		Format: MBZ																		
	14:12	<b>RoundInterAC,</b> rounding precision for non-Intra AC000: +1/16001: +2/16010: +3/16011: +4/16100: +5/16101: +6/16110: +7/16111: +8/16																		
	11	<b>Reserved</b>																		

<b>MFX_MPEG2_PIC_STATE</b>																			
	10:8	<b>RoundIntraAC</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U3</td> </tr> </table> rounding precision for Intra AC000: +1/16001: +2/16010: +3/16011: +4/16100: +5/16101: +6/16110: +7/16111: +8/16	Project:	All	Format:	U3													
	Project:	All																	
	Format:	U3																	
	7	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ															
	Format:	MBZ																	
	6:4	<b>RoundInterDC</b> rounding Precision for non-Intra-DC000: +1/16001: +2/16010: +3/16011: +4/16100: +5/16101: +6/16110: +7/16111: +8/16																	
3	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ																
Format:	MBZ																		
2:1	<b>RoundIntraDC</b> rounding Precision for Intra-DC00: +1/801: +2/810: +3/811: +4/8																		
0	<b>Reserved</b>																		
5	31:17	<b>Reserved</b> (for future Mask bits)																	
	16	<b>FrameSizeControlMask</b> Frame size conformance maskThis field is used when MacroblockStatEnable is set to 1. <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 10%;">Name</th> <th style="width: 80%;">Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td></td> <td>Do not change Slice Quantization Parameter values in MFC_MPEG2_SLICEGROUP_STATE with suggested slice QP value for frame level Rate control</td> </tr> <tr> <td>1h</td> <td></td> <td>Replace Slice Quantization Parameter values in MFC_MPEG2_SLICEGROUP_STATE with suggested slice QP value for frame level Rate control values in MFC_IMAGE_STATUS control register.</td> </tr> </tbody> </table>	Value	Name	Description	0h		Do not change Slice Quantization Parameter values in MFC_MPEG2_SLICEGROUP_STATE with suggested slice QP value for frame level Rate control	1h		Replace Slice Quantization Parameter values in MFC_MPEG2_SLICEGROUP_STATE with suggested slice QP value for frame level Rate control values in MFC_IMAGE_STATUS control register.								
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	1h		Replace Slice Quantization Parameter values in MFC_MPEG2_SLICEGROUP_STATE with suggested slice QP value for frame level Rate control values in MFC_IMAGE_STATUS control register.																
15:13	<b>Reserved</b>																		
12	<b>InterMBForceCBPZeroControlMask</b> <table border="1" style="width: 100%; margin-top: 5px;"> <tr> <td>Format:</td> <td>U1</td> </tr> </table> Inter MB Force CBP ZERO mask. <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 10%;">Name</th> <th style="width: 55%;">Description</th> <th style="width: 20%;">Project</th> </tr> </thead> <tbody> <tr> <td>[0, FFFFFFFFh]</td> <td></td> <td></td> <td></td> </tr> <tr> <td>0h</td> <td></td> <td>No effect</td> <td>All</td> </tr> <tr> <td>1h</td> <td></td> <td>Zero out all A/C coefficients for the inter MB violating Inter Conformance</td> <td>All</td> </tr> </tbody> </table>	Format:	U1	Value	Name	Description	Project	[0, FFFFFFFFh]				0h		No effect	All	1h		Zero out all A/C coefficients for the inter MB violating Inter Conformance	All
Format:	U1																		
Value	Name	Description	Project																
[0, FFFFFFFFh]																			
0h		No effect	All																
1h		Zero out all A/C coefficients for the inter MB violating Inter Conformance	All																
11:10	<b>MinFrameWSizeUnits</b> This field is the Minimum Frame Size Units																		

<b>MFX_MPEG2_PIC_STATE</b>				
	<b>Value</b>	<b>Name</b>	<b>Description</b>	
	00b	compatibility mode	Minimum Frame Size is in old mode (words, 2bytes)	
	01b	16 byte	Minimum Frame Size is in 16bytes	
	10b	4Kb	Minimum Frame Size is in 4Kbytes	
	11b	16Kb	Minimum Frame Size is in 16Kbytes	
9	<b>MBRateControlMask</b> This field is ignored when MacroblockStatEnable is disabled or MB level Rate control flag for the current MB is disable in Macroblock Status Buffer.			
	<b>Value</b>	<b>Name</b>	<b>Description</b>	
	0h		Do not change QP values of inter macroblock with suggested QP values in Macroblock Status Buffer	
	1h		Apply RC QP delta for all macroblock	
8	<b>Reserved</b>			
7	<b>Reserved</b>			
6:4	<b>Reserved</b>			
3	<b>FrameBitRateMinReportMask</b> This is a mask bit controlling if the condition of frame level bit count is less than FrameBitRateMin.			
	<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>
	0h	Disable	Do not update bit0 of MFC_IMAGE_STATUS control register.	All
	1h	Enable	set bit0 and bit 1 of MFC_IMAGE_STATUS control register if the total frame level bit counter is less than or equal to Frame Bit rate Minimum limit.	All
2	<b>FrameBitRateMaxReportMask</b> This is a mask bit controlling if the condition of frame level bit count exceeds FrameBitRateMax.			
	<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>
	0h	Disable	Do not update bit0 of MFC_IMAGE_STATUS control register.	All
	1h	Enable	set bit0 and bit 1 of MFC_IMAGE_STATUS control register if the total frame level bit counter is greater than or equal to Frame Bit rate Maximum limit.	All
1	<b>InterMBMaxSizeReportMask</b> This is a mask bit controlling if the condition of any inter MB in the frame exceeds InterMBMaxSize.			
	<b>Value</b>	<b>Name</b>	<b>Description</b>	
	0h		Do not update bit0 of MFC_IMAGE_STATUS control register.	
	1h		set bit0 of MFC_IMAGE_STATUS control register if the total bit counter for the current MB is greater than the Inter MB Conformance Max size limit.	

<b>MFX_MPEG2_PIC_STATE</b>															
	0	<p><b>IntraMBMaxSizeReportMask</b> This is a mask bit controlling if the condition of any intra MB in the frame exceeds IntraMBMaxSize.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td></td> <td>Do not update bit0 of MFC_IMAGE_STATUS control register.</td> </tr> <tr> <td>1h</td> <td></td> <td>set bit0 of MFC_IMAGE_STATUS control register if the total bit counter for the current MB is greater than the Intra MB Conformance Max size limit.</td> </tr> </tbody> </table>	Value	Name	Description	0h		Do not update bit0 of MFC_IMAGE_STATUS control register.	1h		set bit0 of MFC_IMAGE_STATUS control register if the total bit counter for the current MB is greater than the Intra MB Conformance Max size limit.				
Value	Name	Description													
0h		Do not update bit0 of MFC_IMAGE_STATUS control register.													
1h		set bit0 of MFC_IMAGE_STATUS control register if the total bit counter for the current MB is greater than the Intra MB Conformance Max size limit.													
6  [ExistsIf]Encode Only	31:28	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ											
	Format:	MBZ													
	27:16	<p><b>InterMBMaxSize</b></p> <table border="1"> <tr> <td>Default Value:</td> <td>FFFh</td> </tr> </table> <p>This field, Inter MB Conformance Max size limit, indicates the allowed max bit count size for Inter MB</p>	Default Value:	FFFh											
	Default Value:	FFFh													
15:12	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ												
Format:	MBZ														
11:0	<p><b>IntraMBMaxSize</b></p> <table border="1"> <tr> <td>Default Value:</td> <td>FFFh</td> </tr> </table> <p>This field, Intra MB Conformance Max size limit, indicates the allowed max bit count size for Intra MB</p>	Default Value:	FFFh												
Default Value:	FFFh														
7	31:1	<p><b>Reserved</b></p>													
	0	<p><b>VSL top MB Trans8x8flag</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Encode Only</td> </tr> </table> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Disable</td> <td>VSL will only fetch the current MB data.</td> </tr> <tr> <td>1</td> <td>Enable</td> <td>When this bit is set VSL will make extra fetch to memory to fetch the MB data for top MB.</td> </tr> </tbody> </table>	Project:	CHV, BSW	Exists If:	//Encode Only	Value	Name	Description	0	Disable	VSL will only fetch the current MB data.	1	Enable	When this bit is set VSL will make extra fetch to memory to fetch the MB data for top MB.
	Project:	CHV, BSW													
Exists If:	//Encode Only														
Value	Name	Description													
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1	Enable	When this bit is set VSL will make extra fetch to memory to fetch the MB data for top MB.													
8  [ExistsIf]Encode Only	31:24	<p><b>SliceDeltaQPMax[3]</b></p> <table border="1"> <tr> <td>Format:</td> <td>S7</td> </tr> </table> <p>This field is the Slice level delta QP for total bit-count above FrameBitRateMax - first 1/8 region This field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame exceeds FrameBitRateMax but is within 1/8 of FrameBitRateMaxDelta above FrameBitRateMax, i.e., in the range of (FrameBitRateMax, (FrameBitRateMax+ FrameBitRateMaxDelta»3).</p> <p>Range: [-30,30]</p>	Format:	S7											
	Format:	S7													



		<b>MFX_MPEG2_PIC_STATE</b>	
		Value	Name
		0h	Disable
		1h	Enable
	23:16	<b>SliceDeltaQPMax[2]</b>	
		Format:	S7
		Range: [-30,30] This field is the Slice level delta QP for bit-count above FrameBitRateMax - above 1/8 and below 1/4 This field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame is between 1/8 and 1/4 of FrameBitRateMaxDelta above FrameBitRateMax, i.e., in the range of ((FrameBitRateMax+ FrameBitRateMaxDelta>3), (FrameBitRateMax+ FrameBitRateMaxDelta>2)).	
	15:8	<b>SliceDeltaQPMax[1]</b>	
		Format:	S7
		Range: [-30,30] This field is the Slice level delta QP for bit-count above FrameBitRateMax - above 1/4 and below 1/2 This field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame is between 1/4 and 1/2 of FrameBitRateMaxDelta above FrameBitRateMax, i.e., in the range of ((FrameBitRateMax+ FrameBitRateMaxDelta>2), (FrameBitRateMax+ FrameBitRateMaxDelta>1)).	
	7:0	<b>SliceDeltaQPMax[0]</b>	
		Format:	S7
		Range: [-30,30] This field is the Slice level delta QP for bit-count above FrameBitRateMax - above 1/2 This field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame is above FrameBitRateMax by more than half the distance of FrameBitRateMaxDelta , i.e., in the range of ((FrameBitRateMax+ FrameBitRateMaxDelta>1), infinite).	
9	31:24	<b>SliceDeltaQPMin[3]</b>	
[ExistsIf]Encode Only		Format:	S7
		Range: [-30,30] This field is the Slice level delta QP for total bit-count below FrameBitRateMin - first 1/8 region This field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame is less than FrameBitRateMin and greater than or equal to 1/8 the distance of FrameBitRateMinDelta from FrameBitRateMin, i.e., in the range of [(FrameBitRateMin- FrameBitRateMinDelta>3), FrameBitRateMin).	

<b>MFX_MPEG2_PIC_STATE</b>													
	<p><b>23:16 SliceDeltaQPMin[2]</b></p> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td style="text-align: center;">S7</td> </tr> </table> <p>Range: [-30,30]</p> <p>This field is the Slice level delta QP for bit-count below FrameBitRateMin - below 1/ 8 and above 1/ 4This field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame is between one-eighth and quarter the distance of FrameBitRateMinDelta from FrameBitRateMin, i.e., in the range of [(FrameBitRateMin- FrameBitRateMinDelta»2), (FrameBitRateMin- FrameBitRateMinDelta»3)).</p>	Format:	S7										
	Format:	S7											
	<p><b>15:8 SliceDeltaQPMin[1]</b></p> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td style="text-align: center;">S7</td> </tr> </table> <p>Range: [-30,30]</p> <p>This field is the Slice level delta QP for bit-count below FrameBitRateMin- below 1/4 and above 1/ 2This field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame is between quarter and half the distance of FrameBitRateMinDelta from FrameBitRateMin, i.e., in the range of [(FrameBitRateMin- FrameBitRateMinDelta»1), (FrameBitRateMin- FrameBitRateMinDelta»2)).</p>	Format:	S7										
Format:	S7												
<p><b>7:0 SliceDeltaQPMin[0]</b></p> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td style="text-align: center;">S7</td> </tr> </table> <p>Range: [-30,30]</p> <p>This field is the Slice Level Delta QP for bit-count below FrameBitRateMin - below 1/ 2This field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame is below FrameBitRateMin by more than half the distance of FrameBitRateMinDelta , i.e., in the range of [0, (FrameBitRateMin- FrameBitRateMinDelta»1).</p>	Format:	S7											
Format:	S7												
<p>10</p> <p>[ExistsIf]Encode Only</p>	<p><b>31 FrameBitrateMaxUnit</b></p> <p>This field is the Frame Bitrate Maximum Limit Units.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Byte</td> <td>FrameBitRateMax is in units of 32 Bytes when FrameBitrateMaxUnitMode is 1 and in units of 128 Bytes if FrameBitrateMaxUnitMode is 0</td> <td>All</td> </tr> <tr> <td>1h</td> <td>Kilobyte</td> <td>FrameBitRateMax is in units of 4KBytes Bytes when FrameBitrateMaxUnitMode is 1 and in units of 16KBytes if FrameBitrateMaxUnitMode is 0</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	0h	Byte	FrameBitRateMax is in units of 32 Bytes when FrameBitrateMaxUnitMode is 1 and in units of 128 Bytes if FrameBitrateMaxUnitMode is 0	All	1h	Kilobyte	FrameBitRateMax is in units of 4KBytes Bytes when FrameBitrateMaxUnitMode is 1 and in units of 16KBytes if FrameBitrateMaxUnitMode is 0	All
Value	Name	Description	Project										
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<b>MFX_MPEG2_PIC_STATE</b>															
	30	<p><b>FrameBitrateMaxUnitMode</b> BitFiel This field is the Frame Bitrate Maximum Limit Units.dDesc</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Compatibility mode</td> <td>FrameBitRateMaxUnit is in old mode (128b/16Kb)</td> <td>All</td> </tr> <tr> <td>1h</td> <td>New mode</td> <td>FrameBitRateMaxUnit is in new mode (32byte/4Kb)</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	0h	Compatibility mode	FrameBitRateMaxUnit is in old mode (128b/16Kb)	All	1h	New mode	FrameBitRateMaxUnit is in new mode (32byte/4Kb)	All	
	Value	Name	Description	Project											
	0h	Compatibility mode	FrameBitRateMaxUnit is in old mode (128b/16Kb)	All											
	1h	New mode	FrameBitRateMaxUnit is in new mode (32byte/4Kb)	All											
	29:16	<p><b>FrameBitRateMax</b> This field is the Frame Bitrate Maximum Limit. This field along with FrameBitrateMaxUnit determines maximum allowed bits in a frame before multi-pass gets triggered (when enabled). In other words, multi-pass is triggered when the actual frame byte count exceeds this value. When FrameBitrateMaxUnitMode is 0(compatibility mode) bits 16:27 should be used, bits 28 and 29 should be 0.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0-512KB</td> <td></td> <td>The programmable range 0-512KB when FrameBitrateMaxUnit is 0.</td> </tr> <tr> <td>0-8190KB</td> <td></td> <td>The programmable range 0-8190KB when FrameBitrateMaxUnit is 1.</td> </tr> </tbody> </table>	Value	Name	Description	0-512KB		The programmable range 0-512KB when FrameBitrateMaxUnit is 0.	0-8190KB		The programmable range 0-8190KB when FrameBitrateMaxUnit is 1.				
	Value	Name	Description												
	0-512KB		The programmable range 0-512KB when FrameBitrateMaxUnit is 0.												
	0-8190KB		The programmable range 0-8190KB when FrameBitrateMaxUnit is 1.												
	15	<p><b>FrameBitrateMinUnit</b> This field is the Frame Bitrate Minimum Limit Units.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Byte</td> <td>FrameBitRateMax is in units of 32 Bytes when FrameBitrateMinUnitMode is 1 and in units of 128 Bytes if FrameBitrateMinUnitMode is 0</td> <td>All</td> </tr> <tr> <td>1h</td> <td>KiloByte</td> <td>FrameBitRateMax is in units of 4KBytes Bytes when FrameBitrateMaxUnitMode is 1 and in units of 16KBytes if FrameBitrateMaxUnitMode is 0</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	0h	Byte	FrameBitRateMax is in units of 32 Bytes when FrameBitrateMinUnitMode is 1 and in units of 128 Bytes if FrameBitrateMinUnitMode is 0	All	1h	KiloByte	FrameBitRateMax is in units of 4KBytes Bytes when FrameBitrateMaxUnitMode is 1 and in units of 16KBytes if FrameBitrateMaxUnitMode is 0	All	
	Value	Name	Description	Project											
0h	Byte	FrameBitRateMax is in units of 32 Bytes when FrameBitrateMinUnitMode is 1 and in units of 128 Bytes if FrameBitrateMinUnitMode is 0	All												
1h	KiloByte	FrameBitRateMax is in units of 4KBytes Bytes when FrameBitrateMaxUnitMode is 1 and in units of 16KBytes if FrameBitrateMaxUnitMode is 0	All												
14	<p><b>FrameBitrateMinUnitMode</b> This field is the Frame Bitrate Minimum Limit Units.ValueNameDescriptionProject</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>compatibility mode</td> <td>FrameBitRateMaxUnit is in old mode (128b/16Kb)</td> <td>All</td> </tr> <tr> <td>1h</td> <td>New Mode</td> <td>FrameBitRateMaxUnit is in new mode (32byte/4Kb)</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	0h	compatibility mode	FrameBitRateMaxUnit is in old mode (128b/16Kb)	All	1h	New Mode	FrameBitRateMaxUnit is in new mode (32byte/4Kb)	All		
Value	Name	Description	Project												
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1h	New Mode	FrameBitRateMaxUnit is in new mode (32byte/4Kb)	All												
13:0	<p><b>FrameBitRateMin</b> This field is the Frame Bitrate Minimum Limit ()This field along with FrameBitrateMinUnit determines minimum allowed bits in a Frame before Multi-Pass gets triggered (when enabled). In other words, multi-pass is triggered when the actual frame byte count is less than this value. When FrameBitrateMinUnitMode is 0 (compatibility mode) bits 0:11 should be used, bits 12 and 13 should be 0. Range: The programmable range 0-512KB When FrameBitrateMinUnit is in 0. Programmable range is 0-8190 KB when FrameBitrateMinUnit is in 1</p>														
11	31	<b>Reserved</b>													

<b>MFX_MPEG2_PIC_STATE</b>												
[ExistsIf]Encode Only	30:16	<b>FrameBitRateMaxDelta</b> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>0h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Access:</td> <td>None</td> </tr> <tr> <td>Format:</td> <td>U15</td> </tr> </table> <p>This field is used to select the slice delta QP when FrameBitRateMax Is exceeded. It shares the same FrameBitrateMaxUnit. The programmable range is either 0- 512KB or 4MBB in FrameBitrateMaxUnit of 128 Bytes or 16KB respectively.</p> <p>This field is used to select the slice delta QP when FrameBitRateMax Is exceeded. It shares the same FrameBitrateMaxUnit. When FrameBitrateMaxUnitMode is 0(compatibility mode) bits 16:27 should be used, bits 28, 29 and 30 should be 0.</p>	Default Value:	0h	Project:	All	Access:	None	Format:	U15		
		Default Value:	0h									
		Project:	All									
		Access:	None									
Format:	U15											
15	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ							
	Project:	All										
Format:	MBZ											
14:0	<b>FrameBitRateMinDelta</b> This field is used to select the slice delta QP when FrameBitRateMin Is exceeded. It shares the same FrameBitrateMinUnit. When FrameBitrateMinUnitMode is 0(compatibility mode) bits 0:11 should be used, bits 12, 13 and 14 should be 0.Note: HW requires the following condition $FrameBitRateMinDelta \leq 2 * FrameBitRateMinMust$ be true, otherwise it may cause unpredicted behavior.											
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 70%;">Description</th> </tr> </thead> <tbody> <tr> <td>0-1024KB</td> <td></td> <td>The programmable range 0-1024KB When FrameBitrateMinUnit is in 32Bytes.</td> </tr> <tr> <td>0-16380KB</td> <td></td> <td>Programmable range is 0-16380KB when FrameBitrateMinUnit is in 4Kbytes.</td> </tr> </tbody> </table>	Value	Name	Description	0-1024KB		The programmable range 0-1024KB When FrameBitrateMinUnit is in 32Bytes.	0-16380KB		Programmable range is 0-16380KB when FrameBitrateMinUnit is in 4Kbytes.		
	Value	Name	Description									
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0-16380KB		Programmable range is 0-16380KB when FrameBitrateMinUnit is in 4Kbytes.										
12	31:21	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ								
		Format:	MBZ									
	<b>VMD Error Logic</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 45%;">Name</th> <th style="width: 40%;">Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Disable <b>[Default]</b></td> <td></td> </tr> <tr> <td>1</td> <td>Enable</td> <td>Error Handling</td> </tr> </tbody> </table>	Project:	CHV, BSW	Value	Name	Description	0	Disable <b>[Default]</b>		1	Enable	Error Handling
	Project:	CHV, BSW										
Value	Name	Description										
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1	Enable	Error Handling										
20	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ									
	Format:	MBZ										
<b>VAD Error Logic</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table>	Project:	CHV, BSW										
Project:	CHV, BSW											

<b>MFX_MPEG2_PIC_STATE</b>			
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0	Enable <b>[Default]</b>	Error reporting ON in case of premature Slice done
	1	Disable	CABAC Engine will auto decode the bitstream in case of premature slice done.
	17	<b>Reserved</b>	
		Project:	CHV, BSW
	16	<b>Reserved</b>	
		Project:	CHV, BSW
	15:0	<b>Reserved</b>	
		Format:	MBZ

## MFX\_PAK\_INSERT\_OBJECT

<b>MFX_PAK_INSERT_OBJECT</b>	
Project:	CHV, BSW
Source:	VideoCS
Length Bias:	2
<b>Description</b>	
<p>The MFX_PAK_INSERT_OBJECT command is the first primitive command for the AVC and MPEG2 Encoding Pipeline. The MFX_PAK_INSERT_OBJECT command is the first primitive command for the AVC, MPEG2, JPEG, and VP8 Encoding Pipeline.</p> <p>This command is issued to setup the control and parameters of inserting a chunk of compressed/encoded bits into the current bitstream output buffer starting at the specified bit location to perform the actual insertion by transferring the command inline data to the output buffer max, 32 bits at a time.</p> <p>It is a variable length command as the data to be inserted are presented as inline data of this command. It is a multiple of 32-bit (1 DW), as the data bus to the bitstream buffer is 32-bit wide.</p> <p>Multiple insertion commands can be issued back to back in a series. It is host software's responsibility to make sure their corresponding data will properly stitch together to form a valid H.264 bitstream.</p> <p>Internally, MFX hardware will keep track of the very last two bytes' (the very last byte can be a partial byte) values of the previous insertion. It is required that the next Insertion Object Command or the next PAK Object Command to perform the start code emulation sequence check and prevention 0x03 byte insertion with this end condition of the previous insertion.</p> <p>Hardware will keep track of an output bitstream buffer current byte position and the associated next bit insertion position index. Data to be inserted can be a valid H.264 NAL units or a partial NAL unit. Certain NAL unit has a minimum byte size requirement. As such the hardware will optionally (enabled by STATE Command) determines the number of CABAC_ZERO_WORD to be inserted to the end of the current NAL, based on the minimum byte size of a NAL and the actual bin count of the encoded Slice. Since prior to the CABAC_ZERO_WORD insertion, the RBSP or EBSP is already byte-aligned, so each CABAC_ZERO_WORD insertion is actually a 3-byte sequence 0x00 00 03. The inline data may have already been processed for start code emulation byte insertion, except the possibility of the last 2 bytes plus the very last partial byte (if any). Hence, when hardware performing the concatenation of multiple consecutive insertion commands, or concatenation of an insertion command and a PAK object command, it must check and perform the necessary start code emulation byte insert at the junction. The inline data is required to be byte aligned on the left (first transmitted bit order) and may or may not be byte aligned on the right (last transmitted bits).</p> <p>The command will specify the bit offset of the last valid DW. Each insertion state command defines a chunk of bits (compressed data) to be inserted at a specific location of the output compressed bitstream in the output buffer. Depend on CABAC or CAVLC encoding mode (from Slice State), PAK Object Command is always ended in byte aligned output bitstream except for CABAC header insertion which is bit aligned. In the aligned cases, PAK will perform 0 filling in CAVLC mode, and 1 filling in CABAC mode.</p> <p>Insertion data can include: any encoded syntax elements bit data before the encoded Slice Data (PAK Object Command) of the current Slice SPS NAL PPS NAL SEI NAL Other Non-Slice NAL Leading_Zero_8_bits (as many bytes as there is) Start Code Prefix NAL Header Byte Slice Header Any encoded syntax elements bit data after the encoded Slice Data (PAK Object Command) of the current Slice and prior to the next encoded Slice Data of the next Slice or prior to the end of the bistream, whichever comes first Cabac_Zero_Word or Trailing_Zero_8bits (as many bytes as there is).</p> <p>Anything listed above before a Slice Data Context switch interrupt is not supported by this command.</p>	

DWord	Bit	Description									
0	31:29	<b>Command Type</b>									
		Default Value:	3h PARALLEL_VIDEO_PIPE								
		Format:	OpCode								
	28:27	<b>Pipeline</b>									
		Default Value:	2h MFX_PAK_INSERT_OBJECT								
		Format:	OpCode								
	26:24	<b>Media Command Opcode</b>									
		Default Value:	0h MFX_COMMON								
		Format:	OpCode								
	23:21	<b>SubOpcode A</b>									
Default Value:		2h									
Format:		OpCode									
20:16	<b>SubOpcode B</b>										
	Default Value:	8h									
	Format:	OpCode									
15:12	<b>Reserved</b>										
11:0	<b>DWord Length</b>										
	Default Value:	0h Excludes DWord (0,1) = Variable Length in DW									
	Format:	=n Total Length - 2									
1	31:18	<b>Reserved</b>									
		Format:	MBZ								
	17:16	<b>DataByteOffset - SrcDataStartingByteOffset[1:0]</b>									
		Source Data Starting Byte Position within the very first inline DW.									
		<table border="1"> <thead> <tr> <th colspan="2">Programming Notes</th> </tr> </thead> <tbody> <tr> <td colspan="2">Must be set to 0 for JPEG encoder</td> </tr> </tbody> </table>		Programming Notes		Must be set to 0 for JPEG encoder					
Programming Notes											
Must be set to 0 for JPEG encoder											
15	<b>HeaderLengthExcludeFrmSize</b>										
	In case this flag is on, bits are NOT accumulated during current access unit coding neither for Cabac Zero Word insertion bits counting or for output in MMIO register MFC_BITSTREAM_BYTECOUNT_FRAME_NO_HEADER. When using HeaderLenghtExcludeFrmSize for header insertion, the software needs to make sure that data comes already with inserted start code emulation bytes. SW shouldn't set EmulationFlag bit ( Bit 3 of DWORD1 of MFX_PAK_INSERT_OBJECT).										
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>NO_ACCUMULATION</td> <td>Bits during current call are not accumulated</td> </tr> <tr> <td>0</td> <td>ACCUMULATE</td> <td>All bits accumulated</td> </tr> </tbody> </table>	Value	Name	Description	1	NO_ACCUMULATION	Bits during current call are not accumulated	0	ACCUMULATE	All bits accumulated	
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<table border="1"> <thead> <tr> <th>Programming Notes</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>Must be set to 0 for JPEG encoder</td> <td>CHV, BSW</td> </tr> </tbody> </table>		Programming Notes	Project	Must be set to 0 for JPEG encoder	CHV, BSW						
Programming Notes	Project										
Must be set to 0 for JPEG encoder	CHV, BSW										

## MFX\_PAK\_INSERT\_OBJECT

14	<b>Slice Header Indicator</b>	<p>This bit indicates if the insert object is a slice header. In the VDEnc mode, PAK only gets this command at the beginning of the frame for slice position X=0, Y=0. It internally generates the header that needs to be inserted per slice. For VDEnc mode, this bit should always be set.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 75%;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">1</td> <td>SLICE_HEADER</td> <td>Insertion Object is a Slice Header. The command is stored internally by HW and is used for inserting slice headers.</td> </tr> <tr> <td style="text-align: center;">0</td> <td>LEGACY</td> <td>Legacy Insertion Object command. The PAK Insertion Object command is not stored in HW.</td> </tr> </tbody> </table> <div style="border: 1px solid black; padding: 5px; margin-top: 10px;"> <p style="text-align: center; color: blue; font-weight: bold;">Programming Notes</p> <p>In VDENC mode, we support only Slice layer without partitioning RBSP syntax. The payload for PAK_INS_OBJ should contain only start code for Slice header followed by NAL_type and slice header (slice_header() in AVC spec). The payload for PAK_INS_OBJ shouldn't contain CABAC Byte alignment bits. HW adds these alignment bits which are part of slice_data. Example PAK_INS_OBJ payload : 00 00 01 &lt;NAL_type&gt; &lt;slice_header_Byte0&gt; .....&lt;slice_header_Byte LAST&gt; Any zero_bytes that are added before slice header can be inserted by any preceding general PAK_INS_OBJ.</p> </div>	Value	Name	Description	1	SLICE_HEADER	Insertion Object is a Slice Header. The command is stored internally by HW and is used for inserting slice headers.	0	LEGACY	Legacy Insertion Object command. The PAK Insertion Object command is not stored in HW.
Value	Name	Description									
1	SLICE_HEADER	Insertion Object is a Slice Header. The command is stored internally by HW and is used for inserting slice headers.									
0	LEGACY	Legacy Insertion Object command. The PAK Insertion Object command is not stored in HW.									
13:8	<b>DataBitsInLastDW - SrCDataEndingBitInclusion[5:0]</b>	<p>Source Data to be included in the very last inline DW. Follows the MSBit is the upper bit of each byte within the DW. The lower byte is actually processed first. For example, SrCDataEndingBitInclusion = 9, bit 7:0 and bit 15 are included as valid header data.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">[1,32]</td> <td></td> </tr> </tbody> </table>	Value	Name	[1,32]						
Value	Name										
[1,32]											
7:4	<b>SkipEmulByteCnt - Skip Emulation Byte Count</b>	<p>Skip emulation check for number of starting bytes. It can be programmed from 0 to 15 bytes. For example, to skip the start code that has already prefixed in the bitstream.</p> <div style="border: 1px solid black; padding: 5px; margin-top: 10px;"> <p style="text-align: center; color: blue; font-weight: bold;">Programming Notes</p> <p>Must be set to 0 for JPEG encoder</p> </div>									
3	<b>EmulationFlag - EmulationByteBitsInsertEnable</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 75%;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>NONE</td> <td>No emulation</td> </tr> <tr> <td style="text-align: center;">1</td> <td>EMULATE</td> <td>Instruct the hardware to perform Start Code Prefix (0x 00 00 01/02/03/00) Search and Prevention Byte (0x 03) insertion on the insertion data of this command. It is required that hardware will handle a start code prefix crossing the boundary between insertion commands, or an insertion command followed by a PAK Object command.</td> </tr> </tbody> </table> <div style="border: 1px solid black; padding: 5px; margin-top: 10px;"> <p style="text-align: center; color: blue; font-weight: bold;">Programming Notes</p> <p>Must be set to 0 for JPEG encoder</p> </div>	Value	Name	Description	0	NONE	No emulation	1	EMULATE	Instruct the hardware to perform Start Code Prefix (0x 00 00 01/02/03/00) Search and Prevention Byte (0x 03) insertion on the insertion data of this command. It is required that hardware will handle a start code prefix crossing the boundary between insertion commands, or an insertion command followed by a PAK Object command.
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<b>MFX_PAK_INSERT_OBJECT</b>													
	2	<p><b>LastHeaderFlag - LastSrcHeaderDataInsertCommandFlag</b>                      To process a series of consecutive insertion commands, this flag (=1) indicates the current command is the last 'header' insertion in the series. In CABAC, hardware must perform the "1" insert for byte align for Slice Header before Slice Data comes in in the next PAK-OBJECT command. In CAVLC, hardware ignores this bit</p>											
	1	<p><b>EndOfSliceFlag - LastDstDataInsertCommandFlag</b>                      No more insertion command and no more PAK-OBJECT command follows. Flush data out to memory</p>											
	0	<p><b>BitstreamStartReset - ResetBitStreamStartingPos</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">RESET</td> <td>Reset the bitstream buffer insertion position to the bitstream buffer starting position.</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">INSERT</td> <td>Insert the current command inline data starting at the current bitstream buffer insertion position</td> </tr> </tbody> </table> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Programming Notes</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Must be set to 1 for JPEG encoder</td> </tr> </tbody> </table>	Value	Name	Description	1	RESET	Reset the bitstream buffer insertion position to the bitstream buffer starting position.	0	INSERT	Insert the current command inline data starting at the current bitstream buffer insertion position	Programming Notes	Must be set to 1 for JPEG encoder
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0	INSERT	Insert the current command inline data starting at the current bitstream buffer insertion position											
Programming Notes													
Must be set to 1 for JPEG encoder													
2..n	31:0	<p><b>Insert Data Payload</b>                      Actual Data to be inserted to the output bitstream buffer.</p>											

## MFX\_PIPE\_BUF\_ADDR\_STATE

MFX_PIPE_BUF_ADDR_STATE			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>This state command provides the memory base addresses for all row stores, StreamOut buffer and reconstructed picture output buffers required by the MFD or MFC Engine (that are in addition to the row stores of the Bit Stream Decoding/Encoding Unit (BSD/BSE) and the reference picture buffers). This is a picture level state command and is common among all codec standards and for both encoder and decoder operating modes. However, some fields may only applicable to a specific codec standard. All Pixel Surfaces (original, reference frame and reconstructed frame) in the Encoder are programmed with the same surface state (NV12 and TileY format), except each has its own frame buffer base address. In the tile format, there is no need to provide buffer offset for each slice; since from each MB address, the hardware can calculated the corresponding memory location within the frame buffer directly.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h MFX_PIPE_BUF_ADDR_STATE
		Format:	OpCode
	26:24	<b>Common Opcode</b>	
		Default Value:	0h MFX_COMMON_STATE
		Format:	OpCode
	23:21	<b>SubOpcode A</b>	
		Default Value:	0h
		Format:	OpCode
	20:16	<b>SubOpcode B</b>	
		Default Value:	2h
Format:		OpCode	
15:12	<b>Reserved</b>		
	Format:	MBZ	
11:0	<b>DWord Length</b>		
	Format:	=n	
	Fixed Length		
	Value	Name	Description
3Bh	DWORD_COUNT_n [Default]	Excludes DWord (0,1)	CHV, BSW

<b>MFX_PIPE_BUF_ADDR_STATE</b>													
1	31:6	<p><b>Pre Deblocking Destination Address</b></p> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[31:6]</td> </tr> </table> <p>Specifies the 4K byte aligned frame buffer address for outputting the non-filtered reconstructed YUV picture (i.e. output of final adder in each codec standard, and prior to the deblocking filter unit). This field is ignored if PreDeblockOutEnable is set to 0 (disable).</p>	Format:	GraphicsAddress[31:6]									
	Format:	GraphicsAddress[31:6]											
5:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table>	Project:	CHV, BSW										
Project:	CHV, BSW												
2	31:16	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ									
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15:0	<p><b>Pre Deblocking Destination Address High</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>This field is for the upper range of Pre-Deblocking Destination Address. This field is ignored if <b>PreDeblockOutEnable</b> is set to 0 (disable).</p>	Project:	CHV, BSW	Format:	GraphicsAddress[47:32]								
Project:	CHV, BSW												
Format:	GraphicsAddress[47:32]												
3	31:15	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ									
	Format:	MBZ											
	14:13	<p><b>Reserved</b></p>											
	12:11	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ									
	Format:	MBZ											
	10:9	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ							
	Project:	CHV, BSW											
Format:	MBZ												
8:7	<p><b>Pre Deblocking - Arbitration Priority Control</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This field controls the priority of arbitration used in the GAC/GAM pipeline for this surface.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Highest priority</td> </tr> <tr> <td>01b</td> <td>Second highest priority</td> </tr> <tr> <td>10b</td> <td>Third highest priority</td> </tr> <tr> <td>11b</td> <td>Lowest priority</td> </tr> </tbody> </table>	Project:	CHV, BSW	Value	Name	00b	Highest priority	01b	Second highest priority	10b	Third highest priority	11b	Lowest priority
Project:	CHV, BSW												
Value	Name												
00b	Highest priority												
01b	Second highest priority												
10b	Third highest priority												
11b	Lowest priority												
6:5	<p><b>Memory Type: LLC/eLLC Cacheability Control (LeLLCCC) for Pre Deblocking Destination Address</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This is the field used in GT interface block to determine what type of access need to be generated to uncore. For the cases where the LeLLCCC is set, cacheable transaction are generated to enable LLC usage for particular stream.</p>	Project:	CHV, BSW										
Project:	CHV, BSW												

<b>MFX_PIPE_BUF_ADDR_STATE</b>																	
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 20%;">Value</th> <th style="width: 40%;">Name</th> <th style="width: 40%;">Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Use Cacheability Controls from page table</td> <td></td> </tr> <tr> <td>01b</td> <td>UC</td> <td>Uncacheable - non-cacheable</td> </tr> <tr> <td>10b</td> <td>WT</td> <td>Writethrough</td> </tr> <tr> <td>11b</td> <td>WB</td> <td>Writeback</td> </tr> </tbody> </table>	Value	Name	Description	00b	Use Cacheability Controls from page table		01b	UC	Uncacheable - non-cacheable	10b	WT	Writethrough	11b	WB	Writeback
Value	Name	Description															
00b	Use Cacheability Controls from page table																
01b	UC	Uncacheable - non-cacheable															
10b	WT	Writethrough															
11b	WB	Writeback															
	4:3	<p><b>Target Cache (TC) Pre Deblocking Destination Address</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This field allows the choice of LLC vs eLLC for caching.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 20%;">Value</th> <th style="width: 80%;">Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>eLLC Only - not snooped in GT</td> </tr> <tr> <td>01b</td> <td>LLC Only</td> </tr> <tr> <td>10b</td> <td>LLC/eLLC Allowed</td> </tr> <tr> <td>11b</td> <td>L3, LLC, eLLC Allowed</td> </tr> </tbody> </table>	Project:	CHV, BSW	Value	Name	00b	eLLC Only - not snooped in GT	01b	LLC Only	10b	LLC/eLLC Allowed	11b	L3, LLC, eLLC Allowed			
	Project:	CHV, BSW															
Value	Name																
00b	eLLC Only - not snooped in GT																
01b	LLC Only																
10b	LLC/eLLC Allowed																
11b	L3, LLC, eLLC Allowed																
	2	<b>Reserved</b>															
	1:0	<p><b>Age for QUADLRU (AGE) Pre Deblocking Destination Address</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This field allows the selection of AGE parameter for a given surface in LLC or eLLC. If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 20%;">Value</th> <th style="width: 80%;">Name</th> </tr> </thead> <tbody> <tr> <td>11b</td> <td>Good chance of generating hits</td> </tr> <tr> <td>10b</td> <td>Next good chance of generating hits</td> </tr> <tr> <td>01b</td> <td>Decent chance of generating hits</td> </tr> <tr> <td>00b</td> <td>Poor chance of generating hits</td> </tr> </tbody> </table>	Project:	CHV, BSW	Value	Name	11b	Good chance of generating hits	10b	Next good chance of generating hits	01b	Decent chance of generating hits	00b	Poor chance of generating hits			
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4	31:6	<p><b>Post Deblocking Destination Address</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[31:6]</td> </tr> </table> <p>Specifies the 4K byte aligned frame buffer address for outputting the post-loop filtered reconstructed YUV picture (i.e. output of the deblocking filter unit)This field is ignored if PostDeblockOutEnable is set to 0 (disable).</p>	Format:	GraphicsAddress[31:6]													
	Format:	GraphicsAddress[31:6]															
5:0	<p><b>Reserved</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table>	Project:	CHV, BSW														
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5	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ													
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15:0	<p><b>Post Deblocking Destination Address High</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table>	Project:	CHV, BSW	Format:	GraphicsAddress[47:32]												
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<b>MFX_PIPE_BUF_ADDR_STATE</b>				
		This field is for the upper range of Post-Deblocking Destination Address. This field is ignored if <b>PostDeblockOutEnable</b> is set to 0 (disable).		
6	31:15	<b>Reserved</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td>MBZ</td></tr></table>		MBZ
		MBZ		
	14:13	<b>Reserved</b> Project: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td>CHV, BSW</td></tr></table>		CHV, BSW
			CHV, BSW	
	Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td>MBZ</td></tr></table>		MBZ	
		MBZ		
	12:11	<b>Reserved</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td>MBZ</td></tr></table>		MBZ
		MBZ		
	10:9	<b>Reserved</b> Project: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td>CHV, BSW</td></tr></table>		CHV, BSW
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8:7	<b>Post Deblocking - Arbitration Priority Control</b> Project: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td>CHV, BSW</td></tr></table>			CHV, BSW
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	This field controls the priority of arbitration used in the GAC/GAM pipeline for this surface.			
	<b>Value</b>	<b>Name</b>		
	00b	Highest priority		
	01b	Second highest priority		
10b	Third highest priority			
11b	Lowest priority			
6:5	<b>Memory Type: LLC/eLLC Cacheability Control (LeLLCCC) for Post Deblocking Destination Address</b> Project: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td>CHV, BSW</td></tr></table>			CHV, BSW
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	<b>Value</b>	<b>Name</b>		
	00b	Use Cacheability Controls from page table		
	01b	UC		
10b	WT			
11b	WB			
4:3	<b>Target Cache (TC) for Post Deblocking Destination Address</b> Project: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td>CHV, BSW</td></tr></table>			CHV, BSW
		CHV, BSW		
This field controls the L3\$, LLC and eLLC (eDRAM) cacheability for a given surface. Setting of "00" points to PTE settings which defaults to eDRAM (when present). If no eDRAM, the access will be allocated to LLC. Setting of "01", allocates into LLC and victimizes the line to eDRAM. Setting of "10" allows the line to be allocated in either LLC or eDRAM. Setting of "11" is the only option for				

## MFX\_PIPE\_BUF\_ADDR\_STATE

		<p>a memory access to be allocated in L3\$ as well as LLC/eLLC            00b: eLLC Only ("00" setting points TC selection to PTE which defaults to eLLC)            01b: LLC Only (Works at the allocation time, later victimization from LLC downgrades the line to eLLC if present).            10b: LLC/eLLC Allowed.            11b: L3, LLC, eLLC Allowed.</p> <p><b>Errata CHV:A-E (FIXED BY:G0 Stepping):</b>            For all system that does NOT use SVM (i.e. coherent L3\$ surfaces), back snoops from LLC has to be disabled (<b>Dis_GtCvUpdtOnRd = "1"</b>). Than target Cache settings can be programmed as POR requirements of L3/LLC/eDRAM caching.            For all systems that does use SVM (i.e. coherent L3\$ surfaces), the recomend setting would be "00" in target cache settings. In case of L3 surfaces, the performance has to be tuned between "00" and "11" setting based on the benefits of L3 caching outweighing the degradation of backsnoops.            Post G0-stepping, the above w/a for coherent L3\$ surfaces is not needed.</p> <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 10px;"> <thead> <tr> <th style="width: 20%;">Value</th> <th style="width: 80%;">Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>eLLC Only - not snooped in GT</td> </tr> <tr> <td>01b</td> <td>LLC Only</td> </tr> <tr> <td>10b</td> <td>LLC/eLLC Allowed</td> </tr> <tr> <td>11b</td> <td>L3, LLC, eLLC Allowed</td> </tr> </tbody> </table>	Value	Name	00b	eLLC Only - not snooped in GT	01b	LLC Only	10b	LLC/eLLC Allowed	11b	L3, LLC, eLLC Allowed		
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	2	<p><b>Reserved</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table>	Project:	CHV, BSW										
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	1:0	<p><b>Age for QUADLRU (AGE) for Post Deblocking Destination Address</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches.</p> <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 10px;"> <thead> <tr> <th style="width: 20%;">Value</th> <th style="width: 80%;">Name</th> </tr> </thead> <tbody> <tr> <td>11b</td> <td>Good chance of generating hits.</td> </tr> <tr> <td>10b</td> <td>Next good chance of generating hits</td> </tr> <tr> <td>01b</td> <td>Decent good chance of generating hits</td> </tr> <tr> <td>00b</td> <td>Poor good chance of generating hits</td> </tr> </tbody> </table>	Project:	CHV, BSW	Value	Name	11b	Good chance of generating hits.	10b	Next good chance of generating hits	01b	Decent good chance of generating hits	00b	Poor good chance of generating hits
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Format:	GraphicsAddress[31:6]													
	5:0	<p><b>Reserved</b></p>												

<b>MFX_PIPE_BUF_ADDR_STATE</b>																		
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15:0	<p><b>Original Uncompressed Picture Source Address High</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>This field is for the upper range of Original Uncompressed Picture Source Address. This field is valid for <b>encoding</b> mode only.</p>	Project:	CHV, BSW	Format:	GraphicsAddress[47:32]													
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8:7	<p><b>Original Uncompressed Picture Source - Arbitration Priority Control</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This field controls the priority of arbitration used in the GAC/GAM pipeline for this surface.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Highest priority</td> </tr> <tr> <td>01b</td> <td>Second highest priority</td> </tr> <tr> <td>10b</td> <td>Third highest priority</td> </tr> <tr> <td>11b</td> <td>Lowest priority</td> </tr> </tbody> </table>	Project:	CHV, BSW	Value	Name	00b	Highest priority	01b	Second highest priority	10b	Third highest priority	11b	Lowest priority					
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10	31:6	<p><b>StreamOut Data Destination Base Address</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[31:6]</td> </tr> </table> <p>Specifies the 64 byte aligned address for outputting the per-MB indirect data to memory when <b>StreamOutEnable</b> is set in the MFX_PIPE_MODE_SELECT command. For Decoder : This field is used for transcoding purpose. For Encoder : This field is used for dynamic repeat of frame in PAK for Rate Control. Also used for feeding coding information back to the Host, Video Preprocessing Unit and ENC Unit. All data are written in fixed formats, and therefore all record sizes are known in the hardware. Hardware can calculate the offset into this base address for per-MB data.</p>	Format:	GraphicsAddress[31:6]										
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5:0	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ									
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11	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ										
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15:0	<p><b>StreamOut Data Destination Base Address High</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>This field is for the upper range of Original Uncompressed Picture Source Address</p>	Project:	CHV, BSW	Format:	GraphicsAddress[47:32]									
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12	31:15	<b>Reserved</b>												



<b>MFX_PIPE_BUF_ADDR_STATE</b>		
	Format:	MBZ
14:13	<b>Reserved</b>	
	Project:	CHV, BSW
	Format:	MBZ
12:11	<b>Reserved</b>	
	Format:	MBZ
8:7	<b>StreamOut Data Destination - Arbitration Priority Control</b>	
	Project:	CHV, BSW
	This field controls the priority of arbitration used in the GAC/GAM pipeline for this surface.	
	<b>Value</b>	<b>Name</b>
	00b	Highest priority
	01b	Second highest priority
10b	Third highest priority	
11b	Lowest priority	
6:5	<b>Memory Type: LLC/eLLC Cacheability Control (LeLLCCC) for StreamOut Data Destination Base Address</b>	
	Project:	CHV, BSW
	This is the field used in GT interface block to determine what type of access need to be generated to uncore. For the cases where the LeLLCCC is set, cacheable transaction are generated to enable LLC usage for particular stream.	
	<b>Value</b>	<b>Name</b>
	00b	Use Cacheability Controls from page table
	01b	UC
10b	WT	
11b	WB	
4:3	<b>Target Cache (TC) for StreamOut Data Destination Base Address</b>	
	Project:	CHV, BSW
	This field allows the choice of LLC vs eLLC for caching	
	<b>Value</b>	<b>Name</b>
	00b	eLLC Only - not snooped in GT
	01b	LLC Only
10b	LLC/eLLC Allowed	
11b	L3, LLC, eLLC Allowed	
2	<b>Reserved</b>	
	Project:	CHV, BSW
1:0	<b>Age for QUADLRU (AGE) for StreamOut Data Destination Base Address</b>	

<b>MFX_PIPE_BUF_ADDR_STATE</b>																
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13	31:6	<p><b>Intra Row Store Scratch Buffer Base Address</b></p> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[31:6]</td> </tr> </table> <p>This field provides the base address of the scratch buffer (read/write) used by the AVC/VP8 IntraPrediction unit to store MB information of the previous row for processing of each macroblock in the current row. The Intra Row Store buffer must be 64-byte cacheline aligned. Hardware uses the horizontal address of the current macroblock to address the Intra Row Store. This field is ignored in MPEG2 and VC1 mode. Max 256 cachelines for 4K pixels (1 cacheline for either MBAFF or non-MBAFF) Intra Row Store Scratch Buffer - Arbitration Priority Control</p> <table border="1"> <tr> <th style="text-align: center;">Programming Notes</th> </tr> <tr> <td> <p>This is one of the four RowStore Scratch Buffers which can be programmed to use the internal Media Cache (total size 640 Cacheline). When Intra Row Store Scratch Buffer Cache Select is programmed to "1", this data will be stored inside MFX Media Internal Storage. Driver then needs to program this Base Address between 0 to 639, indicating starting cachelines address to Media Cache. Driver needs to make sure the whole buffer fits into MFX Media Internal Storage. (Notes: 1 cacheline per MB, and the buffer needs to have enough space for 1 MB row).</p> </td> </tr> </table>	Format:	GraphicsAddress[31:6]	Programming Notes	<p>This is one of the four RowStore Scratch Buffers which can be programmed to use the internal Media Cache (total size 640 Cacheline). When Intra Row Store Scratch Buffer Cache Select is programmed to "1", this data will be stored inside MFX Media Internal Storage. Driver then needs to program this Base Address between 0 to 639, indicating starting cachelines address to Media Cache. Driver needs to make sure the whole buffer fits into MFX Media Internal Storage. (Notes: 1 cacheline per MB, and the buffer needs to have enough space for 1 MB row).</p>										
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<b>MFX_PIPE_BUF_ADDR_STATE</b>		
12	<b>Intra Row Store Scratch Buffer Cache Select</b>	
	Project:	CHV, BSW
	This field controls if Intra Row Store is going to store inside Media Cache or to LLC.	
	<b>Value</b>	<b>Name</b>
		<b>Description</b>
	0	Buffer going to LLC.
	1	Buffer going to Internal Media Storage
11	<b>Reserved</b>	
	Project:	CHV, BSW
	Format:	MBZ
10:9	<b>Reserved</b>	
	Project:	CHV, BSW
	Format:	MBZ
8:7	<b>Intra Row Store Scratch Buffer - Arbitration Priority Control</b>	
	Project:	CHV, BSW
	This field controls the priority of arbitration used in the GAC/GAM pipeline for this surface.	
	<b>Value</b>	<b>Name</b>
	00b	Highest priority
	01b	Second highest priority
10b	Third highest priority	
11b	Lowest priority	
6:5	<b>Memory Type: LLC/eLLC Cacheability Control (LeLLCCC) for Intra Row Store Scratch Buffer Base Address</b>	
	Project:	CHV, BSW
	This is the field used in GT interface block to determine what type of access need to be generated to uncore. For the cases where the LeLLCCC is set, cacheable transaction are generated to enable LLC usage for particular stream.	
	<b>Value</b>	<b>Name</b>
	00b	Use Cacheability Controls from page table
	01b	UC
	10b	WT
	11b	WB
	00b	Uncacheable - non-cacheable
	10b	Writethrough
11b	Writeback	
4:3	<b>Reserved</b>	
2	<b>Reserved</b>	
1:0	<b>Age for QUADLRU (AGE) for Intra Row Store Scratch Buffer Base Address</b>	
	Project:	CHV, BSW
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16	31:6	<p><b>Deblocking Filter Row Store Scratch Base Address</b></p> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[31:6]</td> </tr> </table> <p>Deblocking Filter Row Store is needed for:</p> <ul style="list-style-type: none"> <li>• AVC and VC1 In-Loop Deblocking Filter</li> <li>• VC1 Overlap-smoothing Filter</li> <li>• AVC, VC1, and MPEG-2 Out-Of-Loop Deblocking Filter (Intel extension)</li> </ul> <p>This field provides the 64 byte aligned base address of the scratch buffer (read and write) used by the deblocking filter unit to store MB information of the previous row for filtering of each macroblock in the current row. The Deblocking Filter Row Store buffer must be 64-byte cacheline aligned. Hardware uses the horizontal address of the current macroblock to address the Deblocking Filter Row Store. Max 6 cachelines for VC1 and MPEG2, and max 4 for AVC (for MBAFF, 2 for non-MBAFF)</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Programming Notes</th> </tr> </thead> <tbody> <tr> <td> <p>This is one of the four RowStore Scratch Buffers which can programmed to use the internal Media Cache (total size 640 CacheLine). When Deblocking Filter Row Store Scratch Buffer Cache Select is programmed to "1", this will be stored inside MFX Media Internal Storage. Driver then needs to program this Base Address between 0 to 639, indicating starting cachelines address location for this buffer. Driver needs to make sure the whole buffer fits into Media Internal Storage.</p> <p><i>(Notes: 2 cachelines per MB for non-mbaff; 4 cahcelines per MB pair for mbaff, and the buffer needs to have enough space for 1 MB (pair) row).</i></p> </td> </tr> </tbody> </table>		Format:	GraphicsAddress[31:6]	Programming Notes	<p>This is one of the four RowStore Scratch Buffers which can programmed to use the internal Media Cache (total size 640 CacheLine). When Deblocking Filter Row Store Scratch Buffer Cache Select is programmed to "1", this will be stored inside MFX Media Internal Storage. Driver then needs to program this Base Address between 0 to 639, indicating starting cachelines address location for this buffer. Driver needs to make sure the whole buffer fits into Media Internal Storage.</p> <p><i>(Notes: 2 cachelines per MB for non-mbaff; 4 cahcelines per MB pair for mbaff, and the buffer needs to have enough space for 1 MB (pair) row).</i></p>						
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	12	<b>Deblocking Filter Row Store Scratch Buffer Cache Select</b>											

<b>MFX_PIPE_BUF_ADDR_STATE</b>		
	Project:	CHV, BSW
	This field controls if Intra Row Store is going to store inside Media Internal Storage or to LLC.	
	<b>Value</b>	<b>Name</b> <b>Description</b>
	0	Buffer going to LLC
	1	Buffer going to Media Internal Storage
11	<b>Reserved</b>	
10:9	<b>Reserved</b>	
8:7	<b>Deblocking Filter Row Store Scratch - Arbitration Priority Control</b>	
	Project:	CHV, BSW
	This field controls the priority of arbitration used in the GAC/GAM pipeline for this surface.	
	<b>Value</b>	<b>Name</b>
	00b	Highest priority
	01b	Second highest priority
	10b	Third highest priority
	11b	Lowest priority
6:5	<b>Memory Type: LLC/eLLC Cacheability Control (LeLLCCC) for Deblocking Filter Row Store Scratch Base Address</b>	
	Project:	CHV, BSW
	This is the field used in GT interface block to determine what type of access need to be generated to uncore. For the cases where the LeLLCCC is set, cacheable transaction are generated to enable LLC usage for particular stream.	
	<b>Value</b>	<b>Name</b> <b>Description</b>
	00b	Use Cacheability Controls from page table
	01b	UC Uncacheable - non-cacheable
	10b	WT Writethrough
	11b	WB Writeback
4:3	<b>Target Cache (TC) for Deblocking Filter Row Store Scratch Base Address</b>	
	Project:	CHV, BSW
	This field allows the choice of LLC vs eLLC for caching	
	<b>Value</b>	<b>Name</b>
	00b	eLLC Only - not snooped in GT
	01b	LLC Only
	10b	LLC/eLLC Allowed
	11b	L3, LLC, eLLC Allowed
2	<b>Reserved</b>	
1:0	<b>Age for QUADLRU (AGE) for Deblocking Filter Row Store Scratch Base Address</b>	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC.If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older	

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19..50	63:48	<b>Reserved</b>											
	47:32	<b>Reference Picture Address [n] High</b>											
		Project:	CHV, BSW										
		Format:	Address[47:32]										
		This field is for the upper range of Reference Picture Addresses											
19..50	31:6	<b>Reference Picture Address [n]</b>											
		Format:	Address[31:6]										
	<p>Specifies the 64 byte aligned reference frame buffer addresses for the motion compensation operation in AVC/ /MPEG2. AVC can specify up to 16 YUV frame-based surfaces for both forward and backward references, i.e. L0+L1 total = 16 max. Any entry can be assigned to L0 or L1 or both lists. But VC1 and MPEG2, worst case, can use up to 2 YUV frame-based surfaces for both forward and backward references:</p> <ul style="list-style-type: none"> <li>• P-MB : RefAddr[0] - temporal closest previous field of a reference frame (can be the current frame)</li> <li>• RefAddr[1]- next temporal closest previous field of a reference frame (must be different from the current frame)</li> </ul> <p>It is a variant (without the LongTermRefPic specification) of the RefFrameList[16] defined in AVC DXVA Spec. RefAddr[0-15] is indexed by frame_storeID »1. It is not a packed list, i.e. invalid entries can scatter among the list. All invalid addresses must be set to a valid address RefAddr[0] by the driver. The same applies to VC1 and MPEG2.</p>												
	<b>Programming Notes</b>												
AVC: Always specifies all 16 addresses even some of them are not needed as indicated by the max num of active reference pictures. This is done for preventing data corruption (error, fault condition, etc.) by having all the references being set to a legal location.													
19..50	5:0	<b>Reserved</b>											
		Project:	CHV, BSW										
		Format:	MBZ										
51	31:15	<b>Reserved</b>											
		Format:	MBZ										
	14:13	<b>Reserved</b>											
	Project:	CHV, BSW											

<b>MFX_PIPE_BUF_ADDR_STATE</b>			
	Format:	MBZ	
12:9	<b>Reserved</b>		
	Format:	MBZ	
8:7	<b>Reference Picture - Arbitration Priority Control</b>		
	Project:	CHV, BSW	
	This field controls the priority of arbitration used in the GAC/GAM pipeline for this surface.		
	<b>Value</b>	<b>Name</b>	
	00b	Highest priority	
	01b	Second highest priority	
	10b	Third highest priority	
	11b	Lowest priority	
6:5	<b>Memory Type: LLC/eLLC Cacheability Control (LeLLCCC) for Reference Picture Addresses</b>		
	Project:	CHV, BSW	
	This is the field used in GT interface block to determine what type of access need to be generated to uncore. For the cases where the LeLLCCC is set, cacheable transaction are generated to enable LLC usage for particular stream. <b>Note: There is ONLY ONE LLC/eLLC Cacheability Control (LeLLCCC) for all 16 Reference Picture Addresses (RefAddr[0-15])</b>		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	00b	Use Cacheability Controls from page table	
	01b	UC	Uncacheable - non-cacheable
	10b	WT	Writethrough
	11b	WB	Writeback
4:3	<b>Target Cache (TC) for Reference Picture Addresses</b>		
	Project:	CHV, BSW	
	This field allows the choice of LLC vs eLLC for caching. <b>NOTE: There is ONLY ONE Target Cache (TC) for all 16 Reference Picture Addresses (RefAddr[0-15])</b>		
	<b>Value</b>	<b>Name</b>	
	00b	eLLC Only - not snooped in GT	
	01b	LLC Only	
	10b	LLC/eLLC Allowed	
	11b	L3, LLC, eLLC Allowed	
2	<b>Reserved</b>		
	Project:	CHV, BSW	
1:0	<b>Age for QUADLRU (AGE) for Reference Picture Addresses</b>		
	Project:	CHV, BSW	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces		

		<b>MFX_PIPE_BUF_ADDR_STATE</b>											
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52	31:6	<p><b>Macroblock Buffer Base Address or Decoded Picture Error/Status Buffer Base Address</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW)</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[31:6]</td> </tr> </table> <p><b>For decoder:</b> Specifies the 64 byte aligned buffer address for writing a single error/status record into the memory when <b>Pic Error/Status Report Enable</b> is set in the MFX_PIPE_MODE_SELECT Command. The error/status record is written by HW at the end of decoding one single picture. The record is written in a fixed format, total 96-bits in size always. Please refer to "Media VDBOX -&gt; Video Codec -&gt; Other Codec Functions -&gt; MFX Error Handling -&gt; Decoder" session for the output format.</p> <p><b>For encoder:</b> Specifies the 64 byte aligned buffer address for reading the per-MB indirect data from memory when <b>MacroblockStatEnable</b> is set in the MFX_AVC_IMG_STATE Command. This field is used for dynamic repeat of frame in PAK for Rate Control. Also used for feeding coding information back to the Host, Video Preprocessing Unit, and ENC Unit. All data are written in fixed formats, and therefore all record sizes are known in the hardware. Hardware can calculate the offset into this base address for per-MB data.</p>		Project:	CHV, BSW)	Format:	GraphicsAddress[31:6]						
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<b>MFX_PIPE_BUF_ADDR_STATE</b>			
	Format:	MBZ	
10:9	<b>Reserved</b>		
	Project:	CHV, BSW	
	Format:	MBZ	
8:7	<b>Macroblock Status Buffer - Arbitration Priority Control</b>		
	Project:	CHV, BSW	
	This field controls the priority of arbitration used in the GAC/GAM pipeline for this surface.		
	Value	Name	
	00b	Highest priority	
	01b	Second highest priority	
	10b	Third highest priority	
11b	Lowest priority		
6:5	<b>Memory Type: LLC/eLLC Cacheability Control (LeLLCCC) for Macroblock Status Buffer Base Address</b>		
	Project:	CHV, BSW	
	This is the field used in GT interface block to determine what type of access need to be generated to uncore. For the cases where the LeLLCCC is set, cacheable transaction are generated to enable LLC usage for particular stream.		
	Value	Name	Description
	00b	Use Cacheability Controls from page table	
	01b	UC	Uncacheable - non-cacheable
	10b	WT	Writethrough
11b	WB	Writeback	
4:3	<b>Target Cache (TC) for Macroblock Status Buffer Base Address</b>		
	Project:	CHV, BSW	
	This field allows the choice of LLC vs eLLC for caching.		
	Value	Name	
	00b	eLLC Only - not snooped in GT	
	01b	LLC Only	
	10b	LLC/eLLC Allowed	
11b	L3, LLC, eLLC Allowed		
2	<b>Reserved</b>		
	Project:	CHV, BSW	
1:0	<b>Age for QUADLRU (AGE) for Macroblock Status Buffer Base Address</b>		
	Project:	CHV, BSW	
This field allows the selection of AGE parameter for a given surface in LLC or eLLC.If a particular			

		<b>MFX_PIPE_BUF_ADDR_STATE</b>										
		<p>allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>11b</td> <td>Good chance of generating hits.</td> </tr> <tr> <td>10b</td> <td>Next good chance of generating hits</td> </tr> <tr> <td>01b</td> <td>Decent chance of generating hits</td> </tr> <tr> <td>00b</td> <td>Poor chance of generating hits</td> </tr> </tbody> </table>	Value	Name	11b	Good chance of generating hits.	10b	Next good chance of generating hits	01b	Decent chance of generating hits	00b	Poor chance of generating hits
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Value	Name																
11b	Good chance of generating hits.																
10b	Next good chance of generating hits																
01b	Decent chance of generating hits																
00b	Poor chance of generating hits																
58	31:6	<b>Second Macroblock ILDB StreamOut Buffer Base Address</b>															
	Format:	GraphicsAddress[31:6]															

<b>MFX_PIPE_BUF_ADDR_STATE</b>										
		64 byte aligned buffer. Specifies the 64 byte aligned buffer address for writing MB ILDB parameter per MB to memory when Debocker streamout enable is set in the MFX_PIPE_MODE_SELECT Command. The ildb MB control parameters are written by HW at the end of each decoding MB. Only AVC edge information is being streamed out. It is used in AVC decode mode only.								
	5:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ				
Project:	CHV, BSW									
Format:	MBZ									
59	31:16	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ						
	Format:	MBZ								
15:0	<p><b>Second Macroblock ILDB StreamOut Buffer Base Address High</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>This field is for the upper range of Second Macroblock ILDB StreamOutBuffer Base Address.</p>	Project:	CHV, BSW	Format:	GraphicsAddress[47:32]					
Project:	CHV, BSW									
Format:	GraphicsAddress[47:32]									
60	31:15	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ						
	Format:	MBZ								
	14:13	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ				
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	Format:	MBZ								
	12:11	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ						
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10:9	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ					
Project:	CHV, BSW									
Format:	MBZ									
8:7	<p><b>Second Macroblock ILDB StreamOut Buffer - Arbitration Priority Control</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This field controls the priority of arbitration used in the GAC/GAM pipeline for this surface.</p>	Project:	CHV, BSW							
Project:	CHV, BSW									
6:5	<p><b>Memory Type: LLC/eLLC Cacheability Control (LeLLCCC) for Second Macroblock ILDB StreamOut Buffer Base Address</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This is the field used in GT interface block to determine what type of access need to be generated to uncore. For the cases where the LeLLCCC is set, cacheable transaction are generated to enable LLC usage for particular stream.</p>		Project:	CHV, BSW						
	Project:	CHV, BSW								
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Use Cacheability Controls from page table</td> <td></td> </tr> <tr> <td>01b</td> <td>UC</td> <td>Uncacheable</td> </tr> </tbody> </table>	Value	Name	Description	00b	Use Cacheability Controls from page table		01b	UC
Value	Name	Description								
00b	Use Cacheability Controls from page table									
01b	UC	Uncacheable								

<b>MFX_PIPE_BUF_ADDR_STATE</b>			
	10b	WT	Writethrough
	11b	WB	Writeback
4:3	<b>Second Macroblock ILDB StreamOut Buffer Base Address - Target Cache (TC)</b>		
	Project:		CHV, BSW
	This field allows the choice of LLC vs eLLC for caching		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	00b	eLLC Only	not snooped in GT
	01b	LLC Only	
	10b	LLC/eLLC Allowed	
	11b	L3, LLC, eLLC Allowed	
2	<b>Reserved</b>		
1:0	<b>Age for QUADLRU (AGE) for Second Macroblock ILDB StreamOut Buffer Base Address</b>		
	Project:		CHV, BSW
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches.		
	<b>Value</b>	<b>Name</b>	
	00b	Poor chance of generating hits	
	01b	Decent chance of generating hits	
	10b	Next good chance of generating hits	
	11b	Good chance of generating hits	

## MFX\_PIPE\_MODE\_SELECT

MFX_PIPE_MODE_SELECT			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>Specifies which codec and hardware module is being used to encode/decode the video data, on a per-frame basis.</p> <p>The MFX_PIPE_MODE_SELECT command specifies which codec and hardware module is being used to encode/decode the video data, on a per-frame basis. It also configures the hardware pipeline according to the active encoder/decoder operating mode for encoding/decoding the current picture. Commands issued specifically for AVC and MPEG2 are ignored when VC1 is the active codec.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h MFX_COMMON
		Format:	OpCode
	26:24	<b>Opcode</b>	
		Default Value:	0h MFX_COMMON_STATE
		Format:	OpCode
	23:21	<b>SubOpA</b>	
Default Value:		0h	
Format:		OpCode	
20:16	<b>SubOpB</b>		
	Default Value:	0h MFX_PIPE_MODE_SELECT	
	Format:	OpCode	
15:12	<b>Reserved</b>		
	Format:	MBZ	
11:0	<b>DWord Length</b>		
	Format:	=n Total Length - 2	
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	3h	DWORD_COUNT_n [Default]	Excludes DWord (0,1)
1	31	<b>Reserved</b>	
	30	<b>Reserved</b>	
		Project:	CHV, BSW

<b>MFX_PIPE_MODE_SELECT</b>														
29	<b>Reserved</b>													
28:27	<b>Reserved</b>													
26	<b>Reserved</b>													
25	<b>Reserved</b>													
24	<b>Reserved</b>													
23:19	<b>Reserved</b>													
18	<p><b>Extended stream out enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U1</td> </tr> </table> <p>This bit can be set only when VDEnc_Mode is set.                      When this bit is set and MB stream out is enabled, per MB 1CL of data is streamed out. The actual contents of the stream out are listed in Media VDBOX &gt; Encoder VDEnc mode StreamOut Data Structure Definition.                      When this bit is not set, per MB ¼ CL data is streamed out. The actual contents of the stream out are listed in Media VDBOX &gt; Encoder StreamOut Mode Data Structure Definition.</p>		Format:	U1										
Format:	U1													
17	<p><b>Decoder Short Format Mode</b>                      For IT mode, this bit must be 0.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 40%;">Name</th> <th style="width: 50%;">Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>Long Format Driver Interface</td> <td>[CHV, BSW] AVC/VC1/MVC/ VP8 Long Format Mode is in use.</td> </tr> <tr> <td>0</td> <td>Short Format Driver Interface <b>[Default]</b></td> <td>AVC/VC1/MVC/ VP8 Short Format Mode is in use  <b>Note: There is no Short Format for VP8 yet, so this field must be set to 1 for VP8.</b></td> </tr> </tbody> </table>		Value	Name	Description	1	Long Format Driver Interface	[CHV, BSW] AVC/VC1/MVC/ VP8 Long Format Mode is in use.	0	Short Format Driver Interface <b>[Default]</b>	AVC/VC1/MVC/ VP8 Short Format Mode is in use <b>Note: There is no Short Format for VP8 yet, so this field must be set to 1 for VP8.</b>			
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16:15	<p><b>Decoder Mode select</b>                      Each coding standard supports two entry points: VLD entry point and IT (IDCT) entry point. This field selects which one is in use. This field is only valid if Codec Select is 0 (decoder).</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 75%;">Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>VLD Mode</td> <td>All codec minimum must support this mode                      Configure the MFD Engine for VLD Mode Note: All codec minimum must support this mode</td> </tr> <tr> <td>1h</td> <td>IT Mode</td> <td>Configure the MFD Engine for IT Mode Note: Only VC1 and MPEG2 support this mode</td> </tr> <tr> <td>2h</td> <td>Deblocker Mode</td> <td>Configure the MFD Engine for Standalone Deblocker Mode. Require streamout AVC edge control information from preceeding decoding pass.</td> </tr> </tbody> </table>		Value	Name	Description	0h	VLD Mode	All codec minimum must support this mode Configure the MFD Engine for VLD Mode Note: All codec minimum must support this mode	1h	IT Mode	Configure the MFD Engine for IT Mode Note: Only VC1 and MPEG2 support this mode	2h	Deblocker Mode	Configure the MFD Engine for Standalone Deblocker Mode. Require streamout AVC edge control information from preceeding decoding pass.
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14:13	<b>Reserved</b>													
12	<p><b>Deblocker Stream-Out Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td style="width: 50%;">CHV, BSW</td> </tr> </table> <p>This field indicates if Deblocker information is going to be streamout during VLD decoding. For AVC, it is needed to enable the deblocker streamout as the AVC Disable_DLKFilterIdc is a slice</p>		Project:	CHV, BSW										
Project:	CHV, BSW													

<b>MFX_PIPE_MODE_SELECT</b>											
		<p>level parameters. Driver needs to determine ahead of time if at least one slice of the current frame/ has deblocker ON.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disable</td> <td>Disable streamout of deblocking control information for standalone deblocker operation.</td> </tr> <tr> <td>1h</td> <td>Enable</td> <td></td> </tr> </tbody> </table>	Value	Name	Description	0h	Disable	Disable streamout of deblocking control information for standalone deblocker operation.	1h	Enable	
Value	Name	Description									
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11	<p><b>Pic Error/Status Report Enable.</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This field control whether the error/status reporting is enable or not.0: Disable1: Enable In decoder modes: Error reporting is written out once per frame. The Error Report frame ID listed in DW3 along with the VLD/IT error status bits are packed into one cache and written to the "Decoded Picture Error/Status Buffer address" listed in the MFX_PIPE_BUF_ADDR_STATE Command. Note: driver shall program different error buffer addresses between pictures; otherwise, hardware might overwrite previous written data if driver does not read it fast enough. In encoder modes: Not used Please refer to "Media VDBOX -&gt; Video Codec -&gt; Other Codec Functions -&gt; MFX Error Handling -&gt; Decoder" session for the output format.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disable</td> </tr> <tr> <td>1h</td> <td>Enable</td> </tr> </tbody> </table>		Project:	CHV, BSW	Value	Name	0h	Disable	1h	Enable	
Project:	CHV, BSW										
Value	Name										
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1h	Enable										
10	<p><b>Stream-Out Enable</b></p> <p>This field controls whether the macroblock parameter stream-out is enabled during VLD decoding for transcoding purpose.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disable</td> </tr> <tr> <td>1h</td> <td>Enable</td> </tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>In decoder modes: The Stream-Out feature is added to support transcoding. While decoding the input compressed stream, selected decoded information may be used by the encoder for re-compression. In encoder modes: This feature used to perform dynamic Multipass of PAK for conformance pupose. Also it provides feedback to host (ENC) for future needs. Software can use this bit to disable writing PAK steam data to the streamout buffer for last pass of frame in PAK. Thus, save memory bandwidth.</p>		Value	Name	0h	Disable	1h	Enable			
Value	Name										
0h	Disable										
1h	Enable										
9	<p><b>Post Deblocking Output Enable (PostDeblockOutEnable)</b></p> <p>This field controls the output write for the reconstructed pixels AFTER the deblocking filter.In MPEG2 decoding mode, if this is enabled, VC1 deblocking filter is used.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disable</td> </tr> <tr> <td>1h</td> <td>Enable</td> </tr> </tbody> </table>		Value	Name	0h	Disable	1h	Enable			
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7:6	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>		Project:	CHV, BSW	Format:	MBZ																										
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5	<p><b>Stitch Mode</b></p> <table border="1"> <tr> <td>Exists If:</td> <td>//CodecSel=Encode and StandardSel=AVC</td> </tr> </table> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Not in stitch mode</td> <td></td> </tr> <tr> <td>1h</td> <td>In the special stitch mode</td> <td>This mode can be used for any Codec as long as bitfield conditions are met.</td> </tr> </tbody> </table>		Exists If:	//CodecSel=Encode and StandardSel=AVC	Value	Name	Description	0h	Not in stitch mode		1h	In the special stitch mode	This mode can be used for any Codec as long as bitfield conditions are met.																			
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Value	Name	Description																														
0000b	MPEG2																															
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28	<p><b>Reserved</b></p>																															

<b>MFX_PIPE_MODE_SELECT</b>		
27	<b>Reserved</b>	
26	<b>Reserved</b>	
	Project:	CHV, BSW
25	<b>Reserved</b>	
	Project:	CHV, BSW
24	<b>VHR MVC Field Reference List Logic Enable</b>	
	Project:	CHV, BSW
	<b>Value</b>	<b>Name</b>
	0	Disable <b>[Default]</b>
	1	Enable
		<b>Description</b>
		Disable MVC Field Logic
		VHR MVC Field Enable
23	<b>Reserved</b>	
22:21	<b>Reserved</b>	
20:19	<b>Reserved</b>	
	Project:	CHV, BSW
	Format:	MBZ
18	<b>Reserved</b>	
	Format:	MBZ
17	<b>Reserved</b>	
	Project:	CHV, BSW
16	<b>Reserved</b>	
15	<b>Reserved</b>	
14	<b>VLF 720i (Odd Height) in VC1 Mode</b>	
	Project:	CHV, BSW
	This bit indicates VLF write out VC1 picture with odd height (in MBs).	
	<b>Value</b>	<b>Name</b>
	0	Disable <b>[Default]</b>
	1	Enable
		<b>Description</b>
		720i Enable
13	<b>Reserved</b>	
12	<b>Reserved</b>	
11	<b>Reserved</b>	
10	<b>MPC pref08x8_disable Flag (Default 0)</b>	
	<b>Value</b>	<b>Name</b>
	0	Disable
	1	Enable
9	<b>Reserved</b>	

<b>MFX_PIPE_MODE_SELECT</b>		
		Format: MBZ
8	<b>Reserved</b>	
	Project:	CHV, BSW
7	<b>Reserved</b>	
6	<b>Clock gate Enable at Slice-level</b>	
	BitFieldDesc:	
	<b>Value</b>	<b>Name</b> <b>Description</b>
	0	Disable      Disable Slice-level Clock gating, Unit-level Clock gating will apply
	1	Enable      Enable Slice-level Clock gating, overrides any Unit level Clock gating
5	<b>Reserved</b>	
4	<b>Reserved</b>	
3	<b>VDS ILDB Calculation</b>	
	Project:	CHV, BSW
	This bit forces all MB into INTRA MBs before doing ILDB control generation in VDS.	
	<b>Value</b>	<b>Name</b> <b>Description</b>
	0	Disable <b>[Default]</b> Use original definition for ILDB calculation.
	1	Enable      Force neighbor Intra MB = 1 on ILDB BS calculation.
	<b>Programming Notes</b>	
	When the bit is '0', the ILDB control generation will be the same as the original spec (AVC/VC1).	
2:1	<b>Reserved</b>	
	Project:	CHV, BSW
0	<b>Reserved</b>	
	Project:	CHV, BSW
3	31:0	<b>Pic Status/Error Report ID</b>
	Exists If:	//Decoder Mode Only
	Format:	U32
	In decoder modes: Error reporting is written out once per frame. This field along with the VLD error status bits are packed into one cache and written to the memory location specified by "Decoded Picture Error/Status Buffer address" listed in the MFX_PIPE_BUF_ADDR_STATE Command.	
	<b>Value</b>	<b>Name</b> <b>Description</b>
	0h	32-bit unsigned      Unique ID Number
	1h	Reserved
4	31:0	<b>Media Soft-Reset Counter (per 1000 clocks)</b>
	Project:	CHV, BSW
	In decoder modes, this indicates the number of clocks (per 1000) VINunit will wait for inactivity from MFX pipeline before issuing media soft reset. If this counter is set to 0, VINunit will never	

## MFX\_PIPE\_MODE\_SELECT

issue soft media reset. In encoder modes: This counter must be set to 0 to disable media soft reset since encoder mode is not supported.

Value	Name	Project
0	Disable	CHV, BSW

## MFX\_QM\_STATE

<b>MFX_QM_STATE</b>			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>This is a common state command for AVC encoder modes. For encoder, it represents both the forward QM matrices as well as the decoding QM matrices. This is a Frame-level state. Only Scaling Lists specified by an application are being sent to the hardware. The driver is responsible for determining the final set of scaling lists to be used for decoding the current slice, based on the AVC Spec Table 7-2 (Fall-Back Rules A and B). In MFX AVC PAK mode, PAK needs both forward Q scaling lists and IQ scaling lists. The IQ scaling lists are sent as in MFD in raster scan order. But the Forward Q scaling lists are sent in column-wise raster order (column-by-column) to simplify the H/W. Driver will perform all the scan order conversion for both ForwardQ and IQ.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h MFX_MULTI_DW
		Format:	OpCode
	26:24	<b>Media Command Opcode</b>	
		Default Value:	0h MFX_COMMON_STATE
		Format:	OpCode
	23:21	<b>SubOpcode A</b>	
		Default Value:	0h
		Format:	OpCode
	20:16	<b>SubOpcode B</b>	
		Default Value:	7h
Format:		OpCode	
15:12	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
11:0	<b>DWord Length</b>		
	Default Value:	20h Excludes DWord (0,1)	
	Project:	All	
	Format:	=n Total Length - 2	
1	31:2	<b>Reserved</b>	
		Format:	MBZ

<b>MFX_QM_STATE</b>													
1:0	<p><b>AVC</b></p> <table border="1"> <tr> <td>Exists If:</td> <td>//AVC- Decoder Only</td> </tr> </table> <p><b>For AVC QM Type:</b> This field specifies which Quantizer Matrix is loaded.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>AVC_4x4_Intra_MATRIX, (Y-4DWs, Cb-4DWs, Cr-4DWs, reserved-4DWs)</td> </tr> <tr> <td>1</td> <td>AVC_4x4_Inter_MATRIX, (Y-4DWs, Cb-4DWs, Cr-4DWs, reserved-4DWs)</td> </tr> <tr> <td>2</td> <td>AVC_8x8_Intra_MATRIX</td> </tr> <tr> <td>3</td> <td>AVC_8x8_Inter_MATRIX</td> </tr> </tbody> </table>	Exists If:	//AVC- Decoder Only	Value	Name	0	AVC_4x4_Intra_MATRIX, (Y-4DWs, Cb-4DWs, Cr-4DWs, reserved-4DWs)	1	AVC_4x4_Inter_MATRIX, (Y-4DWs, Cb-4DWs, Cr-4DWs, reserved-4DWs)	2	AVC_8x8_Intra_MATRIX	3	AVC_8x8_Inter_MATRIX
	Exists If:	//AVC- Decoder Only											
	Value	Name											
	0	AVC_4x4_Intra_MATRIX, (Y-4DWs, Cb-4DWs, Cr-4DWs, reserved-4DWs)											
	1	AVC_4x4_Inter_MATRIX, (Y-4DWs, Cb-4DWs, Cr-4DWs, reserved-4DWs)											
	2	AVC_8x8_Intra_MATRIX											
	3	AVC_8x8_Inter_MATRIX											
	1:0	<p><b>MPEG2</b></p> <table border="1"> <tr> <td>Exists If:</td> <td>//MPEG2- Decoder Only</td> </tr> </table> <p><b>For MPEG2 QM Type:</b> This field specifies which Quantizer Matrix is loaded.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>MPEG_INTRA_QUANTIZER_MATRIX</td> </tr> <tr> <td>1</td> <td>MPEG_NON_INTRA_QUANTIZER_MATRIX</td> </tr> <tr> <td>2-3</td> <td>Reserved</td> </tr> </tbody> </table>	Exists If:	//MPEG2- Decoder Only	Value	Name	0	MPEG_INTRA_QUANTIZER_MATRIX	1	MPEG_NON_INTRA_QUANTIZER_MATRIX	2-3	Reserved	
		Exists If:	//MPEG2- Decoder Only										
		Value	Name										
0		MPEG_INTRA_QUANTIZER_MATRIX											
1		MPEG_NON_INTRA_QUANTIZER_MATRIX											
2-3	Reserved												
1:0	<p><b>JPEG</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table> <table border="1"> <tr> <td>Exists If:</td> <td>//JPEG- Encoder Only</td> </tr> </table> <p><b>For JPEG QM Type:</b> This field specifies which Quantizer Matrix is loaded.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>JPEG_Luma_Y_QUANTIZER_MATRIX (or R)</td> </tr> <tr> <td>1</td> <td>JPEG_Chroma_Cb_QUANTIZER_MATRIX (or G)</td> </tr> <tr> <td>2</td> <td>JPEG_Chroma_Cr_QUANTIZER_MATRIX (or B)</td> </tr> </tbody> </table>	Project:	CHV, BSW	Exists If:	//JPEG- Encoder Only	Value	Name	0	JPEG_Luma_Y_QUANTIZER_MATRIX (or R)	1	JPEG_Chroma_Cb_QUANTIZER_MATRIX (or G)	2	JPEG_Chroma_Cr_QUANTIZER_MATRIX (or B)
	Project:	CHV, BSW											
	Exists If:	//JPEG- Encoder Only											
	Value	Name											
	0	JPEG_Luma_Y_QUANTIZER_MATRIX (or R)											
	1	JPEG_Chroma_Cb_QUANTIZER_MATRIX (or G)											
	2	JPEG_Chroma_Cr_QUANTIZER_MATRIX (or B)											
<b>Programming Notes</b>													
For JPEG encoder, each quantization element presents 16-bit $1/QM[i][j]$ . In RGB encoding, because the order input image components can be RGB, GBR, BGR, YUV, the value 0 is used for the first image component, the value 1 is used for the second image component, and the value 2 is used for the third image component.													
2..33	<p>31:0 <b>Forward Quantizer Matrix</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>The format of a Quantizer Matrix is an 8x8 matrix in raster order. Each element is an unsigned byte.</p>	Project:	All	Format:	U32								
Project:	All												
Format:	U32												

## MFX\_STATE\_POINTER

### MFX\_STATE\_POINTER

Project: CHV, BSW  
 Source: VideoCS  
 Length Bias: 2

The MFX\_STATE\_POINTER command, issued at picture level, is used to set up the indirect pointers for VCS to fetch all the MFX states (Image state, Slice state, etc.) needed for the encoding/decoding process in PAK/IT mode. The encoding/decoding states are presented by state commands, which are grouped into separate sets (picture level, slice level, etc.), and each is stored in its own memory buffer referred by an indirect state pointer. The content of each indirect state buffer is a list of MFX state commands with no special format requirements. The sequence of commands in each indirect state buffer is terminated by a MI\_BATCH\_BUFFER\_END command (acts as the last command marker). Therefore, indirect state buffers can have different and variable length of command sequences.

The indirection is designed to facilitate context switching in the middle of a codec operation. The smallest granularity of interruption is designed to be at a completed MB row in AVC/VC1/MPEG2 IT and AVC PAK operating modes as well as in VC1/MPEG2 VLD mode. There is no support for context switch in AVC VLD mode. Hardware supports up to 4 separate indirect state pointers, allowing software to manage the grouping of state commands. During context switch, hardware restores (re-issues) the latest version of each indirect state pointer, if present.

MFX\_STATE\_POINTER command can only program one indirect state pointer at a time. MI\_FLUSH will invalidate all indirect state buffer pointers inside VCS.

DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 3h GFX_PIPE
		Format: OpCode
	28:27	<b>Pipeline</b>
		Default Value: 2h Media
		Format: OpCode
	26:24	<b>Media Command Opcode</b>
		Default Value: 0h MFX_COMMON_STATE
		Format: OpCode
	23:21	<b>SubOpcode A</b>
		Default Value: 0h
		Format: OpCode
20:16	<b>SubOpcode B</b>	
	Default Value: 6h	
	Format: OpCode	
15:12	<b>Reserved</b>	

<b>MFX_STATE_POINTER</b>				
	11:0	<b>DWord Length</b>		
		Default Value:	0h DWORD_COUNT_n	
		Project:	All	
		Format:	=n Total Length - 2	
1	31:5	<b>State Pointer</b>		
		Format:	GeneralStateOffset[31:5]Indirect State Buffer	
	Specifies the 32-byte aligned address of an Indirect State Buffer. This pointer is relative to the General State Base Address.			
	4:2	<b>Reserved</b>		
		Project:	All	
		Format:	MBZ	
	1:0	<b>State Pointer Index</b>		
		Specifies one of the four indirect state pointers to program.		
		<b>Value</b>	<b>Name</b>	<b>Description</b>
		00b		indirect state pointer 0 (image state)
01b			indirect state pointer 1 (slice state)sc	
10b			indirect state pointer 2	
11b		indirect state pointer 3		
		<b>Project</b>		
		All		
		All		



## MFX\_STITCH\_OBJECT

<b>MFX_STITCH_OBJECT</b>			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>The MFC_STITCH_OBJECT command is used when stitch-enabled is set to 1, while CodecSel and StandardSel are set to ENCODE and AVC, respectively. This command is used, for example, to stitch multiple bitstreams to form a transport stream.</p> <p>It is a variable length command as the data to be inserted are presented as either inline data and/or indirect data of this command. Multiple insertion commands can be issued back to back in a series. It is host software's responsibility to make sure their corresponding data will properly stitch together to form a valid output. Hardware keeps track of an output bitstream buffer current byte position and the associated next bit insertion position index. Context switch interrupt is not supported by this command.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h MFC_STITCH_OBJECT
		Format:	OpCode
	26:24	<b>Media Command Opcode</b>	
		Default Value:	0h MFX_COMMON
		Format:	OpCode
	23:21	<b>SubOpcode A</b>	
Default Value:		2h	
Format:		OpCode	
20:16	<b>SubOpcode B</b>		
	Default Value:	Ah	
	Format:	OpCode	
15:12	<b>Reserved</b>		
11:0	<b>DWord Length</b>		
	Default Value:	0h Excludes DWord (0,1) = Variable Length in DW (>= 3)	
	Format:	=n Total Length - 2	
If it is 3, it indicates the absent of inline data.			
1	31:18	<b>Reserved</b>	
	17:16	<b>Source Data Starting Byte Offset</b> Source Data Starting Byte Position within the very first inline DW.	

<b>MFX_STITCH_OBJECT</b>	
15:14	<b>Reserved</b>
	Format: MBZ
	<b>13:8 Source Data Ending Bit Inclusion</b> Source Data to be included in the very last inline DW. Follows the MSBit is the upper bit of each byte within the DW. The lower byte is actually processed first. For example, SrCDataEndingBitInclusion =9, bit 7:0 and bit 15 are included as valid header data.
	<b>Value</b>
	<b>Name</b>
	[1,32]
	<b>7:4 Reserved</b>
	<b>3 Reserved</b>
	<b>2 Last Source Header Data Insert Command Flag</b> To process a series of consecutive insertion commands, this flag (=1) indicates the current command is the last 'header' insertion in the series. In CABAC, hardware must perform the "1" insert for byte align for Slice Header before Slice Data comes in in the next PAK-OBJECT command. In CAVLC, hardware ignores this bit.
	<b>1 Last Destination Data Insert Command Flag</b> THIS FIELD MUST BE THE SAME AS Last Source Header Data Insert Command Flag No more insertion command and no more PAK-OBJECT command follows. Flush data out to memory
<b>0 Reserved</b>	
2	<b>31:19 Reserved</b>
	Format: MBZ
	<b>18:0 Indirect Data Length</b> Project: CHV, BSW Format: U19 This field provides the length in bytes of the indirect data. A value zero indicates that indirect data fetching is disabled - subsequently, the Indirect Data Start Address field is ignored. This field must have the same alignment as the Indirect Object Data Start Address.
3	<b>31:0 Indirect Data Start Address</b>
	Format: MfxIndirectBitstreamObjectAddress[31:0] This field specifies the Graphics Memory starting address of the data to be loaded into the kernel for processing. This pointer is relative to the MFX Indirect Bitstream Object Base Address. Hardware ignores this field if indirect data is not present.
4..n	<b>31:0 Insert Data Payload</b> Inline data to be inserted to the output bitstream buffer

## MFX\_SURFACE\_STATE

<b>MFX_SURFACE_STATE</b>	
Project:	CHV, BSW
Source:	VideoCS
Length Bias:	2
<p>This command is common for all encoding/decoding modes, to specify the uncompressed YUV picture (i.e. destination surface) or intermediate streamout in/out surface (e.g. coefficient/residual) (field, frame or interleaved frame) format for reading and writing:</p> <ul style="list-style-type: none"> <li>Uncompressed, original input picture to be encoded</li> <li>Reconstructed non-filtered/filtered display picture (becoming reference pictures as well for subsequent temporal inter-prediction)</li> </ul> <p>Since there is only one media surface state being active during the entire encoding/decoding process, all the uncompressed/reconstructed pictures are defined to have the same surface state. The primary difference among picture surface states is their individual programmed base addresses, which are provided by other state commands and not included in this command. MFX engine is making the association of surface states and corresponding buffer base addresses.</p> <p>MFX engine currently supports only one media surface type for video and that is the NV12 (Planar YUV420 with interleaved U (Cb) and V (Cr)). For optimizing memory efficiency based on access patterns, only TileY is supported. For JPEG decoder, only IMC1 and IMC3 are supported. Pitch can be wider than the Picture Width in pixels and garbage will be there at the end of each line. The following describes all the different formats that are supported and not supported in Gen7 MFX :</p> <ul style="list-style-type: none"> <li>NV12 - 4:2:0 only; UV interleaved; Full Pitch, U and V offset is set to 0 (the only format supported for video codec); vertical UV offset is MB aligned; UV xoffsets = 0. JPEG does not support NV12 format because non-interleave JPEG has performance issue with partial write (in interleaved UV format)</li> <li>IMC 1 &amp; 3 - Full Pitch, U and V are separate plane; (JPEG only; U plane + garbage first in full pitch followed by V plane + garbage in full pitch). U and V vertical offsets are block aligned; U and V xoffset = 0; there is no gap between Y, U and V planes. IMC1 and IMC3 are different by a swap of U and V. This is the only format supported in JPEG for all video subsampling types (4:4:4, 4:2:2 and 4:2:0)</li> <li>We are not supporting IMC 2 &amp; 4 - Full Pitch, U and V are separate plane (JPEG only; U plane first in full pitch followed by V plane in full pitch - U and V plane are side-by-side). U and V vertical offsets are 16-pixel aligned; V xoffset is half-pitch aligned; U xoffset is 0; there is no gap between Y, U and V planes. IMC2 and IMC4 are different by a swap of U and V.</li> <li>We are not supporting YV12 - half pitch for each U and V plane, and separate planes for Y, U and V (U plane first in half pitch followed by V plane in half pitch). For YV12, U and V vertical offsets are block aligned; U and V xoffset = 0; there is no gap between Y, U and V planes</li> </ul> <p>Note that the following data structures are not specified through the media surface state</p> <ul style="list-style-type: none"> <li>1D buffers for row-store and other miscellaneous information.</li> <li>2D buffers for per-MB data-structures (e.g. DMV biffer, MB info record, ILDB Control and Tcoeff/Stocoeff).</li> </ul> <p>This surface state here is identical to the Surface State for deinterlace and sample_8x8 messages described in the Shared Function Volume and Sampler Chapter.</p> <p>For non pixel data, such as row stores, indirect data (Compressed Slice Data, AVC MV record, Coeff record and</p>	

## MFX\_SURFACE\_STATE

AVC ILDB record) and streamin/out and output compressed bitstream, a linear buffer is employed. For row stores, the H/W is designed to guarantee legal memory accesses (read and write). For the remaining cases, indirect object base address, indirect object address upper bound, object data start address (offset) and object data length are used to fully specified their corresponding buffer. This mechanism is chosen over the pixel surface type because of their variable record sizes.

All row store surfaces are linear surface. Their addresses are programmed in Pipe\_Buf\_Base\_State or Bsp\_Buf\_Base\_Addr\_State

### Programming Notes

VC1 I picture scaling: Even though VC1 allows I reconstructed picture scaling (via RESPIC), as such scaling is only allowed at I picture. All subsequent P (and B) pictures must have the same picture dimensions with the preceding I picture. Therefore, all reference pictures for P or B picture can share the same surface state with the current P and B picture. Note : H/W is not processing RESPIC. Application is no longer expecting intel decoder pipeline and kernel to perform this function, it is going to be done in the video post-processing scaler or display controller scale as a separate step and controller.

All video codec surfaces must be NV12 Compliant, except JPEG. U/V vertical must be MB aligned for all video codec (further constrained for field picture), but JPEG can be block aligned. All video codec and JPEG uses Tiled - Y format only, for uncompressed pixel surfaces.

Even for JPEG planar 420 surface, application may provide only 1 buffers, but there is still only one single surface state for all of them. If IMC equal to 1, 2, 3 or 4, U and V have the pitch same as Y. And U and V will have different offset, each offset is block aligned.

DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h MFX_COMMON
		Format:	OpCode
	26:24	<b>Opcode</b>	
		Default Value:	0h MFX_COMMON_STATE
		Format:	OpCode
	23:21	<b>SubOpA</b>	
		Default Value:	0h
		Format:	OpCode
	20:16	<b>SubOpB</b>	
		Default Value:	1h
		Format:	OpCode
15:12	<b>Reserved</b>		
	Format:	MBZ	

<b>MFX_SURFACE_STATE</b>																							
	11:0	<b>DWord Length</b> Format: =n Total Length - 2																					
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>4h</td> <td>DWORD_COUNT_n <b>[Default]</b></td> <td>Excludes DWord (0,1)</td> </tr> </tbody> </table>	Value	Name	Description	4h	DWORD_COUNT_n <b>[Default]</b>	Excludes DWord (0,1)															
Value	Name	Description																					
4h	DWORD_COUNT_n <b>[Default]</b>	Excludes DWord (0,1)																					
1	31:4	<b>Reserved</b> Format: MBZ																					
	3:0	<b>Surface Id</b> Project: CHV, BSW Format: U4																					
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>Reserved</td> <td></td> </tr> <tr> <td>0001b</td> <td>Reserved</td> <td></td> </tr> <tr> <td>0010b</td> <td>Reserved</td> <td></td> </tr> <tr> <td>0011b</td> <td>Reserved</td> <td></td> </tr> <tr> <td>0100b</td> <td>Source Input Picture (encoder)</td> <td>8-bit uncompressed data</td> </tr> <tr> <td>0101b</td> <td>Reconstructed Scaled Reference Picture</td> <td>8-bit data</td> </tr> </tbody> </table>	Value	Name	Description	0000b	Reserved		0001b	Reserved		0010b	Reserved		0011b	Reserved		0100b	Source Input Picture (encoder)	8-bit uncompressed data	0101b	Reconstructed Scaled Reference Picture	8-bit data
		Value	Name	Description																			
0000b		Reserved																					
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0011b	Reserved																						
0100b	Source Input Picture (encoder)	8-bit uncompressed data																					
0101b	Reconstructed Scaled Reference Picture	8-bit data																					
2	31:18	<b>Height</b> Format: U14-1 Height This field specifies the height of the Picture in units of pixels/residuals. For PLANAR surface formats, this field indicates the height of the Y (luma) plane. Note : Gen7 Video Codecs must program less than and equal to 4K.(In future, it will be ideal to have this field define in a WORD boundary.)AVC - multiple of 2 MB rows for field pictureVC1 - multiple of 4 pixels for field pictureMPEG2 - multiple of 2 MB rows for field picJPEG - multiple of integral MCU (8 or 16 pixels) per picture																					
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[0,16383]</td> <td></td> <td>representing heights [1,16384]</td> </tr> </tbody> </table>	Value	Name	Description	[0,16383]		representing heights [1,16384]															
	Value	Name	Description																				
[0,16383]		representing heights [1,16384]																					
		<p style="text-align: center;"><b>Programming Notes</b></p> <ul style="list-style-type: none"> <li>For AVC : For frame picture is a multiple of 16; for field picture is a multiple of 32</li> <li>For VC1 : For progressive frames, the frame height and frame width is a multiple of 2 pixels. For interlaced frames, the frame height shall be a multiple of 4 pixels, and its width is a multiple of 2 pixels, based on a PLANAR_420 surface.</li> </ul>																					
	17:4	<b>Width</b> Format: U14-1 Width This field specifies the width of the Picture in units of pixels/residuals. For PLANAR surface formats, this field indicates the width of the Y (luma) plane.																					
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> </tbody> </table>	Value	Name	Description																		
Value	Name	Description																					

<b>MFX_SURFACE_STATE</b>			
	[0,16383]	representing widths [1,16384]	
	<b>Programming Notes</b>		
	<ul style="list-style-type: none"> <li>The Width specified by this field multiplied by the pixel size in bytes must be less than or equal to the surface pitch (specified in bytes via the Surface Pitch field).</li> <li>Width (field value + 1) must be a multiple of 2 for PLANAR_420</li> <li>MFX HW does not use this field, the picture width is read from IMG State instead, because this field may not equal to the actual picture width. This field is used by the KMD to allocate surface in GTT.</li> </ul>		
3:2	<b>Reserved</b>		
	Format:	MBZ	
1:0	<b>Cr(V)/Cb(U) Pixel Offset V Direction</b>		
	Project:	All	
	Format:	U0.2 exactly as shown in the original spec	
	Specifies the distance to the U/V values with respect to the even numbered Y channels in the V direction		
	<b>Programming Notes</b>		
	This field is ignored for all formats except PLANAR_420_8		
3	31:28	<b>Surface Format</b>	
	Format:	U4	
	Specifies the format of the surface. All of the Y and G channels will use table 0 and all of the Cr/Cb/R/B channels will use table 1.Usage: For 420 planar YUV surface, use 4; for monochrome surfaces, use 12. For monochrome surfaces, hardware ignores control fields for Chroma planes.This field must be set to 4 - PLANAR_420_8, or 12 - Y8_UNORMNot used for MFX, and is ignored. But for JPEG decoding, this field should be programmed to the same format as JPEG_PIC_STATE. For video codec, it should set to 4 always.		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0	YCRCB_NORMAL	
	1	YCRCB_SWAPUVY	
	2	YCRCB_SWAPUV	
	3	YCRCB_SWAPY	
	4	PLANAR_420_8	(NV12, IMC1,2,3,4, YV12)
	5	PLANAR_411_8	Deinterlace Only
	6	PLANAR_422_8	Deinterlace Only
	7	STMM_DN_STATISTICS	Deinterlace Only
	8	R10G10B10A2_UNORM	Sample_8x8 Only
	9	R8G8B8A8_UNORM	Sample_8x8 Only
	10	R8B8_UNORM (CrCb	Sample_8x8 Only

<b>MFX_SURFACE_STATE</b>			
	11	R8_UNORM (Cr/Cb)	Sample_8x8 Only
	12	Y8_UNORM	Sample_8x8 Only
27	<b>Interleave Chroma</b>		
	Format:		Enable
	This field indicates that the chroma fields are interleaved in a single plane rather than stored as two separate planes. This field is only used for PLANAR surface formats. For AVC/VC1/MPEG VLD and IT modes : set to Enable to support interleave U/V only. For JPEG : set to Disable for all formats (including 4:2:0) - because JPEG does not support NV12. (This field is needed only if JPEG will support NV12; otherwise is ignored.)		
	<b>Value</b>		<b>Name</b>
	1		Enable
	0		Disable
26:20	<b>Reserved</b>		
	Format:		MBZ
19:3	<b>Surface Pitch</b>		
	Format:	U17-1 pitch in Bytes	
	This field specifies the surface pitch in (#Bytes).		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	[0,2047]		to [1B, 2048B]
	<b>Programming Notes</b>		
	For tiled surfaces, the pitch must be a multiple of the tile width (i.e.128 bytes aligned). If Half Pitch for Chroma is set, this field must be a multiple of two tile widths for tiled surfaces, or a multiple of 2 bytes for linear surfaces. For Y-tiled surfaces: Range = [127, 524287] to [128B,256KB] = [1 tile, 2048 tiles]		
2	<b>Half Pitch for Chroma</b>		
	Format:		Enable
	(This field must be set to Disable) This field indicates that the chroma plane(s) will use a pitch equal to half the value specified in the Surface Pitch field. This field is only used for PLANAR surface formats. This field is ignored by MFX (unless we support YV12)		
1	<b>Tiled Surface</b>		
	Format:		Boolean
	(This field must be set to TRUE: Tiled) This field specifies whether the surface is tiled. This field is ignored by MFX		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0	False	Linear
	1	True	Tiled

<b>MFX_SURFACE_STATE</b>																						
	<table border="1" style="width: 100%;"> <tr> <th colspan="2" style="text-align: center;">Programming Notes</th> </tr> <tr> <td colspan="2">Linear surfaces can be mapped to Main Memory (uncached) or System Memory (cacheable, snooped). Tiled surfaces can only be mapped to Main Memory. The corresponding cache(s) must be invalidated before a previously accessed surface is accessed again with an altered state of this bit.</td> </tr> </table>	Programming Notes		Linear surfaces can be mapped to Main Memory (uncached) or System Memory (cacheable, snooped). Tiled surfaces can only be mapped to Main Memory. The corresponding cache(s) must be invalidated before a previously accessed surface is accessed again with an altered state of this bit.																		
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<b>MFX_SURFACE_STATE</b>	
	multiple MBs. For JPEG, this field must be a multiple of 16 pixels.
5	31:29 <b>Reserved</b>
	28:16 <b>X Offset for V(Cr)</b>
	Format: U13 Offset in Pixels
	<p>This field must be zero for NV12 and IMC 1 and 3</p> <p>This field specifies the horizontal offset in pixels from the Surface Base Address to the start (origin) of the V(Cr) plane. This field is only used for PLANAR surface formats with Interleave Chroma disabled.</p>
	<p style="text-align: center;"><b>Programming Notes</b></p> <p>For PLANAR_420 and PLANAR_422 surface formats, this field must indicate an even number of pixels.</p>
15:0	<b>Y Offset for V(Cr)</b>
	Format: U16 Row Offset in Pixels
	<p>This field specifies the vertical offset in rows from the Surface Base Address to the start (origin) of the V(Cr) plane. This field is only used for PLANAR surface formats with Interleave Chroma disabled. This field is ignored by all video codec, only used by JPEG.</p>
	<p style="text-align: center;"><b>Programming Notes</b></p> <p>For PLANAR_420 surface formats, this field must be multiple of 16 pixels - i.e. multiple MBs. For JPEG, this field must be a multiple of 16 pixels.</p>

## MFX\_VC1\_DIRECTMODE\_STATE

MFX_VC1_DIRECTMODE_STATE			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
Exists If:	//VC1 decoding in VLD modes		
<p>This is a picture level command and should be issued only once, even for a multi-slices picture. There is only one DMV buffer for read (when processing a B-picture) and one for write (when processing a P-Picture). Each DMV record is 64 bits per MB, to store the top and bottom field MVs (32-bit MV<sub>x,y</sub> each).</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h MFX_VC1_DIRECTMODE_STATE
		Format:	OpCode
	26:24	<b>Media Command Opcode</b>	
		Default Value:	2h VC1_COMMON
		Format:	OpCode
	23:21	<b>SubOpcode A</b>	
Default Value:		0h	
Format:		OpCode	
20:16	<b>SubOpcode B</b>		
	Default Value:	2h	
	Format:	OpCode	
15:12	<b>Reserved</b>		
11:0	<b>DWord Length</b>		
	Default Value:	0005h Excludes DWord (0,1)	
	Project:	All	
	Format:	=n Total Length - 2	
1	31:6	<p><b>Direct MV Write Buffer Base Address for the Current Picture</b></p> <p>This field provides the base address of the DMV write buffer to store the motion vectors decoded in the current picture. It is a private buffer used by the MPR hardware only. Its content is not accessed by software. This buffer must be 64-byte cacheline aligned. The write buffer size is 557,056 bytes for 1 frame. Scalable with frame height, but do not scale with frame width as the hardware assumes frame width (in MBs) fixed at 128 (smallest power of 2 value larger than 120 - 1920x1088 screen resolution). This field is only valid for a P picture</p>	

<b>MFX_VC1_DIRECTMODE_STATE</b>											
	5:0	<b>Reserved</b>									
		Project: CHV, BSW									
		Format: MBZ									
2 <b>Project:</b> CHV, BSW	31:16	<b>Reserved</b>									
		Project: CHV, BSW									
		Format: MBZ									
	15:0	<b>Direct MV Write Buffer Base Address for the Current Picture [47:32]</b>									
		Project: CHV, BSW This field is for the upper range of Direct MV Write Buffer Base Address for the Current Picture. This field is used for 48-bit addressing.									
3 <b>Project:</b> CHV, BSW	31:15	<b>Reserved</b>									
		Project: CHV, BSW									
		Format: MBZ									
	14:13	<b>Reserved</b>									
	12:11	<b>Reserved</b>									
	10:9	<b>Reserved</b>									
	8:7	<b>Direct MV Write Buffer Base Address for the Current Picture - Arbitration Priority Control</b>									
		Project: CHV, BSW									
		Format: U2									
		This field controls the priority of arbitration used in the GAC/GAM pipeline for this surface.									
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00b	Highest priority										
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6:5	<b>Memory Type: LLC/eLLC Cacheability Control (LeLLCCC) for Direct MV Write Buffer for the Current Picture</b>										
	Project: CHV, BSW										
	This is the field used in GT interface block to determine what type of access need to be generated to uncore. For the cases where the LeLLCCC is set, cacheable transaction are generated to enable LLC usage for particular stream.										
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<b>MFX_VC1_DIRECTMODE_STATE</b>																
	4:3	<p><b>Target Cache (TC) for Direct MV Write Buffer for the Current Picture</b></p> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This field allows the choice of LLC vs eLLC for caching</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>eLLC Only - not snooped in GT</td> </tr> <tr> <td>01b</td> <td>LLC Only</td> </tr> <tr> <td>10b</td> <td>LLC/eLLC Allowed</td> </tr> <tr> <td>11b</td> <td>L3, LLC, eLLC Allowed</td> </tr> </tbody> </table>	Project:	CHV, BSW	Value	Name	00b	eLLC Only - not snooped in GT	01b	LLC Only	10b	LLC/eLLC Allowed	11b	L3, LLC, eLLC Allowed		
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	2	<b>Reserved</b>														
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4	31:6	<p><b>Direct MV Read Buffer Base Address for the Reference Picture</b></p> <p>This field provides the base address of the DMV buffer for reference picture. It is a private buffer used by the MPR hardware only. Its content is not accessed by software. All these buffers must be 64-byte cacheline aligned. This field is only valid for a B picture.</p>														
	5:0	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ										
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<b>MFX_VC1_DIRECTMODE_STATE</b>															
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Project:	CHV, BSW														

<b>MFX_VC1_DIRECTMODE_STATE</b>															
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00b	Poor chance of generating hits.														

## MFX\_VC1\_PRED\_PIPE\_STATE

<b>MFX_VC1_PRED_PIPE_STATE</b>			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>This command is used to set the operating states of the MFD Engine beyond the BSD unit. It is used with both VC1 Long and Short format. Driver is responsible to take the intensity compensation enable signal, the LumScale and the LumShift provided from the DXVA2 VC1 interface, and maintain a history of these values for reference pictures. Together with these three parameters specified for the current picture being decoded, driver will derive and supply the above sets of LumScaleX, LumShiftX and intensity compensation enable (single or double, forward or backward) signals. H/W is responsible to take these state values, and use them to build the lookup table (including the derivation of iScale and iShift) for remapping the reference frame pixels, as well as performing the actual pixel remapping calculations/process.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h MFX_VC1_PRED_PIPE_STATE
		Format:	OpCode
	26:24	<b>Media Command Opcode</b>	
		Default Value:	2h VC1_COMMON
		Format:	OpCode
	23:21	<b>SubOpcode A</b>	
		Default Value:	0h
		Format:	OpCode
	20:16	<b>SubOpcode B</b>	
		Default Value:	1h
Format:		OpCode	
15:12	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
11:0	<b>DWord Length</b>		
	Default Value:	0004h Excludes DWord (0,1)	
	Project:	All	
	Format:	=n Total Length - 2	
1	31:16	<b>Reserved</b>	

<b>MFX_VC1_PRED_PIPE_STATE</b>							
2	<table border="1"> <tr> <td style="width: 50px;">15:14</td> <td><b>vin_intensitycomp_Double_FWDen</b></td> </tr> <tr> <td colspan="2">Format: U2</td> </tr> <tr> <td colspan="2">for forward reference picture only, to enable top or/and bottom of the reference field enable for single compensation. For frame, may only need one bit. This field is maintained and provided by driver for both long and short VC1 interface format. And is derived from the intensity compensation enable flag, wBitstreamPCElement and wBitstreamFcodes parameters provided by the DXVA2 VC1 interface to the driver for each current picture.</td> </tr> </table>	15:14	<b>vin_intensitycomp_Double_FWDen</b>	Format: U2		for forward reference picture only, to enable top or/and bottom of the reference field enable for single compensation. For frame, may only need one bit. This field is maintained and provided by driver for both long and short VC1 interface format. And is derived from the intensity compensation enable flag, wBitstreamPCElement and wBitstreamFcodes parameters provided by the DXVA2 VC1 interface to the driver for each current picture.	
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<b>MFX_VC1_PRED_PIPE_STATE</b>				
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<b>MFX_VC1_PRED_PIPE_STATE</b>	
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## MFX\_VP8\_BSP\_BUF\_BASE\_ADDR\_STATE

MFX_VP8_BSP_BUF_BASE_ADDR_STATE											
Project:	CHV, BSW										
Source:	VideoCS										
Length Bias:	2										
DWord	Bit	Description									
0	31:29	<b>Command Type</b>									
		Default Value:	3h PARALLEL_VIDEO_PIPE								
		Format:	OpCode								
	28:27	<b>Pipeline</b>									
		Default Value:	2h Video Codec								
		Format:	OpCode								
	26:24	<b>Media Command OpCode</b>									
Default Value:		4h VP8									
Format:		OpCode									
23:21	<b>Sub Opcode A</b>										
	Default Value:	2h VP8 Common									
	Format:	OpCode									
20:16	<b>Sub Opcode B</b>										
	Default Value:	3h MFX_VP8_BSP_BUF_BASE_ADDR_STATE									
	Format:	OpCode									
15:12	<b>Reserved</b>										
	Format:	MBZ									
11:0	<b>DWord Length</b>	Format:	=n								
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000h</td> <td>Excludes DWord (0,1) <b>[Default]</b></td> <td>A special case to provide a dummy image state for stitch mode operation. In this case, fields in DW1 which is part of the dummy image state command are ignored by hardware."</td> </tr> <tr> <td>008h</td> <td></td> <td>Used for normal encode mode</td> </tr> </tbody> </table>		Value	Name	Description	000h	Excludes DWord (0,1) <b>[Default]</b>	A special case to provide a dummy image state for stitch mode operation. In this case, fields in DW1 which is part of the dummy image state command are ignored by hardware."	008h	
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008h		Used for normal encode mode									
1	31:6	<b>Frame Header Base Addr</b>									
		Format:	StreamInAddress[31:6] 64 bytes aligned buffer in linear format.								
		48-bit Abs. Address StreamIn Surface									
		<b>Note:</b> The format is linear vs. tile for better performance.									

<b>MFX_VP8_BSP_BUF_BASE_ADDR_STATE</b>																
	5:0	<b>Reserved</b>														
		Format: MBZ														
2	31:16	<b>Reserved</b>														
		Format: MBZ														
	15:0	<b>Frame Header Base Addr - Upper Range</b>														
3	31:9	<b>Reserved</b>														
		Format: MBZ														
	8:7	<b>Frame Header Base Addr - Arbitration Priority Control</b> This field controls the priority of arbitration used in the GAC/GAM pipeline for this surface.														
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Highest priority</td> </tr> <tr> <td>01b</td> <td>Second highest priority</td> </tr> <tr> <td>10b</td> <td>Third highest priority</td> </tr> <tr> <td>11b</td> <td>Lowest priority</td> </tr> </tbody> </table>	Value	Name	00b	Highest priority	01b	Second highest priority	10b	Third highest priority	11b	Lowest priority				
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	01b	Second highest priority														
	10b	Third highest priority														
	11b	Lowest priority														
	6:5	<b>for FrameHeaderBaseAddr - LLC/eLLC Cacheability Control (LeLLCCC)</b> This is the field used in GT interface block to determine what type of access need to be generated to uncore. For the cases where the LeLLCCC is set, cacheable transaction are generated to enable LLC usage for particular stream.														
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Cacheable</td> <td>Use Cacheability Controls from page table</td> </tr> <tr> <td>01b</td> <td>UC</td> <td>Uncacheable - non-cacheable</td> </tr> <tr> <td>10b</td> <td>WT</td> <td>Writethrough</td> </tr> <tr> <td>11b</td> <td>WB</td> <td>Writeback</td> </tr> </tbody> </table>	Value	Name	Description	00b	Cacheable	Use Cacheability Controls from page table	01b	UC	Uncacheable - non-cacheable	10b	WT	Writethrough	11b	WB	Writeback
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01b	UC	Uncacheable - non-cacheable														
10b	WT	Writethrough														
11b	WB	Writeback														
4:3	<b>Frame Header Base Addr - Target Cache (TC)</b> This field allows the choice of LLC vs eLLC for caching															
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>eLLC Only - not snooped in GT</td> </tr> <tr> <td>01b</td> <td>LLC Only</td> </tr> <tr> <td>10b</td> <td>LLC/eLLC Allowed</td> </tr> <tr> <td>11b</td> <td>L3, LLC, eLLC Allowed</td> </tr> </tbody> </table>	Value	Name	00b	eLLC Only - not snooped in GT	01b	LLC Only	10b	LLC/eLLC Allowed	11b	L3, LLC, eLLC Allowed					
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01b	LLC Only															
10b	LLC/eLLC Allowed															
11b	L3, LLC, eLLC Allowed															
2	<b>Reserved</b>															
1:0	<b>Frame Header Base Addr - Age for QUADLRU (AGE)</b> This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches.															
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<b>MFX_VP8_BSP_BUF_BASE_ADDR_STATE</b>																
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<b>MFX_VP8_BSP_BUF_BASE_ADDR_STATE</b>		
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7	31:0	<b>Intermediate Buffer Partition-1 Offset</b> Format: <span style="float: right;">U32</span>
<b>Programming Notes</b>		
All <b>Intermediate Buffer Partition-[i] Offset</b> (i = 1 to 8) and <b>Intermediate Buffer Max Size</b> need to be cacheline aligned (64Byte aligned).		
8	31:0	<b>Intermediate Buffer Partition-2 Offset</b> Format: <span style="float: right;">U32</span>
9	31:0	<b>Intermediate Buffer Partition-3 Offset</b> Format: <span style="float: right;">U32</span>
10	31:0	<b>Intermediate Buffer Partition-4 Offset</b> Format: <span style="float: right;">U32</span>
11	31:0	<b>Intermediate Buffer Partition-5 Offset</b> Format: <span style="float: right;">U32</span>
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15	31:0	<b>Intermediate Buffer Max Size</b> Format: <span style="float: right;">U32</span>
16	31:6	<b>Final Frame Base Addr</b> Format: <span style="float: right;">StreamInAddress[31:6] 64 bytes aligned buffer in linear format</span>



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	5:0	<b>FinalFrameByteOffset</b> Format: _____ U6 Specify byte offset within a 64-byte cacheline where the bitstream should be inserted at.											
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## MFX\_VP8\_BSP\_BUF\_BASE\_ADDR\_STATE

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	6:5	<p><b>Memory Type: LLC/eLLC Cacheability Control (LeLLCCC) for CoeffProbs StreamIn Surface</b></p> <p>This is the field used in GT interface block to determine what type of access need to be generated to uncore. For the cases where the LeLLCCC is set, cacheable transaction are generated to enable LLC usage for particular stream.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Use Cacheability Controls from page table</td> <td></td> </tr> <tr> <td>01b</td> <td>UC</td> <td>Uncacheable - non-cacheable</td> </tr> <tr> <td>10b</td> <td>WT</td> <td>Writethrough</td> </tr> </tbody> </table>	Value	Name	Description	00b	Use Cacheability Controls from page table		01b	UC	Uncacheable - non-cacheable	10b	WT	Writethrough			
Value	Name	Description															
00b	Use Cacheability Controls from page table																
01b	UC	Uncacheable - non-cacheable															
10b	WT	Writethrough															

<b>MFX_VP8_BSP_BUF_BASE_ADDR_STATE</b>			
	11b	WB Writeback	
4:3	<b>Token Statistics Surface - Target Cache (TC)</b> This field allows the choice of LLC vs eLLC for caching.		
	<b>Value</b>	<b>Name</b>	
	00b	eLLC Only - not snooped in GT	
	01b	LLC Only	
	10b	LLC/eLLC Allowed	
	11b	L3, LLC, eLLC Allowed	
2	<b>Reserved</b>		
1:0	<b>Token Statistics Surface - Age for QUADLRU (AGE)</b> This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches.		
	<b>Value</b>	<b>Name</b>	
	11b	Good chance of generating hits.	
	10b	Next good chance of generating hits	
	01b	Decent chance of generating hits	
	00b	Poor chance of generating hits	
29	31:6	<b>MPC RowStore Surface Address Low</b> Format: GraphicsAddress[31:6] 48-bit Abs. Address StreamIn/StreamOut Surface. <b>Note:</b> The format is linear vs. tile for better performance.	
	5:4	<b>MPC RowStore Base Addr - Arbitration Priority Control</b> <b>This field controls the priority of arbitration used in the GAC/GAM pipeline for this surface.</b>	
		<b>Value</b>	<b>Name</b>
		00b	Highest priority
01b		Second highest priority	
10b		Third highest priority	
	11b	Lowest priority	
3	<b>Reserved</b>		
2	<b>MPC RowStore Surface Graphics Data Type (GFDT)</b> Format: U1 <b>This field contains the GFDT bit for this surface when writes occur. GFDT can also be set by the GTT. The effective GFDT is the logical OR of this field with the GFDT from the GTT entry. This field is ignored for reads.</b>		

<b>MFX_VP8_BSP_BUF_BASE_ADDR_STATE</b>																	
	1:0	<p><b>MPC RowStore Surface - Cacheability Control</b>  <b>This field controls cacheability in the mid-level cache (MLC) and last-level cache (LLC).</b></p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>GTT Entry</td> <td>Use cacheability control bits from GTT entry</td> </tr> <tr> <td>01b</td> <td>Not LLC or MLC</td> <td>Data is not cached in LLC or MLC</td> </tr> <tr> <td>10b</td> <td>LLC but not MLC</td> <td>Data is cached in LLC but not MLC</td> </tr> <tr> <td>11b</td> <td>Both LLC and MLC</td> <td>Data is cached in both LLC and MLC</td> </tr> </tbody> </table>	Value	Name	Description	00b	GTT Entry	Use cacheability control bits from GTT entry	01b	Not LLC or MLC	Data is not cached in LLC or MLC	10b	LLC but not MLC	Data is cached in LLC but not MLC	11b	Both LLC and MLC	Data is cached in both LLC and MLC
	Value	Name	Description														
	00b	GTT Entry	Use cacheability control bits from GTT entry														
	01b	Not LLC or MLC	Data is not cached in LLC or MLC														
	10b	LLC but not MLC	Data is cached in LLC but not MLC														
11b	Both LLC and MLC	Data is cached in both LLC and MLC															
30	31:16	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ													
Format:	MBZ																
	15:0	<p><b>MPC RowStore Surface Address High</b></p> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>This field is for the upper range of Token Statistics Address.</p>	Format:	GraphicsAddress[47:32]													
Format:	GraphicsAddress[47:32]																
31	31:9	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ													
Format:	MBZ																
	8:7	<p><b>MPC RowStore - Arbitration Priority Control</b>  <b>This field controls the priority of arbitration used in the GAC/GAM pipeline for this surface.</b></p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Highest Priority</td> </tr> <tr> <td>01b</td> <td>Second highest Priority</td> </tr> <tr> <td>10b</td> <td>Third highest Priority</td> </tr> <tr> <td>11b</td> <td>Lowest Priority</td> </tr> </tbody> </table>	Value	Name	00b	Highest Priority	01b	Second highest Priority	10b	Third highest Priority	11b	Lowest Priority					
Value	Name																
00b	Highest Priority																
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	6:5	<p><b>MPC RowStore - Memory Type: LLC/eLLC Cacheability Control</b>  <b>This field controls the priority of arbitration used in the GAC/GAM pipeline for this surface.</b></p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Use Cacheability Controls from page table</td> <td></td> </tr> <tr> <td>01b</td> <td>UC</td> <td>Uncacheable - non-cacheable</td> </tr> <tr> <td>10b</td> <td>WT</td> <td>Writethrough</td> </tr> <tr> <td>11b</td> <td>WB</td> <td>Writeback</td> </tr> </tbody> </table>	Value	Name	Description	00b	Use Cacheability Controls from page table		01b	UC	Uncacheable - non-cacheable	10b	WT	Writethrough	11b	WB	Writeback
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01b	UC	Uncacheable - non-cacheable															
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11b	WB	Writeback															
	4:3	<p><b>MPC RowStore - Target Cache</b></p> <table border="1"> <tr> <td>Format:</td> <td>U2</td> </tr> </table> <p><b>This field controls the priority of arbitration used in the GAC/GAM pipeline for this surface.</b></p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>eLLC Only</td> </tr> <tr> <td>01b</td> <td>LLC Only</td> </tr> <tr> <td>10b</td> <td>LLC/eLLC Allowed</td> </tr> <tr> <td>11b</td> <td>L3, LLC, eLLC Allowed</td> </tr> </tbody> </table>	Format:	U2	Value	Name	00b	eLLC Only	01b	LLC Only	10b	LLC/eLLC Allowed	11b	L3, LLC, eLLC Allowed			
Format:	U2																
Value	Name																
00b	eLLC Only																
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<b>MFX_VP8_BSP_BUF_BASE_ADDR_STATE</b>											
2	<b>Reserved</b>										
1:0	<p><b>MPC RowStore Surface - Age for QUADLRU (AGE)</b>                      This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">11b</td> <td>Good chance of generating hits.</td> </tr> <tr> <td style="text-align: center;">10b</td> <td>Next good chance of generating hits.</td> </tr> <tr> <td style="text-align: center;">01b</td> <td>Decent chance of generating hits.</td> </tr> <tr> <td style="text-align: center;">00b</td> <td>Poor chance of generating hits.</td> </tr> </tbody> </table>	Value	Name	11b	Good chance of generating hits.	10b	Next good chance of generating hits.	01b	Decent chance of generating hits.	00b	Poor chance of generating hits.
Value	Name										
11b	Good chance of generating hits.										
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00b	Poor chance of generating hits.										

## MFX\_VP8\_Encoder\_CFG

<b>MFX_VP8_Encoder_CFG</b>				
Project:	CHV, BSW			
Source:	VideoCS			
Length Bias:	2			
<p>This must be the very first command to issue after the surface state, the pipe select and base address setting commands and must be issued before MFX_VP8_PIC_STATE.</p>				
DWord	Bit	Description		
0	31:29	<b>Command Type</b>		
		Default Value:	3h PARALLEL_VIDEO_PIPE	
		Format:	OpCode	
	28:27	<b>Pipeline</b>		
		Default Value:	2h Video Codec	
		Format:	OpCode	
	26:24	<b>Media Command OpCode</b>		
		Default Value:	4h VP8	
		Format:	OpCode	
	23:21	<b>Sub OpCode A</b>		
		Default Value:	2h VP8 Common	
		Format:	OpCode	
	20:16	<b>Sub OpCode B</b>		
		Default Value:	1h MFX_VP8_ENCODER_CFG	
Format:		OpCode		
15:12	<b>Reserved</b>			
	Format:	MBZ		
11:0	<b>DWord Length</b>			
	Format:	=n		
	Value	Name	Description	Project
	000h	Excludes DWord (0,1) <b>[Default]</b>	A special case to provide a dummy image state for stitch mode operation. In this case, fields in DW1 which is part of the dummy image state command are ignored by hardware."	
01Ch		Used for normal encode mode	CHV, BSW	

<b>MFX_VP8_Encoder_CFG</b>											
1	31:11	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ							
	Format:	MBZ									
	10	<b>VBSPunitPowerClock Gating Disable</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> VBSPunit Power Clock Gating Disable.	Project:	CHV, BSW	Format:	U1					
	Project:	CHV, BSW									
	Format:	U1									
	9	<b>Compressed Bitstream Output Disable</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> Disable Compressed Bitstream Output. <b>(Both Final Bitstream and Intermediate bit buffer)</b>	Project:	CHV, BSW	Format:	U1					
	Project:	CHV, BSW									
	Format:	U1									
	7	<b>Per Segment Delta Qindex / LoopFilter Disable</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>+, CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> Disable Per Segment Delta Qindex / Loop Filter in Rate Control.	Project:	+, CHV, BSW	Format:	U1					
	Project:	+, CHV, BSW									
Format:	U1										
6	<b>Rate Control Initial Pass</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">1</td> <td>Initial pass</td> </tr> <tr> <td style="text-align: center;">0</td> <td>Subsequence Pass(es)</td> </tr> </tbody> </table>	Project:	CHV, BSW	Format:	U1	Value	Name	1	Initial pass	0	Subsequence Pass(es)
Project:	CHV, BSW										
Format:	U1										
Value	Name										
1	Initial pass										
0	Subsequence Pass(es)										
5	<b>Skip Final Bitstream when Over / Under flow</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>U1</td> </tr> </table> Skip Final Bitstream conditionally on Over/Under flow in rate control and intermediate Bit Buffer Overrun.	Format:	U1								
Format:	U1										
4	<b>Update Segment Feature Data Flag</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Exists If:</td> <td>//VP8 Encoder</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> Enable for Frame Header per Segment Quantizer / LoopFilter Update	Exists If:	//VP8 Encoder	Format:	U1						
Exists If:	//VP8 Encoder										
Format:	U1										
3	<b>Bitstream Statistics Output Enable</b> Enable Bitstream Statistics Output at Memory Surface in MFX_VBSP_BUF_ADDR_STATE DW[26:28]										
2	<b>Token Statistics Output Enable</b> Enable Token Statistics Output at Memory Surface in MFX_VBSP_BUF_ADDR_STATE DW[26:28]										
1	<b>Final Bitstream Output Disable</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>U1</td> </tr> </table> Disable Final Bitstream Output.	Format:	U1								
Format:	U1										

<b>MFX_VP8_Encoder_CFG</b>						
2	0	<p><b>Performance Counter Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U1</td> </tr> </table> <p>Enable Performance Counter in Streamout.</p>	Format:	U1		
	Format:	U1				
	31:8	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">MBZ</td> </tr> </table>	Format:	MBZ		
	Format:	MBZ				
	7	<p><b>Qindex_Clamp_High_mask for overflow</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td style="width: 50%;">CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>If current frame is overflow and this mask is set, it would mask out MFX_VP8_Img_Status register. DW1.bit1. In another word, subsequent passes would be skipped.</p>	Project:	CHV, BSW	Format:	U1
	Project:	CHV, BSW				
	Format:	U1				
	6	<p><b>Qindex_Clamp_High_mask for underflow</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td style="width: 50%;">CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>If current frame is underflow and this mask is set, it would mask out MFX_VP8_Img_Status register. DW1.bit0. In another word, subsequent passes would be skipped</p>	Project:	CHV, BSW	Format:	U1
	Project:	CHV, BSW				
	Format:	U1				
5	<p><b>Final Bistream Buffer Overrun Enable Mask</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td style="width: 50%;">CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>Enable Final Bitstream Buffer Overrun detection feature.</p>	Project:	CHV, BSW	Format:	U1	
Project:	CHV, BSW					
Format:	U1					
4	<p><b>Intermediate Bit Buffer Overrun Enable Mask</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U1</td> </tr> </table> <p>Enable Intermediate Bit Buffer Overrun detection feature.</p>	Format:	U1			
Format:	U1					
3	<p><b>Max Intra MB Bit Count Check Enable Mask</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U1</td> </tr> </table> <p>Enable Max. Intra MB bit count check in Streamout.</p>	Format:	U1			
Format:	U1					
2	<p><b>Max Inter MB Bit Count Check Enable Mask</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U1</td> </tr> </table> <p>Enable Max. Inter MB bit count check in Streamout.</p>	Format:	U1			
Format:	U1					
1	<p><b>Min Frame Bit Count Rate Control Enable Mask</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U1</td> </tr> </table> <p>Enable Min. Frame Rate Control. This is a mask bit controlling if the condition of frame level bit count is less than or equal to FrameBitRateMin.</p>	Format:	U1			
Format:	U1					

<b>MFX_VP8_Encoder_CFG</b>											
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td></td> <td>If (Total Frame Level Bit Counter) = &lt; (Frame Bit Rate Minimum limit) Set bit[0] and bit[1] of MFX_VP8_IMAGE_STATUS Control Register.</td> </tr> <tr> <td>0</td> <td></td> <td>Do not update bit[0] of MFX_VP8_IMAGE_STATUS Control Register.</td> </tr> </tbody> </table>	Value	Name	Description	1		If (Total Frame Level Bit Counter) = < (Frame Bit Rate Minimum limit) Set bit[0] and bit[1] of MFX_VP8_IMAGE_STATUS Control Register.	0		Do not update bit[0] of MFX_VP8_IMAGE_STATUS Control Register.
Value	Name	Description									
1		If (Total Frame Level Bit Counter) = < (Frame Bit Rate Minimum limit) Set bit[0] and bit[1] of MFX_VP8_IMAGE_STATUS Control Register.									
0		Do not update bit[0] of MFX_VP8_IMAGE_STATUS Control Register.									
	0	<p><b>Max Frame bit count Rate Control Enable Mask</b></p> <p>Format: <span style="float: right;">U1</span></p> <p>Enable Max. Frame Rate Control. This is a mask bit controlling if the condition of frame level bit count is greater than or equal to FrameBitRateMax.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td></td> <td>If (Total Frame Level Bit Counter) &gt;= (Frame Bit Rate Maximum Limit) Set bit[0] and bit[1] of MFX_VP8_IMAGE_STATUS control register.</td> </tr> <tr> <td>0</td> <td></td> <td>Do not update bit[0] of MFX_VP8_IMAGE_STATUS control register.</td> </tr> </tbody> </table>	Value	Name	Description	1		If (Total Frame Level Bit Counter) >= (Frame Bit Rate Maximum Limit) Set bit[0] and bit[1] of MFX_VP8_IMAGE_STATUS control register.	0		Do not update bit[0] of MFX_VP8_IMAGE_STATUS control register.
Value	Name	Description									
1		If (Total Frame Level Bit Counter) >= (Frame Bit Rate Maximum Limit) Set bit[0] and bit[1] of MFX_VP8_IMAGE_STATUS control register.									
0		Do not update bit[0] of MFX_VP8_IMAGE_STATUS control register.									
3	31:28	<b>Reserved</b>									
	27:16	<p><b>Max Intra MB Bit Count Limit</b></p> <p>Format: <span style="float: right;">U12</span></p> <p>12-bit bit count for Max Intra MB Limit.</p>									
	15:12	<p><b>Reserved</b></p> <p>Format: <span style="float: right;">MBZ</span></p>									
	11:0	<p><b>Max Inter MB bit count</b></p> <p>Format: <span style="float: right;">U12</span></p> <p>12-bit bit count for Max Inter MB Limit.</p>									
4	31	<p><b>Frame Bitrate Min Unit Mode</b></p> <p>Format: <span style="float: right;">U1</span></p> <p>This field is the Frame Bitrate Minimum Limit Units.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Compatibility Mode</td> <td>Frame BitRate Min Unit is in old mode <b>(128b/16Kb)</b></td> </tr> <tr> <td>1h</td> <td>New Mode</td> <td>Frame BitRate Min Unit is in new mode <b>(32byte/4Kb)</b></td> </tr> </tbody> </table>	Value	Name	Description	0h	Compatibility Mode	Frame BitRate Min Unit is in old mode <b>(128b/16Kb)</b>	1h	New Mode	Frame BitRate Min Unit is in new mode <b>(32byte/4Kb)</b>
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	30	<p><b>Frame Bit Rate Min Unit</b></p> <p>Format: <span style="float: right;">U1</span></p> <p><i>This field is Frame Bitrate Minimum Mode.</i></p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>32-B</td> </tr> <tr> <td>1</td> <td>4-KB</td> </tr> </tbody> </table>	Value	Name	0	32-B	1	4-KB			
Value	Name										
0	32-B										
1	4-KB										
29:16	<p><b>Frame Bit Rate Min</b></p> <p>Format: <span style="float: right;">U14</span></p> <p>If either BRC Underflow or overflow is enabled. Frame Bit Rate Min and Frame Bit Rate Max need to be programmed with unambiguous values</p>										

<b>MFX_VP8_Encoder_CFG</b>													
	15	<p><b>Frame Bitrate Max Unit Mode</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U1</td> </tr> </table> <p>This field is the Frame Bitrate Maximum Limit Units.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 30%;">Name</th> <th style="width: 55%;">Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Compatibility Mode</td> <td>Frame BitRate Max Unit is in old mode <b>(128b/16Kb)</b></td> </tr> <tr> <td>1h</td> <td>New Mode</td> <td>Frame BitRate Max Unit is in new mode <b>(32byte/4Kb)</b></td> </tr> </tbody> </table>	Format:	U1	Value	Name	Description	0h	Compatibility Mode	Frame BitRate Max Unit is in old mode <b>(128b/16Kb)</b>	1h	New Mode	Frame BitRate Max Unit is in new mode <b>(32byte/4Kb)</b>
	Format:	U1											
	Value	Name	Description										
	0h	Compatibility Mode	Frame BitRate Max Unit is in old mode <b>(128b/16Kb)</b>										
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14	<p><b>Frame Bit Rate Max Unit</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U1</td> </tr> </table> <p><i>This field is Frame Bitrate Maximum Mode</i></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 40%;">Value</th> <th style="width: 60%;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>32-B</td> </tr> <tr> <td style="text-align: center;">1</td> <td>4-KB</td> </tr> </tbody> </table>	Format:	U1	Value	Name	0	32-B	1	4-KB				
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Value	Name												
0	32-B												
1	4-KB												
13:0	<p><b>Frame Bit Rate Max</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U14</td> </tr> </table> <p>If either BRC Underflow or overflow is enabled. Frame Bit Rate Min and Frame Bit Rate Max need to be programmed with unambiguous values</p>	Format:	U14										
Format:	U14												
5	<p><b>31:24 Frame Delta QIndex Max[3]</b></p> <p>This field is the Frame level delta Qindex for total bit-count above FrameBitRateMax - First 1/8 Region.</p> <p>This field is used to calculate the suggested Frame Qindex into the MFX_VP8_IMAGE_STATUS control register when total bit count for the entire frame exceeds FrameBitRateMax but is within 1/8 of FrameBitRateMaxDelta above <b>FrameBitRateMax</b>; i.e., In the range of (FrameBitRateMax, (FrameBitRateMax + FrameBitRateMaxDelta » 3)].</p>												
	<p><b>23:16 Frame DeltaQ Index Max[2]</b></p> <p>This field is the Frame level delta Qindex for bit-count above FrameBitRateMax - Above 1/8 and Below 1/4.</p> <p>This field is used to calculate the suggested Frame Qindex into the MFX_VP8_IMAGE_STATUS control register when total bit count for the entire frame is between 1/8 and 1/4 of FrameBitRateMaxDelta above <b>FrameBitRateMax</b>; i.e., In the range of ((FrameBitRateMax + FrameBitRateMaxDelta » 3), (FrameBitRateMax+ FrameBitRateMaxDelta » 2)].</p>												
	<p><b>15:8 Frame Delta QIndex Max[1]</b></p> <p>This field is the Frame level delta QINDEX for bit-count above FrameBitRateMax - Above 1/4 and Below 1/2.</p> <p>This field is used to calculate the suggested Frame QINDEX into the MFX_VP8_IMAGE_STATUS control register when total bit count for the entire frame is between 1/4 and 1/2 of FrameBitRateMaxDelta above <b>FrameBitRateMax</b>; i.e., In the range of [(FrameBitRateMax+ FrameBitRateMaxDelta » 2), (FrameBitRateMax+ FrameBitRateMaxDelta » 1)].</p>												

<b>MFX_VP8_Encoder_CFG</b>			
	<p>7:0 <b>Frame Delta QIndex Max [0]</b>                      This field is the Frame level delta QINDEX for bit-count above FrameBitRateMax - Above 1/2. This field is used to calculate the suggested Frame QINDEX into the MFX_VP8_IMAGE_STATUS control register when total bit count for the entire frame is above FrameBitRateMax by more than half the distance of <b>FrameBitRateMax</b>; i.e., In the range of <math>[(\text{FrameBitRateMax} + \text{FrameBitRateMaxDelta} \gg 1), \infty (\text{Infinite})]</math>.</p>		
6	<p>31:24 <b>Frame Delta QIndex Min[3]</b>                      This field is the Frame level delta QINDEX for total bit-count below FrameBitRateMin - First 1/8 Region. This field is used to calculate the suggested Frame QINDEX into the MFX_VP8_IMAGE_STATUS control register when total bit count for the entire frame is less than FrameBitRateMin and greater than or equal to 1/8 the distance of FrameBitRateMinDelta from <b>FrameBitRateMin</b>; i.e., In the range of <math>[(\text{FrameBitRateMin} - \text{FrameBitRateMinDelta} \gg 3), \text{FrameBitRateMin}]</math>.</p>		
	<p>23:16 <b>Frame Delta QIndex Min[2]</b>                      This field is the Frame level delta QINDEX for bit-count below FrameBitRateMin - Below 1/ 8 and Above 1/4. This field is used to calculate the suggested Frame QINDEX into the MFX_VP8_IMAGE_STATUS control register when total bit count for the entire frame is between one-eighth and quarter the distance of FrameBitRateMinDelta from <b>FrameBitRateMin</b>; i.e., In the range of <math>[(\text{FrameBitRateMin} - \text{FrameBitRateMinDelta} \gg 2), (\text{FrameBitRateMin} - \text{FrameBitRateMinDelta} \gg 3)]</math>.</p>		
	<p>15:8 <b>Frame Delta QIndex Min[1]</b>                      This field is the Frame level delta QINDEX for bit-count below FrameBitRateMin- Below 1/4 and Above 1/2. This field is used to calculate the suggested Frame QINDEX into the MFX_VP8_IMAGE_STATUS control register when total bit count for the entire frame is between quarter and half the distance of FrameBitRateMinDelta from <b>FrameBitRateMin</b>; i.e., In the range of <math>[(\text{FrameBitRateMin} - \text{FrameBitRateMinDelta} \gg 1), (\text{FrameBitRateMin} - \text{FrameBitRateMinDelta} \gg 2)]</math>.</p>		
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7	<p>31:0 <b>Per Segment Frame Delta QIndex Max[1]</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table> <p>Reserved in CHV, BSW, Need to be programmed with same value as Segment0. Per Segment BRC is not validated in CHV, BSW FulSIM</p>	Project:	CHV, BSW
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<b>MFX_VP8_Encoder_CFG</b>				
9	31:0	<b>Per Segment Frame Delta QIndex Max[2]</b>		
		<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table> <p>Reserved in CHV, BSW, Need to be programmed with same value as Segment0. Per Segment BRC is not validated in CHV, BSW FulSIM</p>	Project:	CHV, BSW
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13	31:24	<b>Frame Delta Loop Filter Max[3]</b>		
		<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>U8</td> </tr> </table> <p>This field is the Frame level delta LoopFilter for total bit-count above FrameBitRateMax - First 1/8 region.</p> <p>This field is used to calculate the suggested Frame LoopFilter into the MFX_VP8_IMAGE_STATUS control register when total bit count for the entire frame exceeds FrameBitRateMax but is within 1/8 of FrameBitRateMaxDelta above FrameBitRateMax. i.e., in the range of (FrameBitRateMax, (FrameBitRateMax+ FrameBitRateMaxDelta » 3)].</p>	Format:	U8
	Format:	U8		
23:16	<b>Frame Delta Loop Filter Max[2]</b>			
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	15:8	<b>Frame Delta Loop Filter Max[1]</b>		
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<b>MFX_VP8_Encoder_CFG</b>			
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18	31:0	<p><b>Per Segment Frame Delta LoopFilter Min[2]</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Project:</td> <td style="width: 30%;">+, CHV, BSW</td> </tr> </table>	Project:	+, CHV, BSW						
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19	31:0	<p><b>Per Segment Frame Delta LoopFilter Max[3]</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Project:</td> <td style="width: 30%;">+, CHV, BSW</td> </tr> </table>	Project:	+, CHV, BSW						
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20	31:0	<p><b>Per Segment Frame Delta LoopFilter Min[3]</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Project:</td> <td style="width: 30%;">+, CHV, BSW</td> </tr> </table>	Project:	+, CHV, BSW						
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21	31	<p><b>Reserved</b></p>								
	30:16	<p><b>FrameBitRateMinDelta</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U15</td> </tr> </table> <p>This field is used to select the frame delta QINDEX when FrameBitRateMin Is exceeded. It shares the same FrameBitrateMinUnit.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 70%;">Description</th> </tr> </thead> <tbody> <tr> <td>[0-4095]</td> <td></td> <td>When FrameBitrateMinUnit is in Bytes, this range is in Bytes. When FrameBitrateMinUnit is in KB, this range is in KB units.</td> </tr> </tbody> </table>	Format:	U15	Value	Name	Description	[0-4095]		When FrameBitrateMinUnit is in Bytes, this range is in Bytes. When FrameBitrateMinUnit is in KB, this range is in KB units.
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22	31:24	<p><b>Reserved</b></p>								

<b>MFX_VP8_Encoder_CFG</b>											
23	23	<b>Show Frame</b>									
		Format: U1 VP8 Frame Tag, Show Frame Field									
22:20	22:20	<b>Bitstream Format Version</b>									
		Format: U3 VP8 Frame Tag, Verison Field									
19:18	19:18	<b>Reserved</b>									
		Format: MBZ									
17:16	17:16	<b>Min Frame WSize Unit</b>									
		Format: U2									
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Compatibility Mode</td> <td>MinFrameWSizeUnit is in old mode (128b/16Kb)</td> </tr> <tr> <td>1h</td> <td>New Mode</td> <td>MinFrameWSizeUnit is in new mode (32byte/4Kb)</td> </tr> </tbody> </table>	Value	Name	Description	0h	Compatibility Mode	MinFrameWSizeUnit is in old mode (128b/16Kb)	1h	New Mode	MinFrameWSizeUnit is in new mode (32byte/4Kb)
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15:0	15:0	<b>Min Frame WSize</b>									
		Exists If: //Encoder Only									
		This field (in Word, 16-bit) is specified to compensate for Intel® Rate Control. Zero padding would be performed.									
23	31:16	<b>Vertical_Size_Code</b>									
		Format: U16 Frame Tag Vertical Size Code, composed of {VerticalScale[15:14], FrameHeight[13:0]}									
15:0	15:0	<b>Horizontal_Size_Code</b>									
		Format: U16 Frame Tag Horizontal Size Code, composed of {HorizontalScale[15:14], FrameWidth[13:0]}									
24	31:0	<b>Frame Header Bit Count</b>									
		Format: U32 Binarized Header Bit Count.									
25	31:0	<b>Frame Header Bin Buffer Qindex Update Pointer</b>									
		Format: U32 Binarized Header Qindex Update Pointer If Segment Enabled and UpdateSegmentFeature enabled, 4 per segment Qindices would be updated in Binarized header (Only ABS mode supported). Else Base Qindex would be updated									
26	31:0	<b>Frame Header Bin Buffer LoopFilter Update Pointer</b>									
		Format: U32 Binarized Header LoopFilter Update Pointer If Segment Enabled and UpdateSegmentFeature enabled, 4 per segment LoopFilters would be updated in Binarized header (Only ABS mode supported). Else Base LoopFilter would be updated.									

<b>MFX_VP8_Encoder_CFG</b>																																	
27	31:0	<b>Frame Header Bin Buffer Token Update Pointer</b>																															
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28	31:0	<b>Frame Header Bin Buffer MVUpdate Pointer</b>																															
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29	31:28	<b>ClampValues - CV7</b>																															
	27:24	<b>CV6</b>																															
	23:20	<b>CV5</b>																															
	19:16	<b>CV4</b>																															
	15:12	<b>CV3</b>																															
	11:8	<b>CV2</b>																															
	7:4	<b>CV1</b>																															
	3:0	<b>CV0 - Clamp Value 0</b>																															
	<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">U4</td> </tr> </table>		Format:	U4																													
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<p>If the magnitude of coefficients at locations assigned with CV0 (mapping shown below) exceeds <math>2CV0-1</math>, they are replaced with <math>2CV0-1</math>. For coefficients at locations marked as 'none', no clamping is performed. The following mappings are only applied to luma and chroma blocks\subblocks containing AC coefficients (blocks\subblocks with only DC coeffs will not be clamped).</p> <p><b>For 4x4 frame block, each coefficient is mapped to one of the eight CV values as following:</b></p> <table border="1" style="width: 100%; text-align: center;"> <tr><td>none</td><td>CV7</td><td>CV5</td><td>CV4</td></tr> <tr><td>CV7</td><td>CV6</td><td>CV4</td><td>CV3</td></tr> <tr><td>CV5</td><td>CV4</td><td>CV2</td><td>CV1</td></tr> <tr><td>CV4</td><td>CV3</td><td>CV1</td><td>CV0</td></tr> </table> <p><b>For 4x4 field block, each coefficient is mapped to one of the eight CV values as following:</b></p> <table border="1" style="width: 100%; text-align: center;"> <tr><td>none</td><td>CV6</td><td>CV3</td><td>CV1</td></tr> <tr><td>CV7</td><td>CV6</td><td>CV3</td><td>CV1</td></tr> <tr><td>CV5</td><td>CV4</td><td>CV2</td><td>CV0</td></tr> <tr><td>CV5</td><td>CV4</td><td>CV2</td><td>CV0</td></tr> </table>		none	CV7	CV5	CV4	CV7	CV6	CV4	CV3	CV5	CV4	CV2	CV1	CV4	CV3	CV1	CV0	none	CV6	CV3	CV1	CV7	CV6	CV3	CV1	CV5	CV4	CV2	CV0	CV5	CV4	CV2	CV0
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<p><b>Programming Notes:</b> In this project, the only value permitted for CV7 through CV0 is 0xf The only value permitted for CV7 through CV0 is 0xf</p>																																	

## MFX\_VP8\_PAK\_OBJECT

<b>MFX_VP8_PAK_OBJECT</b>			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>The MFX_VP8_PAK_OBJECT command is the second primitive command for the VP8 Encoding Pipeline. The MV Data portion of the bitstream is loaded as indirect data object. Before issuing a MFX_VP8_PAK_OBJECT command, all VP8 MFX states need to be valid; therefore the commands used to set these states need to have been issued prior to the issue of this command. MB record must be consecutive with no gaps, hence we do not need MB(x,y) in each MB command. Internal counter will keep track of the current MB address, starting from the first MB. MFX_VP8_PAK_OBJECT command follows the MbType definition like MFD. Encoding statistical data such as the total size of the output bitstream are provided through MMIO registers. Software may access these registers through MI_STORE_REGISTER_MEM command.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h MFX_VP8_PAK_OBJECT
		Format:	OpCode
	26:24	<b>Media Command Opcode</b>	
		Default Value:	4h VP8_ENC
		Format:	OpCode
	23:21	<b>SubOpcode A</b>	
		Default Value:	2h
		Format:	OpCode
20:16	<b>SubOpcode B</b>		
	Default Value:	9h	
	Format:	OpCode	
15:12	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
11:0	<b>DWord Length</b>		
	Default Value:	5h DWORD_COUNT_n	
	Project:	All	
	Format:	=n Length -2	
1	31:30	<b>Reserved</b>	

<b>MFX_VP8_PAK_OBJECT</b>						
	29	<b>Reserved</b>				
		<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ
	Project:	CHV, BSW				
Format:	MBZ					
	28:10	<b>Reserved</b>				
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ
	Project:	All				
Format:	MBZ					
	9:0	<b>Indirect PAK-MV Data Length</b>				
		<table border="1"> <tr> <td>Format:</td> <td>U10</td> </tr> </table> <p>This field provides the length in bytes of the indirect data, which contains all the MVs for the current MB (in any partitioning and subpartitioning form). A value zero indicates that indirect data fetching is disabled - subsequently, the Indirect PAK-MV Data Start Address field is ignored. This field must have the same alignment as the Indirect PAK-MV Data Start Address. This field must be DW aligned (since each MV is 4 bytes in size). Driver has to derived this field from MVsize (MVquantity in DXVA, exact size) *4 bytes per MV.</p>	Format:	U10		
Format:	U10					
2	31:29	<b>Reserved</b>				
		<table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ					
	28:0	<b>Indirect PAK-MV Data Start Address Offset</b>				
		<p>This field specifies the memory starting address (offset) of the MV data to be fetched into PAK Subsystem for processing. This pointer is relative to the MFC Indirect PAK-MV Object Base Address. Hardware ignores this field if indirect data is not present, i.e. the Indirect PAK-MV Data Length is set to 0. It is a Dword aligned address in all AVC encoding configuration, since each MV is 4 bytes in size.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>[0,512MB)</td> <td></td> </tr> </tbody> </table>	Value	Name	[0,512MB)	
Value	Name					
[0,512MB)						
3..6	127:0	<b>Inline Data</b>				
		<p>All the required MB level controls and parameters for encoding are captured as Inline Data Description - VP8 PAK OBJECT. It has a fixed size of 4 DWs. Its definition is described in the next section.</p>				

## MFX\_VP8\_PIC\_STATE

MFX_VP8_PIC_STATE			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
This must be the very first command to issue after the surface state, the pipe select and base address setting commands and must be issued before MFX_VP8_IMG_STATE.			
Programming Notes		Project	
Only able to use this instruction for decoder workloads.		CHV, BSW	
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Pipeline</b>	
		Default Value:	2h Video Codec
		Format:	OpCode
	26:24	<b>Media Command OpCode</b>	
		Default Value:	4h VP8
		Format:	OpCode
	23:21	<b>Sub Opcode A</b>	
		Default Value:	0h VP8 Common
		Format:	OpCode
	20:16	<b>Sub Opcode B</b>	
		Default Value:	0h MFX_VP8_PIC_STATE
Format:		OpCode	
15:12	<b>Reserved</b>		
	Format:	MBZ	
11:0	<b>DWord Length</b>	Format:	=n
		Value	Name
	000h	Excludes DWord (0,1) <b>[Default]</b>	A special case to provide a dummy image state for stitch mode operation. In this case, fields in DW1 which is part of the dummy image state command are ignored by hardware."
	024h		Used for normal decode and encode mode

<b>MFX_VP8_PIC_STATE</b>												
1	31:24	<b>Reserved</b>										
		Exists If: //Decoder / Encoder										
		Format: MBZ										
	23:16	<b>Frame Height Minus 1</b>										
		Exists If: //Decoder / Encoder										
		Format: U8 Picture Height in integer number of MBs minus 1, so the min pic height can be program is 16 rows of pixels.										
	15:8	<b>Reserved</b>										
		Exists If: //Decoder / Encoder										
		Format: MBZ										
	7:0	<b>Frame Width Minus 1</b>										
		Exists If: //Decoder / Encoder										
		Format: U8 Picture Width in integer number of MBs minus 1, so the min pic width can be program is 16 pixels.										
2	31:26	<b>Reserved</b>										
		Exists If: //Decoder / Encoder										
		Format: MBZ										
	25:24	<b>Log2 Num of Partition</b>										
		Exists If: //Decoder / Encoder										
		Format: U2										
		<table border="1" style="width: 100%; text-align: center;"><thead><tr><th>Value</th><th>Name</th></tr></thead><tbody><tr><td>0</td><td>1 Token partition</td></tr><tr><td>1</td><td>2 Token partition</td></tr><tr><td>2</td><td>4 Token partition</td></tr><tr><td>3</td><td>8 Token partition</td></tr></tbody></table>	Value	Name	0	1 Token partition	1	2 Token partition	2	4 Token partition	3	8 Token partition
		Value	Name									
		0	1 Token partition									
	1	2 Token partition										
	2	4 Token partition										
	3	8 Token partition										
	23:19	<b>Reserved</b>										
Exists If: //Decoder / Encoder												
Format: MBZ												
18:16	<b>Deblock Sharpness Level</b>											
	Exists If: //Decoder / Encoder											
	Format: U3 Specify the sharpness level, as one of the regular deblocking strength control parameters.											



<b>MFX_VP8_PIC_STATE</b>		
<b>Programming Notes</b>		
Set to 0 to disable the use of sharpness control.		
15:14	<b>Reserved</b>	
	Exists If:	//Decoder / Encoder
	Format:	MBZ
13	<b>Alternate Ref Pic MV SignBias Flag</b>	
	Exists If:	//Decoder / Encoder
Alternate Reference Picture MV sign bias flag, specified for non-key frame only.		
12	<b>Golden Ref Picture MV SignBias Flag</b>	
	Exists If:	//Decoder / Encoder
Golden Reference Picture MV sign bias flag, specified for non-key frame only.		
11	<b>Mode Reference Loop Filter Delta Enabled</b>	
	Exists If:	//Decoder / Encoder
	<b>Value</b>	<b>Name</b> <b>Description</b>
	0	Mode or Reference Loop Filter Delta Adjustment for current frame is disabled.
	1	Mode or Reference Loop Filter Delta Adjustment for current frame is enabled.
10	<b>MB NoCoeff SkipFlag</b>	
	Exists If:	//Decoder / Encoder
Frame level control if Skip MB (with no non-zero coefficient) is allowed or not.		
	<b>Value</b>	<b>Name</b> <b>Description</b>
	0	All MBs will have its MB level signaling mb_skip_coeff forced to 0. That is, no skip of coefficient record in the bitstream (even their values are all 0s)
	1	Skip MB is enabled in the per MB record.
9	<b>Update MBSegment Map Flag</b>	
	Exists If:	//Decoder / Encoder
	<b>Value</b>	<b>Name</b> <b>Description</b>
	0	Disable segmentation update
	1	Enable segmentation update, and to enable reading segment_id for each MB.
8	<b>Segment Enable Flag</b>	
	Exists If:	//Decoder / Encoder
	<b>Value</b>	<b>Name</b> <b>Description</b>
	0	Disable Segmentation processing in the current frame

<b>MFX_VP8_PIC_STATE</b>		
1		Enable Segmentation processing in the current frame
7	<b>Segmentation ID StreamIn Enable</b>	
	Exists If:	//Decoder Only
	<b>Value</b>	<b>Name</b>
	0	StreamIn Disabled
	1	StreamIn Enabled
	<b>Programming Notes</b>	
	When 0, no input needed.	
7:6	<b>Reserved</b>	
	Exists If:	//Encoder Only
	Format:	MBZ
6	<b>Segmentation ID StreamOut Enable</b>	
	Exists If:	//Decoder Only
	<b>Value</b>	<b>Name</b>
	0	StreamOut Disabled
	1	StreamOut Enabled
	<b>Programming Notes</b>	
	When 0, no output needed.	
5	<b>sKeyFrameFlag</b>	
	Exists If:	//Decoder / Encoder
	<b>Value</b>	<b>Name</b>
	0	Non-Key Frame (P-Frame)
	1	Key Frame (I-Frame)
4	<b>DBLKFilterType</b>	
	Exists If:	//Decoder / Encoder
	To specify VP8 Profile of operation.	
	<b>Value</b>	<b>Name</b>
	0	Use a full feature normal deblocking filter
	1	Use a simple filter for deblocking
3:2	<b>Reserved</b>	
	Exists If:	//Decoder / Encoder

<b>MFX_VP8_PIC_STATE</b>			
		Format: MBZ	
1	<b>Chroma Full Pixel MC Filter Mode</b>		
	Exists If:	//Decoder / Encoder	
	To specify VP8 Profile of operation.		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0		Chroma MC filter operates in sub-pixel mode
	1		Chroma MC filter only operates in full pixel position, i.e. no sub-pixel interpolation.
	0	<b>MC Filter Select</b>	
		Exists If:	//Decoder / Encoder
		To specify VP8 Profile of operation.	
		<b>Value</b>	<b>Name</b>
0			6-tap filter (regular filter mode)
1			2-tap bilinear filter (simple profile/version mode)
3	31:30	<b>Reserved</b>	
	Exists If:	//Decoder / Encoder	
	Format:	MBZ	
	29:24	<b>DBLKFilterLevel for Segment3</b>	
	Exists If:	//Decoder / Encoder	
	Format:	U6	
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0	Signifies disable in loop deblocking operation	This is used to set a VP8 profile without in loop deblocker.
	<b>Programming Notes</b>		
	There are max 4 segments per frame, each segment can have its own deblocking filter level. When segmentation is disabled, only segment 0 parameter is used for the entire frame.		
	<b>Restriction</b>		
	For VP8 Encoder: $\text{Max}(\text{DBLKFilterLevel for Segment0}, \text{DBLKFilterLevel for Segment1}, \text{DBLKFilterLevel for Segment2}, \text{DBLKFilterLevel for Segment3}) + \text{Max}(\text{RefLFDelta0}, \text{RefLFDelta1}, \text{RefLFDelta2}, \text{RefLFDelta3}) + \text{Max}(\text{ModeLFDelta0}, \text{ModeLFDelta1}, \text{ModeLFDelta2}, \text{ModeLFDelta3}) < 128$		
	23:22	<b>Reserved</b>	
	Exists If:	//Decoder / Encoder	

<b>MFX_VP8_PIC_STATE</b>			
	Format:	MBZ	
21:16	<b>DBLKFilterLevel for Segment2</b>		
	Exists If:	//Decoder / Encoder	
	Format:	U6	
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0	Signifies disable in loop deblocking operation	This is used to set a VP8 profile without in loop deblocker.
	<b>Programming Notes</b>		
	There are max 4 segments per frame, each segment can have its own deblocking filter level. When segmentation is disabled, only segment 0 parameter is used for the entire frame.		
	<b>Restriction</b>		
	For VP8 Encoder: Max (DBLKFilterLevel for Segment0, DBLKFilterLevel for Segment1, DBLKFilterLevel for Segment2, DBLKFilterLevel for Segment3) + Max (RefLFDelta0, RefLFDelta1, RefLFDelta2, RefLFDelta3) + Max (ModeLFDelta0, ModeLFDelta1, ModeLFDelta2, ModeLFDelta3) < 128		
	15:14	<b>Reserved</b>	
Exists If:		//Decoder / Encoder	
Format:		MBZ	
13:8	<b>DBLKFilterLevel for Segment1</b>		
	Exists If:	//Decoder / Encoder	
	Format:	U6	
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0	Signifies disable in loop deblocking operation	This is used to set a VP8 profile without in loop deblocker.
	<b>Programming Notes</b>		
	There are max 4 segments per frame, each segment can have its own deblocking filter level. When segmentation is disabled, only segment 0 parameter is used for the entire frame.		
	<b>Restriction</b>		
	For VP8 Encoder: Max (DBLKFilterLevel for Segment0, DBLKFilterLevel for Segment1, DBLKFilterLevel for Segment2, DBLKFilterLevel for Segment3) + Max (RefLFDelta0, RefLFDelta1, RefLFDelta2, RefLFDelta3) + Max (ModeLFDelta0, ModeLFDelta1, ModeLFDelta2, ModeLFDelta3) < 128		
	7:6	<b>Reserved</b>	
Exists If:		//Decoder / Encoder	

<b>MFX_VP8_PIC_STATE</b>								
		Format: MBZ						
	5:0	<b>DBLFilterLevel for Segment0</b>						
		Exists If: //Decoder / Encoder						
		Format: U6						
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Signifies disable in loop deblocking operation</td> <td>This is used to set a VP8 profile without in loop deblocker.</td> </tr> </tbody> </table>	Value	Name	Description	0	Signifies disable in loop deblocking operation	This is used to set a VP8 profile without in loop deblocker.
Value	Name	Description						
0	Signifies disable in loop deblocking operation	This is used to set a VP8 profile without in loop deblocker.						
		<b>Programming Notes</b>						
		There are max 4 segments per frame, each segment can have its own deblocking filter level. When segmentation is disabled, only segment 0 parameter is used for the entire frame.						
		<table border="1"> <thead> <tr> <th>Restriction</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>For VP8 Encoder: Max (DBLFilterLevel for Segment0, DBLFilterLevel for Segment1, DBLFilterLevel for Segment2, DBLFilterLevel for Segment3) + Max (RefLFDelta0, RefLFDelta1, RefLFDelta2, RefLFDelta3) + Max (ModeLFDelta0, ModeLFDelta1, ModeLFDelta2, ModeLFDelta3) &lt; 128</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Restriction	Project	For VP8 Encoder: Max (DBLFilterLevel for Segment0, DBLFilterLevel for Segment1, DBLFilterLevel for Segment2, DBLFilterLevel for Segment3) + Max (RefLFDelta0, RefLFDelta1, RefLFDelta2, RefLFDelta3) + Max (ModeLFDelta0, ModeLFDelta1, ModeLFDelta2, ModeLFDelta3) < 128	CHV, BSW		
Restriction	Project							
For VP8 Encoder: Max (DBLFilterLevel for Segment0, DBLFilterLevel for Segment1, DBLFilterLevel for Segment2, DBLFilterLevel for Segment3) + Max (RefLFDelta0, RefLFDelta1, RefLFDelta2, RefLFDelta3) + Max (ModeLFDelta0, ModeLFDelta1, ModeLFDelta2, ModeLFDelta3) < 128	CHV, BSW							
4 <b>Project:</b> CHV, BSW	31	<b>Reserved</b>						
		Project: CHV, BSW						
		Exists If: //Encoder Only						
		Format: MBZ						
	30:24	<b>Seg 3 Qindex</b>						
		Project: CHV, BSW						
		Exists If: //Encoder Only						
		Format: U7						
		Quantizer Value for Segment ID 3						
	23	<b>Reserved</b>						
		Project: CHV, BSW						
		Exists If: //Encoder Only						
		Format: MBZ						
	22:16	<b>Seg 2 Qindex</b>						
		Project: CHV, BSW						
	Exists If: //Encoder Only							
	Format: U7							
	Quantizer Value for Segment ID 2							
15	<b>Reserved</b>							
	Project: CHV, BSW							

<b>MFX_VP8_PIC_STATE</b>																	
	<table border="1"> <tr> <td>Exists If:</td> <td>//Encoder Only</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Exists If:	//Encoder Only	Format:	MBZ												
Exists If:	//Encoder Only																
Format:	MBZ																
14:8	<p><b>Seg 1 Qindex</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Encoder Only</td> </tr> <tr> <td>Format:</td> <td>U7</td> </tr> </table> <p>Quantizer Value for Segment ID 1</p>	Project:	CHV, BSW	Exists If:	//Encoder Only	Format:	U7										
Project:	CHV, BSW																
Exists If:	//Encoder Only																
Format:	U7																
7	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Encoder Only</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Exists If:	//Encoder Only	Format:	MBZ										
Project:	CHV, BSW																
Exists If:	//Encoder Only																
Format:	MBZ																
31:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Decoder Only</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Exists If:	//Decoder Only	Format:	MBZ										
Project:	CHV, BSW																
Exists If:	//Decoder Only																
Format:	MBZ																
6:0	<p><b>Seg 0 Qindex</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Encoder Only</td> </tr> <tr> <td>Format:</td> <td>U7</td> </tr> </table> <p>Quantizer Value for Segment ID 0.</p> <table border="1" style="background-color: #e6f2ff;"> <tr> <td colspan="2" style="text-align: center;"><b>Programming Notes</b></td> </tr> <tr> <td colspan="2">This is the <b>[Default]</b> Qindex</td> </tr> </table>	Project:	CHV, BSW	Exists If:	//Encoder Only	Format:	U7	<b>Programming Notes</b>		This is the <b>[Default]</b> Qindex							
Project:	CHV, BSW																
Exists If:	//Encoder Only																
Format:	U7																
<b>Programming Notes</b>																	
This is the <b>[Default]</b> Qindex																	
5	<p>31:29 <b>Reserved</b></p> <table border="1"> <tr> <td>Exists If:</td> <td>//Encoder Only</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>28 <b>UVac Qindex Delta Sign</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Encoder Only</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>Sign of Quantization index delta for UVac</p> <p>27:24 <b>UVac QindexDelta</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Encoder Only</td> </tr> <tr> <td>Format:</td> <td>U4</td> </tr> </table> <p>Absolute Quantization index delta for UVac</p> <p>23:21 <b>Reserved</b></p>	Exists If:	//Encoder Only	Format:	MBZ	Project:	CHV, BSW	Exists If:	//Encoder Only	Format:	U1	Project:	CHV, BSW	Exists If:	//Encoder Only	Format:	U4
Exists If:	//Encoder Only																
Format:	MBZ																
Project:	CHV, BSW																
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Format:	U1																
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Format:	U4																

<b>MFX_VP8_PIC_STATE</b>							
	<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Encoder Only</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Exists If:	//Encoder Only	Format:	MBZ
Project:	CHV, BSW						
Exists If:	//Encoder Only						
Format:	MBZ						
20	<p><b>UVdc Qindex Delta Sign</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Encoder Only</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>Sign of Quantization index delta for UVdc</p>	Project:	CHV, BSW	Exists If:	//Encoder Only	Format:	U1
Project:	CHV, BSW						
Exists If:	//Encoder Only						
Format:	U1						
19:16	<p><b>UVdc Qindex Delta</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Encoder Only</td> </tr> <tr> <td>Format:</td> <td>U4</td> </tr> </table> <p>Absolute Quantization index delta for UVdc</p>	Project:	CHV, BSW	Exists If:	//Encoder Only	Format:	U4
Project:	CHV, BSW						
Exists If:	//Encoder Only						
Format:	U4						
15:13	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Encoder Only</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Exists If:	//Encoder Only	Format:	MBZ
Project:	CHV, BSW						
Exists If:	//Encoder Only						
Format:	MBZ						
12	<p><b>Y2ac Qindex Sign</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Encoder Only</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>Sign of Quantization index delta for Y2ac</p>	Project:	CHV, BSW	Exists If:	//Encoder Only	Format:	U1
Project:	CHV, BSW						
Exists If:	//Encoder Only						
Format:	U1						
11:8	<p><b>Y2ac Qindex Delta</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Encoder Only</td> </tr> <tr> <td>Format:</td> <td>U4</td> </tr> </table> <p>Absolute Quantization index delta for Y2ac</p>	Project:	CHV, BSW	Exists If:	//Encoder Only	Format:	U4
Project:	CHV, BSW						
Exists If:	//Encoder Only						
Format:	U4						
7:5	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Encoder Only</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Exists If:	//Encoder Only	Format:	MBZ
Project:	CHV, BSW						
Exists If:	//Encoder Only						
Format:	MBZ						
4	<p><b>Y2ac Qindex Delta Sign</b></p>						

<b>MFX_VP8_PIC_STATE</b>		
		Project: CHV, BSW
		Exists If: //Encoder Only
		Format: U1
		Sign of Quantization index delta for Y2dc
		This is the <b>[Default]</b> Qindex Delta Sign
	31:0	<b>Reserved</b>
		Exists If: //Decoder Only
		Format: MBZ
	3:0	<b>Y2dc Qindex Delta</b>
		Project: CHV, BSW
	Exists If: //Encoder Only	
	Format: U4	
	Absolute Quantization index delta for Y2dc	
	This is the <b>[Default]</b> Qindex Delta	
6	31:5	<b>Reserved</b>
		Exists If: //Encoder Only
		Format: MBZ
	4	<b>Y1dc Qindex Delta Sign</b>
		Project: CHV, BSW
		Exists If: //Encoder Only
		Format: U1
		Sign of Quantization index delta for Y1dc
	This is the <b>[Default]</b> Qindex Delta Sign	
	31:0	<b>Reserved</b>
		Project: CHV, BSW
		Exists If: //Decoder Only
		Format: MBZ
	3:0	<b>Y1dc Qindex Delta</b>
		Project: CHV, BSW
Exists If: //Encoder Only		
Absolute Quantization index delta for Y1dc		
	This is the <b>[Default]</b> Qindex Delta	
7	31:15	<b>Reserved</b>



<b>MFX_VP8_PIC_STATE</b>								
<b>Project:</b> CHV, BSW		<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Encoder Only</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Exists If:	//Encoder Only	Format:	MBZ
	Project:	CHV, BSW						
	Exists If:	//Encoder Only						
	Format:	MBZ						
	14:8	<p><b>Clamp Qindex high</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Encoder Only</td> </tr> <tr> <td>Format:</td> <td>U7</td> </tr> </table> <p>Maximum Clamp Value for Qindex used in quantization.</p>	Project:	CHV, BSW	Exists If:	//Encoder Only	Format:	U7
	Project:	CHV, BSW						
	Exists If:	//Encoder Only						
	Format:	U7						
	7	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Encoder Only</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Exists If:	//Encoder Only	Format:	MBZ
	Project:	CHV, BSW						
	Exists If:	//Encoder Only						
	Format:	MBZ						
	31:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Decoder Only</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Exists If:	//Decoder Only	Format:	MBZ
	Project:	CHV, BSW						
	Exists If:	//Decoder Only						
Format:	MBZ							
6:0	<p><b>Clamp Qindex Low</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Encoder Only</td> </tr> <tr> <td>Format:</td> <td>U7</td> </tr> </table> <p>Minimum Clamp Value for Qindex used in quantization.</p>	Project:	CHV, BSW	Exists If:	//Encoder Only	Format:	U7	
Project:	CHV, BSW							
Exists If:	//Encoder Only							
Format:	U7							
8	31:25	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Exists If:</td> <td>//Decoder Only</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Exists If:	//Decoder Only	Format:	MBZ		
	Exists If:	//Decoder Only						
	Format:	MBZ						
	24:16	<p><b>Quantizer Value [1][BlockType3=UVAC]</b></p> <table border="1"> <tr> <td>Exists If:</td> <td>//Decoder Only</td> </tr> <tr> <td>Format:</td> <td>U9</td> </tr> </table> <p><b>Quantizer Value [n = Segment_Id = 0..3][BlockType = 0..5]</b></p>	Exists If:	//Decoder Only	Format:	U9		
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Format:	U9							
15:9	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Exists If:</td> <td>//Decoder Only</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Exists If:	//Decoder Only	Format:	MBZ			
Exists If:	//Decoder Only							
Format:	MBZ							
31:0	<p><b>Reserved</b></p>							

<b>MFX_VP8_PIC_STATE</b>				
		Exists If:	//Encoder Only	
		Format:	MBZ	
8:0		<b>Quantizer Value [1][BlockType2=UVDC]</b>		
		Exists If:	//Decoder Only	
		<b>Quantizer Value [n = Segment_Id = 0..3][BlockType = 0..5]</b>		
9	31:25	<b>Reserved</b>		
		Exists If:	//Decoder Only	
		Format:	MBZ	
	24:16	<b>Quantizer Value [1][BlockType5=Y2AC]</b>		
		Exists If:	//Decoder Only	
		Format:	U9	
			<b>Quantizer Value [n = Segment_Id = 0..3][BlockType = 0..5]</b>	
	15:9	<b>Reserved</b>		
		Exists If:	//Decoder Only	
		Format:	MBZ	
	31:0	<b>Reserved</b>		
		Exists If:	//Encoder Only	
		Format:	MBZ	
	8:0	<b>Quantizer Value [1][BlockType4=Y2DC]</b>		
		Exists If:	//Decoder Only	
			<b>Quantizer Value [n = Segment_Id = 0..3][BlockType = 0..5]</b>	
	10	31:25	<b>Reserved</b>	
			Exists If:	//Decoder Only
Format:			MBZ	
24:16		<b>Quantizer Value [2][BlockType1=Y1AC]</b>		
		Exists If:	//Decoder Only	
		Format:	U9	
		<b>Quantizer Value [n = Segment_Id = 0..3][BlockType = 0..5]</b>		
15:9		<b>Reserved</b>		
		Exists If:	//Decoder Only	
		Format:	MBZ	
31:0		<b>Reserved</b>		
		Exists If:	//Encoder Only	
		Format:	MBZ	
8:0		<b>Quantizer Value [2][BlockType0=Y1DC]</b>		

<b>MFX_VP8_PIC_STATE</b>									
		<table border="1"> <tr> <td>Exists If:</td> <td>//Decoder Only</td> </tr> <tr> <td colspan="2"><b>Quantizer Value [n = Segment_Id = 0..3][BlockType = 0..5]</b></td> </tr> </table>	Exists If:	//Decoder Only	<b>Quantizer Value [n = Segment_Id = 0..3][BlockType = 0..5]</b>				
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<b>Quantizer Value [n = Segment_Id = 0..3][BlockType = 0..5]</b>									
11	31:25	<b>Reserved</b>							
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	<b>Quantizer Value [2][BlockType3=UVAC]</b>								
	Exists If:	//Decoder Only							
	Format:	U9							
	<b>Quantizer Value [n = Segment_Id = 0..3][BlockType = 0..5]</b>								
	15:9	<b>Reserved</b>							
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31:0	<b>Reserved</b>								
	<table border="1"> <tr> <td>Exists If:</td> <td>//Encoder Only</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Exists If:	//Encoder Only	Format:	MBZ				
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Format:	MBZ								
<table border="1"> <tr> <td colspan="2"><b>Quantizer Value [2][BlockType2=UVDC]</b></td> </tr> <tr> <td>Exists If:</td> <td>//Decoder Only</td> </tr> <tr> <td colspan="2"><b>Quantizer Value [n = Segment_Id = 0..3][BlockType = 0..5]</b></td> </tr> </table>	<b>Quantizer Value [2][BlockType2=UVDC]</b>		Exists If:	//Decoder Only	<b>Quantizer Value [n = Segment_Id = 0..3][BlockType = 0..5]</b>				
<b>Quantizer Value [2][BlockType2=UVDC]</b>									
Exists If:	//Decoder Only								
<b>Quantizer Value [n = Segment_Id = 0..3][BlockType = 0..5]</b>									
12	31:25	<b>Reserved</b>							
		<table border="1"> <tr> <td>Exists If:</td> <td>//Decoder Only</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Exists If:	//Decoder Only	Format:	MBZ			
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	Format:	MBZ							
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	15:9	<b>Reserved</b>							
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Format:	MBZ								
31:0	<b>Reserved</b>								
	<table border="1"> <tr> <td>Exists If:</td> <td>//Encoder Only</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Exists If:	//Encoder Only	Format:	MBZ				
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Format:	MBZ								
<table border="1"> <tr> <td colspan="2"><b>Quantizer Value [2][BlockType4=Y2DC]</b></td> </tr> <tr> <td>Exists If:</td> <td>//Decoder Only</td> </tr> <tr> <td colspan="2"><b>Quantizer Value [n = Segment_Id = 0..3][BlockType = 0..5]</b></td> </tr> </table>	<b>Quantizer Value [2][BlockType4=Y2DC]</b>		Exists If:	//Decoder Only	<b>Quantizer Value [n = Segment_Id = 0..3][BlockType = 0..5]</b>				
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Exists If:	//Decoder Only								
<b>Quantizer Value [n = Segment_Id = 0..3][BlockType = 0..5]</b>									
13	31:25	<b>Reserved</b>							

<b>MFX_VP8_PIC_STATE</b>			
		Exists If: //Decoder Only	
		Format: MBZ	
	24:16	<b>Quantizer Value [3][BlockType1=Y1AC]</b>	
		Exists If: //Decoder Only	
		Format: U9	
	<b>Quantizer Value [n = Segment_Id = 0..3][BlockType = 0..5]</b>		
	15:9	<b>Reserved</b>	
		Exists If: //Decoder Only	
		Format: MBZ	
	31:0	<b>Reserved</b>	
Exists If: //Encoder Only			
Format: MBZ			
8:0	<b>Quantizer Value [3][BlockType0=Y1DC]</b>		
	Exists If: //Decoder Only		
	<b>Quantizer Value [n = Segment_Id = 0..3][BlockType = 0..5]</b>		
14	31:25	<b>Reserved</b>	
		Exists If: //Decoder Only	
		Format: MBZ	
	24:16	<b>Quantizer Value [3][BlockType3=UVAC]</b>	
		Exists If: //Decoder Only	
		Format: U9	
	<b>Quantizer Value [n = Segment_Id = 0..3][BlockType = 0..5]</b>		
	15:9	<b>Reserved</b>	
		Exists If: //Decoder Only	
		Format: MBZ	
	31:0	<b>Reserved</b>	
		Exists If: //Encoder Only	
		Format: MBZ	
	8:0	<b>Quantizer Value [3][BlockType2=UVDC]</b>	
		Exists If: //Decoder Only	
<b>Quantizer Value [n = Segment_Id = 0..3][BlockType = 0..5]</b>			
15	31:25	<b>Reserved</b>	

<b>MFX_VP8_PIC_STATE</b>			
		Exists If:	//Decoder Only
		Format:	MBZ
	24:16	<b>Quantizer Value [3][BlockType5=Y2AC]</b>	
		Exists If:	//Decoder Only
		Format:	U9
		<b>Quantizer Value [n = Segment_Id = 0..3][BlockType = 0..5]</b>	
	15:9	<b>Reserved</b>	
		Exists If:	//Decoder Only
		Format:	MBZ
	31:0	<b>Reserved</b>	
	Exists If:	//Encoder Only	
	Format:	MBZ	
16	8:0	<b>Quantizer Value [3][BlockType4=Y2DC]</b>	
		Exists If:	//Decoder Only
		<b>Quantizer Value [n = Segment_Id = 0..3][BlockType = 0..5]</b>	
	31:6	<b>CoeffProbability StreamIn Base Address</b>	
		Exists If:	//Decoder Only
		Format:	StreamInAddress[31:6] 64 bytes aligned buffer in linear format. (not tile for better performance)
		It is specified for non-key frame only. It is the final computed probability table for parsing Coeff in the bitstream. The buffer is unsigned 8-bit * 1056 entries (CoeffProbs[4][8][3][11].	
	31:0	<b>Reserved</b>	
		Exists If:	//Encoder Only
		Format:	MBZ
17 <b>Project:</b> CHV, BSW	5:0	<b>Reserved</b>	
		Project:	CHV, BSW
		Exists If:	//Decoder Only
		Format:	MBZ
	31:16	<b>Reserved</b>	
		Project:	CHV, BSW
		Exists If:	//Decoder Only
		Format:	MBZ
	31:0	<b>Reserved</b>	

<b>MFX_VP8_PIC_STATE</b>																	
	<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Encoder Only</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Exists If:	//Encoder Only	Format:	MBZ										
	Project:	CHV, BSW															
	Exists If:	//Encoder Only															
	Format:	MBZ															
	15:0	<p><b>CoeffProbability StreamIn Address</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Decoder Only</td> </tr> </table> <p>This field is for the upper range of CoeffProbability StreamIn Address</p>	Project:	CHV, BSW	Exists If:	//Decoder Only											
	Project:	CHV, BSW															
Exists If:	//Decoder Only																
18 <b>Project:</b> CHV, BSW	31:15	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Decoder Only</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Exists If:	//Decoder Only	Format:	MBZ									
	Project:	CHV, BSW															
	Exists If:	//Decoder Only															
	Format:	MBZ															
	14:13	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Decoder Only</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Exists If:	//Decoder Only	Format:	MBZ									
	Project:	CHV, BSW															
Exists If:	//Decoder Only																
Format:	MBZ																
12:11	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Decoder Only</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Exists If:	//Decoder Only	Format:	MBZ										
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10:9	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Decoder Only</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Exists If:	//Decoder Only	Format:	MBZ										
Project:	CHV, BSW																
Exists If:	//Decoder Only																
Format:	MBZ																
8:7	<p><b>CoeffProbability StreamIn - Arbitration Priority Control</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Decoder Only</td> </tr> <tr> <td>Format:</td> <td>U2</td> </tr> </table> <p>This field controls the priority of arbitration used in the GAC/GAM pipeline for this surface.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Highest priority</td> </tr> <tr> <td>01b</td> <td>Second highest priority</td> </tr> <tr> <td>10b</td> <td>Third highest priority</td> </tr> <tr> <td>11b</td> <td>Lowest priority</td> </tr> </tbody> </table>	Project:	CHV, BSW	Exists If:	//Decoder Only	Format:	U2	Value	Name	00b	Highest priority	01b	Second highest priority	10b	Third highest priority	11b	Lowest priority
	Project:	CHV, BSW															
	Exists If:	//Decoder Only															
	Format:	U2															
	Value	Name															
	00b	Highest priority															
01b	Second highest priority																
10b	Third highest priority																
11b	Lowest priority																
6:5	<p><b>Memory Type: LLC/eLLC Cacheability Control (LeLLCCC) for CoeffProbability StreamIn</b></p>																

## MFX\_VP8\_PIC\_STATE

<b>Address</b>			
Project:	CHV, BSW		
Exists If:	//Decoder Only		
<p>This is the field used in GT interface block to determine what type of access need to be generated to uncore. For the cases where the LeLLCCC is set, cacheable transaction are generated to enable LLC usage for particular stream.</p>			
<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Exists If</b>
00b	Use Cacheability Controls from page table		//Decoder Only
01b	UC	Uncacheable - non-cacheable	
10b	WT	Writethrough	
11b	WB	Writeback	
4:3	<b>CoeffProbability StreamIn Address - Target Cache (TC)</b>		
Project:		CHV, BSW	
Exists If:		//Decoder Only	
<p>This field allows the choice of LLC vs eLLC for caching</p>			
<b>Value</b>	<b>Name</b>		
00b	eLLC Only - not snooped in GT		
01b	LLC Only		
10b	LLC/eLLC Allowed		
11b	L3, LLC, eLLC Allowed		
2	<b>Reserved</b>		
Project:		CHV, BSW	
31:0	<b>Reserved</b>		
Project:		CHV, BSW	
Exists If:		//Encoder Only	
Format:		MBZ	
1:0	<b>CoeffProbability StreamIn Address - Age for QUADLRU (AGE)</b>		
Project:		CHV, BSW	
Exists If:		//Decoder Only	
<p>This field allows the selection of AGE parameter for a given surface in LLC or eLLC.</p>			
<b>Value</b>	<b>Name</b>		
11b	Good chance of generating hits.		
10b	Next good chance of generating hits		
01b	Decent chance of generating hits		
00b	Poor chance of generating hits		

<b>MFX_VP8_PIC_STATE</b>		
19	31:24	<b>Reserved</b>
		Exists If: //Decoder / Encoder
		Format: MBZ
	23:16	<b>MBSegmentIDTreeProbs[2]</b>
		Exists If: //Decoder / Encoder
		Format: U8 MBSegmentIDTreeProbs[2:0] probability tree table for CPBAC parsing Segment_ID of each MB.
	15:8	<b>MBSegmentIDTreeProbs[1]</b>
		Exists If: //Decoder / Encoder
		Format: U8 MBSegmentIDTreeProbs[2:0] probability tree table for CPBAC parsing Segment_ID of each MB.
	7:0	<b>MBSegmentIDTreeProbs[0]</b>
		Exists If: //Decoder / Encoder
		Format: U8 MBSegmentIDTreeProbs[2:0] probability tree table for CPBAC parsing Segment_ID of each MB.
20	31:24	<b>MBNoCoeffSkipFalseProb</b>
		Exists If: //Decoder / Encoder
		Format: U8 8-bit probability value for CPBAC parsing of the MBNoCoeffSkip Flag in the bistream.
	23:16	<b>IntraMBProb</b>
		Exists If: //Decoder / Encoder
		Format: U8 8-bit probability value for CPBAC parsing of the intra or inter MB type flag in the bitstream.
	15:8	<b>InterPredFromLastRefProb</b>
		Exists If: //Decoder / Encoder
		Format: U8 8-bit probability value for CPBAC parsing of the flag in the bitstream that determines which reference frame to be used for the current MB motion compensation.
	7:0	<b>InterPredFromGRefRefProb</b>
		Exists If: //Decoder / Encoder
		Format: U8 8-bit probability value for CPBAC parsing of the flag in the bitstream that determines which reference frame to be used for the current MB motion compensation.
21	31:24	<b>YModeProb[3]</b>
		Exists If: //Decoder / Encoder



<b>MFX_VP8_PIC_STATE</b>						
		<table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>YModeProb[3:0] probability tree table for CPBAC parsing Luma MBType of each MB.</p>	Format:	U8		
Format:	U8					
	23:16	<p><b>YModeProb[2]</b></p> <table border="1"> <tr> <td>Exists If:</td> <td>//Decoder / Encoder</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>YModeProb[3:0] probability tree table for CPBAC parsing Luma MBType of each MB.</p>	Exists If:	//Decoder / Encoder	Format:	U8
Exists If:	//Decoder / Encoder					
Format:	U8					
	15:8	<p><b>YModeProb[1]</b></p> <table border="1"> <tr> <td>Exists If:</td> <td>//Decoder / Encoder</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>YModeProb[3:0] probability tree table for CPBAC parsing Luma MBType of each MB.</p>	Exists If:	//Decoder / Encoder	Format:	U8
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Format:	U8					
	7:0	<p><b>YModeProb[0]</b></p> <table border="1"> <tr> <td>Exists If:</td> <td>//Decoder / Encoder</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>YModeProb[3:0] probability tree table for CPBAC parsing Luma MBType of each MB.</p>	Exists If:	//Decoder / Encoder	Format:	U8
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Format:	U8					
22	31:24	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Exists If:</td> <td>//Decoder / Encoder</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Exists If:	//Decoder / Encoder	Format:	MBZ
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	23:16	<p><b>UVModeProb[2]</b></p> <table border="1"> <tr> <td>Exists If:</td> <td>//Decoder / Encoder</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>UVModeProb[2:0] probability tree table for CPBAC parsing Chroma MBType of each MB.</p>	Exists If:	//Decoder / Encoder	Format:	U8
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Format:	U8					
	15:8	<p><b>UVModeProb[1]</b></p> <table border="1"> <tr> <td>Exists If:</td> <td>//Decoder / Encoder</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>UVModeProb[2:0] probability tree table for CPBAC parsing Chroma MBType of each MB.</p>	Exists If:	//Decoder / Encoder	Format:	U8
Exists If:	//Decoder / Encoder					
Format:	U8					
	7:0	<p><b>UVModeProb[0]</b></p> <table border="1"> <tr> <td>Exists If:</td> <td>//Decoder / Encoder</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>UVModeProb[2:0] probability tree table for CPBAC parsing Chroma MBType of each MB.</p>	Exists If:	//Decoder / Encoder	Format:	U8
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		Exists If:	//Decoder / Encoder
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	Exists If:	//Decoder / Encoder	
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27	31:24	<b>Reserved</b>	
		Exists If:	//Decoder / Encoder
		Format:	MBZ
	23:16	<b>MVUpdateProbs[0][18]</b>	
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	7:0	<b>MVUpdateProbs[0][16]</b>	
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28	31:24	<b>MVUpdateProbs[1][3]</b>	
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30:24	<p><b>RefLFDelta3 (for ALTREF FRAME)</b></p> <table border="1"> <tr> <td>Exists If:</td> <td>//Decoder / Encoder</td> </tr> <tr> <td>Format:</td> <td>S6 2's Compliment</td> </tr> </table> <p>Delta value for reference frame based adjustment of the MB-level's filter level value. RefLFDeltas [ref_frametype = 0 to 3]</p> <p style="text-align: center;"><b>Programming Notes</b></p> <p>Please note that although RefDelta is signed 2's complement, bitstream is sign bit + 6 bit magnitude.</p>	Exists If:	//Decoder / Encoder	Format:	S6 2's Compliment	
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<b>MFX_VP8_PIC_STATE</b>			
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	7	<b>Reserved</b>	
		Exists If:	//Decoder / Encoder
		Format:	MBZ
	6:0	<b>RefLFDelta0 (for INTRA FRAME)</b>	
		Exists If:	//Decoder / Encoder
		Format:	S6 2's Compliment
		Delta value for reference frame based adjustment of the MB-level's filter level value. RefLFDeltas [ref_frametype = 0 to 3]	
		<b>Programming Notes</b>	
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34	31	<b>Reserved</b>	
		Exists If:	//Decoder / Encoder
		Format:	MBZ
	30:24	<b>ModeLFDelta3 (for SPLITMV mode)</b>	
		Exists If:	//Decoder / Encoder
		Format:	S6 2's Compliment
		Delta value for mode based adjustment of the MB-level's filter level value. ModeLFDeltas[MB_Type = 0 to 3]	
		<b>Programming Notes</b>	
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14:8	<b>ModeLFDelta1 (for ZEROMV mode)</b>	<table border="1"> <tr> <td>Exists If:</td> <td>//Decoder / Encoder</td> </tr> <tr> <td>Format:</td> <td>S6 2's Compliment</td> </tr> </table> <p>Delta value for mode based adjustment of the MB-level's filter level value. ModeLFDeltas[MB_Type = 0 to 3]</p> <p style="text-align: center;"><b>Programming Notes</b></p> <p>Please note that although ModeLFDelta is signed 2's complement, bitstream is sign bit + 6 bit magnitude.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Restriction</th> <th style="text-align: center;">Project</th> </tr> </thead> <tbody> <tr> <td></td> <td></td> </tr> </tbody> </table>	Exists If:	//Decoder / Encoder	Format:	S6 2's Compliment	Restriction	Project		
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	6:0	<p><b>ModeLFDelta0 (for B_PRED mode)</b></p> <table border="1"> <tr> <td>Exists If:</td> <td>//Decoder / Encoder</td> </tr> <tr> <td>Format:</td> <td>S6 2's Compliment</td> </tr> </table> <p>Delta value for mode based adjustment of the MB-level's filter level value.</p> <p>ModeLFDeltas[MB_Type = 0 to 3]</p> <p style="text-align: center;"><b>Programming Notes</b></p> <p>Please note that although ModeLFDelta is signed 2's complement, bitstream is sign bit + 6 bit magnitude.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Restriction</th> <th style="text-align: center;">Project</th> </tr> </thead> <tbody> <tr> <td>For VP8 Encoder: Max (DBLKFilterLevel for Segment0, DBLKFilterLevel for Segment1, DBLKFilterLevel for Segment2, DBLKFilterLevel for Segment3) + Max (RefLFDelta0, RefLFDelta1, RefLFDelta2, RefLFDelta3) + Max (ModeLFDelta0, ModeLFDelta1, ModeLFDelta2, ModeLFDelta3) &lt; 128</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Exists If:	//Decoder / Encoder	Format:	S6 2's Compliment	Restriction	Project	For VP8 Encoder: Max (DBLKFilterLevel for Segment0, DBLKFilterLevel for Segment1, DBLKFilterLevel for Segment2, DBLKFilterLevel for Segment3) + Max (RefLFDelta0, RefLFDelta1, RefLFDelta2, RefLFDelta3) + Max (ModeLFDelta0, ModeLFDelta1, ModeLFDelta2, ModeLFDelta3) < 128	CHV, BSW
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35 <b>Project:</b> CHV, BSW	31:0	<p><b>Segmentation ID Stream Base Address</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Decoder Only</td> </tr> <tr> <td>Format:</td> <td>StreamAddress[31:0] 64 bytes linear aligned buffer</td> </tr> </table> <p>It is specified when <b>SegmentationIDStreamInEnable</b> or <b>SegmentationIDStreamOutEnable</b> is specified.</p> <p style="text-align: center;"><b>Programming Notes</b></p> <p>Each cache has only 8 bits for 4 segmentation ID from 4 continuous MBs.</p>	Project:	CHV, BSW	Exists If:	//Decoder Only	Format:	StreamAddress[31:0] 64 bytes linear aligned buffer		
Project:	CHV, BSW									
Exists If:	//Decoder Only									
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36 <b>Project:</b> CHV, BSW	31:16	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Decoder Only</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Exists If:	//Decoder Only	Format:	MBZ		
Project:	CHV, BSW									
Exists If:	//Decoder Only									
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	15:0	<p><b>Segmentation ID Stream Base Address [47:32]</b></p>								

<b>MFX_VP8_PIC_STATE</b>								
		<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Decoder Only</td> </tr> </table> <p>This field is for the upper range of <b>Segmentation ID Stream Base Address</b></p>	Project:	CHV, BSW	Exists If:	//Decoder Only		
Project:	CHV, BSW							
Exists If:	//Decoder Only							
37 <b>Project:</b> CHV, BSW	31:15	<b>Reserved</b>						
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	14:13	<b>Reserved</b>						
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Exists If:	//Decoder Only							
Format:	MBZ							
12:11	<b>Reserved</b>							
	<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Decoder Only</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Exists If:	//Decoder Only	Format:	MBZ	
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Exists If:	//Decoder Only							
Format:	MBZ							
10:9	<b>Reserved</b>							
	<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ			
Project:	CHV, BSW							
Format:	MBZ							
8:7	<b>Segmentation ID Stream - Arbitration Priority Control</b>							
	<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Decoder Only</td> </tr> <tr> <td>Format:</td> <td>U2</td> </tr> </table>	Project:	CHV, BSW	Exists If:	//Decoder Only	Format:	U2	
	Project:	CHV, BSW						
	Exists If:	//Decoder Only						
	Format:	U2						
	This field controls the priority of arbitration used in the GAC/GAM pipeline for this surface.							
	<b>Value</b>	<b>Name</b>						
00b	Highest priority							
01b	Second highest priority							
10b	Third highest priority							
11b	Lowest priority							
6:5	<b>Memory Type: LLC/eLLC Cacheability Control (LeLLCCC) for Segmentation ID Stream Base Address</b>							
	<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Exists If:</td> <td>//Decoder Only</td> </tr> </table>	Project:	CHV, BSW	Exists If:	//Decoder Only			
	Project:	CHV, BSW						
	Exists If:	//Decoder Only						
This is the field used in GT interface block to determine what type of access need to be generated to uncore. For the cases where the LeLLCCC is set, cacheable transaction are generated to enable LLC usage for particular stream.								
<b>Value</b>	<b>Name</b>	<b>Description</b>						

<b>MFX_VP8_PIC_STATE</b>		
	00b	Use Cacheability Controls from page table
	01b	UC Uncacheable - non-cacheable
	10b	WT Writethrough
	11b	WB Writeback
4:3	<b>Target Cache (TC) Segmentation ID Stream Base Address</b>	
	Project:	CHV, BSW
	Exists If:	//Decoder Only
	<p>This field controls the L3\$, LLC and eLLC (eDRAM) cacheability for a given surface. Setting of "00" points to PTE settings which defaults to eDRAM (when present). If no eDRAM, the access will be allocated to LLC. Setting of "01", allocates into LLC and victimizes the line to eDRAM. Setting of "10" allows the line to be allocated in either LLC or eDRAM. Setting of "11" is the only option for a memory access to be allocated in L3\$ as well as LLC/eLLC</p> <p>00b: eLLC Only ("00" setting points TC selection to PTE which defaults to eLLC)                      01b: LLC Only (Works at the allocation time, later victimization from LLC downgrades the line to eLLC if present).                      10b: LLC/eLLC Allowed.                      11b: L3, LLC, eLLC Allowed.</p> <p><b>Errata CHV:A-E (FIXED BY:G0 Stepping):</b>                      For all system that does NOT use SVM (i.e. coherent L3\$ surfaces), back snoops from LLC has to be disabled (<b>Dis_GtCvUpdtOnRd = "1"</b>). Then target Cache settings can be programmed as POR requirements of L3/LLC/eDRAM caching.                      For all systems that does use SVM (i.e. coherent L3\$ surfaces), the recommended setting would be "00" in target cache settings. In case of L3 surfaces, the performance has to be tuned between "00" and "11" setting based on the benefits of L3 caching outweighing the degradation of backsnoops.                      Post G0-stepping, the above w/a for coherent L3\$ surfaces is not needed.</p>	
	<b>Value</b>	<b>Name</b>
	00b	eLLC Only - not snooped in GT
	01b	LLC Only
	10b	LLC/eLLC Allowed
	11b	L3, LLC, eLLC Allowed
2	<b>Reserved</b>	
1:0	<b>Age for QUADLRU (AGE) Segmentation ID Stream Base Address</b>	
	Project:	CHV, BSW
	Exists If:	//Decoder Only
	<p>This field allows the selection of AGE parameter for a given surface in LLC or eLLC. If a particular allocation is done at youngest age ("0,1,2") it tends to stay longer in the cache. This option is given to GFX software to be able to decide which surfaces are more likely to generate</p>	

### MFX\_VP8\_PIC\_STATE

HITs, hence need to be replaced least often in caches.

Value	Name
11b	Good chance of generating hits.
10b	Next good chance of generating hits
01b	Decent chance of generating hits
00b	Poor chance of generating hits

## MFX\_WAIT

<b>MFX_WAIT</b>			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	1		
<p>This command can be considered the same as an MI_NOOP except that the command parser will not parse the next command until the following happens</p> <ul style="list-style-type: none"> <li>• <b>AVC or VC1 BSD mode:</b> The command will stall the parser until completion of the BSD object</li> <li>• <b>IT, encoder, and MPEG2 BSD mode:</b> The command will stall the parser until the object package is sent down the pipeline. This command should be used to ensure the preemption enable window occurs during the time the object command is being executed down the pipeline.</li> </ul>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	03h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	<b>Command Subtype</b>	
		Default Value:	01h MFX_SINGLE_DW
		Format:	OpCode
	26:16	<b>Sub-Opcode</b>	
		Default Value:	0h MFX_WAIT
		Format:	OpCode
	15:10	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	9	<b>Reserved</b>	
	8	<b>MFX Sync Control Flag</b> If set, VCS will stall the parser until all prior MFX objects are completed down the MFX pipeline	
7:6	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
5:0	<b>DWord Length</b>		
	Default Value:	0h Excludes DWord (0,1)	
	Project:	All	
	Format:	=n	
		Total Length - 2	

## MI\_ARB\_CHECK

<b>MI_ARB_CHECK</b>			
Project:	CHV, BSW		
Source:	VideoEnhancementCS		
Length Bias:	1		
Description			
<p>The MI_ARB_CHECK is used to check for a change in arbitration. If executed as part of a Ring Buffer the command checks the UHPTR valid bit and if set the head of the ring will jump to the value of the head pointer programmed in the UHPTR.</p>			
Programming Notes			
<p>This instruction cannot be placed in a batch buffer.</p>			
<p>If execlist is enabled, there is a pending execution list and this command is parsed, then the command streamer will preempt the current context and start executing the new execution list.</p>			
DWord	Bit	Description	
0	31:29	<b>MI Instruction Type</b>	
		Default Value:	0h MI_INSTRUCTION
		Format:	OpCode
	28:23	<b>MI Instruction Opcode</b>	
		Default Value:	05h MI_ARB_CHECK
		Format:	OpCode
	22:0	<b>Reserved</b>	
		Project:	All
		Format:	MBZ



## MI\_ARB\_CHECK

<b>MI_ARB_CHECK</b>		
Project:	CHV, BSW	
Source:	BlitterCS	
Length Bias:	1	
Description		Project
The MI_ARB_CHECK is used to check for a change in arbitration. If executed as part of a Ring Buffer the command checks the UHPTR valid bit and if set the head of the ring will jump to the value of the head pointer programmed in the UHPTR.		
Programming Notes		Project
This instruction cannot be placed in a batch buffer.		
If execlist is enabled, there is a pending execution list and this command is parsed, then the command streamer will preempt the current context and start executing the new execution list.		CHV, BSW
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 0h MI_INSTRUCTION
		Format: OpCode
	28:23	<b>MI Command Opcode</b>
		Default Value: 05h MI_ARB_CHECK
		Format: OpCode
	22:0	<b>Reserved</b>
		Format: MBZ

## MI\_ARB\_CHECK

<b>MI_ARB_CHECK</b>		
Project:	CHV, BSW	
Source:	RenderCS	
Length Bias:	1	
Description		
<p>The MI_ARB_CHECK instruction is used to check the ring buffer double buffered head pointer (register UHPTR). This instruction can be used to pre-empt the current execution of the ring buffer. Note that the valid bit in the updated head pointer register needs to be set for the command streamer to be pre-empted.</p>		
Programming Notes		
<p>Ring Buffer mode of scheduling:</p> <ul style="list-style-type: none"> <li>The current head pointer is loaded with the updated head pointer register independent of the location of the updated head.</li> <li>If the current head pointer and the updated head pointer register are equal, hardware will automatically reset the valid bit corresponding to the UHPTR.</li> <li>For pre-emption, the wrap count in the ring buffer head register is no longer maintained by hardware. The hardware updates the wrap count to the value in the UHPTR register.</li> </ul> <p>Execlist mode of scheduling: MI_ARB_CHECK will be used to indicate a command boundary on which Preemption will be honored by Command Streamer in the execlist mode of operation. UHPTR is ignored when processing MI_ARB_CHECK in execlist mode.</p> <p>This instruction can be in either a ring buffer or batch buffer.</p> <p>MI_ARB_CHECK command must not be programmed in INDIRECT_CTX and BB_PER_CTX_PTR buffers.</p>		
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 0h MI_COMMAND
	Format: OpCode	
	28:23	<b>MI Command Opcode</b>
		Default Value: 05h MI_ARB_CHECK
	Format: OpCode	
22:0	<b>Reserved</b>	
	Format: MBZ	

## MI\_ARB\_CHECK

<b>MI_ARB_CHECK</b>			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	1		
Description			
<p>The MI_ARB_CHECK is used to check for a change in arbitration. If executed as part of a Ring Buffer the command checks the UHPTR valid bit and if set the head of the ring will jump to the value of the head pointer programmed in the UHPTR.</p>			
Programming Notes			
<p>This instruction cannot be placed in a batch buffer.</p>			
<p>If execlist is enabled, there is a pending execution list and this command is parsed, then the command streamer will preempt the current context and start executing the new execution list.</p>			
DWord	Bit	Description	
0	31:29	<b>MI Instruction Type</b>	
		Default Value:	0h MI_INSTRUCTION
		Format:	OpCode
	28:23	<b>MI Instruction Opcode</b>	
		Default Value:	05h MI_ARB_CHECK
		Format:	OpCode
	22:0	<b>Reserved</b>	
		Format:	MBZ

## MI\_ARB\_ON\_OFF

<b>MI_ARB_ON_OFF</b>						
Project:	CHV, BSW					
Source:	CommandStreamer					
Length Bias:	1					
<p>The MI_ARB_ON_OFF instruction is used to disable/enable context switching. This instruction can be used to prevent submission of a new execlist from interrupting a command sequence, however lite restore preemption is allowed with in the arbitration disabled command execution zone. Note that context switching will remain disabled until re-enabled through use of this command. This command will also prevent a switch in the case of waiting on events, running out of commands. These will effectively hang the device if allowed to occur while arbitration is off (context switching is disabled.) This command should always be used as an off-on pair with the sequence of instructions to be protected from context switch between MI_ARB_OFF and MI_ARB_ON. Software must use this arbitration control with caution since it has the potential to increase the response time of the Render Engine to pre-emption requests. This is a privileged command; it will not be effective (will be converted to a no-op) if executed from within a non-privileged batch buffer.</p>						
<p>Execution List Mode of Scheduling: The MI_ARB_ON_OFF instruction is used to disable/enable context switching. Context switching could be either due to preemption or un-succesfull wait for events or semaphore waits. This instruction can be used to prevent submission of a new execlist from interrupting a command sequence, however lite restore preemption is allowed with in the arbitration disabled command execution zone. Note that context switching will remain disabled until re-enabled through use of this command. This command will also prevent a switch in the case of waiting on events, running out of commands. These will effectively hang the device if allowed to occur while arbitration is off (context switching is disabled.)</p> <p>Ring Buffer Mode of Scheduling: The MI_ARB_ON_OFF instruction is used to disable preemption on the preemptable commands. SW can explicitly make section of commands in a command buffer non-preemptable by sandwiching them between ARB_OFF and ARB_ON, HW will ingore preemption request (UHPTR Valid) until arbitration is enabled.</p>						
<b>Programming Notes</b>						
<p>This command must be always be programmed in pairs of off/on in the same command dispatch. Sequence of instructions to be protected from cntext switch or preemption must be programmed between the MI_ARB_OFF and MI_ARB_ON. Software must use this arbitration control with caution since it has the potential to increase the response time of the Render Engine to pre-emption requests. This is a privileged command; it will not be effective (will be converted to a no-op) if executed from within a non-privileged batch buffer.</p>						
<p>HW doesn't treat Arbitration Disabled as equivalent to "Inhibit Synchronous Context Switch" set in CTXT_SR_CTL register. Power management optimizations (RDOP on WT4EVT) available on setting "Inhibit Synchronous Context Switch" are not enabled by default on Arbitration Disabled. SW must explicitly program "Inhibit Synchronous Switch" when Arbitration Disabled to enable power management optimizations.</p>						
DWord	Bit	Description				
0	31:29	<p><b>Command Type</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Default Value:</td> <td>0h MI_COMMAND</td> </tr> <tr> <td>Format:</td> <td>OpCode</td> </tr> </table>	Default Value:	0h MI_COMMAND	Format:	OpCode
Default Value:	0h MI_COMMAND					
Format:	OpCode					

<b>MI_ARB_ON_OFF</b>						
	28:23	<b>MI Command Opcode</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Default Value:</td> <td>08h MI_ARB_ON_OFF</td> </tr> <tr> <td>Format:</td> <td>OpCode</td> </tr> </table>	Default Value:	08h MI_ARB_ON_OFF	Format:	OpCode
	Default Value:	08h MI_ARB_ON_OFF				
	Format:	OpCode				
22:1	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ			
Format:	MBZ					
0	<b>Arbitration Enable</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables or disables context switches due to pre-emption (a new execlist).</p>	Format:	Enable			
Format:	Enable					

# MI\_ATOMIC

<b>MI_ATOMIC</b>											
Project:	CHV, BSW										
Source:	PRM										
Length Bias:	2										
<b>Description</b>											
<p>MI_ATOMIC is used to carry atomic operation on data in graphics memory. Atomic operations are supported on data granularity of 4B, 8B and 16B. The atomic operation leads to a read-modify-write operation on the data in graphics memory with the option of returning value. The data in graphics memory is modified by doing arithmetic and logical operation with the inline/indirect data provided with the MI_ATOMIC command. Inline/Indirect provided in the command can be one or two operands based on the atomic operation. Ex: Atomic-Compare operation needs two operands while Atomic-Add operation needs single operand and Atomic-increment requires no operand. Refer Vol1i L3 URB [CHV, BSW] B-spec for detailed atomic operations supported. Atomic operations can be enabled to return value by setting "Return Data Control" field in the command, return data is stored to CS_GPR registers. CS_GPR4/5 registers are updated with memory Return Data based on the "Data Size". Each GPR register is qword in size and occupies two MMIO registers. Note: Any references to CS_GPR registers in the command should be understood as the CS_GPR registers belonging to the corresponding engines *CS_GPR registers.</p> <table border="1"> <thead> <tr> <th>Engine Name</th> <th>Corresponding GPR Registers</th> </tr> </thead> <tbody> <tr> <td>RCS</td> <td>CS_GPR</td> </tr> <tr> <td>BCS</td> <td>BCS_GPR</td> </tr> <tr> <td>VCS</td> <td>VCS_GPR</td> </tr> <tr> <td>VECS</td> <td>VECS_GPR</td> </tr> </tbody> </table> <p><b>Indirect Source Operands:</b>            Operand1 is sourced from [CS_GPR1, CS_GPR0]            Operand2 is sourced from [CS_GPR3, CS_GPR2]            Read return Data is stored in [CS_GPR_5, CS_GPR4]</p> <p>When "Data Size" is QWORD or DWORD only CS_GPR4 (Qword) is updated with the qword data returned from memory. When the data size is OCTWORD CS_GPR4/5 are updated with the OCTWORD data returned from memory. CS_GPR4 is loaded with lower qword returned from memory and CS_GPR5 is loaded with upper qword returned from memory.</p>		Engine Name	Corresponding GPR Registers	RCS	CS_GPR	BCS	BCS_GPR	VCS	VCS_GPR	VECS	VECS_GPR
Engine Name	Corresponding GPR Registers										
RCS	CS_GPR										
BCS	BCS_GPR										
VCS	VCS_GPR										
VECS	VECS_GPR										
<b>Programming Notes</b>											
<ul style="list-style-type: none"> <li>When Inline Data mode is not set, Dwords 3..10 must not be included as part of the command. Dword Length field in the header must be programmed accordingly.</li> <li>When Inline Data Mode is set, Dwords 3..10 must be included based on the Data Size field of the header. Both Operand-1 and Operand-2 dwords must be programmed based on the Data Size field. Operand-2 must be programmed to 0x0 if the atomic operation doesn't require it. Dword Length field in the header must be programmed accordingly.</li> </ul>											

DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	2Fh MI_ATOMIC
		Format:	OpCode
	22	<b>Memory Type</b>	
		This bit will be ignored and treated as if clear when executing from a non-privileged batch buffer. It is allowed for this bit to be clear when executing this command from a privileged (secure) batch buffer. This bit must be 1 if the <b>Per Process GTT Enable</b> bit is clear.	
		<b>Value</b>	<b>Name</b>
		0h	Per Process Graphics Address
1h	Global Graphics Address	This command will use the global GTT to translate the Address and this command must be executing from a privileged (secure) batch buffer.	
21	<b>Reserved</b>		
	Source:	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS	
	Format:	MBZ	
21	<b>Post-Sync Operation</b>		
	Source:	RenderCS	
	<b>Value</b>	<b>Name</b>	
	0h	No Post Sync Operation	Command is executed as usual.
	1h	Post Sync Operation	MI_ATOMIC command is executed as a pipelined PIPE_CONTROL flush command with Atomics operation as post sync operation. Flush completion only guarantees the workload prior to this command is pushed till Windower unit and completion of any outstanding flushes issued prior to this command. When this bit set following restriction apply to atomic operation: <ul style="list-style-type: none"> <li>Non-Compare atomic operations are supported on data granularity of 4B and 8B. DW3 is the lower dword of the operand and DW4 is the upper dword of the operand for the atomic operation.</li> <li>Compare atomic operations are supported on data granularity of 4B. DW3 is Operand-0 and DW4 is Operand-1 for the atomic operation.</li> <li>Atomic operations to GGTT/PPGTT memory surface are supported.</li> </ul>

<b>MI_ATOMIC</b>																	
		<ul style="list-style-type: none"> <li>• Only Inline data mode for atomic operand is supported, no support for indirect data mode.</li> <li>• No support for Return Data Control functionality.</li> <li>• No support for atomic operations on data granularity of 16B.</li> <li>• No support for compare atomic operations on data granularity of 8B.</li> </ul>															
<b>Programming Notes</b>																	
Any desired pipeline flush operation can be achieved by programming PIPE_CONTROL command prior to this command.																	
AWhen this bit is set Command Streamer sends a flush down the pipe and the atomic operation is saved as post sync operation. Command streamer goes on executing the following commands. Atomic operation saved as post sync operation is executed at some point later on completion of corresponding flush issued.																	
AWhen this bit is set atomic semaphore signal operation will be out of order with rest of the MI commands programmed in the ring buffer or batch buffer, it will be in order with respect to the post sync operations resulting due to PIPE_CONTROL command.																	
This bit must not be set due to known HW issues. OR "Post Sync Operation" feature in MI_ATOMIC can be enabled provided "CS Stall" bit is always set in all PIPE_CONTROL commands programmed with "Post Sync Operation" set to "Report Time Stamp" or "Report PS Depth Count".																	
<b>Workaround</b>																	
Workaround: "Post Sync Operation" bit must not be set when MI_ATOMIC command is programmed by GPGPU and MEDIA workloads (i.e when PIPELINE_SELECT command is set to GPGPU or MEDIA). This is to WA FFDOP CG issue.																	
20:1	<b>Data Size</b>																
9		This field indicates the size of the operand in dword/qword/octword on which atomic operation will be performed. Data size must match with the Atomic Opcode. Operation Data size could be 4B, 8B or 16B															
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>DWORD</td> <td>Operand size used by Atomic Operation is DWORD.</td> </tr> <tr> <td>1h</td> <td>QWORD</td> <td>Operand Size used by Atomic Operation is QWORD.</td> </tr> <tr> <td>2h</td> <td>OCTWORD</td> <td>Operand Size used by Atomic Operation is OCTWORD.</td> </tr> <tr> <td>3h</td> <td>RESERVED</td> <td></td> </tr> </tbody> </table>	Value	Name	Description	0h	DWORD	Operand size used by Atomic Operation is DWORD.	1h	QWORD	Operand Size used by Atomic Operation is QWORD.	2h	OCTWORD	Operand Size used by Atomic Operation is OCTWORD.	3h	RESERVED	
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3h	RESERVED																
18	<b>Inline Data</b>																
		This bit when set indicates the source operands are provided in line within the command. When reset the source operands are in CS_GPR registers.															
<b>Programming Notes</b>																	



<b>MI_ATOMIC</b>													
		CS_GPR registers must be programmed with appropriate values before issuing MI_ATOMIC command with this field reset.											
17	<b>CS STALL</b>	<p>This bit when set command stream waits for completion of this command before executing the next command.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th colspan="2" style="text-align: center;">Programming Notes</th> <th style="text-align: center;">Source</th> </tr> </thead> <tbody> <tr> <td style="width: 80%;">Render Command Streamer Only: CS will not guarantee atomic operation to be complete upon setting this bit along with Post Sync Operation set. When Post Sync Operation is set, this bit has no significance.</td> <td></td> <td style="text-align: center;">RenderCS</td> </tr> </tbody> </table> <table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">Workaround</th> </tr> </thead> <tbody> <tr> <td>Workaround When CS STALL bit is set, Return Data Control must also be set in MI_ATOMIC command.</td> </tr> </tbody> </table>	Programming Notes		Source	Render Command Streamer Only: CS will not guarantee atomic operation to be complete upon setting this bit along with Post Sync Operation set. When Post Sync Operation is set, this bit has no significance.		RenderCS	Workaround	Workaround When CS STALL bit is set, Return Data Control must also be set in MI_ATOMIC command.			
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16	<b>Return Data Control</b>	<table border="1" style="width: 100%;"> <tr> <td style="width: 15%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Source:</td> <td>RenderCS, BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS</td> </tr> </table> <table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td>When "Data Size" is QWORD or DWORD only CS_GPR4 (Qword) is updated with the qword data returned from memory. When the data size is OCTWORD CS_GPR4/5 are updated with the OCTWORD data returned from memory. CS_GPR4 is loaded with lower qword returned from memory and CS_GPR5 is loaded with upper qword returned from memory</td> </tr> </tbody> </table> <table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">Workaround</th> </tr> </thead> <tbody> <tr> <td>Workaround: When Return Data Control bit is set, CS STALL must also be set in MI_ATOMIC command.</td> </tr> </tbody> </table>	Project:	CHV, BSW	Source:	RenderCS, BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS	Description	When "Data Size" is QWORD or DWORD only CS_GPR4 (Qword) is updated with the qword data returned from memory. When the data size is OCTWORD CS_GPR4/5 are updated with the OCTWORD data returned from memory. CS_GPR4 is loaded with lower qword returned from memory and CS_GPR5 is loaded with upper qword returned from memory	Workaround	Workaround: When Return Data Control bit is set, CS STALL must also be set in MI_ATOMIC command.			
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15:8	<b>ATOMIC OPCODE</b>	<p>This field selects the kind of atomic operation to be performed. Refer Vol1i L3 URB [CHV, BSW] B-spec for atomic opcode corresponding to an atomic operation.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">Programming Notes</th> </tr> </thead> <tbody> <tr> <td>Atomic Opcode must not be set to 0x00 (no-atomic).</td> </tr> </tbody> </table>	Programming Notes	Atomic Opcode must not be set to 0x00 (no-atomic).									
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7:0	<b>DWord Length</b>	<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="text-align: center;">=n</td> </tr> </table> <p>Total Length - 2. Excludes DWord (0,1).</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Exists If</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">1h</td> <td style="text-align: center;"><b>[Default]</b></td> <td style="text-align: center;">([Inline Data]= =0)</td> </tr> <tr> <td style="text-align: center;">9h</td> <td></td> <td style="text-align: center;">([Inline Data]= =1)</td> </tr> </tbody> </table>	Format:	=n	Value	Name	Exists If	1h	<b>[Default]</b>	([Inline Data]= =0)	9h		([Inline Data]= =1)
Format:	=n												
Value	Name	Exists If											
1h	<b>[Default]</b>	([Inline Data]= =0)											
9h		([Inline Data]= =1)											
1	31:2	<b>Memory Address</b>											

<b>MI_ATOMIC</b>														
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[31:2]</td> </tr> <tr> <td colspan="2"> <p>This field contains the graphics memory address of the data on which atomic operation has to be performed. Atomic operation can be performed on data granularity of 4B, 8B or 16B and hence the Address has to be correspondingly aligned to 4B,8B or 16B respectively.</p> </td> </tr> <tr> <td colspan="2" style="text-align: center;"><b>Programming Notes</b></td> </tr> <tr> <td>Memory Address must be qword aligned for all dword atomic operations. Upper Dword of the memory location should be initialized to 0x0.</td> <td style="text-align: center;"><b>Project</b></td> </tr> <tr> <td></td> <td style="text-align: center;">CHV, BSW</td> </tr> </table>	Project:	All	Format:	GraphicsAddress[31:2]	<p>This field contains the graphics memory address of the data on which atomic operation has to be performed. Atomic operation can be performed on data granularity of 4B, 8B or 16B and hence the Address has to be correspondingly aligned to 4B,8B or 16B respectively.</p>		<b>Programming Notes</b>		Memory Address must be qword aligned for all dword atomic operations. Upper Dword of the memory location should be initialized to 0x0.	<b>Project</b>		CHV, BSW
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	1:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ										
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2	31:1	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ										
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6	<p><b>Memory Address High</b> This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space.</p>													
3	31:0	<p><b>Operand1 Data Dword 0</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Dword0 of Operand1 when Inline Data mode is set.</p>	Format:	U32										
		Format:	U32											
<p><b>Operand2 Data Dword 0</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Dword0 of Operand2 when Inline Data mode is set.</p>	Format:	U32												
Format:	U32													
5	31:0	<p><b>Operand1 Data Dword 1</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Dword1 of Operand1 when Inline Data mode is set.</p>	Format:	U32										
		Format:	U32											
<p><b>Operand2 Data Dword 1</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Dword1 of Operand2 when Inline Data mode is set.</p>	Format:	U32												
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7	31:0	<p><b>Operand1 Data Dword 2</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Dword2 of Operand1 when Inline Data mode is set.</p>	Format:	U32										
		Format:	U32											
<p><b>Operand2 Data Dword 2</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Dword2 of Operand2 when Inline Data mode is set.</p>	Format:	U32												
Format:	U32													

<b>MI_ATOMIC</b>		
9	31:0	<b>Operand1 Data Dword 3</b> Format: <span style="float: right;">U32</span> Dword3 of Operand1 when Inline Data mode is set.
		<b>Operand2 Data Dword 3</b> Format: <span style="float: right;">U32</span> Dword3 of Operand2 when Inline Data mode is set.

## MI\_BATCH\_BUFFER\_END

MI_BATCH_BUFFER_END			
Project:	CHV, BSW		
Source:	VideoEnhancementCS		
Length Bias:	1		
The MI_BATCH_BUFFER_END command is used to terminate the execution of commands stored in a batch buffer initiated using a MI_BATCH_BUFFER_START command.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	0Ah MI_BATCH+_BUFFER_END
		Format:	OpCode
	22:0	<b>Reserved</b>	
		Project:	All
		Format:	MBZ

## MI\_BATCH\_BUFFER\_END

MI_BATCH_BUFFER_END		
Project:	CHV, BSW	
Source:	BlitterCS	
Length Bias:	1	
The MI_BATCH_BUFFER_END command is used to terminate the execution of commands stored in a batch buffer initiated using a MI_BATCH_BUFFER_START command.		
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 0h MI_COMMAND
	28:23	<b>MI Command Opcode</b>
		Default Value: 0Ah MI_BATCH_BUFFER_END
	22:0	<b>Reserved</b>
		Project:
Format:		MBZ

## MI\_BATCH\_BUFFER\_END

MI_BATCH_BUFFER_END			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	1		
The MI_BATCH_BUFFER_END command is used to terminate the execution of commands stored in a batch buffer initiated using a MI_BATCH_BUFFER_START command.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	0Ah MI_BATCH_BUFFER_END
		Format:	OpCode
	22:0	<b>Reserved</b>	
		Format:	MBZ

## MI\_BATCH\_BUFFER\_END

MI_BATCH_BUFFER_END			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	1		
The MI_BATCH_BUFFER_END command is used to terminate the execution of commands stored in a batch buffer initiated using a MI_BATCH_BUFFER_START command.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	0Ah MI_BATCH+_BUFFER_END
		Format:	OpCode
	22:0	<b>Reserved</b>	
		Format:	MBZ

## MI\_BATCH\_BUFFER\_START

<b>MI_BATCH_BUFFER_START</b>				
Project:	CHV, BSW			
Source:	RenderCS			
Length Bias:	2			
<p>The MI_BATCH_BUFFER_START command is used to initiate the execution of commands stored in a <i>batch</i> buffer. For restrictions on the location of batch buffers, see Batch Buffers in the Device Programming Interface chapter of <i>MI Functions</i>. The batch buffer can be specified as privileged or non-privileged, determining the operations considered valid when initiated from within the buffer and any attached (chained) batch buffers. See Batch Buffer Protection in the Device Programming Interface chapter of <i>MI Functions</i>.</p>				
Programming Notes				
<ul style="list-style-type: none"> <li>A batch buffer initiated with this command must end either with a MI_BATCH_BUFFER_END command or by chaining to another batch buffer with an MI_BATCH_BUFFER_START command.</li> <li>It is essential that the address location beyond the current page be populated inside the GTT. HW performs over-fetch of the command addresses and any over-fetch requires a valid TLB entry. A single extra page beyond the batch buffer is sufficient.</li> </ul>				
DWord	Bit	Description		
0	31:29	<b>Command Type</b>		
		Default Value:	0h MI_COMMAND	
		Format:	OpCode	
28:23		<b>MI Command Opcode</b>		
		Default Value:	31h MI_BATCH_BUFFER_START	
		Format:	OpCode	
22		<b>2nd Level Batch Buffer</b>		
		<p>The command streamer contains three storage elements; one for the ring head address, one for the batch head address, and one for the 2nd level batch head address. When performing batch buffer chaining, hardware simply updates the head pointer of the 1st level batch address storage. There is no stack in hardware. When this bit is set, hardware uses the 2nd level batch head address storage element. Upon MI_BATCH_BUFFER_END, it will automatically return to the 1st (traditional) level batch buffer address. this allows hardware to mimic a simple 3-level stack.</p>		
		Value	Name	Description
		0h	1st level batch	Place the batch buffer address in the 1st (traditional) level batch address storage element.
1h	2nd level batch	Place the batch buffer address in the 2nd-level batch address storage element.		



<b>MI_BATCH_BUFFER_START</b>		
<b>Programming Notes</b>		
Within a second level batch buffer there can't be any chained batch buffers. MI_BATCH_BUFFER_START command is not allowed inside a second level batch buffer.		
21:17	<b>Reserved</b>	
	Format:	MBZ
16	<b>Add Offset Enable</b>	
	Format:	Enable
If this bit is set then the value stored in the BB_OFFSET MMIO register will be added to the Batch Buffer Start Address and the summation will be used as the address to fetch from memory. <b>Specific to the render command stream only.</b>		
15	<b>Predication Enable</b>	
This bit is used to enable predication of this command. If this bit is set and Bit 0 of the Predicate Result-1 register is clear, this command is ignored. Otherwise the command is performed normally. <b>Specific to the Render command stream only.</b>		
14:12	<b>Reserved</b>	
11	<b>Reserved</b>	
10	<b>Resource Streamer Enable</b>	
	Format:	Enable
When this bit is set, the Resource Streamer will execute the batch buffer. When this bit is clear the Resource Streamer will not execute the batch buffer. <b>Specific to the Render command stream only.</b>		
9	<b>Reserved</b>	
8	<b>Address Space Indicator</b>	
Batch buffers accessed via PPGTT are considered as non-privileged. Certain operations (e.g., MI_STORE_DATA_IMM commands to GGTT memory) are prohibited within non-privileged buffers. More details mentioned in User Mode Privileged command section. When MI_BATCH_BUFFER_START command is executed from within a batch buffer (i.e., is a "chained" or "second level" batch buffer command), the current active batch buffer's "Address Space Indicator" and this field determine the "Address Space Indicator" of the next buffer in the chain.		
<ul style="list-style-type: none"> <li>Chained or Second level batch buffer can be in GGTT or PPGTT if the parent batch buffer is in GGTT.</li> <li>Chained or Second level batch buffer can only be in PPGTT if the parent batch buffer is in PPGTT. This is enforced by Hardware.</li> </ul>		
<b>Value</b>	<b>Name</b>	<b>Description</b>
0h	GGTT	This batch buffer is located in GGTT memory and is privileged.
1h	PPGTT	This batch buffer is located in PPGTT memory and is Non-Privileged.
<b>Programming Notes</b>		
This field must be '0' unless the Per-Process GTT Enable is '1'		

<b>MI_BATCH_BUFFER_START</b>				
	7:0	<b>DWord Length</b>		
		<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1h</td> </tr> <tr> <td>Format:</td> <td>=n</td> </tr> </table> <p>Total - Bias. Excludes DWord (0,1).</p>	Default Value:	1h
Default Value:	1h			
Format:	=n			
1	31:2	<b>Batch Buffer Start Address</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 20%;">Format:</td> <td>GraphicsAddress[31:2]BatchBuffer</td> </tr> </table> <p>This field specifies Bits 31:2 of the starting address of the batch buffer.</p>	Format:	GraphicsAddress[31:2]BatchBuffer
	Format:	GraphicsAddress[31:2]BatchBuffer		
1:0	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ			
2	31:16	<b>Reserved</b>		
	15:0	<b>Batch Buffer Start Address High</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 20%;">Format:</td> <td>GraphicsAddress[47:32]BatchBuffer</td> </tr> </table> <p>This field specifies the 4GB aligned base address of Gfx 4GB virtual address spece within the hosts 64-bit virtual address space.</p>	Format:	GraphicsAddress[47:32]BatchBuffer
Format:	GraphicsAddress[47:32]BatchBuffer			

## MI\_BATCH\_BUFFER\_START

MI_BATCH_BUFFER_START				
Project:	CHV, BSW			
Source:	VideoEnhancementCS			
Length Bias:	2			
<p>The MI_BATCH_BUFFER_START command is used to initiate the execution of commands stored in a <i>batch buffer</i>. For restrictions on the location of batch buffers, see Batch Buffers in the Device Programming Interface chapter of <i>MI Functions</i>.</p> <p>The batch buffer can be specified as secure or non-secure, determining the operations considered valid when initiated from within the buffer and any attached (chained) batch buffers. See Batch Buffer Protection in the Device Programming Interface chapter of <i>MI Functions</i>.</p>				
DWord	Bit	Description		
0	31:29	<b>Command Type</b>		
		Default Value:	0h MI_COMMAND	
		Format:	OpCode	
	28:23	<b>MI Command Opcode</b>		
		Default Value:	31h MI_BATCH_BUFFER_START	
		Format:	OpCode	
	22	<b>2nd Level Batch Buffer</b>		
		<p>The command streamer contains 3 storage elements; 1 for the ring head address, 1 for the batch head address, and 1 for the 2nd level batch head address. When performing batch buffer chaining, hardware simply updates the head pointer of the 1st level batch address storage. There is no stack in hardware.</p> <p>When this bit is set, hardware uses the 2nd level batch head address storage element. Upon MI_BATCH_BUFFER_END, it will automatically return to the 1st (traditional) level batch buffer address. this allows hardware to mimic a simple 3 level stack.</p>		
		<b>Value</b>	<b>Name</b>	<b>Description</b>
		0h	1st level batch	Place the batch buffer address in the 1st (traditional) level batch address storage element
1h		2nd level batch	Place the batch buffer address in the 2nd level batch address storage element	
21:13	<b>Reserved</b>			
	Format:	MBZ		
12	<b>Reserved</b>			
11:9	<b>Reserved</b>			
	Format:	MBZ		
8	<b>Address Space Indicator</b>			
	Project:	CHV, BSW		
Batch buffers accessed via PPGTT are considered as non-privileged. Certain operations (e.g.,				

<b>MI_BATCH_BUFFER_START</b>											
		<p>MI_STORE_DATA_IMM commands to GGTT memory) are prohibited within non-privileged buffers. More details mentioned in User Mode Privileged command section. When MI_BATCH_BUFFER_START command is executed from within a batch buffer (i.e., is a "chained" or "second level" batch buffer command), the current active batch buffer's "Address Space Indicator" and this field determine the "Address Space Indicator" of the next buffer in the chain.</p> <ul style="list-style-type: none"> <li>• Chained or Second level batch buffer can be in GGTT or PPGTT if the parent batch buffer is in GGTT.</li> <li>• Chained or Second level batch buffer can only be in PPGTT if the parent batch buffer is in PPGTT. This is enforced by Hardware.</li> </ul> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>GGTT</td> <td>This batch buffer is located in GGTT memory and is privileged.</td> </tr> <tr> <td>1h</td> <td>PPGTT</td> <td>This batch buffer is located in PPGTT memory and is Non-Privileged.</td> </tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>This field must be '0' unless the Per-Process GTT Enable is '1'</p>	Value	Name	Description	0h	GGTT	This batch buffer is located in GGTT memory and is privileged.	1h	PPGTT	This batch buffer is located in PPGTT memory and is Non-Privileged.
Value	Name	Description									
0h	GGTT	This batch buffer is located in GGTT memory and is privileged.									
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	7:0	<p><b>DWord Length (Excludes D-Word 0,1) = 0</b></p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>1h</td> <td>Excludes DWord (0,1) [Default]</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Value	Name	Project	1h	Excludes DWord (0,1) [Default]	CHV, BSW			
Value	Name	Project									
1h	Excludes DWord (0,1) [Default]	CHV, BSW									
1	31:2	<p><b>Batch Buffer Start Address</b></p> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[31:2]</td> </tr> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <ul style="list-style-type: none"> <li>• A batch buffer initiated with this command must end either with a MI_BATCH_BUFFER_END command or by chaining to another batch buffer with an MI_BATCH_BUFFER_START command.</li> <li>• The selection of PPGTT vs. GGTT for the batch buffer is determined by the <b>Buffer Security Indicator</b> (bit 8).</li> </ul>	Format:	GraphicsAddress[31:2]							
Format:	GraphicsAddress[31:2]										
	1:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ							
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2 <b>Project:</b> CHV, BSW	31:16	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ					
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	Format:	MBZ									
15:0	<p><b>Batch Buffer Start Address High</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[47:32]BatchBuffer</td> </tr> </table> <p>This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space.</p>	Project:	CHV, BSW	Format:	GraphicsAddress[47:32]BatchBuffer						
Project:	CHV, BSW										
Format:	GraphicsAddress[47:32]BatchBuffer										

## MI\_BATCH\_BUFFER\_START

MI_BATCH_BUFFER_START													
Project:	CHV, BSW												
Source:	BlitterCS												
Length Bias:	2												
<p>The MI_BATCH_BUFFER_START command is used to initiate the execution of commands stored in a batch buffer. For restrictions on the location of batch buffers, see Batch Buffers in the Device Programming Interface chapter of MI Functions. The batch buffer can be specified as secure or non-secure, determining the operations considered valid when initiated from within the buffer and any attached (chained) batch buffers. See Batch Buffer Protection in the Device Programming Interface chapter of MI Functions.</p>													
Programming Notes													
<ul style="list-style-type: none"> <li>Batch buffers referenced with physical addresses must not extend beyond the end of the starting physical page (can't span physical pages). However, a batch buffer initiated using a physical address can chain to another buffer in another physical page.</li> <li>A batch buffer initiated with this command must end either with a MI_BATCH_BUFFER_END command or by chaining to another batch buffer with an MI_BATCH_BUFFER_START command.</li> </ul>													
DWord	Bit	Description											
0	31:29	<b>Command Type</b>											
		<table border="1"> <tr> <td>Default Value:</td> <td>0h MI_COMMAND</td> </tr> <tr> <td>Format:</td> <td>OpCode</td> </tr> </table>	Default Value:	0h MI_COMMAND	Format:	OpCode							
Default Value:	0h MI_COMMAND												
Format:	OpCode												
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		<table border="1"> <tr> <td>Default Value:</td> <td>31h MI_BATCH_BUFFER_START</td> </tr> <tr> <td>Format:</td> <td>OpCode</td> </tr> </table>	Default Value:	31h MI_BATCH_BUFFER_START	Format:	OpCode							
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Project:	CHV, BSW												
Value	Name	Description											
0h	1st level batch	Place the batch buffer address in the 1st (traditional) level batch address storage element											
1h	2nd level batch	Place the batch buffer address in the 2nd level batch address storage element											
	21:9	<b>Reserved</b>											

<b>MI_BATCH_BUFFER_START</b>														
8	<b>Address Space Indicator</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table> <p>Batch buffers accessed via PPGTT are considered as non-privileged. Certain operations (e.g., MI_STORE_DATA_IMM commands to GGTT memory) are prohibited within non-privileged buffers. More details mentioned in User Mode Privileged command section. When MI_BATCH_BUFFER_START command is executed from within a batch buffer (i.e., is a "chained" or "second level" batch buffer command), the current active batch buffer's "Address Space Indicator" and this field determine the "Address Space Indicator" of the next buffer in the chain.</p> <ul style="list-style-type: none"> <li>Chained or Second level batch buffer can be in GGTT or PPGTT if the parent batch buffer is in GGTT.</li> <li>Chained or Second level batch buffer can only be in PPGTT if the parent batch buffer is in PPGTT. This is enforced by Hardware.</li> </ul> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>GGTT</td> <td>This batch buffer is located in GGTT memory and is privileged.</td> </tr> <tr> <td>1h</td> <td>PPGTT</td> <td>This batch buffer is located in PPGTT memory and is Non-Privileged.</td> </tr> </tbody> </table> <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 10px;"> <thead> <tr> <th style="text-align: center; background-color: #e6f2ff;">Programming Notes</th> </tr> </thead> <tbody> <tr> <td>This field must be '0' unless the Per-Process GTT Enable is '1'</td> </tr> </tbody> </table>	Project:	CHV, BSW	Value	Name	Description	0h	GGTT	This batch buffer is located in GGTT memory and is privileged.	1h	PPGTT	This batch buffer is located in PPGTT memory and is Non-Privileged.	Programming Notes	This field must be '0' unless the Per-Process GTT Enable is '1'
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This field must be '0' unless the Per-Process GTT Enable is '1'														
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Format:	=n													
Value	Name	Project												
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1	31:2	<b>Batch Buffer Start Address</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[31:2]BatchBuffer</td> </tr> </table> <p>This field specifies Bits 31:2 of the starting address of the batch buffer.</p>	Format:	GraphicsAddress[31:2]BatchBuffer										
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1:0	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ											
Format:	MBZ													
2 <b>Project:</b> CHV, BSW	31:16	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ								
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Project:	CHV, BSW													
Format:	GraphicsAddress[47:32]BatchBuffer													

## MI\_BATCH\_BUFFER\_START

MI_BATCH_BUFFER_START			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>The MI_BATCH_BUFFER_START command is used to initiate the execution of commands stored in a batch buffer. For restrictions on the location of batch buffers, see Batch Buffers in the Device Programming Interface chapter of MI Functions. The batch buffer can be specified as secure or non-secure, determining the operations considered valid when initiated from within the buffer and any attached (chained) batch buffers. See Batch Buffer Protection in the Device Programming Interface chapter of MI Functions.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	31h MI_BATCH_BUFFER_START
		Format:	OpCode
	22	<b>2nd Level Batch Buffer</b>	
		Project:	CHV, BSW
		<p>The command streamer contains 3 storage elements; 1 for the ring head address, 1 for the batch head address, and 1 for the 2nd level batch head address. When performing batch buffer chaining, hardware simply updates the head pointer of the 1st level batch address storage. There is no stack in hardware. When this bit is set, hardware uses the 2nd level batch head address storage element. Upon MI_BATCH_BUFFER_END, it will automatically return to the 1st (traditional) level batch buffer address. this allows hardware to mimic a simple 3 level stack.</p>	
		Value	Name
0h		1st level batch	Place the batch buffer address in the 1st (traditional) level batch address storage element
1h		2nd level batch	Place the batch buffer address in the 2nd level batch address storage element
Programming Notes			
<ul style="list-style-type: none"> <li>2nd level batch buffer chaining is not supported.</li> </ul>			
21:10		<b>Reserved</b>	
		<b>Reserved</b>	
9	<b>Reserved</b>		

<b>MI_BATCH_BUFFER_START</b>											
	8	<p><b>Address Space Indicator</b></p> <p>Batch buffers accessed via PPGTT are considered as non-privileged. Certain operations (e.g., MI_STORE_DATA_IMM commands to GGTT memory) are prohibited within non-privileged buffers. More details mentioned in User Mode Privileged command section. When MI_BATCH_BUFFER_START command is executed from within a batch buffer (i.e., is a "chained" or "second level" batch buffer command), the current active batch buffer's "Address Space Indicator" and this field determine the "Address Space Indicator" of the next buffer in the chain.</p> <ul style="list-style-type: none"> <li>Chained or Second level batch buffer can be in GGTT or PPGTT if the parent batch buffer is in GGTT.</li> <li>Chained or Second level batch buffer can only be in PPGTT if the parent batch buffer is in PPGTT. This is enforced by Hardware.</li> </ul> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>GGTT</td> <td>This batch buffer is located in GGTT memory and is privileged.</td> </tr> <tr> <td>1h</td> <td>PPGTT</td> <td>This batch buffer is located in PPGTT memory and is Non-Privileged.</td> </tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>This field must be '0' unless the Per-Process GTT Enable is '1'.</p>	Value	Name	Description	0h	GGTT	This batch buffer is located in GGTT memory and is privileged.	1h	PPGTT	This batch buffer is located in PPGTT memory and is Non-Privileged.
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	1h	PPGTT	This batch buffer is located in PPGTT memory and is Non-Privileged.								
	7:0	<p><b>DWord Length</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 40%;">Format:</td> <td>=n Total Length - 2</td> </tr> </table> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 60%;">Name</th> <th style="width: 25%;">Project</th> </tr> </thead> <tbody> <tr> <td>1h</td> <td>Excludes DWord (0,1) <b>[Default]</b></td> <td>CHV, BSW</td> </tr> </tbody> </table>	Format:	=n Total Length - 2	Value	Name	Project	1h	Excludes DWord (0,1) <b>[Default]</b>	CHV, BSW	
Format:	=n Total Length - 2										
Value	Name	Project									
1h	Excludes DWord (0,1) <b>[Default]</b>	CHV, BSW									
1	31:2	<p><b>Batch Buffer Start Address</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 40%;">Format:</td> <td>GraphicsAddress[31:2]</td> </tr> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <ul style="list-style-type: none"> <li>A batch buffer initiated with this command must end either with a MI_BATCH_BUFFER_END command or by chaining to another batch buffer with an MI_BATCH_BUFFER_START command.</li> <li>The selection of PPGTT vs. GGTT for the batch buffer is determined by the Buffer Security Indicator (bit8).</li> </ul>	Format:	GraphicsAddress[31:2]							
Format:	GraphicsAddress[31:2]										
	1:0	<b>Reserved</b>									
2	31:16	<b>Reserved</b>									
<b>Project:</b> CHV, BSW	15:0	<p><b>Batch Buffer Start Address High</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 40%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[47:32]BatchBuffer</td> </tr> </table> <p>This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space.</p>	Project:	CHV, BSW	Format:	GraphicsAddress[47:32]BatchBuffer					
	Project:	CHV, BSW									
	Format:	GraphicsAddress[47:32]BatchBuffer									



## MI\_CLFLUSH

<b>MI_CLFLUSH</b>											
Project:	CHV, BSW										
Source:	RenderCS										
Length Bias:	2										
Flushes out the page given in the command out to system memory. This command is specific to the render engine and is not privileged.											
DWord	Bit	Description									
0	31:29	<b>Command Type</b>									
		Default Value:	0h MI_COMMAND								
		Format:	OpCode								
	28:23	<b>MI Command Opcode</b>									
		Default Value:	27h Store DW MI_CLFLUSH								
		Format:	OpCode								
	22	<b>Use Global GTT</b>									
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Per Process Graphics Address</td> <td></td> </tr> <tr> <td>1h</td> <td>Global Graphics Address</td> <td>This command will use the global GTT to translate the Address.</td> </tr> </tbody> </table>	Value	Name	Description	0h	Per Process Graphics Address		1h	Global Graphics Address	This command will use the global GTT to translate the Address.
		Value	Name	Description							
		0h	Per Process Graphics Address								
1h	Global Graphics Address	This command will use the global GTT to translate the Address.									
<b>Reserved</b>											
Format:	MBZ										
9:0	<b>DWord Length</b>										
	Format:	n Total Length - 2									
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1h</td> <td>[Default]</td> <td>Excludes DWord (0,1)</td> </tr> </tbody> </table>	Value	Name	Description	1h	[Default]	Excludes DWord (0,1)				
	Value	Name	Description								
	1h	[Default]	Excludes DWord (0,1)								
	<b>Programming Notes</b>										
The value of this field must not exceed a value 3Fh when programmed in a batch buffer with resource streamer enabled.											
<b>Project</b>											
CHV, BSW											
1	31:12	<b>Page Base Address</b>									
		Format:	GraphicsAddress[31:12]								
	4KB aligned Page Address which software requires hardware to flush to DRAM.										
11:6	<b>Starting Cacheline Offset</b>										
	Format:	U6 Zero based starting cacheline offset in to the Page Base Address									

<b>MI_CLFLUSH</b>					
	5:0	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ				
2	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
	Format:	MBZ			
15:0	<p><b>Page Base Address High</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space.</p>	Format:	GraphicsAddress[47:32]		
Format:	GraphicsAddress[47:32]				
3..n	31:0	<p><b>DW Representing a Half Cache Line</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table> <p>The information given to hardware is the DW itself, not the contents. Hardware uses the DW count of the command to determine the offset from the base to flush out. The offset is ½ cache line (8 DW = 1HW) granular so for a full page, the command will need 4096 bytes / 4 bytes per DW / 8 DW per HW = 128 DW.</p> <table border="1" style="width: 100%; background-color: #e6f2ff;"> <tr> <td style="text-align: center;"><b>Programming Notes</b></td> </tr> </table> <p>Always even number of "DW Representing 1/2 cacheline" terms must be programmed.</p>	Format:	MBZ	<b>Programming Notes</b>
Format:	MBZ				
<b>Programming Notes</b>					

## MI\_CONDITIONAL\_BATCH\_BUFFER\_END

MI_CONDITIONAL_BATCH_BUFFER_END			
Project:	CHV, BSW		
Source:	BlitterCS		
Length Bias:	2		
<p>The MI_CONDITIONAL_BATCH_BUFFER_END command is used to conditionally terminate the execution of commands stored in a batch buffer initiated using a MI_BATCH_BUFFER_START command. Termination of second level batch buffer due to this command will also terminate the parent/first level batch buffer.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	36h MI_CONDITIONAL_BATCH_BUFFER_END
		Format:	OpCode
	22	<b>Use Global GTT</b>	
		Default Value:	0h
		Format:	Boolean
	<p>If set, this command uses the global GTT to translate the Compare Address and this command must be executing from a privileged (secure) batch buffer. If clear, the PPGTT is used to translate the Compare Address.</p>		
21	<b>Compare Semaphore</b>		
	Default Value:	0h	
	Format:	Boolean	
<p>If set, the value from the Compare Data Dword is compared to the value from the Compare Address in memory. If the value at Compare Address is greater than the Compare Data Dword, execution of the current command buffer should continue. If clear, the parser will continue to the next command and not exit the batch buffer.</p>			
20	<b>Reserved</b>		
19:8	<b>Reserved</b>		
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	2h Excludes DWord (0,1)	
	Format:	=n Total Length - 2. Excludes DWord (0,1).	
1	31:0	<b>Compare Data Dword</b> Data DWord to compare to memory. The Data DWord is supplied by software to control	

<b>MI_CONDITIONAL_BATCH_BUFFER_END</b>					
		execution of the command buffer. If the compare is enabled and the data at Semaphore Address is greater than this DWord, the execution of the command buffer should continue.			
2	31:3	<p><b>Compare Address</b></p> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>GraphicsAddress[31:3]</td> </tr> </table> <p>Qword address to fetch Data Dword(DW0) from memory. HW will compare the Data Dword(DW0) with Compare Data Dword</p>	Format:	GraphicsAddress[31:3]	
	Format:	GraphicsAddress[31:3]			
2:0	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ
Project:	All				
Format:	MBZ				
3	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
	Format:	MBZ			
15:0	<p><b>Compare Address High</b></p> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>This field specifies the 4 GB-aligned base address of GFX 4 GB virtual address space within the host's 64-bit virtual address space.</p>	Format:	GraphicsAddress[47:32]		
Format:	GraphicsAddress[47:32]				

## MI\_CONDITIONAL\_BATCH\_BUFFER\_END

DWord		Bit	Description
<p><b>MI_CONDITIONAL_BATCH_BUFFER_END</b></p> <p>Project: CHV, BSW                      Source: VideoEnhancementCS                      Length Bias: 2</p> <p>The MI_CONDITIONAL_BATCH_BUFFER_END command is used to conditionally terminate the execution of commands stored in a batch buffer initiated using a MI_BATCH_BUFFER_START command. Termination of second level batch buffer due to this command will also terminate the parent/first level batch buffer.</p>			
<b>Programming Notes</b>			
This command is only valid with a 1st level batch buffer (bit 22 in MI_BATCH_BUFFER_START is set to '0')			
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	36h MI_CONDITIONAL_BATCH_BUFFER_END
		Format:	OpCode
	22	<b>Use Global GTT</b>	
		Default Value:	0h
		Format:	Boolean
	If set, this command will use the global GTT to translate the <b>Compare Address</b> and this command must be executing from a privileged (secure) batch buffer. If clear, the PPGTT will be used to translate the <b>Compare Address</b> .		
21	<b>Compare Semaphore</b>		
	Default Value:	0h	
	Format:	Boolean	
If set, the value from the <b>Compare Data Dword</b> is compared to the value from the <b>Compare Address</b> in memory. If the value at <b>Compare Address is greater than the Compare Data Dword</b> , execution of current command buffer should continue. If clear, the parser will continue to the next command and not exit the batch buffer.			
20	<b>Reserved</b>		
19:8	<b>Reserved</b>		
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Format:	=n Total Length - 2	

MI_CONDITIONAL_BATCH_BUFFER_END							
	Value	Name	Project				
	1h	Excludes DWord (0,1) <b>[Default]</b>	CHV, BSW				
1	31:0	<p><b>Compare Data Dword</b></p> <p>Data dword to compare memory. The Data dword is supplied by software to control execution of the command buffer. If the compare is enabled and the data at <b>Semaphore Address</b> is greater than this dword, the execution of the command buffer should continue.</p>					
2	31:3	<p><b>Compare Address</b></p> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[31:3]</td> </tr> </table> <p>Qword address to fetch Data Dword(DW0) from memory. HW will compare the Data Dword(DW0) with Compare Data Dword</p>	Format:	GraphicsAddress[31:3]			
	Format:	GraphicsAddress[31:3]					
2:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ				
Format:	MBZ						
3 <b>Project:</b> CHV, BSW	31:16	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ	
		Project:	CHV, BSW				
	Format:	MBZ					
	15:0	<p><b>Compare Address High</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space</p>	Project:	CHV, BSW	Format:	GraphicsAddress[47:32]	
Project:		CHV, BSW					
Format:	GraphicsAddress[47:32]						

## MI\_CONDITIONAL\_BATCH\_BUFFER\_END

MI_CONDITIONAL_BATCH_BUFFER_END			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>The MI_CONDITIONAL_BATCH_BUFFER_END command is used to conditionally terminate the execution of commands stored in a batch buffer initiated using a MI_BATCH_BUFFER_START command. Termination of second level batch buffer due to this command will also terminate the parent/first level batch buffer.</p>			
<b>Programming Notes</b>			
This command is only valid with a 1st level batch buffer (bit 22 in MI_BATCH_BUFFER_START is set to 0).			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	36h MI_CONDITIONAL_BATCH_BUFFER_END
		Format:	OpCode
	22	<b>Use Global GTT</b>	
		Default Value:	0h DefaultVaueDesc
		Format:	Boolean
		Format:	U1 FormatDesc
<b>Description</b>			
If set, this command will use the global GTT to translate the Compare Address and this command must be executing from a privileged (secure) batch buffer. If clear, the PPGTT will be used to translate the Compare Address.		<b>Project</b>	
21	<b>Compare Semaphore</b>		
	Default Value:	0h DefaultVaueDesc	
	Format:	Boolean	
If set, the value from the Compare Data Dword is compared to the value from the Compare Address in memory. If the value at Compare Address is greater than the Compare Data Dword, execution of current command buffer should continue.If clear, no comparison takes place.			
20	<b>Reserved</b>		
19:8	<b>Reserved</b>		
7:0	<b>DWord Length</b>		
	Format:	=n Total Length - 2	

<b>MI_CONDITIONAL_BATCH_BUFFER_END</b>						
Value	Name	Project				
1h	Excludes DWord (0,1) <b>[Default]</b>	CHV, BSW				
1	31:0	<p><b>Compare Data Dword</b> Data dword to compare memory. The Data dword is supplied by software to control execution of the command buffer. If the compare is enabled and the data at Semaphore Address is greater than this dword, the execution of the command buffer should continue.</p>				
2	31:3	<p><b>Compare Address</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[31:3]</td> </tr> </table> <p>Qword address to fetch compare Mask (DW0) and Data Dword(DW1) from memory. HW will do AND operation on Mask(DW0) with Data Dword(DW1) and then compare the result against Semaphore Data Dword</p>	Format:	GraphicsAddress[31:3]		
Format:	GraphicsAddress[31:3]					
	2:0	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ					
3 <b>Project:</b> CHV, BSW	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ
Project:	CHV, BSW					
Format:	MBZ					
	15:0	<p><b>Compare Address High</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space</p>	Project:	CHV, BSW	Format:	GraphicsAddress[47:32]
Project:	CHV, BSW					
Format:	GraphicsAddress[47:32]					



## MI\_CONDITIONAL\_BATCH\_BUFFER\_END

MI_CONDITIONAL_BATCH_BUFFER_END			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
<p>The MI_CONDITIONAL_BATCH_BUFFER_END command is used to conditionally terminate the execution of commands stored in a batch buffer initiated using a MI_BATCH_BUFFER_START command. Termination of second level batch buffer due to this command will also terminate the parent/first level batch buffer.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	36h MI_CONDITIONAL_BATCH_BUFFER_END
		Format:	OpCode
	22	<b>Use Global GTT</b>	
	Default Value:		0h
	<p>If set, this command will use the global GTT to translate the <b>Compare Address</b> and this command must be executing from a privileged (secure) batch buffer. If clear, the PPGTT will be used to translate the <b>Compare Address</b>.</p>		
	21	<b>Compare Semaphore</b>	
Default Value:		0h	
<p>If set, the value from the Compare Data Dword is compared to the value from the Compare Address in memory. If the value at Compare Address is greater than the Compare Data Dword, execution of current command buffer should continue. If clear, the parser will continue to the next command and not exit the batch buffer.</p>			
20	<b>Reserved</b>		
19:8	<b>Reserved</b>		
7:0	<b>DWord Length</b>		
	Format:	=n Total Length - 2. Excludes DWord (0,1).	
	<b>Value</b>	<b>Name</b>	<b>Project</b>
	1h	[Default]	CHV, BSW
1	31:0	<b>Compare Data Dword</b>	
<p>Data dword to compare memory. The Data dword is supplied by software to control execution of the command buffer. If the compare is enabled and the data at Compare Address is greater than this dword, the execution of the command buffer should continue.</p>			

<b>MI_CONDITIONAL_BATCH_BUFFER_END</b>					
2	31:3	<p><b>Compare Address</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[31:3]</td> </tr> </table> <p>Qword address to fetch Data Dword(DW0) from memory. HW will compare the Data Dword(DW0) with Compare Data Dword</p>	Format:	GraphicsAddress[31:3]	
	Format:	GraphicsAddress[31:3]			
2:0	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ				
3 <b>Project:</b> CHV, BSW	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table>	Project:	CHV, BSW	
	Project:	CHV, BSW			
	15:0	<p><b>Compare Address High</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>This field specifies the 4GB aligned base address of Gfx 4GB virtual address space within the host's 64-bit virtual address space.</p>	Project:	CHV, BSW	Format:
Project:	CHV, BSW				
Format:	GraphicsAddress[47:32]				

## MI\_COPY\_MEM\_MEM

MI_COPY_MEM_MEM			
Project:	CHV, BSW		
Source:	BlitterCS		
Length Bias:	2		
<p>The MI_COPY_MEM_MEM command reads a DWord from memory and stores the value of that DWord to back to memory. The source and destination addresses are specified in the command. The command temporarily halts command execution.</p>			
<b>Programming Notes</b>			
<p>This command should not be used within a "non_privilege"batch buffer to access global virtual space, doing so will be treated as privilege access violation. Refer "User Mode Privilege Command" in MI_BATCH_BUFFER_START command section to know HW behavior on encountering privilege access violation. This command can be used within ring buffers and/or privilege batch buffers to access global virtual space.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	2Eh MI_MEM_TO_MEM
		Format:	OpCode
	22	<b>Use Global GTT Source</b>	
		It is allowed for this bit to be set when executing this command from a privileged (secure) batch buffer or ring buffer. This bit must be clear when programmed from within a non-privileged batch buffer. This bit must be 1 if the Per Process GTT Enable bit is clear.	
		<b>Value</b>	<b>Name</b>
		0h	Per Process Graphics Address
21	<b>Use Global GTT Destination</b>		
	It is allowed for this bit to be set when executing this command from a privileged (secure) batch buffer or ring buffer. This bit must be clear when programmed from within a non-privileged batch buffer. This bit must be 1 if the Per Process GTT Enable bit is clear.		
	<b>Value</b>	<b>Name</b>	
	0h	Per Process Graphics Address	
1h	Global Graphics Address	This command will use the global GTT to translate the Address and this command must be executing from a privileged (secure) batch buffer.	

<b>MI_COPY_MEM_MEM</b>						
	20:8	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td style="text-align: right;">MBZ</td> </tr> </table>	Format:	MBZ		
	Format:	MBZ				
7:0	<b>DWord Length</b> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: right;">3</td> </tr> <tr> <td>Format:</td> <td style="text-align: right;">=n Total Length - 2</td> </tr> </table>	Default Value:	3	Format:	=n Total Length - 2	
Default Value:	3					
Format:	=n Total Length - 2					
1	31:2	<b>Destination Memory Address</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td style="text-align: right;">All</td> </tr> <tr> <td>Format:</td> <td style="text-align: right;">GraphicsAddress[31:2]</td> </tr> </table> <p>Surface Type: MMIO Register            This field specifies the address of the memory location where the value fetched specified in the DWord address above will be written. The address specifies the DWord location of the data.            Range = GraphicsVirtualAddress[31:2] for a DWord register</p>	Project:	All	Format:	GraphicsAddress[31:2]
	Project:	All				
Format:	GraphicsAddress[31:2]					
1:0	<b>Reserved</b>					
2	31:16	<b>Reserved</b>				
	15:0	<b>Destination Memory Address High</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td style="text-align: right;">All</td> </tr> <tr> <td>Format:</td> <td style="text-align: right;">GraphicsAddress[47:32]</td> </tr> </table> <p>Surface Type: MMIO Register            This field specifies the address of the memory location where the value is located that will be written to the address below. The address specifies the DWord location of the data.            Range = GraphicsVirtualAddress[47:32] for a DWord register</p>	Project:	All	Format:	GraphicsAddress[47:32]
Project:	All					
Format:	GraphicsAddress[47:32]					
3	31:2	<b>Source Memory Address</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td style="text-align: right;">All</td> </tr> <tr> <td>Format:</td> <td style="text-align: right;">GraphicsAddress[31:2]</td> </tr> </table> <p>Surface Type: MMIO Register            This field specifies the address of the memory location where the value is located that will be written to the address below. The address specifies the DWord location of the data.            Range = GraphicsVirtualAddress[31:2] for a DWord register</p>	Project:	All	Format:	GraphicsAddress[31:2]
	Project:	All				
Format:	GraphicsAddress[31:2]					
1:0	<b>Reserved</b>					
4	31:16	<b>Reserved</b>				
	15:0	<b>Source Memory Address High</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td style="text-align: right;">All</td> </tr> <tr> <td>Format:</td> <td style="text-align: right;">GraphicsAddress[47:32]</td> </tr> </table> <p>Surface Type: MMIO Register            This field specifies the address of the memory location where the value is located that will be written to the address below. The address specifies the DWord location of the data.            Range = GraphicsVirtualAddress[47:32] for a DWord register</p>	Project:	All	Format:	GraphicsAddress[47:32]
Project:	All					
Format:	GraphicsAddress[47:32]					

## MI\_COPY\_MEM\_MEM

<b>MI_COPY_MEM_MEM</b>			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
<p>The MI_COPY_MEM_MEM command reads a DWord from memory and stores the value of that DWord to back to memory. The source and destination addresses are specified in the command. The command temporarily halts command execution.</p>			
<b>Programming Notes</b>			
<p>This command should not be used within a "non_privilege"batch buffer to access global virtual space, doing so will be treated as privilege access violation. Refer "User Mode Privilege Command" in MI_BATCH_BUFFER_START command section to know HW behavior on encountering privilege access violation. This command can be used within ring buffers and/or privilege batch buffers to access global virtual space.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	2Eh MI_MEM_TO_MEM
		Format:	OpCode
	22	<b>Use Global GTT Source</b>	
		It is allowed for this bit to be set when executing this command from a privileged (secure) batch buffer or ring buffer. This bit must be clear when programmed from within a non-privileged batch buffer. This bit must be 1 if the Per Process GTT Enable bit is clear.	
		<b>Value</b>	<b>Name</b>
		<b>Description</b>	
0h	Per Process Graphics Address		
	1h	Global Graphics Address	It is allowed for this bit to be set when executing this command from a privileged (secure) batch buffer or ring buffer. This bit must be clear when programmed from within a non-privileged batch buffer. This bit must be 1 if the Per Process GTT Enable bit is clear.
21	<b>Use Global GTT Destination</b>		
	This bit will be ignored and treated as if clear when executing from a non-privileged batch buffer. It is allowed for this bit to be clear when executing this command from a privileged (secure) batch buffer. This bit <i>must</i> be '1' if the <b>Per Process GTT Enable</b> bit is clear. This bit will determine write to memory uses Global or Per Process GTT.		

<b>MI_COPY_MEM_MEM</b>				
		<b>Value</b>	<b>Name</b>	<b>Description</b>
		0h	Per Process Graphics Address	
		1h	Global Graphics Address	This command will use the global GTT to translate the Address and this command must be executing from a privileged (secure) batch buffer.
	20:8	<b>Reserved</b>		
		Format:		MBZ
	7:0	<b>Dword Length</b>		
		Default Value:		3
		Format:		=n Total Length - 2
1..2	63:2	<b>Destination Memory Address</b>		
		Project:		All
		Format:		GraphicsAddress[63:2]
		Surface Type: MMIO Register This field specifies the address of the memory location where the value fetched specified in the DWord address above will be written. The address specifies the DWord location of the data. Range = GraphicsVirtualAddress[63:2] for a DWord register GraphicsAddress [63:48] are ignored by the HW and assumed to be in correct canonical form [63:48] == [47].		
	1:0	<b>Reserved</b>		
		Project:		All
		Format:		MBZ
3..4	63:2	<b>Source Memory Address</b>		
		Project:		All
		Format:		GraphicsAddress[63:2]
		Surface Type: MMIO Register This field specifies the address of the memory location where the value is located that will be written to the address below. The address specifies the DWord location of the data. Range = GraphicsVirtualAddress[63:2] for a DWord register GraphicsAddress [63:48] are ignored by the HW and assumed to be in correct canonical form [63:48] == [47].		
	1:0	<b>Reserved</b>		
		Project:		All
		Format:		MBZ

## MI\_COPY\_MEM\_MEM

MI_COPY_MEM_MEM			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>The MI_COPY_MEM_MEM command reads a DWord from memory and stores the value of that DWord to back to memory. The source and destination addresses are specified in the command. The command temporarily halts command execution.</p>			
<b>Programming Notes</b>			
<p>This command should not be used within a "non_privilege"batch buffer to access global virtual space, doing so will be treated as privilege access violation. Refer "User Mode Privilege Command" in MI_BATCH_BUFFER_START command section to know HW behavior on encountering privilege access violation. This command can be used within ring buffers and/or privilege batch buffers to access global virtual space.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value: 0h MI_COMMAND	
	Format: OpCode		
	28:23	<b>MI Command Opcode</b>	
Default Value: 2Eh MI_MEM_TO_MEM			
22		<b>Use Global GTT Source</b>	
		It is allowed for this bit to be set when executing this command from a privileged (secure) batch buffer or ring buffer. This bit must be clear when programmed from within a non-privileged batch buffer. This bit must be 1 if the Per Process GTT Enable bit is clear.	
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0h	Per Process Graphics Address	
1h	Global Graphics Address	This command will use the global GTT to translate the Address and this command must be executing from a privileged (secure) batch buffer.	
21		<b>Use Global GTT Destination</b>	
		It is allowed for this bit to be set when executing this command from a privileged (secure) batch buffer or ring buffer. This bit must be clear when programmed from within a non-privileged batch buffer. This bit must be 1 if the Per Process GTT Enable bit is clear.	
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0h	Per Process Graphics Address	
1h	Global Graphics Address	This command will use the global GTT to translate the Address and this command must be executing from a privileged (secure) batch buffer.	

<b>MI_COPY_MEM_MEM</b>		
	20:8	<b>Reserved</b>
	7:0	<b>DWord Length</b>
		Default Value: 3 Format: =n Total Length - 2
1	31:2	<b>Destination Memory Address</b>
		Project: All Format: GraphicsAddress[31:2]
	Surface Type: MMIO Register This field specifies the address of the memory location where the value fetched specified in the DWord address above will be written. The address specifies the DWord location of the data. Range = GraphicsVirtualAddress[31:2] for a DWord register	
	1:0	<b>Reserved</b>
2	31:16	<b>Reserved</b>
	15:0	<b>Destination Memory Address High</b>
		Project: All Format: GraphicsAddress[47:32]
Surface Type: MMIO Register This field specifies the address of the memory location where the value is located that will be written to the address below. The address specifies the DWord location of the data. Range = GraphicsVirtualAddress[47:32] for a DWord register		
3	31:2	<b>Source Memory Address</b>
		Project: All Format: GraphicsAddress[31:2]
	Surface Type: MMIO Register This field specifies the address of the memory location where the value is located that will be written to the address below. The address specifies the DWord location of the data. Range = GraphicsVirtualAddress[31:2] for a DWord register	
	1:0	<b>Reserved</b>
4	31:16	<b>Reserved</b>
	15:0	<b>Source Memory Address High</b>
		Project: All Format: GraphicsAddress[47:32]
Surface Type: MMIO Register This field specifies the address of the memory location where the value is located that will be written to the address below. The address specifies the DWord location of the data. Range = GraphicsVirtualAddress[47:32] for a DWord register		



## MI\_COPY\_MEM\_MEM

MI_COPY_MEM_MEM			
Project:	CHV, BSW		
Source:	VideoEnhancementCS		
Length Bias:	2		
<p>The MI_COPY_MEM_MEM command reads a DWord from memory and stores the value of that DWord to back to memory. The source and destination addresses are specified in the command. The command temporarily halts command execution.</p>			
<b>Programming Notes</b>			
<p>This command should not be used within a "non_privilege"batch buffer to access global virtual space, doing so will be treated as privilege access violation. Refer "User Mode Privilege Command" in MI_BATCH_BUFFER_START command section to know HW behavior on encountering privilege access violation. This command can be used within ring buffers and/or privilege batch buffers to access global virtual space.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value: 0h MI_COMMAND	
	Format: OpCode		
	28:23	<b>MI Command Opcode</b>	
Default Value: 2Eh MI_MEM_TO_MEM			
22		<b>Use Global GTT Source</b>	
		It is allowed for this bit to be set when executing this command from a privileged (secure) batch buffer or ring buffer. This bit must be clear when programmed from within a non-privileged batch buffer. This bit must be 1 if the Per Process GTT Enable bit is clear.	
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0h	Per Process Graphics Address	
1h	Global Graphics Address	This command will use the global GTT to translate the Address and this command must be executing from a privileged (secure) batch buffer.	
21		<b>Use Global GTT Destination</b>	
		It is allowed for this bit to be set when executing this command from a privileged (secure) batch buffer or ring buffer. This bit must be clear when programmed from within a non-privileged batch buffer. This bit must be 1 if the Per Process GTT Enable bit is clear.	
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0h	Per Process Graphics Address	
1h	Global Graphics Address	This command will use the global GTT to translate the Address and this command must be executing from a privileged (secure) batch buffer.	

<b>MI_COPY_MEM_MEM</b>						
	20:8	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
	Format:	MBZ				
	7:0	<b>DWord Length</b> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">3</td> </tr> <tr> <td>Format:</td> <td>=n Total Length - 2</td> </tr> </table>	Default Value:	3	Format:	=n Total Length - 2
Default Value:	3					
Format:	=n Total Length - 2					
1	31:2	<b>Destination Memory Address</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[31:2]</td> </tr> </table> <p>Surface Type: MMIO Register            This field specifies the address of the memory location where the value fetched specified in the DWord address above will be written. The address specifies the DWord location of the data.            Range = GraphicsVirtualAddress[31:2] for a DWord register</p>	Project:	All	Format:	GraphicsAddress[31:2]
Project:	All					
Format:	GraphicsAddress[31:2]					
	1:0	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ
Project:	All					
Format:	MBZ					
2	31:16	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ
	Project:	All				
Format:	MBZ					
	15:0	<b>Destination Memory Address High</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>Surface Type: MMIO Register            This field specifies the address of the memory location where the value is located that will be written to the address below. The address specifies the DWord location of the data.            Range = GraphicsVirtualAddress[47:32] for a DWord register</p>	Project:	All	Format:	GraphicsAddress[47:32]
Project:	All					
Format:	GraphicsAddress[47:32]					
3	31:2	<b>Source Memory Address</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[31:2]</td> </tr> </table> <p>Surface Type: MMIO Register            This field specifies the address of the memory location where the value is located that will be written to the address below. The address specifies the DWord location of the data.            Range = GraphicsVirtualAddress[31:2] for a DWord register</p>	Project:	All	Format:	GraphicsAddress[31:2]
	Project:	All				
Format:	GraphicsAddress[31:2]					
	1:0	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ
Project:	All					
Format:	MBZ					
4	31:16	<b>Reserved</b>				

<b>MI_COPY_MEM_MEM</b>					
15:0	<p><b>Source Memory Address High</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>Surface Type: MMIO Register                      This field specifies the address of the memory location where the value is located that will be written to the address below. The address specifies the DWord location of the data.                      Range = GraphicsVirtualAddress[47:32] for a DWord register</p>	Project:	All	Format:	GraphicsAddress[47:32]
Project:	All				
Format:	GraphicsAddress[47:32]				

## MI\_DISPLAY\_FLIP

<b>MI_DISPLAY_FLIP</b>	
Project:	CHV, BSW
Source:	BlitterCS
Length Bias:	2
<p>The MI_DISPLAY_FLIP command is used to request a specific display plane to switch (flip) to display a new buffer. The buffer is specified with a starting address and pitch. The tiled attribute of the buffer start address is programmed as part of the packet.</p>	
<p>The operation this command performs is also known as a "display flip request" operation - in that the flip operation itself will occur at some point in the future. This command specifies when the flip operation is to occur: either synchronously with vertical retrace to avoid tearing artifacts</p>	
<b>Programming Notes</b>	
<p>This command simply requests a display flip operation -- command execution then continues normally. There is no guarantee that the flip (even if asynchronous) will occur prior to subsequent commands being executed. (Note that completion of the MI_FLUSH_DW command does not guarantee that outstanding flip operations have completed). The MI_WAIT_FOR_EVENT command must be used to provide this synchronization to avoid back to back MI_DISPLAY_FLIP commands to the same display plane - by pausing command execution until a pending flip has actually completed. This synchronization can also be performed by use of the Display Flip Pending hardware status. See Display Flip Synchronization in the Device Programming Interface chapter of MI Functions.</p>	
<p>After a display flip operation is requested, software is responsible for initiating any required synchronization with subsequent buffer clear or blitter operations. For multi-buffering (e.g., double buffering) operations, this will typically require updating SURFACE_STATE or the binding table to change the blitter (back) buffer. In addition, prior to any subsequent clear or blitter operations, software must typically ensure that the new blitter buffer is not actively being displayed. Again, the MI_WAIT_FOR_EVENT command or Display Flip Pending hardware status can be used to provide this synchronization. See Display Flip Synchronization in the Device Programming Interface chapter of MI Functions.</p>	
<p>The display buffer command uses the X and Y offset for the tiled buffers from the Display Interface registers. Software is allowed to change the offset via the MMIO interface irrespective of the flip commands enqueued in the command stream. For tiled buffers, the display subsystem uses the X and Y offset in generation of the final request to memory. The offset is always updated on the next vblank for both Synchronous and Asynch Flips. It is not necessary to have a flip enqueued to update the X and Y offset</p>	
<p>The display buffer command uses the linear DWord offset for the linear buffers from the Display Interface registers. Software is allowed to change the offset via the MMIO interface irrespective of the flip commands enqueued in the command stream. For linear buffers, the display subsystem uses the Dword offset in generation of the final request to memory.</p> <ul style="list-style-type: none"> <li>• For synchronous flips the offset is updated on the next vblank. It is not necessary to have a sync flip enqueued to update the DWord offset.</li> <li>• Linear memory does not support asynchronous flips.</li> </ul>	
<p>Events must be unmasked in the Display Engine Render Response Mask Register (DE RRMR 0x44050) prior to</p>	

## MI\_DISPLAY\_FLIP

waiting for them with a MI\_WAIT\_FOR\_EVENT command, or in the case of flips or scanlines, prior to starting the flip or loading the scanline. Unmasked events will wake command streamer as they occur, so for improved power savings it is recommended to only unmask events that are required. Programming the DE RRMR register can be done through MMIO or a LOAD\_REGISTER\_IMMEDIATE command.

DWord	Bit	Description		
0	31:29	<b>Command Type</b>		
		Default Value: 0h MI_COMMAND		
		Format: OpCode		
	28:23	28:23	<b>MI Command Opcode</b>	
			Default Value: 14h MI_DISPLAY_FLIP	
			Format: OpCode	
	22	22	<b>Async Flip Indicator</b>	
			Format: Enable	
	This bit should always be set if DW2 [1:0] == '01' (async flip). This field is required due to HW limitations. This bit is used by the blitter pipe while DW2 is used by the display hardware.			
	21:19	21:19	<b>Display (Plane) Select</b>	
			This field selects which display plane is to perform the flip operation.	
			<b>Value</b>	<b>Name</b>
0h			Display Plane A	
1h			Display Plane B	
2h			Display Sprite A	
3h			Display Sprite B	
4h			Display Plane C	
5h	Display Sprite C			
18:17	18:17	<b>Reserved</b>		
16	16	<b>Override Pipe/Plane</b>		
		Project: CHV, BSW		
		<b>Value</b>	<b>Name</b>	<b>Description</b>
		1h	Use 15:8 bits	
0h	Use bits 21:19	("client mode")		
15:13	15:13	<b>Reserved</b>		
		Format: MBZ		
12:8	12:8	<b>Display Plane Select</b>		
		Project: CHV, BSW		

		<b>MI_DISPLAY_FLIP</b>			
		Value	Name		
		00000b	Display Plane A		
		00001b	Display Plane B		
		00010b	Display Plane C		
		00011b	Reserved		
		00100b	Display Sprite A		
		00101b	Display Sprite B		
		00110b	Display Sprite C		
		00111b	Display Sprite A2		
		01000b	Display Sprite B2		
		01001b	Display Sprite C2		
		01010b	Display Sprite A3		
		01011b	Display Sprite B3		
		01100b	Display Sprite C3		
		01101b	Reserved		
		01110b	Reserved		
		01111b	Reserved		
		1xxxxb	Remaining encodings reserved		
	7:0	<b>DWord Length</b>			
		Format:	=n Total Length - 2		
		For Synchronous Flips and Asynchronous Flips, this field must be programmed to 1h for a total length of 3.			
		Value	Name	Project	Exists If
		0h	Excludes DWord (0,1) <b>[Default]</b>		
		1h			(([Flip Type]!='Stereo 3D Flip')
		2h		CHV, BSW	(([Flip Type]='Stereo 3D Flip')
1	31	<b>Reserved</b>			
		Project:	CHV, BSW		
	30:16	<b>Reserved</b>			
		Project:	All		
		Format:	MBZ		
	15:6	<b>Reserved</b>			
		Project:	All		
	5:1	<b>Reserved</b>			
		Project:	All		

<b>MI_DISPLAY_FLIP</b>			
		Format:	MBZ
	0	<b>Tile Parameter</b>	
		Project:	CHV, BSW
		Format:	Enable
		For Asynchronous Flips, this parameter cannot be changed. All the flips in a flip chain should maintain the same tile parameter as programmed with the last synchronous flip or direct thru MMIO.	
		<b>Value</b>	<b>Name</b>
		<b>Description</b>	
		0h	Linear <b>[Default]</b>
		1h	Tiled X
		<b>Programming Notes</b>	
		Performing a synchronous or asynchronous flip will drop any previous synchronous flip that has not yet completed.	
2	31:12	<b>Display Buffer Base Address</b>	
		Project:	All
		Format:	GraphicsAddress[31:12]
		This field specifies Bits 31:12 of the Graphics Address of the new display buffer.	
		<b>Programming Notes</b>	
		The Display buffer must reside completely in Main Memory.	
		This address is always translated via the global (rather than per-process) GTT	
	11:3	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	2	<b>Reserved</b>	
		Project:	CHV, BSW
	1:0	<b>Flip Type</b>	
		Project:	CHV, BSW
		This field specifies whether the flip operation should be performed asynchronously to vertical retrace.	
		<b>Value</b>	<b>Name</b>
		<b>Description</b>	<b>Project</b>
		00b	Sync Flip <b>[Default]</b>
		01b	Async Flip
		1b	Reserved
		<b>Programming Notes</b>	

<b>MI_DISPLAY_FLIP</b>			
		<ul style="list-style-type: none"> <li>The Display Buffer Pitch and Tile parameter cannot be changed for asynchronous flips (i.e., the new buffer must have the same pitch/tile format as the previous buffer).</li> <li>Async flips are supported on X-Tiled Frame buffers only.</li> <li>For Asynch Flips the Buffers used must be 32KB aligned.</li> <li>Asynch flips are supported on Display Planes A and B and C only.</li> </ul>	
<b>3</b> <b>Project:</b> CHV, BSW	31:12	<b>Reserved</b>	
	11:3	<b>Reserved</b>	
		Project:	CHV, BSW
	Format:	MBZ	
	2	<b>Reserved</b>	
	Project:	CHV, BSW	
1:0	<b>Flip Type</b> Project: CHV, BSW This field specifies whether the flip operation should be performed asynchronously to vertical retrace.		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	00b	Sync Flip <b>[Default]</b>	The flip will occur during the vertical blanking interval - thus avoiding any tearing artifacts.
	01b	Asynch Flip	The flip will occur "as soon as possible" - and may exhibit tearing artifacts
	<b>Programming Notes</b>		
	<ul style="list-style-type: none"> <li>The Display Buffer Pitch and Tile parameter cannot be changed for asynchronous flips (i.e., the new buffer must have the same pitch/tile format as the previous buffer).</li> <li>Async flips are supported on X-Tiled Frame buffers only.</li> <li>For Asynch Flips the Buffers used must be 32KB aligned.</li> <li>Asynch flips are supported on Display Planes A and B and C only.</li> </ul>		



## MI\_FLUSH\_DW

<b>MI_FLUSH_DW</b>	
Project:	CHV, BSW
Source:	VideoEnhancementCS
Length Bias:	2

The MI\_FLUSH\_DW command is used to perform an internal "flush" operation. The parser pauses on an internal flush until all drawing engines have completed any pending operations. In addition, this command can also be used to:

- Flush any dirty data to memory.
- Invalidate the TLB cache inside the hardware

Usage note: After this command is completed with a Store DWord enabled, CPU access to graphics memory will be coherent (assuming the Render Cache flush is not inhibited).

DWord	Bit	Description	
0	31:29	<b>Command Type</b> Default Value: 0h MI_COMMAND	
	28:23	<b>MI Command Opcode</b> Default Value: 26h MI_FLUSH_DW	
	22	<b>Reserved</b> Project: All	
	21	<b>Store Data Index</b> Project: All Format: U1	
		<b>Description</b> <b>Ring Buffer Mode Scheduling:</b> This field is valid only if the post-sync operation is not 0. If this bit is set, the store data address is actually an index into the global hardware status page. This bit only applies to the Global HW status page. If this field is 1, the Destination Address Type in this command must be set to 1 (GGTT). <b>Execlist Mode Scheduling:</b> This field is valid only if the post-sync operation is not 0. If this bit is set, the store data address is index into the global hardware status page when destination address type in the command is set to 1 (GGTT). The store data address is index into the per-process hardware status page when destination address type in the command is set to 0 (PPGT).	
		<b>Reserved</b>	
	20:19	<b>Reserved</b>	
	18	<b>TLB Invalidate</b> Project: All Format: U1	

<b>MI_FLUSH_DW</b>			
		<b>Description</b>	
		<p>If ENABLED, all TLBs belonging to Video Enhancement Engine will be invalidated once the flush operation is complete. This bit is only valid when the Post-Sync Operation field is a value of 1h or 3h.</p> <p>If GFX_MODE (0x229c) bit 13, this command will cause a config write to MMIO register space with the address 0x4f100.</p>	
	17	<b>Reserved</b>	
		Project:	CHV, BSW
		Format:	MBZ
	16	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	15:14	<b>Post-Sync Operation</b>	
		Project:	All
		<b>Value</b>	<b>Name</b>
		<b>Description</b>	<b>Project</b>
		0h	No Write
		1h	Write Immediate Data
		2h	Reserved
		3h	Write TIMESTAMP register
		<p>No write occurs as a result of this instruction. This can be used to implement a "trap" operation, etc.</p> <p>Write the QWord containing Immediate Data Low, High DWs to the Destination Address</p> <p>Reserved</p> <p>Write the TIMESTAMP register to the Destination Address. The upper 28 bits of the TIMESTAMP register are tied to '0'.</p>	
		<b>Programming Notes</b>	
		<p>If executed in non-secure batch buffer, the address given will be in a PPGTT address space. If in a secure ring or batch, address given will be in GGTT space</p>	
	13:10	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	9	<b>Reserved</b>	
	8	<b>Notify Enable</b>	
		Project:	All
		Format:	U1
		<p>If ENABLED, a Sync Completion Interrupt will be generated (if enabled by the MI Interrupt Control registers) once the sync operation is complete. See Interrupt Control Registers in Memory Interface Registers for details.</p>	

<b>MI_FLUSH_DW</b>				
	7	<b>Reserved</b>		
		Project:	All	
	Format:	MBZ		
	6	<b>Reserved</b>		
		Project:	CHV, BSW	
	5:0	<b>DWord Length</b>		
		Project:	All	
		Format:	=n Total Length - 2	
		<b>Value</b>	<b>Name</b>	<b>Project</b>
		3h	Excludes DWord (0,1) = 2 for DWord, 3 for QWord <b>[Default]</b>	CHV, BSW
1	31:3	<b>Address</b>		
		Project:	All	
		Format:	GraphicsAddress[31:3]U28	
		This field specifies Bits 31:3 of the Address where the DWord or QWord will be stored. Note that the address can only be QWord aligned, irrespective of data size.		
	2	<b>Destination Address Type</b>		
		Project:	All	
		Defines address space of Destination Address		
		<b>Value</b>	<b>Name</b>	<b>Description</b>
		0h	PPGTT	Use PPGTT address space for DW write
		1h	GGTT	Use GGTT address space for DW write
<b>Programming Notes</b>				
Ignored if "No write" is the selected in Operation.				
1:0	<b>Reserved</b>			
	Project:	All		
Format:	MBZ			
2 <b>Project:</b> CHV, BSW	31:16	<b>Reserved</b>		
		Project:	CHV, BSW	
	Format:	MBZ		
	15:0	<b>Address High</b>		
		Project:	CHV, BSW	
Format:		GraphicsAddress[47:32]U64		
This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space				

<b>MI_FLUSH_DW</b>				
3..4 <b>Project:</b> CHV, BSW	31:0	<p><b>Immediate Data</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This field specifies the DWord value to be written to the targeted location. DW2 is the lower DW if QW is desired. Only valid when 15:14 in header is set to 1h</p> <p>To avoid hitting a known hardware bug, drivers cannot send a QW write when bit 5 of the address is '1'</p>	Project:	CHV, BSW
Project:	CHV, BSW			

## MI\_FLUSH\_DW

MI_FLUSH_DW						
Project:	CHV, BSW					
Source:	BlitterCS					
Length Bias:	2					
<p>The MI_FLUSH_DW command is used to perform an internal "flush" operation. The parser pauses on an internal flush until all drawing engines have completed any pending operations. In addition, this command can also be used to: Flush any dirty data to memory. Invalidate the TLB cache inside the hardware</p> <p><b>Usage note: After this command is completed with a Store DWord enabled, CPU access to graphics memory will be coherent (assuming the Render Cache flush is not inhibited).</b></p>						
DWord	Bit	Description				
0	31:29	<b>Command Type</b> Default Value: 0h MI_COMMAND				
	28:23	<b>MI Command Opcode</b> Default Value: 26h MI_FLUSH_DW				
	22	<b>Reserved</b> Project: All Format: U1				
	21	<b>Store Data Index</b> Project: CHV, BSW Format: U1  <table border="1"> <thead> <tr> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td> <b>Ring Buffer Mode Scheduling:</b> This field is valid only if the post-sync operation is not 0. If this bit is set, the store data address is actually an index into the global hardware status page. This bit only applies to the Global HW status page. If this field is 1, the Destination Address Type in this command must be set to 1 (GGTT).  <b>Execlist Mode Scheduling:</b> This field is valid only if the post-sync operation is not 0. If this bit is set, the store data address is index into the global hardware status page when destination address type in the command is set to 1 (GGTT). The store data address is index into the per-process hardware status page when destination address type in the command is set to 0 (PPGTT).                             </td> <td>CHV, BSW</td> </tr> </tbody> </table>	Description	Project	<b>Ring Buffer Mode Scheduling:</b> This field is valid only if the post-sync operation is not 0. If this bit is set, the store data address is actually an index into the global hardware status page. This bit only applies to the Global HW status page. If this field is 1, the Destination Address Type in this command must be set to 1 (GGTT). <b>Execlist Mode Scheduling:</b> This field is valid only if the post-sync operation is not 0. If this bit is set, the store data address is index into the global hardware status page when destination address type in the command is set to 1 (GGTT). The store data address is index into the per-process hardware status page when destination address type in the command is set to 0 (PPGTT).	CHV, BSW
	Description	Project				
	<b>Ring Buffer Mode Scheduling:</b> This field is valid only if the post-sync operation is not 0. If this bit is set, the store data address is actually an index into the global hardware status page. This bit only applies to the Global HW status page. If this field is 1, the Destination Address Type in this command must be set to 1 (GGTT). <b>Execlist Mode Scheduling:</b> This field is valid only if the post-sync operation is not 0. If this bit is set, the store data address is index into the global hardware status page when destination address type in the command is set to 1 (GGTT). The store data address is index into the per-process hardware status page when destination address type in the command is set to 0 (PPGTT).	CHV, BSW				
	20:19	<b>Reserved</b> Project: All Format: MBZ				
	18	<b>TLB Invalidate</b> Project: CHV, BSW Format: U1				

<b>MI_FLUSH_DW</b>		
	<b>Description</b>	
	If ENABLED, all TLBs belonging to Blitter Engine will be invalidated once the flush operation is complete. This bit is only valid when the Post-Sync Operation field is a value of 1h or 3h.	
	If GFX_MODE (0x229c) bit 13, this command will cause a config write to MMIO register space with the address 0x4f100.	
17	<b>Reserved</b>	
	Project:	CHV, BSW
	Format:	MBZ
16	<b>Reserved</b>	
	Project:	All
	Format:	MBZ
15:14	<b>Post-Sync Operation</b>	
	Project:	CHV, BSW
	BitFieldDesc	
	<b>Value</b>	<b>Name</b>
	<b>Description</b>	
	0h	No Write
	1h	Write Immediate Data QWord
	2h	Reserved
	3h	Write TIMESTAMP Register
		No write occurs as a result of this instruction. This can be used to implement a "trap" operation, etc.
		Write the QWord containing Immediate Data Low, High DWs to the Destination Address
		Reserved
		Write the TIMESTAMP register to the Destination Address. The upper 28 bits of the TIMESTAMP register are tied to '0'.
	<b>Programming Notes</b>	
	If executed in a non-secure batch buffer, the address given is in a PPGTT address space. If in a secure ring or batch, the address given is in GGTT space.	
13:10	<b>Reserved</b>	
	Project:	All
	Format:	MBZ
9	<b>Reserved</b>	
	Project:	CHV, BSW
	Format:	MBZ
8	<b>Notify Enable</b>	
	Project:	CHV, BSW
	Format:	U1
	If ENABLED, a Sync Completion Interrupt will be generated (if enabled by the MI Interrupt Control registers) once the sync operation is complete. See Interrupt Control Registers in Memory Interface Registers for details.	

<b>MI_FLUSH_DW</b>													
	7:6	<b>Reserved</b>											
	5:0	<b>DWord Length</b>											
		Project:	All										
		Format:	=n Total Length - 2										
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>3h</td> <td>Excludes DWord (0,1) = 2 for DWord, 3 for QWord <b>[Default]</b></td> <td>CHV, BSW</td> </tr> </tbody> </table>	Value	Name	Project	3h	Excludes DWord (0,1) = 2 for DWord, 3 for QWord <b>[Default]</b>	CHV, BSW					
Value	Name	Project											
3h	Excludes DWord (0,1) = 2 for DWord, 3 for QWord <b>[Default]</b>	CHV, BSW											
1	31:3	<b>Address</b>											
		Project:	CHV, BSW										
		Format:	GraphicsAddress[31:3]U28										
		This field specifies Bits 31:3 of the Address where the DWord or QWord will be stored. Note that the address can only be QWord aligned, irrespective of data size.											
	2	<b>Destination Address Type</b>											
	Project:	All											
	Defines address space of Destination Address												
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>PPGTT</td> <td>Use PPGTT address space for DW write</td> <td>All</td> </tr> <tr> <td>1h</td> <td>GGTT</td> <td>Use GGTT address space for DW write</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	0h	PPGTT	Use PPGTT address space for DW write	All	1h	GGTT	Use GGTT address space for DW write	All
Value	Name	Description	Project										
0h	PPGTT	Use PPGTT address space for DW write	All										
1h	GGTT	Use GGTT address space for DW write	All										
	<b>Programming Notes</b>												
	Ignored if "No write" is the selected in Operation.												
	1:0	<b>Reserved</b>											
2 <b>Project:</b> CHV, BSW	31:16	<b>Reserved</b>											
		Project:	CHV, BSW										
		Format:	MBZ										
	15:0	<b>Address High</b>											
Project:		CHV, BSW											
Format:		GraphicsAddress[47:32]U64											
	This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space												
3.4 <b>Project:</b> CHV, BSW	31:0	<b>Immediate Data</b>											
		Project:	CHV, BSW										
		This field specifies the DWord value to be written to the targeted location. DW2 is the lower DW if QW is desired. Only valid when 15:14 in header is set to 1h											
	To avoid hitting a known hardware bug, drivers cannot send a QW write when bit 5 of the address is '1'												

## MI\_FLUSH\_DW

MI_FLUSH_DW							
Project:	CHV, BSW						
Source:	VideoCS						
Length Bias:	2						
<p>The MI_FLUSH_DW command is used to perform an internal "flush" operation. The parser pauses on an internal flush until all drawing engines have completed any pending operations. In addition, this command can also be used to: Flush any dirty data to memory. Invalidate the TLB cache inside the hardware Usage note: After this command is completed with a Store DWord enabled, CPU access to graphics memory will be coherent (assuming the Render Cache flush is not inhibited).</p>							
DWord	Bit	Description					
0	31:29	<b>Command Type</b> Default Value: 0h MI_COMMAND					
	28:23	<b>MI Command Opcode</b> Default Value: 26h MI_FLUSH_DW					
	22	<b>Reserved</b> Project: CHV, BSW					
	21	<b>Store Data Index</b> Project: CHV, BSW Format: U1					
		<table border="1"> <thead> <tr> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td> <b>Ring Buffer Mode Scheduling:</b> This field is valid only if the post-sync operation is not 0. If this bit is set, the store data address is actually an index into the global hardware status page. This bit only applies to the Global HW status page. If this field is 1, the Destination Address Type in this command must be set to 1 (GGTT).  <b>Execlist Mode Scheduling:</b> This field is valid only if the post-sync operation is not 0. If this bit is set, the store data address is index into the global hardware status page when destination address type in the command is set to 1 (GGTT). The store data address is index into the per-process hardware status page when destination address type in the command is set to 0 (PPGTT).               </td> <td>CHV, BSW</td> </tr> </tbody> </table>		Description	Project	<b>Ring Buffer Mode Scheduling:</b> This field is valid only if the post-sync operation is not 0. If this bit is set, the store data address is actually an index into the global hardware status page. This bit only applies to the Global HW status page. If this field is 1, the Destination Address Type in this command must be set to 1 (GGTT). <b>Execlist Mode Scheduling:</b> This field is valid only if the post-sync operation is not 0. If this bit is set, the store data address is index into the global hardware status page when destination address type in the command is set to 1 (GGTT). The store data address is index into the per-process hardware status page when destination address type in the command is set to 0 (PPGTT).	CHV, BSW
		Description	Project				
	<b>Ring Buffer Mode Scheduling:</b> This field is valid only if the post-sync operation is not 0. If this bit is set, the store data address is actually an index into the global hardware status page. This bit only applies to the Global HW status page. If this field is 1, the Destination Address Type in this command must be set to 1 (GGTT). <b>Execlist Mode Scheduling:</b> This field is valid only if the post-sync operation is not 0. If this bit is set, the store data address is index into the global hardware status page when destination address type in the command is set to 1 (GGTT). The store data address is index into the per-process hardware status page when destination address type in the command is set to 0 (PPGTT).	CHV, BSW					
	<b>Reserved</b> Format: MBZ						
	18	<b>TLB Invalidate</b> Project: CHV, BSW Format: U1 If ENABLED, all TLBs belonging to Video Engine will be invalidated once the flush operation is complete. This bit is only valid when the Post-Sync Operation field is a value of 1h or 3h.					



<b>MI_FLUSH_DW</b>			
17	<b>Reserved</b>		
	Project:	CHV, BSW	
	Format:	MBZ	
16	<b>Reserved</b>		
	Format:	MBZ	
15:14	<b>Post-Sync Operation</b>		
	Project:	CHV, BSW	
	BitFieldDesc		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0h	No Write	No write occurs as a result of this instruction. This can be used to implement a "trap" operation, etc.
	1h	Write Immediate Data	HW implicitly detects the Data size to be Qword or Dword to be written to memory based on the command dword length programmed . When Dword Length indicates Qword, Writes the QWord containing Immediate Data Low, High DWs to the Destination Address . When Dword Length indicates Dword, Writes the DWord containing Immediate Data Low to the Destination Address
	2h	Reserved	Reserved
3h		Write the TIMESTAMP register to the Destination Address. The upper 28 bits of the TIMESTAMP register are tied to '0'.	
13:10	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
9	<b>Reserved</b>		
	Project:	CHV, BSW	
	Format:	MBZ	
8	<b>Notify Enable</b>		
	Project:	CHV, BSW	
	Format:	U1	
If ENABLED, a Sync Completion Interrupt will be generated (if enabled by the MI Interrupt Control registers) once the sync operation is complete. See Interrupt Control Registers in Memory Interface Registers for details.			
7	<b>Video Pipeline Cache invalidate</b>		
	Project:	CHV, BSW	
	Format:	U1	
Enable the invalidation of the video cache at the end of this flush			
6	<b>Reserved</b>		

<b>MI_FLUSH_DW</b>											
		Project: CHV, BSW									
	5:0	<p><b>DWord Length</b></p> <p>Format: =n Total Length - 2</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>3h</td> <td>Excludes DWord (0,1) = 2 for DWord, 3 for QWord <b>[Default]</b></td> <td>CHV, BSW</td> </tr> </tbody> </table>	Value	Name	Project	3h	Excludes DWord (0,1) = 2 for DWord, 3 for QWord <b>[Default]</b>	CHV, BSW			
Value	Name	Project									
3h	Excludes DWord (0,1) = 2 for DWord, 3 for QWord <b>[Default]</b>	CHV, BSW									
1	31:3	<p><b>Address</b></p> <p>Format: GraphicsAddress[31:3]U28</p> <p>This field specifies Bits 31:3 of the Address where the DWord or QWord will be stored. Note that the address can only be QWord aligned, irrespective of data size.</p>									
	2	<p><b>Destination Address Type</b></p> <p>Defines address space of Destination Address</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>PPGTT</td> <td>Use PPGTT address space for DW write</td> </tr> <tr> <td>1h</td> <td>GGTT</td> <td>Use GGTT address space for DW write</td> </tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>Ignored if "No write" is the selected in Operation.</p>	Value	Name	Description	0h	PPGTT	Use PPGTT address space for DW write	1h	GGTT	Use GGTT address space for DW write
Value	Name	Description									
0h	PPGTT	Use PPGTT address space for DW write									
1h	GGTT	Use GGTT address space for DW write									
	1:0	<p><b>Reserved</b></p> <p>Format: MBZ</p>									
2	31:16	<p><b>Reserved</b></p> <p>Project: CHV, BSW</p> <p>Format: MBZ</p>									
	15:0	<p><b>Address High</b></p> <p>Project: CHV, BSW</p> <p>Format: GraphicsAddress[47:32]U64</p> <p>This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space</p>									
3..4	31:0	<p><b>Immediate Data</b></p> <p>Project: CHV, BSW</p> <p>This field specifies the DWord value to be written to the targeted location. DW2 is the lower DW if QW is desired. Only valid when 15:14 in header is set to 1h</p> <p>To avoid hitting a known hardware bug, drivers cannot send a QW write when bit 5 of the address is '1'</p>									

## MI\_LOAD\_REGISTER\_IMM

<b>MI_LOAD_REGISTER_IMM</b>			
Project:	CHV, BSW		
Source:	VideoEnhancementCS		
Length Bias:	2		
<p>The MI_LOAD_REGISTER_IMM command requests a write of up to a DWord constant supplied in the command to the specified Register Offset (i.e., offset into Memory-Mapped Register Range). The register is loaded before the next command is executed.</p> <ul style="list-style-type: none"> <li>The behavior of this command is controlled by Dword 3, Bit 8 (Disable Register Access) of the RINGBUF register. If this command is disallowed then the command stream converts it to a NOOP.</li> <li>If this command is executed from a batch buffer then the behavior of this command is controlled by Dword 0, Bit 8 (Security Indicator) of the BATCH_BUFFER_START Command. If the batch buffer is non-secure then the command stream converts this command to a NOOP.</li> <li>The following addresses should NOT be used for LRIs                         <ol style="list-style-type: none"> <li>0x8800 - 0x88FF</li> <li>&gt;= 0x40000</li> </ol> </li> </ul> <p>Any offset that is to a destination outside of the GT core will allow the parser to continue once the cycle is at the GT boundry and not destination. Any other address will ensure the destination is updated prior to parsing the next command</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	22h MI_LOAD_REGISTER_IMM
		Format:	OpCode
	22:12	<b>Reserved</b>	
	11:8	<b>Byte Write Disables</b>	
		Project:	All
		Format:	Enable[4] (bit 8 corresponds to Data DWord [7:0]).
Range: Must specify a valid register write operation			
If [11:8] is '1111b', then the register write will not occur. If [11:8] is '0000b', then the register DW will be updated. Any other value, the behavior will be specifically specified by the register or the behavior is undefined.			

<b>MI_LOAD_REGISTER_IMM</b>						
	7:0	<b>DWord Length</b>				
		Default Value:	0h Excludes DWord (0,1)			
		Project:	All			
		Format:	=n Total Length - 2			
1	31:23	<b>Reserved</b>				
		Project:	All			
		Format:	MBZ			
	22:2	<b>Register Offset</b>				
		Project:	All			
		Format:	MmioAddress[22:2]			
		This field specifies bits [22:2] of the offset into the Memory Mapped Register Range (i.e., this field specifies a DWord offset).Mapped				
		<table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">Programming Notes</th> <th style="text-align: center;">Project</th> </tr> </thead> <tbody> <tr> <td>Bits 22:18 must be zero. Setting these bits could cause a hang due to PM requesting a stop at the same time the request is going to a MMIO space outside the GT core.</td> <td>CHV, BSW</td> </tr> </tbody> </table>		Programming Notes	Project	Bits 22:18 must be zero. Setting these bits could cause a hang due to PM requesting a stop at the same time the request is going to a MMIO space outside the GT core.
	Programming Notes	Project				
	Bits 22:18 must be zero. Setting these bits could cause a hang due to PM requesting a stop at the same time the request is going to a MMIO space outside the GT core.	CHV, BSW				
1:0	<b>Reserved</b>					
	Project:	All				
	Format:	MBZ				
2	31:0	<b>Data DWord</b>				
		Project:	All			
		Format:	U32			
This field specifies the DWord value to be written to the targeted location.						

## MI\_LOAD\_REGISTER\_IMM

MI_LOAD_REGISTER_IMM						
Project:	CHV, BSW					
Source:	BlitterCS					
Length Bias:	2					
<p>The MI_LOAD_REGISTER_IMM command requests a write of up to a DWord constant supplied in the command to the specified Register Offset (i.e., offset into Memory-Mapped Register Range). The register is loaded before the next command is executed.</p> <p>Any offset that is to a destination outside of the GT core will allow the parser to continue once the cycle is at the GT boundry and not destination. Any other address will ensure the destination is updated prior to parsing the next command</p>						
DWord	Bit	Description				
0	31:29	<b>Command Type</b> <table border="1"> <tr> <td>Default Value:</td> <td>0h MI_COMMAND</td> </tr> </table>	Default Value:	0h MI_COMMAND		
	Default Value:	0h MI_COMMAND				
	28:23	<b>MI Command Opcode</b> <table border="1"> <tr> <td>Default Value:</td> <td>22h MI_</td> </tr> </table>	Default Value:	22h MI_		
	Default Value:	22h MI_				
	22:12	<b>Reserved</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ
	Project:	All				
Format:	MBZ					
11:8	<b>Byte Write Disables</b> <table border="1"> <tr> <td>Format:</td> <td>Enable[4] Bit 8 corresponds to Data DWord [7:0]</td> </tr> </table> <p>Range: Must specify a valid register write operation</p> <p>If [11:8] is '1111b', then the register write will not occur. If [11:8] is '0000b', then the register DW will be updated. Any other value, the behavior will be specifically specified by the register or the behavior is undefined.</p>	Format:	Enable[4] Bit 8 corresponds to Data DWord [7:0]			
Format:	Enable[4] Bit 8 corresponds to Data DWord [7:0]					
7:0	<b>DWord Length</b> <table border="1"> <tr> <td>Default Value:</td> <td>1h Excludes DWord (0,1)</td> </tr> <tr> <td>Format:</td> <td>=n Total Length - 2</td> </tr> </table>	Default Value:	1h Excludes DWord (0,1)	Format:	=n Total Length - 2	
Default Value:	1h Excludes DWord (0,1)					
Format:	=n Total Length - 2					
1	31:23	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
	Format:	MBZ				
	22:2	<b>Register Offset</b> <table border="1"> <tr> <td>Format:</td> <td>U21</td> </tr> <tr> <td>Format:</td> <td>MmioAddress[22:2]</td> </tr> </table> <p>This field specifies bits [22:2] of the offset into the Memory Mapped Register Range (i.e., this field specifies a DWord offset).</p>	Format:	U21	Format:	MmioAddress[22:2]
Format:		U21				
Format:	MmioAddress[22:2]					

<b>MI_LOAD_REGISTER_IMM</b>				
		<b>Programming Notes</b>		<b>Project</b>
		Bits 22:18 must be zero. Setting these bits could cause a hang due to PM requesting a stop at the same time the request is going to a MMIO space outside the GT core.		CHV, BSW
	1:0	<b>Reserved</b>		
		Project:	All	
		Format:	MBZ	
2	31:0	<b>Data DWord</b>		
		Mask:	Bytes Write Disables	
		Format:	U32	
		This field specifies the DWord value to be written to the targeted location.		

## MI\_LOAD\_REGISTER\_IMM

<b>MI_LOAD_REGISTER_IMM</b>	
Project:	CHV, BSW
Source:	RenderCS
Length Bias:	2
<p>The MI_LOAD_REGISTER_IMM command requests a write of up to a DWord constant supplied in the command to the specified Register Offset (i.e., offset into Memory-Mapped Register Range).</p> <p>Any offset that is to a destination outside of the GT core will allow the parser to continue once the cycle is at the GT boundry and not destination. Any other address will ensure the destination is updated prior to parsing the next command</p>	
<b>Programming Notes</b>	
<p>A stalling flush must be sent down pipeline before issuing this command. The behavior of this command is controlled by Dword 3, Bit 8 (Disable Register Access) of the RINGBUF register. If this command is disallowed then the command stream converts it to a NOOP.</p> <p>If this command is executed from a BB then the behavior of this command is controlled by Dword 0, Bit 8 (Security Indicator) of the BATCH_BUFFER_START Command. If the batch buffer is insecure then the command stream converts this command to a NOOP. Note that the corresponding ring buffer must allow a register update for this command to execute.</p> <p>To ensure this command gets executed before upcoming commands in the ring, either a stalling pipeControl should be sent after this command, or MMIO 0x20C0 bit 7 should be set to 1.</p> <p>When base address of 0x180000 is added to the Register Offset, when executed will result in updating of the register in the other GT in GTB mode of operation then the GT from which this instruction is executed. When this instruction is executed by Command Streamer with COREID-0 will result in updating the register in GT with COREID-1 and vice versa, when base address of 0x180000 is added to the register offset.</p> <p>The following addresses should NOT be used for LRIs:</p> <ol style="list-style-type: none"> <li>1. 0x8800 - 0x88FF</li> <li>2. &gt;= 0xC0000</li> </ol> <p>Limited LRI cycles to the Display Engine 0x40000-0xBFFFF) are allowed, but must be spaced to allow only one pending at a time. This can be done by issuing an SRM to the same address immediately after each LRI.</p>	
<p>Programming an MMIO register is equivalent to programming a non-pipeline state to the hardware and hence an explicit stalling flush needs to be programmed prior to programming this command. However for certain MMIO registers based on their functionality doing an explicit stalling flush is exempted. Listed below are the exempted registers.</p> <ul style="list-style-type: none"> <li>• 3DPRIM_END_OFFSET - Auto Draw End Offset [CHV, BSW]</li> <li>• 3DPRIM_START_VERTEX - Load Indirect Start Vertex [CHV, BSW]</li> <li>• 3DPRIM_VERTEX_COUNT - Load Indirect Vertex Count [CHV, BSW]</li> <li>• 3DPRIM_INSTANCE_COUNT - Load Indirect Instance Count [CHV, BSW]</li> <li>• 3DPRIM_START_INSTANCE - Load Indirect Start Instance [CHV, BSW]</li> <li>• 3DPRIM_BASE_VERTEX - Load Indirect Base Vertex [CHV, BSW]</li> </ul>	
<p>Writes to the range 0x9400-0x97FF must be either be avoided, or serialized with a read (e.g. STORE_REGISTER_MEM) between them.</p>	

DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 0h MI_COMMAND
		Format: OpCode
	28:23	<b>MI Command Opcode</b>
		Default Value: 22h MI_LOAD_REGISTER_IMM
		Format: OpCode
	22:13	<b>Reserved</b>
		Format: MBZ
12	<b>Reserved</b>	
	Project: CHV, BSW	
11:8	<b>Byte Write Disables</b>	
	Format: Enable[4] Bit 8 corresponds to Data DWord [7:0]	
	Range: Must specify a valid register write operation	
	If [11:8] is '1111b', then this command will behave as a NOOP. Otherwise, the value is forwarded to the destination register.	
7:0	<b>DWord Length</b>	
	Default Value: 1h Excludes DWord (0,1)	
	Format: =n Total Length - 2. Excludes DWord (0,1).	
1	31:23	<b>Reserved</b>
		Format: MBZ
	22:2	<b>Register Offset</b>
		Format: MmioAddress[22:2] This field specifies bits [22:2] of the offset into the Memory Mapped Register Range (i.e., this field specifies a DWord offset).
1:0	<b>Reserved</b>	
	Format: MBZ	
2	31:0	<b>Data DWord</b>
		Mask: Bytes Write Disables
		Format: U32
		This field specifies the DWord value to be written to the targeted location.



## MI\_LOAD\_REGISTER\_IMM

<b>MI_LOAD_REGISTER_IMM</b>			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>The MI_LOAD_REGISTER_IMM command requests a write of up to a DWord constant supplied in the command to the specified Register Offset (i.e., offset into Memory-Mapped Register Range). The register is loaded before the next command is executed.</p> <p>Any offset that is to a destination outside of the GT core will allow the parser to continue once the cycle is at the GT boundry and not destination. Any other address will ensure the destination is updated prior to parsing the next command</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	22h MI_LOAD_REGISTER_IMM
22:12	<b>Reserved</b>		
11:8	<b>Byte Write Disables</b>		
	Format:	Enable[4] (bit 8 corresponds to Data DWord [7:0]).	
Range: Must specify a valid register write operation			
If [11:8] is '1111b', then the register write will not occur. If [11:8] is '0000b', then the register DW will be updated. Any other value, the behavior will be specifically specified by the register or the behavior is undefined.			
7:0	<b>DWord Length</b>		
	Default Value:	0h Excludes DWord (0,1)	
	Format:	=n Total Length - 2	
1	31:23	<b>Reserved</b>	
	22:2	<b>Register Offset</b>	
		Format:	MmioAddress[22:2]
	This field specifies bits [22:2] of the offset into the Memory Mapped Register Range (i.e., this field specifies a DWord offset).Mapped		
<b>Programming Notes</b>			
Bits 22:18 must be zero. Setting these bits could cause a hang due to PM requesting a stop at the same time the request is going to a MMIO space outside the GT core.			
<b>Project</b>			
		CHV, BSW	

<b>MI_LOAD_REGISTER_IMM</b>				
	1:0	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			
2	31:0	<p><b>Data DWord</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 40%;">Format:</td> <td>U32 FormatDesc</td> </tr> </table> <p>This field specifies the DWord value to be written to the targeted location.</p>	Format:	U32 FormatDesc
Format:	U32 FormatDesc			

## MI\_LOAD\_REGISTER\_MEM

<b>MI_LOAD_REGISTER_MEM</b>			
Project:	CHV, BSW		
Source:	RenderCS, BlitterCS, VideoCS, VideoEnhancementCS		
Length Bias:	2		
The MI_LOAD_REGISTER_MEM command requests from a memory location and stores that DWord to a register.			
Programming Notes			
The command temporarily halts commands that will cause cycles down the 3D pipeline.			
The following addresses should NOT be used for MMIO writes: <ul style="list-style-type: none"> <li>• 0x8800 - 0x88FF</li> <li>• &gt;= 0xC0000</li> </ul> Limited MMIO writes cycles to the Display Engine 0x40000-0xBFFFF are allowed, but must be spaced to allow only one pending at a time. This can be done by issuing an SRM to the same address immediately after each MMIO write.			
Any updates to the memory location exercised by this command must be ensured to be coherent in memory prior to programming of this command. This must be achieved by programming MI_ATOMIC (write to scratch space) with "CS STALL" set prior to programming of this command. Example: MI_STORE_REGISTER_MEM (0x2288, 0x2CF0_0000) ..... MI_ATOMIC (MOV, Dummy data, Scratch Address) MI_LOAD_REGISTER_MEM(0x2288, 0x2CF0_0000)			
This command should not be used within a non-privilege batch buffer to access global virtual space, doing so will be treated as privilege access violation. Refer "User Mode Privilege Command" in MI_BATCH_BUFFER_START command section to know HW behavior on encountering privilege access violation.			
This command is not allowed to update the privilege register range when executed from a non-privilege batch buffer.			
Writes to the range 0x9400-0x97FF must be either be avoided, or serialized with a read (e.g. STORE_REGISTER_MEM) between them.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
28:23		<b>MI Command Opcode</b>	
		Default Value:	29h MI_LOAD_REGISTER_MEM
		Format:	OpCode
22		<b>Use Global GTT</b>	
		Format:	Boolean
This bit if set when executing from a non-privileged batch buffer will be treated as privilege access violation. It is allowed for this bit to be clear when executing this command from a			

<b>MI_LOAD_REGISTER_MEM</b>									
	<p>privileged (secure) batch buffer or ring buffer. This command will use the global GTT to translate the Address and this command must be executing from a privileged (secure) batch buffer.</p>								
21	<p><b>Async Mode Enable</b> If this bit is set then the command stream will not wait for completion of this command before executing the next command. Please refer to the LOAD_INDIRECT and Predicate registers for usage of this bit.</p>								
20	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Project:</td> <td></td> </tr> </table>	Project:							
Project:									
19:8	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ						
Format:	MBZ								
7:0	<p><b>DWord Length</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 20%;">Format:</td> <td>=n Total Length - 2. Excludes DWord (0,1).</td> </tr> </table> <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 60%;">Name</th> <th style="width: 25%;">Project</th> </tr> </thead> <tbody> <tr> <td>2h</td> <td>Excludes DWord (0,1) <b>[Default]</b></td> <td>CHV, BSW</td> </tr> </tbody> </table>	Format:	=n Total Length - 2. Excludes DWord (0,1).	Value	Name	Project	2h	Excludes DWord (0,1) <b>[Default]</b>	CHV, BSW
Format:	=n Total Length - 2. Excludes DWord (0,1).								
Value	Name	Project							
2h	Excludes DWord (0,1) <b>[Default]</b>	CHV, BSW							
1	<p>31:23 <b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ						
	Format:	MBZ							
	<p>22:2 <b>Register Address</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>MMIOAddress[22:2]</td> </tr> </table> <p>This field specifies Bits 22:2 of the Register offset the DWord will be written to. As the register address must be DWord-aligned, Bits 1:0 of that address MBZ.</p> <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th style="width: 50%;">Programming Notes</th> <th style="width: 15%;">Project</th> <th style="width: 35%;">Source</th> </tr> </thead> <tbody> <tr> <td>Bits 22:18 must be zero. Setting these bits could cause a hang due to PM requesting a stop at the same time the request is going to a MMIO space outside the GT core.</td> <td>CHV, BSW</td> <td>BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS</td> </tr> </tbody> </table>	Format:	MMIOAddress[22:2]	Programming Notes	Project	Source	Bits 22:18 must be zero. Setting these bits could cause a hang due to PM requesting a stop at the same time the request is going to a MMIO space outside the GT core.	CHV, BSW	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS
Format:	MMIOAddress[22:2]								
Programming Notes	Project	Source							
Bits 22:18 must be zero. Setting these bits could cause a hang due to PM requesting a stop at the same time the request is going to a MMIO space outside the GT core.	CHV, BSW	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS							
<p>1:0 <b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ							
Format:	MBZ								
2..3 <b>Project:</b> CHV, BSW	<p>63:2 <b>Memory Address</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[63:2]</td> </tr> </table> <p>This field specifies the address of the memory location where the register value specified in the DWord above will read from. The address specifies the DWord location of the data. Range = GraphicsVirtualAddress[63:2] for a DWord register GraphicsAddress [63:48] are ignored by the HW and assumed to be in correct canonical form [63:48] == [47].</p>	Project:	CHV, BSW	Format:	GraphicsAddress[63:2]				
	Project:	CHV, BSW							
Format:	GraphicsAddress[63:2]								
1:0	<p><b>Reserved</b></p>								

## MI\_LOAD\_REGISTER\_REG

<b>MI_LOAD_REGISTER_REG</b>			
Project:	CHV, BSW		
Source:	CommandStreamer		
Length Bias:	2		
<p>The MI_LOAD_REGISTER_REG command reads from a source register location and writes that value to a destination register location.</p> <p>Any offset that is to a destination outside of the GT core will allow the parser to continue once the cycle is at the GT boundry and not destination. Any other address will ensure the destination is updated prior to parsing the next command</p>			
<b>Programming Notes</b>			
The command temporarily halts commands that will cause cycles down the 3D pipeline.			
Destination register with mask implemented will not get updated unless the value read from source register has the bits corresponding to the mask bits set. Note that any mask implemented register when read returns "0" for the bits corresponding to mask location. When the source and destination are mask implemented registers, destination register will not get updated with the source register contents.			
This command is not allowed to update the privilege register range when executed from a non-privilege batch buffer.			
Writes to the range 0x9400-0x97FF must be either be avoided, or serialized with a read (e.g. STORE_REGISTER_MEM) between them.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	2Ah
		Format:	OpCode
	22:8	<b>Reserved</b>	
		Format:	MBZ
7:0	<b>DWord Length</b>		
	Default Value:	1h	
	Format:	=n Total Length - 2. Excludes DWord (0,1).	
1	31:23	<b>Reserved</b>	
		<b>Source Register Address</b>	
	22:2	Format: MMIOAddress[22:2]MMIO_Register	
This field specifies Bits 22:2 of the Register offset the DWord will be written to. As the register address must be DWord-aligned, Bits 1:0 of that address MBZ.			

<b>MI_LOAD_REGISTER_REG</b>									
		<table border="1"> <thead> <tr> <th style="text-align: center;">Programming Notes</th> <th style="text-align: center;">Project</th> <th style="text-align: center;">Source</th> </tr> </thead> <tbody> <tr> <td>Bits 22:18 must be zero. Setting these bits could cause a hang due to PM requesting a stop at the same time the request is going to a MMIO space outside the GT core.</td> <td>CHV, BSW</td> <td>BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS</td> </tr> </tbody> </table>	Programming Notes	Project	Source	Bits 22:18 must be zero. Setting these bits could cause a hang due to PM requesting a stop at the same time the request is going to a MMIO space outside the GT core.	CHV, BSW	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS	
Programming Notes	Project	Source							
Bits 22:18 must be zero. Setting these bits could cause a hang due to PM requesting a stop at the same time the request is going to a MMIO space outside the GT core.	CHV, BSW	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS							
	1:0	<b>Reserved</b> Format: _____ MBZ							
2	31:23	<b>Reserved</b> Format: _____ MBZ							
	22:2	<b>Destination Register Address</b> Format: _____ MMIOAddress[22:2]MMIO_Register This field specifies Bits 22:2 of the Register offset the DWord will be written to. As the register address must be DWord-aligned, Bits 1:0 of that address MBZ.							
		<table border="1"> <thead> <tr> <th style="text-align: center;">Programming Notes</th> <th style="text-align: center;">Project</th> <th style="text-align: center;">Source</th> </tr> </thead> <tbody> <tr> <td>Bits 22:18 must be zero. Setting these bits could cause a hang due to PM requesting a stop at the same time the request is going to a MMIO space outside the GT core.</td> <td>CHV, BSW</td> <td>BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS</td> </tr> </tbody> </table>	Programming Notes	Project	Source	Bits 22:18 must be zero. Setting these bits could cause a hang due to PM requesting a stop at the same time the request is going to a MMIO space outside the GT core.	CHV, BSW	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS	
	Programming Notes	Project	Source						
Bits 22:18 must be zero. Setting these bits could cause a hang due to PM requesting a stop at the same time the request is going to a MMIO space outside the GT core.	CHV, BSW	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS							
1:0	<b>Reserved</b> Format: _____ MBZ								

## MI\_LOAD\_SCAN\_LINES\_EXCL

MI_LOAD_SCAN_LINES_EXCL			
Project:	CHV, BSW		
Source:	BlitterCS		
Length Bias:	2		
<p>The MI_LOAD_SCAN_LINES_EXCL command is used to initialize the Scan Line Window registers for a specific Display Pipe. If the display refresh is <i>outside</i> this window the Display Engine asserts a signal that is used by the command parser to process the WAIT_FOR_EVENT command (i.e., the parser will wait while outside). This command overrides the Scan Line Window defined by any previous MI_LOAD_SCAN_LINES_INCL or MI_LOAD_SCAN_LINES_EXCL commands targeting the specific display pipe.</p> <p>Note: The two scan-line numbers are inclusive. If programmed to the same values, that single line defines the region in question.</p> <p>Always place an even number of MI_LOAD_SCAN_LINES_EXCL/INCL at a time into the ring buffer. If only a single MI_LOAD_SCAN_LINES_EXCL/INCL is desired, just add a second identical MI_LOAD_SCAN_LINES_EXCL/INCL command.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	13h MI_LOAD_SCAN_LINES_EXCL
		Format:	OpCode
	22	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	21:19	<b>Display Pipe Select</b>	
		Project:	All
		Format:	U3
This field selects which Display Engine (pipe) this command is targeting.			
<b>Value</b>		<b>Name</b>	<b>Project</b>
0h		Display Pipe A	All
1h		Display Pipe B	All
4h	Display Pipe C	All	
18:17	<b>Reserved</b>		
16:6	<b>Reserved</b>		
5:0	<b>DWord Length</b>		
	Default Value:	0h Excludes DWord (0,1)	
	Format:	=n Total Length - 2	

<b>MI_LOAD_SCAN_LINES_EXCL</b>				
1	31:16	<p><b>Start Scan Line Number</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 10%;">Format:</td> <td>U16 In scan lines, where scan line 0 is the first line of the display frame.</td> </tr> </table> <p>This field specifies the starting scan line number of the Scan Line Window. Range: [0, Display Buffer height in lines-1]</p>	Format:	U16 In scan lines, where scan line 0 is the first line of the display frame.
	Format:	U16 In scan lines, where scan line 0 is the first line of the display frame.		
15:0	<p><b>End Scan Line Number</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 10%;">Format:</td> <td>U16 In scan lines, where scan line 0 is the first line of the display frame.</td> </tr> </table> <p>This field specifies the ending scan line number of the Scan Line Window. Range: [0, Display Buffer height in lines-1]</p>	Format:	U16 In scan lines, where scan line 0 is the first line of the display frame.	
Format:	U16 In scan lines, where scan line 0 is the first line of the display frame.			



## MI\_LOAD\_SCAN\_LINES\_EXCL

MI_LOAD_SCAN_LINES_EXCL			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
<p>The MI_LOAD_SCAN_LINES_EXCL command is used to initialize the Scan Line Window registers for a specific Display Pipe. If the display refresh is <b>outside</b> this window the Display Engine asserts a signal that is used by the command parser to process the WAIT_FOR_EVENT command (i.e., the parser will wait while outside). This command overrides the Scan Line Window defined by any previous MI_LOAD_SCAN_LINES_INCL or MI_LOAD_SCAN_LINES_EXCL commands targeting the specific display pipe. <b>Note:</b> The two scan-line numbers are inclusive. If programmed to the same values, that single line defines the region in question. Always place an even number of MI_LOAD_SCAN_LINES_EXCL/INCL at a time into the ring buffer. If only a single MI_LOAD_SCAN_LINES_EXCL/INCL is desired, just add a second identical MI_LOAD_SCAN_LINES_EXCL/INCL command.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	13h MI_LOAD_SCAN_LINES_EXCL
		Format:	OpCode
	22	<b>Reserved</b>	
	21:19	<b>Display (Plane) Select</b>	
		Format:	U3
		This field selects which display plane is to perform the scanline operation.	
Value		Name	
0h		Display Plane A	
1h		Display Plane B	
2h		Reserved	
3h		Reserved	
4h	Display Plane C		
5h	Reserved		
18:17	<b>Reserved</b>		
16:6	<b>Reserved</b>		
5:0	<b>DWord Length</b>		
	Default Value:	0h	
	Format:	=n Total Length - 2. Excludes DWord (0,1).	

<b>MI_LOAD_SCAN_LINES_EXCL</b>		
1	31:29	<b>Reserved</b>
		Format: <span style="float: right;">MBZ</span>
	28:16	<b>Start Scan Line Number</b>
		Format: U13 In scan lines, where scan line 0 is the first line of the display frame.
		Range: [0, Display Buffer height in lines-1]
		This field specifies the starting scan line number of the Scan Line Window.
	15:13	<b>Reserved</b>
		Format: <span style="float: right;">MBZ</span>
	12:0	<b>End Scan Line Number</b>
		Format: U13 In scan lines, where scan line 0 is the first line of the display frame.
		This field specifies the ending scan line number of the Scan Line Window.
		Range: [0, Display Buffer height in lines-1]

## MI\_LOAD\_SCAN\_LINES\_INCL

MI_LOAD_SCAN_LINES_INCL			
Project:	CHV, BSW		
Source:	BlitterCS		
Length Bias:	2		
<p>The MI_LOAD_SCAN_LINES_INCL command is used to initialize the Scan Line Window registers for a specific Display Engine. If the display refresh is <i>within</i> this window the Display Engine asserts a signal that is used by the command parser to process the WAIT_FOR_EVENT command (i.e., the parser will wait while inside of the window). This command overrides the Scan Line Window defined by any previous MI_LOAD_SCAN_LINES_INCL or MI_LOAD_SCAN_LINES_EXCL commands targeting the specific display.</p> <p>Always place an even number of MI_LOAD_SCAN_LINES_EXCL/INCL at a time into the ring buffer. If only a single MI_LOAD_SCAN_LINES_EXCL/INCL is desired, just add a second identical</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	12h MI_LOAD_SCAN_LINES_INCL
		Format:	OpCode
	22	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	21:19	<b>Display Pipe Select</b>	
		Project:	All
		Format:	U3
		This field selects which Display Engine (pipe) this command is targeting.	
		<b>Value</b>	<b>Name</b>
0h		Display Pipe A	
1h		Display Pipe B	
4h	Display Pipe C		
18:17	<b>Reserved</b>		
16:6	<b>Reserved</b>		
	Project:	CHV, BSW	
	Format:	MBZ	
5:0	<b>DWord Length</b>		
	Default Value:	0h Excludes DWord (0,1)	

<b>MI_LOAD_SCAN_LINES_INCL</b>		
		Format: =n Total Length - 2
1	31:16	<p><b>Start Scan Line Number</b></p> <p>Format: U16 In scan lines, where scan line 0 is the first line of the display frame.</p> <p>This field specifies the starting scan line number of the Scan Line Window. Range: [0, Display Buffer height in lines-1]</p>
	15:0	<p><b>End Scan Line Number</b></p> <p>Format: U16 In scan lines, where scan line 0 is the first line of the display frame.</p> <p>This field specifies the ending scan line number of the Scan Line Window. Range: [0, Display Buffer height in lines-1]</p>

## MI\_LOAD\_SCAN\_LINES\_INCL

MI_LOAD_SCAN_LINES_INCL			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
<p>The MI_LOAD_SCAN_LINES_INCL command is used to initialize the Scan Line Window registers for a specific Display Engine. If the display refresh is <b>within</b> this window the Display Engine asserts a signal that is used by the command parser to process the WAIT_FOR_EVENT command (i.e., the parser will wait while inside the window). This command overrides the Scan Line Window defined by any previous MI_LOAD_SCAN_LINES_INCL or MI_LOAD_SCAN_LINES_EXCL commands targeting the specific display.</p> <p>Always place an even number of MI_LOAD_SCAN_LINES_EXCL/INCL at a time into the ring buffer. If only a single MI_LOAD_SCAN_LINES_EXCL/INCL is desired, just add a second identical MI_LOAD_SCAN_LINES_EXCL/INCL command.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	12h MI_LOAD_SCAN_LINES_INCL
		Format:	OpCode
	22	<b>Reserved</b>	
		Format:	MBZ
	21:19	<b>Display (Plane) Select</b>	
		Project:	CHV, BSW
		Format:	U3
		This field selects which display plane is to perform the scanline operation.	
		<b>Value</b>	<b>Name</b>
		0h	Display Plane A
1h		Display Plane B	
2h		Reserved	
3h		Reserved	
4h		Display Plane C	
5h	Reserved		
18:17	<b>Reserved</b>		
	16:6	<b>Reserved</b>	
Project:		CHV, BSW	
Format:		MBZ	

<b>MI_LOAD_SCAN_LINES_INCL</b>								
	5:0	<p><b>DWord Length</b></p> <table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> <tr> <td>Format:</td> <td>=n Total Length - 2. Excludes DWord (0,1).</td> </tr> </table>	Default Value:	0h	Format:	=n Total Length - 2. Excludes DWord (0,1).		
Default Value:	0h							
Format:	=n Total Length - 2. Excludes DWord (0,1).							
1	31	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Must Be One</td> </tr> </table>	Project:	CHV, BSW	Format:	Must Be One		
		Project:	CHV, BSW					
	Format:	Must Be One						
	30	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ		
		Project:	CHV, BSW					
	Format:	MBZ						
	29	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ				
	Format:	MBZ						
	28:16	<p><b>Start Scan Line Number</b></p> <table border="1"> <tr> <td>Format:</td> <td>U13 In scan lines, where scan line 0 is the first line of the display frame.</td> </tr> <tr> <td colspan="2">Range: [0, Display Buffer height in lines-1]</td> </tr> <tr> <td colspan="2">This field specifies the starting scan line number of the Scan Line window.</td> </tr> </table>	Format:	U13 In scan lines, where scan line 0 is the first line of the display frame.	Range: [0, Display Buffer height in lines-1]		This field specifies the starting scan line number of the Scan Line window.	
		Format:	U13 In scan lines, where scan line 0 is the first line of the display frame.					
Range: [0, Display Buffer height in lines-1]								
This field specifies the starting scan line number of the Scan Line window.								
15:13	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ					
	Format:	MBZ						
12:0	<p><b>End Scan Line Number</b></p> <table border="1"> <tr> <td>Format:</td> <td>U13 In scan lines, where scan line 0 is the first line of the display frame.</td> </tr> <tr> <td colspan="2">Range: [0, Display Buffer height in lines-1]</td> </tr> <tr> <td colspan="2">This field specifies the ending scan line number of the Scan Line Window.</td> </tr> </table>	Format:	U13 In scan lines, where scan line 0 is the first line of the display frame.	Range: [0, Display Buffer height in lines-1]		This field specifies the ending scan line number of the Scan Line Window.		
	Format:	U13 In scan lines, where scan line 0 is the first line of the display frame.						
	Range: [0, Display Buffer height in lines-1]							
This field specifies the ending scan line number of the Scan Line Window.								

## MI\_LOAD\_URB\_MEM

MI_LOAD_URB_MEM						
Project:	CHV, BSW					
Source:	RenderCS					
Length Bias:	2					
The MI_LOAD_URB_MEM command requests from a memory location and stores that DWord to the URB.						
<b>Programming Notes</b>						
The command temporarily halts commands that will cause cycles down the 3D pipeline.						
DWord	Bit	Description				
0	31:29	<b>Command Type</b>				
		Default Value: 0h MI_COMMAND Format: OpCode				
	28:23	<b>MI Command Opcode</b>				
		Default Value: 2Ch MI_LOAD_URB_MEM Format: OpCode				
22:8	<b>Reserved</b>					
7:0	<b>DWord Length</b>					
	Format: =n Total Length - 2. Excludes DWord (0,1).					
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>2h</td> <td>[Default]</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Value	Name	Project	2h	[Default]
Value	Name	Project				
2h	[Default]	CHV, BSW				
1	31:15	<b>Reserved</b>				
		Format: MBZ				
	14:2	<b>URB Address</b> This field specifies Bits 14:2 of the URB offset the DWord will be written in the URB. This command only supports writing below 32KB of the URB space.				
1:0	<b>Reserved</b>					
	Format: MBZ					
2.3 <b>Project:</b> CHV, BSW	63:6	<b>Memory Address</b>				
		Project: CHV, BSW Format: GraphicsAddress[63:6]				
	This field specifies the address of the location of where the value will be read from memory. The value must be in the first DW location of the cache line. Range = GraphicsVirtualAddress[47:6] GraphicsAddress [63:48] are ignored by the HW and assumed to be in correct canonical form [63:48] == [47].					
	5:0	<b>Reserved</b>				

## MI\_MATH

<b>MI_MATH</b>					
Project:	CHV, BSW				
Source:	BlitterCS				
Length Bias:	2				
<p>The MI_MATH command allows software to send instructions to the ALU in the Command Streamer. This command is the means by which the ALU is accessed. ALU instructions form the data payload of the MI_MATH command. An ALU instruction takes one DWord in size. The MI_MATH DWord Length is programmed based on the number of ALU instructions included, limited only by the max DWord Length supported. When the command streamer parses an MI_MATH command, it sends the included ALU instructions to the ALU. The ALU processes any instruction in a single clock. See the ALU section for more details.</p>					
DWord	Bit	Description			
0	31:29	<b>Command Type</b>			
		<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Default Value:</td> <td>0h MI_COMMAND</td> </tr> <tr> <td>Format:</td> <td>OpCode</td> </tr> </table>	Default Value:	0h MI_COMMAND	Format:
	Default Value:	0h MI_COMMAND			
	Format:	OpCode			
28:23	<b>MI Command Opcode</b>				
	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Default Value:</td> <td>1Ah MI_MATH</td> </tr> <tr> <td>Format:</td> <td>OpCode</td> </tr> </table>	Default Value:	1Ah MI_MATH	Format:	OpCode
Default Value:	1Ah MI_MATH				
Format:	OpCode				
22:8	<b>Reserved</b>				
	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ				
7:0	<b>DWord Length</b>				
	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Default Value:</td> <td>0h</td> </tr> <tr> <td>Format:</td> <td>=n Total Length - 2. Excludes DWord (0,1).</td> </tr> </table>	Default Value:	0h	Format:	=n Total Length - 2. Excludes DWord (0,1).
	Default Value:	0h			
Format:	=n Total Length - 2. Excludes DWord (0,1).				
1	31:0	<b>ALU INSTRUCTION 1</b>			
		<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>Table Entry</td> </tr> </table>	Format:	Table Entry	
Format:	Table Entry				
2	31:0	<b>ALU INSTRUCTION 2</b>			
		<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>Table Entry</td> </tr> </table>	Format:	Table Entry	
Format:	Table Entry				
3..n	31:0	<b>ALU INSTRUCTION n</b>			
		<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>Table Entry</td> </tr> </table>	Format:	Table Entry	
Format:	Table Entry				



## MI\_MATH

<b>MI_MATH</b>		
Project:	CHV, BSW	
Source:	VideoCS	
Length Bias:	2	
<p>The MI_MATH command allows software to send instructions to the ALU in the Command Streamer. This command is the means by which the ALU is accessed. ALU instructions form the data payload of the MI_MATH command. An ALU instruction takes one DWord in size. The MI_MATH DWord Length is programmed based on the number of ALU instructions included, limited only by the max DWord Length supported. When the command streamer parses an MI_MATH command, it sends the included ALU instructions to the ALU. The ALU processes any instruction in a single clock. See the ALU section for more details.</p>		
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 0h MI_COMMAND Format: OpCode
	28:23	<b>MI Command Opcode</b>
		Default Value: 1Ah MI_MATH Format: OpCode
22:8	<b>Reserved</b>	
	Format: MBZ	
7:0	<b>DWord Length</b>	
	Default Value: 0h	
	Format: =n Total Length - 2. Excludes DWord (0,1).	
1	31:0	<b>ALU INSTRUCTION 1</b>
	Format: Table Entry	
2	31:0	<b>ALU INSTRUCTION 2</b>
	Format: Table Entry	
3..n	31:0	<b>ALU INSTRUCTION n</b>
	Format: Table Entry	

## MI\_MATH

<b>MI_MATH</b>		
Project:	CHV, BSW	
Source:	VideoEnhancementCS	
Length Bias:	2	
<p>The MI_MATH command allows software to send instructions to the ALU in the Command Streamer. This command is the means by which the ALU is accessed. ALU instructions form the data payload of the MI_MATH command. An ALU instruction takes one DWord in size. The MI_MATH DWord Length is programmed based on the number of ALU instructions included, limited only by the max DWord Length supported. When the command streamer parses an MI_MATH command, it sends the included ALU instructions to the ALU. The ALU processes any instruction in a single clock. See the ALU section for more details.</p>		
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 0h MI_COMMAND Format: OpCode
	28:23	<b>MI Command Opcode</b>
		Default Value: 1Ah MI_MATH Format: OpCode
22:8	<b>Reserved</b>	
	Format: MBZ	
7:0	<b>DWord Length</b>	
	Default Value: 0h	
	Format: =n Total Length - 2. Excludes DWord (0,1).	
1	31:0	<b>ALU INSTRUCTION 1</b>
	Format: Table Entry	
2	31:0	<b>ALU INSTRUCTION 2</b>
	Format: Table Entry	
3..n	31:0	<b>ALU INSTRUCTION n</b>
	Format: Table Entry	

## MI\_MATH

<b>MI_MATH</b>		
Project:	CHV, BSW	
Source:	RenderCS	
Length Bias:	2	
<p>The MI_MATH command allows SW to send instruction to ALU in Render Command Streamer. MI_MATH command is the means by which ALU can be accessed. ALU instructions form the data payload of MI_MATH command, ALU instruction is dword in size. MI_MATH Dword Length should be programmed based on the number of ALU instruction packed, max number is limited by the max Dword Length supported. When MI_MATH command is parsed by command streamer it outputs the payload dwords (ALU instructions) to the ALU. ALU takes single clock to process any given instruction. Refer to B-spec "Command Streamer (CS) ALU Programming" section in Command Streamer Programming.</p>		
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 0h MI_COMMAND
		Format: OpCode
	28:23	<b>MI Command Opcode</b>
		Default Value: 1Ah MI_MATH
		Format: OpCode
	22:8	<b>Reserved</b>
		Format: MBZ
	7:6	<b>Reserved</b>
		Project: CHV, BSW
		Format: MBZ
	5:0	<b>DWord Length</b>
		Default Value: 0h
		Project: CHV, BSW
		Format: =n Total Length - 2. Excludes DWord (0,1).
1	31:0	<b>ALU INSTRUCTION 1</b>
		Format: Table Entry
2	31:0	<b>ALU INSTRUCTION 2</b>
		Format: Table Entry
3..n	31:0	<b>ALU INSTRUCTION n</b>
		Format: Table Entry

# MI\_NOOP

<b>MI_NOOP</b>			
Project:	CHV, BSW		
Source:	VideoEnhancementCS		
Length Bias:	1		
<p>The MI_NOOP command basically performs a "no operation" in the command stream and is typically used to pad the command stream (e.g., in order to pad out a batch buffer to a QWord boundary). However, there is one minor (optional) function this command can perform - a 22-bit value can be loaded into the MI NOPID register. This provides a general-purpose command stream tagging ("breadcrumb") mechanism (e.g., to provide sequencing information for a subsequent breakpoint interrupt).</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	00h MI_NOOP
		Format:	OpCode
	22	<b>Identification Number Register Write Enable</b>	
		Format:	Enable
		<p>This field enables the value in the Identification Number field to be written into the MI NOPID register. If disabled, that register is unmodified - making this command an effective "no operation" function.</p>	
		<b>Value</b>	<b>Name</b>
1		Write th NOP_ID Register	
0	Do not write the NOP_ID register		
21:0	<b>Identification Number</b>		
	Project:	All	
	Format:	U22	
	<p>This field contains a 22-bit number which can be written to the MI NOPID register.</p>		

## MI\_NOOP

<b>MI_NOOP</b>				
Project:	CHV, BSW			
Source:	BlitterCS			
Length Bias:	1			
<p>The MI_NOOP command basically performs a "no operation" in the command stream and is typically used to pad the command stream (e.g., in order to pad out a batch buffer to a QWord boundary). However, there is one minor (optional) function this command can perform - a 22-bit value can be loaded into the MI NOPID register. This provides a general-purpose command stream tagging ("breadcrumb") mechanism (e.g., to provide sequencing information for a subsequent breakpoint interrupt).</p>				
DWord	Bit	Description		
0	31:29	<b>Command Type</b>		
		Default Value:	0h MI_COMMAND	
	28:23	<b>MI Command Opcode</b>		
		Default Value:	0h MI_NOOP	
22	<b>Identification Number Register Write Enable</b>			
		Project:	All	
		Format:	Enable	
	<p>This field enables the value in the Identification Number field to be written into the MI NOPID register. If disabled, that register is unmodified - making this command an effective "no operation" function.</p>			
		<b>Value</b>	<b>Name</b>	<b>Description</b>
	0h	Disable	Do not write the NOP_ID register.	All
	1h	Enable	Write the NOP_ID register.	All
21:0	<b>Identification Number</b>			
		Project:	All	
		Format:	U22	
<p>This field contains a 22-bit number which can be written to the MI NOPID register.</p>				

## MI\_NOOP

<b>MI_NOOP</b>											
Project:	CHV, BSW										
Source:	RenderCS										
Length Bias:	1										
<p>The MI_NOOP command basically performs a "no operation" in the command stream and is typically used to pad the command stream (e.g., in order to pad out a batch buffer to a QWord boundary). However, there is one minor (optional) function this command can perform - a 22-bit value can be loaded into the MI NOPID register. This provides a general-purpose command stream tagging ("breadcrumb") mechanism (e.g., to provide sequencing information for a subsequent breakpoint interrupt).</p>											
<b>Performance</b>		<b>Project</b>									
<p>The MI_NOOP process time is reduced to 1 clock. An example use of the improved NOOP throughput is for some multi-pass media applications where some unwanted media object commands are replaced by MI_NOOP commands without repacking the commands in a batch buffer.</p>		CHV, BSW									
DWord	Bit	Description									
0	31:29	<b>Command Type</b> Default Value: 0h MI_COMMAND									
	28:23	<b>MI Command Opcode</b> Default Value: 0h MI_NOOP									
	22	<b>Identification Number Register Write Enable</b> Format: Enable This field enables the value in the Identification Number field to be written into the MI NOPID register. If disabled, that register is unmodified, making this command an effective "no operation" function. <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disable</td> <td>Do not write the NOP_ID register.</td> </tr> <tr> <td>1h</td> <td>Enable</td> <td>Write the NOP_ID register.</td> </tr> </tbody> </table>	Value	Name	Description	0h	Disable	Do not write the NOP_ID register.	1h	Enable	Write the NOP_ID register.
	Value	Name	Description								
	0h	Disable	Do not write the NOP_ID register.								
1h	Enable	Write the NOP_ID register.									
21:0	<b>Identification Number</b> Format: U22 This field contains a 22-bit number which can be written to the MI NOPID register.										

## MI\_NOOP

<b>MI_NOOP</b>			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	1		
<p>The MI_NOOP command basically performs a "no operation" in the command stream and is typically used to pad the command stream (e.g., in order to pad out a batch buffer to a QWord boundary). However, there is one minor (optional) function this command can perform - a 22-bit value can be loaded into the MI NOPID register. This provides a general-purpose command stream tagging ("breadcrumb") mechanism (e.g., to provide sequencing information for a subsequent breakpoint interrupt).</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	00h MI_NOOP
		Format:	OpCode
	22	<b>Identification Number Register Write Enable</b>	
		Format:	Enable
		This field enables the value in the Identification Number field to be written into the MI NOPID register. If disabled, that register is unmodified - making this command an effective "no operation" function.	
		<b>Value</b>	<b>Name</b>
1		Write the NOP_ID register.	
21:0	<b>Identification Number</b>		
	Format:	U22	
	This field contains a 22-bit number which can be written to the MI NOPID register.		

## MI\_PREDICATE

MI_PREDICATE				
Project:	CHV, BSW			
Source:	RenderCS			
Length Bias:	1			
DWord	Bit	Description		
0	31:29	<b>Command Type</b>		
		Default Value:	0h MI_COMMAND	
		Format:	OpCode	
	28:23	<b>MI Command Opcode</b>		
		Default Value:	0Ch MI_PREDICATE	
		Format:	OpCode	
	22:8	<b>Reserved</b>		
		Format:	MBZ	
	7:6	<b>Load Operation</b>		
		This field controls if/how the Predicate state bit is modified.		
		<b>Value</b>	<b>Name</b>	<b>Description</b>
		0h	KEEP	The Predicate state bit is unmodified.
		1h	Reserved	
		2h	LOAD	The Predicate state bit is loaded with the combine operation result.
	3h	LOADINV	The Predicate state bit is loaded with the inverted combine operation result.	
	5	<b>Reserved</b>		
Format:		MBZ		
4:3	<b>Combine Operation</b>			
	This field controls if/how the result of the compare operation is combined with the current Predicate state bit.			
	<b>Value</b>	<b>Name</b>	<b>Description</b>	
	0h	SET	The combine operation output the compare result unmodified.	
	1h	AND	The combine operation outputs the AND of the compare result and the current Predicate state bit.	
	2h	OR	The combine operation outputs the OR of the compare result and the current Predicate state bit.	
3h	XOR	The combine operation outputs the XOR of the compare result and the current Predicate state bit.		
2	<b>Reserved</b>			
	Format:	MBZ		



<b>MI_PREDICATE</b>																	
1:0	<p><b>Compare Operation</b>                      This field controls how Data DWord 0 and Data DWord 1 fields are used to generate a compare operation result and possibly modify the PredicateData register.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0h</td> <td style="text-align: center;">TRUE</td> <td>The compare operation outputs TRUE. The PredicateData register is unmodified.</td> </tr> <tr> <td style="text-align: center;">1h</td> <td style="text-align: center;">FALSE</td> <td>The compare operation outputs FALSE. The PredicateData register is unmodified.</td> </tr> <tr> <td style="text-align: center;">2h</td> <td style="text-align: center;">SRCS_EQUAL</td> <td>(MItemp0 - MItemp1) is computed and loaded into the PredicateData register. The compare operation outputs (MItemp0 == MItemp1).</td> </tr> <tr> <td style="text-align: center;">3h</td> <td style="text-align: center;">DELTAS_EQUAL</td> <td>(MItemp0 - MItemp1) is computed and compared to the PredicateData register. If the values are equal, the compare operation outputs TRUE, otherwise it outputs FALSE. The PredicateData register is unmodified.</td> </tr> </tbody> </table>		Value	Name	Description	0h	TRUE	The compare operation outputs TRUE. The PredicateData register is unmodified.	1h	FALSE	The compare operation outputs FALSE. The PredicateData register is unmodified.	2h	SRCS_EQUAL	(MItemp0 - MItemp1) is computed and loaded into the PredicateData register. The compare operation outputs (MItemp0 == MItemp1).	3h	DELTAS_EQUAL	(MItemp0 - MItemp1) is computed and compared to the PredicateData register. If the values are equal, the compare operation outputs TRUE, otherwise it outputs FALSE. The PredicateData register is unmodified.
Value	Name	Description															
0h	TRUE	The compare operation outputs TRUE. The PredicateData register is unmodified.															
1h	FALSE	The compare operation outputs FALSE. The PredicateData register is unmodified.															
2h	SRCS_EQUAL	(MItemp0 - MItemp1) is computed and loaded into the PredicateData register. The compare operation outputs (MItemp0 == MItemp1).															
3h	DELTAS_EQUAL	(MItemp0 - MItemp1) is computed and compared to the PredicateData register. If the values are equal, the compare operation outputs TRUE, otherwise it outputs FALSE. The PredicateData register is unmodified.															

## MI\_REPORT\_HEAD

MI_REPORT_HEAD			
Project:	CHV, BSW		
Source:	VideoEnhancementCS		
Length Bias:	1		
<p>The MI_REPORT_HEAD command causes the Head Pointer value of the ring buffer to be written to a cacheable (snooped) system memory location.</p> <p>When the <b>Per-Process Virtual Address Space and Execlist Enable bit</b> is reset: The location written is relative to the address programmed in the Hardware Status Page Address Register. When the <b>Execlist Enable</b> is set, the head pointer will be reported to the PP HW Status Page.</p>			
Programming Notes			
This command must not be executed from a Batch Buffer (Refer to the description of the HWS_PGA register).			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	07h MI_REPORT_HEAD
		Format:	OpCode
	22:0	<b>Reserved</b>	
		Project:	All
		Format:	MBZ

## MI\_REPORT\_HEAD

<b>MI_REPORT_HEAD</b>		
Project:	CHV, BSW	
Source:	BlitterCS	
Length Bias:	1	
<p>The MI_REPORT_HEAD command causes the Head Pointer value of the active ring buffer to be written to a cacheable (snooped) system memory location.</p> <p>When the <b>Execlist Enable</b> bit is reset:                      The location written is relative to the address programmed in the Hardware Status Page Address Register.</p>		
<b>Programming Notes</b>		
<p>This command must not be executed from a Batch Buffer (Refer to the description of the HWS_PGA register).                      When the <b>Execlist Disable</b> is clear, the head pointer will be reported to the PP HW Status Page.</p>		
DWord	Bit	Description
0	31:29	<b>Command Type</b> Default Value: 0h MI_COMMAND
	28:23	<b>MI Command Opcode</b> Default Value: 07h MI_REPORT_HEAD
	22:0	<b>Reserved</b> Project: All Format: MBZ

## MI\_REPORT\_HEAD

<b>MI_REPORT_HEAD</b>		
Project:	CHV, BSW	
Source:	RenderCS	
Length Bias:	1	
<p>The MI_REPORT_HEAD command causes the Head Pointer value of the active ring buffer to be written to a cacheable (snooped) system memory location. When Execlist Enable is set, the head pointer will be reported to the PP HW Status Page. The location written is relative to the address programmed in the Hardware Status Page Address Register.</p>		
<b>Programming Notes</b>		
This command must not be executed from a Batch Buffer. (Refer to the description of the HWS_PGA register.)		
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 0h MI_COMMAND
		Format: OpCode
	28:23	<b>MI Command Opcode</b>
		Default Value: 07h MI_REPORT_HEAD
		Format: OpCode
	22:0	<b>Reserved</b>
		Format: MBZ

## MI\_REPORT\_HEAD

<b>MI_REPORT_HEAD</b>		
Project:	CHV, BSW	
Source:	VideoCS	
Length Bias:	1	
<p>The MI_REPORT_HEAD command causes the Head Pointer value of the ring buffer to be written to a cacheable (snooped) system memory location. When the Per-Process Virtual Address Space and Execlist Enable bits are reset, the location written is relative to the address programmed in the Hardware Status Page Address Register. When the Execlist Enable is set, the head pointer will be reported to the PP HW Status Page.</p>		
<b>Programming Notes</b>		
This command must not be executed from a Batch Buffer (Refer to the description of the HWS_PGA register).		
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 0h MI_COMMAND
		Format: OpCode
	28:23	<b>MI Command Opcode</b>
		Default Value: 07h MI_REPORT_HEAD
		Format: OpCode
	22:0	<b>Reserved</b>
		Format: MBZ

## MI\_RS\_CONTROL

<b>MI_RS_CONTROL</b>	
Project:	CHV, BSW
Source:	RenderCS
Length Bias:	1
The MI_RS_CONTROL command is used to start or stop the Resource Streamer.	
<b>Programming Notes</b>	
<ul style="list-style-type: none"> <li>• This command must be programmed only inside a Resource Streamer enabled batch buffer.</li> <li>• This command provides means to selectively disable or enable Resource Streamer for set of commands in a Resource Streamer enabled batch buffer</li> <li>• On re-enabling the Resource Streamer through this command, command streamer will start Resource Streamer on the next non-sync command of the batch buffer.</li> <li>• This command status is render context save/restored during context switching.</li> <li>• The scope of MI_RS_CONTROL is within the batch buffer it is programmed, it doesn't get carried to the following chained batch buffer or second level batch buffer. RS control status goes back to default mode of Resource Streamer Enabled on all batch buffer arbitration boundaries. Batch buffer arbitration boundaries includes calling a chained or a second level batch buffer through MI_BATCH_BUFFER_START command or terminating a batch buffer through MI_BATCH_BUFFER_END command.</li> <li>• Example:               <ol style="list-style-type: none"> <li>1. MI_BATCH_START (Primary batch buffer with RS enable)</li> <li>2. Command 1 --&gt; CS starts RS</li> <li>3. Command 2</li> <li>4. :</li> <li>5. MI_RS_CONTROL (stop option) -&gt; RS will stop on this command, CS sets RS control status to STOP.</li> <li>6. Command 3</li> <li>7. MI_BATCH_START (2<sup>nd</sup> level batch with RS enable not set, RS control status gets reset to default status of START )</li> <li>8. :</li> <li>9. MI_BATCH_END (Second Level Batch End)</li> <li>10. Command 4 --&gt; CS starts RS here as RS control flag gets reset to START at step-7</li> <li>11. MI_BATCH_BUFFER_END</li> </ol> </li> </ul>	
<b>Workaround</b>	
<p>Workaround:</p> <p>Due to known HW issue "Resource Streamer Control" status of MI_RS_CONTROL command is not context save/restored across context switches. SW must ensure all pool allocations (3DSTATE_BINDING_TABLE_POOL_ALLOC, 3DSTATE_GATHER_POOL_ALLOC, 3DSTATE_DX9_CONSTANT_BUFFER_POOL_ALLOC) are disabled and no Resource Streamer specific commands are programmed when the "Resource Streamer Control" is programmed to "Stop".</p>	

## MI\_RS\_CONTROL

**Example:**

```

.....
MI_RS_CONTROL (Stop Resource Streamer)
3DSTATE_BINDING_TABLE_POOL_ALLOC (Binding Table Pool Disable)
3DSTATE_GATHER_POOL_ALLOC (Gather Pool Disable)
3DSTATE_DX9_CONSTANT_BUFFER_POOL_ALLOC (Constant Buffer Pool Disable)
//Following Commands must not be programmed
//3DSTATE_BINDING_TABLE_EDIT_*
//3DSTATE_GATHER_CONSTANT_*
//3DSTATE_DX9_CONSTANTF_*
.....
MI_RS_CONTROL (Start Resource Streamer)
3DSTATE_BINDING_TABLE_POOL_ALLOC (Binding Table Pool Enable)
3DSTATE_GATHER_POOL_ALLOC (Gather Pool Enable)
3DSTATE_DX9_CONSTANT_BUFFER_POOL_ALLOC (Constant Buffer Pool Enable)
.....
    
```

DWord	Bit	Description		
0	31:29	<b>Command Type</b>		
		Default Value: 0h MI_COMMAND		
		Format: OpCode		
	28:23	<b>MI Command Opcode</b>		
		Default Value: 06h MI_RS_CONTROL		
		Format: OpCode		
	22:1	<b>Reserved</b>		
		Format: MBZ		
	0	0	<b>Resource Streamer Control</b>	
			Format: U1	
This bit specifies whether the command is starting or stopping the Resource Streamer.				
<b>Value</b>			<b>Name</b>	<b>Description</b>
0h			Stop	Stop and disable the Resource Streamer
1h	Start	Start and enable the Resource Streamer		

## MI\_RS\_STORE\_DATA\_IMM

MI_RS_STORE_DATA_IMM			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
The MI_RS_STORE_DATA_IMM command requests a write of the DWord constant supplied in the packet to the specified Memory Address.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	2Bh
		Format:	OpCode
			MI_RS_STORE_DATA_IMM
	22	<b>Reserved</b>	
		Project:	CHV, BSW
			Format:
21	<b>Reserved</b>		
20:8	<b>Reserved</b>		
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	2h	
	Format:	=n Total Length - 2. Excludes DWord (0,1).	
1..2 <b>Project:</b> CHV, BSW	63:2	<b>Destination Address</b>	
		Project:	CHV, BSW
		Format:	GraphicsAddress[63:2]
	<p>This field specifies Bits 47:2 of the Address where the DWord will be stored. GraphicsAddress [63:48] are ignored by the HW and assumed to be in correct canonical form [63:48] == [47].</p> <p>When render engine is PPGTT enabled this Address is translated using PPGTT, else GGTT is used for translation.</p>		
	1	<b>Reserved</b>	
		Project:	CHV, BSW
		Format:	MBZ



<b>MI_RS_STORE_DATA_IMM</b>				
	0	<p><b>Core Mode Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table> <p>If this bit is set then the address will be offset by the Core ID:                      If Core ID 0, then there is no offset                      If Core ID 1, then the Memory is offset by the size of the data.</p>	Project:	CHV, BSW
Project:	CHV, BSW			
3	31:0	<p><b>Data DWord 0</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>U32</td> </tr> </table> <p>This field specifies the DWord value to be written to the targeted location.</p>	Format:	U32
Format:	U32			

## MI\_SEMAPHORE\_SIGNAL

<b>MI_SEMAPHORE_SIGNAL</b>			
Project:	CHV, BSW		
Source:	CommandStreamer		
Length Bias:	2		
<p>This command is used to signal the target engine stating the memory semaphore update occurrence to one of its contexts with <b>Target Context ID</b>. MI_SEMPHORE_SIGNAL and MI_SEMAPHORE_WAIT together replace the MI_SEMAPHORE_MBOX command. MI_ATOMIC (non-posted) command will be programmed prior to this command to update the semaphore data in memory.</p>			
Programming Notes		Source	
<p>[All Command Streamers]: When SW intends to use semaphore signaling between Command streamers, it must avoid lite restores in HW by programming "Force Restore" bit to '1' in context descriptor during context submission, this is required to avoid known HW issue.</p>			
Workaround		Project	
Workaround: Post-Sync operation bit must not be set when Target Engine Select is set to RCS.		CHV, BSW	
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	1Bh MI_SEMAPHORE_SIGNAL
		Format:	OpCode
	22	<b>Reserved</b>	
		Format:	MBZ
	21	<b>Post-Sync Operation</b>	
		Project:	CHV, BSW
Source:		RenderCS	
Value		Name	Description
0h		No Post Sync Operation	Command is executed as usual.
1h	Post Sync Operation	MI_SEMAPHORE_SIGNAL command is executed as a pipelined PIPE_CONTROL flush command with Semaphore Signal as post sync operation. Flush completion only guarantees the workload prior to this command is pushed till Windower unit and completion of any outstanding	

<b>MI_SEMAPHORE_SIGNAL</b>																	
	flushes issued prior to this command.																
<b>Programming Notes</b>																	
<p>Any desired pipeline flush operation can be achieved by programming PIPE_CONTROL command prior to this command.</p> <p>When this bit is set Command Streamer sends a flush down the pipe and the atomic operation is saved as post sync operation. Command streamer goes on executing the following commands. Atomic operation saved as post sync operation is executed at some point later on completion of corresponding flush issued.</p> <p>When this bit is set atomic semaphore signal operation will be out of order with rest of the MI commands programmed in the ring buffer or batch buffer, it will be in order with respect to the post sync operations resulting due to PIPE_CONTROL command.</p> <p>This bit must not be set due to known HW issues.</p>																	
<b>Workaround</b>																	
<p>Workaround: "Post Sync Operation" bit must not be set when MI_SEMAPHORE_SIGNAL command is programmed by GPGPU and MEDIA workloads (i.e when PIPELINE_SELECT command is set to GPGPU or MEDIA). This is to WA FFDOP CG issue.</p> <p>Workaround: Post-Sync operation bit must not be set when Target Engine Select is set to RCS.</p>																	
21	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Source:</td> <td>BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Source:	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS	Format:	MBZ												
Source:	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS																
Format:	MBZ																
20:18	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ														
Format:	MBZ																
17:15	<p><b>Target Engine Select</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This field selects the target engine to which SIGNAL will be send to.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>RCS</td> </tr> <tr> <td>1h</td> <td>VCS0</td> </tr> <tr> <td>2h</td> <td>BCS</td> </tr> <tr> <td>3h</td> <td>VECS</td> </tr> <tr> <td>4h</td> <td>VCS1</td> </tr> <tr> <td>5h-7h</td> <td>Reserved</td> </tr> </tbody> </table>	Project:	CHV, BSW	Value	Name	0h	RCS	1h	VCS0	2h	BCS	3h	VECS	4h	VCS1	5h-7h	Reserved
Project:	CHV, BSW																
Value	Name																
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14:8	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ														
Format:	MBZ																
7:0	<b>DWord Length</b>																

<b>MI_SEMAPHORE_SIGNAL</b>						
		<table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> <tr> <td>Format:</td> <td>=n</td> </tr> </table> <p>Total Length - 2. Excludes DWord (0,1).</p>	Default Value:	0h	Format:	=n
Default Value:	0h					
Format:	=n					
1	31:0	<p><b>Target Context ID</b></p> <table border="1"> <thead> <tr> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td> <p>In execlist based scheduling this field contains the Context ID corresponding to the context of the target engine that this command is signaling. Target engine waiting on MI_SEMAPHORE_WAIT in signal mode will re-fetch the data from memory or comparison if its context ID is same as this signaled Context ID. When execlists are enabled, Target engine on receiving this Context ID sends message to the SHIM if it doesn't have the context with the same Context ID running. Message send to SHIM carries the Context ID which will be looked at by UC for rescheduling the signaled Context ID. Target engine waiting on MI_SEMAPHORE_WAIT in signal mode will fetch data from memory for comparison on receiving signal irrespective of the context id received.</p> </td> </tr> <tr> <td> <p>In ring buffer mode of scheduling this field doesn't have any relevance.</p> </td> </tr> </tbody> </table>	Description	<p>In execlist based scheduling this field contains the Context ID corresponding to the context of the target engine that this command is signaling. Target engine waiting on MI_SEMAPHORE_WAIT in signal mode will re-fetch the data from memory or comparison if its context ID is same as this signaled Context ID. When execlists are enabled, Target engine on receiving this Context ID sends message to the SHIM if it doesn't have the context with the same Context ID running. Message send to SHIM carries the Context ID which will be looked at by UC for rescheduling the signaled Context ID. Target engine waiting on MI_SEMAPHORE_WAIT in signal mode will fetch data from memory for comparison on receiving signal irrespective of the context id received.</p>	<p>In ring buffer mode of scheduling this field doesn't have any relevance.</p>	
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<p>In ring buffer mode of scheduling this field doesn't have any relevance.</p>						

## MI\_SEMAPHORE\_WAIT

<b>MI_SEMAPHORE_WAIT</b>	
Project:	CHV, BSW
Source:	CommandStreamer
Length Bias:	2
Description	
<p>This command supports memory based Semaphore WAIT. Memory based semaphores will be used for synchronization between the Producer and the Consumer contexts. Producer and Consumer Contexts could be running on different engines or on the same engine inside GT. Running on the same engine is only possible when execlists are enabled. Producer Context implements a Signal and Consumer context implements a Wait. Command Streamer on parsing this command fetches data from the Semaphore Address mentioned in this command and compares it with the inline Semaphore Data Dword.</p> <ul style="list-style-type: none"> <li>• If comparison passes, the command streamer moves to the next command.</li> <li>• When execlists are enabled, if comparison fails Command streamer switches out the context. Context switch can be inhibited by setting "Inhibit Synchronous Context Switch" in CTXT_SR_CTL register.</li> <li>• In ring buffer mode of scheduling or Execlist with "Inhibit Synchronous context Switch", if comparison fails, Command Streamer evaluates the Compare Operation based on the Wait Mode until the compare operation is true or Wait is canceled by SW.</li> <li>• Exec-List Scheduling: CS generates semaphore wait interrupt to the scheduler when MI_SEMAPHORE_WAIT command is un-successful and when "Inhibit Synchronous Context Switch" is set. Scheduler can use this interrupt to preempt the context waiting on semaphore wait.</li> </ul> <p>MI_SEMPHORE_SIGNAL and MI_SEMAPHORE_WAIT together replace the MI_SEMAPHORE_MBOX command.</p>	
Programming Notes	Source
<p><b>Render CS Only:</b> SW must always program PIPE_CONTROL with "CS Stall" and "Render Target Cache Flush Enable" set prior to programming MI_SEMAPHORE_WAIT command for GPGPU workloads i.e when pipeline select is GPGPU via PIPELINE_SELECT command. This is required to achieve better GPGPU preemption latencies for certain programming sequences. If programming PIPE_CONTROL has performance implications then preemption latencies can be trade off against performance by not implementing this programming note.</p>	RenderCS
<p><b>Render CS Only:</b> Ring Buffer Scheduling: CS doesn't generate semaphore wait interrupt to the scheduler when MI_SEMAPHORE_WAIT command is un-successful.</p>	RenderCS
<p><b>[Ring Buffer Mode Of scheduling] [BlitterCS, VideoCS, VideoEnhancementCS, VideoCS2: Command Streamers Only]:</b> HW loses Page Directory (PPGTT) information on becoming IDLE. SW must always program the PD information following MI_SEMAPHORE_WAIT command. This will ensure Page Directory information gets reprogrammed after exiting IDLE flow triggered on MI_SEMAPHORE_WAIT command. Alternatively SW can disable IDLE flows on MI_SEMAPHORE_WAIT by setting "Semaphore Wait Event IDLE Message Disable" bit in "BCS_ECOSKPD" register.</p>	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS

<b>MI_SEMAPHORE_WAIT</b>				
<b>Workaround</b>				
Workaround: [All Command Streamers][Ring Buffer Mode of Scheduling]: MI_SEMAPHORE_WAIT command must be always programmed with "Wait Mode" set to "Polling Mode"				
DWord	Bit	Description		
0	31:29	<b>Command Type</b>		
		Default Value:	0h MI_COMMAND	
		Format:	OpCode	
	28:23	<b>MI Command Opcode</b>		
		Default Value:	1Ch MI_SEMAPHORE_WAIT	
		Format:	OpCode	
	22	<b>Memory Type</b>	This bit will be ignored and treated as if clear when executing from a non-privileged batch buffer. It is allowed for this bit to be clear when executing this command from a privileged (secure) batch buffer. This bit <i>must</i> be 1 if the <b>Per Process GTT Enable</b> bit is clear.	
		<b>Value</b>	<b>Name</b>	<b>Description</b>
		0h	Per Process Graphics Address	
		1h	Global Graphics Address	This command will use the global GTT to translate the Address and this command must be executing from a privileged (secure) batch buffer.
21:18	<b>Reserved</b>			
	Format:	MBZ		
17	<b>Reserved</b>			
	Format:	MBZ		
16	<b>Reserved</b>			
	Project:	CHV, BSW		
15	<b>Wait Mode</b>	This bit specifies the WAIT behavior when the semaphore comparison fails and before the context is switched out.		
	<b>Value</b>	<b>Name</b>	<b>Description</b>	
	1h	Polling Mode	In this mode HW periodically reads the semaphore data from memory for comparison until it is context switched out. Periodicity will be mentioned in a SEMA_WAIT_POLL register.	
	0h	Signal Mode	In this mode HW will reacquire the semaphore data from memory on receiving SIGNAL with the same Context ID. In ring buffer mode of scheduling Context ID associated with SIGNAL is ignored and always treated as a match.	
14:12	<b>Compare Operation</b>			
	This field specifies the operation that will be executed to create the result that will either			

<b>MI_SEMAPHORE_WAIT</b>																													
		<p>allow the context to continue or wait.</p> <p>SAD = Semaphore Address Data SDD = Semaphore Data Dword</p>																											
		<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>SAD_GREATER_THAN_SDD</td> <td>If Indirect fetched data is greater than inline data then continue.</td> </tr> <tr> <td>1h</td> <td>SAD_GREATER_THAN_OR_EQUAL_SDD</td> <td>If Indirect fetched data is greater than or equal to inline data then continue.</td> </tr> <tr> <td>2h</td> <td>SAD_LESS_THAN_SDD</td> <td>If Indirect fetched data is less than inline data then continue.</td> </tr> <tr> <td>3h</td> <td>SAD_LESS_THAN_OR_EQUAL_SDD</td> <td>If Indirect fetched data is less than or equal to inline data then continue.</td> </tr> <tr> <td>4h</td> <td>SAD_EQUAL_SDD</td> <td>If Indirect fetched data is equal to inline data then continue.</td> </tr> <tr> <td>5h</td> <td>SAD_NOT_EQUAL_SDD</td> <td>If Indirect fetched data is not equal to inline data then continue.</td> </tr> <tr> <td>6h</td> <td>Reserved</td> <td></td> </tr> <tr> <td>7h</td> <td>Reserved</td> <td></td> </tr> </tbody> </table>	Value	Name	Description	0h	SAD_GREATER_THAN_SDD	If Indirect fetched data is greater than inline data then continue.	1h	SAD_GREATER_THAN_OR_EQUAL_SDD	If Indirect fetched data is greater than or equal to inline data then continue.	2h	SAD_LESS_THAN_SDD	If Indirect fetched data is less than inline data then continue.	3h	SAD_LESS_THAN_OR_EQUAL_SDD	If Indirect fetched data is less than or equal to inline data then continue.	4h	SAD_EQUAL_SDD	If Indirect fetched data is equal to inline data then continue.	5h	SAD_NOT_EQUAL_SDD	If Indirect fetched data is not equal to inline data then continue.	6h	Reserved		7h	Reserved	
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Format:	MBZ																												
	7:0	<p><b>DWord Length</b></p> <table border="1"> <tr> <td>Default Value:</td> <td>2h</td> </tr> <tr> <td>Format:</td> <td>=n Total Length - 2. Excludes DWord (0,1)</td> </tr> </table>	Default Value:	2h	Format:	=n Total Length - 2. Excludes DWord (0,1)																							
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Format:	=n Total Length - 2. Excludes DWord (0,1)																												
1	31:0	<p><b>Semaphore Data Dword</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>This Data dword is supplied by software to control execution of the command buffer. This value is used as part of the comparison to result in waiting or continuing in the command parser if enabled.</p>	Format:	U32																									
Format:	U32																												
2..3 <b>Project:</b> CHV, BSW	63:2	<p><b>Semaphore Address</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[63:2]</td> </tr> </table> <p>This field is the Graphics Memory Address of the 32-bit value for the semaphore. GraphicsAddress [63:48] are ignored by the HW and assumed to be in correct canonical form.</p>	Project:	CHV, BSW	Format:	GraphicsAddress[63:2]																							
Project:	CHV, BSW																												
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	1:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table>	Project:	CHV, BSW																									
Project:	CHV, BSW																												

## MI\_SEMAPHORE\_WAIT

		Format:	MBZ
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## MI\_SEMAPHORE\_WAIT

<b>MI_SEMAPHORE_WAIT</b>			
Project:	CHV, BSW		
Source:	BlitterCS		
Length Bias:	2		
Description			
<p>This command supports memory based Semaphore WAIT. Memory based semaphores will be used for synchronization between the Producer and the Consumer contexts. Producer and Consumer Contexts could be running on different engines or on the same engine inside GT, same engine only possible when execlists are enabled. Producer Context implements a Signal and Consumer context implements a Wait. Command Streamer on parsing this command fetches data from the Semaphore Address mentioned in this command and compares it with the inline Semaphore Data Dword.</p> <ul style="list-style-type: none"> <li>• If comparison passes, the command streamer moves to the next command.</li> <li>• When execlists are enabled, if comparison fails Command streamer switches out the context. Context switch can be inhibited by setting "Inhibit Synchronous Context Switch" in BCS_CTXT_SR_CTL register.</li> <li>• In ring buffer mode of scheduling or Execlist with "Inhibit Synchronous context Switch", if comparison fails, Command Streamer evaluates the Compare Operation based on the Wait Mode until the compare operation is true or Wait is canceled by SW.</li> <li>• BCS always generates an interrupt to the scheduler on encountering semaphore failure.</li> </ul>			
MI_SEMPHORE_SIGNAL and MI_SEMAPHORE_WAIT together replace the MI_SEMAPHORE_MBOX command.			
Programming Notes			
<p>[Ring Buffer Mode Of scheduling][Video CS, Video Enhancement CS, Blitter CS]: HW loses Page Directory (PPGTT) information on becoming IDLE. SW must always program the PD information following MI_SEMAPHORE_WAIT command. This will ensure Page Directory information gets reprogrammed after exiting IDLE flow triggered on MI_SEMAPHORE_WAIT command. Alternatively SW can disable IDLE flows on MI_SEMAPHORE_WAIT by setting "Semaphore Wait Event IDLE Message Disable" bit in "BCS_ECOSKPD" register.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	1Ch MI_SEMAPHORE_WAIT
		Format:	OpCode
22	<b>Memory Type</b>	This bit will be ignored and treated as if clear when executing from a non-privileged batch buffer. It is allowed for this bit to be clear when executing this command from a privileged (secure) batch buffer. This bit must be '1' if the Per Process GTT Enable bit is clear.	

<b>MI_SEMAPHORE_WAIT</b>			
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0h	Per Process Graphics Address	
	1h	Global Graphics Address	This command will use the global GTT to translate the Address and this command must be executing from a privileged (secure) batch buffer.
21:16	<b>Reserved</b>		
15	<b>Wait Mode</b> This bit specifies the WAIT behavior when the semaphore comparison fails and before the context is switched out.		
	Value	Name	Description
	1h	Polling Mode	In this mode HW periodically reads the semaphore data from memory for comparison until it is context switched out. Periodicity will be mentioned in a SEMA_WAIT_POLL register.
	0h	Signal Mode	In this mode HW will reacquire the semaphore data from memory on receiving SIGNAL with the same Context ID. In ring buffer mode of scheduling Context ID associated with SIGNAL is ignored and always treated as a match.
14:12	<b>Compare Operation</b> This field specifies the operation that will be executed to create the result that will either allow the context to continue or wait. If the below operation is TRUE then SAD = Semaphore Address Data SDD = Semaphore Data Dword		
	Value	Name	Description
	0h	SAD > SDD	If Indirect fetched data is greater than inline data then continue
	1h	SAD >= SDD	If Indirect fetched data is greater than or equal to inline data then continue.
	2h	SAD < SDD	If Indirect fetched data is less than inline data then continue.
	3h	SAD <= SDD	If Indirect fetched data is less than or equal to inline data then continue.
	4h	SAD == SDD	If Indirect fetched data is equal to inline data then continue.
	5h	SAD != SDD	If Indirect fetched data is not equal to inline data then continue.
	6h	Reserved	
	7h	Reserved	
11:8	<b>Reserved</b> Format: <span style="float: right;">MBZ</span>		
7:0	<b>DWord Length</b> Default Value: <span style="float: right;">2h Excludes DWord (0,1)</span>		

<b>MI_SEMAPHORE_WAIT</b>				
		<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">=n</td> </tr> </table> <p>Total Length - 2</p>	Format:	=n
Format:	=n			
1	31:0	<p><b>Semaphore Data Dword</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U32</td> </tr> </table> <p>Data dword to compare. The Data dword is supplied by software to control execution of the command buffer. If the data at Semaphore Address is greater than this dword, the execution of the command buffer continues.</p>	Format:	U32
Format:	U32			
2..3	63:48	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
	47:2	<p><b>Semaphore Address</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 40%;">Format:</td> <td style="width: 60%;">GraphicsAddress[47:2]</td> </tr> </table> <p>This field is the Graphics Memory Address of the 32 bit value for the semaphore.</p>	Format:	GraphicsAddress[47:2]
Format:	GraphicsAddress[47:2]			
1:0	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ			

## MI\_SEMAPHORE\_WAIT

<b>MI_SEMAPHORE_WAIT</b>			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
<p>This command supports memory based Semaphore WAIT. Memory based semaphores will be used for synchronization between the Producer and the Consumer contexts. Producer and Consumer Contexts could be running on different engines or on the same engine inside GT. Running on the same engine is only possible when execlists are enabled. Producer Context implements a Signal and Consumer context implements a Wait. Command Streamer on parsing this command fetches data from the Semaphore Address mentioned in this command and compares it with the inline Semaphore Data Dword.</p> <ul style="list-style-type: none"> <li>• If comparison passes, the command streamer moves to the next command.</li> <li>• When execlists are enabled, if comparison fails Command streamer switches out the context. Context switch can be inhibited by setting "Inhibit Synchronous Context Switch" in CTXT_SR_CTL register</li> <li>• . In ring buffer mode of scheduling or Execlist with "Inhibit Synchronous context Switch", if comparison fails, Command Streamer evaluates the Compare Operation based on the Wait Mode until the compare operation is true or Wait is canceled by SW.</li> <li>• Exec-List Scheduling: CS generates semaphore wait interrupt to the scheduler when MI_SEMAPHORE_WAIT command is un-successful and when "Inhibit Synchronous Context Switch" is set. Scheduler can use this interrupt to preempt the context waiting on semaphore wait.</li> </ul> <p>MI_SEMAPHORE_SIGNAL and MI_SEMAPHORE_WAIT together replace the MI_SEMAPHORE_MBOX command.</p>			
<b>Programming Notes</b>			
<p><b>Render CS Only:</b> SW must always program PIPE_CONTROL with "CS Stall" and "Render Target Cache Flush Enable" set prior to programming MI_SEMAPHORE_WAIT command for GPGPU workloads i.e when pipeline select is GPGPU via PIPELINE_SELECT command. This is required to achieve better GPGPU preemption latencies for certain programming sequences. If programming PIPE_CONTROL has performance implications then preemption latencies can be trade off against performance by not implementing this programming note.</p>			
<p><b>Render CS Only:</b> Ring Buffer Scheduling: CS doesn't generate semaphore wait interrupt to the scheduler when MI_SEMAPHORE_WAIT command is un-successful.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	1Ch MI_SEMAPHORE_WAIT
		Format:	OpCode
22	<b>Memory Type</b>	This bit will be ignored and treated as if clear when executing from a non-privileged batch	

## MI\_SEMAPHORE\_WAIT

		buffer. It is allowed for this bit to be clear when executing this command from a privileged (secure) batch buffer. This bit <i>must</i> be 1 if the <b>Per Process GTT Enable</b> bit is clear.	
		<b>Value</b>	<b>Name</b>
		<b>Description</b>	
	0h	Per Process Graphics Address	
	1h	Global Graphics Address	This command will use the global GTT to translate the Address and this command must be executing from a privileged (secure) batch buffer.
21:16	<b>Reserved</b>		
15	<b>Wait Mode</b>		
	This bit specifies the WAIT behavior when the semaphore comparison fails and before the context is switched out.		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	1h	Polling Mode	In this mode HW periodically reads the semaphore data from memory for comparison until it is context switched out. Periodicity will be mentioned in a SEMA_WAIT_POLL register.
	0h	Signal Mode	In this mode HW will reacquire the semaphore data from memory on receiving SIGNAL with the same Context ID. In ring buffer mode of scheduling Context ID associated with SIGNAL is ignored and always treated as a match.
14:12	<b>Compare Operation</b>		
	This field specifies the operation that will be executed to create the result that will either allow the context to continue or wait.		
	SAD = Semaphore Address Data SDD = Semaphore Data Dword		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0h	SAD_GREATER_THAN_SDD	If Indirect fetched data is greater than inline data then continue.
	1h	SAD_GREATER_THAN_OR_EQUAL_SDD	If Indirect fetched data is greater than or equal to inline data then continue.
	2h	SAD_LESS_THAN_SDD	If Indirect fetched data is less than inline data then continue.
	3h	SAD_LESS_THAN_OR_EQUAL_SDD	If Indirect fetched data is less than or equal to inline data then continue.
	4h	SAD_EQUAL_SDD	If Indirect fetched data is equal to inline data then continue.
	5h	SAD_NOT_EQUAL_SDD	If Indirect fetched data is not equal to inline data then continue.
	6h	Reserved	

<b>MI_SEMAPHORE_WAIT</b>		
	7h	Reserved
	11:8	<b>Reserved</b>
	7:0	<b>DWord Length</b>
		Default Value: 2h
		Format: =n Total Length - 2. Excludes DWord (0,1)
1	31:0	<b>Semaphore Data Dword</b>
		Format: U32
		Data dword to compare. The Data dword is supplied by software to control execution of the command buffer. If the data at <b>Semaphore Address</b> is greater than this dword, the execution of the command buffer continues.
2	31:2	<b>Semaphore Address</b>
		Format: GraphicsAddress[31:2]
		This field is the Graphics Memory Address of the 32-bit value for the semaphore.
	1:0	<b>Reserved</b>
3	31:16	<b>Reserved</b>
	15:0	<b>Semaphore Address High</b>
		Format: GraphicsAddress[47:32]
		This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space.

## MI\_SEMAPHORE\_WAIT

<b>MI_SEMAPHORE_WAIT</b>		
Project:	CHV, BSW	
Source:	VideoCS	
Length Bias:	2	
<p>This command supports memory based Semaphore WAIT. Memory based semaphores will be used for synchronization between the Producer and the Consumer contexts. Producer and Consumer Contexts could be running on different engines or on the same engine inside GT, same engine only possible when execlists are enabled. Producer Context implements a Signal and Consumer context implements a Wait.</p> <p>Command Streamer on parsing this command fetches data from the Semaphore Address mentioned in this command and compares it with the inline Semaphore Data Dword.</p> <ul style="list-style-type: none"> <li>• If comparison passes, the command streamer moves to the next command.</li> <li>• When execlists are enabled, if comparison fails Command streamer switches out the context. Context switch can be inhibited by setting "Inhibit Synchronous Context Switch" in VCS_CTXT_SR_CTL register.</li> <li>• In ring buffer mode of scheduling or Execlist with "Inhibit Synchronous context Switch", if comparison fails, Command Streamer evaluates the Compare Operation based on the Wait Mode until the compare operation is true or Wait is canceled by SW.</li> <li>• VCS always generates an interrupt to the scheduler on encountering semaphore failure.</li> </ul> <p>MI_SEMPHORE_SIGNAL and MI_SEMAPHORE_WAIT together replace the MI_SEMAPHORE_MBOX command.</p>		
<b>Programming Notes</b>		
<p>[Ring Buffer Mode Of scheduling][Video CS]: HW loses Page Directory (PPGTT) information on becoming IDLE. SW must always program the PD information following MI_SEMAPHORE_WAIT command. This will ensure Page Directory information gets reprogrammed after exiting IDLE flow triggered on MI_SEMAPHORE_WAIT command. Alternatively SW can disable IDLE flows on MI_SEMAPHORE_WAIT command by setting "Semaphore Wait Event IDLE Message Disable" bit in "VCS_ECOSKPD" register.</p>		
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value:
	Format:	OpCode
	28:23	<b>MI Command Opcode</b>
		Default Value:
	Format:	OpCode
22	<b>Memory Type</b>	
	This bit will be ignored and treated as if clear when executing from a non-privileged batch buffer. It is allowed for this bit to be clear when executing this command from a privileged (secure) batch buffer. This bit <i>must</i> be '1' if the <b>Per Process GTT Enable</b> bit is clear.	
	<b>Value</b>	<b>Name</b>
0h	Per Process Graphics Address	

<b>MI_SEMAPHORE_WAIT</b>			
21:16	<b>Reserved</b>		
	Format:	MBZ	
	15	<b>Wait Mode</b>	
		This bit specifies the WAIT behavior when the semaphore comparison fails and before the context is switched out.	
		<b>Value</b>	<b>Name</b> <b>Description</b>
	1h	Polling Mode	In this mode HW periodically reads the semaphore data from memory for comparison until it is context switched out. Periodicity will be mentioned in a SEMA_WAIT_POLL register.
	0h	Signal Mode	In this mode HW will reacquire the semaphore data from memory on receiving SIGNAL with the same Context ID. In ring buffer mode of scheduling Context ID associated with SIGNAL is ignored and always treated as a match.
	14:12	<b>Compare Operation</b>	
		This field specifies the operation that will be executed to create the result that will either allow the context to continue or wait. If the below operation is TRUE then	
		<b>Value</b>	<b>Name</b> <b>Description</b>
0h		SAD > SDD	If Indirect fetched data is greater than inline data then continue.
1h		SAD >= SDD	If Indirect fetched data is greater than or equal to inline data then continue.
2h		SAD < SDD	If Indirect fetched data is less than inline data then continue.
3h		SAD <= SDD	If Indirect fetched data is less than or equal to inline data then continue.
4h		SAD == SDD	If Indirect fetched data is equal to inline data then continue.
5h		SAD != SDD	If Indirect fetched data is not equal to inline data then continue.
6h		Reserved	
7h	Reserved		
<b>Programming Notes</b>			
SAD = Semaphore Address Data SDD = Semaphore Data Dword			
11:8	<b>Reserved</b>		
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	2h Excludes DWord (0,1)	
	Format:	=n	
	Total Length - 2		
1	31:0	<b>Semaphore Data Dword</b>	



<b>MI_SEMAPHORE_WAIT</b>				
		<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>U32</td> </tr> </table> <p>Data dword to compare. The Data dword is supplied by software to control execution of the command buffer. If the data at <b>Semaphore Address</b> is greater than this dword, the execution of the command buffer continues.</p>	Format:	U32
Format:	U32			
2	31:2	<p><b>Semaphore Address</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>GraphicsVirtualAddress[31:2]</td> </tr> </table> <p>This field is the Graphics Memory Address of the 32 bit value for the semaphore.</p>	Format:	GraphicsVirtualAddress[31:2]
	Format:	GraphicsVirtualAddress[31:2]		
1:0	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ			
3	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
15:0	<p><b>Semaphore Address High</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space.</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			

## MI\_SEMAPHORE\_WAIT

### MI\_SEMAPHORE\_WAIT

Project: CHV, BSW  
 Source: VideoEnhancementCS  
 Length Bias: 2

This command supports memory based Semaphore WAIT. Memory based semaphores will be used for synchronization between the Producer and the Consumer contexts. Producer and Consumer Contexts could be running on different engines or on the same engine inside GT, same engine only possible when execlists are enabled. Producer Context implements a Signal and Consumer context implements a Wait. Command Streamer on parsing this command fetches data from the Semaphore Address mentioned in this command and compares it with the inline Semaphore Data Dword.

- If comparison passes, the command streamer moves to the next command.
- When execlists are enabled, if comparison fails Command streamer switches out the context. Context switch can be inhibited by setting "Inhibit Synchronous Context Switch" in VECS\_CTXT\_SR\_CTL register.
- In ring buffer mode of scheduling or execlist with "Inhibit Synchronous context Switch", if comparison fails, Command Streamer evaluates the Compare Operation based on the Wait Mode until the compare operation is true or Wait is canceled by SW.
- VECS always generates an interrupt to the scheduler on encountering semaphore failure.

MI\_SEMPHORE\_SIGNAL and MI\_SEMAPHORE\_WAIT together replace the MI\_SEMAPHORE\_MBOX command.

#### Programming Notes

[Ring Buffer Mode Of scheduling][Video Enhancement CS]: HW loses Page Directory (PPGTT) information on becoming IDLE. SW must always program the PD information following MI\_SEMAPHORE\_WAIT command. This will ensure Page Directory information gets reprogrammed after exiting IDLE flow triggered on MI\_SEMAPHORE\_WAIT command. Alternatively SW can disable IDLE flows on MI\_SEMAPHORE\_WAIT by setting "Semaphore Wait Event IDLE Message Disable" bit in "VECS\_ECOSKPD" register.

DWord	Bit	Description		
0	31:29	<b>Command Type</b>		
		Default Value: 0h MI_COMMAND		
	Format: OpCode			
	28:23	<b>MI Command Opcode</b>		
		Default Value: 1Ch MI_SEMAPHORE_WAIT		
	Format: OpCode			
22	<b>Memory Type</b>			
	This bit will be ignored and treated as if clear when executing from a non-privileged batch buffer. It is allowed for this bit to be clear when executing this command from a privileged (secure) batch buffer. This bit <i>must</i> be '1' if the <b>Per Process GTT Enable</b> bit is clear.			
	<table border="1" style="width: 100%;"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Per Process Graphics Address</td> </tr> </tbody> </table>	Value	Name	0h
Value	Name			
0h	Per Process Graphics Address			

<b>MI_SEMAPHORE_WAIT</b>			
21:16	<b>Reserved</b>		
	Format:	MBZ	
	15	<b>Wait Mode</b> This bit specifies the WAIT behavior when the semaphore comparison fails and before the context is switched out.	
		<b>Value</b>	<b>Name</b>
		<b>Description</b>	
	1h	Polling Mode	In this mode HW periodically reads the semaphore data from memory for comparison until it is context switched out. Periodicity will be mentioned in a SEMA_WAIT_POLL register.
	0h	Signal Mode	In this mode HW will reacquire the semaphore data from memory on receiving SIGNAL with the same Context ID. In ring buffer mode of scheduling Context ID associated with SIGNAL is ignored and always treated as a match.
	14:12	<b>Compare Operation</b> This field specifies the operation that will be executed to create the result that will either allow the context to continue or wait. If the below operation is TRUE then	
		<b>Value</b>	<b>Name</b>
		<b>Description</b>	
0h		SAD > SDD	If Indirect fetched data is greater than inline data then continue.
1h		SAD >= SDD	If Indirect fetched data is greater than or equal to inline data then continue.
2h		SAD < SDD	If Indirect fetched data is less than inline data then continue.
3h		SAD <= SDD	If Indirect fetched data is less than or equal to inline data then continue.
4h		SAD == SDD	If Indirect fetched data is equal to inline data then continue.
5h		SAD != SDD	If Indirect fetched data is not equal to inline data then continue.
6h		Reserved	
7h	Reserved		
<b>Programming Notes</b>			
SAD = Semaphore Address Data SDD = Semaphore Data Dword			
11:8	<b>Reserved</b>		
	7:0	<b>DWord Length</b>	
Default Value:		2h Excludes DWord (0,1)	
Format:		=n	
Total Length - 2			
1	31:0	<b>Semaphore Data Dword</b>	

<b>MI_SEMAPHORE_WAIT</b>				
		<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>U32</td> </tr> </table> <p>Data dword to compare. The Data dword is supplied by software to control execution of the command buffer. If the data at <b>Semaphore Address</b> is greater than this dword, the execution of the command buffer continues.</p>	Format:	U32
Format:	U32			
2	31:2	<p><b>Semaphore Address</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>GraphicsVirtualAddress[31:2]</td> </tr> </table> <p>This field is the Graphics Memory Address of the 32 bit value for the semaphore.</p>	Format:	GraphicsVirtualAddress[31:2]
	Format:	GraphicsVirtualAddress[31:2]		
1:0	<b>Reserved</b>			
3	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
15:0	<p><b>Semaphore Address High</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space.</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			

## MI\_SET\_CONTEXT

<b>MI_SET_CONTEXT</b>			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
<p>The MI_SET_CONTEXT command is used to specify the logical context associated with the hardware context. A logical context is an area in memory used to store hardware context information, and the context is referenced via a 2KB-aligned pointer. If the (new) logical context is different (i.e., at a different memory address), the device saves the current HW context values to the current logical context address, and then restores (loads) the new logical context by reading the context from the new address and loading it into the hardware context state. If the logical context address specified in this command matches the current logical context address, this command is effectively treated as a NOOP. Specific to the Render command stream only. This command also includes some controls over the context save/restore process. The Force Restore bit can be used to refresh the on-chip device state from the same memory address if the indirect state buffers have been modified. The Restore Inhibit bit can be used to prevent the new context from being loaded at all. This must be used to prevent an uninitialized context from being loaded. Once software has initialized a context (by setting all state variables to initial values via commands), the context can then be stored and restored normally. When switching from a generic media context to a 3D context, the generic media state must be cleared via the Generic Media State Clear bit 16 in PIPE_CONTROL (or bit 4 in MI_FLUSH) before saving 3D context. MI_SET_CONTEXT commands are permitted only within a ring buffer (not within a batch buffer).</p>			
<b>Programming Notes</b>			
This command is legal only if Execlist Enable in the GFX_MODE register is reset. Otherwise, execlists must be used to switch context in lieu of MI_SET_CONTEXT.			
This command needs to be always followed by a single MI_NOOP instruction to workaround a silicon issue.			
[CHV, BSW]: MI_ARB_ON_OFF with 'Arbitration Enable Reset' set should be programmed before an MI_SET_CONTEXT command. MI_ARB_ON_OFF with 'Arbitration Enable' set should be programmed after an MI_SET_CONTEXT command.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
Default Value:		18h MI_SET_CONTEXT	
Format:		OpCode	
22:8	<b>Reserved</b>		
1	31:12	<b>Logical Context Address</b>	
		Default Value:	0h
		Format:	=n Total Length - 2. Excludes DWord (0,1).

<b>MI_SET_CONTEXT</b>							
	<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[31:12]LogicalContext</td> </tr> </table>	Project:	CHV, BSW	Format:	GraphicsAddress[31:12]LogicalContext		
Project:	CHV, BSW						
Format:	GraphicsAddress[31:12]LogicalContext						
	<table border="1"> <tr> <th colspan="2" style="text-align: center;">Description</th> </tr> <tr> <td colspan="2"> <p>This field contains the 4KB-aligned graphics memory address of the Logical Context that is to be loaded into the hardware context. If this address is equal to the CCID register associated with the current ring, no load will occur. Prior to loading this new context, the device will save the existing context as required. After the context switch operation completes, this address will be loaded into the associated CCID register.</p> </td> </tr> <tr> <td colspan="2"> <p>This field needs to be 4KB aligned virtual address.</p> </td> </tr> </table>	Description		<p>This field contains the 4KB-aligned graphics memory address of the Logical Context that is to be loaded into the hardware context. If this address is equal to the CCID register associated with the current ring, no load will occur. Prior to loading this new context, the device will save the existing context as required. After the context switch operation completes, this address will be loaded into the associated CCID register.</p>		<p>This field needs to be 4KB aligned virtual address.</p>	
Description							
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11:10	<table border="1"> <tr> <td colspan="2"><b>Reserved</b></td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	<b>Reserved</b>		Format:	MBZ		
<b>Reserved</b>							
Format:	MBZ						
9	<b>Reserved</b>						
8	<table border="1"> <tr> <td colspan="2"><b>Reserved, Must be 1</b></td> </tr> <tr> <td>Format:</td> <td>Must Be One</td> </tr> </table>	<b>Reserved, Must be 1</b>		Format:	Must Be One		
<b>Reserved, Must be 1</b>							
Format:	Must Be One						
7:5	<b>Reserved</b>						
4	<table border="1"> <tr> <td colspan="2"><b>Core Mode Enable</b></td> </tr> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>If set the Context Image will be offset based off the Core ID:            If Core ID 0, no offset            If Core ID 1, 36KB Offset</p>	<b>Core Mode Enable</b>		Project:	CHV, BSW	Format:	Enable
<b>Core Mode Enable</b>							
Project:	CHV, BSW						
Format:	Enable						
3	<table border="1"> <tr> <td colspan="2"><b>Resource Streamer State Save Enable</b></td> </tr> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>If set, the resource streamer state identified in the Logical Context Data section of the Memory Data Formats chapter is saved as part of switching away from this logical context. This bit will be stored in the associated CCID register to control the context save operation when switching away from this context (as part of a subsequent MI_SET_CONTEXT command).</p>	<b>Resource Streamer State Save Enable</b>		Project:	CHV, BSW	Format:	Enable
<b>Resource Streamer State Save Enable</b>							
Project:	CHV, BSW						
Format:	Enable						
2	<table border="1"> <tr> <td colspan="2"><b>Resource Streamer State Restore Enable</b></td> </tr> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>If set, the resource streamer state identified in the Logical Context Data section of the Memory Data Formats chapter is loaded (or restored) as part of switching to this logical context. This bit affects the switch (if required) to the context specified in Logical Context Address. This bit will also be stored in the associated CCID register to control a subsequent context save operation when switching to this context (as part of a subsequent ring buffer switch).</p>	<b>Resource Streamer State Restore Enable</b>		Project:	CHV, BSW	Format:	Enable
<b>Resource Streamer State Restore Enable</b>							
Project:	CHV, BSW						
Format:	Enable						
1	<b>Force Restore</b>						

<b>MI_SET_CONTEXT</b>	
	<p>When switching to this logical context a comparison between Logical Context Address and the contents of the CCID register is performed. Normally, matching addresses prevent a context restore from occurring; however, when this bit is set a context restore is forced to occur. This bit cannot be set with Restore Inhibit. Note: This bit is not saved in the associated CCID register. It only affects the processing of this command.</p>
0	<p><b>Restore Inhibit</b>                      If set, the restore of the HW context from the logical context specified by Logical Context Address is inhibited (i.e., the existing HW context values are maintained). This bit must be used to prevent the loading of an uninitialized logical context. If clear, the context switch proceeds normally. This bit cannot be set with Force Restore. Note: This bit is not saved in the associated CCID register. It only affects the processing of this command.</p>

# MI\_SET\_PREDICATE

<b>MI_SET_PREDICATE</b>		
Project:	CHV, BSW	
Source:	RenderCS	
Length Bias:	1	
Description		
<p>This command sets the Predication Check for the subsequent commands in the command buffer except for MI_SET_PREDICATE itself. Render Command Streamer NOOPs the following commands based on the PREDICATE_ENABLE from MI_SET_PREDICATE, MI_SET_PREDICATE_RESULT and MI_SET_PREDICATE_RESULT_2 status. Resource Streamer doesn't take any action of parsing MI_SET_PREDICATE, this command is similar to any other command which is not meant for resource streamer.</p> <p>Executing MI_SET_PREDICATE command sets PREDICATE_ENABLE bits in MI_MODE register, MI_MODE register gets render context save restored.</p>		
Programming Notes		
<ul style="list-style-type: none"> <li>MI_SET_PREDICATE predication scope must be confined within a Batch Buffer to set of commands.</li> <li>MI_SET_PREDICATE with Predicate Enable Must always have a corresponding MI_SET_PREDICATE with Predicate Disable within the same Batch Buffer.</li> <li>MI_ARB_CHK command must be programmed outside the Predication Scope of MI_SET_PREDICATE.</li> <li>MI_SET_PREDICATE Predication Scope must not involve any RC6 triggering events.</li> </ul> <p>Only the following command(s) can be programmed between the MI_SET_PREDICATE command enabled for predication: 3DSTATE_URB_VS 3DSTATE_URB_HS 3DSTATE_URB_DS 3DSTATE_URB_GS 3DSTATE_PUSH_CONSTANT_ALLOC_VS 3DSTATE_PUSH_CONSTANT_ALLOC_HS 3DSTATE_PUSH_CONSTANT_ALLOC_DS 3DSTATE_PUSH_CONSTANT_ALLOC_GS 3DSTATE_PUSH_CONSTANT_ALLOC_PS MI_LOAD_REGISTER_IMM MEDIA_VFE_STATE MEDIA_OBJECT MEDIA_OBJSCT_WALKER MEDIA_INTERFACE_DESCRIPTOR_LOAD 3DSTATE_WM_HZ_OP</p>		
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 0h MI_COMMAND
	Format: OpCode	
	28:23	<b>MI Command Opcode</b>
Default Value: 01h MI_SET_PREDICATE		
Format: OpCode		
22:4	<b>Reserved</b>	
3:0	<b>PREDICATE ENABLE</b>	
	Project: CHV, BSW	
This field sets the predication logic in render command streamer when parsed. Predicate Disable is the default mode of operation.		



## MI\_SET\_PREDICATE

		Value	Name	Description
		0h	NOOP Never	Predication is Disabled and RCS will process commands as usual.
		1h	NOOP on Result2 clear	Following Commands will be NOOPED by RCS only if the MI_PREDICATE_RESULT_2 is clear.
		2h	NOOP on Result2 set	Following Commands will be NOOPED by RCS only if the MI_PREDICATE_RESULT_2 is set.
		3h	NOOP on Result clear	Following Commands will be NOOPED by RCS only if the MI_PREDICATE_RESULT is clear.
		4h	NOOP on Result set	Following Commands will be NOOPED by RCS only if the MI_PREDICATE_RESULT is set.
		5h	Execute when one slice enabled.	Following Commands will be Executed by RCS only when one slice is enabled.
		6h	Execute when two slices are enabled.	Following Commands will be Executed by RCS only when two slices are enabled.
		7h	Execute when three slices are enabled.	Following Commands will be Executed by RCS only when all the three slices are enabled.
		8h- Ah	Reserved	
		Bh, Ch	Reserved	
		Dh, Eh	Reserved	
		Fh	NOOP Always	Following Commands will be NOOPED by RCS unconditionally.

## MI\_STORE\_DATA\_IMM

<b>MI_STORE_DATA_IMM</b>			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>The MI_STORE_DATA_IMM command requests a write of the QWord or DWord constant supplied in the packet to the specified Memory Address. This command also supports writing to consecutive dword or qword memory locations from the starting address. As the write targets a System Memory Address, the write operation is coherent with the CPU cache (i.e., the processor cache is snooped).</p>			
<b>Programming Notes</b>			
<p>This command can be used for general software synchronization through variables in cacheable memory (i.e., where software does not need to poll un-cached memory or device registers).</p>			
<p>This command simply initiates the write operation with command execution proceeding normally. Although the write operation is guaranteed to complete "eventually", there is no mechanism to synchronize command execution with the completion (or even initiation) of these operations.</p>			
<p>This command should not be used within a non_privilege batch buffer to access global virtual space, doing so will be treated as privilege access violation. Refer "User Mode Privilege Command" in MI_BATCH_BUFFER_START command section to know HW behavior on encountering privilege access violation.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	20h MI_STORE_DATA_IMM
		Format:	OpCode
	22	<b>Use Global GTT</b>	
		Format:	U1
<p>If set, this command will use the global GTT to translate the Address and this command must be executing from a privileged (secure) batch or ring buffer. If clear, the PPGTT will be used. It is allowed for this bit to be clear when executing this command from a privileged (secure) batch buffer. This bit must be '1' if the Per Process GTT Enable bit is clear.</p>			
21	<b>Store Qword</b>	Format:	U1
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0h	Store Dword	If set, this command generates dword writes to memory. Number of dwords generated depends upon the number of 'Data Dword' programmed in the command. If 'x' number of data dwords are programmed in the command it results in 'x' dword writes to memory.

<b>MI_STORE_DATA_IMM</b>			
	1h	Store Qword	If set, this command generates Qword writes to memory, two 'Data Dword' are paired to form a Qword. Number of qwords generated depends upon the number of 'Data Dword' programmed in the command. If 'x' number of data dwords are programmed in the command it results in 'x/2' qword writes to memory.
	20:10	<b>Reserved</b>	
		Format:	MBZ
	9:0	<b>DWord Length</b>	
		Default Value:	0h Excludes DWord (0,1)
		Format:	=n Total Length - 2
1..2	63:2	<b>Destination Address</b>	
		Format:	GraphicsAddress[63:2]
		This field specifies the 4GB aligned base address within the host's 64-bit virtual address space. As the store address must be DWord-aligned, Bits 1:0 of that address MBZ. This address must be 8B aligned if "Store Qword" is enabled. GraphicsAddress [63:48] are ignored by the HW and assumed to be in correct canonical form [63:48] == [47].	
	1:0	<b>Reserved</b>	
		Format:	MBZ
3	31:0	<b>Data DWord 0</b>	
		Format:	U32 FormatDesc
		This field specifies the DWord value to be written to the targeted location. For a QWord write this DWord is the lower DWord of the QWord to be reported (DW 0).	
4	31:0	<b>Data DWord 1</b>	
		Format:	U32 FormatDesc
		This field specifies the upper DWord value to be written to the targeted QWord location (DW 1).	

## MI\_STORE\_DATA\_IMM

<b>MI_STORE_DATA_IMM</b>			
Project:	CHV, BSW		
Source:	VideoEnhancementCS		
Length Bias:	2		
<p>The MI_STORE_DATA_IMM command requests a write of the QWord or DWord constant supplied in the packet to the specified Memory Address. This command also supports writing to consecutive dword or qword memory locations from the starting address. As the write targets a System Memory Address, the write operation is coherent with the CPU cache (i.e., the processor cache is snooped).</p>			
<b>Programming Notes</b>			
<p>This command should not be used within a "non_privilege" batch buffer to access global virtual space, doing so will be treated as privilege access violation. Refer "User Mode Privilege Command" in MI_BATCH_BUFFER_START command section to know HW behavior on encountering privilege access violation. This command can be used within ring buffers and/or "privilege" batch buffers. If used within a non-privilege batch buffer, <b>Use Global GTT</b> must be clear. This command can be used for general software synchronization through variables in cacheable memory (i.e., where software does not need to poll un-cached memory or device registers). This command simply initiates the write operation with command execution proceeding normally. Although the write operation is guaranteed to complete "eventually", there is no mechanism to synchronize command execution with the completion (or even initiation) of these operations.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	20h MI_STORE_DATA_IMM
		Format:	OpCode
	22	<b>Use Global GTT</b>	
		Project:	All
		Format:	U1
	<p>If set, this command will use the global GTT to translate the Address and this command must be executing from a privileged (secure) batch buffer. If clear, the PPGTT will be used. It is allowed for this bit to be clear when executing this command from a privileged (secure) batch buffer. This bit must be '1' if the Per Process GTT Enable bit is clear.</p>		
21	<b>Store Qword</b>		
	Value	Name	Description
	0h	Store Dword	If set, this command generates dword writes to memory. Number of dwords generated depends upon the number of 'Data Dword' programmed in the command. If 'x' number of data dwords are programmed in the command it results in 'x' dword writes to memory.

<b>MI_STORE_DATA_IMM</b>			
	1h	Store Qword	If set, this command generates Qword writes to memory, two 'Data Dword' are paired to form a Qword. Number of qwords generated depends upon the number of 'Data Dword' programmed in the command. If 'x' number of data dwords are programmed in the command it results in 'x/2' qword writes to memory.
	20:10	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	9:0	<b>DWord Length</b>	
		Default Value:	0h Excludes DWord (0,1)
		Format:	=n Total Length - 2
1	31:2	<b>Address</b>	
		Format:	GraphicsAddress[31:2]U32(2)
		This field specifies Bits 31:2 of the Address where the DWord will be stored. As the store address must be DWord-aligned, Bits 1:0 of that address MBZ. This address must be 8B aligned for a store "QW" command.	
	1:0	<b>Reserved</b>	
		Format:	MBZ
2	31:16	<b>Reserved</b>	
		Format:	MBZ
	15:0	<b>Address High</b>	
		Format:	GraphicsAddress[47:32]U16
		This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space.	
3	31:0	<b>Data DWord 0</b>	
		Format:	U32
		This field specifies the DWord value to be written to the targeted location. For a QWord write this DWord is the lower DWord of the QWord to be reported (DW 0).	
4	31:0	<b>Data DWord 1</b>	
		Format:	U32
		This field specifies the upper DWord value to be written to the targeted QWord location (DW 1).	

## MI\_STORE\_DATA\_IMM

<b>MI_STORE_DATA_IMM</b>										
Project:	CHV, BSW									
Source:	BlitterCS									
Length Bias:	2									
Description										
<p>The MI_STORE_DATA_IMM command requests a write of the QWord constant supplied in the packet to the specified Memory Address. As the write targets a System Memory Address, the write operation is coherent with the CPU cache (i.e., the processor cache is snooped).</p> <p>This command supports writing to multiple consecutive dword or qword memory locations from the starting address.</p>										
Programming Notes										
<p>This command can be used for general software synchronization through variables in cacheable memory (i.e., where software does not need to poll un-cached memory or device registers). However, the cacheable nature of the transaction is determined by the setting of the "mapping type" in the GTT entry. This command simply initiates the write operation with command execution proceeding normally. Although the write operation is guaranteed to complete "eventually", there is no mechanism to synchronize command execution with the completion (or even initiation) of these operations. All writes to memory generated using this command are expected to finish in order.</p> <p>This command should not be used within a "non_privilege" batch buffer to access global virtual space, doing so will be treated as privilege access violation. Refer "User Mode Privilege Command" in MI_BATCH_BUFFER_START command section to know HW behavior on encountering privilege access violation.</p>										
DWord	Bit	Description								
0	31:29	<b>Command Type</b> Default Value: 0h MI_COMMAND								
	28:23	<b>MI Command Opcode</b> Default Value: 20h MI_STORE_DATA_IMM								
	22	<b>Use Global GTT</b> Project: All This bit must be '1' if the Per Process GTT Enable bit is clear. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Per Process Graphics Address</td> <td></td> </tr> <tr> <td>1h</td> <td>Global Graphics Address</td> <td>This command will use the global GTT to translate the Address and this command must be executing from a privileged (secure) batch buffer.</td> </tr> </tbody> </table>	Value	Name	Description	0h	Per Process Graphics Address		1h	Global Graphics Address
Value	Name	Description								
0h	Per Process Graphics Address									
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<b>MI_STORE_DATA_IMM</b>											
	21	<p><b>Store Qword</b></p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Store Dword</td> <td>If set, this command generates dword writes to memory. Number of dwords generated depends upon the number of "Data Dword" programmed in the command. If 'x' number of data dwords are programmed in the command it results in "x" dword writes to memory.</td> </tr> <tr> <td>1h</td> <td>Store Qword</td> <td>If set, this command generates Qword writes to memory, two "Data Dword" are paired to form a Qword. Number of qwords generated depends upon the number of "Data Dword" programmed in the command. If 'x' number of data dwords are programmed in the command it results in "x/2" qword writes to memory.</td> </tr> </tbody> </table>	Value	Name	Description	0h	Store Dword	If set, this command generates dword writes to memory. Number of dwords generated depends upon the number of "Data Dword" programmed in the command. If 'x' number of data dwords are programmed in the command it results in "x" dword writes to memory.	1h	Store Qword	If set, this command generates Qword writes to memory, two "Data Dword" are paired to form a Qword. Number of qwords generated depends upon the number of "Data Dword" programmed in the command. If 'x' number of data dwords are programmed in the command it results in "x/2" qword writes to memory.
	Value	Name	Description								
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9:0	<p><b>DWord Length</b></p> <table border="1"> <tr> <td>Default Value:</td> <td>2h Excludes DWord (0,1) = 2 for DWord, 3 for QWord</td> </tr> <tr> <td>Format:</td> <td>=n Total Length - 2</td> </tr> </table>	Default Value:	2h Excludes DWord (0,1) = 2 for DWord, 3 for QWord	Format:	=n Total Length - 2						
Default Value:	2h Excludes DWord (0,1) = 2 for DWord, 3 for QWord										
Format:	=n Total Length - 2										
1 <b>Project:</b> CHV, BSW	31:2	<p><b>Address</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[31:2]U32(2)</td> </tr> </table> <p>This field specifies Bits 31:2 of the Address where the DWord will be stored. As the store address must be DWord-aligned, Bits 1:0 of that address MBZ. This address must be 8B aligned for a store "QW" command.</p>	Project:	CHV, BSW	Format:	GraphicsAddress[31:2]U32(2)					
	Project:	CHV, BSW									
	Format:	GraphicsAddress[31:2]U32(2)									
1	<b>Reserved</b>										
0	<p><b>Core Mode Enable</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>This bit is set then the address will be offset by the Core ID: If Core ID 0, then there is no offset If Core ID 1, then the Memory is offset by the size of the data(32b or 64b based off number of DW length).</p>	Project:	CHV, BSW	Format:	U1						
Project:	CHV, BSW										
Format:	U1										
2 <b>Project:</b> CHV, BSW	31:16	<b>Reserved</b>									
	15:0	<p><b>Address High</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[47:32]U32(2)</td> </tr> </table> <p>This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space.</p>	Project:	CHV, BSW	Format:	GraphicsAddress[47:32]U32(2)					
Project:	CHV, BSW										
Format:	GraphicsAddress[47:32]U32(2)										
3	31:0	<p><b>Data DWord 0</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>This field specifies the DWord value to be written to the targeted location. For a QWord write this DWord is the lower DWord of the QWord to be reported (DW 0).</p>	Project:	All	Format:	U32					
Project:	All										
Format:	U32										

<b>MI_STORE_DATA_IMM</b>						
4	31:0	<p><b>Data DWord 1</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>This field specifies the upper DWord value to be written to the targeted QWord location (DW 1).</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					



## MI\_STORE\_DATA\_IMM

<b>MI_STORE_DATA_IMM</b>			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
Description			
<p>The MI_STORE_DATA_IMM command requests a write of the QWord constant supplied in the packet to the specified Memory Address. As the write targets a System Memory Address, the write operation is coherent with the CPU cache (i.e., the processor cache is snooped).</p> <p>This command supports writing to multiple consecutive dwords or qwords memory locations from the starting address.</p>			
Programming Notes			
<ul style="list-style-type: none"> <li>This command should not be used within a "non-privilege" batch buffer to access global virtual space, doing so will be treated as privilege access violation. Refer "User Mode Privilege Command" in MI_BATCH_BUFFER_START command section to know HW behavior on encountering privilege access violation. This command can be used within ring buffers and/or privilege batch buffers to access global virtual space.</li> <li>This command can be used for general software synchronization through variables in cacheable memory (i.e., where software does not need to poll un-cached memory or device registers).</li> <li>This command simply initiates the write operation with command execution proceeding normally. Although the write operation is guaranteed to complete eventually, there is no mechanism to synchronize command execution with the completion (or even initiation) of these operations.</li> </ul> <p>Number of consecutive dwords or qwords programmed must be restricted such that the DWord Length doesn't exceed 0x3FE, i.e single command supports updating 1021 consecutive dword locations or 510 qword locations.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	20h MI_STORE_DATA_IMM
		Format:	OpCode
22	<b>Use Global GTT</b>		
	Project:	All	
	Format:	Boolean	

<b>MI_STORE_DATA_IMM</b>																							
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If set, this command will use the global GTT to translate the Address and this command must be executing from a privileged (secure) batch buffer. If clear, the PPGTT will be used. It is allowed for this bit to be clear when executing this command from a privileged (secure) batch buffer. This bit must be '1' if the Per Process GTT Enable bit is clear.																							
21	<table border="1" style="width: 100%;"> <thead> <tr> <th colspan="2">Store Qword</th> </tr> </thead> <tbody> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Boolean</td> </tr> <tr> <td colspan="2">If set, this command generates Qword writes to memory, two "Data Dword" are paired to form a Qword. Number of qwords generated depends upon the number of "Data Dword" programmed in the command. If 'x' number of "Data Dwords" are programmed in this command it results in "x/2" qword writes to memory. If reset this command generates Dwords writes to memory. Number of dwords generated depends upon the number of "Data Dword" programmed in the command. If 'x' number of "Data Dwords" are programmed in this command it results in "x" dword writes to memory.</td> </tr> </tbody> </table>	Store Qword		Project:	CHV, BSW	Format:	Boolean	If set, this command generates Qword writes to memory, two "Data Dword" are paired to form a Qword. Number of qwords generated depends upon the number of "Data Dword" programmed in the command. If 'x' number of "Data Dwords" are programmed in this command it results in "x/2" qword writes to memory. If reset this command generates Dwords writes to memory. Number of dwords generated depends upon the number of "Data Dword" programmed in the command. If 'x' number of "Data Dwords" are programmed in this command it results in "x" dword writes to memory.															
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<b>MI_STORE_DATA_IMM</b>				
3	31:0	<p><b>Data DWord 0</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U32</td> </tr> </table> <p>This field specifies the DWord value to be written to the targeted location. For a QWord write this DWord is the lower DWord of the QWord to be reported (DW 0).</p>	Format:	U32
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4	31:0	<p><b>Data DWord 1</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U32</td> </tr> </table> <p>This field specifies the upper DWord value to be written to the targeted QWord location (DW 1).</p>	Format:	U32
Format:	U32			

## MI\_STORE\_DATA\_INDEX

MI_STORE_DATA_INDEX			
Project:	CHV, BSW		
Source:	VideoEnhancementCS		
Length Bias:	2		
<p>The MI_STORE_DATA_INDEX command requests a write of the data constant supplied in the packet to the specified offset from the System Address defined by the Hardware Status Page Address Register. As the write targets a System Address, the write operation is coherent with the CPU cache (i.e., the processor cache is snooped).</p>			
<b>Programming Notes</b>			
<ul style="list-style-type: none"> <li>Use of this command with an invalid or uninitialized value in the Hardware Status Page Address Register is UNDEFINED.</li> <li>This command can be used for general software synchronization through variables in cacheable memory (i.e., where software does not need to poll uncached memory or device registers).</li> <li>This command simply initiates the write operation with command execution proceeding normally. Although the write operation is guaranteed to complete "eventually", there is no mechanism to synchronize command execution with the completion (or even initiation) of these operations.</li> </ul>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	21h MI_STORE_DATA_INDEX
		Format:	OpCode
	22	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	21	<b>Use Per-Process Hardware Status Page</b>	
Project:		CHV, BSW	
<p>If this bit is set, this command will index into the per-process hardware status page at offset 0K from the LRCA. If clear, the Global Hardware Status Page will be indexed. This bit must be '0' if the Execlist Enable bit is clear.</p>			
20:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	

<b>MI_STORE_DATA_INDEX</b>							
	7:0	<b>DWord Length</b>					
		Default Value: 0h Excludes DWord (0,1) = 2 for QWord					
		Project: All Format: =n Total Length - 2					
1	31:12	<b>Reserved</b>					
		Project: All Format: MBZ					
	11:2	<b>Offset</b>					
		Project: All					
		Format: U10 Zero-based DWord offset into the HW status page					
		Format: GraphicsAddress[11:2]U32					
			This field specifies the offset (into the hardware status page) to which the data will be written. Note that the first few DWords of this status page are reserved for special-purpose data storage - targeting these reserved locations via this command is UNDEFINED. For a QWord write, the offset is valid down to bit 3 only.				
			<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>[16, 1023]</td> <td></td> </tr> </tbody> </table>	Value	Name	[16, 1023]	
	Value	Name					
	[16, 1023]						
1:0	<b>Reserved</b>						
	Project: All Format: MBZ						
2	31:0	<b>Data DWord 0</b>					
		Format: U32 This field specifies the upper DWord value to be written to the targeted QWord location (DW 1).					
3	31:0	<b>Data Word 1</b>					
		Format: U32 This field specifies the upper DWord value to be written to the targeted QWord location (DW 1).					

## MI\_STORE\_DATA\_INDEX

MI_STORE_DATA_INDEX		
Project:	CHV, BSW	
Source:	BlitterCS	
Length Bias:	2	
<p>The MI_STORE_DATA_INDEX command requests a write of the data constant supplied in the packet to the specified offset from the System Address defined by the Hardware Status Page Address Register. As the write targets a System Address, the write operation is coherent with the CPU cache (i.e., the processor cache is snooped).</p>		
Programming Notes		
<p>Use of this command with an invalid or uninitialized value in the Hardware Status Page Address Register is UNDEFINED. This command can be used for general software synchronization through variables in cacheable memory (i.e., where software does not need to poll uncached memory or device registers). This command simply initiates the write operation with command execution proceeding normally. Although the write operation is guaranteed to complete "eventually", there is no mechanism to synchronize command execution with the completion (or even initiation) of these operations.</p>		
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 0h MI_COMMAND
	28:23	<b>MI Command Opcode</b>
		Default Value: 21h MI_STORE_DATA_INDEX
	22	<b>Reserved</b>
	21	<b>Use Per-Process Hardware Status Page</b>
Project: CHV, BSW If this bit is set, this command will index into the per-process hardware status page at offset 0K from the LRCA. If clear, the Global Hardware Status Page will be indexed. This bit must be '0' if the Execlist Enable bit is clear.		
20:8	<b>Reserved</b>	
	Project: All Format: MBZ	
7:0	<b>DWord Length</b>	
	Default Value: 1h Excludes DWord (0,1) = 1 for DWord, 2 for QWord Format: =n Total Length - 2	
1	31:12	<b>Reserved</b>
		Project: All
		Format: MBZ

<b>MI_STORE_DATA_INDEX</b>												
	11:2	<b>Offset</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U10 zero-based DWord offset into the HW status page.</td> </tr> <tr> <td>Format:</td> <td>HardwareStatusPageOffset[11:2]U32</td> </tr> </table> <p>This field specifies the offset (into the hardware status page) to which the data will be written. Note that the first few DWords of this status page are reserved for special-purpose data storage - targeting these reserved locations via this command is UNDEFINED. This address must be 8B aligned for a store "QW" command.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>[16, 1023]</td> <td></td> </tr> </tbody> </table>	Project:	All	Format:	U10 zero-based DWord offset into the HW status page.	Format:	HardwareStatusPageOffset[11:2]U32	Value	Name	[16, 1023]	
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Project:	All											
Format:	MBZ											
2	31:0 <b>Data DWord 0</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>This field specifies the DWord value to be written to the targeted location. For a QWord write this DWord is the lower DWord of the QWord to be reported (DW 0).</p>	Project:	All	Format:	U32							
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3	31:0 <b>Data DWord 1</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>This field specifies the upper DWord value to be written to the targeted QWord location (DW 1).</p>	Project:	All	Format:	U32							
Project:	All											
Format:	U32											

## MI\_STORE\_DATA\_INDEX

<b>MI_STORE_DATA_INDEX</b>			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
<p>The MI_STORE_DATA_INDEX command requests a write of the data constant supplied in the packet to the specified offset from the System Address defined by the Hardware Status Page Address Register. As the write targets a System Address, the write operation is coherent with the CPU cache (i.e., the processor cache is snooped).</p>			
<b>Programming Notes</b>			
<ul style="list-style-type: none"> <li>Use of this command with an invalid or uninitialized value in the Hardware Status Page Address Register is UNDEFINED.</li> <li>This command can be used for general software synchronization through variables in cacheable memory (i.e., where software does not need to poll uncached memory or device registers).</li> <li>This command simply initiates the write operation with command execution proceeding normally. Although the write operation is guaranteed to complete eventually, there is no mechanism to synchronize command execution with the completion (or even initiation) of these operations.</li> </ul>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	21h MI_STORE_DATA_INDEX
		Format:	OpCode
	22	<b>Reserved</b>	
		Project:	CHV, BSW
	21	<b>Use Per-Process Hardware Status Page</b>	
		Project:	CHV, BSW
	If this bit is set, this command will index into the per-process hardware status page at offset 0K from the LRCA. If clear, the Global Hardware Status Page will be indexed. This bit must be 0 if the Execlist Enable bit is clear.		
20:8	<b>Reserved</b>		
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	1h	
	Format:	=n Total Length - 2. Excludes DWord (0,1) = 1 for DWord, 2 for QWord.	



<b>MI_STORE_DATA_INDEX</b>										
1	31:12	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ						
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Format:	MBZ									
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3	31:0	<b>Data DWord 1</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>U32</td> </tr> </table> <p>This field specifies the upper DWord value to be written to the targeted QWord location (DW 1).</p>	Format:	U32						
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## MI\_STORE\_DATA\_INDEX

MI_STORE_DATA_INDEX			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	2		
<p>The MI_STORE_DATA_INDEX command requests a write of the data constant supplied in the packet to the specified offset from the System Address defined by the Hardware Status Page Address Register. As the write targets a System Address, the write operation is coherent with the CPU cache (i.e., the processor cache is snooped).</p>			
<b>Programming Notes</b>			
<ul style="list-style-type: none"> <li>Use of this command with an invalid or uninitialized value in the Hardware Status Page Address Register is UNDEFINED.</li> <li>This command can be used for general software synchronization through variables in cacheable memory (i.e., where software does not need to poll uncached memory or device registers).</li> <li>This command simply initiates the write operation with command execution proceeding normally. Although the write operation is guaranteed to complete "eventually", there is no mechanism to synchronize command execution with the completion (or even initiation) of these operations.</li> </ul>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	21h MI_STORE_DATA_INDEX
		Format:	OpCode
	22	<b>Reserved</b>	
		Format:	MBZ
	21	<b>Use Per-Process Hardware Status Page</b>	
		Project:	CHV, BSW
			If this bit is set, this command will index into the per-process hardware status page at offset 0K from the LRCA. If clear, the Global Hardware Status Page will be indexed. This bit must be '0' if the Execlist Enable bit is clear.
	20:8	<b>Reserved</b>	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	0h Excludes DWord (0,1) = 2 for QWord	
	Format:	=n Total Length - 2	

<b>MI_STORE_DATA_INDEX</b>										
1	31:12	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ						
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	11:2	<p><b>Offset</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 20%;">Format:</td> <td>U10 zero-based DWord offset into the HW status page</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[11:2]U32</td> </tr> </table> <p>This field specifies the offset (into the hardware status page) to which the data will be written. For a QWord write, the offset is valid down to bit 3 only.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 60%;">Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>[16, 1023]</td> <td></td> </tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>The first few DWords of this status page are reserved for special-purpose data storage - targeting these reserved locations via this command is UNDEFINED.</p>	Format:	U10 zero-based DWord offset into the HW status page	Format:	GraphicsAddress[11:2]U32	Value	Name	[16, 1023]	
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## MI\_STORE\_REGISTER\_MEM

<b>MI_STORE_REGISTER_MEM</b>	
Project:	CHV, BSW
Source:	CommandStreamer
Length Bias:	2

The MI\_STORE\_REGISTER\_MEM command requests a register read from a specified memory mapped register location in the device and store of that DWord to memory. The register address is specified along with the command to perform the read.

Programming Notes	Source
<ul style="list-style-type: none"> <li>The command temporarily halts command execution.</li> <li>The memory address for the write is snooped on the host bus.</li> <li>This command should not be used from within a "non-privilege" batch buffer to access global virtual space. doing so will be treated as privilege access violation. Refer "User Mode Privilege Command" in MI_BATCH_BUFFER_START command section to know HW behavior on encountering privilege access violation. This command can be used within ring buffers and/or "privilege" batch buffers to access global virtual space.</li> <li>This command will cause undefined data to be written to memory if given register addresses for the PGTBL_CTL_0 or FENCE registers.</li> </ul>	
Source: BlitterCS, VideoCS, VideoEnhancementCS The source MMIO offset must be limited to any MMIO that is not replicated due to multiple slice configurations. If slice zero is disabled, then any MMIO read from this command streamer to a register replicated in the slice will cause a return value of zero.	BlitterCS, VideoCS, VideoEnhancementCS

DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	24h MI_STORE_REGISTER_MEM
		Format:	OpCode
	22	<b>Use Global GTT</b>	
		Format:	Boolean
	It is allowed for this bit to be set when executing this command from a privileged (secure) batch or ring buffer. This bit must be clear when programmed from within a non-privileged batch buffer. This bit must be 1 if the Per Process GTT Enable bit is clear. This command will use the global GTT to translate the Address and this command must be executing from a privileged (secure) batch buffer.		

<b>MI_STORE_REGISTER_MEM</b>									
	21	<b>Reserved</b>							
	21	<b>Predicate Enable</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Source:</td> <td>RenderCS</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>If set, this command is executed (or not) depending on the current value of the MI Predicate internal state bit. This command is ignored only if PredicateEnable is set and the Predicate state bit is 0.</p>	Project:	CHV, BSW	Source:	RenderCS	Format:	U1	
	Project:	CHV, BSW							
	Source:	RenderCS							
Format:	U1								
20:8	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ						
Format:	MBZ								
7:0	<b>DWord Length</b> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>=n Total Length - 2</td> </tr> </table> <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Project</th> </tr> </thead> <tbody> <tr> <td>2h</td> <td>Excludes DWord (0,1) <b>[Default]</b></td> <td>CHV, BSW</td> </tr> </tbody> </table>	Format:	=n Total Length - 2	Value	Name	Project	2h	Excludes DWord (0,1) <b>[Default]</b>	CHV, BSW
Format:	=n Total Length - 2								
Value	Name	Project							
2h	Excludes DWord (0,1) <b>[Default]</b>	CHV, BSW							
1	31:23	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ					
	Format:	MBZ							
	22:2	<b>Register Address</b> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>MMIOAddress[22:2]MMIO_Register</td> </tr> </table> <p>This field specifies Bits 22:2 of the Register offset the DWord will be read from. As the register address must be DWord-aligned, Bits 1:0 of that address MBZ.</p> <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th style="text-align: center;">Programming Notes</th> </tr> </thead> <tbody> <tr> <td> <ul style="list-style-type: none"> <li>Storing a VGA register is not permitted and will store an UNDEFINED value.</li> <li>The values of PGTBL_CTL0 or any of the FENCE registers cannot be stored to memory; UNDEFINED values will be written to memory if the addresses of these registers are specified.</li> </ul> </td> </tr> </tbody> </table>	Format:	MMIOAddress[22:2]MMIO_Register	Programming Notes	<ul style="list-style-type: none"> <li>Storing a VGA register is not permitted and will store an UNDEFINED value.</li> <li>The values of PGTBL_CTL0 or any of the FENCE registers cannot be stored to memory; UNDEFINED values will be written to memory if the addresses of these registers are specified.</li> </ul>			
Format:	MMIOAddress[22:2]MMIO_Register								
Programming Notes									
<ul style="list-style-type: none"> <li>Storing a VGA register is not permitted and will store an UNDEFINED value.</li> <li>The values of PGTBL_CTL0 or any of the FENCE registers cannot be stored to memory; UNDEFINED values will be written to memory if the addresses of these registers are specified.</li> </ul>									
1:0	<b>Reserved</b>								
2..3 <b>Project:</b> CHV, BSW	63:2	<b>Memory Address</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[63:2]MMIO</td> </tr> </table> <p>This field specifies the address of the memory location where the register value specified in the DWord above will be written. The address specifies the DWord location of the data. Range = GraphicsVirtualAddress[63:2] for a DWord register GraphicsAddress [63:48] are ignored by the HW and assumed to be in correct canonical form [63:48] == [47].</p>	Project:	CHV, BSW	Format:	GraphicsAddress[63:2]MMIO			
	Project:	CHV, BSW							
Format:	GraphicsAddress[63:2]MMIO								
1:0	<b>Reserved</b>								

## MI\_STORE\_URB\_MEM

MI_STORE_URB_MEM						
Project:	CHV, BSW					
Source:	RenderCS					
Length Bias:	2					
<p>The MI_STORE_URB_MEM command requests a URB read from a specified memory mapped URB location in the device and store of that DWord to memory. The URB address is specified along with the command to perform the read.</p>						
Programming Notes						
<ul style="list-style-type: none"> <li>The command temporarily halts command execution.</li> <li>This command should not be used within a "non-secure" batch buffer to access global virtual space. Doing so will cause the command parser to perform the write with byte enables turned off. This command can be used within ring buffers and/or "secure" batch buffers.</li> </ul>						
DWord	Bit	Description				
0	31:29	<b>Command Type</b>				
		Default Value:	0h MI_COMMAND			
		Format:	OpCode			
	28:23	<b>MI Command Opcode</b>				
		Default Value:	2Dh MI_STORE_URB_MEM			
		Format:	OpCode			
	22:8	<b>Reserved</b>				
		Format:	MBZ			
	7:0	<b>DWord Length</b>				
		Format:	=n			
Total Length - 2. Excludes DWord (0,1).						
<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>2h</td> <td>[Default]</td> <td>CHV, BSW</td> </tr> </tbody> </table>		Value	Name	Project	2h	[Default]
Value	Name	Project				
2h	[Default]	CHV, BSW				
1	31:15	<b>Reserved</b>				
		Format:	MBZ			
	14:2	<b>URB Address</b>				
		This field specifies Bits 14:2 of the URB offset the DWord will be read in the URB. This command only supports reading from the lower 32KB of the URB space.				
	1:0	<b>Reserved</b>				
Format:	MBZ					

<b>MI_STORE_URB_MEM</b>					
2..3 <b>Project:</b> CHV, BSW	63:6	<b>Memory Address</b>			
		<table border="1" style="width: 100%;"> <tr> <td style="width: 40%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[63:6]</td> </tr> </table> <p>This field specifies the address of the location of where the value will be written to memory. The value must be in the first DW location of the cache line. GraphicsAddress [63:48] are ignored by the HW and assumed to be in correct canonical form [63:48] == [47].</p>	Project:	CHV, BSW	Format:
	Project:	CHV, BSW			
	Format:	GraphicsAddress[63:6]			
5:0	<b>Reserved</b>				
	<table border="1" style="width: 100%;"> <tr> <td style="width: 40%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ
Project:	CHV, BSW				
Format:	MBZ				

## MI\_SUSPEND\_FLUSH

MI_SUSPEND_FLUSH			
Project:	CHV, BSW		
Source:	VideoEnhancementCS		
Length Bias:	1		
Description		Project	
Blocks PM Flush Requests.		CHV, BSW	
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value: 0h MI_COMMAND	
	28:23	<b>MI Command Opcode</b>	
		Default Value: 0Bh MI_SUSPEND_FLUSH	
	22:1	<b>Reserved</b>	
		Project: All	
		Format: MBZ	
	0	<b>Suspend Flush</b>	Project: All
			Format: Enable
		Description	
This field suspends flush due to a PM flush request.		CHV, BSW	



## MI\_SUSPEND\_FLUSH

MI_SUSPEND_FLUSH				
Project:	CHV, BSW			
Source:	BlitterCS			
Length Bias:	1			
Description		Project		
Blocks PM Flush Requests.		CHV, BSW		
DWord	Bit	Description		
0	31:29	<b>Command Type</b>		
		Default Value: 0h MI_COMMAND		
	28:23	<b>MI Command Opcode</b>		
		Default Value: 0Bh MI_SUSPEND_FLUSH		
	22:1	<b>Reserved</b>		
		Project: All		
		Format: MBZ		
	0	<b>Suspend Flush</b>	Project: All	
			Format: Enable	
		Description		Project
		This field suspends flush due to a PM flush request.		CHV, BSW

## MI\_SUSPEND\_FLUSH

MI_SUSPEND_FLUSH			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	1		
Description		Project	
Blocks PM Flush Requests.		CHV, BSW	
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	0Bh MI_SUSPEND_FLUSH
		Format:	OpCode
	22:1	<b>Reserved</b>	
		Format:	MBZ
	0	<b>Suspend Flush</b>	
		Format:	Enable
		Description	Project
	This field suspends flush due to a PM flush request.		CHV, BSW

## MI\_SUSPEND\_FLUSH

MI_SUSPEND_FLUSH		
Project:	CHV, BSW	
Source:	VideoCS	
Length Bias:	1	
Description		Project
Blocks PM Flush Requests.		CHV, BSW
DWord	Bit	Description
0	31:29	<b>Command Type</b> Default Value: 0h MI_COMMAND
	28:23	<b>MI Command Opcode</b> Default Value: 0Bh MI_SUSPEND_FLUSH
	22:1	<b>Reserved</b> Format: MBZ
	0	<b>Suspend Flush</b> Format: Enable
Description		Project
This field suspends flush due to a PM flush request.		CHV, BSW

## MI\_TOPOLOGY\_FILTER

MI_TOPOLOGY_FILTER			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	1		
<p>This command is used to specify a specific 3DPrimType value, where the CS will ignore all 3DPRIMITIVE commands that do not have a matching 3DPrimType. This primitive culling is optional (turned off by using this command with a Topology Filter Value of 0). <b>This command is specific to the Render command stream only.</b></p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	0Dh MI_TOPOLOGY_FILTER
		Format:	OpCode
	22:6	<b>Reserved</b>	
		Format:	MBZ
	5:0	<b>Topology Filter Value</b>	
		Format:	3D_Prim_Topo_Type [CHV, BSW]
	<p>When non-zero, the CS will discard all 3DPRIMITIVE commands which do not match the specified 3DPrimTopologyType. When zero, no filtering is performed (normal operation).</p>		

## MI\_UPDATE\_GTT

<b>MI_UPDATE_GTT</b>		
Project:	CHV, BSW	
Source:	BlitterCS	
Length Bias:	2	
<p>The MI_UPDATE_GTT command is used to update GGTT page table entries in a coherent manner and at a predictable place in the command flow.</p> <p>A MI_FLUSH_DWORD flush command with "CS Stall" bit set must be programmed prior to MI_UPDATE_GTT command, since work associated with preceding commands that are still in the pipeline may be referencing GTT entries that will be changed by its execution. The flush must also invalidate TLBs and read caches that may become invalid as a result of the changed GTT entries. A MI_FLUSH_DWORD flush command with "CS Stall" bit set must be programmed post MI_UPDATE_GTT command to ensure the GGTT is updated with modified page table entries before the following workload references the modified entries.</p> <p>MI_FLUSH_DWORD flush is not required if it can be guaranteed that the pipeline is free of any work that relies on changing GTT entries (such as MI_UPDATE_GTT contained in a paging DMA buffer that is doing only update/mapping activities and no rendering).</p> <p>MI_UPDATE_GTT command is privilege operation and will be converted to a no-op and an error flagged if it is executed from within a non-secure batch buffer.</p> <p>PPGTT updates cannot be done via <b>MI_UPDATE_GTT</b>, gfx driver will have to use MI_STORE_DATA_IMM for PPGTT inline updates.</p>		
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 0h MI_COMMAND
		Format: OpCode
	28:23	<b>MI Command Opcode</b>
Default Value: 23h MI_UPDATE_GTT		
Format: OpCode		
22:10	<b>Reserved</b>	
9:0	9:0	<b>DWord Length</b>
		Default Value: 0h Excludes DWord (0,1)
		Format: =n
	Total Length - 2	
1	31:12	<b>Entry Address</b>
		Format: GraphicsAddress[31:12] This field holds the QW offset of the first table entry to be modified in GGTT.
11:0	<b>Reserved</b>	
2..n	31:0	<b>Entry Data</b>
		Format: PageTableEntry This Dword becomes the lower dword new page table entry. See PPGTT/Global GTT Table Entries (PTEs) in Memory Interface Registers.

## MI\_UPDATE\_GTT

<b>MI_UPDATE_GTT</b>			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
<p>The MI_UPDATE_GTT command is used to update GTT page table entries in a coherent manner and at a predictable place in the command flow.</p> <p>A PIPE_CONTROL flush command with "CS Stall" bit set must be programmed prior to MI_UPDATE_GTT command, since work associated with preceding commands that are still in the pipeline may be referencing GTT entries that will be changed by its execution. The flush must also invalidate TLBs and read caches that may become invalid as a result of the changed GTT entries. A PIPE_CONTROL flush command with "CS Stall" bit set must be programmed post MI_UPDATE_GTT command to ensure the GGTT is updated with modified page table entries before the following workload references the modified entries.</p> <p>PIPE_CONTROL flush is not required if it can be guaranteed that the pipeline is free of any work that relies on changing GTT entries (such as MI_UPDATE_GTT contained in a paging DMA buffer that is doing only update/mapping activities and no rendering).</p> <p>MI_UPDATE_GTT command is privilege operation and will be converted to a no-op and an error flagged if it is executed from within a non-secure batch buffer.</p> <p>PPGTT updates cannot be done via <b>MI_UPDATE_GTT</b>, gfx driver will have to use MI_STORE_DATA_IMM for PPGTT inline updates.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	23h MI_UPDATE_GTT
		Format:	OpCode
	22:10	<b>Reserved</b>	
	9:0	<b>DWord Length</b>	
		Default Value:	0h
		Format:	=n Total Length - 2. Excludes DWord (0,1).
<b>Programming Notes</b>			
The value of this field must not exceed a value 3Fh when programmed in a batch buffer with resource streamer enabled.			
1	31:12	<b>Entry Address</b>	
		Format:	GraphicsAddress[31:12]
		This field holds the QW offset of the first table entry to be modified in GGTT.	

<b>MI_UPDATE_GTT</b>		
	11:0	<b>Reserved</b>
2..n	63:0	<b>Entry Data</b>
		<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>PageTableEntry</td> </tr> </table> <p>This Dword becomes the new page table entry. See PPGTT/Global GTT Table Entries (PTEs) in Memory Interface Registers.</p>
Format:	PageTableEntry	

## MI\_UPDATE\_GTT

<b>MI_UPDATE_GTT</b>		
Project:	CHV, BSW	
Source:	VideoCS	
Length Bias:	2	
<p>The MI_UPDATE_GTT command is used to update GGTT page table entries in a coherent manner and at a predictable place in the command flow.</p> <p>A MI_FLUSH_DWORD flush command with "CS Stall" bit set must be programmed prior to MI_UPDATE_GTT command, since work associated with preceding commands that are still in the pipeline may be referencing GTT entries that will be changed by its execution. The flush must also invalidate TLBs and read caches that may become invalid as a result of the changed GTT entries. A MI_FLUSH_DWORD flush command with "CS Stall" bit set must be programmed post MI_UPDATE_GTT command to ensure the GGTT is updated with modified page table entries before the following workload references the modified entries.</p> <p>MI_FLUSH_DWORD flush is not required if it can be guaranteed that the pipeline is free of any work that relies on changing GTT entries (such as MI_UPDATE_GTT contained in a paging DMA buffer that is doing only update/mapping activities and no rendering).</p> <p>MI_UPDATE_GTT command is privilege operation and will be converted to a no-op and an error flagged if it is executed from within a non-secure batch buffer.</p> <p>PPGTT updates cannot be done via <b>MI_UPDATE_GTT</b>, gfx driver will have to use MI_STORE_DATA_IMM for PPGTT inline updates.</p>		
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 0h MI_COMMAND
		Format: OpCode
	28:23	<b>MI Command Opcode</b>
Default Value: 23h MI_UPDATE_GTT		
22:10	<b>Reserved</b>	
	9:0	<b>DWord Length</b>
		Default Value: 0h Excludes DWord (0,1)
		Format: =n
Total Length - 2		
1	31:12	<b>Entry Address</b>
		Format: GraphicsAddress[31:12]
This field holds the QW offset of the first table entry to be modified in GGTT.		
<b>Reserved</b>		
2..n	63:0	<b>Entry Data</b>
		Format: PageTableEntry
This Dword becomes the lower dword new page table entry. See PPGTT/Global GTT Table Entries (PTEs) in Memory Interface Registers.		



## MI\_UPDATE\_GTT

<b>MI_UPDATE_GTT</b>			
Project:	CHV, BSW		
Source:	VideoEnhancementCS		
Length Bias:	2		
<p>The MI_UPDATE_GTT command is used to update GGTT page table entries in a coherent manner and at a predictable place in the command flow.</p> <p>A MI_FLUSH_DWORD flush command with "CS Stall" bit set must be programmed prior to MI_UPDATE_GTT command, since work associated with preceding commands that are still in the pipeline may be referencing GTT entries that will be changed by its execution. The flush must also invalidate TLBs and read caches that may become invalid as a result of the changed GTT entries. A MI_FLUSH_DWORD flush command with "CS Stall" bit set must be programmed post MI_UPDATE_GTT command to ensure the GGTT is updated with modified page table entries before the following workload references the modified entries.</p> <p>MI_FLUSH_DWORD flush is not required if it can be guaranteed that the pipeline is free of any work that relies on changing GTT entries (such as MI_UPDATE_GTT contained in a paging DMA buffer that is doing only update/mapping activities and no rendering).</p> <p>MI_UPDATE_GTT command is privilege operation and will be converted to a no-op and an error flagged if it is executed from within a non-secure batch buffer.</p> <p>PPGTT updates cannot be done via <b>MI_UPDATE_GTT</b>, gfx driver will have to use MI_STORE_DATA_IMM for PPGTT inline updates.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
Default Value:		23h MI_UPDATE_GTT	
22:10	9:0	<b>Reserved</b>	
		<b>DWord Length</b>	
		Default Value:	0h Excludes DWord (0,1)
1	31:12	Format:	GraphicsAddress[31:12]
		This field holds the QW offset of the first table entry to be modified in GGTT.	
2..n	63:0	<b>Reserved</b>	
		<b>Entry Data</b>	
		Format:	PageTableEntry
This Dword becomes the lower dword new page table entry. See PPGTT/Global GTT Table Entries (PTEs) in Memory Interface Registers.			

## MI\_URB\_ATOMIC\_ALLOC

MI_URB_ATOMIC_ALLOC						
Project:	CHV, BSW					
Source:	RenderCS					
Length Bias:	1					
This command is used to specify the region in URB allocated for URB atomic value storage. <b>This command is specific to the Render command stream only.</b>						
Programming Notes						
This command can only be sent after a flush has occurred.						
DWord	Bit	Description				
0	31:29	<b>Command Type</b>				
		Default Value:	0h MI_COMMAND			
		Format:	OpCode			
	28:23	<b>MI Command Opcode</b>				
		Default Value:	09h MI_URB_ALLOC			
		Format:	OpCode			
	22:20	<b>Reserved</b>				
		Format:	MBZ			
	19:12	<b>URB Atomic Storage Offset</b>				
		Format:	U8 Number of 128B Entries			
This field specifies the offset of a 128B granular starting address in the URB. The value of <b>URB Atomic Storage Offset</b> plus the value of the <b>URB Atomic Storage Size</b> must not exceed 256.						
<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[0,255]</td> <td></td> <td>0-(32KB-128B)</td> </tr> </tbody> </table>		Value	Name	Description	[0,255]	
Value	Name	Description				
[0,255]		0-(32KB-128B)				
11:9	<b>Reserved</b>					
	Format:	MBZ				
8:0	<b>URB Atomic Storage Size</b>					
	Format:	U9 Number of 128B Entries				
	This field specifies the size of the buffer in the URB in number of 128B entries. If this field has a value of zero then the URB Atomic allocation is disabled and will not be context save/restored.					
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[0,256]</td> <td></td> <td>0-32KB</td> </tr> </tbody> </table>	Value	Name	Description	[0,256]	
Value	Name	Description				
[0,256]		0-32KB				

## MI\_URB\_CLEAR

<b>MI_URB_CLEAR</b>					
Project:	CHV, BSW				
Source:	RenderCS				
Length Bias:	2				
The MI_URB_CLEAR command allows SW to clear (write zero) to a section in the URB.					
Programming Notes					
<ul style="list-style-type: none"> <li>The command temporarily halts command execution.</li> <li>This command is part of context save/restore. Only the last instance will be part of context.</li> <li>This command requires the 3D pipeline to be flushed before execution.</li> </ul>					
DWord	Bit	Description			
0	31:29	<b>Command Type</b>			
		Default Value: 0h MI_COMMAND Format: OpCode			
	28:23	<b>MI Command Opcode</b>			
		Default Value: 19h MI_URB_CLEAR Format: OpCode			
22:8	<b>Reserved</b>				
Format: MBZ					
7:0	<b>DWord Length</b>				
	Default Value:	0h			
	Format:	=n Total Length - 2. Excludes DWord (0,1).			
1	31:30	<b>Reserved</b>			
	29:16	<b>URB Clear Length</b>			
		Project: CHV, BSW			
		This field specifies the number of 256b entries in the URB to be cleared to zero.			
<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>[0,16383]</td> <td></td> </tr> </tbody> </table>		Value	Name	[0,16383]	
Value	Name				
[0,16383]					
15	<b>Reserved</b>				
14:0	<b>URB Address</b>				
	Project:	CHV, BSW			
	Format:	URBAddress[19:5] 256b aligned			
This field specifies Bits 19:5 of the URB Address					

## MI\_USER\_INTERRUPT

MI_USER_INTERRUPT			
Project:	CHV, BSW		
Source:	VideoEnhancementCS		
Length Bias:	1		
<p>The MI_USER_INTERRUPT command is used to generate a User Interrupt condition. The parser will continue parsing after processing this command. See User Interrupt.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	02h MI_USER_INTERRUPT
		Format:	OpCode
	22:0	<b>Reserved</b>	
		Project:	All
		Format:	MBZ

## MI\_USER\_INTERRUPT

MI_USER_INTERRUPT		
Project:	CHV, BSW	
Source:	BlitterCS	
Length Bias:	1	
<p>The MI_USER_INTERRUPT command is used to generate a User Interrupt condition. The parser will continue parsing after processing this command. See User Interrupt.</p>		
DWord	Bit	Description
0	31:29	<b>Command Type</b>
		Default Value: 0h MI_COMMAND
	28:23	<b>MI Command Opcode</b>
		Default Value: 02h MI_USER_INTERRUPT
	22:0	<b>Reserved</b>
		Project:
Format:		MBZ

## MI\_USER\_INTERRUPT

MI_USER_INTERRUPT			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	1		
<p>The MI_USER_INTERRUPT command is used to generate a User Interrupt condition. The parser will continue parsing after processing this command. See User Interrupt.</p>			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	02h MI_USER_INTERRUPT
		Format:	OpCode
	22:0	<b>Reserved</b>	
		Format:	MBZ

## MI\_USER\_INTERRUPT

MI_USER_INTERRUPT			
Project:	CHV, BSW		
Source:	VideoCS		
Length Bias:	1		
The MI_USER_INTERRUPT command is used to generate a User Interrupt condition. The parser will continue parsing after processing this command. See User Interrupt.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	02h MI_USER_INTERRUPT
		Format:	OpCode
	22:0	<b>Reserved</b>	
		Format:	MBZ

## MI\_WAIT\_FOR\_EVENT

<b>MI_WAIT_FOR_EVENT</b>	
Project:	CHV, BSW
Source:	BlitterCS
Length Bias:	1

The MI\_WAIT\_FOR\_EVENT command is used to pause command stream processing until a specific event occurs or while a specific condition exists. Only one event/condition can be specified -- specifying multiple events is UNDEFINED. The effect of the wait operation depends on the source of the command. If executed from a batch buffer, the parser will halt (and suspend command arbitration) until the event/condition occurs. If executed from a ring buffer, further processing of that ring will be suspended, although command arbitration (from other rings) will continue. Note that if a specified condition does not exist (the condition code is inactive) at the time the parser executes this command, the parser proceeds, treating this command as a no-operation. If execution of this command from a primary ring buffer causes a wait to occur, the active ring buffer will effectively give up the remainder of its time slice (required in order to enable arbitration from other primary ring buffers).

### Programming Notes

[Ring Buffer Mode Of scheduling Only][Blitter CS]: HW loses Page Directory (PPGTT) information on becoming IDLE. SW must always program the PD information following MI\_WAIT\_FOR\_EVENT command. This will ensure Page Directory information gets reprogrammed on exiting IDLE flow triggered on MI\_WAIT\_FOR\_EVENT. Alternatively SW can disable IDLE flows on MI\_WAIT\_FOR\_EVENT by setting below bits in "BCS\_ECOSKPD" register. Disable GT C6 Enter Due to Blitter Waiting on Vblank Disable GT C6 Enter Due to Blitter Waiting on Scanline Disable GT C6 Enter Due to Blitter Waiting on Flip Done

DWor d	Bit	Description			
0	31:2 9	<b>Command Type</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Default Value:</td> <td style="width: 50%;">0h MI_COMMAND</td> </tr> </table>	Default Value:	0h MI_COMMAND	
	Default Value:	0h MI_COMMAND			
	28:2 3	<b>MI Command Opcode</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Default Value:</td> <td style="width: 50%;">03h MI_WAIT_FOR_EVENT</td> </tr> </table>	Default Value:	03h MI_WAIT_FOR_EVENT	
	Default Value:	03h MI_WAIT_FOR_EVENT			
22	<b>Reserved</b>				
21	<b>Display Pipe C Vertical Blank Wait Enable</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td style="width: 50%;">CHV, BSW</td> </tr> <tr> <td style="width: 50%;">Format:</td> <td style="width: 50%;">Enable</td> </tr> </table> <p>This field enables a wait until the next Display Pipe C "Vertical Blank" event occurs. This event is described as the start of the next Display C vertical blank period. Note that this can cause a wait for up to an entire refresh period. See Vertical Blank Event in the Device Programming Interface chapter of MI Functions.</p>	Project:	CHV, BSW	Format:	Enable
Project:	CHV, BSW				
Format:	Enable				
<h3 style="margin: 0;">Programming Notes</h3> <p>If this bit is set, then RC6 cannot occur while waiting for this event to complete. SW must disable IDLE sequence or RC6 prior to the command. IDLE sequence and RC6 must be reenabled after the command to allow the hardware to enter RC6.</p>					



## MI\_WAIT\_FOR\_EVENT

20	<b>Display Sprite C Flip Pending Wait Enable</b>	
	Project:	All
	Format:	Enable
	<p>This field enables a wait for the duration of a Display Sprite C "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers).</p>	
	<p><b>Programming Notes</b></p> <p>If this bit is set, then RC6 cannot occur while waiting for this event to complete. SW must disable IDLE sequence or RC6 prior to the command. IDLE sequence and RC6 must be reenabled after the command to allow the hardware to enter RC6.</p>	
19	<b>Display Sprite C3 Flip Pending Wait Enable</b>	
	Project:	CHV, BSW
	Format:	Enable
<p>This field enables a wait for the duration of a Display Sprite C3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers).</p>		
18	<b>Display Sprite B3 Flip Pending Wait Enable</b>	
	Project:	CHV, BSW
	Format:	Enable
<p>This field enables a wait for the duration of a Display Sprite B3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers).</p>		
17	<b>Display Sprite A3 Flip Pending Wait Enable</b>	
	Project:	CHV, BSW
	Format:	Enable
<p>This field enables a wait for the duration of a Display Sprite A3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers).</p>		
16	<b>Display Sprite C2 Flip Pending Wait Enable</b>	
	Project:	CHV, BSW
	Format:	Enable
<p>This field enables a wait for the duration of a Display Sprite C2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers).</p>		
15	<b>Display Plane C Flip Pending Wait Enable</b>	
	Project:	All
	Format:	Enable

<b>MI_WAIT_FOR_EVENT</b>									
	<p>This field enables a wait for the duration of a Display Plane C "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers).</p> <table border="1" style="width: 100%; text-align: center;"> <tr> <td colspan="2"><b>Programming Notes</b></td> </tr> <tr> <td colspan="2">If this bit is set, then RC6 cannot occur while waiting for this event to complete. SW must disable IDLE sequence or RC6 prior to the command. IDLE sequence and RC6 must be reenabled after the command to allow the hardware to enter RC6.</td> </tr> </table>	<b>Programming Notes</b>		If this bit is set, then RC6 cannot occur while waiting for this event to complete. SW must disable IDLE sequence or RC6 prior to the command. IDLE sequence and RC6 must be reenabled after the command to allow the hardware to enter RC6.					
<b>Programming Notes</b>									
If this bit is set, then RC6 cannot occur while waiting for this event to complete. SW must disable IDLE sequence or RC6 prior to the command. IDLE sequence and RC6 must be reenabled after the command to allow the hardware to enter RC6.									
14	<p><b>Display Pipe C Scan Line Wait Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait while a Display Pipe C "Scan Line" condition exists. This condition is defined as the the start of the scan line specified in the Pipe C Display Scan Line Count Range Compare Register.</p> <table border="1" style="width: 100%; text-align: center;"> <tr> <td colspan="2"><b>Programming Notes</b></td> </tr> <tr> <td colspan="2">If this bit is set, then RC6 cannot occur while waiting for this event to complete. SW must disable IDLE sequence or RC6 prior to the command. IDLE sequence and RC6 must be reenabled after the command to allow the hardware to enter RC6.</td> </tr> </table>	Project:	CHV, BSW	Format:	Enable	<b>Programming Notes</b>		If this bit is set, then RC6 cannot occur while waiting for this event to complete. SW must disable IDLE sequence or RC6 prior to the command. IDLE sequence and RC6 must be reenabled after the command to allow the hardware to enter RC6.	
Project:	CHV, BSW								
Format:	Enable								
<b>Programming Notes</b>									
If this bit is set, then RC6 cannot occur while waiting for this event to complete. SW must disable IDLE sequence or RC6 prior to the command. IDLE sequence and RC6 must be reenabled after the command to allow the hardware to enter RC6.									
13:1 2	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ				
Project:	All								
Format:	MBZ								
11	<p><b>Display Pipe B Vertical Blank Wait Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait until the next Display Pipe B "Vertical Blank" event occurs. This event is described as the start of the next Display Pipe B vertical blank period. Note that this can cause a wait for up to an entire refresh period.</p>	Project:	CHV, BSW	Format:	Enable				
Project:	CHV, BSW								
Format:	Enable								
10	<p><b>Display Sprite B Flip Pending Wait Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Sprite B "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers).</p>	Project:	All	Format:	Enable				
Project:	All								
Format:	Enable								
9	<p><b>Display Plane B Flip Pending Wait Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane B "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers).</p>	Project:	All	Format:	Enable				
Project:	All								
Format:	Enable								

## MI\_WAIT\_FOR\_EVENT

8	<b>Display Pipe B Scan Line Wait Enable</b>	
	Project:	CHV, BSW
	Format:	Enable
	<p>This field enables a wait while a Display Pipe B "Scan Line" condition exists. This condition is defined as the the start of the scan line specified in the Pipe B Display Scan Line Count Range Compare Register.</p>	
	<b>Programming Notes</b>	
	<p>If this bit is set, then RC6 cannot occur while waiting for this event to complete. SW must disable IDLE sequence or RC6 prior to the command. IDLE sequence and RC6 must be reenabled after the command to allow the hardware to enter RC6.</p>	
7	<b>Display Sprite B2 Flip Pending Wait Enable</b>	
	Project:	CHV, BSW
	Format:	Enable
	<p>This field enables a wait for the duration of a Display Sprite B2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers).</p>	
6	<b>Display Sprite A2 Flip Pending Wait Enable</b>	
	Project:	CHV, BSW
	Format:	Enable
	<p>This field enables a wait for the duration of a Display Sprite A2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers).</p>	
5:4	<b>Reserved</b>	
	Project:	All
	Format:	MBZ
3	<b>Display Pipe A Vertical Blank Wait Enable</b>	
	Project:	CHV, BSW
	Format:	Enable
	<p>This field enables a wait until the next Display Pipe A "Vertical Blank" event occurs. This event is described as the start of the next Display Pipe A vertical blank period. Note that this can cause a wait for up to an entire refresh period.</p>	
2	<b>Display Sprite A Flip Pending Wait Enable</b>	
	Project:	All
	Format:	Enable
	<p>This field enables a wait for the duration of a Display Sprite A "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers).</p>	

<b>MI_WAIT_FOR_EVENT</b>						
1	<p><b>Display Plane A Flip Pending Wait Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane A "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers).</p>	Project:	All	Format:	Enable	
Project:	All					
Format:	Enable					
0	<p><b>Display Pipe A Scan Line Wait Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait while a Display Pipe A "Scan Line" condition exists. This condition is defined as the the start of the scan line specified in the Pipe A Display Scan Line Count Range Compare Register.</p> <table border="1" style="width: 100%; background-color: #e6f2ff;"> <tr> <td style="text-align: center;"><b>Programming Notes</b></td> </tr> </table> <p>If this bit is set, then RC6 cannot occur while waiting for this event to complete. SW must disable IDLE sequence or RC6 prior to the command. IDLE sequence and RC6 must be reenabled after the command to allow the hardware to enter RC6.</p>	Project:	CHV, BSW	Format:	Enable	<b>Programming Notes</b>
Project:	CHV, BSW					
Format:	Enable					
<b>Programming Notes</b>						

## MI\_WAIT\_FOR\_EVENT

<b>MI_WAIT_FOR_EVENT</b>	
Project:	CHV, BSW
Source:	RenderCS
Length Bias:	1
<b>Description</b>	
<p>The MI_WAIT_FOR_EVENT command is used to pause command stream processing <b>of this pipe only</b> until a specific event occurs or while a specific condition exists. See Wait Events/Conditions, Device Programming Interface in <i>MI Functions</i>. Only one event/condition can be specified. Specifying multiple events is UNDEFINED. Once parsed, the parser will halt (and suspend command arbitration) until the event/condition occurs. Note that if a specified condition does not exist (the condition code is inactive) at the time the parser executes this command, the parser proceeds, treating this command as a no-operation.</p> <p>If CSunit is waiting for V-blank or flip done, HW can go into RC1/RC6 state.</p> <p>MI_NOOP setting NOP register (or any other benign command) must be set after MI_WAIT_FOR_EVENT under the following conditions:</p> <ul style="list-style-type: none"> <li>• Back-to-back MI_WAIT_FOR_EVENT commands</li> <li>• MI_WAIT_FOR_EVENT is the last command before head = tail</li> </ul> <p>Events must be unmasked in the Display Engine Render Response Mask Register (DE RRMR 0x44050) prior to waiting for them with a MI_WAIT_FOR_EVENT command, or in the case of flips or scanlines, prior to starting the flip or loading the scanline. Unmasked events will wake command streamer as they occur, so for improved power savings it is recommended to only unmask events that are required. Programming the DE RRMR register can be done through MMIO or a LOAD_REGISTER_IMMEDIATE command.</p> <p><b>Execution List Mode of Scheduling:</b> CS on evaluating MI_WAIT_FOR_EVENT to be unsuccessful (has to wait for event to happen) triggers synchronous context switch stating the switch reason in Context Status Buffer. Note that synchronous context switch can be inhibited through programming "<b>Inhibit Synchronous Context Switch</b>" bit in CTXT_SR_CTL register or by disabling arbitration through MI_ARB_ON_OFF command.</p>	
<b>Programming Notes</b>	
<p><b>Ring Buffer Mode of Scheduling Only:</b> SW must always program a dummy <b>MI_SEMAPHORE_WAIT</b> command in <b>Signal Mode</b> which is always successful prior to programming MI_WAIT_FOR_EVENT.</p> <p>If the above programming restriction is not followed, in certain order of programming sequences HW would enter IDLE_DOP instead of IDLE_C6 on encountering MI_WAIT_FOR_EVENT unsuccessful.</p> <p><b>Render CS Only:</b> SW must always program PIPE_CONTROL with "CS Stall" and "Render Target Cache Flush Enable" set prior to programming MI_WAIT_FOR_EVENT command for GPGPU workloads i.e when pipeline select is GPGPU via PIPELINE_SELECT command. This is required to achieve better GPGPU preemption latencies for certain programming sequences.</p> <p>If programming PIPE_CONTROL has performance implications then preemption latencies can be trade off against performance by not implementing this programming note.</p> <p><b>Execlist Mode of Scheduling Only:</b> When MI_WAIT_FOR_EVENT command results in context switch on "Wait On V-blank", "Display Plane" field indicates the Display pipe for which the wait for event was un-successful.</p>	

## MI\_WAIT\_FOR\_EVENT

When a context switched out due to "Wait on V-blank" is resubmitted by scheduler without waiting for the corresponding V-blank event to be satisfied, it might happen that the context can get switched out again by HW due to V-blank not satisfied, when this condition occurs due to known HW issue "Display Plane" field is not indicated correctly. To work around this issue SW must do one of the below

1. Always program MI\_WAIT\_FOR\_EVENT for V-blank with Inhibit Synchronous Context Switch Set so that a context never gets switched out with context switch reason as only due to "Wait On V-blank". However a context waiting for V-blank event to be satisfied can get switched out due to preemption on submission of a pending execlist. In this case scheduler can resubmit the switched out context at appropriate time similar to any other preempted context. **OR**
2. When MI\_WAIT\_FOR\_EVENT for V-blank is programmed with Inhibit Synchronous Context Switch Reset. Scheduler on detecting a context switched out due to Wait On V-blank must not resubmit the context unless the corresponding V-blank event is satisfied. **OR**
3. Scheduler must maintain its own record of the Pipe assigned to a given context for Wait on V-blank and must not look at the "Display Plane" field reported in the context switch status.

**Execlist Mode of Scheduling:** CS takes couple of clocks to parse MI\_WAIT\_FOR\_EVENT command and in a specific clock while parsing it makes the decision to do Synchronous Context Switch if the event is unsuccessful. When CS receives Display message satisfying the MI\_WAIT\_FOR\_EVENT on the same clock when it makes decision to do synchronous context switch. Only way this issue can be avoided is by inhibiting synchronous context switch on MI\_WAIT\_FOR\_EVENT command. Synchronous context switch on MI\_WAIT\_FOR\_EVENT can be inhibited by setting "**Inhibit Synchronous Context Switch**" bit in CTXT\_SR\_CTL register through MI\_LOAD\_REGISTER\_IMM command prior to MI\_WAIT\_FOR\_EVENT command and resetting the same after MI\_WAIT\_FOR\_EVENT command.

Ex:

```
MI_LOAD_REGISTER_IMM (CTXT_SR_CTL, Inhibit Synchronous Context Switch set)
MI_WAIT_FOR_EVENT
MI_LOAD_REGISTER_IMM (CTXT_SR_CTL, Inhibit Synchronous Context Switch reset)
```

When the above sequence has to be programmed in a non-privileged batch buffer, SW has to ensure CTXT\_SR\_CTL register is forced to non-privileged register through one of the FORCE\_TO\_NONPRIV registers.

DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	<b>MI Command Opcode</b>	
		Default Value:	03h MI_WAIT_FOR_EVENT
		Format:	OpCode
22	<b>Reserved</b>		

## MI\_WAIT\_FOR\_EVENT

21	<b>Display Pipe C Vertical Blank Wait Enable</b>	
	Project:	CHV, BSW
	Format:	Enable
	<b>Description</b>	
	<p>This field enables a wait until the next Display Pipe C Vertical Blank event occurs. This event is described as the start of the next Display C vertical blank period. Note that this can cause a wait for up to an entire refresh period.</p> <p><b>Render and Blitter Engines</b></p>	
20	<b>Display Sprite C Flip Pending Wait Enable</b>	
	Project:	CHV, BSW
	Format:	Enable
	<b>Description</b>	
<p>This field enables a wait for the duration of a Display Sprite C Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers).</p> <p><b>Render and Blitter Engines</b></p>		
19	<b>Display Sprite C3 Flip Pending Wait Enable</b>	
	Project:	CHV, BSW
	Format:	Enable
	<p>This field enables a wait for the duration of a Display Sprite C3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers).</p>	
18	<b>Display Sprite B3 Flip Pending Wait Enable</b>	
	Project:	CHV, BSW
	Format:	Enable
	<p>This field enables a wait for the duration of a Display Sprite B3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers).</p>	
17	<b>Display Sprite A3 Flip Pending Wait Enable</b>	
	Project:	CHV, BSW
	Format:	Enable
	<p>This field enables a wait for the duration of a Display Sprite A3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers).</p>	

<b>MI_WAIT_FOR_EVENT</b>				
16	<b>Display Sprite C2 Flip Pending Wait Enable</b>			
	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Sprite C2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers).</p>	Project:	CHV, BSW	Format:
Project:	CHV, BSW			
Format:	Enable			
15	<b>Display Plane C Flip Pending Wait Enable</b>			
	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <div style="border: 1px solid black; background-color: #e6f2ff; padding: 5px; text-align: center;"><b>Description</b></div> <p>This field enables a wait for the duration of a Display Plane C "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers).</p> <p><b>Render and Blitter Engines</b></p>	Project:	CHV, BSW	Format:
Project:	CHV, BSW			
Format:	Enable			
14	<b>Display Pipe C Scan Line Wait Enable</b>			
	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <div style="border: 1px solid black; background-color: #e6f2ff; padding: 5px; text-align: center;"><b>Description</b></div> <p>This field enables a wait while a Display Pipe C Scan Line condition exists. This condition is defined as the start of the scan line specified in the Pipe C Display Scan Line Count Range Compare Register.</p> <p><b>Render and Blitter Engines</b></p>	Project:	CHV, BSW	Format:
Project:	CHV, BSW			
Format:	Enable			
13	<b>Reserved</b>			
	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:
Project:	CHV, BSW			
Format:	MBZ			
12	<b>Reserved</b>			
11	<b>Display Pipe B Vertical Blank Wait Enable</b>			
	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>Enable</td> </tr> </table> <div style="border: 1px solid black; background-color: #e6f2ff; padding: 5px; text-align: center;"><b>Description</b></div> <p>This field enables a wait until the next Display Pipe B "Vertical Blank" event occurs. This event is described as the start of the next Display Pipe B vertical blank period. Note that this can cause a wait for up to an entire refresh period.</p> <p><b>Render and Blitter Engines</b></p>	Format:	Enable	
Format:	Enable			



<b>MI_WAIT_FOR_EVENT</b>	
10	<b>Display Sprite B Flip Pending Wait Enable</b>
	Format: <span style="float: right;">Enable</span>
	<b>Description</b>
	This field enables a wait for the duration of a Display Sprite B "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers).
	<b>Render and Blitter Engines</b>
9	<b>Display Plane B Flip Pending Wait Enable</b>
	Format: <span style="float: right;">Enable</span>
	<b>Description</b>
	This field enables a wait for the duration of a Display Plane B Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers).
	<b>Render and Blitter Engines</b>
8	<b>Display Pipe B Scan Line Wait Enable</b>
	Format: <span style="float: right;">Enable</span>
	<b>Description</b>
	This field enables a wait while a Display Pipe B Scan Line condition exists. This condition is defined as the start of the scan line specified in the Pipe B Display Scan Line Count Range Compare Register.
	<b>Render and Blitter Engines</b>
7	<b>Display Sprite B2 Flip Pending Wait Enable</b>
	Project: <span style="float: right;">CHV, BSW</span>
	Format: <span style="float: right;">Enable</span>
	This field enables a wait for the duration of a Display Sprite B2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers).
	<b>Render and Blitter Engines</b>
6	<b>Display Sprite A2 Flip Pending Wait Enable</b>
	Project: <span style="float: right;">CHV, BSW</span>
	Format: <span style="float: right;">Enable</span>
	This field enables a wait for the duration of a Display Sprite A2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers).
	<b>Render and Blitter Engines</b>
5	<b>Reserved</b>
4	<b>Reserved</b>

<b>MI_WAIT_FOR_EVENT</b>	
3	<b>Display Pipe A Vertical Blank Wait Enable</b>
	Format: <span style="float: right;">Enable</span>
	<b>Description</b>
	This field enables a wait until the next Display Pipe A "Vertical Blank" event occurs. This event is described as the start of the next Display Pipe A vertical blank period. Note that this can cause a wait for up to an entire refresh period.
<b>Render and Blitter Engines</b>	
2	<b>Display Sprite A Flip Pending Wait Enable</b>
	Format: <span style="float: right;">Enable</span>
	<b>Description</b>
	This field enables a wait for the duration of a Display Sprite A "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers).
<b>Render and Blitter Engines</b>	
1	<b>Display Plane A Flip Pending Wait Enable</b>
	Format: <span style="float: right;">Enable</span>
	<b>Description</b>
	This field enables a wait for the duration of a Display Plane A "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers).
<b>Render and Blitter Engines</b>	
0	<b>Display Pipe A Scan Line Wait Enable</b>
	Format: <span style="float: right;">Enable</span>
	<b>Description</b>
	This field enables a wait while a Display Pipe A "Scan Line" condition exists. This condition is defined as the start of the scan line specified in the Pipe A Display Scan Line Count Range Compare Register.
<b>Render and Blitter Engines</b>	

## Move

<b>mov - Move</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
<p>The mov instruction moves the components in src0 into the channels of dst. If src0 and dst are of different types, format conversion is performed. If src0 is a scalar immediate, the immediate value is loaded into enabled channels of dst. A mov with the same source and destination type, no source modifier, and no saturation is a raw move. A packed byte destination region (B or UB type with HorzStride == 1 and ExecSize &gt; 1) can only be written using raw move.</p>			
<p>When denorm mode is flush to zero, a raw mov instruction with saturation modifier will not flush the denorm input or output to zero (Denorm is preserved).</p>			
<p>Format: [(pred)] mov[.cmod] (exec_size) dst src0</p>			
<b>Programming Notes</b>			
<p>A <i>mov</i> instruction with a source modifier always copies a denorm source value to a denorm destination value (in the manner of a raw move).</p>			
<p>There is no direct conversion from B/UB to DF or DF to B/UB. Use two instructions and a word or DWord intermediate type.</p>			
<p>There is no direct conversion from B/UB to Q/UQ or Q/UQ to B/UB. Use two instructions and a word or DWord intermediate integer type.</p>			
<p>There is no direct conversion from HF to DF or DF to HF. Use two instructions and F (Float) as an intermediate type.</p>			
<p>There is no direct conversion from HF to Q/UQ or Q/UQ to HF. Use two instructions and F (Float) or a word integer type or a DWord integer type as an intermediate type.</p>			
<b>Restriction</b>			
<p>Raw move is not supported for Float values in ALT mode if any values are infinities or NaNs.</p>			
<p>An accumulator can be a source or destination operand but not both.</p>			
<b>Syntax</b>			
<p>[(pred)] mov[.cmod] (exec_size) reg reg [(pred)] mov[.cmod] (exec_size) reg imm32 [(pred)] mov[.cmod] (exec_size) reg imm64</p>			
<b>Pseudocode</b>			
<p>Evaluate(WrEn); for ( n = 0; n &lt; exec_size; n++ ) { if ( WrEn.chan[n] ) { dst.chan[n] = src0.chan[n]; } }</p>			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	Y	Y	Y

## mov - Move

Src Types	Dst Types	Project
*B,*W,*D	*B,*W,*D	
*B,*W,*D	F	
F	*B,*W,*D	
F	F	
*W,*D	DF	CHV, BSW
F	DF	CHV, BSW
DF	*W,*D	CHV, BSW
DF	F	CHV, BSW
DF	DF	CHV, BSW
*W,*D,*Q	*W,*D,*Q	CHV, BSW
F	*Q	CHV, BSW
DF	*Q	CHV, BSW
*Q	F	CHV, BSW
*Q	DF	CHV, BSW
*B,*W,*D	HF	CHV, BSW
F	HF	CHV, BSW
HF	*B,*W,*D	CHV, BSW
HF	F	CHV, BSW
HF	HF	CHV, BSW

DWord	Bit	Description
0..3	127:64	<b>RegSource</b>
		Exists If: ([Operand Controls][Src0.RegFile]!='IMM')
	Format: EU_INSTRUCTION_SOURCES_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>
Exists If: ([Operand Controls][Src0.RegFile]='IMM')		
Format: EU_INSTRUCTION_SOURCES_IMM32 [CHV, BSW]		
63:32	<b>Operand Controls</b>	
	Format: EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]	
31:0	<b>Header</b>	
	Format: EU_INSTRUCTION_HEADER [CHV, BSW]	

## Move Indexed

<b>movi - Move Indexed</b>	
Project:	CHV, BSW
Source:	Eulsa
Length Bias:	4
<p>The movi instruction performs a fast component-wise indexed move for subfields from src0 to dst. The source operand must be an indirectly-addressed register. All channels of the source operand share the same register number, which is provided by the register field of the first address subregister, with a possible immediate register offset. The register fields of the subsequent address subregisters are ignored by hardware. The subregister number of a source channel is provided by the subregister field of the corresponding address subregister, with a possible immediate subregister offset.</p> <p>The destination register may be either a directly-addressed or an indirectly-addressed register. This instruction effectively performs a subfield shuffling from one register to another. Up to eight subfields can be selected by an instruction.</p>	
Format: [(pred)] movi (exec_size) dst src0 src1	
<b>Programming Notes</b>	
<p><b>HW Implementation Details:</b></p> <p>The source register is calculated by adding the register portion of the first index register with the register portion of the address immediate, <math>a0.0[11:5] + \text{addr\_imm}[9:5]</math></p> <p>For byte movi, byte0 of the destination is selected by <math>(a0.0[4:0])</math>, byte1 is selected by <math>(a0.1[4:0])</math>, ..., and byte7 is selected by <math>(a0.7[4:0])</math>. The rest of the bytes are undefined.</p> <p>For word movi, byte0 of the destination is selected by <math>(a0.0[4:1] \&amp; 0)</math>, byte1 is selected by <math>(a0.0[4:1] \&amp; 1)</math>, byte2 is selected by <math>(a0.1[4:1] \&amp; 0)</math>, byte3 is selected by <math>(a0.1[4:1] \&amp; 1)</math>, ..., and byte15 is selected by <math>(a0.7[4:1] \&amp; 1)</math>. The rest of the bytes are undefined.</p> <p>For DWord or float movi, byte0 of the destination is selected by <math>(a0.0[4:2] \&amp; 00b)</math>, byte1 is selected by <math>(a0.0[4:2] \&amp; 01b)</math>, byte2 is selected by <math>(a0.0[4:2] \&amp; 10b)</math>, byte3 is selected by <math>(a0.0[4:2] \&amp; 11b)</math>, byte4 is selected by <math>(a0.1[4:2] \&amp; 00b)</math>, byte5 is selected by <math>(a0.1[4:2] \&amp; 01b)</math>, ..., byte31 is selected by <math>(a0.7[4:2] \&amp; 11b)</math>.</p> <p>For all 3 conditions above, <math>a0.n[4:0] = a0.n[4:0] + \text{addr\_imm}[4:0]</math>.</p>	
<b>Restriction</b>	
Source operand cannot be accumulators. The source operand must be a general register.	
The source and destination must have the same type.	
The execution size must be 8.	
The address register for the source must be aligned to the base (a0.0).	
The destination register (directly or indirectly addressed) must be 16-byte aligned.	
The destination region (directly or indirectly addressed) must point to the same GRF register.	
The destination stride in bytes must equal the source element size in bytes.	
The Align16 access mode is not allowed.	
All the index registers (address subregisters) used must point to the same GRF register.	
The instruction must use 1x1 indirect regioning.	

## movi - Move Indexed

The destination offset is only used to create channel enables. Each element of the destination is directly mapped to the index registers for the movi instruction. i.e. a0.0 -> dst.0, a0.1 -> dst.1, a0.2 -> dst.2, etc.

Only 8 address subregisters are used (a0.0-a0.7). Destination element 8 will be sourced from address register zero (a0.0), dst.9 < -a0.1, etc. This is an exception to the above restriction, for example:  
`movi (8) r31.8:uw r[a0.0,0]<8;8,1>:uw // r31.8:uw<-a0.0:uw, r31.9:uw<-a0.1:uw, etc.`

Conditional Modifier is not allowed for this instruction.

### Syntax

[[pred)] movi (exec\_size) reg reg imm

### Pseudocode

```
Evaluate(WrEn); srcregfile = regfile(src0); srcregbase = reg(address[0]) + reg(addr_imm); for ( n = 0; n <
RegWidth; n++ ) { if ( WrEn.chan[n] ) { srcsubreg = subreg(address[n] + addr_imm); dst.chan[n] =
srcregfile.srcreg.srcsubreg; } }
```

Predication	Conditional Modifier	Saturation	Source Modifier
Y	N	Y	Y

Src Types	Dst Types
B	B
UB	UB
W	W
UW	UW
D	D
UD	UD
F	F

DWord	Bit	Description
0..3	127:64	<b>RegSource</b>
		Exists If: (([Operand Controls][Src0.RegFile]!='IMM')
	Format: EU_INSTRUCTION_SOURCES_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>
Exists If: (([Operand Controls][Src0.RegFile]='IMM')		
Format: EU_INSTRUCTION_SOURCES_IMM32 [CHV, BSW]		
63:32	<b>Operand Controls</b>	
	Format: EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]	
31:0	<b>Header</b>	
	Format: EU_INSTRUCTION_HEADER [CHV, BSW]	

# Multiply

mul - Multiply			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
<p>The mul instruction performs component-wise multiplication of src0 and src1 and stores the results in dst. When multiplying integer datatypes, if src0 is DW and src1 is W, irrespective of the destination datatype, the accumulator maintains full 48-bit precision. This is required to handle the macro for 32x32 multiplication. The macro described in the mach instruction should be used to obtain the full precision 64-bit multiplication results. Note: A 32x32 multiply operation is handled natively, without a macro. When operating in this mode, the resulting 64-bit data is packed, unlike the macro, where the lower and upper 32 bits of the result are written to different general registers by two separate instructions. Refer to the macro description for details. When multiplying integer data types, if one of the sources is a DW, the resulting full precision data is stored in the accumulator. However, if the destination data type is either W or DW, the low bits of the result are written to the destination register and the remaining high bits are discarded. This results in undefined Overflow and Sign flags. Therefore, conditional modifiers and saturation (.sat) cannot be used in this case.</p>			
Format: [(pred)] mul[.cmod] (exec_size) dst src0 src1			
Restriction			
Integer source operands cannot be accumulators.			
When multiplying a DW and any lower precision integer, the DW operand must on src0.			
[CHV, BSW-A]: DW * W is not supported outside MACH macro.			
[CHV, BSW]: When multiplying DW x DW, the dst cannot be accumulator.			
Syntax			
[(pred)] mul[.cmod] (exec_size) reg reg reg [(pred)] mul[.cmod] (exec_size) reg reg imm32			
Pseudocode			
Evaluate(WrEn); for ( n = 0; n < exec_size; n++ ) { if ( WrEn.chan[n] ) { dst.chan[n] = src0.chan[n] * src1.chan[n]; } }			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	Y	Y	Y
Src Types	Dst Types	Project	
*B	*B		
*B	*W		
*B	*D		
*W	*W		
*W	*D		
*W,*D	*D		

## mul - Multiply

DWord	Bit	Description
*D	*Q	
F	F	
DF	DF	
HF	HF	
HF, F	HF, F	CHV, BSW
0..3	127:64	<b>RegSource</b>
		Exists If: ([RegSource][Src1.RegFile]!='IMM')
	Format: EU_INSTRUCTION_SOURCES_REG_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>
Exists If: ([ImmSource][Src1.RegFile]='IMM')		
Format: EU_INSTRUCTION_SOURCES_REG_IMM [CHV, BSW]		
63:32	<b>Operand Controls</b>	
	Format: EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]	
31:0	<b>Header</b>	
	Format: EU_INSTRUCTION_HEADER [CHV, BSW]	



## Multiply Accumulate

<b>mac - Multiply Accumulate</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
The mac instruction takes component-wise multiplication of src0 and src1, adds the results with the corresponding accumulator values, and then stores the final results in dst.			
Format: <code>[(pred)] mac[.cmod] (exec_size) dst src0 src1</code>			
Programming Notes			
When source and destination datatypes are different, the implied datatype for the accumulator operand is always the destination datatype.			
Restriction			
Accumulator is an implicit source and thus cannot be an explicit source operand.			
Syntax			
<code>[(pred)] mac[.cmod] (exec_size) reg reg reg [(pred)] mac[.cmod] (exec_size) reg reg imm32</code>			
Pseudocode			
Evaluate(WrEn); for ( n = 0; n < exec_size; n++ ) { if ( WrEn.chan[n] ) { dst.chan[n] = src0.chan[n] * src1.chan[n] + acc0.chan[n]; } }			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	Y	Y	Y
Src Types	Dst Types	Project	
*B,*W	*B,*W,*D		
F	F		
DF	DF	CHV, BSW	
HF	HF	CHV, BSW	
HF, F	HF, F	CHV, BSW	
DWord	Bit	Description	
0.3	127:64	<b>RegSource</b>	
		Exists If:	<code>([RegSource][Src1.RegFile]!='IMM')</code>
	Format:	<code>EU_INSTRUCTION_SOURCES_REG_REG [CHV, BSW]</code>	
	127:64	<b>ImmSource</b>	
Exists If:		<code>([ImmSource][Src1.RegFile]='=IMM')</code>	
Format:	<code>EU_INSTRUCTION_SOURCES_REG_IMM [CHV, BSW]</code>		

<b>mac - Multiply Accumulate</b>		
	63:32	<b>Operand Controls</b> Format: EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]
	31:0	<b>Header</b> Format: EU_INSTRUCTION_HEADER [CHV, BSW]

## Multiply Accumulate High

<b>mach - Multiply Accumulate High</b>	
Project:	CHV, BSW
Source:	Eulsa
Length Bias:	4
<p>The mach instruction performs DWord integer multiply-accumulate operation and outputs the high DWord (bits 63:32). For each enabled channel, this instruction multiplies the DWord in src0 with the high word of the DWord in src1, left shifts the result by 16 bits, adds it with the corresponding accumulator values, and keeps the whole 64-bit result in the accumulator. It then stores the high DWord (bits 63:32) of the results in dst. This instruction is intended to be used to emulate 32-bit DWord integer multiplication by using the large number of bits available in the accumulator. For example, the following instructions perform vector multiplication of two 32-bit signed integer sources from r2 and r3 and store the resulting vectors with the high 32 bits in r5 and the low 32 bits in r6. <code>mul (8) acc0:d r2.0&lt;8;8,1&gt;:d r3.0&lt;16;8,2&gt;:uw mach (8) r5.0&lt;1&gt;:d r2.0&lt;8;8,1&gt;:d r3.0&lt;8;8,1&gt;:d mov (8) r6.0&lt;1&gt;:d acc0:d // Low 32 bits.</code> Here is a different example including negation. An added preliminary <code>mov</code> is required for source modification on src1. <code>mov (8) r3.0&lt;1&gt;:d -r3&lt;8;8,1&gt;:d mul (8) acc0:d r2.0&lt;8;8,1&gt;:d r3.0&lt;16;8,2&gt;:uw mach (8) r5.0&lt;1&gt;:d r2.0&lt;8;8,1&gt;:d r3.0&lt;8;8,1&gt;:d // High 32 bits mov (8) r6.0&lt;1&gt;:d acc0:d // Low 32 bits.</code> The mach should have channel enable from the destHI of IMUL, the mov should have the channel enable from the destLO of IMUL. As mach is used to generate part of the 64-bit DWord integer results, saturation modifier should not be used. In fact, saturation modifier should not be used for any of these four instructions. Source and destination operands must be DWord integers. Source and destination must be of the same type, signed integer or unsigned integer. If dst is UD, src0 and src1 may be UD and/or D. However, if any of src0 and src1 is D, source modifier (abs) must be present to convert it to match with dst. If dst is D, src0 and src1 must also be D. They cannot be UD as it may cause unexpected overflow because the computed results are limited to 64 bits.</p>	
Format: [(pred)] mach[.cmod] (exec_size) dst src0 src1	
<b>Restriction</b>	
Accumulator is an implicit source and thus cannot be an explicit source operand.	
AccWrEn is required.	
<b>Syntax</b>	
[(pred)] mach[.cmod] (exec_size) reg reg reg [(pred)] mach[.cmod] (exec_size) reg reg imm32	
<b>Pseudocode</b>	
<pre> Evaluate(WrEn); for ( n = 0; n &lt; exec_size; n++ ) { if ( WrEn.chan[n] ) { acc.chan[n][63:0] = (src1.chan[n][31:16] * src0.chan[n][31:0]) &lt;&lt; 16 + acc.chan[n][63:0]; dst.chan[n][31:0] = acc.chan[n][63:32]; } }                     </pre>	
<b>Errata</b>	<b>Description</b>
	A source modifier must not be used on src1 for the macro operation. This applies to both mul and mach of the macro. If source modifier is required, an additional mov instruction may be used before the macro.

<b>mach - Multiply Accumulate High</b>			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	N	Y	Y
Src Types	Dst Types		
D	D		
UD	UD		
DWord	Bit	Description	
0..3	127:64	<b>RegSource</b>	
		Exists If:	([RegSource][Src1.RegFile]!='IMM')
	Format:	EU_INSTRUCTION_SOURCES_REG_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>	
Exists If:		([ImmSource][Src1.RegFile]=='IMM')	
Format:	EU_INSTRUCTION_SOURCES_REG_IMM [CHV, BSW]		
63:32	<b>Operand Controls</b>		
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]	
31:0	<b>Header</b>		
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]	

## Multiply Add

<b>mad - Multiply Add</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
The mad instruction takes component-wise multiplication of src1 and src2, adds the results with the corresponding src0 values, and then stores the final results in dst.			
Format: [(pred)] mad[.cmod] (exec_size) dst src0 src1 src2			
Restriction			Project
[CHV, BSW]: No explicit accumulator access because this is a three-source instruction. AccWrEn is allowed for implicitly updating the accumulator.			CHV, BSW
[CHV, BSW]: All three-source instructions have certain restrictions, described in Instruction Formats [CHV, BSW].			CHV, BSW
Syntax			
[(pred)] mad[.cmod] (exec_size) reg reg reg reg			
Pseudocode			
Evaluate(WrEn); for ( n = 0; n < exec_size; n++ ) { if ( WrEn.chan[n] ) { dst.chan[n] = src1.chan[n] * src2.chan[n] + src0.chan[n]; } }			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	Y	Y	Y
Src Types	Dst Types	Project	
F	F		
DF	DF	CHV, BSW	
HF	HF	CHV, BSW	
HF, F	HF, F	CHV, BSW	
DWord	Bit	Description	
0..3	127:126	<b>Reserved</b>	
		Format:	MBZ
	125:106	<b>Source 2</b>	
		Format:	EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC [CHV, BSW]
105		<b>Reserved</b>	
		Format:	MBZ
104:85		<b>Source 1</b>	
		Format:	EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC [CHV, BSW]

<b>mad - Multiply Add</b>		
84	<b>Reserved</b>	Format: MBZ
83:64	<b>Source 0</b>	Format: EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC [CHV, BSW]
63:56	<b>Destination Register Number</b>	Format: DstRegNum [CHV, BSW]
55:53	<b>Destination Subregister Number</b>	Format: DstSubRegNum[2:0]
52:49	<b>Destination Channel Enable</b>	Format: ChanEn[4] Four channel enables are defined for controlling which channels are written into the destination region. These channel mask bits are applied in a modulo-four manner to all ExecSize channels. There is 1-bit Channel Enable for each channel within the group of 4. If the bit is cleared, the write for the corresponding channel is disabled. If the bit is set, the write is enabled. Mnemonics for the bit being set for the group of 4 are x, y, z, and w, respectively, where x corresponds to Channel 0 in the group and w corresponds to channel 3 in the group
48:42	<b>Reserved</b>	Format: MBZ
41:40	<b>Source 2 Modifier</b>	Exists If: $\text{!}([Property[Source\ Modifier]] = 'true')$ Format: SrcMod [CHV, BSW]
39:38	<b>Source 1 Modifier</b>	Exists If: $\text{!}([Property[Source\ Modifier]] = 'true')$ Format: SrcMod [CHV, BSW]
41:36	<b>Reserved</b>	Exists If: $\text{!}([Property[Source\ Modifier]] = 'false')$ Format: MBZ
37:36	<b>Source 0 Modifier</b>	Exists If: $\text{!}([Property[Source\ Modifier]] = 'true')$ Format: SrcMod [CHV, BSW]
35	<b>Reserved</b>	Format: MBZ
34	<b>Reserved</b>	Format: MBZ
33	<b>Flag Subregister Number</b>	This field contains the flag subregister number for instructions with a non-zero Conditional Modifier.

<b>mad - Multiply Add</b>		
	32	<b>Reserved</b>
		Format: MBZ
	31:0	<b>Header</b>
		Format: EU_INSTRUCTION_HEADER [CHV, BSW]

## Multiply Add for Macro

<b>madm - Multiply Add for Macro</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
<p>The madm instruction takes component-wise multiplication of src1 and src2, adds the results with the corresponding src0 values, and then stores the final results in dst. The source and destination operands have a higher precision carried in the exponent for this operation. The madm instruction is used for macro operations, where precision is accumulated over several instructions. This accumulation requires the exponent to increase by 2 extra bits across multiple madm operations. Refer to Macros Defined in 'Math' Section for usage and restrictions of this operation.</p>			
Format: [(pred)] madm[.cmod] (exec_size) dst src0 src1 src2			
Restriction			
Accumulator access is restricted to the special accumulators (acc2-acc9). Refer to the Accumulator Section for details on the special accumulators.			
Syntax			
[(pred)] madm[.cmod] (exec_size) reg reg reg reg			
Pseudocode			
Evaluate(WrEn); for ( n = 0; n < exec_size; n++ ) { if ( WrEn.chan[n] ) { dst.chan[n] = src1.chan[n] * src2.chan[n] + src0.chan[n]; } }			
Predication	Conditional Modifier	Saturation	Source Modifier
N	N	N	N
Src Types	Dst Types		
F	F		
DF	DF		
DWord	Bit	Description	
0..3	127:126	<b>Reserved</b>	
		Format:	MBZ
	125:106	<b>Source 2</b>	
		Format:	EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC [CHV, BSW]
105		<b>Reserved</b>	
		Format:	MBZ
104:85		<b>Source 1</b>	
		Format:	EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC [CHV, BSW]



<b>madm - Multiply Add for Macro</b>		
84	<b>Reserved</b>	Format: MBZ
83:64	<b>Source 0</b>	Format: EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC [CHV, BSW]
63:56	<b>Destination Register Number</b>	Format: DstRegNum [CHV, BSW]
55:53	<b>Destination Subregister Number</b>	Format: DstSubRegNum[2:0]
52:49	<b>Destination Channel Enable</b>	Format: ChanEn[4] Four channel enables are defined for controlling which channels are written into the destination region. These channel mask bits are applied in a modulo-four manner to all ExecSize channels. There is 1-bit Channel Enable for each channel within the group of 4. If the bit is cleared, the write for the corresponding channel is disabled. If the bit is set, the write is enabled. Mnemonics for the bit being set for the group of 4 are x, y, z, and w, respectively, where x corresponds to Channel 0 in the group and w corresponds to channel 3 in the group
48:42	<b>Reserved</b>	Format: MBZ
41:40	<b>Source 2 Modifier</b>	Exists If: $///([Property[Source\ Modifier]] = 'true')$ Format: SrcMod [CHV, BSW]
39:38	<b>Source 1 Modifier</b>	Exists If: $///([Property[Source\ Modifier]] = 'true')$ Format: SrcMod [CHV, BSW]
41:36	<b>Reserved</b>	Exists If: $///([Property[Source\ Modifier]] = 'false')$ Format: MBZ
37:36	<b>Source 0 Modifier</b>	Exists If: $///([Property[Source\ Modifier]] = 'true')$ Format: SrcMod [CHV, BSW]
35	<b>Reserved</b>	Format: MBZ
34	<b>Reserved</b>	Format: MBZ
33	<b>Flag Subregister Number</b>	This field contains the flag subregister number for instructions with a non-zero Conditional Modifier.

<b>madm - Multiply Add for Macro</b>		
	32	<b>Reserved</b>
		Format: <span style="float: right;">MBZ</span>
	31:0	<b>Header</b>
		Format: <span style="float: right;">EU_INSTRUCTION_HEADER [CHV, BSW]</span>

## No Operation

<b>nop - No Operation</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
Do nothing. The nop instruction takes an instruction dispatch but performs no operation. It can be used for assembly patching in memory, or to insert a delay in the program sequence.			
Format: nop			
Restriction			
The nop instruction takes no instruction options other than Breakpoint.			
Syntax			
nop			
Pseudocode			
{ ; // The null statement, which does nothing. }			
Predication	Conditional Modifier	Saturation	Source Modifier
N	N	N	N
DWord	Bit	Description	
0..3	127:31	<b>Reserved</b> Format: <span style="border: 1px solid black; padding: 2px;">MBZ</span>	
	30	<b>Reserved</b>	
	29:7	<b>Reserved</b> Format: <span style="border: 1px solid black; padding: 2px;">MBZ</span>	
	6:0	<b>Opcode</b> Format: <span style="border: 1px solid black; padding: 2px;">EU_OPCODE</span>	

## Oword Block Read MSD

<b>MSD0R_OWB - Oword Block Read MSD</b>								
Project:	CHV, BSW							
Source:	DataPort 0							
Length Bias:	1							
Family:	Block R/W							
Group:	OW Block R/W							
DWord	Bit	Description						
0	19	<p><b>Header Present</b></p> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_MHR</td> </tr> </table> <p>Indicates that the message requires a header.</p>	Project:	All	Format:	MDC_MHR		
	Project:	All						
	Format:	MDC_MHR						
	18	<p><b>Legacy Message</b></p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>0h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Legacy Message</p>	Default Value:	0h	Project:	All	Format:	Opcode
	Default Value:	0h						
	Project:	All						
	Format:	Opcode						
	17:14	<p><b>Message Type</b></p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>00h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Oword Block Read message</p>	Default Value:	00h	Project:	All	Format:	Opcode
Default Value:	00h							
Project:	All							
Format:	Opcode							
13	<p><b>Invalidate After Read</b></p> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_IAR [CHV, BSW]</td> </tr> </table> <p>Specifies if L3 cache lines accessed by the message should be invalidated after the read occurs</p>	Project:	All	Format:	MDC_IAR [CHV, BSW]			
Project:	All							
Format:	MDC_IAR [CHV, BSW]							
12:11	<p><b>Reserved</b></p>							
10:8	<p><b>Data Elements</b></p> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_DB_OW</td> </tr> </table> <p>Specifies the number of contiguous Owords to be read or written</p>	Project:	All	Format:	MDC_DB_OW			
Project:	All							
Format:	MDC_DB_OW							
7:0	<p><b>Binding Table Index</b></p> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_BTS_A32</td> </tr> </table> <p>Specifies the Binding Table Index for the message</p>	Project:	All	Format:	MDC_BTS_A32			
Project:	All							
Format:	MDC_BTS_A32							

## Oword Block Write MSD

<b>MSD0W_OWB - Oword Block Write MSD</b>		
Project:	CHV, BSW	
Source:	DataPort 0	
Length Bias:	1	
Family:	Block R/W	
Group:	OW Block R/W	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHR [CHV, BSW]
	Indicates that the message requires a header.	
	18	<b>Legacy Message</b>
		Default Value: 0h
Project: All		
Format: Opcode		
Legacy Message		
17:14	<b>Message Type</b>	
	Default Value: 08h	
	Project: All	
	Format: Opcode	
Oword Block Write message		
13:11	<b>Reserved</b>	
	Project: All	
	Format: MBZ	
Ignored		
10:8	<b>Data Elements</b>	
	Project: All	
	Format: MDC_DB_OW	
Specifies the number of contiguous Owords to be read or written		
7:0	<b>Binding Table Index</b>	
	Project: All	
	Format: MDC_BTS_A32	
Specifies the Binding Table Index for the message		

## Oword Dual Block Read MSD

MSD0R_OWDB - Oword Dual Block Read MSD			
Project:	CHV, BSW		
Source:	DataPort 0		
Length Bias:	1		
Family:	Block R/W		
Group:	OW Dual Block R/W		
DWord	Bit	Description	
0	19	<b>Header Present</b>	
		Project:	All
		Format:	Enable
		If set, indicates that the message includes the header.	
	18	<b>Legacy Message</b>	
		Default Value:	0h
		Project:	All
		Format:	Opcode
	Legacy Message		
	17:14	<b>Message Type</b>	
Default Value:		02h	
Project:		All	
Format:		Opcode	
Oword Block Read message			
13	<b>Invalidate After Read</b>		
	Project:	All	
	Format:	MDC_IAR [CHV, BSW]	
Specifies if L3 cache lines accessed by the message should be invalidated after the read occurs			
12:10	<b>Reserved</b>		
9:8	<b>Data Elements</b>		
	Project:	All	
	Format:	MDC_DB_OWDB [CHV, BSW]	
Specifies the number of contiguous Owords to be read or written			
7:0	<b>Binding Table Index</b>		
	Project:	All	
	Format:	MDC_BTS_A32 [CHV, BSW]	
Specifies the Binding Table Index for the message			

## Oword Dual Block Write MSD

<b>MSD0W_OWDB - Oword Dual Block Write MSD</b>								
Project:	CHV, BSW							
Source:	DataPort 0							
Length Bias:	1							
Family:	Block R/W							
Group:	OW Dual Block R/W							
DWord	Bit	Description						
0	19	<b>Header Present</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> If set, indicates that the message includes the header.	Project:	All	Format:	Enable		
	Project:	All						
	Format:	Enable						
	18	<b>Legacy Message</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td>0h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> Legacy Message	Default Value:	0h	Project:	All	Format:	Opcode
	Default Value:	0h						
	Project:	All						
	Format:	Opcode						
	17:14	<b>Message Type</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td>0Ah</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> Oword Block Read message	Default Value:	0Ah	Project:	All	Format:	Opcode
	Default Value:	0Ah						
	Project:	All						
Format:	Opcode							
13:10	<b>Reserved</b>							
9:8	<b>Data Elements</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_DB_OWD [CHV, BSW]</td> </tr> </table> Specifies the number of contiguous Owords to be read or written	Project:	All	Format:	MDC_DB_OWD [CHV, BSW]			
Project:	All							
Format:	MDC_DB_OWD [CHV, BSW]							
7:0	<b>Binding Table Index</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_BTS_A32 [CHV, BSW]</td> </tr> </table> Specifies the Binding Table Index for the message	Project:	All	Format:	MDC_BTS_A32 [CHV, BSW]			
Project:	All							
Format:	MDC_BTS_A32 [CHV, BSW]							

## Oword Unaligned Block Read MSD

<b>MSD0R_OWUB - Oword Unaligned Block Read MSD</b>								
Project:	CHV, BSW							
Source:	DataPort 0							
Length Bias:	1							
Family:	Block R/W							
Group:	OW Unaligned Block R/W							
DWord	Bit	Description						
0	19	<p><b>Header Present</b></p> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_MHR [CHV, BSW]</td> </tr> </table> <p>Indicates that the message requires a header.</p>	Project:	All	Format:	MDC_MHR [CHV, BSW]		
	Project:	All						
	Format:	MDC_MHR [CHV, BSW]						
	18	<p><b>Legacy Message</b></p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>0h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Legacy Message</p>	Default Value:	0h	Project:	All	Format:	Opcode
	Default Value:	0h						
Project:	All							
Format:	Opcode							
17:14	<p><b>Message Type</b></p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>01h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Oword Unaligned Block Read message</p>	Default Value:	01h	Project:	All	Format:	Opcode	
Default Value:	01h							
Project:	All							
Format:	Opcode							
13:11	<p><b>Reserved</b></p>							
10:8	<p><b>Data Elements</b></p> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_DB_OW [CHV, BSW]</td> </tr> </table> <p>Specifies the number of contiguous Owords to be read</p>	Project:	All	Format:	MDC_DB_OW [CHV, BSW]			
Project:	All							
Format:	MDC_DB_OW [CHV, BSW]							
7:0	<p><b>Binding Table Index</b></p> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_BTS_A32 [CHV, BSW]</td> </tr> </table> <p>Specifies the Binding Table Index for the message</p>	Project:	All	Format:	MDC_BTS_A32 [CHV, BSW]			
Project:	All							
Format:	MDC_BTS_A32 [CHV, BSW]							



## PIPE\_CONTROL

PIPE_CONTROL			
Project:	CHV, BSW		
Source:	RenderCS		
Length Bias:	2		
The PIPE_CONTROL command is used to effect the synchronization described above.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	<b>Command SubType</b>	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	<b>3D Command Opcode</b>	
		Default Value:	2h PIPE_CONTROL
		Format:	OpCode
	23:16	<b>3D Command Sub Opcode</b>	
		Default Value:	0h PIPE_CONTROL
		Format:	OpCode
	15:8	<b>Reserved</b>	
		Project:	All
Format:		MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	4h DWORD_COUNT_n	
	Project:	CHV, BSW	
	Format:	=n	
	Total Length - 2. Excludes DWord (0,1).		
1	31:29	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	28	<b>Reserved</b>	
		Project:	CHV, BSW
		Format:	MBZ
	27	<b>Reserved</b>	
		Project:	CHV, BSW

<b>PIPE_CONTROL</b>			
26	<b>Reserved</b>		
25	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
24	<b>Destination Address Type</b>		
	Project:	CHV, BSW	
	Defines address space of Destination Address		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0h	PPGTT	Use PPGTT address space for DW write
	1h	GGTT	Use GGTT address space for DW write
			<b>Project</b>
			All
			All
	<b>Programming Notes</b>		
	Ignored if ""No Write" is selected in Operation.		
23	<b>LRI Post Sync Operation</b>		
	Project:	CHV, BSW	
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0h	No LRI Operation	No LRI operation occurs as a result of this instruction. The Post-Sync Operation field is valid and may be used to specify an operation.
	1h	MMIO Write Immediate Data	Write the DWord contained in Immediate Data Low (DW3) to the MMIO offset specified in the Address field.
			<b>Project</b>
			All
			All
	<b>Programming Notes</b>		
	This bit causes a post sync operation with an LRI (Load Register Immediate) operation. If this bit is set then the Post-Sync Operation field must be cleared.		
22	<b>Reserved</b>		
	Project:	All	
21	<b>Store Data Index</b>		
	Project:		
	Format:	U1	
	<p>Ring Buffer Mode Scheduling: This field is valid only if the post-sync operation is not 0. If this bit is set, the store data address is actually an index into the global hardware status page. This bit only applies to the Global HW status page. If this field is 1, the Destination Address Type in this command must be set to 1 (GGTT). Execlist Mode Scheduling: This field is valid only if the post-sync operation is not 0. If this bit is set, the store data address is index into the global hardware status page when destination address type in the command is set to 1 (GGTT). The store data address is index into the per-process hardware status page when destination address type in the command is set to 0 (PPGTT).</p>		

<b>PIPE_CONTROL</b>						
20	<p><b>Command Streamer Stall Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>If ENABLED, the sync operation will not occur until all previous flush operations pending a completion of those previous flushes will complete, including the flush produced from this command. This enables the command to act similar to the legacy MI_FLUSH command.</p> <table border="1" style="width: 100%; background-color: #e6f2ff;"> <tr> <th style="text-align: center;">Programming Notes</th> </tr> </table> <p>One of the following must also be set:</p> <ul style="list-style-type: none"> <li>• Render Target Cache Flush Enable ([12] of DW1)</li> <li>• Depth Cache Flush Enable ([0] of DW1)</li> <li>• Stall at Pixel Scoreboard ([1] of DW1)</li> <li>• Depth Stall ([13] of DW1)</li> <li>• Post-Sync Operation ([13] of DW1)</li> <li>• DC Flush Enable([5] of DW1)</li> </ul> <p>This field must always be set in all PIPE_CONTROL commands having "Post-Sync Operation" set to "Report PS Depth Count" or "Report Time Stamp" when user wishes to set "Post-Sync Operation" bit in any of the MI_ATOMIC or MI_SEMAPHORE_SIGNAL commands programmed.</p> <p>This bit must be always set when PIPE_CONTROL command is programmed by GPGPU and MEDIA workloads, except for the cases when only Read Only Cache Invalidation bits are set (State Cache Invalidation Enable, Instruction cache Invalidation Enable, Texture Cache Invalidation Enable, Constant Cache Invalidation Enable). This is to WA FFDOP CG issue.</p>	Project:	All	Format:	U1	Programming Notes
Project:	All					
Format:	U1					
Programming Notes						
19	<b>Reserved</b>					
18	<p><b>TLB Invalidate</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>If ENABLED, all TLBs belonging to Render Engine will be invalidated once the flush operation is complete. Note that if the flush TLB invalidation mode is clear, a TLB invalidate will occur irrespective of this bit setting</p> <p>If ENABLED, PIPE_CONTROL command will flush the in flight data written out by render engine to Global Observation point on flush done. Also Requires stall bit ([20] of DW1) set.</p> <table border="1" style="width: 100%; background-color: #e6f2ff;"> <tr> <th style="text-align: center;">Programming Notes</th> </tr> </table> <p>If ENABLED, all TLBs belonging to Render Engine will be invalidated once the flush operation is complete. Note that if the flush TLB invalidation mode is clear, a TLB invalidate will occur irrespective of this bit setting.</p>	Project:	All	Format:	U1	Programming Notes
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17	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table>	Project:	CHV, BSW			
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<b>PIPE_CONTROL</b>																																																	
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16	<p><b>Generic Media State Clear</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Disable</td> </tr> </table> <p>If set, all generic media state context information will be invalidated. Any state invalidated will not be saved as part of the render engine context image. The state only become valid once it is parsed by the command streamer.</p>	Project:	CHV, BSW	Format:	Disable																																												
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15:14	<p><b>Post Sync Operation</b></p> <table border="1"> <tr> <th colspan="4" style="text-align: center;">Description</th> </tr> <tr> <td colspan="4">This field specifies an optional action to be taken upon completion of the synchronization operation.</td> </tr> <tr> <td colspan="4">This field must be cleared if the LRI Post-Sync Operation bit is set.</td> </tr> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> <tr> <td>0h</td> <td>No Write</td> <td>No write occurs as a result of this instruction. This can be used to implement a "trap" operation, etc.</td> <td>All</td> </tr> <tr> <td>1h</td> <td>Write Immediate Data</td> <td>Write the QWord containing Immediate Data Low, High DWs to the Destination Address</td> <td>All</td> </tr> <tr> <td>2h</td> <td>Write PS Depth Count</td> <td>Write the 64-bit PS_DEPTH_COUNT register to the Destination Address</td> <td>All</td> </tr> <tr> <td>3h</td> <td>Write Timestamp</td> <td>Write the 64-bit TIMESTAMP register to the Destination Address</td> <td>All</td> </tr> <tr> <th colspan="4" style="text-align: center;">Programming Notes</th> </tr> <tr> <td colspan="4">If executed in non-secure batch buffer, the address given will be in a PPGTT address space. If in a secure ring or batch, address given will be in GGTT space</td> </tr> <tr> <th colspan="4" style="text-align: center;">Workaround</th> </tr> <tr> <td colspan="4">Workaround: PIPECONTROL command with "Command Streamer Stall Enable" must be programmed prior to programming a PIPECONTROL command with Post Sync Op in GPGPU mode of operation (i.e when PIPELINE_SELECT command is set to GPGPU mode of operation).</td> </tr> </table>	Description				This field specifies an optional action to be taken upon completion of the synchronization operation.				This field must be cleared if the LRI Post-Sync Operation bit is set.				Value	Name	Description	Project	0h	No Write	No write occurs as a result of this instruction. This can be used to implement a "trap" operation, etc.	All	1h	Write Immediate Data	Write the QWord containing Immediate Data Low, High DWs to the Destination Address	All	2h	Write PS Depth Count	Write the 64-bit PS_DEPTH_COUNT register to the Destination Address	All	3h	Write Timestamp	Write the 64-bit TIMESTAMP register to the Destination Address	All	Programming Notes				If executed in non-secure batch buffer, the address given will be in a PPGTT address space. If in a secure ring or batch, address given will be in GGTT space				Workaround				Workaround: PIPECONTROL command with "Command Streamer Stall Enable" must be programmed prior to programming a PIPECONTROL command with Post Sync Op in GPGPU mode of operation (i.e when PIPELINE_SELECT command is set to GPGPU mode of operation).			
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13	<p><b>Depth Stall Enable</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This bit must be set when obtaining a "visible pixel" count to preclude the possible inclusion in the PS_DEPTH_COUNT value written to memory of some fraction of pixels from objects initiated after the PIPE_CONTROL command.</p>	Project:	All	Format:	Enable																																												
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Format:	Enable																																																

<b>PIPE_CONTROL</b>				
	<b>Value</b>	<b>Name</b>	<b>Description</b>	
	0h	Disable	3D pipeline will not stall subsequent primitives at the Depth Test stage.	
	1h	Enable	3D pipeline will stall any subsequent primitives at the Depth Test stage until the Sync and Post-Sync operations complete.	
<b>Programming Notes</b>				
This bit must be DISABLED for operations other than writing PS_DEPTH_COUNT.				
This bit will have no effect (besides preventing write cache flush) if set in a PIPE_CONTROL command issued to the Media pipe.				
12	<b>Render Target Cache Flush Enable</b>			
	Project:	All		
	Format:	Enable		
Setting this bit will force Render Cache to be flushed to memory prior to this synchronization point completing. This bit must be set for all write fence sync operations to assure that results from operations initiated prior to this command are visible in memory once software observes this synchronization.				
	<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>
	0h	Disable Flush	Render Target Cache is NOT flushed.	All
	1h	Enable Flush	Render Target Cache is flushed.	All
<b>Programming Notes</b>				
This bit must be DISABLED for End-of-pipe (Read) fences, PS_DEPTH_COUNT or TIMESTAMP queries.				
This bit must not be set when Depth Stall Enable bit is set in this packet.				
11	<b>Instruction Cache Invalidate Enable</b>			
	Project:	All		
	Format:	Enable		
Setting this bit is independent of any other bit in this packet. This bit controls the invalidation of the L1 and L2 at the top of the pipe i.e. at the parsing time.				
10	<b>Texture Cache Invalidation Enable</b>			
	Project:	All		
	Format:	Enable		
Setting this bit is independent of any other bit in this packet. This bit controls the invalidation of the texture caches at the top of the pipe i.e. at the parsing time.				
9	<b>Indirect State Pointers Disable</b>			
	Project:	All		

<b>PIPE_CONTROL</b>							
	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>Enable</td> </tr> </table>	Format:	Enable				
Format:	Enable						
	<table border="1" style="width: 100%;"> <tr> <th style="text-align: center; background-color: #e1eef6;">Description</th> </tr> <tr> <td> <p>At the completion of the post-sync operation associated with this pipe control packet, the indirect state pointers in the hardware are considered invalid; the indirect pointers are not saved in the context. If any new indirect state commands are executed in the command stream while the pipe control is pending, the new indirect state commands are preserved.</p> <p>[CHV, BSW]: Using Invalidate State Pointer (ISP) only inhibits context restoring of Push Constant (3DSTATE_CONSTANT_*) commands. Push Constant commands are only considered as Indirect State Pointers. Once ISP is issued in a context, SW must initialize by programming push constant commands for all the shaders (at least to zero length) before attempting any rendering operation for the same context.</p> </td> </tr> </table>	Description	<p>At the completion of the post-sync operation associated with this pipe control packet, the indirect state pointers in the hardware are considered invalid; the indirect pointers are not saved in the context. If any new indirect state commands are executed in the command stream while the pipe control is pending, the new indirect state commands are preserved.</p> <p>[CHV, BSW]: Using Invalidate State Pointer (ISP) only inhibits context restoring of Push Constant (3DSTATE_CONSTANT_*) commands. Push Constant commands are only considered as Indirect State Pointers. Once ISP is issued in a context, SW must initialize by programming push constant commands for all the shaders (at least to zero length) before attempting any rendering operation for the same context.</p>				
Description							
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8	<p><b>Notify Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>If ENABLED, a Sync Completion Interrupt will be generated (if enabled by the MI Interrupt Control registers) once the sync operation is complete. See Interrupt Control Registers in Memory Interface Registers for details.</p>	Project:	All	Format:	Enable		
Project:	All						
Format:	Enable						
7	<p><b>Pipe Control Flush Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>Hardware on parsing PIPECONTROL command with Pipe Control Flush Enable set will wait for all the outstanding post sync operations corresponding to previously executed PIPECONTROL commands are complete before making forward progress.</p>	Project:	CHV, BSW	Format:	Enable		
Project:	CHV, BSW						
Format:	Enable						
6	<p><b>Reserved</b></p>						
5	<p><b>DC Flush Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>Setting this bit enables flushing of the L3\$ portions that caches DC writes.</p> <table border="1" style="width: 100%;"> <tr> <th style="text-align: center; background-color: #e1eef6;">Programming Notes</th> </tr> <tr> <td> <p>DC Flush (L3 Flush) by default doesn't result in flushing/invalidating the IA Coherent lines from L3\$, however this can be achieved by setting control bit "<b>Pipe line flush Coherent lines</b>" in "L3SQCREG4" register.</p> </td> </tr> </table>	Project:	CHV, BSW	Format:	Enable	Programming Notes	<p>DC Flush (L3 Flush) by default doesn't result in flushing/invalidating the IA Coherent lines from L3\$, however this can be achieved by setting control bit "<b>Pipe line flush Coherent lines</b>" in "L3SQCREG4" register.</p>
Project:	CHV, BSW						
Format:	Enable						
Programming Notes							
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4	<p><b>VF Cache Invalidation Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>Setting this bit is independent of any other bit in this packet. This bit controls the invalidation of VF address based cache at the top of the pipe i.e. at the parsing time.</p>	Project:	All	Format:	Enable		
Project:	All						
Format:	Enable						

<b>PIPE_CONTROL</b>				
	<b>Workaround</b>		<b>Project</b>	
	Workaround: When VF Cache Invalidate is set "Post Sync Operation" must be enabled to "Write Immediate Data" or "Write PS Depth Count" or "Write Timestamp".		CHV, BSW	
3	<b>Constant Cache Invalidation Enable</b>			
	Project:	All		
	Format:	Enable		
	Setting this bit is independent of any other bit in this packet. This bit controls the invalidation of the constant cache at the top of the pipe i.e. at the parsing time.			
2	<b>State Cache Invalidation Enable</b>			
	Project:	All		
	Format:	Enable		
	Setting this bit is independent of any other bit in this packet. This bit controls the invalidation of the L1 and L2 state caches at the top of the pipe i.e. at the parsing time.			
1	<b>Stall At Pixel Scoreboard</b>			
	Project:	All		
	Format:	Enable		
	Defines the behavior of PIPE_CONTROL command at the pixel scoreboard.			
	<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>
	0h	Disable	Stall at the pixel scoreboard is disabled.	All
	1h	Enable	Stall at the pixel scoreboard is enabled.	All
	<b>Programming Notes</b>			
	This bit must be DISABLED for End-of-pipe (Read) fences, PS_DEPTH_COUNT or TIMESTAMP queries. This bit is ignored if Depth Stall Enable is set. Further the render cache is not flushed even if Write Cache Flush Enable bit is set.			
0	<b>Depth Cache Flush Enable</b>			
	Project:	All		
	Format:	Enable		
	Setting this bit enables flushing (i.e. writing back the dirty lines to memory and invalidating the tags) of depth related caches. This bit applies to HiZ cache, Stencil cache and depth cache.			
	<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>
	0h	Flush Disabled	Depth relates caches (HiZ, Stencil and Depth) are NOT flushed.	All
	1h	Flush Enabled	Depth relates caches (HiZ, Stencil and Depth) are flushed.	All
	<b>Programming Notes</b>			
	Ideally depth caches need to be flushed only when depth is required to be coherent in memory for later use as a texture, source or honoring CPU lock. This bit must be DISABLED			

<b>PIPE_CONTROL</b>						
		for End-of-pipe (Read) fences, PS_DEPTH_COUNT or TIMESTAMP queries.				
2	31:2	<p><b>Address</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[31:2]U32</td> </tr> </table> <p>If <b>Post Sync Operation</b> is set to 1h ([CHV, BSW]: <b>LRI Post-Sync Operation</b> must be clear): Bits 31:3 specify the QW address of where the Immediate Data following this DW in the packet to be stored. Bit 2 MBZ Ignored if "No Write" is the selected in Post-Sync Operation [CHV, BSW]: If <b>LRI Post-Sync Operation</b> is set: Bits 22:2 (Bits 31:23 are reserved MBZ) specify the MMIO offset destination for the data in the <b>Immediate Data Low</b> (DW3) field. Only DW writes are valid.</p>	Project:	CHV, BSW	Format:	GraphicsAddress[31:2]U32
	Project:	CHV, BSW				
Format:	GraphicsAddress[31:2]U32					
1:0	<b>Reserved</b>					
3	31:16	<b>Reserved</b>				
	15:0	<p><b>Address High</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[47:32]U32</td> </tr> </table> <p>This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space. This field is valid only if the post-sync operation is not 0 and the LRI Post-Sync Operation is clear.</p>	Project:	All	Format:	GraphicsAddress[47:32]U32
Project:	All					
Format:	GraphicsAddress[47:32]U32					
4..5	63:0	<p><b>Immediate Data</b></p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U64</td> </tr> </table> <p>This field specifies the QWord value to be written to the targeted location. Only valid when Post-Sync Operation is 1h (Write Immediate Data) or LRI Post-Sync Operation is set. Ignored if Post-Sync Operation is "No write", "Write PS_DEPTH_COUNT" or "Write TIMESTAMP".</p>	Project:	CHV, BSW	Format:	U64
		Project:	CHV, BSW			
Format:	U64					
<table border="1"> <thead> <tr> <th style="text-align: center;"><b>Programming Notes</b></th> <th style="text-align: center;"><b>Project</b></th> </tr> </thead> <tbody> <tr> <td>This field must be programmed to 0 when Post-Sync Operation is set to Write PS Depth Count or Write Timestamp.</td> <td>CHV, BSW</td> </tr> </tbody> </table>	<b>Programming Notes</b>	<b>Project</b>	This field must be programmed to 0 when Post-Sync Operation is set to Write PS Depth Count or Write Timestamp.	CHV, BSW		
<b>Programming Notes</b>	<b>Project</b>					
This field must be programmed to 0 when Post-Sync Operation is set to Write PS Depth Count or Write Timestamp.	CHV, BSW					



## PIPELINE\_SELECT

<b>PIPELINE_SELECT</b>	
Project:	CHV, BSW
Source:	PRM
Length Bias:	1
<b>Description</b>	
The PIPELINE_SELECT command is used to specify which GPE pipeline is to be considered the 'current' active pipeline. Issuing 3D-pipeline-specific commands when the Media pipeline is selected, or vice versa, is UNDEFINED.	
Issuing 3D-pipeline-specific commands when the GPGPU pipeline is selected, or vice versa, is UNDEFINED.	
Programming common non pipeline commands (e.g., STATE_BASE_ADDRESS) is allowed in all pipeline modes.	
<b>Programming Notes</b>	
Software must ensure all the write caches are flushed through a stalling PIPE_CONTROL command followed by another PIPE_CONTROL command to invalidate read only caches prior to programming MI_PIPELINE_SELECT command to change the Pipeline Select Mode. Example: ... Workload-3Dmode PIPE_CONTROL (CS Stall, Depth Cache Flush Enable, Render Target Cache Flush Enable, DC Flush Enable) PIPE_CONTROL (Constant Cache Invalidate, Texture Cache Invalidate, Instruction Cache Invalidate, State Cache invalidate) PIPELINE_SELECT ( GPGPU)	
Software must clear the <b>COLOR_CALC_STATE Valid</b> field in 3DSTATE_CC_STATE_POINTERS command prior to send a PIPELINE_SELECT with <b>Pipeline Select</b> set to GPGPU.	
Render CS Only: SW must always program PIPE_CONTROL with CS Stall and Render Target Cache Flush Enable set prior to programming PIPELINE_SELECT command for GPGPU workloads i.e when pipeline mode is set to GPGPU. This is required to achieve better GPGPU preemption latencies for certain programming sequences. If programming PIPE_CONTROL has performance implications then preemption latencies can be trade off against performance by not implementing this programming note.	
Hardware Binding Tables are only supported for 3D workloads. Resource streamer must be enabled only for 3D workloads. Resource streamer must be disabled for Media and GPGPU workloads. Batch buffer containing both 3D and GPGPU workloads must take care of disabling and enabling Resource Streamer appropriately while changing the PIPELINE_SELECT mode from 3D to GPGPU and vice versa. Resource streamer must be disabled using MI_RS_CONTROL command and Hardware Binding Tables must be disabled by programming 3DSTATE_BINDING_TABLE_POOL_ALLOC with "Binding Table Pool Enable" set to disable (i.e. value '0'). Example below shows disabling and enabling of resource streamer in a batch buffer for 3D and GPGPU workloads. MI_BATCH_BUFFER_START (Resource Streamer Enabled) PIPELINE_SELECT (3D) 3DSTATE_BINDING_TABLE_POOL_ALLOC (Binding Table Pool Enabled) 3D WORKLAOD MI_RS_CONTROL (Disable Resource Streamer) 3DSTATE_BINDING_TABLE_POOL_ALLOC (Binding Table Pool Disabled) PIPELINE_SELECT (GPGPU) GPGPU Workload 3DSTATE_BINDING_TABLE_POOL_ALLOC (Binding Table Pool Enabled) MI_RS_CONTROL (Enable Resource Streamer) 3D WORKLOAD MI_BATCH_BUFFER_END	
Render command streamer (RCS) does Fixed Function DOP CG for media and gpgpu workloads. During context restore 3D semi pipeline state is restored to WM, which triggers implicit flush. Theoretically under certain conditions RCS can trigger FFDOP CG while WM in doing implicit flush leading to hangs. Only way to work around this issue is by disabling FFDOP CG feature. This issue is being fixed on G0 stepping.	

## PIPELINE\_SELECT

So far this issue is not yet hit in pre-silicon validation, emulation, Silicon-SV or Silicon-Driver being a rare condition. Work around to disable FFDOP CG is not being applied at this point to allow validation to make progress on FFDOP CG feature, further decision will be taken when this issue occurs. Validation teams are requested to triage any GPGPU workload hangs with WM no done with FFDOP CG disabled to eliminate this scenario.

DWord	Bit	Description												
0	31:29	<b>Command Type</b>												
		Default Value:	3h GFXPIPE											
		Format:	OpCode											
	28:27	<b>Command SubType</b>												
		Default Value:	1h GFXPIPE_SINGLE_DW											
		Format:	OpCode											
	26:24	<b>3D Command Opcode</b>												
		Format:	OpCode											
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>1h</td> <td>GFXPIPE_NONPIPELINED [Default]</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Value	Name	Project	1h	GFXPIPE_NONPIPELINED [Default]	CHV, BSW						
	Value	Name	Project											
1h	GFXPIPE_NONPIPELINED [Default]	CHV, BSW												
23:16	<b>3D Command Sub Opcode</b>													
	Default Value:	04h GFXPIPE												
	Format:	OpCode												
6	<b>Reserved</b>	Project: CHV, BSW												
15:2	<b>Reserved</b>	Project: CHV, BSW												
1:0	<b>Pipeline Selection</b>	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>3D</td> <td>3D pipeline is selected</td> </tr> <tr> <td>1</td> <td>Media</td> <td>Media pipeline is selected (Includes HD optical disc playback, HD video playback, and generic media workloads)</td> </tr> <tr> <td>2</td> <td>GPGPU</td> <td>GPGPU pipeline is selected</td> </tr> </tbody> </table>	Value	Name	Description	0	3D	3D pipeline is selected	1	Media	Media pipeline is selected (Includes HD optical disc playback, HD video playback, and generic media workloads)	2	GPGPU	GPGPU pipeline is selected
		Value	Name	Description										
		0	3D	3D pipeline is selected										
		1	Media	Media pipeline is selected (Includes HD optical disc playback, HD video playback, and generic media workloads)										
2	GPGPU	GPGPU pipeline is selected												

## Plane

<b>pln - Plane</b>	
Project:	CHV, BSW
Source:	Eulsa
Length Bias:	4
<p>The pln instruction computes a component-wise plane equation (<math>w = p*u+q*v+r</math> where <math>u/v/w</math> are vectors and <math>p/q/r</math> are scalars) of src0 and src1 and stores the results in dst. src1 is the input vector u. src0 provides input scalars p, q, and r, where p is the scalar value based on the region description of src0 and q and r are the scalar values implied from the src0 region. Specifically, q is the second component and r is the fourth component of the 4-tuple (128-bit aligned) that p belongs to.</p>	
Format: [(pred)] pln[.cmod] (exec_size) dst src0 src1	
Restriction	Project
This is a specialized instruction that only supports an execution size (ExecSize) of 8 or 16.	
The src0 region must be a replicated scalar (with HorzStride == VertStride == 0).	
src0 must specify .0 or .4 as the subregister number, corresponding to a subregister byte offset of 0 or 16.	
Source operands cannot be accumulators.	CHV, BSW
Syntax	
[(pred)] pln[.cmod] (exec_size) reg reg reg	
Pseudocode	
<pre> Evaluate (WrEn); for ( n = 0; n &lt; exec_size; n++ ) {     float dwP = src0.RegNum.SubRegNum[bits4:2];           // A DWord-aligned scalar.     float dwQ = src0.RegNum.(SubRegNum[bit4:2]   0x1);    // Second component.     float dwR = src0.RegNum.(SubRegNum[bit4:2]   0x3);    // Fourth component.     if ( ExecSize == 8 ) {         u = src1.RegNum         v = src1.(RegNum + 1)     } else {         if ( n &lt; 8 ) {             u = src1.RegNum             v = src1.(RegNum + 1)         } else {             u = src1.(RegNum + 2)             v = src1.(RegNum + 3)         }     }      if ( WrEn.chan[n] ) {         dst.chan[n] = dwP * u.chan[n] + dwQ * v.chan[n] + dwR;     } }                 </pre>	

<b>pln - Plane</b>			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	Y	Y	N
Src Types	Dst Types		
F	F		
DWord	Bit	Description	
0..3	127:64	<b>RegSource</b>	
		Exists If:	(([RegSource][Src1.RegFile]!='IMM')
	Format:	EU_INSTRUCTION_SOURCES_REG_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>	
Exists If:		(([ImmSource][Src1.RegFile]='IMM')	
Format:	EU_INSTRUCTION_SOURCES_REG_IMM [CHV, BSW]		
63:32	<b>Operand Controls</b>		
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]	
31:0	<b>Header</b>		
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]	

## REP16 Render Target Write MSD

MSD_RTW_REP16 - REP16 Render Target Write MSD			
Project:	CHV, BSW		
Source:	Render Cache DataPort		
Length Bias:	1		
Family:	Other		
Group:	Render Target R/W		
DWord	Bit	Description	
0	31	<b>Reserved</b>	
		Project: All	
		Format: MBZ	
			Ignored
	30	<b>Message Precision Subtype</b>	
		Default Value:	0h
		Project:	All
		Format:	Opcode
			Full precision data message
	29	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
		Ignored	
28:25	<b>Message Length</b>		
	Project:	All	
		Format: U4	
		Specifies the number of 256-bit GRF registers sent as the message payload (including the header). Valid value ranges are 1 to 15.	
24:20	<b>Response Length</b>		
	Project:	All	
	Format:	U5	
		Specifies the number of 256-bit GRF registers expected as the message response payload. Valid value ranges are 0 to 16.	
19	<b>Header Present</b>		
	Project:	All	
	Format:	MDC_MHP [CHV, BSW]	
		If set, indicates that the message includes the 2-register header.	

## MSD\_RTW\_REP16 - REP16 Render Target Write MSD

18	<b>Reserved</b>	
17:14	<b>Message Type</b>	
	Default Value:	0Ch
	Project:	All
	Format:	Opcode
	Render Target Write message	
13	<b>Reserved</b>	
12	<b>Last Render Target Select</b>	
	Project:	All
	Format:	Enable
	<p>This bit must be set on the last render target write message sent for each group of pixels. For single render target pixel shaders, this bit is set on all render target write messages. For multiple render target pixel shaders, this bit is set only on messages sent to the last render target. This bit must be zero for SIMD8 Image Write message. In general, when threads are not launched by 3D FF, this bit must be zero.</p>	
	<b>Programming Notes</b>	
	<p>When a pixel shader has render target writes at finer granularity than the dispatch rate, last render target write to a null surface must be present at the dispatch rate with this bit set. In particular, if a kernel is dispatched at pixel rate and it only writes to render targets at sample-rate, it must include a pixel-rate render target write to a null surface with Last Render Target Select bit enabled.</p>	
11	<b>Slot Group Select</b>	
	Project:	All
	Format:	MDC_RT_SGS [CHV, BSW]
	This field selects whether slots 15:0 or slots 31:16 are used for bypassed data.	
10:8	<b>Render Target Message Subtype</b>	
	Default Value:	1h
	Project:	All
	Format:	Opcode
	SIMD16 Single source message with replicated data. Use slots [15:0] for pixel enables, X/Y addresses, and oMask.	
	<b>Programming Notes</b>	
	The above slots indicated are within the 16 slots selected by Slot Group Select. If SLOTGRP_HI is selected, slots [31:16] are referenced instead of [15:0].	
7:0	<b>Binding Table Index</b>	
	Project:	All
	Format:	MDC_BTS [CHV, BSW]
	Specifies the Binding Table Index for the message	

## Return

<b>ret - Return</b>				
Project:	CHV, BSW			
Source:	Eulsa			
Length Bias:	4			
Description				
Return execution to the code sequence that called a subroutine. The ret instruction can be predicated or non-predicated. If non-predicated, all channels jump to the return IP in the first channel of src0 and restore CallMask from the second channel of src0. If predicated, the enabled channels jump to the return IP from the first channel of src0 and the corresponding bits in the CallMask are cleared to zero; if all CallMask bits are zero after the ret instruction, then execution jumps to the return IP from the first channel of src0. When SPF is on, the predication control must be scalar.				
Format: [(pred)] ret (exec_size) null src0				
Restriction				
This instruction cannot take accumulator as source.				
The src0 regioning control must be <2;2,1>				
Syntax				
[(pred)] ret (exec_size) null reg				
Pseudocode				
Evaluate(WrEn); for ( n = 0; n < exec_size; n++ ) { if ( WrEn.chan[n] ) { PclP[n] = src0.chan[0]; CallMask[n] = 0; } else { PclP[n] = IP + 1; } } for ( n = exec_size; n < 32; n++ ) { PclP[n] = IP + 1; } if ( CallMask[n:0] == 0 ) { // all channels are zero Jump(src0.chan[0]); CallMask = src0.chan[1]; }				
Predication	Conditional Modifier	Saturation	Source Modifier	Src Types
Y	N	N	N	D, UD
DWord	Bit	Description		
0..3	127:64	<b>RegSource</b>		
		Exists If:	([Operand Controls][Src0.RegFile]!='IMM')	
	Format:	EU_INSTRUCTION_SOURCES_REG [CHV, BSW]		
	127:64	<b>ImmSource</b>		
Exists If:		([Operand Controls][Src0.RegFile]='IMM')		
Format:	EU_INSTRUCTION_SOURCES_IMM32 [CHV, BSW]			
63:32	<b>Operand Controls</b>			
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]		
31:0	<b>Header</b>			
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]		

## Round Down

<b>rndd - Round Down</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
<p>The rndd instruction takes component-wise floating point downward rounding (to the integral float number closer to negative infinity) of src0 and storing the rounded integral float results in dst. This is commonly referred to as the floor() function. Each result follows the rules in the following tables based on the floating-point mode.</p>			
Format: [(pred)] rndd[.cmod] (exec_size) dst src0			
Syntax			
[(pred)] rndd[.cmod] (exec_size) reg reg [(pred)] rndd[.cmod] (exec_size) reg imm32			
Pseudocode			
Evaluate(WrEn); for ( n = 0; n < exec_size; n++ ) { if ( WrEn.chan[n] ) { dst.chan[n] = floor(src0.chan[n]); } }			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	Y	Y	Y
Src Types	Dst Types		
F	F		
DWord	Bit	Description	
0..3	127:64	<b>RegSource</b>	
		Exists If:	(([Operand Controls][Src0.RegFile]!='IMM')
	Format:	EU_INSTRUCTION_SOURCES_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>	
Exists If:		(([Operand Controls][Src0.RegFile]='IMM')	
Format:	EU_INSTRUCTION_SOURCES_IMM32 [CHV, BSW]		
63:32	<b>Operand Controls</b>		
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]	
31:0	<b>Header</b>		
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]	



## Round to Nearest or Even

<b>rnde - Round to Nearest or Even</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
<p>The rnde instruction takes component-wise floating point round-to-even operation of src0 with results in two pieces - a downward rounded integral float results stored in dst and the round-to-even increments stored in the rounding increment bits. The round-to-even increment must be added to the results in dst to create the final round-to-even values to emulate the round-to-even operation, commonly known as the round() function. The final results are the one of the two integral float values that is nearer to the input values. If the neither possibility is nearer, the even alternative is chosen. Each result follows the rules in the following tables based on the floating-point mode.</p>			
Format: [(pred)] rnde[.cmod] (exec_size) dst src0			
Syntax			
[(pred)] rnde[.cmod] (exec_size) reg reg [(pred)] rnde[.cmod] (exec_size) reg imm32			
Pseudocode			
<pre>Evaluate(WrEn); for ( n = 0; n &lt; exec_size; n++ ) { if ( WrEn.chan[n] ) { if ( src0.chan[n] - floor(src0.chan[n]) &gt; 0.5f ) { dst.chan[n] = floor(src0.chan[n]) + 1; } else if ( src0.chan[n] - floor(src0.chan[n]) &lt; 0.5f ) { dst.chan[n] = floor(src0.chan[n]); } else { if ( floor(src0.chan[n]) is odd ) { dst.chan[n] = floor(src0.chan[n]) + 1; } else { dst.chan[n] = floor(src0.chan[n]); } } }</pre>			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	Y	Y	Y
Src Types	Dst Types		
F	F		
DWord	Bit	Description	
0..3	127:64	<b>RegSource</b>	
		Exists If:	(([Operand Controls][Src0.RegFile]!='IMM')
	Format:	EU_INSTRUCTION_SOURCES_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>	
Exists If:		(([Operand Controls][Src0.RegFile]='IMM')	
Format:	EU_INSTRUCTION_SOURCES_IMM32 [CHV, BSW]		
63:32	<b>Operand Controls</b>		
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]	
31:0	<b>Header</b>		
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]	

## Round to Zero

<b>rndz - Round to Zero</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
<p>The rndz instruction takes component-wise floating point round-to-zero operation of src0 with results in two pieces - a downward rounded integral float results stored in dst and the round-to-zero increments stored in the rounding increment bits. The round-to-zero increment must be added to the results in dst to create the final round-to-zero values to emulate the round-to-zero operation, commonly known as the truncate() function. The final results are the one of the two closest integral float values to the input values that is nearer to zero.</p>			
Format: [(pred)] rndz[.cmod] (exec_size) dst src0			
Syntax			
[(pred)] rndz[.cmod] (exec_size) reg reg [(pred)] rndz[.cmod] (exec_size) reg imm32			
Pseudocode			
Evaluate(WrEn); for ( n = 0; n < exec_size; n++ ) { if ( WrEn.chan[n] ) { dst.chan[n] = floor(src0.chan[n]); if ( abs(src0.chan[n]) < abs(dst.chan[n]) ) { dst.chan[n] = floor(src0.chan[n]) + 1; } else { dst.chan[n] = floor(src0.chan[n]); } } }			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	Y	Y	Y
Src Types	Dst Types		
F	F		
DWord	Bit	Description	
0..3	127:64	<b>RegSource</b>	
		Exists If:	(([Operand Controls][Src0.RegFile]!='IMM')
	Format:	EU_INSTRUCTION_SOURCES_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>	
Exists If:		(([Operand Controls][Src0.RegFile]=='IMM')	
Format:	EU_INSTRUCTION_SOURCES_IMM32 [CHV, BSW]		
63:32	<b>Operand Controls</b>		
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]	
31:0	<b>Header</b>		
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]	

## Round Up

<b>rndu - Round Up</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
<p>The rndu instruction takes component-wise floating point upward rounding (to the integral float number closer to positive infinity) of src0, commonly known as the ceiling() function. Each result follows the rules in the following tables based on the floating-point mode.</p>			
Format: [(pred)] rndu[.cmod] (exec_size) dst src0			
Syntax			
[(pred)] rndu[.cmod] (exec_size) reg reg [(pred)] rndu[.cmod] (exec_size) reg imm32			
Pseudocode			
<pre>Evaluate(WrEn); for ( n = 0; n &lt; exec_size; n++ ) { if ( WrEn.chan[n] ) { if ( src0.chan[n] - floor(src0.chan[n]) &gt; 0.0f ) { dst.chan[n] = floor(src0.chan[n]) + 1; } else { dst.chan[n] = src0.chan[n]; } } }</pre>			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	Y	Y	Y
Src Types	Dst Types		
F	F		
DWord	Bit	Description	
0..3	127:64	<b>RegSource</b>	
		Exists If:	(([Operand Controls][Src0.RegFile]!='IMM')
	Format:	EU_INSTRUCTION_SOURCES_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>	
Exists If:		(([Operand Controls][Src0.RegFile]='IMM')	
Format:	EU_INSTRUCTION_SOURCES_IMM32 [CHV, BSW]		
63:32	<b>Operand Controls</b>		
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]	
31:0	<b>Header</b>		
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]	

## Scattered Move

<b>smov - Scattered Move</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
<p>The smov instruction moves the components in src0 into dst. For each enabled channel, copy src0 to dst. The immediate is used to selectively enable channels without using flags. When predication is enabled, the predicate mask is not generated from the flags. Instead, the immediate is used to mask the execution mask. If any channel is enabled as a result of this masking, the instruction is executed. When predication is not enabled, the immediate masks the execution mask. This provides flexibility to mask out any channel with an immediate.</p>			
Format: [(pred)] smov[.cmod] (exec_size) dst src0 src1			
Programming Notes			
When predication is disabled, the immediate provides the flexibility to perform a select operation without the use of flags.			
When predication is enabled, the usage model provides flexibility to select any bit in the flag registers for predication for execution size of 1.			
Syntax			
[(pred)] smov[.cmod] (exec_size) reg reg imm32			
Pseudocode			
if pred emask = OR (emask AND imm32) Else pmask = imm32. Evaluate(WrEn); for ( n = 0; n < 32; n++ ) { if ( WrEn.chan[n] ) { dst.chan[n] = src0.chan[n]; } }			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	N	N	N
DWord	Bit	Description	
0..3	127:64	<b>RegSource</b>	
		Exists If:	(([RegSource][Src1.RegFile]!='IMM')
	Format:	EU_INSTRUCTION_SOURCES_REG_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>	
Exists If:		([ImmSource][Src1.RegFile]='IMM')	
Format:	EU_INSTRUCTION_SOURCES_REG_IMM [CHV, BSW]		
63:32	<b>Operand Controls</b>		
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]	
31:0	<b>Header</b>		
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]	

## Scratch Block Read MSD

MSD0R_HWB - Scratch Block Read MSD							
Project:	CHV, BSW						
Source:	DataPort 0						
Length Bias:	1						
Family:	Block R/W						
Group:	HW Block R/W						
DWord	Bit	Description					
0	19	<b>Header Present</b>					
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_MHR [CHV, BSW]</td> </tr> </table> <p>Indicates that the message requires a header.</p>	Project:	All	Format:	MDC_MHR [CHV, BSW]	
	Project:	All					
	Format:	MDC_MHR [CHV, BSW]					
	18	<b>Scratch Block Message</b>					
<table border="1"> <tr> <td>Default Value:</td> <td>1h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Scratch Block Message</p>		Default Value:	1h	Project:	All	Format:	Opcode
Default Value:		1h					
Project:	All						
Format:	Opcode						
<table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Scratch Block Read message</p>	Default Value:	0h	Project:	All	Format:	Opcode	
Default Value:	0h						
Project:	All						
Format:	Opcode						
16	<b>Channel Mode</b>						
	<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MDC_CMODE [CHV, BSW]</td> </tr> </table> <p>Specifies whether the read or write operation occurs on all 4 Dwords if any of those channel enables are set, or else only on the dwords whose corresponding channel enable is set.</p>	Project:	CHV, BSW	Format:	MDC_CMODE [CHV, BSW]		
Project:	CHV, BSW						
Format:	MDC_CMODE [CHV, BSW]						
15	<b>Invalidate After Read</b>						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_IAR [CHV, BSW]</td> </tr> </table> <p>Specifies if L3 cache lines accessed by the message should be invalidated after the read occurs</p>	Project:	All	Format:	MDC_IAR [CHV, BSW]		
Project:	All						
Format:	MDC_IAR [CHV, BSW]						
14	<b>Reserved</b>						

<b>MSD0R_HWB - Scratch Block Read MSD</b>					
13:12	<p><b>Data Elements</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_DB_HW [CHV, BSW]</td> </tr> </table> <p>Specifies the number of registers to be read or written</p>	Project:	All	Format:	MDC_DB_HW [CHV, BSW]
	Project:	All			
Format:	MDC_DB_HW [CHV, BSW]				
11:0	<p><b>Address Offset</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>GeneralStateOffset[17:6]</td> </tr> </table> <p>DWORD (32 byte) based address offset to the BufferAddress in the Message Header.</p>	Project:	All	Format:	GeneralStateOffset[17:6]
	Project:	All			
Format:	GeneralStateOffset[17:6]				

## Scratch Block Write MSD

<b>MSD0W_HWB - Scratch Block Write MSD</b>								
Project:	CHV, BSW							
Source:	DataPort 0							
Length Bias:	1							
Family:	Block R/W							
Group:	HW Block R/W							
DWord	Bit	Description						
0	19	<b>Header Present</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_MHR [CHV, BSW]</td> </tr> </table> <p>Indicates that the message requires a header.</p>	Project:	All	Format:	MDC_MHR [CHV, BSW]		
	Project:	All						
	Format:	MDC_MHR [CHV, BSW]						
	18	<b>Scratch Block Message</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td>1h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Scratch Block Message</p>	Default Value:	1h	Project:	All	Format:	Opcode
	Default Value:	1h						
	Project:	All						
	Format:	Opcode						
	17	<b>Operation Type</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td>1h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Scratch Block Write message</p>	Default Value:	1h	Project:	All	Format:	Opcode
	Default Value:	1h						
	Project:	All						
Format:	Opcode							
16	<b>Channel Mode</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MDC_CMODE [CHV, BSW]</td> </tr> </table> <p>Specifies whether the read or write operation occurs on all 4 Dwords if any of those channel enables are set, or else only on the dwords whose corresponding channel enable is set.</p>	Project:	CHV, BSW	Format:	MDC_CMODE [CHV, BSW]			
Project:	CHV, BSW							
Format:	MDC_CMODE [CHV, BSW]							
15:14	<b>Reserved</b>							
13:12	<b>Data Elements</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_DB_HW [CHV, BSW]</td> </tr> </table> <p>Specifies the number of registers to be read or written</p>	Project:	All	Format:	MDC_DB_HW [CHV, BSW]			
Project:	All							
Format:	MDC_DB_HW [CHV, BSW]							
11:0	<b>Address Offset</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>GeneralStateOffset[17:6]</td> </tr> </table> <p>WORD (32 byte) based address offset to the BufferAddress in the Message Header.</p>	Project:	All	Format:	GeneralStateOffset[17:6]			
Project:	All							
Format:	GeneralStateOffset[17:6]							

## Select

<b>sel - Select</b>	
Project:	CHV, BSW
Source:	Eulsa
Length Bias:	4
<b>Description</b>	
<p>The sel instruction selectively moves the components in src0 or src1 into the channels of dst based on the predication. On a channel by channel basis, if the channel condition is true, data in src0 is moved into dst. Otherwise, data in src1 is moved into dst.</p> <p>As the predication is used to select the two sources, it is not included in the evaluation of WrEn. The predicate clause is mandatory if cmod is omitted/0000b. If both predication and the conditional modifier are omitted, the results are undefined.</p> <p>If the conditional modifier is specified (not 0000b, a compare is performed and the resulting condition flag is used for the sel instruction. Conditional modifiers .ge and .l follow the cmpn rules, and all other conditional modifiers follow the cmp rules. Predication is not allowed in this mode.</p> <p>A sel instruction with cmod .l is used to emulate a MIN instruction.</p> <p>A sel instruction with cmod .ge is used to emulate a MAX instruction.</p> <p>For a sel instruction with a .l or .ge conditional modifier, if one source is NaN and the other not NaN, the non-NaN source is the result. If both sources are NaNs, the result is NaN. For all other conditional modifiers, if either source is NaN then src1 is selected.</p> <p>A sel instruction without a conditional modifier always copies a denorm source value to a denorm destination value (in the manner of a raw move). This applies even if the source modifies are set on the sel instruction sources.</p> <p>The sel instruction uses any conditional modifier internally and does not update the flag register if a conditional modifier is used.</p> <p>A sel instruction with cmod or source modifier will flush denorm to zero, depending on the denorm mode bit; a sel instruction without cmod and source modifier will retain denorm.</p>	
Format: (pred) sel[.cmod] (exec_size) dst src0 src1	
<b>Restriction</b>	
Predicated sel instruction cannot be used in mixed mode operation with packed half float destination.	
<b>Syntax</b>	
(pred) sel[.cmod] (exec_size) reg reg reg (pred) sel[.cmod] (exec_size) reg reg imm32	
<b>Pseudocode</b>	
<pre>Evaluate(WrEn, NoPMask); if (cmod == "0000") { // no CMod Evaluate(PMask); for ( n = 0; n &lt; exec_size; n++ ) { if ( WrEn.chan[n] ) { if ( PMask.channel[n] ) { dst.chan[n] = src0.chan[n]; } else { dst.chan[n] = src1.chan[n]; } } } else { // with CMod Evaluate(CMod); for ( n = 0; n &lt; exec_size; n++ ) { if ( WrEn.chan[n] ) { if ( CMod.chan[n] ) { dst.chan[n] = src0.chan[n]; } else { dst.chan[n] = src1.chan[n]; } } } }</pre>	



## sel - Select

Predication	Conditional Modifier	Saturation	Source Modifier
Y	Y	Y	Y

  

Src Types	Dst Types	Project
*B,*W*D	*B,*W,*D	
F	F	
DF	DF	CHV, BSW
*W,*D,*Q	*W,*D,*Q	CHV, BSW
HF	HF	CHV, BSW
HF, F	HF, F	CHV, BSW

  

DWord	Bit	Description				
0..3	127:64	<b>RegSource</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 15%;">Exists If:</td> <td>([RegSource][Src1.RegFile]!='IMM')</td> </tr> <tr> <td>Format:</td> <td>EU_INSTRUCTION_SOURCES_REG_REG [CHV, BSW]</td> </tr> </table>	Exists If:	([RegSource][Src1.RegFile]!='IMM')	Format:	EU_INSTRUCTION_SOURCES_REG_REG [CHV, BSW]
	Exists If:	([RegSource][Src1.RegFile]!='IMM')				
	Format:	EU_INSTRUCTION_SOURCES_REG_REG [CHV, BSW]				
	127:64	<b>ImmSource</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 15%;">Exists If:</td> <td>([ImmSource][Src1.RegFile]=='IMM')</td> </tr> <tr> <td>Format:</td> <td>EU_INSTRUCTION_SOURCES_REG_IMM [CHV, BSW]</td> </tr> </table>	Exists If:	([ImmSource][Src1.RegFile]=='IMM')	Format:	EU_INSTRUCTION_SOURCES_REG_IMM [CHV, BSW]
Exists If:	([ImmSource][Src1.RegFile]=='IMM')					
Format:	EU_INSTRUCTION_SOURCES_REG_IMM [CHV, BSW]					
63:32	<b>Operand Controls</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 15%;">Format:</td> <td>EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]</td> </tr> </table>	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]			
Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]					
31:0	<b>Header</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 15%;">Format:</td> <td>EU_INSTRUCTION_HEADER [CHV, BSW]</td> </tr> </table>	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]			
Format:	EU_INSTRUCTION_HEADER [CHV, BSW]					

## Shift Left

<b>shl - Shift Left</b>						
Project:		CHV, BSW				
Source:		Eulsa				
Length Bias:		4				
Description						
<p>Perform component-wise logical left shift of the bits in src0 by the shift count indicated in src1, storing the results in dst, inserting zero bits in the number of LSBs indicated by the shift count. Hardware detects overflow properly and uses it to perform any saturation operation on the result, as long as the shifted result is within 33 bits. Otherwise, the result is undefined. Note: For word and DWord operands, the accumulators have 33 bits.</p> <p>In QWord mode, the shift count is taken from the low six bits of src1 regardless of the src1 type and treated as an unsigned integer in the range 0 to 63. Otherwise the shift count is taken from the low five bits of src1 regardless of the src1 type and treated as an unsigned integer in the range 0 to 31. The operation uses QWord mode if src0 or dst has the Q or UQ type but not if src1 is the only operand with the Q or UQ type.</p> <p>Format: [(pred)] shl[.cmod] (exec_size) dst src0 src1</p>						
Restriction						
Accumulator cannot be destination, implicit or explicit.						
Syntax						
[(pred)] shl[.cmod] (exec_size) reg reg reg [(pred)] shl[.cmod] (exec_size) reg reg imm32						
Pseudocode						
<pre>Evaluate(WrEn); for ( n = 0; n &lt; exec_size; n++ ) { if ( WrEn.chan[n] ) { shiftCnt = src0 or dst has Q or UQ type ? src1.chan[n] &amp; 0x3F : src1.chan[n] &amp; 0x1F dst.chan[n] = src0.chan[n] &lt;&lt; shiftCnt; } }</pre>						
Predication	Conditional Modifier	Saturation	Source Modifier	Src Types	Dst Types	
Y	Y	Y	Y	*B,*W,*D	*B,*W,*D	
DWord	Bit	Description				
0..3	127:64	<b>RegSource</b>				
		Exists If:	([RegSource][Src1.RegFile]!='IMM')			
	Format:	EU_INSTRUCTION_SOURCES_REG_REG [CHV, BSW]				
	127:64	<b>ImmSource</b>				
Exists If:		([ImmSource][Src1.RegFile]='IMM')				
Format:	EU_INSTRUCTION_SOURCES_REG_IMM [CHV, BSW]					
63:32	<b>Operand Controls</b>					
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]				
31:0	<b>Header</b>					
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]				

## Shift Right

<b>shr - Shift Right</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
Description			
<p>Perform component-wise logical right shift with zero insertion of the bits in src0 by the shift count indicated in src1, storing the results in dst. Insert zero bits in the number of MSBs indicated by the shift count. src0 and dst can have different types and can be signed or unsigned. Note: For word and DWord operands, the accumulators have 33 bits. Note: For unsigned src0 types, shr and asr produce the same result.</p> <p>In QWord mode, the shift count is taken from the low six bits of src1 regardless of the src1 type and treated as an unsigned integer in the range 0 to 63. Otherwise the shift count is taken from the low five bits of src1 regardless of the src1 type and treated as an unsigned integer in the range 0 to 31. The operation uses QWord mode if src0 or dst has the Q or UQ type but not if src1 is the only operand with the Q or UQ type.</p> <p>Format: [(pred)] shr[.cmod] (exec_size) dst src0 src1</p>			
Syntax			
[(pred)] shr[.cmod] (exec_size) reg reg reg [(pred)] shr[.cmod] (exec_size) reg reg imm32			
Pseudocode			
Evaluate(WrEn); for ( n = 0; n < exec_size; n++ ) { if ( WrEn.chan[n] ) { shiftCnt = src0 or dst has Q or UQ type ? src1.chan[n] & 0x3F : src1.chan[n] & 0x1F dst.chan[n] = src0.chan[n] » shiftCnt; } }	Project CHV, BSW		
Predication	Conditional Modifier	Saturation	Source Modifier
Y	Y	Y	Y
Src Types	Dst Types	Project	
UB, UW, UD	UB, UW, UD		
UW, UD, UQ	UW, UD, UQ	CHV, BSW	
DWord	Bit	Description	
0..3	127:64	<b>RegSource</b>	
		Exists If:	(([RegSource])[Src1.RegFile]!='IMM')
	Format:	EU_INSTRUCTION_SOURCES_REG_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>	
Exists If:		(([ImmSource])[Src1.RegFile]=='IMM')	
Format:	EU_INSTRUCTION_SOURCES_REG_IMM [CHV, BSW]		
63:32	<b>Operand Controls</b>		
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]	
31:0	<b>Header</b>		
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]	

## SIMD8 Render Target Write MSD

MSD_RTW_SIMD8 - SIMD8 Render Target Write MSD			
Project:	CHV, BSW		
Source:	Render Cache DataPort		
Length Bias:	1		
Family:	Other		
Group:	Render Target R/W		
DWord	Bit	Description	
0	31	<b>Reserved</b>	
	30	<b>Message Precision Subtype</b>	
		Default Value:	0h
		Project:	All
		Format:	Opcode
			Full precision data message
	29	<b>Reserved</b>	
	28:25	<b>Message Length</b>	
		Project:	All
		Format:	U4
		Specifies the number of 256-bit GRF registers sent as the message payload (including the header). Valid value ranges are 1 to 15.	
24:20	<b>Response Length</b>		
	Project:	All	
	Format:	U5	
		Specifies the number of 256-bit GRF registers expected as the message response payload. Valid value ranges are 0 to 16.	
19	<b>Header Present</b>		
	Project:	All	
	Format:	MDC_MHP [CHV, BSW]	
		If set, indicates that the message includes the 2-register header.	
18	<b>Reserved</b>		
17:14	<b>Message Type</b>		
	Default Value:	0Ch	
	Project:	All	
	Format:	Opcode	
		Render Target Write message	

<b>MSD_RTW_SIMD8 - SIMD8 Render Target Write MSD</b>	
13	<b>Reserved</b>
	Project: CHV, BSW
	Format: MBZ
	Ignored
12	<b>Last Render Target Select</b>
	Project: All
	Format: Enable
	<p>This bit must be set on the last render target write message sent for each group of pixels. For single render target pixel shaders, this bit is set on all render target write messages. For multiple render target pixel shaders, this bit is set only on messages sent to the last render target. This bit must be zero for SIMD8 Image Write message. In general, when threads are not launched by 3D FF, this bit must be zero.</p> <p style="text-align: center;"><b>Programming Notes</b></p> <p>When a pixel shader has render target writes at finer granularity than the dispatch rate, last render target write to a null surface must be present at the dispatch rate with this bit set. In particular, if a kernel is dispatched at pixel rate and it only writes to render targets at sample-rate, it must include a pixel-rate render target write to a null surface with Last Render Target Select bit enabled.</p>
11	<b>Slot Group Select</b>
	Project: All
	Format: MDC_RT_SGS [CHV, BSW]
This field selects whether slots 15:0 or slots 31:16 are used for bypassed data.	
10:8	<b>Render Target Message Subtype</b>
	Default Value: 4h
	Project: All
	Format: Opcode
	<p>SIMD8 single source message. Use slots [7:0] for pixel enables, X/Y addresses, and oMask.</p> <p style="text-align: center;"><b>Programming Notes</b></p> <p>The above slots indicated are within the 16 slots selected by Slot Group Select. If SLOTGRP_HI is selected, slots [23:16] are referenced instead of [7:0].</p>
7:0	<b>Binding Table Index</b>
	Project: All
	Format: MDC_BTS [CHV, BSW]
Specifies the Binding Table Index for the message	

## SIMD16 Render Target Write MSD

MSD_RTW_SIMD16 - SIMD16 Render Target Write MSD			
Project:	CHV, BSW		
Source:	Render Cache DataPort		
Length Bias:	1		
Family:	Other		
Group:	Render Target R/W		
DWord	Bit	Description	
0	31	<b>Reserved</b>	
	30	<b>Message Precision Subtype</b>	
		Default Value:	0h
		Project:	All
		Format:	Opcode
			Full precision data message
	29	<b>Reserved</b>	
	28:25	<b>Message Length</b>	
		Project:	All
		Format:	U4
		Specifies the number of 256-bit GRF registers sent as the message payload (including the header). Valid value ranges are 1 to 15.	
24:20	<b>Response Length</b>		
	Project:	All	
	Format:	U5	
		Specifies the number of 256-bit GRF registers expected as the message response payload. Valid value ranges are 0 to 16.	
19	<b>Header Present</b>		
	Project:	All	
	Format:	MDC_MHP [CHV, BSW]	
		If set, indicates that the message includes the 2-register header.	
18	<b>Reserved</b>		
17:14	<b>Message Type</b>		
	Default Value:	0Ch	
	Project:	All	
	Format:	Opcode	
		Render Target Write message	

## MSD\_RTW\_SIMD16 - SIMD16 Render Target Write MSD

13	<b>Reserved</b>		
	Project:	CHV, BSW	
	Format:	MBZ	
	Ignored		
12	<b>Last Render Target Select</b>		
	Project:	All	
	Format:	Enable	
	<p>This bit must be set on the last render target write message sent for each group of pixels. For single render target pixel shaders, this bit is set on all render target write messages. For multiple render target pixel shaders, this bit is set only on messages sent to the last render target. This bit must be zero for SIMD8 Image Write message. In general, when threads are not launched by 3D FF, this bit must be zero.</p>		
	<b>Programming Notes</b>		
	<p>When a pixel shader has render target writes at finer granularity than the dispatch rate, last render target write to a null surface must be present at the dispatch rate with this bit set. In particular, if a kernel is dispatched at pixel rate and it only writes to render targets at sample-rate, it must include a pixel-rate render target write to a null surface with Last Render Target Select bit enabled.</p>		
11	<b>Slot Group Select</b>		
	Project:	All	
	Format:	MDC_RT_SGS [CHV, BSW]	
	This field selects whether slots 15:0 or slots 31:16 are used for bypassed data.		
10:8	<b>Render Target Message Subtype</b>		
	Default Value:	0h	
	Project:	All	
	Format:	Opcode	
	SIMD16 Single source message. Use slots [15:0] for pixel enables, X/Y addresses, and oMask.		
	<b>Programming Notes</b>		
	The above slots indicated are within the 16 slots selected by Slot Group Select. If SLOTGRP_HI is selected, slots [31:16] are referenced instead of [15:0].		
7:0	<b>Binding Table Index</b>		
	Project:	All	
	Format:	MDC_BTS [CHV, BSW]	
	Specifies the Binding Table Index for the message		

## STATE\_BASE\_ADDRESS

<b>STATE_BASE_ADDRESS</b>		
Project:	CHV, BSW	
Source:	PRM	
Length Bias:	2	
<p>The STATE_BASE_ADDRESS command sets the base pointers for subsequent state, instruction, and media indirect object accesses by the GPE.</p> <p>For more information see the Base Address Utilization table in the Memory Access Indirection narrative topic.</p>		
Programming Notes		
<p>The following commands must be reissued following any change to the base addresses:</p> <ul style="list-style-type: none"> <li>• 3DSTATE_CC_POINTERS</li> <li>• 3DSTATE_BINDING_TABLE_POINTERS</li> <li>• 3DSTATE_SAMPLER_STATE_POINTERS</li> <li>• 3DSTATE_VIEWPORT_STATE_POINTERS</li> <li>• MEDIA_STATE_POINTERS</li> </ul> <p>Execution of this command causes a full pipeline flush, thus its use should be minimized for higher performance.</p>		
<p>SW must always program PIPE_CONTROL with "CS Stall" and "Render Target Cache Flush Enable" set before programming STATE_BASE_ADDRESS command for GPGPU workloads i.e when pipeline select is GPGPU via PIPELINE_SELECT command. This is required to achieve better GPGPU preemption latencies in certain workload programming sequences. If programming PIPE_CONTROL has performance implications then preemption latencies can be traded off against performance by not implementing this programming note.</p>		
Project		
CHV, BSW		
DWord	Bit	Description
0	31:29	<b>Command Type</b> Default Value: 3h GFXPIPE
	28:27	<b>Command SubType</b> Default Value: 0h GFXPIPE_COMMON
	26:24	<b>3D Command Opcode</b> Default Value: 1h GFXPIPE_NONPIPELINED
	23:16	<b>3D Command Sub Opcode</b> Default Value: 01h STATE_BASE_ADDRESS
	15:8	<b>Reserved</b> Project: All Format: MBZ



<b>STATE_BASE_ADDRESS</b>				
	7:0	<b>DWord Length</b>		
		Project:	CHV, BSW	
		Format:	=n Total Length - 2	
		<b>Value</b>	<b>Name</b>	<b>Description</b>
		Eh	DWORD_COUNT_n <b>[Default]</b>	Excludes DWord (0,1)
1..2	63:12	<b>General State Base Address</b>		
		Project:	All	
		Format:	GraphicsAddress[63:12]	
		Specifies the 4K-byte aligned base address for general state accesses. GraphicsAddress [63:48] are ignored by the HW and assumed to be in correct canonical form [63:48] == [47].		
		<b>Programming Notes</b>		
		Bounds checking is performed on general state accesses by Data Port Shared Functions for stateless A32 messages. Bounds checking is enabled when General State Base Address [46:12] + General State Buffer Size [31:12] is $\leq 2^{47}$ . This ensures that the General State Buffer does not straddle the canonical address boundary where GraphicsAddress [47] changes.		
		<b>Restriction</b>		
		General State Base Address [47:12] + General State Buffer Size [31:12] must be $< 2^{48}$ . It is illegal programming for this to be $\geq 2^{48}$ .		
		When using stateless (A32) Data Port messages, General State Base Address [47:12] + Buffer Base Address [31:0] must be $< 2^{48}$ . It is illegal for this to be $\geq 2^{48}$ .		
		11	<b>Reserved</b>	
Project:	All			
Format:	MBZ			
10:4	<b>General State Memory Object Control State</b>			
	Project:	All		
	Format:	MEMORY_OBJECT_CONTROL_STATE		
Specifies the memory object control state for indirect state using the <b>General State Base Address</b> , with the exception of the stateless data port accesses.				
3:1	<b>Reserved</b>			
0	<b>General State Base Address Modify Enable</b>			
	Project:	All		
	Format:	Enable		
	The other fields in this DWord and the following DWord are updated only when this bit is set.			
	<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>
0h	Disable	Ignore the updated address.	All	
1h	Enable	Modify the address.	All	

<b>STATE_BASE_ADDRESS</b>				
3	31:23	<b>Reserved</b>		
		Project:	All	
	Format:	MBZ		
22:16	<b>Stateless Data Port Access Memory Object Control State</b>			
	Project:	All		
	Format:	MEMORY_OBJECT_CONTROL_STATE		
Specifies the memory object control state for stateless data port accesses.				
15:0	<b>Reserved</b>			
	Project:	All		
	Format:	MBZ		
4.5	63:12	<b>Surface State Base Address</b>		
		Project:	All	
	Format:	GraphicsAddress[63:12]		
	Specifies the 4K-byte aligned base address for binding table and surface state accesses. GraphicsAddress [63:48] are ignored by the HW and assumed to be in correct canonical form [63:48] == [47].			
	11	<b>Reserved</b>		
		Project:	All	
	Format:	MBZ		
	10:4	<b>Surface State Memory Object Control State</b>		
		Project:	All	
	Format:	MEMORY_OBJECT_CONTROL_STATE		
Specifies the memory object control state for indirect state using the <b>Surface State Base Address</b> .				
3:1	<b>Reserved</b>			
	Project:	All		
Format:	MBZ			
0	<b>Surface State Base Address Modify Enable</b>			
	Project:	All		
	Format:	Enable		
	The other fields in this DWord and the following DWord are updated only when this bit is set.			
	<b>Value</b>	<b>Name</b>	<b>Description</b>	
	0h	Disable	Ignore the updated address.	
	1h	Enable	Modify the address.	
			<b>Project</b>	
			All	
			All	

		<b>STATE_BASE_ADDRESS</b>	
		<b>Programming Notes</b>	
		Setting this bit to 1 in a batch buffer causes the resource streamer to stop; for performance reasons the SW should only place commands with this bit set in the ring buffer.	
		Before programming the Surface State Base Address, the RS must be disabled. Within a batch buffer where the RS is enabled, RS may be disabled thru a MI_RS_CONTROL command with Resource Streamer Control cleared prior to the STATE_BASE_ADDRESS with Surface State Base Address Modify Enable set and then re-enabled with another MI_RS_CONTROL with Resource Streamer Control set.	
6..7	63:12	<b>Dynamic State Base Address</b>	
		Project:	All
		Format:	GraphicsAddress[63:12]
		Specifies the 4K-byte aligned base address for sampler and viewport state accesses. GraphicsAddress [63:48] are ignored by the HW and assumed to be in correct canonical form [63:48] == [47].	
	11	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	10:4	<b>Dynamic State Memory Object Control State</b>	
		Project:	All
		Format:	MEMORY_OBJECT_CONTROL_STATE
		Specifies the memory object control state for indirect state using the <b>Dynamic State Base Address</b> . Push constants defined in 3DSTATE_CONSTANT_(VS   GS   PS) commands do not use this control state, although they can use the corresponding base address. The memory object control state for push constants is defined within the command.	
	3:1	<b>Reserved</b>	
		Project:	All
		Format:	MBZ
	0	<b>Dynamic State Base Address Modify Enable</b>	
		Project:	All
		Format:	Enable
		The other fields in this DWORD and the following DWORD are updated only when this bit is set.	
		<b>Value</b>	<b>Name</b>
		<b>Description</b>	<b>Project</b>
		0h	Disable
		Ignore the updated address.	All
		1h	Enable
		Modify the address.	All
8..9	63:12	<b>Indirect Object Base Address</b>	
		Project:	All
		Format:	GraphicsAddress[63:12]IndirectObject
		Specifies the 4K-byte aligned base address for indirect object load in MEDIA_OBJECT command.	

<b>STATE_BASE_ADDRESS</b>					
	11	<b>Reserved</b>			
		Project:	All		
		Format:	MBZ		
	10:4	<b>Indirect Object Memory Object Control State</b>			
		Project:	All		
		Format:	MEMORY_OBJECT_CONTROL_STATE		
	Specifies the memory object control state for indirect objects using the <b>Indirect Object Base Address</b> .				
	3:1	<b>Reserved</b>			
		Project:	All		
		Format:	MBZ		
	0	<b>Indirect Object Base Address Modify Enable</b>			
		Project:	All		
		Format:	Enable		
	The other fields in this DWord and the following DWord are updated only when this bit is set.				
		<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>
		0h	Disable	Ignore the updated address.	All
		1h	Enable	Modify the address.	All
	10..11	63:12	<b>Instruction Base Address</b>		
		Project:	All		
		Format:	GraphicsAddress[63:12]		
Specifies the 4K-byte aligned base address for all EU instruction accesses. GraphicsAddress[63:48] are ignored by the HW and assumed to be in correct canonical form [63:48] == [47].					
	11	<b>Reserved</b>			
		Project:	All		
		Format:	MBZ		
	10:4	<b>Instruction Memory Object Control State</b>			
		Project:	All		
		Format:	MEMORY_OBJECT_CONTROL_STATE		
	Specifies the memory object control state for EU instructions using the <b>Instruction Base Address</b> .				
	3:1	<b>Reserved</b>			
		Project:	All		
		Format:	MBZ		

		<b>STATE_BASE_ADDRESS</b>											
	0	<b>Instruction Base Address Modify Enable</b>											
		Project:	All										
		Format:	Enable										
		The other fields in this DWord and the following DWord are updated only when this bit is set.											
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Value	Name	Description	Project										
0h	Disable	Ignore the updated address.	All										
1h	Enable	Modify the address.	All										
12	31:12	<b>General State Buffer Size</b>											
		Project:	All										
		Format:	U20										
		FormatDesc											
		This field specifies the size of the buffer in 4K pages. Any access that straddles or goes past the end of the buffer returns 0. Note that BufferSize=0 indicates that there is no valid data in the buffer.											
		<table border="1"> <thead> <tr> <th>Workaround</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>When the General State Buffer Size is programmed to 0, SLM accesses are treated as out-of-bounds (should only apply to Stateless accesses). Workaround is to program the General State Buffer Size to a value &gt; 0.</td> <td>CHV, BSW</td> </tr> <tr> <td>If Per Thread Scratch Space Size bounds checking is enabled by GT_MODE[15], then General State Buffer Size must be set larger than the maximum Per Thread Scratch Space Size.</td> <td>CHV, BSW [CHV, BSW]</td> </tr> </tbody> </table>		Workaround	Project	When the General State Buffer Size is programmed to 0, SLM accesses are treated as out-of-bounds (should only apply to Stateless accesses). Workaround is to program the General State Buffer Size to a value > 0.	CHV, BSW	If Per Thread Scratch Space Size bounds checking is enabled by GT_MODE[15], then General State Buffer Size must be set larger than the maximum Per Thread Scratch Space Size.	CHV, BSW [CHV, BSW]				
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		<b>Reserved</b>											
0	<b>General State Buffer Size Modify Enable</b>												
	Project:	All											
	Format:	Enable											
	The bound in this DWord is updated only when this bit is set.												
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Value	Name	Description	Project										
0h	Disable	Ignore the updated bound.	All										
1h	Enable	Modify the updated bound.	All										
13	31:12	<b>Dynamic State Buffer Size</b>											
		Project:	All										
		Format:	U20										
		FormatDesc											
		This field specifies the size of the buffer in 4K pages. Any access that straddles or goes past the end of the buffer returns 0. Note that BufferSize=0 indicates that there is no valid data in the buffer.											

<b>STATE_BASE_ADDRESS</b>															
	11:1	<b>Reserved</b>													
	0	<b>Dynamic State Buffer Size Modify Enable</b>													
		Project:	All												
		Format:	Enable												
		FormatDesc													
		The bound in this DWord is updated only when this bit is set.													
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Value	Name	Description	Project												
0h	Disable	Ignore the updated bound.	All												
1h	Enable	Modify the updated bound.	All												
14	31:12	<b>Indirect Object Buffer Size</b>													
		Project:	All												
		Format:	U20												
		FormatDesc													
		This field specifies the size of the buffer in 4K pages. Any access that straddles or goes past the end of the buffer returns 0. Note that BufferSize=0 indicates that there is no valid data in the buffer.													
	11:1	<b>Reserved</b>													
	0	<b>Indirect Object Buffer Size Modify Enable</b>													
		Project:	All												
		Format:	Enable												
		FormatDesc													
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Value	Name	Description	Project												
0h	Disable	Ignore the updated bound.	All												
1h	Enable	Modify the updated bound.	All												
15	31:12	<b>Instruction Buffer Size</b>													
		Project:	All												
		Format:	U20												
		FormatDesc													
		This field specifies the size of the buffer in 4K pages. Any access that straddles or goes past the end of the buffer returns 0. Note that BufferSize=0 indicates that there is no valid data in the buffer.													
	11:1	<b>Reserved</b>													

<b>STATE_BASE_ADDRESS</b>				
0	<b>Instruction Buffer size Modify Enable</b>			
	Project:	All		
	Format:	Enable		
	FormatDesc			
	The bound in this DWord is updated only when this bit is set.			
	<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>
	0h	Disable	Ignore the updated bound.	All

## STATE\_PREFETCH

STATE_PREFETCH							
Project:	CHV, BSW						
Source:	PRM						
Length Bias:	2						
<p>(This command is provided strictly for performance optimization opportunities, and likely requires some experimentation to evaluate the overall impact of additional prefetching.)</p> <p>The STATE_PREFETCH command causes the GPE to attempt to prefetch a sequence of 64-byte cache lines into the GPE-internal cache ("L2 ISC") used to access EU kernel instructions and fixed/shared function indirect state data. While state descriptors, surface state, and sampler state are automatically prefetched by the GPE, this command may be used to prefetch data not automatically prefetched, such as: 3D viewport state; Media pipeline Interface Descriptors; EU kernel instructions.</p>							
Restriction		Project					
Restriction: Due to know HW issue this command doesn't achieve its intended purpose and must not be exercised/programmed by SW.		CHV, BSW					
DWord	Bit	Description					
0	31:29	<b>Command Type</b>					
		Default Value: 3h GFXPIPE					
	28:27	<b>Command SubType</b>					
		Default Value: 0h GFXPIPE_COMMON					
	26:24	<b>3D Command Opcode</b>					
		Default Value: 0h GFXPIPE_PIPELINED					
	23:16	<b>3D Command Sub Opcode</b>					
Default Value: 03h STATE_PREFETCH							
15:8	<b>Reserved</b>						
7:0	<b>DWord Length</b>	Project: All					
		Format: =n Total Length - 2					
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>DWORD_COUNT_n <b>[Default]</b></td> <td>Excludes DWord (0,1)</td> </tr> </tbody> </table>	Value	Name	Description	0h	DWORD_COUNT_n <b>[Default]</b>	Excludes DWord (0,1)
	Value	Name	Description				
0h	DWORD_COUNT_n <b>[Default]</b>	Excludes DWord (0,1)					
1	31:6	<b>Prefetch Pointer</b>					
		Project: All					
	Format: GraphicsAddress[31:6]						
Specifies the 64-byte aligned address to start the prefetch from. This pointer is an absolute virtual address, it is not relative to any base pointer.							
5:3	<b>Reserved</b>						



<b>STATE_PREFETCH</b>												
	2:0	<p><b>Prefetch Count</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U3-1 count of cache lines</td> </tr> </table> <p>Indicates the number of contiguous 64-byte cache lines that will be prefetched.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #e1eef6;"> <th style="width: 25%;">Value</th> <th style="width: 25%;">Name</th> <th style="width: 50%;">Description</th> </tr> </thead> <tbody> <tr> <td>[0,7]</td> <td></td> <td>indicating a count of [1,8]</td> </tr> </tbody> </table>	Project:	All	Format:	U3-1 count of cache lines	Value	Name	Description	[0,7]		indicating a count of [1,8]
Project:	All											
Format:	U3-1 count of cache lines											
Value	Name	Description										
[0,7]		indicating a count of [1,8]										

## STATE\_SIP

STATE_SIP			
Project:	All		
Source:	PRM		
Length Bias:	2		
The STATE_SIP command specifies the starting instruction location of the System Routine that is shared by all threads in execution.			
DWord	Bit	Description	
0	31:29	<b>Command Type</b>	
	Default Value:		3h GFXPIPE
	28:27	<b>Command SubType</b>	
	Default Value:		0h GFXPIPE_COMMON
	26:24	<b>3D Command Opcode</b>	
	Default Value:		1h GFXPIPE_NONPIPELINED
	23:16	<b>3D Command Sub Opcode</b>	
Default Value:		02h STATE_SIP	
15:8	<b>Reserved</b>		
	Project:	All	
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Project:	All	
	Format:	=n Total Length - 2	
	<b>Value</b>	<b>Name</b>	<b>Description</b>
1h	DWORD_COUNT_n <b>[Default]</b>	Excludes DWord (0,1)	CHV, BSW
1..2 <b>Project:</b> CHV, BSW	63:4	<b>System Instruction Pointer</b>	
		Project:	All
	Format:	InstructionBaseOffset[63:4]Kernel	
	Specifies the instruction address of the system routine associated with the current context as a 128-bit granular offset from the Instruction Base Address. SIP is shared by all threads in execution. The address specifies the double quadword aligned instruction location. GraphicsAddress [63:48] are ignored by the HW and assumed to be in correct canonical form [63:48] == [47].		
<b>Programming Notes</b>			
This portion of the command is not context save/restored. The context image may restore this command as a 2 dword command rather than a 3 dword command.			
	3:0	<b>Reserved</b>	

## Sum of Absolute Difference 2

<b>sad2 - Sum of Absolute Difference 2</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
<p>The sad2 instruction takes source data channels from src0 and src1 in groups of 2-tuples. For each 2-tuple, it computes the sum-of-absolute-difference (SAD) between src0 and src1 and stores the scalar result in the first channel of the 2-tuple in dst. The results are also stored in the accumulator register. The destination operand and the accumulator maintain 16 bits per channel precision. The destination register must be aligned to even word (DWord). The even words in the destination region will contain the correct data. The odd words are also written but with undefined values.</p>			
Format: [(pred)] sad2[.cmod] (exec_size) dst src0 src1			
Restriction			
Source operands cannot be accumulators.			
The execution size cannot be 1 as the computation requires at least two data channels.			
Syntax			
[(pred)] sad2[.cmod] (exec_size) reg reg reg [(pred)] sad2[.cmod] (exec_size) reg reg imm32			
Pseudocode			
Evaluate(WrEn); for ( n = 0; n < exec_size; n += 2 ) { if ( WrEn.chan[n] ) { dst.chan[n] = abs(src0.chan[n] - src1.chan[n]) + abs(src0.chan[n+1] - src1.chan[n+1]); } }			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	Y	Y	Y
Src Types	Dst Types		
B, UB	W, UW		
DWord	Bit	Description	
0..3	127:64	<b>RegSource</b>	
		Exists If:	([RegSource][Src1.RegFile]!='IMM')
	Format:	EU_INSTRUCTION_SOURCES_REG_REG [CHV, BSW]	
	127:64	<b>ImmSource</b>	
Exists If:		([ImmSource][Src1.RegFile]=='IMM')	
Format:	EU_INSTRUCTION_SOURCES_REG_IMM [CHV, BSW]		
63:32	<b>Operand Controls</b>		
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]	
31:0	<b>Header</b>		
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]	

## Sum of Absolute Difference Accumulate 2

<b>sada2 - Sum of Absolute Difference Accumulate 2</b>						
Project:	CHV, BSW					
Source:	Eulsa					
Length Bias:	4					
<p>The sada2 instruction takes source data channels from src0 and src1 in groups of 2-tuples. For each 2-tuple, it computes the sum-of-absolute-difference (SAD) between src0 and src1, adds the intermediate result with the accumulator value corresponding to the first channel, and stores the scalar result in the first channel of the 2-tuple in dst. The destination operand and the accumulator maintain 16 bits per channel precision. Higher precision (guide bits) stored in the accumulator allows up to 64 rounds of sada2 instructions to be issued back to back without overflowing the accumulator. The destination register must be aligned to even word (DWord). The even words in the destination region will contain the correct data. The odd words are also written but with undefined values.</p>						
Format: [(pred)] sada2[.cmod] (exec_size) dst src0 src1						
Restriction						
Source operands cannot be accumulators.						
The execution size cannot be 1 as the computation requires at least two data channels.						
Syntax						
[(pred)] sada2[.cmod] (exec_size) reg reg reg [(pred)] sada2[.cmod] (exec_size) reg reg imm32						
Pseudocode						
Evaluate(WrEn); for ( n = 0; n < exec_size; n += 2 ) { uwTmp = abs(src0.chan[n] - src1.chan[n]) + abs(src0.chan[n+1] - src1.chan[n+1]); if ( WrEn.chan[n] ) { dst.chan[n] = uwTmp + acc[n]; } }						
Predication	Conditional Modifier	Saturation	Source Modifier	Src Types	Dst Types	
Y	Y	Y	Y	B, UB	W, UW	
DWord	Bit	Description				
0..3	127:64	<b>RegSource</b>				
		Exists If:	([RegSource][Src1.RegFile]!='IMM')			
	Format:	EU_INSTRUCTION_SOURCES_REG_REG [CHV, BSW]				
	127:64	<b>ImmSource</b>				
Exists If:		([ImmSource][Src1.RegFile]='IMM')				
Format:	EU_INSTRUCTION_SOURCES_REG_IMM [CHV, BSW]					
63:32	<b>Operand Controls</b>					
	Format:	EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]				
31:0	<b>Header</b>					
	Format:	EU_INSTRUCTION_HEADER [CHV, BSW]				

## SWTESS\_BASE\_ADDRESS

<b>SWTESS_BASE_ADDRESS</b>						
Project:	CHV, BSW					
Source:	PRM					
Length Bias:	2					
<p>The SWTESS_BASE_ADDRESS command sets the base pointers for SW Tessellation data read access by the TE unit.</p>						
Programming Notes						
<p>This base address must also be comprehended in the SURFACE_STATE used by the HS kernel to write the SW tessellation data.</p> <p>Execution of this command causes a full pipeline flush, thus its use should be minimized for higher performance.</p>						
DWord	Bit	Description				
0	31:29	<b>Command Type</b> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>3h GFXPIPE</td> </tr> </table>	Default Value:	3h GFXPIPE		
	Default Value:	3h GFXPIPE				
	28:27	<b>Command SubType</b> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>0h GFXPIPE_COMMON</td> </tr> </table>	Default Value:	0h GFXPIPE_COMMON		
	Default Value:	0h GFXPIPE_COMMON				
	26:24	<b>3D Command Opcode</b> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>1h GFXPIPE_NONPIPELINED</td> </tr> </table>	Default Value:	1h GFXPIPE_NONPIPELINED		
	Default Value:	1h GFXPIPE_NONPIPELINED				
	23:16	<b>3D Command Sub Opcode</b> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>03h SWTESS_BASE_ADDRESS</td> </tr> </table>	Default Value:	03h SWTESS_BASE_ADDRESS		
Default Value:	03h SWTESS_BASE_ADDRESS					
15:8	<b>Reserved</b>					
7:0		<b>DWord Length</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>=n Total Length - 2</td> </tr> </table>	Project:	All	Format:	=n Total Length - 2
		Project:	All			
		Format:	=n Total Length - 2			
<table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>DWORD_COUNT_n [Default]</td> <td>Excludes DWord (0,1)</td> </tr> </tbody> </table>	Value	Name	Description	0h	DWORD_COUNT_n [Default]	Excludes DWord (0,1)
Value	Name	Description				
0h	DWORD_COUNT_n [Default]	Excludes DWord (0,1)				
1	31:12	<b>SW Tessellation Base Address</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[31:12]</td> </tr> </table> <p>Specifies the 4K-byte aligned base address for TE unit SW tessellation data read accesses.</p>	Project:	All	Format:	GraphicsAddress[31:12]
		Project:	All			
		Format:	GraphicsAddress[31:12]			
	11:8	<b>SW Tessellation Memory Object Control State</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MEMORY_OBJECT_CONTROL_STATE</td> </tr> </table> <p>Specifies the memory object control state used by the TE unit to read SW tessellation data from memory.</p>	Project:	All	Format:	MEMORY_OBJECT_CONTROL_STATE
Project:	All					
Format:	MEMORY_OBJECT_CONTROL_STATE					

<b>SWTESS_BASE_ADDRESS</b>			
	7:0	<b>Reserved</b>	
		Project: All	
		Format: MBZ	
2 <b>Project:</b> CHV, BSW	31:16	<b>Reserved</b>	
		Project: All	
		Format: MBZ	
	15:0	<b>SW Tessellation Base Address High</b>	
		Project: CHV, BSW	
		Format: GraphicsAddress[47:32]	
Specifies most significant bits of the 4K-byte aligned base address for TE unit SW tessellation data read accesses. See SW Tessellation Base Address[31:12] in DWord 0.			

## Typed Surface Read MSD

<b>MSD1R_TS - Typed Surface Read MSD</b>								
Project:	CHV, BSW							
Source:	DataPort 1							
Length Bias:	1							
Family:	Typed Surface R/W							
Group:	Scattered Typed Surface R/W							
DWord	Bit	Description						
0	19	<p><b>Header Present</b></p> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_MHP [CHV, BSW]</td> </tr> </table> <p>If set, indicates that the message includes the header.</p>	Project:	All	Format:	MDC_MHP [CHV, BSW]		
	Project:	All						
	Format:	MDC_MHP [CHV, BSW]						
	18:14	<p><b>Message Type</b></p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>05h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Typed Surface Read message</p>	Default Value:	05h	Project:	All	Format:	Opcode
	Default Value:	05h						
Project:	All							
Format:	Opcode							
13:12	<p><b>Slot Group</b></p> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_SG3 [CHV, BSW]</td> </tr> </table> <p>Specifies the Slot Group mode of the message (which slots are processed)</p>	Project:	All	Format:	MDC_SG3 [CHV, BSW]			
Project:	All							
Format:	MDC_SG3 [CHV, BSW]							
11:8	<p><b>Channel Mask</b></p> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_CMASK [CHV, BSW]</td> </tr> </table> <p>Specifies which RGBA channels are included in the message payload.</p>	Project:	All	Format:	MDC_CMASK [CHV, BSW]			
Project:	All							
Format:	MDC_CMASK [CHV, BSW]							
7:0	<p><b>Binding Table Index</b></p> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_BTS [CHV, BSW]</td> </tr> </table> <p>Specifies the Binding Table Index for the message</p>	Project:	All	Format:	MDC_BTS [CHV, BSW]			
Project:	All							
Format:	MDC_BTS [CHV, BSW]							

## Typed Surface Write MSD

MSD1W_TS - Typed Surface Write MSD		
Project:	CHV, BSW	
Source:	DataPort 1	
Length Bias:	1	
Family:	Typed Surface R/W	
Group:	Scattered Typed Surface R/W	
DWord	Bit	Description
0	19	<b>Header Present</b>
		Project: All
		Format: MDC_MHP [CHV, BSW]
	If set, indicates that the message includes the header.	
	18:14	<b>Message Type</b>
Default Value: 0Dh		
Project: All		
Format: Opcode		
Typed Surface Write message		
13:12	<b>Slot Group</b>	
	Project: All	
	Format: MDC_SG3 [CHV, BSW]	
Specifies the Slot Group mode of the message (which slots are processed)		
11:8	<b>Channel Mask</b>	
	Project: All	
	Format: MDC_CMASK [CHV, BSW]	
Specifies which RGBA channels are included in the message payload.		
7:0	<b>Binding Table Index</b>	
	Project: All	
	Format: MDC_BTS [CHV, BSW]	
Specifies the Binding Table Index for the message		



## Untyped Surface Read MSD

<b>MSD1R_US - Untyped Surface Read MSD</b>									
Project:	CHV, BSW								
Source:	DataPort 1								
Length Bias:	1								
Family:	Untyped Surface R/W								
Group:	Scattered Untyped Surface R/W								
DWord	Bit	Description							
0	19	<b>Header Present</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_MHP [CHV, BSW]</td> </tr> </table> If set, indicates that the message includes the header.	Project:	All	Format:	MDC_MHP [CHV, BSW]			
		Project:	All						
		Format:	MDC_MHP [CHV, BSW]						
		18:14	<b>Message Type</b> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>01h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> Untyped Surface Read message	Default Value:	01h	Project:	All	Format:	Opcode
			Default Value:	01h					
Project:	All								
Format:	Opcode								
13:12	<b>SIMD Mode</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_SM3 [CHV, BSW]</td> </tr> </table> Specifies the SIMD mode of the message (number of slots processed)	Project:	All	Format:	MDC_SM3 [CHV, BSW]				
	Project:	All							
Format:	MDC_SM3 [CHV, BSW]								
11:8	<b>Channel Mask</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_CMASK [CHV, BSW]</td> </tr> </table> Specifies which RGBA channels are included in the message payload.	Project:	All	Format:	MDC_CMASK [CHV, BSW]				
Project:	All								
Format:	MDC_CMASK [CHV, BSW]								
7:0	<b>Binding Table Index</b> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_BTS_SLM_A32 [CHV, BSW]</td> </tr> </table> Specifies the Binding Table Index for the message	Project:	All	Format:	MDC_BTS_SLM_A32 [CHV, BSW]				
	Project:	All							
Format:	MDC_BTS_SLM_A32 [CHV, BSW]								

## Untyped Surface Write MSD

<b>MSD1W_US - Untyped Surface Write MSD</b>								
Project:	CHV, BSW							
Source:	DataPort 1							
Length Bias:	1							
Family:	Untyped Surface R/W							
Group:	Scattered Untyped Surface R/W							
DWord	Bit	Description						
0	19	<p><b>Header Present</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_MHP [CHV, BSW]</td> </tr> </table> <p>If set, indicates that the message includes the header.</p>	Project:	All	Format:	MDC_MHP [CHV, BSW]		
	Project:	All						
	Format:	MDC_MHP [CHV, BSW]						
	18:14	<p><b>Message Type</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Default Value:</td> <td>09h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table> <p>Untyped Surface Write message</p>	Default Value:	09h	Project:	All	Format:	Opcode
	Default Value:	09h						
Project:	All							
Format:	Opcode							
13:12	<p><b>SIMD Mode</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_SM3 [CHV, BSW]</td> </tr> </table> <p>Specifies the SIMD mode of the message (number of slots processed)</p>	Project:	All	Format:	MDC_SM3 [CHV, BSW]			
Project:	All							
Format:	MDC_SM3 [CHV, BSW]							
11:8	<p><b>Channel Mask</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_UW_CMASK [CHV, BSW]</td> </tr> </table> <p>Specifies which RGBA channels are included in the message payload.</p>	Project:	All	Format:	MDC_UW_CMASK [CHV, BSW]			
Project:	All							
Format:	MDC_UW_CMASK [CHV, BSW]							
7:0	<p><b>Binding Table Index</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MDC_BTS_SLM_A32 [CHV, BSW]</td> </tr> </table> <p>Specifies the Binding Table Index for the message</p>	Project:	All	Format:	MDC_BTS_SLM_A32 [CHV, BSW]			
Project:	All							
Format:	MDC_BTS_SLM_A32 [CHV, BSW]							

## URB Hword Dual Block Read MSD

MSD_UR_HWDB - URB Hword Dual Block Read MSD			
Project:		CHV, BSW	
Source:		Read-Only DataPort	
Length Bias:		1	
DWord	Bit	Description	
0	19	<b>Header Present</b>	
		Project:	All
		Format:	MDC_MHR [CHV, BSW]
		Indicates that the message requires a header.	
	18	<b>Reserved</b>	
	17	<b>Per Slot Offset</b>	
		Format:	MHC_PSOP
		Specifies if per-slot offsets are present and will be added to the <b>Global Offset</b> .	
	16	<b>Reserved</b>	
	15	<b>Swizzle Control</b>	
	Project:	All	
	Format:	Opcode	
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	1	URB_INTERLEAVED [Default]	Use two URB entries ( <b>URB Handle 0</b> and <b>URB Handle 1</b> ).
	<b>Project</b>	All	
14:4	<b>Global Offset</b>		
	Project:	All	
	Format:	U11	
	Specifes the offset, in units of Hword elements, from the start of the URB handle for the access. If <b>Per Slot Offset</b> is set, the global offset is added to those offsets to form the overall offset. Range [0,1023]		
3:0	<b>URB Opcode</b>		
	Project:	All	
	Format:	Opcode	
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	2	URB_READ_HWORD [Default]	URB Hword Read message
	<b>Project</b>	All	

## URB Hword Dual Block Write MSD

MSD_UW_HWDB - URB Hword Dual Block Write MSD			
Project:		CHV, BSW	
Source:		Read-Only DataPort	
Length Bias:		1	
DWord	Bit	Description	
0	19	<b>Header Present</b>	
		Project:	All
		Format:	MDC_MHR [CHV, BSW]
		Indicates that the message requires a header.	
	18	<b>Reserved</b>	
	17	<b>Per Slot Offset</b>	
		Format:	MHC_PSOP
		Specifies if per-slot offsets are present and will be added to the <b>Global Offset</b> .	
	16	<b>Reserved</b>	
	15	<b>Swizzle Control</b>	
	Project:	All	
	Format:	Opcode	
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	1	URB_INTERLEAVED [Default]	Use two URB entries ( <b>URB Handle 0</b> and <b>URB Handle 1</b> ).
	<b>Project</b>	All	
14:4	<b>Global Offset</b>		
	Project:	All	
	Format:	U11	
	Specifes the offset, in units of Hword elements, from the start of the URB handle for the access. If <b>Per Slot Offset</b> is set, the global offset is added to those offsets to form the overall offset. Range [0,1023]		
3:0	<b>URB Opcode</b>		
	Project:	All	
	Format:	Opcode	
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0	URB_WRITE_HWORD [Default]	URB Hword Read message
	<b>Project</b>	All	

## URB Oword Block Write MSD

MSD_UW_OWB - URB Oword Block Write MSD										
Project:		CHV, BSW								
Source:		Read-Only DataPort								
Length Bias:		1								
DWord	Bit	Description								
0	19	<b>Header Present</b>								
	Project:		All							
	Format:		MDC_MHR [CHV, BSW]							
	Indicates that the message requires a header.									
	18	<b>Reserved</b>								
	17	<b>Per Slot Offset</b>								
	Format:		MHC_PSOP							
	Specifies if per-slot offsets are present and will be added to the <b>Global Offset</b> .									
	16	<b>Reserved</b>								
	15	<b>Swizzle Control</b>								
Project:		All								
Format:		Opcode								
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>URB_NOSWIZZLE [Default]</td> <td>Use a single URB entry (<b>URB Handle 0</b>).</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	0	URB_NOSWIZZLE [Default]	Use a single URB entry ( <b>URB Handle 0</b> ).	All
Value	Name	Description	Project							
0	URB_NOSWIZZLE [Default]	Use a single URB entry ( <b>URB Handle 0</b> ).	All							
14:4	<b>Global Offset</b>									
Project:		All								
Format:		U11								
Specifies the offset, in units of Oword elements, from the start of the URB handle for the access. If <b>Per Slot Offset</b> is set, the global offset is added to those offsets to form the overall offset. Range [0,2047]										
3:0	<b>URB Opcode</b>									
Project:		All								
Format:		Opcode								
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>URB_WRITE_OWORD [Default]</td> <td>URB Oword Write message</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	1	URB_WRITE_OWORD [Default]	URB Oword Write message	All
Value	Name	Description	Project							
1	URB_WRITE_OWORD [Default]	URB Oword Write message	All							

## URB Oword Dual Block Read MSD

MSD_UR_OWDB - URB Oword Dual Block Read MSD			
Project:		CHV, BSW	
Source:		Read-Only DataPort	
Length Bias:		1	
DWord	Bit	Description	
0	19	<b>Header Present</b>	
		Project:	All
		Format:	MDC_MHR [CHV, BSW]
		Indicates that the message requires a header.	
	18	<b>Reserved</b>	
	17	<b>Per Slot Offset</b>	
		Format:	MHC_PSOP
		Specifies if per-slot offsets are present and will be added to the <b>Global Offset</b> .	
	16	<b>Reserved</b>	
	15	<b>Swizzle Control</b>	
	Project:	All	
	Format:	Opcode	
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	1	URB_INTERLEAVED [Default]	Use two URB entries ( <b>URB Handle 0</b> and <b>URB Handle 1</b> ).
	<b>Project</b>	All	
14:4	<b>Global Offset</b>		
	Project:	All	
	Format:	U11	
	Specifes the offset, in units of Oword elements, from the start of the URB handle for the access. If <b>Per Slot Offset</b> is set, the global offset is added to those offsets to form the overall offset. Range [0,2047]		
3:0	<b>URB Opcode</b>		
	Project:	All	
	Format:	Opcode	
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	3	URB_READ_OWORD [Default]	URB Oword Read message
	<b>Project</b>	All	

## URB Oword Dual Block Write MSD

MSD_UW_OWDB - URB Oword Dual Block Write MSD			
Project:		CHV, BSW	
Source:		Read-Only DataPort	
Length Bias:		1	
DWord	Bit	Description	
0	19	<b>Header Present</b>	
		Project:	All
		Format:	MDC_MHR [CHV, BSW]
		Indicates that the message requires a header.	
	18	<b>Reserved</b>	
	17	<b>Per Slot Offset</b>	
		Format:	MHC_PSOP
		Specifies if per-slot offsets are present and will be added to the <b>Global Offset</b> .	
	16	<b>Reserved</b>	
	15	<b>Swizzle Control</b>	
	Project:	All	
	Format:	Opcode	
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	1	URB_INTERLEAVED [Default]	Use two URB entries ( <b>URB Handle 0</b> and <b>URB Handle 1</b> ).
	<b>Project</b>	All	
14:4	<b>Global Offset</b>		
	Project:	All	
	Format:	U11	
	Specifes the offset, in units of Oword elements, from the start of the URB handle for the access. If <b>Per Slot Offset</b> is set, the global offset is added to those offsets to form the overall offset. Range [0,2047]		
3:0	<b>URB Opcode</b>		
	Project:	All	
	Format:	Opcode	
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	1	URB_WRITE_OWORD [Default]	URB Oword Write message
	<b>Project</b>	All	

## VEBOX\_STATE

VEBOX_STATE						
Project:	CHV, BSW					
Source:	VideoEnhancementCS					
Length Bias:	2					
<p>This command controls the internal functions of the VEBOX. This command has a set of indirect state buffers:</p> <ul style="list-style-type: none"> <li>• DN/DI state</li> <li>• Capture Pipe state</li> </ul>						
DWord	Bit	Description				
0	31:29	<b>Command Type</b>				
		Default Value:	3h PARALLEL_VIDEO_PIPE			
		Format:	OpCode			
	28:27	<b>Pipeline</b>				
		Default Value:	2h Media			
		Format:	OpCode			
	26:24	<b>Command OpCode</b>				
		Default Value:	4h VEBOX			
		Format:	OpCode			
	23:21	<b>SubOpcode A</b>				
Default Value:		0h				
Format:		OpCode				
20:16	<b>SubOpcode B</b>					
	Default Value:	2h				
	Format:	OpCode				
15:12	<b>Reserved</b>					
11:0	<b>DWord Length</b>					
	Format:	=n Total Length - 2				
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>Ah</td> <td></td> <td>(Excludes DWords 0, 1)</td> </tr> </tbody> </table>	Value	Name	Description	Ah	
Value	Name	Description				
Ah		(Excludes DWords 0, 1)				
1	31:25	<b>State Surface Control Bits</b>				
	24:23	<b>Reserved</b>				
	22	<b>Reserved</b>				
	21	<b>Reserved</b>				
	20	<b>Reserved</b>				



<b>VEBOX_STATE</b>																							
19:15	<b>Reserved</b>																						
14	<b>Single Slice VEBOX Enable</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table> <p>For products that have 2 entire VEBOXes that automatically split the frame, this enable emulates a 1 VEBOX product, running at 1/2 speed and only outputting a single set of per command statistics.</p>		Project:	CHV, BSW																			
Project:	CHV, BSW																						
13	<b>Hot Pixel Filtering Enable</b> Enables hot pixel detection/filtering.																						
12	<b>Alpha Plane Enable</b> Enables the reading of an independent Alpha plane. Mutually exclusive with Vignette Enable. If <b>Alpha from State Select</b> is set it overrides this bit.																						
11	<b>Reserved</b>																						
10	<b>Demosaic Enable</b> The Demosaic will be used, and White balance statistics will be gathered. The Capture Pipe State Table will be read. This bit is mutually exclusive with <b>DI Enable</b> .																						
9:8	<b>DI Output Frames</b> Indicates which frames to output in DI mode. <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 10px;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">00b</td> <td>Output Both Frames</td> </tr> <tr> <td style="text-align: center;">01b</td> <td>Output Previous Frame Only</td> </tr> <tr> <td style="text-align: center;">10b</td> <td>Output Current Frame Only</td> </tr> </tbody> </table> <div style="margin-top: 10px; border: 1px solid black; padding: 5px;"> <p style="text-align: center; margin: 0;"><b>Programming Notes</b></p> <p>Field is ignored if DI Enable = 0. If Previous Frame Only or Current Frame Only are selected, then the <b>LACE Single Histogram Set</b> must not try to collect a histogram from the disabled frame.</p> <p>Field must be programmed to 10 (Output Current Frame Only) for DI First Frame.</p> </div>		Value	Name	00b	Output Both Frames	01b	Output Previous Frame Only	10b	Output Current Frame Only													
Value	Name																						
00b	Output Both Frames																						
01b	Output Previous Frame Only																						
10b	Output Current Frame Only																						
7	<b>444 -&gt; 422 Downsample Method</b> <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 10px;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">1</td> <td>Average horizontally aligned chromas</td> </tr> <tr> <td style="text-align: center;">0</td> <td>Drop right chroma of the pair <b>[Default]</b></td> </tr> </tbody> </table> <div style="margin-top: 10px; border: 1px solid black; padding: 5px;"> <p style="text-align: center; margin: 0;"><b>Programming Notes</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">444-&gt;422</th> <th style="text-align: center;">422-&gt;420</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td>No averaging, only down sampling</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td>Not Supported</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td>Only Horizontal averaging</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td>Horizontal and Vertical averaging</td> </tr> </tbody> </table> </div>		Value	Name	1	Average horizontally aligned chromas	0	Drop right chroma of the pair <b>[Default]</b>	444->422	422->420	Description	0	0	No averaging, only down sampling	0	1	Not Supported	1	0	Only Horizontal averaging	1	1	Horizontal and Vertical averaging
Value	Name																						
1	Average horizontally aligned chromas																						
0	Drop right chroma of the pair <b>[Default]</b>																						
444->422	422->420	Description																					
0	0	No averaging, only down sampling																					
0	1	Not Supported																					
1	0	Only Horizontal averaging																					
1	1	Horizontal and Vertical averaging																					

<b>VEBOX_STATE</b>									
6	<p><b>422 -&gt; 420 Downsample Method</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table> <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th style="width: 15%;">Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">1</td> <td>Average vertically aligned chromas</td> </tr> <tr> <td style="text-align: center;">0</td> <td>Drop lower chroma of the pair <b>[Default]</b></td> </tr> </tbody> </table> <p style="text-align: center; margin-top: 10px;"><b>Programming Notes</b></p> <p>To enable averaging in case of 420 (NV12/P016) output formats, 444-&gt;422 and 422-&gt;420 should be set.</p>	Project:	CHV, BSW	Value	Name	1	Average vertically aligned chromas	0	Drop lower chroma of the pair <b>[Default]</b>
Project:	CHV, BSW								
Value	Name								
1	Average vertically aligned chromas								
0	Drop lower chroma of the pair <b>[Default]</b>								
5	<p><b>DN/DI First Frame</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>Enable</td> </tr> </table> <p>Indicates that this is the first frame of the stream, so previous clean is not available.</p> <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th style="width: 15%;">Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Not first field; previous clean surface state is valid</td> </tr> <tr> <td style="text-align: center;">1</td> <td>First field; previous clean surface state is invalid</td> </tr> </tbody> </table> <p style="text-align: center; margin-top: 10px;"><b>Programming Notes</b></p> <p>If both DN and DI are disabled, this bit must be 0.</p>	Format:	Enable	Value	Name	0	Not first field; previous clean surface state is valid	1	First field; previous clean surface state is invalid
Format:	Enable								
Value	Name								
0	Not first field; previous clean surface state is valid								
1	First field; previous clean surface state is invalid								
4	<p><b>DI Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>Enable</td> </tr> </table> <p>Deinterlacer is bypassed if this is disabled: the output is the same as the input (same as a 2:2 cadence). FMD and STMM are not calculated and the values in the response message are 0.</p> <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th style="width: 15%;">Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Do not calculate DI</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Calculate DI</td> </tr> </tbody> </table>	Format:	Enable	Value	Name	0	Do not calculate DI	1	Calculate DI
Format:	Enable								
Value	Name								
0	Do not calculate DI								
1	Calculate DI								
3	<p><b>DN Enable</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>Enable</td> </tr> </table> <p>Denoise is bypassed if this is low - BNE is still calculated and output, but the denoised fields are not. VDI does not read in the denoised previous frame but uses the pointer for the original previous frame.</p> <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th style="width: 15%;">Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Do not denoise frame</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Denoise frame</td> </tr> </tbody> </table> <p style="text-align: center; margin-top: 10px;"><b>Programming Notes</b></p> <p>If DN and/or Hotpixel are the only functions enabled then the only output is the Denoised Output which is the same surface format as the input.</p>	Format:	Enable	Value	Name	0	Do not denoise frame	1	Denoise frame
Format:	Enable								
Value	Name								
0	Do not denoise frame								
1	Denoise frame								
2	<b>Reserved</b>								

<b>VEBOX_STATE</b>				
	1	<p><b>Color Gamut Compression Enable</b> Indicates if the Gamut Compression feature is enabled. If set then the Gamut State will be read. VEB_VERTEXTABLE_STATE is only needed if this bit is set.</p>		
	0	<p><b>Color Gamut Expansion Enable</b> Indicates if the Gamut Expansion feature is enabled. If set then the Gamut State will be read.</p>		
2	31:12	<p><b>DN/DI State Pointer Low</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicAddress[31:12]</td> </tr> </table> <p>Bits 31:12 of the starting address of the DN/DI State buffer. This points to a buffer containing the 10 Dwords of the DN/DI state.</p>	Format:	GraphicAddress[31:12]
	Format:	GraphicAddress[31:12]		
11:0	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ			
3	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
15:0	<p><b>DN/DI State Pointer High</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicAddress[47:32]</td> </tr> </table> <p>Bits 47:32 of the starting address of the DN/DI State Buffer.</p>	Format:	GraphicAddress[47:32]	
Format:	GraphicAddress[47:32]			
4	31:12	<p><b>Reserved</b></p>		
	11:0	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			
5	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
15:0	<p><b>Reserved</b></p>			
6	31:12	<p><b>Gamut State Pointer Low</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicAddress[31:12]</td> </tr> </table> <p>Bits 31:12 of the starting address of the Gamut State buffer. This points to a buffer containing the 42 Dwords of Gamut Compression / Gamut Expansion state.</p>	Format:	GraphicAddress[31:12]
	Format:	GraphicAddress[31:12]		
11:0	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ			
7	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
15:0	<p><b>Gamut State Pointer High</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicAddress[47:32]</td> </tr> </table> <p>Bits 47:32 of the starting address of the Gamut State Buffer.</p>	Format:	GraphicAddress[47:32]	
Format:	GraphicAddress[47:32]			
8	31:12	<p><b>Vertex Table State Pointer Low</b></p>		

<b>VEBOX_STATE</b>				
		<table border="1"> <tr> <td>Format:</td> <td>GraphicAddress[31:12]</td> </tr> </table> <p>Bits 31:12 of the starting address of the Vertex Table. This points to a buffer containing the 512 Dwords of the Gamut Compression Vertex Table.</p>	Format:	GraphicAddress[31:12]
Format:	GraphicAddress[31:12]			
	11:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			
9	31:16	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			
	15:0	<p><b>Vertex Table State Pointer High</b></p> <table border="1"> <tr> <td>Format:</td> <td>GraphicAddress[47:32]</td> </tr> </table> <p>Bits 47:32 of the starting address of the Vertex State Buffer.</p>	Format:	GraphicAddress[47:32]
Format:	GraphicAddress[47:32]			
10	31:12	<p><b>Capture Pipe State Pointer Low</b></p> <table border="1"> <tr> <td>Format:</td> <td>GraphicAddress[31:12]</td> </tr> </table> <p>Bits 31:12 of the starting address of the Capture Pipe State Table. This points to a buffer containing the X Dwords of the Capture Pipe State.</p>	Format:	GraphicAddress[31:12]
Format:	GraphicAddress[31:12]			
	11:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			
11	31:16	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			
	15:0	<p><b>Capture Pipe State Pointer High</b></p> <table border="1"> <tr> <td>Format:</td> <td>GraphicAddress[47:32]</td> </tr> </table> <p>Bits 47:32 of the starting address of the Capture Pipe State Table.</p>	Format:	GraphicAddress[47:32]
Format:	GraphicAddress[47:32]			

## VEBOX\_SURFACE\_STATE

<b>VEBOX_SURFACE_STATE</b>	
Project:	CHV, BSW
Source:	VideoEnhancementCS
Length Bias:	2
Description	
<p>The input and output data containers accessed are called "surfaces". Surface state is sent to VEBOX via an inline state command rather than using binding tables. SURFACE_STATE contains the parameters defining each surface to be accessed, including its size, format, and offsets to its subsurfaces. The surface's base address is in the execution command. Despite having multiple input and output surfaces, we limit the number of surface states to one for input surfaces and one for output surfaces. The other surfaces are derived from the input/output surface states.</p>	
<p>The Current Frame Input surface uses the Input SURFACE_STATE</p>	
<p>The Previous Denoised Input surface uses the Input SURFACE_STATE. (For 12-bit Bayer pattern inputs this will be 8-bit.)</p>	
<p>The Current Denoised Output surface uses the Input SURFACE_STATE. (For 12-bit Bayer pattern inputs this will be 8-bit.)</p>	
<p>The STMM/Noise History Input surface uses the Input SURFACE_STATE with Tile-Y and Width/Height a multiple of 4.</p>	
<p>The STMM/Noise History Output surface uses the Input SURFACE_STATE with Tile-Y and Width/Height a multiple of 4.</p>	
<p>The FMD per block output / per Frame Output surface uses the Linear SURFACE_STATE (see note below).</p>	
<p>The Alpha surface uses the Linear A8 SURFACE_STATE with Width/Height equal to Input Surface. Pitch is width rounded to next 64.</p>	
<p>The Vignette Correction surface uses the Linear 16-bit SURFACE_STATE with: Width = <math>4 * ((\text{Input Width } 3)/4)</math> Height = <math>((\text{Input Height } 3)/4)</math> Pitch in bytes is <math>(\text{vignette width} * 2)</math> rounded to next 64.</p>	
<p>The STMM height is the same as the Input Surface height except when the input <b>Surface Format</b> is Bayer Pattern and the <b>Bayer Pattern Offset</b> is 10 or 11, in which case the height is the input height + 4. For Bayer pattern inputs when the <b>Bayer Pattern Offset</b> is 10 or 11, the Current Denoised Output/Previous Denoised Input will also have a height which is the input height + 4. For Bayer pattern inputs only the Current Denoised Output/Previous Denoised Input are in Tile-Y.</p>	
<p>The linear surface for FMD statistics is linear (not tiled). The height of the per block statistics is <math>(\text{Input Height } + 3)/4</math> - the Input Surface height in pixels is rounded up to the next even 4 and divided by 4. The width of the per block section in bytes is equal to the width of the Input Surface in pixels rounded up to the next 16 bytes. The pitch of the per block section in bytes is equal to the width of the Input Surface in pixels rounded up to the next 64 bytes.</p>	
<p>The STMM surfaces must be identical to the Input surface except for the tiling mode must be Tile-Y and the pitch must be legal for Tile-Y (increased to the next larger legal pitch). If the input surface is packed (Surface</p>	

## VEBOX\_SURFACE\_STATE

Format from 0 to 3 for DN/DI) or 12/10-bit Bayer Pattern then the pitch for the STMM surface is 1/2 the pitch of the input surface (rounded up to the next larger legal Tile-Y pitch). The width and height must be a multiple of 4 rounded up from the input height.

### Programming Notes

VEBOX may write to memory between the surface width and the surface pitch for output surfaces.

For 8bit Alpha input, when converting to 16bit output it is padded with 8bit zeros in the LSB.

DWord	Bit	Description			
0	31:29	<b>Command Type</b>			
		Default Value:		3h PARALLEL_VIDEO_PIPE	
	Format:		OpCode		
	28:27	<b>Media Command Pipeline</b>			
		Default Value:		2h Media	
	Format:		OpCode		
	26:24	<b>Media Command OpCode</b>			
		Default Value:		4h VEBOX	
	Format:		OpCode		
	23:21	<b>SubOpcode A</b>			
Default Value:		0h VEBOX			
Format:		OpCode			
20:16	<b>SubOpcode B</b>				
	Default Value:		0h VEBOX		
Format:		OpCode			
15:12	<b>Reserved</b>				
	Format:		MBZ		
11:0	<b>DWord Length</b>				
	Format:		=n Total Length - 2		
	<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Project</b>	
	4h	DWORD_COUNT_n [Default]	(Excludes DWords 0, 1)	CHV, BSW	
1	31:1	<b>Reserved</b>			
		<b>Surface Identification</b>			
	Specifies which set of surfaces this command refers to:				
	<b>Value</b>	<b>Name</b>			
1	Output surface (all except the Denoised Current output surface)				
0	Input surface and Denoised Current Output Surface				
2	31:18	<b>Height</b>			

		<b>VEBOX_SURFACE_STATE</b>																	
		Format:	U14																
		This field specifies the height of the surface in units of pixels. For PLANAR surface formats, this field indicates the height of the Y (luma) plane.																	
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Exists If</th> </tr> </thead> <tbody> <tr> <td>[15, 16383]</td> <td></td> <td>representing heights [16,16384]</td> <td></td> </tr> <tr> <td>[15, 8191]</td> <td></td> <td></td> <td>//Scalar Enabled - For Input surface only</td> </tr> <tr> <td>[63, 2047]</td> <td></td> <td></td> <td>//Scalar + SFC Enabled - For Input surface only</td> </tr> </tbody> </table>	Value	Name	Description	Exists If	[15, 16383]		representing heights [16,16384]		[15, 8191]			//Scalar Enabled - For Input surface only	[63, 2047]			//Scalar + SFC Enabled - For Input surface only	
Value	Name	Description	Exists If																
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[15, 8191]			//Scalar Enabled - For Input surface only																
[63, 2047]			//Scalar + SFC Enabled - For Input surface only																
		<b>Programming Notes</b>																	
		<p><b>Height</b> (field value + 1) must be a multiple of 2 for PLANAR_420 surfaces. <b>Height</b> (field value + 1) must be a multiple of 2 when the deinterlace function is enabled (field mode) or when the denoise function is enabled with <b>Progressive DN</b> = 0. It must be a multiple of 4 when interleaved deinterlace/denoise and PLANAR_420 are both being used. <b>VEBOX</b> supports a minimum height of 16.</p> <p><b>Height</b> (field value + 1) must be a multiple of 2 for Bayer surfaces.</p>																	
17:4	<b>Width</b>	Format:	U14																
		This field specifies the width of the surface in units of pixels. For PLANAR surface formats, this field indicates the width of the Y (luma) plane.																	
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Exists If</th> </tr> </thead> <tbody> <tr> <td>[63,16383]</td> <td></td> <td>representing widths [64,16384]</td> <td></td> </tr> <tr> <td>[63,8191]</td> <td></td> <td></td> <td>//Scalar Enabled - For Input surface only</td> </tr> <tr> <td>[63,2047]</td> <td></td> <td></td> <td>//Scalar and SFC Enabled - For Input Surface only</td> </tr> </tbody> </table>	Value	Name	Description	Exists If	[63,16383]		representing widths [64,16384]		[63,8191]			//Scalar Enabled - For Input surface only	[63,2047]			//Scalar and SFC Enabled - For Input Surface only	
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[63,2047]			//Scalar and SFC Enabled - For Input Surface only																
		<b>Programming Notes</b>																	
		<p>The Width specified by this field multiplied by the pixel size in bytes must be less than or equal to the surface pitch (specified in bytes via the <b>Surface Pitch</b> field). <b>Width</b> (field value + 1) must be a multiple of 2 for PLANAR_420, PLANAR_422, and all YCRCB_* surfaces, and must be a multiple of 4 for PLANAR_411 surfaces. <b>VEBOX</b> supports a minimum width of 64</p>																	
	3:0	<b>Reserved</b>																	
3	31:28	<b>Surface Format</b>																	
		Project:	CHV, BSW																
		Format:	U4																
		Specifies the format of the surface. All of the Y and G channels will use table 0 and all of the Cr/Cb/R/B channels will use table 1.																	
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> </tbody> </table>	Value	Name	Description														
Value	Name	Description																	

<b>VEBOX_SURFACE_STATE</b>			
	4	PLANAR_420_8	NV12 with Interleave Chroma set
	14	Bayer pattern	Demosaic input only
	15	Reserved	
27	<b>Interleave Chroma</b>		
	Project:	CHV, BSW	
	Format:	Enable	
	This field indicates that the chroma fields are interleaved in a single plane rather than stored as two separate planes. This field is only used for PLANAR surface formats.		
26:25	<b>Bayer Pattern Offset</b>		
	Project:	CHV, BSW	
	Specifies the starting pixel offset for the Bayer pattern used for Capture Pipe.		
	<b>Value</b>	<b>Name</b>	
	00b	Pixel at X=0, Y=0 is Blue	
	01b	Pixel at X=0, Y=0 is Red	
	10b	Pixel at X=0, Y=0 is Green, Pixel at X=1, Y=0 is Red	
	11b	Pixel at X=0, Y=0 is Green, Pixel at X=1, Y=0 is Blue	
24	<b>Bayer Pattern Format</b>		
	Project:	CHV, BSW	
	Specifies the format of the Bayer Pattern:		
	<b>Value</b>	<b>Name</b>	<b>Project</b>
	0b	8-bit input at a 8-bit stride	
	1b	12 or 10-bit input at a 16-bit stride. Valid data is in the MSBs	CHV, BSW
23:21	<b>Reserved</b>		
	Project:		
	Format:	MBZ	
20	<b>Reserved</b>		
	Project:	CHV, BSW	
	Format:	MBZ	
19:3	<b>Surface Pitch</b>		
	Format:	U17 pitch in (Bytes - 1)	
	This field specifies the surface pitch in (#Bytes - 1):		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	[63, 131071]	For other linear surfaces	[64B, 128KB]
	[511, 131071]	For X-tiled surface	[512B, 128KB] = [1tile, 256 tiles]
	[127, 131071]	For Y-tiled surfaces	[128B,128KB] = [1 tile, 1024 tiles]



<b>VEBOX_SURFACE_STATE</b>													
		<p style="text-align: center;"><b>Programming Notes</b></p> <p>For tiled surfaces, the pitch must be a multiple of the tile width. For linear surfaces, the pitch must be a multiple of 64. If Half Pitch for Chroma is set, this field must be a multiple of two tile widths for tiled surfaces, or a multiple of 2 bytes for linear surfaces.</p>											
	2	<p><b>Half Pitch for Chroma</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field indicates that the chroma plane(s) will use a pitch equal to half the value specified in the <b>Surface Pitch</b> field. This field is only used for PLANAR surface formats.</p> <p style="text-align: center;"><b>Programming Notes</b></p> <p>Must be programmed to Zero always as this field is not used</p>	Format:	Enable									
Format:	Enable												
	1	<p><b>Tiled Surface</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Boolean</td> </tr> </table> <p>This field specifies whether the surface is tiled.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 20%;">Value</th> <th style="width: 30%;">Name</th> <th style="width: 50%;">Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>True</td> <td>Tiled</td> </tr> <tr> <td>0</td> <td>False</td> <td>Linear</td> </tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>Linear surfaces can be mapped to Main Memory (uncached) or System Memory (cacheable, snooped). Tiled surfaces can only be mapped to Main Memory. The corresponding cache(s) must be invalidated before a previously accessed surface is accessed again with an altered state of this bit.</p>	Format:	Boolean	Value	Name	Description	1	True	Tiled	0	False	Linear
Format:	Boolean												
Value	Name	Description											
1	True	Tiled											
0	False	Linear											
	0	<p><b>Tile Walk</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>3D_TileWalk</td> </tr> </table> <p>This field specifies the type of memory tiling (XMajor or YMajor) employed to tile this surface. See <i>Memory Interface Functions</i> for details on memory tiling and restrictions. This field is ignored when the surface is linear.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 20%;">Value</th> <th style="width: 80%;">Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>TILEWALK_XMAJOR</td> </tr> <tr> <td>1</td> <td>TILEWALK_YMAJOR</td> </tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>The corresponding cache(s) must be invalidated before a previously accessed surface is accessed again with an altered state of this bit.</p>	Format:	3D_TileWalk	Value	Name	0	TILEWALK_XMAJOR	1	TILEWALK_YMAJOR			
Format:	3D_TileWalk												
Value	Name												
0	TILEWALK_XMAJOR												
1	TILEWALK_YMAJOR												
4	31:29	<b>Reserved</b>											
	28:16	<p><b>X Offset for U</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>U13 Pixel Offset</td> </tr> </table> <p>This field must be zero for the VEBOX surface formats</p>	Format:	U13 Pixel Offset									
Format:	U13 Pixel Offset												

<b>VEBOX_SURFACE_STATE</b>						
	15	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
	Format:	MBZ				
14:0	<p><b>Y Offset for U</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 40%;">Format:</td> <td>U15 Row Offset</td> </tr> </table> <p>This field specifies the vertical offset in rows from the <b>Surface Base Address</b> to the start (origin) of the U(Cb) plane or the interleaved UV plane if <b>Interleave Chroma</b> is enabled. This field is only used for PLANAR surface formats.</p> <table border="1" style="width: 100%; background-color: #e6f2ff;"> <tr> <th colspan="2" style="text-align: center;">Programming Notes</th> </tr> </table> <p>This field must indicate an even number (bit 0 = 0). This field must be evenly divisible by 4 for Tile-Y surfaces (so the offset points to the start of a cache line) For Planar formats, if the surface is in YS or YF tile modes, the Y Offset for U should be an integral multiple of the Tile height of the Luma plane</p>	Format:	U15 Row Offset	Programming Notes		
Format:	U15 Row Offset					
Programming Notes						
5	31:29	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
	Format:	MBZ				
	28:16	<p><b>X Offset for V</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 40%;">Format:</td> <td>U13 Pixel Offset</td> </tr> </table> <p>This field must be zero for the VEBOX surface formats.</p>	Format:	U13 Pixel Offset		
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15	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ			
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14:0	<p><b>Y Offset for V</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 40%;">Format:</td> <td>U15 Row Offset</td> </tr> </table> <p>This field specifies the vertical offset in rows from the <b>Surface Base Address</b> to the start (origin) of the V(Cr) plane. This field is only used for PLANAR surface formats with <b>Interleave Chroma</b> disabled.</p> <table border="1" style="width: 100%; background-color: #e6f2ff;"> <tr> <th colspan="2" style="text-align: center;">Programming Notes</th> </tr> </table> <p>This field must indicate an even number (bit 0 = 0). This field must be evenly divisible by 4 for Tile-Y surfaces (so the offset points to the start of a cache line). For Planar formats, if the surface is in YS or YF tile modes, the Y Offset for V should be an integral multiple of the Tile height of the Luma plane</p>	Format:	U15 Row Offset	Programming Notes		
Format:	U15 Row Offset					
Programming Notes						
6..7	31:0	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 40%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ
Project:	CHV, BSW					
Format:	MBZ					

## Wait Notification

<b>wait - Wait Notification</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
<p>The wait instruction evaluates the value of the notification count register nreg. If nreg is zero, thread execution is suspended and the thread is put in 'wait_for_notification' state. If nreg is not zero (i.e., one or more notifications have been received), nreg is decremented by one and the thread continues executing on the next instruction. If a thread is in the 'wait_for_notification' state, when a notification arrives, the notification count register is incremented by one. As the notification count register becomes nonzero, the thread wakes up to continue execution and at the same time the notification register is decremented by one. If only one notification arrived, the notification register value becomes zero. However, during the above mentioned time period, it is possible that more notifications may arrive, making the notification register nonzero again. When multiple notifications are received, software must use wait instructions to decrement notification count registers for each notification. Notification register n0.0:ud is for thread to thread communication (via the Message Gateway shared function) and n0.1:ud for host to thread communication (through MMIO registers). See the Message Gateway chapter for thread-thread communication.</p>			
Format: wait (exec_size) nreg			
<b>Restriction</b>			
src0 and dst must be n0.0, n0.1, or n0.2.			
Execution size must be 1 as the notification registers are scalar.			
Predication is not allowed.			
Two back-to-back wait instructions are not allowed. At minimum, a nop instruction must be inserted between two wait instructions			
<b>Syntax</b>			
wait (1) n#			
<b>Pseudocode</b>			
N/A			
Predication	Conditional Modifier	Saturation	Source Modifier
N	N	N	N
Src Types	Dst Types		
UD	UD		

DWord	Bit	Description
0	127:64	<b>Sources</b>
		Exists If: ((Operand Control)[Src1.RegFile]!='IMM')
	Format: EU_INSTRUCTION_SOURCES_REG [CHV, BSW]	
	127:64	<b>Sources</b>
		Exists If: ((Operand Control)[Src1.RegFile]='IMM')
	Format: EU_INSTRUCTION_SOURCES_IMM32 [CHV, BSW]	
	63:32	<b>Operand Control</b>
		Format: EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]
31:0	<b>Header</b>	
	Format: EU_INSTRUCTION_HEADER [CHV, BSW]	

## While

<b>while - While</b>			
Project:	CHV, BSW		
Source:	Eulsa		
Length Bias:	4		
Description			
<p>The while instruction marks the end of a do-while block. The instruction first evaluates the loop termination condition for each channel based on the current channel enables and the predication flags specified in the instruction. If any channel has not terminated, a branch is taken to a destination address specified in the instruction, and the loop continues for those channels. Otherwise, execution continues to the next instruction. It should point to the first instruction with the do label of the do-while block of code. It should be a negative number for the backward referencing. In GEN binary, JIP is at location dst and must be of type W (signed word integer). If SPF is ON, none of the PclP are updated.</p> <p>The following table describes the 32-bit jump target offset JIP. JIP is a signed 32-bit number, added to IP pre-increment, and should point to the first instruction with the do label of the do-while block of code. It should be a negative number for the backward referencing. In GEN binary, JIP is at location src1 and must be of type D (signed dword integer).</p>			
Format: [(pred)] while (exec_size) JIP			
Restriction			
The execution size must be the same for the while instruction and any break and cont instructions of the same code block.			
Syntax	Project		
[(pred)] while (exec_size) imm32	CHV, BSW		
Pseudocode			
<pre>Evaluate(WrEn); for ( n = 0; n &lt; 32; n++ ) { if (WrEn.chan[n] ) { PclP[n] = IP + JIP; } else { PclP[n] = IP + 1; } } if (   PMask == 1 ) { // any enabled channel true Jump(IP + JIP); }</pre>			
Predication	Conditional Modifier	Saturation	Source Modifier
Y	N	N	N
DWord	Bit	Description	
0..3	127:96	<b>JIP</b>	
		Project:	CHV, BSW
		Format:	S31
		Jump Target Offset. The relative offset in bytes if a jump is taken for the instruction.	
	95	<b>Source 0 Address Immediate [9] Sign Bit</b>	
		Project:	CHV, BSW

<b>while - While</b>		
	94:91	<b>Src1.SrcType</b>
		Project: CHV, BSW Format: SrcType [CHV, BSW]
	90:89	<b>Src1.RegFile</b>
		Project: CHV, BSW Format: RegFile [CHV, BSW]
	88:64	<b>Source 0</b>
		Exists If: (Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]== 'Align16') Format: EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN16 [CHV, BSW]
	88:64	<b>Source 0</b>
		Exists If: (Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]== 'Align1') Format: EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN1 [CHV, BSW]
	63:32	<b>Operand Control</b>
		Format: EU_INSTRUCTION_OPERAND_CONTROLS [CHV, BSW]
	31:0	<b>Header</b>
		Format: EU_INSTRUCTION_HEADER [CHV, BSW]

## XY\_COLOR\_BLT

XY_COLOR_BLT			
Project:	CHV, BSW		
Source:	BlitterCS		
Length Bias:	2		
<p>COLOR_BLT is the simplest BLT operation. It performs a color fill to the destination (with a possible ROP). The only operand is the destination operand which is written dependent on the raster operation. The solid pattern color is stored in the pattern background register.</p> <p>This instruction is optimized to run at the maximum memory write bandwidth.</p> <p>The typical (and fastest) Raster operation code = F0 which performs a copy of the pattern background register to the destination.</p>			
DWord	Bit	Description	
0 BR00	31:29	<b>Client</b>	
		Default Value:	02h 2D Processor
		Format:	Opcode
	28:22	<b>Instruction Target(Opcode)</b>	
		Default Value:	50h
		Format:	Opcode
	21:20	<b>32bpp Byte Mask</b>	
		This field is only used for 32bpp.	
		<b>Value</b>	<b>Name</b>
		1xb	Write Alpha Channel
	x1b	Write RGB Channel	
19:12	<b>Reserved</b>		
	Format:	MBZ	
11	<b>Tiling Enable</b>		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0b	Tiling Disabled (Linear Blit)	
	1b	Tiling Enabled	Tile-X or Tile-Y
10:8	<b>Reserved</b>		
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	05h	
1 BR13	31	<b>Reserved</b>	
		Format:	MBZ
	30	<b>Clipping Enabled</b>	
	<b>Value</b>	<b>Name</b>	

<b>XY_COLOR_BLT</b>												
		<table border="1"> <tr> <td>0b</td> <td>Disabled</td> </tr> <tr> <td>1b</td> <td>Enabled</td> </tr> </table>	0b	Disabled	1b	Enabled						
0b	Disabled											
1b	Enabled											
	29:26	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ								
Format:	MBZ											
	25:24	<b>Color Depth</b> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>8 Bit Color</td> </tr> <tr> <td>01b</td> <td>16 Bit Color(565)</td> </tr> <tr> <td>10b</td> <td>16 Bit Color(1555)</td> </tr> <tr> <td>11b</td> <td>32 Bit Color</td> </tr> </tbody> </table>	Value	Name	00b	8 Bit Color	01b	16 Bit Color(565)	10b	16 Bit Color(1555)	11b	32 Bit Color
Value	Name											
00b	8 Bit Color											
01b	16 Bit Color(565)											
10b	16 Bit Color(1555)											
11b	32 Bit Color											
	23:16	<b>Raster Operation</b>										
	15:0	<b>Destination Pitch in DWords</b> 2's complement For Tiled surfaces (bit_11 enabled) this pitch is of 512Byte granularity for Tile-X, 128B granularity for Tile-Y and can be upto 128Kbytes (or 32KDwords).										
2	31:16	<b>Destination Y1 Coordinate (Top)</b> 16 bit signed number.										
BR22	15:0	<b>Destination X1 Coordinate (Left)</b> 16 bit signed number.										
3	31:16	<b>Destination Y2 Coordinate (Bottom)</b> 16 bit signed number.										
BR23	15:0	<b>Destination X2 Coordinate (Right)</b> 16 bit signed number.										
4	31:0	<b>Destination Base Address</b> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[31:0]</td> </tr> </table> Base address of the destination surface: X=0, Y=0. Lower 32bits of the 48bit addressing. When Tiling is enabled (Bit_11 enabled), this address is limited to 4Kbytes. When Tiling is not enabled, this address should be CL (64byte) aligned.	Format:	GraphicsAddress[31:0]								
Format:	GraphicsAddress[31:0]											
BR09												
5	31:16	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> Should be programmed all 0's for 48bit addressing.	Format:	MBZ								
Format:	MBZ											
BR27												
	15:0	<b>Destination Base Address High</b> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> Should be programmed with the upper 16bits of the 48bit addressing.	Format:	GraphicsAddress[47:32]								
Format:	GraphicsAddress[47:32]											
6	31:0	<b>Solid Pattern Color</b> 8 bit = [7:0], 16 bit = [15:0], 32 bit = [31:0]										
BR16												



## XY\_FULL\_BLT

XY_FULL_BLT			
Project:	CHV, BSW		
Source:	BlitterCS		
Length Bias:	2		
<p>The full BLT is the most comprehensive BLT instruction. It provides the ability to specify all 3 operands: destination, source, and pattern. The source and pattern operands are the same bit width as the destination operand.</p> <p>The source and destination operands may overlap, which means that the X and Y directions can be either forward or backwards. The BLT Engine takes care of all situations. The base addresses plus the X and Y coordinates determine if there is an overlap between the source and destination operands. If the base addresses of the source and destination are the same and the Source X1 is less than Destination X1, then the BLT Engine performs the accesses in the X-backwards access pattern. There is no need to look for an actual overlap. If the base addresses are the same and Source Y1 is less than Destination Y1, then the scan line accesses start at Destination Y2 with the corresponding source scan line and the strides are subtracted for every scan line access. All scan lines and pixels that fall within the ClipRect Y and X coordinates are written. Only pixels within the ClipRectX coordinates and the Destination X coordinates are written using the raster operation.</p> <p>The Pattern Seeds correspond to Destination X = 0 (horizontal) and Y = 0 (vertical). The alignment is relative to the destination coordinates. The pixel of the pattern used / scan line is the (destination X coordinate + horizontal seed) modulo 8. The scan line of the pattern used is the (destination Y coordinate + vertical seed) modulo 8.</p>			
DWord	Bit	Description	
0  BR00	31:29	<b>Client</b>	
		Default Value:	02h 2D Processor
		Format:	Opcode
	28:22	<b>Instruction Target(Opcode)</b>	
		Default Value:	55h
		Format:	Opcode
	21:20	<b>32bpp Byte Mask</b>	
		This field is only used for 32bpp.	
		<b>Value</b>	<b>Name</b>
		00b	[Default]
1xb		Write Alpha Channel	
x1b	Write RGB Channel		
19:16	<b>Reserved</b>		
15	<b>Src Tiling Enable</b>		
	<b>Value</b>	<b>Name</b>	
	0b	Tiling Disabled (Linear Blit)	
1b	Tiling Enabled	[CHV, BSW]: Tile-X or Tile-Y.	
14:12	<b>Pattern Horizontal Seed</b>		
	Pixel of the scan line to start on corresponding to DST X=0.		

<b>XY_FULL_BLT</b>											
	11	<b>Dest Tiling Enable</b>									
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 45%;">Name</th> <th style="width: 40%;">Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Tiling Disabled (Linear Blit)</td> <td></td> </tr> <tr> <td>1b</td> <td>Tiling Enabled</td> <td>[CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.</td> </tr> </tbody> </table>	Value	Name	Description	0b	Tiling Disabled (Linear Blit)		1b	Tiling Enabled	[CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.
		Value	Name	Description							
	0b	Tiling Disabled (Linear Blit)									
1b	Tiling Enabled	[CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.									
10:8	<b>Pattern Vertical Seed</b> Starting scan line of the 8x8 pattern corresponding to DST Y=0.										
7:0	<b>DWord Length</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0Ah</td> </tr> </table>	Default Value:	0Ah							
Default Value:	0Ah										
1 BR13	31	<b>Reserved</b>									
	30	<b>Clipping Enabled</b>									
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 45%;">Value</th> <th style="width: 55%;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disabled</td> </tr> <tr> <td>1b</td> <td>Enabled</td> </tr> </tbody> </table>	Value	Name	0b	Disabled	1b	Enabled			
		Value	Name								
	0b	Disabled									
	1b	Enabled									
	29:26	<b>Reserved</b>									
25:24	<b>Color Depth</b>										
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 30%;">Value</th> <th style="width: 70%;">Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>8 Bit Color</td> </tr> <tr> <td>01b</td> <td>16 Bit Color(565)</td> </tr> <tr> <td>10b</td> <td>16 Bit Color(1555)</td> </tr> <tr> <td>11b</td> <td>32 Bit Color</td> </tr> </tbody> </table>	Value	Name	00b	8 Bit Color	01b	16 Bit Color(565)	10b	16 Bit Color(1555)	11b	32 Bit Color
	Value	Name									
	00b	8 Bit Color									
	01b	16 Bit Color(565)									
10b	16 Bit Color(1555)										
11b	32 Bit Color										
23:16	<b>Raster Operation</b>										
15:0	<b>Destination Pitch in DWords</b> 2's complement For Tiled surfaces (bit_15 enabled) this pitch is of 512Byte granularity for Tile-X, 128B granularity for Tile-Y and can be upto 128Kbytes (or 32KDwords).										
2 BR22	31:16	<b>Destination Y1 Coordinate (Top)</b> 16 bit signed number.									
	15:0	<b>Destination X1 Coordinate (Left)</b> 16 bit signed number.									
3 BR23	31:16	<b>Destination Y2 Coordinate (Bottom)</b> 16 bit signed number.									
	15:0	<b>Destination X2 Coordinate (Right)</b> 16 bit signed number.									
4 BR09	31:0	<b>Destination Base Address</b>									
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 35%;">Format:</td> <td>GraphicsAddress[31:0]</td> </tr> </table> <p>Base address of the destination surface: X=0, Y=0. Lower 32bits of the 48bit addressing. When Tiling is enabled (Bit_11 enabled), this address is limited to 4Kbytes. When Tiling is not enabled, this address should be CL (64byte) aligned.</p>	Format:	GraphicsAddress[31:0]							
Format:	GraphicsAddress[31:0]										

<b>XY_FULL_BLT</b>		
5 BR27	31:16	<b>Reserved</b> Format: _____ MBZ Should be programmed all 0's for 48bit addressing.
	15:0	<b>Destination Base Address High</b> Format: _____ GraphicsAddress[47:32] Should be programmed with the upper 16bits of the 48bit addressing.
6 BR11	31:16	<b>Reserved</b> Format: _____ MBZ Should be programmed all 0's for 48bit addressing.
	15:0	<b>Source Pitch (double word aligned and signed) and in DWords</b> 2's complement. For Tiled Src (bit 15 enabled) this pitch is of 512Byte granularity for Tile-X, 128B granularity for Tile-Y and can be upto 128Kbytes (or 32KDwords).
7 BR26	31:16	<b>Source Y1 Coordinate (Top)</b> 16 bit signed number.
	15:0	<b>Source X1 Coordinate (Left)</b> 16 bit signed number.
8 BR12	31:0	<b>Source Address</b> Format: _____ GraphicsAddress[31:0] Base address of the destination surface: X=0, Y=0. Lower 32bits of the 48bit addressing. When Tiling is enabled (Bit_15 enabled), this address is limited to 4Kbytes. When Tiling is not enabled, this address should be CL(64byte) aligned.
9 BR28	31:16	<b>Reserved</b> Format: _____ MBZ Should be programmed all 0's for 48bit addressing.
	15:0	<b>Source Address High</b> Format: _____ GraphicsAddress[47:32] Should be programmed with the upper 16bits of the 48bit addressing.
10 BR15	31:0	<b>Pattern Base Address</b> Format: _____ GraphicsAddress[31:0] (28:06 are implemented ) (Note no NPO2 change here). Lower 32bits of the 48bit addressing. The pattern data must be located in linear memory. The Pattern Base Address programmed, must always be Cache Line (64byte) aligned.
11 BR29	31:16	<b>Reserved</b> Format: _____ MBZ Should be programmed all 0's for 48bit addressing.
	15:0	<b>Pattern Base Address High</b> Format: _____ GraphicsAddress[47:32] Should be programmed with the upper 16bits of the 48bit addressing.

## XY\_FULL\_IMMEDIATE\_PATTERN\_BLT

XY_FULL_IMMEDIATE_PATTERN_BLT			
Project:	CHV, BSW		
Source:	BlitterCS		
Length Bias:	2		
<p>The full BLT is the most comprehensive BLT instruction. It provides the ability to specify all 3 operands: destination, source, and pattern. The source and immediate pattern operands are the same bit width as the destination operand. The immediate data sizes are 64 bytes (16 DWs), 128 bytes (32 DWs), or 256 (64 DWs) for 8, 16, and 32 bpp color patterns. DWL indicates the total number of Dwords of immediate data.</p> <p>The source and destination operands may overlap, which means that the X and Y directions can be either forward or backwards. The BLT Engine takes care of all situations. The base addresses plus the X and Y coordinates determine if there is an overlap between the source and destination operands. If the base addresses of the source and destination are the same and the Source X1 is less than Destination X1, then the BLT Engine performs the accesses in the X-backwards access pattern. There is no need to look for an actual overlap. If the base addresses are the same and Source Y1 is less than Destination Y1, then the scan line accesses start at Destination Y2 with the corresponding source scan line and the strides are subtracted for every scan line access. All scan lines and pixels that fall within the ClipRect Y and X coordinates are written. Only pixels within the ClipRectX coordinates and the Destination X coordinates are written using the raster operation.</p> <p>The Pattern Seeds correspond to Destination X = 0 (horizontal) and Y = 0 (vertical). The alignment is relative to the destination coordinates. The pixel of the pattern used / scan line is the (destination X coordinate + horizontal seed) modulo 8. The scan line of the pattern used is the (destination Y coordinate + vertical seed) modulo 8.</p>			
DWord	Bit	Description	
0  BR00	31:29	<b>Client</b>	
		Default Value:	02h 2D Processor
		Format:	Opcode
	28:22	<b>Instruction Target(Opcode)</b>	
		Default Value:	74h
		Format:	Opcode
	21:20	<b>32bpp Byte Mask</b>	
		This field is only used for 32bpp.	
		<b>Value</b>	<b>Name</b>
		00b	[Default]
1xb		Write Alpha Channel	
	x1b	Write RGB Channel	
19:16	<b>Reserved</b>		
	Format:	MBZ	
15	<b>Src Tiling Enable</b>		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0b	Tiling Disabled (Linear)	

<b>XY_FULL_IMMEDIATE_PATTERN_BLT</b>			
		1b	Tiling Enabled [CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.
	14:12	<b>Pattern Horizontal Seed</b> (pixel of the scan line to start on corresponding to DST X=0)	
	11	<b>Dest Tiling Enable</b>	
		<b>Value</b>	<b>Name</b>
		0b	Tiling Disabled (Linear Blit)
		1b	Tiling Enabled [CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.
	10:8	<b>Pattern Vertical Seed</b> Starting scan line of the 8x8 pattern corresponding to DST Y=0.	
	7:0	<b>DWord Length</b>	
		Default Value:	08h Excludes DWORD 0,1
		08 + DWL = (Number of Immediate double words)h	
1 BR13	31	<b>Reserved</b>	
		Format:	MBZ
	30	<b>Clipping Enabled</b>	
		<b>Value</b>	<b>Name</b>
		0b	Disabled
		1b	Enabled
	29:26	<b>Reserved</b>	
		Format:	MBZ
25:24	<b>Color Depth</b>		
	<b>Value</b>	<b>Name</b>	
	00b	8 Bit Color	
	01b	16 Bit Color(565)	
	10b	16 Bit Color(1555)	
	11b	32 Bit Color	
23:16	<b>Raster Operation</b>		
	15:0	<b>Destination Pitch in DWords</b> 2's complement For Tiled surfaces (bit_15 enabled) this pitch is of 512Byte granularity for Tile-X, 128B granularity for Tile-Y and can be upto 128Kbytes (or 32KDwords).	
2 BR22	31:16	<b>Destination Y1 Coordinate (Top)</b> 16 bit signed number.	
	15:0	<b>Destination X1 Coordinate (Left)</b> 16 bit signed number.	
3 BR23	31:16	<b>Destination Y2 Coordinate (Bottom)</b> 16 bit signed number.	
	15:0	<b>Destination X2 Coordinate (Right)</b>	

<b>XY_FULL_IMMEDIATE_PATTERN_BLT</b>				
		16 bit signed number.		
4 BR9	31:0	<p><b>Destination Base Address</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[31:0]</td> </tr> </table> <p>Base address of the destination surface: X=0, Y=0. Lower 32bits of the 48bit addressing. When Tiling is enabled (Bit_11 enabled), this address is limited to 4Kbytes. When Tiling is not enabled, this address should be CL (64byte) aligned.</p>	Format:	GraphicsAddress[31:0]
Format:	GraphicsAddress[31:0]			
5 BR27	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table> <p>Should be programmed all 0's for 48bit addressing.</p>	Format:	MBZ
Format:	MBZ			
	15:0	<p><b>Destination Base Address High</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>Should be programmed with the upper 16bits of the 48bit addressing.</p>	Format:	GraphicsAddress[47:32]
Format:	GraphicsAddress[47:32]			
6 BR11	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table> <p>Should be programmed all 0's for 48bit addressing.</p>	Format:	MBZ
Format:	MBZ			
	15:0	<p><b>Source Pitch (double word aligned and signed) and in DWords</b></p> <p>2's complement. For Tiled Src (bit 15 enabled) this pitch is of 512Byte granularity for Tile-X, 128B granularity for Tile-Y and can be upto 128Kbytes (or 32KDwords).</p>		
7 BR26	31:16	<p><b>Source Y1 Coordinate (Top)</b></p> <p>16 bit signed number.</p>		
	15:0	<p><b>Source X1 Coordinate (Left)</b></p> <p>16 bit signed number.</p>		
8 BR12	31:0	<p><b>Source Address</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[31:0]</td> </tr> </table> <p>Base address of the destination surface: X=0, Y=0. Lower 32bits of the 48bit addressing. When Src Tiling is enabled (Bit_15 enabled), this address is limited to 4Kbytes. When Tiling is not enabled, this address should be CL (64byte) aligned.</p>	Format:	GraphicsAddress[31:0]
Format:	GraphicsAddress[31:0]			
9 BR28	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table> <p>Should be programmed all 0's for 48bit addressing.</p>	Format:	MBZ
Format:	MBZ			
	15:0	<p><b>Source Address High</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>Should be programmed with the upper 16bits of the 48bit addressing.</p>	Format:	GraphicsAddress[47:32]
Format:	GraphicsAddress[47:32]			
10..n	31:0	<b>Immediate Data 0</b>		

## XY\_FULL\_MONO\_PATTERN\_BLT

<b>XY_FULL_MONO_PATTERN_BLT</b>			
Project:	CHV, BSW		
Source:	BlitterCS		
Length Bias:	2		
<p>The full BLT is the most comprehensive BLT instruction. It provides the ability to specify all 3 operands: destination, source, and pattern. The pattern operand is monochrome and the source operand is the same bit width as the destination operand.</p> <p>The source and destination operands may overlap, which means that the X and Y directions can be either forward or backwards. The BLT Engine takes care of all situations. The base addresses plus the X and Y coordinates determine if there is an overlap between the source and destination operands. If the base addresses of the source and destination are the same and the Source X1 is less than Destination X1, then the BLT Engine performs the accesses in the X-backwards access pattern. There is no need to look for an actual overlap. If the base addresses are the same and Source Y1 is less than Destination Y1, then the scan line accesses start at Destination Y2 with the corresponding source scan line and the strides are subtracted for every scan line access. The monochrome pattern transparency mode indicates whether to use the pattern background color or de-assert the write enables when the bit in the source is 0. When the source bit is 1, then the pattern foreground color is used in the ROP operation.</p> <p>All scan lines and pixels that fall within the ClipRect Y and X coordinates are written. Only pixels within the ClipRectX coordinates and the Destination X coordinates are written using the raster operation.</p> <p>The Pattern Seeds correspond to Destination X = 0 (horizontal) and Y = 0 (vertical). The alignment is relative to the destination coordinates. The pixel of the pattern used / scan line is the (destination X coordinate + horizontal seed) modulo 8. The scan line of the pattern used is the (destination Y coordinate + vertical seed) modulo 8.</p> <p>Setting both Solid Pattern Select = 1 and Mono Pattern Transparency = 1 is mutually exclusive. The device implementation results in NO PIXELS DRAWN.</p>			
DWord	Bit	Description	
0  BR00	31:29	<b>Client</b>	
		Default Value:	02h 2D Processor
		Format:	Opcode
	28:22	<b>Instruction Target(Opcode)</b>	
		Default Value:	57h
		Format:	Opcode
	21:20	<b>32bpp Byte Mask</b>	
		This field is only used for 32bpp.	
		<b>Value</b>	<b>Name</b>
		00b	[Default]
1xb		Write Alpha Channel	
x1b	Write RGB Channel		
19:16	<b>Reserved</b>		

<b>XY_FULL_MONO_PATTERN_BLT</b>											
	15	<b>Src Tiling Enable</b> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Tiling Disabled (Linear Blit)</td> <td></td> </tr> <tr> <td>1b</td> <td>Tiling Enabled</td> <td>[CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.</td> </tr> </tbody> </table>	Value	Name	Description	0b	Tiling Disabled (Linear Blit)		1b	Tiling Enabled	[CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.
	Value	Name	Description								
	0b	Tiling Disabled (Linear Blit)									
	1b	Tiling Enabled	[CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.								
	14:12	<b>Pattern Horizontal Seed</b> (pixel of the scan line to start on corresponding to DST X=0)									
	11	<b>Dest Tiling Enable</b> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Tiling Disabled (Linear Blit)</td> <td></td> </tr> <tr> <td>1b</td> <td>Tiling Enabled</td> <td>[CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.</td> </tr> </tbody> </table>	Value	Name	Description	0b	Tiling Disabled (Linear Blit)		1b	Tiling Enabled	[CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.
	Value	Name	Description								
	0b	Tiling Disabled (Linear Blit)									
	1b	Tiling Enabled	[CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.								
	10:8	<b>Pattern Vectical Seed</b> Starting scan line of the 8x8 pattern corresponding to DST Y=0.									
7:0	<b>DWord Length</b> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0Ch</td> <td></td> </tr> </tbody> </table>	Value	Name	0Ch							
Value	Name										
0Ch											
1 BR13	31	<b>Solid Pattern Select</b> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>No Solid Pattern</td> </tr> <tr> <td>1</td> <td>Solid Pattern</td> </tr> </tbody> </table>	Value	Name	0	No Solid Pattern	1	Solid Pattern			
	Value	Name									
	0	No Solid Pattern									
	1	Solid Pattern									
	30	<b>Clipping Enabled</b> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disabled</td> </tr> <tr> <td>1b</td> <td>Enabled</td> </tr> </tbody> </table>	Value	Name	0b	Disabled	1b	Enabled			
	Value	Name									
	0b	Disabled									
1b	Enabled										
29	<b>Reserved</b> Format: MBZ										
28:27	<b>Mono Source Transparency Mode</b> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Use Background</td> </tr> <tr> <td>1</td> <td>Transparency Enabled</td> </tr> </tbody> </table>	Value	Name	0	Use Background	1	Transparency Enabled				
Value	Name										
0	Use Background										
1	Transparency Enabled										
26	<b>Reserved</b>										
25:24	<b>Color Depth</b> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>8 Bit Color</td> </tr> <tr> <td>01b</td> <td>16 Bit Color(565)</td> </tr> <tr> <td>10b</td> <td>16 Bit Color(1555)</td> </tr> <tr> <td>11b</td> <td>32 Bit Color</td> </tr> </tbody> </table>	Value	Name	00b	8 Bit Color	01b	16 Bit Color(565)	10b	16 Bit Color(1555)	11b	32 Bit Color
Value	Name										
00b	8 Bit Color										
01b	16 Bit Color(565)										
10b	16 Bit Color(1555)										
11b	32 Bit Color										



<b>XY_FULL_MONO_PATTERN_BLT</b>				
	23:16	<b>Raster Operation</b>		
	15:0	<b>Destination Pitch in DWords</b> 2's complement For Tiled surfaces (bit_11 enabled) this pitch is of 512Byte granularity for Tile-X, 128B granularity for Tile-Y and can be upto 128Kbytes (or 32KDwords).		
2	31:16	<b>Destination Y1 Coordinate (Top)</b> 16 bit signed number.		
BR22	15:0	<b>Destination X1 Coordinate (Left)</b> 16 bit signed number.		
3	31:16	<b>Destination Y2 Coordinate (Bottom)</b> 16 bit signed number.		
BR23	15:0	<b>Destination X2 Coordinate (Right)</b> 16 bit signed number.		
4	31:0	<b>Destination Base Address</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;"></td><td>GraphicsAddress[31:0]</td></tr></table> Base address of the destination surface: X=0, Y=0. Lower 32bits of the 48bit addressing. When Tiling is enabled (Bit_11 enabled), this address is limited to 4Kbytes. When Tiling is not enabled, this address should be CL (64byte) aligned.		GraphicsAddress[31:0]
	GraphicsAddress[31:0]			
5	31:16	<b>Reserved</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;"></td><td>MBZ</td></tr></table> Should be programmed all 0's for 48bit addressing.		MBZ
	MBZ			
BR27	15:0	<b>Destination Base Address High</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;"></td><td>GraphicsAddress[47:32]</td></tr></table> Should be programmed with the upper 16bits of the 48bit addressing.		GraphicsAddress[47:32]
	GraphicsAddress[47:32]			
6	31:16	<b>Reserved</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;"></td><td>MBZ</td></tr></table>		MBZ
	MBZ			
BR11	15:0	<b>Source Pitch (double word aligned and signed) and in DWords</b> 2's complement. For Tiled Src (bit 15 enabled) this pitch is of 512Byte granularity for Tile-X, 128B granularity for Tile-Y and can be upto 128Kbytes (or 32KDwords).		
7	31:16	<b>Source Y1 Coordinate (Top)</b> 16 bit signed number.		
BR26	15:0	<b>Source X1 Coordinate (Left)</b> 16 bit signed number.		
8	31:0	<b>Source Address</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;"></td><td>GraphicsAddress[31:0]</td></tr></table> (base address of the source surface: X=0, Y=0). Lower 32bits of the 48bit addressing. When Src Tiling is enabled (Bit 15 enabled), this address is limited to 4Kbytes. When Tiling is not enabled, this address should be CL (64byte) aligned.		GraphicsAddress[31:0]
	GraphicsAddress[31:0]			
BR12				

<b>XY_FULL_MONO_PATTERN_BLT</b>				
9  BR28	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table> <p>Should be programmed all 0's for 48bit addressing.</p>	Format:	MBZ
	Format:	MBZ		
15:0	<p><b>Source Address High</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>Should be programmed with the upper 16bits of the 48bit addressing.</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			
10  BR16	31:0	<p><b>Pattern Background Color</b></p> <p>8 bit = [7:0], 16 bit = [15:0], 32 bit = [31:0]</p>		
11  BR17	31:0	<p><b>Pattern Foreground Color</b></p> <p>8 bit = [7:0], 16 bit = [15:0], 32 bit = [31:0]</p>		
12  BR20	31:0	<p><b>Pattern Data 0</b></p> <p>(least significant DW)</p>		
13  BR21	31:0	<p><b>Pattern Data 1</b></p> <p>(most significant DW)</p>		

## XY\_FULL\_MONO\_PATTERN\_MONO\_SRC\_BLT

<b>XY_FULL_MONO_PATTERN_MONO_SRC_BLT</b>			
Project:	CHV, BSW		
Source:	BlitterCS		
Length Bias:	2		
<p>The full BLT provides the ability to specify all 3 operands: destination, source, and pattern. The pattern and source operands are monochrome.</p> <p>The monochrome source transparency mode indicates whether to use the source background color or de-assert the write enables when the bit in the source is 0. When the source bit is 1, then the source foreground color is used in the ROP operation.</p> <p>All non-text monochrome sources are word aligned. At the end of a scan line the monochrome source, the remaining bits until the next word boundary are ignored. The Monochrome source data bit position field [2:0] indicates which bit position within the first byte should be used as the first source pixel which corresponds to the destination X1 coordinate.</p> <p>The monochrome pattern transparency mode indicates whether to use the pattern background color or de-assert the write enables when the bit in the pattern is 0. When the source bit is 1, then the pattern foreground color is used in the ROP operation. The monochrome source transparency mode works identical to the pattern transparency mode.</p> <p>All scan lines and pixels that fall within the ClipRect Y and X coordinates are written. Only pixels within the ClipRectX coordinates and the Destination X coordinates are written using the raster operation.</p> <p>The Pattern Seeds correspond to Destination X = 0 (horizontal) and Y = 0 (vertical). The alignment is relative to the destination coordinates. The pixel of the pattern used / scan line is the (destination X coordinate + horizontal seed) modulo 8. The scan line of the pattern used is the (destination Y coordinate + vertical seed) modulo 8.</p> <p>Setting both Solid Pattern Select = 1 and Mono Pattern Transparency = 1 is mutually exclusive. The device implementation results in NO PIXELS DRAWN.</p> <p>Negative Stride (= Pitch) is NOT ALLOWED.</p>			
DWord	Bit	Description	
0  BR00	31:29	<b>Client</b>	
		Default Value:	02h 2D Processor
		Format:	Opcode
	28:22	<b>Instruction Target(Opcode)</b>	
		Default Value:	58h
		Format:	Opcode
	21:20	<b>32bpp Byte Mask</b>	
		This field is only used for 32bpp.	
		<b>Value</b>	<b>Name</b>
		00b	<b>[Default]</b>
1xb		Write Alpha Channel	
x1b	Write RGB Channel		
19:17	<b>Monochrome source data bit position of the first pixel within a byte per scan line.</b>		

<b>XY_FULL_MONO_PATTERN_MONO_SRC_BLT</b>											
	16:15	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ							
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10:8	<b>Pattern Vertical Seed</b> Starting scan line of the 8x8 pattern corresponding to DST Y = 0.										
7:0	<b>DWord Length</b> <table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>0Ch</td> <td></td> </tr> </tbody> </table>	Value	Name	0Ch							
Value	Name										
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1 BR13	31	<b>Solid Pattern Select</b> <table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 30%;">Value</th> <th style="width: 70%;">Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>No Solid Pattern</td> </tr> <tr> <td>1</td> <td>Solid Pattern</td> </tr> </tbody> </table>	Value	Name	0	No Solid Pattern	1	Solid Pattern			
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	30	<b>Clipping Enabled</b> <table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 45%;">Value</th> <th style="width: 55%;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disabled</td> </tr> <tr> <td>1b</td> <td>Enabled</td> </tr> </tbody> </table>	Value	Name	0b	Disabled	1b	Enabled			
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	Value	Name									
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Value	Name										
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27:26	<b>Reserved</b>										
25:24	<b>Color Depth</b> <table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 35%;">Value</th> <th style="width: 65%;">Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>8 Bit Color</td> </tr> <tr> <td>01b</td> <td>16 Bit Color(565)</td> </tr> <tr> <td>10b</td> <td>16 Bit Color(1555)</td> </tr> <tr> <td>11b</td> <td>32 Bit Color</td> </tr> </tbody> </table>	Value	Name	00b	8 Bit Color	01b	16 Bit Color(565)	10b	16 Bit Color(1555)	11b	32 Bit Color
Value	Name										
00b	8 Bit Color										
01b	16 Bit Color(565)										
10b	16 Bit Color(1555)										
11b	32 Bit Color										

<b>XY_FULL_MONO_PATTERN_MONO_SRC_BLT</b>				
	23:16	<b>Raster Operation</b>		
	15:0	<b>Destination Pitch in DWords</b> 2's complement For Tiled surfaces (bit_11 enabled) this pitch is of 512Byte granularity for Tile-X, 128B granularity for Tile-Y and can be upto 128Kbytes (or 32KDwords).		
2 BR22	31:16	<b>Destination Y1 Coordinate (Top)</b> 16 bit signed number.		
	15:0	<b>Destination X1 Coordinate (Left)</b> 16 bit signed number.		
3 BR23	31:16	<b>Destination Y2 Coordinate (Bottom)</b> 16 bit signed number.		
	15:0	<b>Destination X2 Coordinate (Right)</b> 16 bit signed number.		
4 BR09	31:0	<b>Destination Base Address</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;"></td><td>GraphicsAddress[31:0]</td></tr></table> Base address of the destination surface: X=0, Y=0. Lower 32bits of the 48bit addressing. When Tiling is enabled (Bit_11 enabled), this address is limited to 4Kbytes. When Tiling is not enabled, this address should be CL (64byte) aligned.		GraphicsAddress[31:0]
		GraphicsAddress[31:0]		
15:0	<b>Destination Base Address High</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;"></td><td>GraphicsAddress[47:32]</td></tr></table> Should be programmed with the upper 16bits of the 48bit addressing.		GraphicsAddress[47:32]	
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6 BR12	31:0	<b>Mono Source Address</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;"></td><td>GraphicsAddress[31:0]</td></tr></table> (address corresponds to DST X1, Y1) (Note no NPO2 change here). Lower 32bits of the 48bit addressing. This Monosource Base Address programmed, must always be Cache Line (64byte) aligned.		GraphicsAddress[31:0]
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15:0	<b>Mono Source Address High</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;"></td><td>GraphicsAddress[47:32]</td></tr></table> Should be programmed with the upper 16bits of the 48bit addressing.		GraphicsAddress[47:32]	
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8 BR18	31:0	<b>Source Background Color</b> 8 bit = [7:0], 16 bit = [15:0], 32 bit = [31:0]		

<b>XY_FULL_MONO_PATTERN_MONO_SRC_BLT</b>		
9 BR19	31:0	<b>Source Foreground Color</b> 8 bit = [7:0], 16 bit = [15:0], 32 bit = [31:0]
10 BR16	31:0	<b>Pattern Background Color</b> 8 bit = [7:0], 16 bit = [15:0], 32 bit = [31:0]
11 BR17	31:0	<b>Pattern Foreground Color</b> 8 bit = [7:0], 16 bit = [15:0], 32 bit = [31:0]
12 BR20	31:0	<b>Pattern Data 0</b> (least significant DW)
13 BR21	31:0	<b>Pattern Data 1</b> (most significant DW)

## XY\_FULL\_MONO\_SRC\_BLT

<b>XY_FULL_MONO_SRC_BLT</b>			
Project:	CHV, BSW		
Source:	BlitterCS		
Length Bias:	2		
<p>The full BLT is the most comprehensive BLT instruction. It provides the ability to specify all 3 operands: destination, source, and pattern. The source operand is monochrome and the pattern operand is the same bit width as the destination.</p> <p>The monochrome source transparency mode indicates whether to use the source background color or de-assert the write enables when the bit in the source is 0. When the source bit is 1, then the source foreground color is used in the ROP operation.</p> <p>All non-text and non-immediate monochrome sources are word aligned. At the end of a scan line the monochrome source, the remaining bits until the next word boundary are ignored. The Monochrome source data bit position field [2:0] indicates which bit position within the first byte should be used as the first source pixel which corresponds to the Destination X1 coordinate.</p> <p>All scan lines and pixels that fall within the ClipRect Y and X coordinates are written. Only pixels within the ClipRectX coordinates and the Destination X coordinates are written using the raster operation.</p> <p>The Pattern Seeds correspond to Destination X = 0 (horizontal) and Y = 0 (vertical). The alignment is relative to the destination coordinates. The pixel of the pattern used / scan line is the (destination X coordinate + horizontal seed) modulo 8. The scan line of the pattern used is the (destination Y coordinate + vertical seed) modulo 8.</p> <p>Negative Stride (= Pitch) is NOT ALLOWED</p>			
DWord	Bit	Description	
0  BR00	31:29	<b>Client</b>	
		Default Value:	02h 2D Processor
		Format:	Opcode
	28:22	<b>Instruction Target(Opcode)</b>	
		Default Value:	56h
		Format:	Opcode
	21:20	<b>32bpp Byte Mask</b>	
		This field is only used for 32bpp.	
		<b>Value</b>	<b>Name</b>
		00b	<b>[Default]</b>
1xb		Write Alpha Channel	
x1b	Write RGB Channel		
19:17	<b>Monochrome source data bit position of the first pixel within a byte per scan line.</b>		
16:15	<b>Reserved</b>		
	Format:	MBZ	
14:12	<b>Pattern Horizontal Seed</b> (pixel of the scan line to start on corresponding to DST X=0)		

<b>XY_FULL_MONO_SRC_BLT</b>											
	11	<b>Tiling Enable</b>									
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1b	Tiling Enabled	[CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.									
10:8	<b>Pattern Vertical Seed</b> Starting scan line of the 8x8 pattern corresponding to DST Y = 0.										
	7:0	<b>DWord Length</b>									
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0Ah</td> <td></td> </tr> </tbody> </table>	Value	Name	0Ah						
Value	Name										
0Ah											
1 BR13	31	<b>Reserved</b>									
		Format: _____ MBZ									
	30	<b>Clipping Enabled</b>									
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29	<b>Mono Source Transparency Mode</b>										
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Use Background</td> </tr> <tr> <td>1</td> <td>Transparency Enabled</td> </tr> </tbody> </table>	Value	Name	0	Use Background	1	Transparency Enabled				
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28:26	<b>Reserved</b>										
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25:24	<b>Color Depth</b>										
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23:16	<b>Raster Operation</b>										
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2 BR22	31:16	<b>Destination Y1 Coordinate (Top)</b> 16 bit signed number.									
	15:0	<b>Destination X1 Coordinate (Left)</b> 16 bit signed number.									
3	31:16	<b>Destination Y2 Coordinate (Bottom)</b> 16 bit signed number.									



<b>XY_FULL_MONO_SRC_BLT</b>				
BR23	15:0	<b>Destination X2 Coordinate (Right)</b> 16 bit signed number.		
4 BR09	31:0	<b>Destination Base Address</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;"> </td><td>GraphicsAddress[31:0]</td></tr></table> Base address of the destination surface: X=0, Y=0. Lower 32bits of the 48bit addressing. When Tiling is enabled (Bit_11 enabled), this address is limited to 4Kbytes. When Tiling is not enabled, this address should be CL (64byte) aligned.		GraphicsAddress[31:0]
	GraphicsAddress[31:0]			
5 BR27	31:16	<b>Reserved</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;"> </td><td>MBZ</td></tr></table> Should be programmed all 0's for 48bit addressing.		MBZ
	MBZ			
	15:0	<b>Destination Base Address High</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;"> </td><td>GraphicsAddress[47:32]</td></tr></table> Should be programmed with the upper 16bits of the 48bit addressing.		GraphicsAddress[47:32]
	GraphicsAddress[47:32]			
6 BR12	31:0	<b>Mono Source Address</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;"> </td><td>GraphicsAddress[31:0]</td></tr></table> (address corresponds to DST X1, Y1) (Note no NPO2 change here). Lower 32bits of the 48bit addressing. This Monosource Base Address programmed, must always be Cache Line (64byte) aligned.		GraphicsAddress[31:0]
	GraphicsAddress[31:0]			
7 BR28	31:16	<b>Reserved</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;"> </td><td>MBZ</td></tr></table> Should be programmed all 0's for 48bit addressing.		MBZ
	MBZ			
	15:0	<b>Mono Source Address High</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;"> </td><td>GraphicsAddress[47:32]</td></tr></table> Should be programmed with the upper 16bits of the 48bit addressing.		GraphicsAddress[47:32]
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8 BR18	31:0	<b>Source Background Color</b> 8 bit = [7:0], 16 bit = [15:0], 32 bit = [31:0]		
9 BR19	31:0	<b>Source Foreground Color</b> 8 bit = [7:0], 16 bit = [15:0], 32 bit = [31:0]		
10 BR15	31:0	<b>Pattern Base Address</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;"> </td><td>GraphicsAddress[31:0]</td></tr></table> (28:06 are implemented ) (Note no NPO2 change here). Lower 32bits of the 48bit addressing. The pattern data must be located in linear memory. The Pattern Base Address programmed, must always be Cache Line (64byte) aligned.		GraphicsAddress[31:0]
	GraphicsAddress[31:0]			

<b>XY_FULL_MONO_SRC_BLT</b>				
11  BR29	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table> <p>Should be programmed all 0's for 48bit addressing.</p>	Format:	MBZ
	Format:	MBZ		
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Format:	GraphicsAddress[47:32]			

## XY\_FULL\_MONO\_SRC\_IMMEDIATE\_PATTERN\_BLT

XY_FULL_MONO_SRC_IMMEDIATE_PATTERN_BLT			
Project:	CHV, BSW		
Source:	BlitterCS		
Length Bias:	2		
<p>The full BLT is the most comprehensive BLT instruction. It provides the ability to specify all 3 operands: destination, source, and pattern. The source operand is a monochrome and the immediate pattern operand is the same bit width as the destination. The immediate data sizes are 64 bytes (16 DWs), 128 bytes (32 DWs), or 256 (64DWs) for 8, 16, and 32 bpp color patterns. The monochrome source transparency mode indicates whether to use the source background color or de-assert the write enables when the bit in the source is 0. When the source bit is 1, then the source foreground color is used in the ROP operation. All non-text monochrome sources are word aligned. At the end of a scan line the monochrome source, the remaining bits until the next word boundary are ignored. The Monochrome source data bit position field [2:0] indicates which bit position within the first byte should be used as the first source pixel which corresponds to the destination X1 coordinate. All scan lines and pixels that fall within the ClipRect Y and X coordinates are written. Only pixels within the ClipRectX coordinates and the Destination X coordinates are written using the raster operation. The Pattern Seeds correspond to Destination X = 0 (horizontal) and Y = 0 (vertical). The alignment is relative to the destination coordinates. The pixel of the pattern used / scan line is the (destination X coordinate + horizontal seed) modulo 8. The scan line of the pattern used is the (destination Y coordinate + vertical seed) modulo 8. Negative Stride (= Pitch) is NOT ALLOWED.</p>			
DWord	Bit	Description	
0  BR00	31:29	<b>Client</b>	
		Default Value:	02h 2D Processor
		Format:	Opcode
	28:22	<b>Instruction Target(Opcode)</b>	
		Default Value:	75h
		Format:	Opcode
	21:20	<b>32bpp Byte Mask</b>	
		This field is only used for 32bpp.	
		<b>Value</b>	<b>Name</b>
		00b	<b>[Default]</b>
1xb		Write Alpha Channel	
x1b	Write RGB Channel		
19:17	<b>Monochrome source data bit position of the first pixel within a byte per scan line.</b>		
16:15	<b>Reserved</b>		
	Format:	MBZ	
14:12	<b>Pattern Horizontal Seed</b> (pixel of the scan line to start on corresponding to DST X=0)		

<b>XY_FULL_MONO_SRC_IMMEDIATE_PATTERN_BLT</b>											
	11	<b>Tiling Enable</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 40%;">Name</th> <th style="width: 45%;">Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Tiling Disabled (Linear Blit)</td> <td></td> </tr> <tr> <td>1b</td> <td>Tiling Enabled</td> <td>[CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.</td> </tr> </tbody> </table>	Value	Name	Description	0b	Tiling Disabled (Linear Blit)		1b	Tiling Enabled	[CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.
	Value	Name	Description								
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10:8	<b>Pattern Vertical Seed</b> Starting scan line of the 8x8 pattern corresponding to DST Y=0.										
7:0	<b>DWord Length</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Default Value:</td> <td>08h Excludes DWORD 0,1</td> </tr> </table> 08 + DWL = (Number of Immediate double words)h	Default Value:	08h Excludes DWORD 0,1								
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1 BR13	31	<b>Reserved</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ							
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	29	<b>Mono Source Transparency Mode</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 25%;">Value</th> <th style="width: 75%;">Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Use Background</td> </tr> <tr> <td>1</td> <td>Transparency Enabled</td> </tr> </tbody> </table>	Value	Name	0	Use Background	1	Transparency Enabled			
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Value	Name										
00b	8 Bit Color										
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23:16	<b>Raster Operation</b>										
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2 BR22	31:16	<b>Destination Y1 Coordinate (Top)</b> 16 bit signed number.									
	15:0	<b>Destination X1 Coordinate (Left)</b> 16 bit signed number.									
3	31:16	<b>Destination Y2 Coordinate (Bottom)</b> 16 bit signed number.									

<b>XY_FULL_MONO_SRC_IMMEDIATE_PATTERN_BLT</b>				
BR23	15:0	<b>Destination X2 Coordinate (Right)</b> 16 bit signed number.		
4 BR09	31:0	<b>Destination Base Address</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;">Format:</td><td>GraphicsAddress[31:0]</td></tr></table> Base address of the destination surface: X=0, Y=0. Lower 32bits of the 48bit addressing. When Tiling is enabled (Bit_11 enabled), this address is limited to 4Kbytes. When Tiling is not enabled, this address should be CL (64byte) aligned.	Format:	GraphicsAddress[31:0]
Format:	GraphicsAddress[31:0]			
5 BR27	31:16	<b>Reserved</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;">Format:</td><td>MBZ</td></tr></table> Should be programmed all 0's for 48bit addressing.	Format:	MBZ
Format:	MBZ			
	15:0	<b>Destination Base Address High</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;">Format:</td><td>GraphicsAddress[47:32]</td></tr></table> Should be programmed with the upper 16bits of the 48bit addressing.	Format:	GraphicsAddress[47:32]
Format:	GraphicsAddress[47:32]			
6 BR12	31:0	<b>Mono Source Address</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;">Format:</td><td>GraphicsAddress[31:0]</td></tr></table> (address corresponds to DST X1, Y1) (Note no NPO2 change here). Lower 32bits of the 48bit addressing. This Monosource Base Address programmed, must always be Cache Line (64byte) aligned.	Format:	GraphicsAddress[31:0]
Format:	GraphicsAddress[31:0]			
7 BR28	31:16	<b>Reserved</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;">Format:</td><td>MBZ</td></tr></table> Should be programmed all 0's for 48bit addressing.	Format:	MBZ
Format:	MBZ			
	15:0	<b>Mono Source Address High</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;">Format:</td><td>GraphicsAddress[47:32]</td></tr></table> Should be programmed with the upper 16bits of the 48bit addressing.	Format:	GraphicsAddress[47:32]
Format:	GraphicsAddress[47:32]			
8 BR18	31:0	<b>Source Background Color</b> 8 bit = [7:0], 16 bit = [15:0], 32 bit = [31:0]		
9 BR19	31:0	<b>Source Foreground Color</b> 8 bit = [7:0], 16 bit = [15:0], 32 bit = [31:0]		
10..n	31:0	<b>Immediate Data</b>		

## XY\_MONO\_PAT\_BLT

XY_MONO_PAT_BLT			
Project:	CHV, BSW		
Source:	BlitterCS		
Length Bias:	2		
<p>MONO_PAT_BLT is used when we have no source and the monochrome pattern is not trivial (is not a solid color only). The monochrome pattern is loaded from the instruction stream.</p> <p>All scan lines and pixels that fall within the ClipRect Y and X coordinates are written. Only pixels within the ClipRectX coordinates and the Destination X coordinates are written using the raster operation.</p> <p>The Pattern Seeds correspond to Destination X = 0 (horizontal) and Y = 0 (vertical). The alignment is relative to the destination coordinates. The pixel of the pattern used / scan line is the (destination X coordinate + horizontal seed) modulo 8. The scan line of the pattern used is the (destination Y coordinate + vertical seed) modulo 8.</p> <p>The monochrome pattern transparency mode indicates whether to use the pattern background color or de-assert the write enables when the bit in the pattern is 0. When the pattern bit is 1, then the pattern foreground color is used in the ROP operation.</p>			
DWord	Bit	Description	
0  BR00	31:29	<b>Client</b>	
		Default Value: 02h 2D Processor	
	Format: Opcode		
	28:22	<b>Instruction Target(Opcode)</b>	
		Default Value: 52h	
	Format: Opcode		
	21:20	<b>32bpp Byte Mask</b>	
		This field is only used for 32bpp.	
		<b>Value</b>	<b>Name</b>
		00b	[Default]
1xb		Write Alpha Channel	
x1b	Write RGB Channel		
19:15	<b>Reserved</b>		
	Format: MBZ		
14:12	<b>Pattern Horizontal Seed</b>		
Pixel of the scan line to start on corresponding to DST X=0.			
11	<b>Tiling Enable</b>		
	<b>Value</b>	<b>Name</b>	
	0b	Tiling Disabled (Linear Blit)	
1b	Tiling Enabled	[CHV, BSW]: Tile-X or Tile-Y.	
10:8	<b>Pattern Vertical Seed</b>		
Scan line of the 8x8 pattern to start on corresponding to DST Y=0.			

<b>XY_MONO_PAT_BLT</b>											
	7:0	<b>DWord Length</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">08h</td> <td></td> </tr> </tbody> </table>	Value	Name	08h						
Value	Name										
08h											
1  BR13	31	<b>Reserved</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">MBZ</td> </tr> </table>	Format:	MBZ							
	Format:	MBZ									
	30	<b>Clipping Enabled</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disabled</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enabled</td> </tr> </tbody> </table>	Value	Name	0b	Disabled	1b	Enabled			
	Value	Name									
	0b	Disabled									
	1b	Enabled									
29	<b>Reserved</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">MBZ</td> </tr> </table>	Format:	MBZ								
Format:	MBZ										
28	<b>Mono Pattern Transparency Mode</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 30%; text-align: center;">Value</th> <th style="width: 70%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">Use Background</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">Transparency Enabled</td> </tr> </tbody> </table>	Value	Name	0	Use Background	1	Transparency Enabled				
Value	Name										
0	Use Background										
1	Transparency Enabled										
27:26	<b>Reserved</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">MBZ</td> </tr> </table>	Format:	MBZ								
Format:	MBZ										
25:24	<b>Color Depth</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 30%; text-align: center;">Value</th> <th style="width: 70%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">00b</td> <td style="text-align: center;">8 Bit Color</td> </tr> <tr> <td style="text-align: center;">01b</td> <td style="text-align: center;">16 Bit Color(565)</td> </tr> <tr> <td style="text-align: center;">10b</td> <td style="text-align: center;">16 Bit Color(1555)</td> </tr> <tr> <td style="text-align: center;">11b</td> <td style="text-align: center;">32 Bit Color</td> </tr> </tbody> </table>	Value	Name	00b	8 Bit Color	01b	16 Bit Color(565)	10b	16 Bit Color(1555)	11b	32 Bit Color
Value	Name										
00b	8 Bit Color										
01b	16 Bit Color(565)										
10b	16 Bit Color(1555)										
11b	32 Bit Color										
	23:16	<b>Raster Operation</b>									
	15:0	<b>Destination Pitch in DWords</b> 2's complement For Tiled surfaces (bit_11 enabled) this pitch is of 512Byte granularity for Tile-X, 128B granularity for Tile-Y and can be upto 128Kbytes (or 32KDwords).									
2  BR22	31:16	<b>Destination Y1 Coordinate (Top)</b> 16 bit signed number.									
	15:0	<b>Destination X1 Coordinate (Left)</b> 16 bit signed number.									
3  BR23	31:16	<b>Destination Y2 Coordinate (Bottom)</b> 16 bit signed number.									
	15:0	<b>Destination X2 Coordinate (Right)</b> 16 bit signed number.									
4  BR09	31:0	<b>Destination Base Address</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 40%;">Format:</td> <td style="width: 60%;">GraphicsAddress[31:0]</td> </tr> </table>	Format:	GraphicsAddress[31:0]							
	Format:	GraphicsAddress[31:0]									

<b>XY_MONO_PAT_BLT</b>				
		Base address of the destination surface: X=0, Y=0. Lower 32bits of the 48bit addressing. When Tiling is enabled (Bit_11 enabled), this address is limited to 4Kbytes. When Tiling is not enabled, this address should be CL (64byte) aligned.		
5  BR27	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">MBZ</td> </tr> </table> <p>Should be programmed all 0's for 48bit addressing.</p>	Format:	MBZ
	Format:	MBZ		
15:0	<p><b>Destination Base Address High</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td style="width: 70%;">GraphicsAddress[47:32]</td> </tr> </table> <p>Should be programmed with the upper 16bits of the 48bit addressing.</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			
6  BR16	31:0	<p><b>Pattern Background Color</b></p> <p>8 bit = [7:0], 16 bit = [15:0], 32 bit = [31:0]</p>		
7  BR17	31:0	<p><b>Pattern Foreground Color</b></p> <p>8 bit = [7:0], 16 bit = [15:0], 32 bit = [31:0]</p>		
8  BR20	31:0	<p><b>Pattern Data 0</b></p>		
9  BR21	31:0	<p><b>Pattern Data 1</b></p>		



## XY\_MONO\_PAT\_FIXED\_BLT

XY_MONO_PAT_FIXED_BLT			
Project:	CHV, BSW		
Source:	BlitterCS		
Length Bias:	2		
<p>MONO_PAT_FIXED_BLT is used when we have no source and the monochrome pattern is not trivial (is not a solid color only). The monochrome pattern is one of 10 fixed patterns described below. The pattern seeds can still be used with the fixed patterns, creating even more fixed patterns. This eliminates 2 doublewords compared to the XY_MONO_PAT_BLT command packet.</p> <p>All scan lines and pixels that fall within the ClipRect Y and X coordinates are written. Only pixels within the ClipRectX coordinates and the Destination X coordinates are written using the raster operation.</p> <p>The Pattern Seeds correspond to Destination X = 0 (horizontal) and Y = 0 (vertical). The alignment is relative to the destination coordinates. The pixel of the pattern used / scan line is the (destination X coordinate + horizontal seed) modulo 8. The scan line of the pattern used is the (destination Y coordinate + vertical seed) modulo 8.</p> <p>The monochrome pattern transparency mode indicates whether to use the pattern background color or de-assert the write enables when the bit in the pattern is 0. When the pattern bit is 1, then the pattern foreground color is used in the ROP operation.</p>			
DWord	Bit	Description	
0  BR00	31:29	<b>Client</b>	
		Default Value:	02h 2D Processor
		Format:	Opcode
	28:22	<b>Instruction Target(Opcode)</b>	
		Default Value:	59h
		Format:	Opcode
	21:20	<b>32bpp Byte Mask</b>	
		This field is only used for 32bpp.	
		<b>Value</b>	<b>Name</b>
		00b	<b>[Default]</b>
1xb		Write Alpha Channel	
x1b	Write RGB Channel		
19	<b>Reserved</b>		
	Format:	MBZ	
18:15	<b>Fixed Pattern</b>		
	<b>Value</b>	<b>Name</b>	
	0000b	HS_HORIZONTAL	
	0001b	HS_VERTICAL	
	0010b	HS_FDIAGONAL	
0011b	HS_BDIAGONAL		

<b>XY_MONO_PAT_FIXED_BLT</b>			
	0100b	HS_CROSS	
	0101b	HS_DIAGCROSS	
	0110b	Reserved	
	0111b	Reserved	
	1000b	Screen Door	
	1001b	SD Wide	
	1010b	Walking Bit (one)	
	1011b	Walking Zero	
	1100b	Reserved	
	1101b	Reserved	
	1110b	Reserved	
	1111b	Reserved	
	14:12	<b>Pattern Horizontal Seed</b> Pixel of the scan line to start on corresponding to DST X=0.	
11	<b>Tiling Enable</b>		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0b	Tiling Disabled (Linear Blit)	
1b	Tiling Enabled	[CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.	
10:8	<b>Pattern Vertical Seed</b> Scan line of the 8x8 pattern to start on corresponding to DST Y=0.		
7:0	<b>DWord Length</b>		
	<b>Value</b>	<b>Name</b>	
06h			
1 BR13	31	<b>Reserved</b>	
		Format:	MBZ
	30	<b>Clipping Enabled</b>	
		<b>Value</b>	<b>Name</b>
		0b	Disabled
1b	Enabled		
29	<b>Reserved</b>		
Format:	MBZ		
28	<b>Mono Pattern Transparency Mode</b>		
	<b>Value</b>	<b>Name</b>	
	0	Use Background	
1	Transparency Enabled		
27:26	<b>Reserved</b>		

<b>XY_MONO_PAT_FIXED_BLT</b>			
	25:24	<b>Color Depth</b>	
		<b>Value</b>	<b>Name</b>
		00b	8 Bit Color
		01b	16 Bit Color(565)
		10b	16 Bit Color(1555)
	11b	32 Bit Color	
	23:16	<b>Raster Operation</b>	
	15:0	<b>Destination Pitch in DWords</b> 2's complement For Tiled surfaces (bit_11 enabled) this pitch is of 512Byte granularity for Tile-X, 128B granularity for Tile-Y and can be upto 128Kbytes (or 32KDwords).	
2 BR22	31:16	<b>Destination Y1 Coordinate (Top)</b> 16 bit signed number.	
	15:0	<b>Destination X1 Coordinate (Left)</b> 16 bit signed number.	
3 BR23	31:16	<b>Destination Y2 Coordinate (Bottom)</b> 16 bit signed number.	
	15:0	<b>Destination X2 Coordinate (Right)</b> 16 bit signed number.	
4 BR09	31:0	<b>Destination Base Address</b>	
		Format: GraphicsAddress[31:0] Base address of the destination surface: X=0, Y=0. Lower 32bits of the 48bit addressing. When Tiling is enabled (Bit_11 enabled), this address is limited to 4Kbytes. When Tiling is not enabled, this address should be CL (64byte) aligned.	
5 BR27	31:16	<b>Reserved</b>	
		Format: MBZ Should be programmed all 0's for 48bit addressing.	
	15:0	<b>Destination Base Address High</b>	
		Format: GraphicsAddress[47:32] Should be programmed with the upper 16bits of the 48bit addressing.	
6 BR16	31:0	<b>Pattern Background Color</b> 8 bit = [7:0], 16 bit = [15:0], 32 bit = [31:0]	
7 BR17	31:0	<b>Pattern Foreground Color</b> 8 bit = [7:0], 16 bit = [15:0], 32 bit = [31:0]	

## XY\_MONO\_SRC\_COPY\_BLT

XY_MONO_SRC_COPY_BLT			
Project:	CHV, BSW		
Source:	BlitterCS		
Length Bias:	2		
<p>This BLT instruction performs a monochrome source copy where the only operands involved is a monochrome source and destination. The source and destination operands cannot overlap therefore the X and Y directions are always forward.</p> <p>All non-text monochrome sources are word aligned. At the end of a scan line of monochrome source, all bits until the next word boundary are ignored. The monochrome source data bit position field [2:0] indicates the bit position within the first byte of the scan line that should be used as the first source pixel which corresponds to the destination X1 coordinate.</p> <p>The monochrome source transparency mode indicates whether to use the source background color or de-assert the write enables when the bit in the source is 0. When the source bit is 1, then the source foreground color is used in the ROP operation. The ROP value chosen must involve source and no pattern data in the ROP operation. Negative Stride (= Pitch) is NOT ALLOWED.</p>			
DWord	Bit	Description	
0  BR00	31:29	<b>Client</b>	
		Default Value:	02h 2D Processor
		Format:	Opcode
	28:22	<b>Instruction Target(Opcode)</b>	
		Default Value:	54h
		Format:	Opcode
	21:20	<b>32bpp Byte Mask</b>	
		This field is only used for 32bpp.	
		<b>Value</b>	<b>Name</b>
		00b	[Default]
1xb		Write Alpha Channel	
	x1b	Write RGB Channel	
19:17	<b>Monochrome source data bit position of the first pixel within a byte per scan line.</b>		
16:12	<b>Reserved</b>		
	Format:	MBZ	
11	<b>Tiling Enable</b>		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0b	Tiling Disabled (Linear Blit)	
	1b	Tiling Enabled	[CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.
10:8	<b>Reserved</b>		
	Format:	MBZ	

<b>XY_MONO_SRC_COPY_BLT</b>											
	7:0	<b>DWord Length</b>									
		<table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>08h</td> <td></td> </tr> </tbody> </table>	Value	Name	08h						
Value	Name										
08h											
1 BR13	31	<b>Reserved</b> Format: <span style="float: right;">MBZ</span>									
	30	<b>Clipping Enabled</b>									
		<table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disabled</td> </tr> <tr> <td>1b</td> <td>Enabled</td> </tr> </tbody> </table>	Value	Name	0b	Disabled	1b	Enabled			
		Value	Name								
	0b	Disabled									
	1b	Enabled									
	29	<b>Mono Source Transparency Mode</b>									
	<table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 30%;">Value</th> <th style="width: 70%;">Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Use Background</td> </tr> <tr> <td>1</td> <td>Transparency Enabled</td> </tr> </tbody> </table>		Value	Name	0	Use Background	1	Transparency Enabled			
	Value	Name									
	0	Use Background									
1	Transparency Enabled										
28:26	<b>Reserved</b> Format: <span style="float: right;">MBZ</span>										
25:24	<b>Color Depth</b>										
	<table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 30%;">Value</th> <th style="width: 70%;">Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>8 Bit Color</td> </tr> <tr> <td>01b</td> <td>16 Bit Color(565)</td> </tr> <tr> <td>10b</td> <td>16 Bit Color(1555)</td> </tr> <tr> <td>11b</td> <td>32 Bit Color</td> </tr> </tbody> </table>	Value	Name	00b	8 Bit Color	01b	16 Bit Color(565)	10b	16 Bit Color(1555)	11b	32 Bit Color
	Value	Name									
	00b	8 Bit Color									
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11b	32 Bit Color										
23:16	<b>Raster Operation</b>										
15:0	<b>Destination Pitch in DWords</b> 2's complement For Tiled surfaces (bit_11 enabled) this pitch is of 512Byte granularity for Tile-X, 128B granularity for Tile-Y and can be upto 128Kbytes (or 32KDwords).										
2 BR22	31:16	<b>Destination Y1 Coordinate (Top)</b> 16 bit signed number.									
	15:0	<b>Destination X1 Coordinate (Left)</b> 16 bit signed number.									
3 BR23	31:16	<b>Destination Y2 Coordinate (Bottom)</b> 16 bit signed number.									
	15:0	<b>Destination X2 Coordinate (Right)</b> 16 bit signed number.									
4 BR09	31:0	<b>Destination Base Address</b>									
		<table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 30%;">Format:</th> <th style="width: 70%;">GraphicsAddress[31:0]</th> </tr> </thead> <tbody> <tr> <td colspan="2">Base address of the destination surface: X=0, Y=0. Lower 32bits of the 48bit addressing. When Tiling is enabled (Bit_11 enabled), this address is limited to 4Kbytes. When Tiling is not enabled, this address should be CL (64byte) aligned.</td> </tr> </tbody> </table>	Format:	GraphicsAddress[31:0]	Base address of the destination surface: X=0, Y=0. Lower 32bits of the 48bit addressing. When Tiling is enabled (Bit_11 enabled), this address is limited to 4Kbytes. When Tiling is not enabled, this address should be CL (64byte) aligned.						
Format:	GraphicsAddress[31:0]										
Base address of the destination surface: X=0, Y=0. Lower 32bits of the 48bit addressing. When Tiling is enabled (Bit_11 enabled), this address is limited to 4Kbytes. When Tiling is not enabled, this address should be CL (64byte) aligned.											

<b>XY_MONO_SRC_COPY_BLT</b>				
5 BR27	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table> <p>Should be programmed all 0's for 48bit addressing.</p>	Format:	MBZ
	Format:	MBZ		
15:0	<p><b>Destination Base Address High</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>Should be programmed with the upper 16bits of the 48bit addressing.</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			
6 BR12	31:0	<p><b>Mono Source Address</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[31:0]</td> </tr> </table> <p>(address corresponds to DST X1, Y1) (Note no NPO2 change here). Lower 32bits of the 48bit addressing. This Monosource Base Address programmed, must always be Cache Line (64byte) aligned.</p>	Format:	GraphicsAddress[31:0]
Format:	GraphicsAddress[31:0]			
7 BR28	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table> <p>Should be programmed all 0's for 48bit addressing.</p>	Format:	MBZ
	Format:	MBZ		
15:0	<p><b>Mono Source Address High</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>Should be programmed with the upper 16bits of the 48bit addressing.</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			
8 BR18	31:0	<p><b>Source Background Color</b></p> <p>8 bit = [7:0], 16 bit = [15:0], 32 bit = [31:0]</p>		
9 BR19	31:0	<p><b>Source Foreground Color</b></p> <p>8 bit = [7:0], 16 bit = [15:0], 32 bit = [31:0]</p>		

## XY\_MONO\_SRC\_COPY\_IMMEDIATE\_BLT

XY_MONO_SRC_COPY_IMMEDIATE_BLT			
Project:	CHV, BSW		
Source:	BlitterCS		
Length Bias:	2		
<p>This instruction allows the Driver to send monochrome data through the instruction stream, eliminating the read latency of the source during command execution.</p> <p>The IMMEDIATE_BLT data MUST transfer an even number of doublewords and the exact number of quadwords. DWL indicates the total number of Dwords of immediate data.</p> <p>All non-text monochrome sources are word aligned. At the end of a scan line of monochrome source, all bits until the next word boundary are ignored. The Monochrome source data bit position field [2:0] indicates the bit position within the first byte of the scan line that should be used as the first source pixel which corresponds to the destination X1 coordinate.</p> <p>The monochrome source transparency mode indicates whether to use the source background color or de-assert the write enables when the bit in the source is 0. When the source bit is 1, then the source foreground color is used in the ROP operation. The ROP value chosen must involve source and no pattern data in the ROP operation. The monochrome source data supplied corresponds to the Destination X1 and Y1 coordinates.</p> <p>Negative Stride (= Pitch) is NOT ALLOWED.</p>			
DWord	Bit	Description	
0  BR00	31:29	<b>Client</b>	
		Default Value: 02h 2D Processor	
			Format: Opcode
	28:22	<b>Instruction Target(Opcode)</b>	
		Default Value: 71h	
			Format: Opcode
	21:20	<b>32bpp Byte Mask</b>	
		This field is only used for 32bpp.	
		<b>Value</b>	<b>Name</b>
		00b	[Default]
1xb		Write Alpha Channel	
		x1b Write RGB Channel	
19:17	<b>Monochrome source data bit position of the first pixel within a byte per scan line.</b>		
16:12	<b>Reserved</b>		
	Format: MBZ		
11	<b>Tiling Enable</b>		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0b	Tiling Disabled (Linear)	
	1b	Tiling Enabled	[CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.

<b>XY_MONO_SRC_COPY_IMMEDIATE_BLT</b>											
	10:8	<b>Reserved</b>									
	7:0	<b>DWord Length</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Default Value:</td> <td>06h Excludes DWORD 0,1</td> </tr> </table> 06 + DWL = (Number of Immediate double words)h	Default Value:	06h Excludes DWORD 0,1							
Default Value:	06h Excludes DWORD 0,1										
1  BR13	31	<b>Reserved</b>									
	30	<b>Clipping Enabled</b> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disabled</td> </tr> <tr> <td>1b</td> <td>Enabled</td> </tr> </tbody> </table>	Value	Name	0b	Disabled	1b	Enabled			
	Value	Name									
	0b	Disabled									
	1b	Enabled									
	29	<b>Mono Source Transparency Mode</b> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 30%;">Value</th> <th style="width: 70%;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Transparency Enabled</td> </tr> <tr> <td>1b</td> <td>Use Background</td> </tr> </tbody> </table>	Value	Name	0b	Transparency Enabled	1b	Use Background			
Value	Name										
0b	Transparency Enabled										
1b	Use Background										
28:26	<b>Reserved</b>										
25:24	<b>Color Depth</b> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 30%;">Value</th> <th style="width: 70%;">Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>8 Bit Color</td> </tr> <tr> <td>01b</td> <td>16 Bit Color(565)</td> </tr> <tr> <td>10b</td> <td>16 Bit Color(1555)</td> </tr> <tr> <td>11b</td> <td>32 Bit Color</td> </tr> </tbody> </table>	Value	Name	00b	8 Bit Color	01b	16 Bit Color(565)	10b	16 Bit Color(1555)	11b	32 Bit Color
Value	Name										
00b	8 Bit Color										
01b	16 Bit Color(565)										
10b	16 Bit Color(1555)										
11b	32 Bit Color										
23:16	<b>Raster Operation</b>										
	15:0	<b>Destination Pitch in DWords</b> 2's complement For Tiled surfaces (bit_11 enabled) this pitch is of 512Byte granularity for Tile-X, 128B granularity for Tile-Y and can be upto 128Kbytes (or 32KDwords).									
2  BR22	31:16	<b>Destination Y1 Coordinate (Top)</b> 16 bit signed number.									
	15:0	<b>Destination X1 Coordinate (Left)</b> 16 bit signed number.									
3  BR23	31:16	<b>Destination Y2 Coordinate (Bottom)</b> 16 bit signed number.									
	15:0	<b>Destination X2 Coordinate (Right)</b> 16 bit signed number.									
4  BR09	31:0	<b>Destination Base Address</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[31:0]</td> </tr> </table> Base address of the destination surface: X=0, Y=0. Lower 32bits of the 48bit addressing. When Tiling is enabled (Bit_11 enabled), this address is limited to 4Kbytes. When Tiling is not enabled, this address should be CL (64byte) aligned.	Format:	GraphicsAddress[31:0]							
	Format:	GraphicsAddress[31:0]									



<b>XY_MONO_SRC_COPY_IMMEDIATE_BLT</b>				
5  BR27	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">MBZ</td> </tr> </table> <p>Should be programmed all 0's for 48bit addressing.</p>	Format:	MBZ
	Format:	MBZ		
15:0	<p><b>Destination Base Address High</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td style="width: 70%;">GraphicsAddress[47:32]</td> </tr> </table> <p>Should be programmed with the upper 16bits of the 48bit addressing.</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			
6  BR18	31:0	<p><b>Source Background Color</b></p> <p>8 bit = [7:0], 16 bit = [15:0], 32 bit = [31:0]</p>		
7  BR19	31:0	<p><b>Source Foreground Color</b></p> <p>8 bit = [7:0], 16 bit = [15:0], 32 bit = [31:0]</p>		
8..n	31:0	<p><b>Immediate Data</b></p>		

## XY\_PAT\_BLT

XY_PAT_BLT			
Project:	CHV, BSW		
Source:	BlitterCS		
Length Bias:	2		
<p>PAT_BLT is used when there is no source and the color pattern is not trivial (is not a solid color only).            If clipping is enabled, all scan lines and pixels that fall within the ClipRect Y and X coordinates are written. Only pixels within the ClipRectX coordinates and the Destination X coordinates are written using the raster operation.            The Pattern Seeds correspond to Destination X = 0 (horizontal) and Y = 0 (vertical). The alignment is relative to the destination coordinates. The pixel of the pattern used / scan line is the (destination X coordinate + horizontal seed) modulo 8. The scan line of the pattern used is the (destination Y coordinate + vertical seed) modulo 8.</p>			
DWord	Bit	Description	
0  BR00	31:29	<b>Client</b>	
		Default Value:	02h 2D Processor
		Format:	Opcode
	28:22	<b>Instruction Target(Opcode)</b>	
		Default Value:	51h
		Format:	Opcode
	21:20	<b>32bpp Byte Mask</b>	
		This field is only used for 32bpp.	
		Value	Name
		00b	[Default]
1xb		Write Alpha Channel	
x1b	Write RGB Channel		
19:15	<b>Reserved</b>		
14:12	<b>Pattern Horizontal Seed</b> Pixel of the scan line to start on corresponding to DST X=0.		
11	<b>Tiling Enable</b>		
	Value	Name	
	0b	Tiling Disabled (Linear Blit)	
1b	Tiling Enabled	[CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.	
10:8	<b>Pattern Vertical Seed</b> Scan line of the 8x8 pattern to start on corresponding to DST Y=0.		
7:0	<b>DWord Length</b>		
	Default Value:	06h	
1	31	<b>Reserved</b>	

<b>XY_PAT_BLT</b>			
BR13	30	<b>Clipping Enabled</b>	
		<b>Value</b>	<b>Name</b>
		0b	Disabled
		1b	Enabled
	29:26	<b>Reserved</b>	
		Format:	MBZ
	25:24	<b>Color Depth</b>	
		<b>Value</b>	<b>Name</b>
		00b	8 Bit Color
		01b	16 Bit Color(565)
10b		16 Bit Color(1555)	
	11b	32 Bit Color	
23:16	<b>Raster Operation</b>		
15:0	<b>Destination Pitch in DWords</b> 2's complement (Negative Pitch Not allowed for Pixel nor Text) For Tiled surfaces (bit_11 enabled) this pitch is of 512Byte granularity for Tile-X, 128B granularity for Tile-Y and can be upto 128Kbytes (or 32KDwords).		
2	31:16	<b>Destination Y1 Coordinate (Top)</b> 16 bit signed number.	
BR22	15:0	<b>Destination X1 Coordinate (Left)</b> 16 bit signed number.	
3	31:16	<b>Destination Y2 Coordinate (Bottom)</b> 16 bit signed number.	
BR23	15:0	<b>Destination X2 Coordinate (Right)</b> 16 bit signed number.	
4	31:0	<b>Destination Base Address</b>	
BR09	Format: GraphicsAddress[31:0]		
	Base address of the destination surface: X=0, Y=0. Lower 32bits of the 48bit addressing. When Tiling is enabled (Bit_11 enabled), this address is limited to 4Kbytes. When Tiling is not enabled, this address should be CL (64byte) aligned.		
5	31:16	<b>Reserved</b>	
		Format: MBZ	
	Should be programmed all 0's for 48bit addressing.		
BR27	15:0	<b>Destination Base Address High</b>	
		Format: GraphicsAddress[47:32]	
Should be programmed with the upper 16bits of the 48bit addressing.			

<b>XY_PAT_BLT</b>				
6 BR15	31:0	<p><b>Pattern Base Address</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[31:0]</td> </tr> </table> <p>(28:06 are implemented ) (Note no NPO2 change here). Lower 32bits of the 48bit addressing. The pattern data must be located in linear memory. The Pattern Base Address programmed, must always be Cache Line (64byte) aligned.</p>	Format:	GraphicsAddress[31:0]
Format:	GraphicsAddress[31:0]			
7 BR29	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table> <p>Should be programmed all 0's for 48bit addressing.</p>	Format:	MBZ
Format:	MBZ			
	15:0	<p><b>Pattern Base Address High</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>Should be programmed with the upper 16bits of the 48bit addressing.</p>	Format:	GraphicsAddress[47:32]
Format:	GraphicsAddress[47:32]			

## XY\_PAT\_BLT\_IMMEDIATE

XY_PAT_BLT_IMMEDIATE			
Project:	CHV, BSW		
Source:	BlitterCS		
Length Bias:	2		
<p>PAT_BLT_IMMEDIATE is used when there is no source and the color pattern is not trivial (is not a solid color only) and the pattern is pulled through the command stream. The immediate data sizes are 64 bytes (16 DWs), 128 bytes (32 DWs), or 256 (64DWs) for 8, 16, and 32 bpp color patterns.</p> <p>DWL indicates the total number of Dwords of immediate data. All scan lines and pixels that fall within the ClipRect Y and X coordinates are written. Only pixels within the ClipRectX coordinates and the Destination X coordinates are written using the raster operation.</p> <p>The Pattern Seeds correspond to Destination X = 0 (horizontal) and Y = 0 (vertical). The alignment is relative to the destination coordinates. The pixel of the pattern used / scan line is the (destination X coordinate + horizontal seed) modulo 8. The scan line of the pattern used is the (destination Y coordinate + vertical seed) modulo 8.</p>			
DWord	Bit	Description	
0  BR00	31:29	<b>Client</b>	
		Default Value:	02h 2D Processor
		Format:	Opcode
	28:22	<b>Instruction Target(Opcode)</b>	
		Default Value:	72h
		Format:	Opcode
	21:20	<b>32bpp Byte Mask</b>	
		This field is only used for 32bpp.	
		<b>Value</b>	<b>Name</b>
		00b	[Default]
		1xb	Write Alpha Channel
	x1b	Write RGB Channel	
	19:15	<b>Reserved</b>	
		Format:	MBZ
14:12	<b>Pattern Horizontal Seed</b>		
		Pixel of the scan line to start on corresponding to DST X=0.	
11	<b>Tiling Enable</b>		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0b	Tiling Disabled (Linear Blit)	
	1b	Tiling Enabled	[CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.
10:8	<b>Pattern Vertical Seed</b>		
		Scan line of the 8x8 pattern to start on corresponding to DST Y=0.	
7:0	<b>DWord Length</b>		

<b>XY_PAT_BLT_IMMEDIATE</b>											
		<table border="1"> <tr> <td>Default Value:</td> <td>04h Excludes DWORD 0,1</td> </tr> <tr> <td colspan="2">04 + DWL = (Number of Immediate double)h</td> </tr> </table>	Default Value:	04h Excludes DWORD 0,1	04 + DWL = (Number of Immediate double)h						
Default Value:	04h Excludes DWORD 0,1										
04 + DWL = (Number of Immediate double)h											
1 BR13	31	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ							
	Format:	MBZ									
	30	<b>Clipping Enabled</b> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disabled</td> </tr> <tr> <td>1b</td> <td>Enabled</td> </tr> </tbody> </table>	Value	Name	0b	Disabled	1b	Enabled			
	Value	Name									
	0b	Disabled									
	1b	Enabled									
29:26	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ								
Format:	MBZ										
25:24	<b>Color Depth</b> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>8 Bit Color</td> </tr> <tr> <td>01b</td> <td>16 Bit Color(565)</td> </tr> <tr> <td>10b</td> <td>16 Bit Color(1555)</td> </tr> <tr> <td>11b</td> <td>32 Bit Color</td> </tr> </tbody> </table>	Value	Name	00b	8 Bit Color	01b	16 Bit Color(565)	10b	16 Bit Color(1555)	11b	32 Bit Color
Value	Name										
00b	8 Bit Color										
01b	16 Bit Color(565)										
10b	16 Bit Color(1555)										
11b	32 Bit Color										
23:16	<b>Raster Operation</b>										
15:0	<b>Destination Pitch in DWords</b> 2's complement (Negative Pitch Not allowed for Pixel nor Text) For Tiled surfaces (bit_11 enabled) this pitch is of 512Byte granularity for Tile-X, 128B granularity for Tile-Y and can be upto 128Kbytes (or 32KDwords).										
2 BR22	31:16	<b>Destination Y1 Coordinate (Top)</b> 16 bit signed number.									
	15:0	<b>Destination X1 Coordinate (Left)</b> 16 bit signed number.									
3 BR23	31:16	<b>Destination Y2 Coordinate (Bottom)</b> 16 bit signed number.									
	15:0	<b>Destination X2 Coordinate (Right)</b> 16 bit signed number.									
4 BR09	31:0	<b>Destination Base Address</b> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[31:0]</td> </tr> </table> Base address of the destination surface: X=0, Y=0. Lower 32bits of the 48bit addressing. When Tiling is enabled (Bit_11 enabled), this address is limited to 4Kbytes. When Tiling is not enabled, this address should be CL (64byte) aligned.	Format:	GraphicsAddress[31:0]							
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5 BR27	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> Should be programmed all 0's for 48bit addressing.	Format:	MBZ								
Format:	MBZ										

<b>XY_PAT_BLT_IMMEDIATE</b>				
	15:0	<p><b>Destination Base Address High</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>Should be programmed with the upper 16bits of the 48bit addressing.</p>	Format:	GraphicsAddress[47:32]
Format:	GraphicsAddress[47:32]			
6..n	31:0	<b>Immediate Data</b>		

## XY\_PAT\_CHROMA\_BLT

XY_PAT_CHROMA_BLT			
Project:	CHV, BSW		
Source:	BlitterCS		
Length Bias:	2		
<p>PAT_BLT is used when there is no source and the color pattern is not trivial (is not a solid color only). All scan lines and pixels that fall within the ClipRect Y and X coordinates are written. Only pixels within the ClipRectX coordinates and the Destination X coordinates are written using the raster operation. The Pattern Seeds correspond to Destination X = 0 (horizontal) and Y = 0 (vertical). The alignment is relative to the destination coordinates. The pixel of the pattern used / scan line is the (destination X coordinate + horizontal seed) modulo 8. The scan line of the pattern used is the (destination Y coordinate + vertical seed) modulo 8.</p>			
DWord	Bit	Description	
0  BR00	31:29	<b>Client</b>	
		Default Value:	02h 2D Processor
		Format:	Opcode
	28:22	<b>Instruction Target(Opcode)</b>	
		Default Value:	76h
		Format:	Opcode
	21:20	<b>32bpp Byte Mask</b>	
		This field is only used for 32bpp.	
		<b>Value</b>	<b>Name</b>
		00b	[Default]
1xb		Write Alpha Channel	
x1b	Write RGB Channel		
19:17	<b>Transparency Range Mode</b>	(chroma-key) - Dst Chroma-key modes ONLY (SRC ILLEGAL)	
16:15	<b>Reserved</b>		
14:12	<b>Pattern Horizontal Seed</b>	Pixel of the scan line to start on corresponding to DST X=0.	
11	<b>Tiling Enable</b>		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0b	Tiling Disabled (Linear Blit)	
	1b	Tiling Enabled	[CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.
10:8	<b>Pattern Vertical Seed</b>	Scan line of the 8x8 pattern to start on corresponding to DST Y=0.	
7:0	<b>DWord Length</b>		
	Default Value:	08h Excludes DWORD 0,1	



<b>XY_PAT_CHROMA_BLT</b>											
1 BR13	31	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ							
	Format:	MBZ									
	30	<b>Clipping Enabled</b> <table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disabled</td> </tr> <tr> <td>1b</td> <td>Enabled</td> </tr> </tbody> </table>	Value	Name	0b	Disabled	1b	Enabled			
	Value	Name									
	0b	Disabled									
	1b	Enabled									
29:26	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ								
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25:24	<b>Color Depth</b> <table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 30%;">Value</th> <th style="width: 70%;">Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>8 Bit Color</td> </tr> <tr> <td>01b</td> <td>16 Bit Color(565)</td> </tr> <tr> <td>10b</td> <td>16 Bit Color(1555)</td> </tr> <tr> <td>11b</td> <td>32 Bit Color</td> </tr> </tbody> </table>	Value	Name	00b	8 Bit Color	01b	16 Bit Color(565)	10b	16 Bit Color(1555)	11b	32 Bit Color
Value	Name										
00b	8 Bit Color										
01b	16 Bit Color(565)										
10b	16 Bit Color(1555)										
11b	32 Bit Color										
23:16	<b>Raster Operation</b>										
15:0	<b>Destination Pitch in DWords</b> 2's complement (Negative Pitch Not allowed for Pixel nor Text) For Tiled surfaces (bit_11 enabled) this pitch is of 512Byte granularity for Tile-X, 128B granularity for Tile-Y and can be upto 128Kbytes (or 32KDwords).										
2 BR22	31:16	<b>Destination Y1 Coordinate (Top)</b> 16 bit signed number.									
	15:0	<b>Destination X1 Coordinate (Left)</b> 16 bit signed number.									
3 BR23	31:16	<b>Destination Y2 Coordinate (Bottom)</b> 16 bit signed number.									
	15:0	<b>Destination X2 Coordinate (Right)</b> 16 bit signed number.									
4 BR09	31:0	<b>Destination Base Address</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[31:0]</td> </tr> </table> Base address of the destination surface: X=0, Y=0. Lower 32bits of the 48bit addressing. When Tiling is enabled (Bit_11 enabled), this address is limited to 4Kbytes. When Tiling is not enabled, this address should be CL (64byte) aligned.	Format:	GraphicsAddress[31:0]							
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Format:	MBZ										
5 BR27	15:0	<b>Destination Base Address High</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> Should be programmed with the upper 16bits of the 48bit addressing.	Format:	GraphicsAddress[47:32]							
	Format:	GraphicsAddress[47:32]									

<b>XY_PAT_CHROMA_BLT</b>				
6 BR15	31:0	<p><b>Pattern Base Address</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[31:0]</td> </tr> </table> <p>(28:06 are implemented ) (Note no NPO2 change here). Lower 32bits of the 48bit addressing. The pattern data must be located in linear memory. The Pattern Base Address programmed, must always be Cache Line (64byte) aligned.</p>	Format:	GraphicsAddress[31:0]
Format:	GraphicsAddress[31:0]			
7 BR29	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table> <p>Should be programmed all 0's for 48bit addressing.</p>	Format:	MBZ
Format:	MBZ			
	15:0	<p><b>Pattern Base Address High</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>Should be programmed with the upper 16bits of the 48bit addressing.</p>	Format:	GraphicsAddress[47:32]
Format:	GraphicsAddress[47:32]			
8 BR18	31:0	<p><b>Transparency Color Low</b> (Chroma-key Low = Pixel Greater or Equal)</p>		
9 BR19	31:0	<p><b>Transparency Color High</b> (Chroma-key High = Pixel Less or Equal)</p>		

## XY\_PAT\_CHROMA\_BLT\_IMMEDIATE

XY_PAT_CHROMA_BLT_IMMEDIATE			
Project:	CHV, BSW		
Source:	BlitterCS		
Length Bias:	2		
<p>PAT_BLT_IMMEDIATE is used when there is no source and the color pattern is not trivial (is not a solid color only) and the pattern is pulled through the command stream. The immediate data sizes are 64 bytes (16 DWs), 128 bytes (32 DWs), or 256 (64DWs) for 8, 16, and 32 bpp color patterns.</p> <p>DWL indicates the total number of Dwords of immediate data. All scan lines and pixels that fall within the ClipRect Y and X coordinates are written. Only pixels within the ClipRectX coordinates and the Destination X coordinates are written using the raster operation.</p> <p>The Pattern Seeds correspond to Destination X = 0 (horizontal) and Y = 0 (vertical). The alignment is relative to the destination coordinates. The pixel of the pattern used / scan line is the (destination X coordinate + horizontal seed) modulo 8. The scan line of the pattern used is the (destination Y coordinate + vertical seed) modulo 8.</p>			
DWord	Bit	Description	
0  BR00	31:29	<b>Client</b>	
		Default Value: 02h 2D Processor	
		Format: Opcode	
	28:22	<b>Instruction Target(Opcode)</b>	
		Default Value: 77h	
		Format: Opcode	
	21:20	<b>32bpp Byte Mask</b>	
		This field is only used for 32bpp.	
		<b>Value</b>	<b>Name</b>
		00b	[Default]
	1xb	Write Alpha Channel	
	x1b	Write RGB Channel	
19:17	<b>Transparency Range Mode</b>		
	(chroma-key) - Dst Chroma-key modes ONLY (SRC ILLEGAL)		
16:15	<b>Reserved</b>		
14:12	<b>Pattern Horizontal Seed</b>		
	Pixel of the scan line to start on corresponding to DST X=0.		
11	<b>Tiling Enable</b>		
	<b>Value</b>	<b>Name</b>	
	0b	Tiling Disabled (Linear Blit)	
	1b	Tiling Enabled [CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.	
10:8	<b>Pattern Vertical Seed</b>		
	Scan line of the 8x8 pattern to start on corresponding to DST Y=0.		

<b>XY_PAT_CHROMA_BLT_IMMEDIATE</b>											
	7:0	<p><b>DWord Length</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Default Value:</td> <td>06h Excludes DWORD 0,1</td> </tr> </table> <p>06 + DWL = (Number of Immediate double)h</p>	Default Value:	06h Excludes DWORD 0,1							
Default Value:	06h Excludes DWORD 0,1										
1 BR13	31	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ							
	Format:	MBZ									
	30	<p><b>Clipping Enabled</b></p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 50%;">Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disabled</td> </tr> <tr> <td>1b</td> <td>Enabled</td> </tr> </tbody> </table>	Value	Name	0b	Disabled	1b	Enabled			
	Value	Name									
	0b	Disabled									
	1b	Enabled									
29:26	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ								
Format:	MBZ										
25:24	<p><b>Color Depth</b></p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 50%;">Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>8 Bit Color</td> </tr> <tr> <td>01b</td> <td>16 Bit Color(565)</td> </tr> <tr> <td>10b</td> <td>16 Bit Color(1555)</td> </tr> <tr> <td>11b</td> <td>32 Bit Color</td> </tr> </tbody> </table>	Value	Name	00b	8 Bit Color	01b	16 Bit Color(565)	10b	16 Bit Color(1555)	11b	32 Bit Color
Value	Name										
00b	8 Bit Color										
01b	16 Bit Color(565)										
10b	16 Bit Color(1555)										
11b	32 Bit Color										
23:16	<p><b>Raster Operation</b></p>										
15:0	<p><b>Destination Pitch in DWords</b></p> <p>2's complement For Tiled surfaces (bit_11 enabled) this pitch is of 512Byte granularity for Tile-X, 128B granularity for Tile-Y and can be upto 128Kbytes (or 32KDwords).</p>										
2 BR22	31:16	<p><b>Destination Y1 Coordinate (Top)</b></p> <p>16 bit signed number.</p>									
	15:0	<p><b>Destination X1 Coordinate (Left)</b></p> <p>16 bit signed number.</p>									
3 BR23	31:16	<p><b>Destination Y2 Coordinate (Bottom)</b></p> <p>16 bit signed number.</p>									
	15:0	<p><b>Destination X2 Coordinate (Right)</b></p> <p>16 bit signed number.</p>									
4 BR09	31:0	<p><b>Destination Base Address</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>GraphicsAddress[31:0]</td> </tr> </table> <p>Base address of the destination surface: X=0, Y=0. Lower 32bits of the 48bit addressing. When Tiling is enabled (Bit_11 enabled), this address is limited to 4Kbytes. When Tiling is not enabled, this address should be CL (64byte) aligned.</p>	Format:	GraphicsAddress[31:0]							
		Format:	GraphicsAddress[31:0]								
<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>MBZ</td> </tr> </table> <p>Should be programmed all 0's for 48bit addressing.</p>	Format:	MBZ									
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5 BR27	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>MBZ</td> </tr> </table> <p>Should be programmed all 0's for 48bit addressing.</p>	Format:	MBZ							
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<b>XY_PAT_CHROMA_BLT_IMMEDIATE</b>				
	15:0	<p><b>Destination Base Address High</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>Should be programmed with the upper 16bits of the 48bit addressing.</p>	Format:	GraphicsAddress[47:32]
Format:	GraphicsAddress[47:32]			
6 BR18	31:0	<p><b>Transparency Color Low</b> (Chroma-key Low = Pixel Greater or Equal)</p>		
7 BR19	31:0	<p><b>Transparency Color High</b> (Chroma-key High = Pixel Less or Equal)</p>		
8..n	31:0	<p><b>Immediate Data</b></p>		

## XY\_PIXEL\_BLT

<b>XY_PIXEL_BLT</b>										
Project:	CHV, BSW									
Source:	BlitterCS									
Length Bias:	2									
<p>The Destination X coordinate and Destination Y coordinate is compared with the ClipRect registers. If it is within all 4 comparisons, then the pixel supplied in the XY_SETUP_BLT instruction is written with the raster operation to (Destination Y Address + (Destination Y coordinate * Destination pitch) + (Destination X coordinate * bytes per pixel)).</p> <p>ROP field must specify pattern or fill with 0's or 1's. There is no source operand.</p> <p>Negative Stride (= Pitch) specified in the Setup command is Not Allowed</p>										
DWord	Bit	Description								
0  BR00	31:29	<b>Client</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Default Value:</td> <td>02h 2D Processor</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table>	Default Value:	02h 2D Processor	Format:	Opcode				
	Default Value:	02h 2D Processor								
	Format:	Opcode								
	28:22	<b>Instruction Target(Opcode)</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Default Value:</td> <td>24h</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table>	Default Value:	24h	Format:	Opcode				
	Default Value:	24h								
	Format:	Opcode								
	21:12	<b>Reserved</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ						
Format:	MBZ									
11	<b>Tiling Enable</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 40%;">Name</th> <th style="width: 50%;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td>Tiling Disabled (Linear Blit)</td> <td></td> </tr> <tr> <td style="text-align: center;">1b</td> <td>Tiling Enabled</td> <td>[CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.</td> </tr> </tbody> </table>	Value	Name	Description	0b	Tiling Disabled (Linear Blit)		1b	Tiling Enabled	[CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.
Value	Name	Description								
0b	Tiling Disabled (Linear Blit)									
1b	Tiling Enabled	[CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.								
10:8	<b>Reserved</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ							
Format:	MBZ									
7:0	<b>DWord Length</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Default Value:</td> <td>00h</td> </tr> </table>	Default Value:	00h							
Default Value:	00h									
1	31:16	<b>Destination Y1 Coordinate (Top)</b> 16 bit signed number.								
BR22	15:0	<b>Destination X1 Coordinate (Left)</b> 16 bit signed number.								

## XY\_SCANLINES\_BLT

<b>XY_SCANLINES_BLT</b>			
Project:	CHV, BSW		
Source:	BlitterCS		
Length Bias:	2		
<p>All scan lines and pixels that fall within the ClipRect Y and X coordinates are written. Only pixels within the ClipRectX coordinates and the Destination X coordinates are written using the raster operation.</p> <p>The Pattern Seeds correspond to Destination X = 0 (horizontal) and Y = 0 (vertical). The alignment is relative to the destination coordinates. The pixel of the pattern used / scan line is the (destination X coordinate + horizontal seed) modulo 8. The scan line of the pattern used is the (destination Y coordinate + vertical seed) modulo 8.</p> <p>Solid pattern should use the XY_SETUP_MONO_PATTERN_SL_BLT instruction.</p> <p>ROP field must specify pattern or fill with 0's or 1's. There is no source operand.</p>			
DWord	Bit	Description	
0  BR00	31:29	<b>Client</b>	
		Default Value:	02h 2D Processor
		Format:	Opcode
	28:22	<b>Instruction Target(Opcode)</b>	
		Default Value:	25h
		Format:	Opcode
	21:15	<b>Reserved</b>	
	14:12	<b>Pattern Horizontal Seed</b> Pixel of the scan line to start on corresponding to DST X=0.	
	11	<b>Tiling Enable</b>	
		<b>Value</b>	<b>Name</b>
0b		Tiling Disabled (Linear Blit)	
1b		Tiling Enabled	[CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.
10:8	<b>Pattern Vertical Seed</b> Scan line of the 8x8 pattern to start on corresponding to DST Y=0.		
7:0	<b>DWord Length</b>		
	Default Value:	01h	
1  BR22	31:16	<b>Destination Y1 Coordinate (Top)</b> 16 bit signed number.	
	15:0	<b>Destination X1 Coordinate (Left)</b> 16 bit signed number.	
2  BR23	31:16	<b>Destination Y2 Coordinate (Bottom)</b> 16 bit signed number.	
	15:0	<b>Destination X2 Coordinate (Right)</b> 16 bit signed number.	

## XY\_SETUP\_BLT

<b>XY_SETUP_BLT</b>			
Project:	CHV, BSW		
Source:	BlitterCS		
Length Bias:	2		
<p>This setup instruction supplies common setup information including clipping coordinates used by the XY commands: XY_PIXEL_BLT, XY_SCANLINE_BLT, XY_TEXT_BLT, and XY_TEXT_BLT_IMMEDIATE. These are the only instructions that require that state be saved between instructions other than the Clipping parameters. There are 5 dedicated registers to contain the state for the 3 setup BLT instructions (XY_SETUP_BLT, XY_SETUP_MONO_PATTERN_SL_BLT, and XY_SETUP_CLIP_BLT. All other BLTs use a temporary version of these. The 5 double word registers are: DW1 (Setup Control), DW6 (Setup Foreground color), DW5 (Setup Background color), DW7 (Setup Pattern address), and DW4 (Setup Destination Base Address).</p>			
DWord	Bit	Description	
0  BR00	31:29	<b>Client</b>	
		Default Value:	02h 2D Processor
		Format:	Opcode
	28:22	<b>Instruction Target(Opcode)</b>	
		Default Value:	01h
		Format:	Opcode
	21:20	<b>32 bpp Byte Mask</b>	
		<b>Value</b>	<b>Name</b>
		1xb	Write Alpha Channel
		x1b	Write RGB Channel
19:12	<b>Reserved</b>		
11	<b>Tiling Enable</b>		
	<b>Value</b>	<b>Name</b>	
	0b	Tiling Disabled (Linear Blit)	
1b	Tiling Enabled (Tile-X or Tile-Y)		
10:8	<b>Reserved</b>		
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	08h	
1  BR01	31	<b>Reserved</b>	
	30	<b>Clipping Enabled</b>	
		<b>Value</b>	<b>Name</b>
		0b	Disabled
1b	Enabled		



<b>XY_SETUP_BLT</b>			
	29	<b>Mono Source Transparency Mode</b>	
		<b>Value</b>	<b>Name</b>
		0b	Use Background
		1b	Transparency Enabled
	28:26	<b>Reserved</b>	
		Format:	MBZ
	25:24	<b>Color Depth</b>	
		<b>Value</b>	<b>Name</b>
		00b	8 Bit Color
		01b	16 Bit Color(565)
10b		16 Bit Color(1555)	
	11b	32 Bit Color	
23:16	<b>Raster Operation</b>		
15:0	<b>Destination Pitch in DWords</b> 2's complement (Negative Pitch Not allowed for Pixel nor Text) For Tiled surfaces (bit_11 enabled) this pitch is of 512Byte granularity for Tile-X, 128B granularity for Tile-Y and can be upto 128Kbytes (or 32KDwords).		
2	31:16	<b>ClipRect Y1 Coordinate (Top)</b> (30:16 = 15 bit positive number)	
	BR24	15:0 <b>ClipRect X1 Coordinate (Left)</b> (14:00 = 15 bit positive number)	
3	31:16	<b>ClipRect Y2 Coordinate (Bottom)</b> (30:16 = 15 bit positive number)	
	BR25	15:0 <b>ClipRect X2 Coordinate (Right)</b> (14:00 = 15 bit positive number)	
4	31:0	<b>Setup Destination Base Address</b>	
	BR09	Format: GraphicsAddress[31:0] Base address of the destination surface: X=0, Y=0. Lower 32bits of the 48bit addressing. When Tiling is enabled (Bit_11 enabled), this address is limited to 4Kbytes. When Tiling is not enabled, this address should be CL (64byte) aligned.	
5	31:16	<b>Reserved</b>	
		Format: MBZ	
	Should be programmed all 0's for 48bit addressing.		
15:0	<b>Setup Destination Base Address High</b>		
	Format: GraphicsAddress[47:32]		
Should be programmed with the upper 16bits of the 48bit addressing.			

<b>XY_SETUP_BLT</b>				
6 BR05	31:0	<p><b>Setup Background Color</b> 8 bit = [7:0], 16 bit = [15:0], 32 bit = [31:0] All</p>		
7 BR06	31:0	<p><b>Setup Foreground Color</b> 8 bit = [7:0], 16 bit = [15:0], 32 bit = [31:0] (SLB and TB only)</p>		
8 BR07	31:0	<p><b>Setup Pattern Base Address for Color Pattern</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[31:0]</td> </tr> </table> <p>(26:06 are implemented) (SLB only) (Note no NPO2 change here). The pattern data must be located in linear memory. Lower 32bits of the 48bit addressing. The Pattern Base Address programmed, must always be Cache Line (64byte) aligned.</p>	Format:	GraphicsAddress[31:0]
Format:	GraphicsAddress[31:0]			
9 BR30	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table> <p>Should be programmed all 0's for 48bit addressing.</p>	Format:	MBZ
Format:	MBZ			
	15:0	<p><b>Setup Pattern Base Address for Color Pattern High</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>Should be programmed with the upper 16bits of the 48bit addressing.</p>	Format:	GraphicsAddress[47:32]
Format:	GraphicsAddress[47:32]			

## XY\_SETUP\_CLIP\_BLT

<b>XY_SETUP_CLIP_BLT</b>		
Project:	CHV, BSW	
Source:	BlitterCS	
Length Bias:	2	
This command is used to only change the clip coordinate registers. These are the same clipping registers as the Setup clipping registers above.		
DWord	Bit	Description
0  BR00	31:29	<b>Client</b>
		Default Value: 02h 2D Processor
		Format: Opcode
	28:22	<b>Instruction Target(Opcode)</b>
		Default Value: 03h
		Format: Opcode
	21:12	<b>Reserved</b>
Format: MBZ		
11	<b>Tiling Enable</b>	
Value	Name	
0b	Tiling Disabled (Linear Blit)	
1b	Tiling Enabled (Tile-X or Tile-Y)	
10:8	<b>Reserved</b>	
Format: MBZ		
7:0	<b>DWord Length</b>	
Default Value: 01h		
1  BR24	31:16	<b>ClipRect Y1 Coordinate (Top)</b> (30:16 = 15 bit positive number)
	15:0	<b>ClipRect X1 Coordinate (Left)</b> (14:00 = 15 bit positive number)
2  BR25	31:16	<b>ClipRect Y2 Coordinate (Bottom)</b> (30:16 = 15 bit positive number)
	15:0	<b>ClipRect X2 Coordinate (Right)</b> (14:00 = 15 bit positive number)

## XY\_SETUP\_MONO\_PATTERN\_SL\_BLT

XY_SETUP_MONO_PATTERN_SL_BLT			
Project:	CHV, BSW		
Source:	BlitterCS		
Length Bias:	2		
<p>This setup instruction supplies common setup information including clipping coordinates used exclusively with the following instruction: XY_SCANLINE_BLT (SLB) - 1 scan line of monochrome pattern and destination are the only operands allowed.</p>			
DWord	Bit	Description	
0 BR00	31:29	<b>Client</b>	
		Default Value:	02h 2D Processor
		Format:	Opcode
	28:22	<b>Instruction Target(Opcode)</b>	
		Default Value:	11h
		Format:	Opcode
	21:20	<b>32 bpp Byte Mask</b>	
		<b>Value</b>	<b>Name</b>
		1xb x1b	Write Alpha Channel Write RGB Channel
	19:12	<b>Reserved</b>	
11	<b>Tiling Enable</b>		
	<b>Value</b>	<b>Name</b>	
	0b 1b	Tiling Disabled (Linear Blit) Tiling Enabled (Tile-X or Tile-Y)	
10:8	<b>Reserved</b>		
7:0	<b>DWord Length</b>		
	Default Value:	08h	
1 BR01	31	<b>Solid Pattern Select</b> (SLB and Pixel only)	
		<b>Value</b>	<b>Name</b>
		0 1	No Solid Pattern Solid Pattern
	30	<b>Clipping Enabled</b>	
		<b>Value</b>	<b>Name</b>
0b 1b		Disabled Enabled	

<b>XY_SETUP_MONO_PATTERN_SL_BLT</b>												
	29	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">MBZ</td> </tr> </table>	Format:	MBZ								
	Format:	MBZ										
	28	<b>Mono Pattern Transparency Mode</b> <table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 30%;">Value</th> <th style="width: 70%;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Use Background</td> </tr> <tr> <td>1b</td> <td>Transparency Enabled</td> </tr> </tbody> </table>	Value	Name	0b	Use Background	1b	Transparency Enabled				
	Value	Name										
	0b	Use Background										
	1b	Transparency Enabled										
	27:26	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">MBZ</td> </tr> </table>	Format:	MBZ								
	Format:	MBZ										
	25:24	<b>Color Depth</b> <table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 30%;">Value</th> <th style="width: 70%;">Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>8 Bit Color</td> </tr> <tr> <td>01b</td> <td>16 Bit Color(565)</td> </tr> <tr> <td>10b</td> <td>16 Bit Color(1555)</td> </tr> <tr> <td>11b</td> <td>32 Bit Color</td> </tr> </tbody> </table>	Value	Name	00b	8 Bit Color	01b	16 Bit Color(565)	10b	16 Bit Color(1555)	11b	32 Bit Color
	Value	Name										
00b	8 Bit Color											
01b	16 Bit Color(565)											
10b	16 Bit Color(1555)											
11b	32 Bit Color											
23:16	<b>Raster Operation</b>											
15:0	<b>Destination Pitch in DWords</b> 2's complement (Negative Pitch Not allowed for Pixel nor Text) For Tiled surfaces (bit_11 enabled) this pitch is of 512Byte granularity for Tile-X, 128B granularity for Tile-Y and can be upto 128Kbytes (or 32KDwords).											
2	31:16	<b>ClipRect Y1 Coordinate (Top)</b> (30:16 = 15 bit positive number)										
BR24	15:0	<b>ClipRect X1 Coordinate (Left)</b> (14:00 = 15 bit positive number)										
3	31:16	<b>ClipRect Y2 Coordinate (Bottom)</b> (30:16 = 15 bit positive number)										
BR25	15:0	<b>ClipRect X2 Coordinate (Right)</b> (14:00 = 15 bit positive number)										
4	31:0	<b>Setup Destination Base Address</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 40%;">Format:</td> <td style="width: 60%;">GraphicsAddress[31:0]</td> </tr> </table> Base address of the destination surface: X=0, Y=0. Lower 32bits of the 48bit addressing. When Tiling is enabled (Bit_11 enabled), this address is limited to 4Kbytes. When Tiling is not enabled, this address should be CL (64byte) aligned.	Format:	GraphicsAddress[31:0]								
Format:	GraphicsAddress[31:0]											
5	BR27	31:16	<b>Reserved</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">MBZ</td> </tr> </table> Should be programmed all 0's for 48bit addressing.	Format:	MBZ							
		Format:	MBZ									
15:0	<b>Setup Destination Base Address High</b> <table border="1" style="width: 100%;"> <tr> <td style="width: 40%;">Format:</td> <td style="width: 60%;">GraphicsAddress[47:32]</td> </tr> </table> Should be programmed with the upper 16bits of the 48bit addressing.	Format:	GraphicsAddress[47:32]									
Format:	GraphicsAddress[47:32]											

<b>XY_SETUP_MONO_PATTERN_SL_BLT</b>		
6 BR05	31:0	<b>Setup Background Color</b> 8 bit = [7:0], 16 bit = [15:0], 32 bit = [31:0] All
7 BR06	31:0	<b>Setup Foreground Color</b> 8 bit = [7:0], 16 bit = [15:0], 32 bit = [31:0] (SLB and TB only)
8 BR20	31:0	<b>DW0 (least significant) for a Monochrome Pattern</b>
9 BR21	31:0	<b>DW1 (most significant) for a Monochrome Pattern</b>

## XY\_SRC\_COPY\_BLT

XY_SRC_COPY_BLT			
Project:	CHV, BSW		
Source:	BlitterCS		
Length Bias:	2		
<p>This BLT instruction performs a color source copy where the only operands involved is a color source and destination of the same bit width.</p> <p>The source and destination operands may overlap, which means that the X and Y directions can be either forward or backwards. The BLT Engine takes care of all situations. The base addresses plus the X and Y coordinates determine if there is an overlap between the source and destination operands. If the base addresses of the source and destination are the same and the Source X1 is less than Destination X1, then the BLT Engine performs the accesses in the X-backwards access pattern. There is no need to look for an actual overlap. If the base addresses are the same and Source Y1 is less than Destination Y1, then the scan line accesses start at Destination Y2 with the corresponding source scan line and the strides are subtracted for every scan line access. The ROP value chosen must involve source and no pattern data in the ROP operation.</p>			
DWord	Bit	Description	
0 BR00	31:29	<b>Client</b>	
		Default Value:	02h 2D Processor
		Format:	Opcode
	28:22	<b>Instruction Target(Opcode)</b>	
		Default Value:	53h
		Format:	Opcode
	21:20	<b>32bpp Byte Mask</b>	
		This field is only used for 32bpp.	
		<b>Value</b>	<b>Name</b>
		00b	[Default]
1xb		Write Alpha Channel	
	x1b	Write RGB Channel	
19:16	<b>Reserved</b>		
15	<b>Src Tiling Enable</b>		
	<b>Value</b>	<b>Name</b>	
	0b	Tiling Disabled (Linear)	
	1b	Tiling Enabled [CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.	
14:12	<b>Reserved</b>		
11	<b>Dest Tiling Enable</b>		
	<b>Value</b>	<b>Name</b>	
	0b	Tiling Disabled (Linear Blit)	
	1b	Tiling Enabled [CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.	

<b>XY_SRC_COPY_BLT</b>											
	10:8	<b>Reserved</b> Format: _____ MBZ									
	7:0	<b>DWord Length</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">08h</td> <td></td> </tr> </tbody> </table>	Value	Name	08h						
Value	Name										
08h											
1  BR13	31	<b>Reserved</b> Format: _____ MBZ									
	30	<b>Clipping Enabled</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disabled</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enabled</td> </tr> </tbody> </table>	Value	Name	0b	Disabled	1b	Enabled			
	Value	Name									
	0b	Disabled									
	1b	Enabled									
	29:26	<b>Reserved</b> Format: _____ MBZ									
25:24	<b>Color Depth</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">00b</td> <td style="text-align: center;">8 Bit Color</td> </tr> <tr> <td style="text-align: center;">01b</td> <td style="text-align: center;">16 Bit Color(565)</td> </tr> <tr> <td style="text-align: center;">10b</td> <td style="text-align: center;">16 Bit Color(1555)</td> </tr> <tr> <td style="text-align: center;">11b</td> <td style="text-align: center;">32 Bit Color</td> </tr> </tbody> </table>	Value	Name	00b	8 Bit Color	01b	16 Bit Color(565)	10b	16 Bit Color(1555)	11b	32 Bit Color
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01b	16 Bit Color(565)										
10b	16 Bit Color(1555)										
11b	32 Bit Color										
23:16	<b>Raster Operation</b>										
	15:0 <b>Destination Pitch in DWords</b> 2's complement For Tiled surfaces (bit_11 enabled) this pitch is of 512Byte granularity for Tile-X, 128B granularity for Tile-Y and can be upto 128Kbytes (or 32KDwords).										
2  BR22	31:16	<b>Destination Y1 Coordinate (Top)</b> 16 bit signed number.									
	15:0	<b>Destination X1 Coordinate (Left)</b> 16 bit signed number.									
3  BR23	31:16	<b>Destination Y2 Coordinate (Bottom)</b> 16 bit signed number.									
	15:0	<b>Destination X2 Coordinate (Right)</b> 16 bit signed number.									
4  BR09	31:0	<b>Destination Base Address</b> Format: _____ GraphicsAddress[31:0] Base address of the destination surface: X=0, Y=0. Lower 32bits of the 48bit addressing. When Tiling is enabled (Bit_11 enabled), this address must be 4KB-aligned. When Tiling is not enabled, this address should be CL (64byte) aligned.									



<b>XY_SRC_COPY_BLT</b>				
5 BR27	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table> <p>Must be all 0's for 48bit addressing.</p>	Format:	MBZ
	Format:	MBZ		
15:0	<p><b>Destination Base Address High</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>The upper 16bits of the 48-bit address.</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			
6 BR26	31:16	<p><b>Source Y1 Coordinate (Top)</b></p> <p>16 bit signed number.</p>		
	15:0	<p><b>Source X1 Coordinate (Left)</b></p> <p>16 bit signed number.</p>		
7 BR11	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
15:0	<p><b>Source Pitch (double word aligned) and in DWords</b></p> <p>2's complement. For Tiled Src (bit 15 enabled) this pitch is of 512Byte granularity for Tile-X, 128B granularity for Tile-Yand can be upto 128Kbytes (or 32KDwords).</p>			
8 BR12	31:0	<p><b>Source Base Address</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[31:0]</td> </tr> </table> <p>Base address of the destination surface: X=0, Y=0. Lower 32bits of the 48bit addressing. When Src Tiling is enabled (Bit_15 enabled), this address must be 4KB-aligned. When Tiling is not enabled, this address should be CL (64byte) aligned.</p>	Format:	GraphicsAddress[31:0]
Format:	GraphicsAddress[31:0]			
9 BR28	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table> <p>Must be all 0's for 48-bit addressing.</p>	Format:	MBZ
	Format:	MBZ		
15:0	<p><b>Source Base Address High</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>The upper 16 bits of the 48-bit address.</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			

## XY\_SRC\_COPY\_CHROMA\_BLT

XY_SRC_COPY_CHROMA_BLT			
Project:	CHV, BSW		
Source:	BlitterCS		
Length Bias:	2		
<p>This BLT instruction performs a color source copy with chroma-keying where the only operands involved is a color source and destination of the same bit width.</p> <p>The source and destination operands may overlap, which means that the X and Y directions can be either forward or backwards. The BLT Engine takes care of all situations. The base addresses plus the X and Y coordinates determine if there is an overlap between the source and destination operands. If the base addresses of the source and destination are the same and the Source X1 is less than Destination X1, then the BLT Engine performs the accesses in the X-backwards access pattern. There is no need to look for an actual overlap. If the base addresses are the same and Source Y1 is less than Destination Y1, then the scan line accesses start at Destination Y2 with the corresponding source scan line and the strides are subtracted for every scan line access. The ROP value chosen must involve source and no pattern data in the ROP operation.</p>			
DWord	Bit	Description	
0 BR00	31:29	<b>Client</b>	
		Default Value:	02h 2D Processor
		Format:	Opcode
	28:22	<b>Instruction Target(Opcode)</b>	
		Default Value:	73h
		Format:	Opcode
	21:20	<b>32bpp Byte Mask</b>	
		This field is only used for 32bpp.	
		<b>Value</b>	<b>Name</b>
		00b	[Default]
1xb		Write Alpha Channel	
19:17	<b>Transparency Range Mode</b>		
	(chroma-key)		
16	<b>Reserved</b>		
	Format:	MBZ	
15	<b>Src Tiling Enable</b>		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0b	Tiling Disabled (Linear)	
	1b	Tiling Enabled	[CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.
14:12	<b>Reserved</b>		
	Format:	MBZ	

<b>XY_SRC_COPY_CHROMA_BLT</b>											
	11	<b>Dest Tiling Enable</b>									
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Tiling Disabled (Linear Blit)</td> <td></td> </tr> <tr> <td>1b</td> <td>Tiling Enabled</td> <td>[CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.</td> </tr> </tbody> </table>	Value	Name	Description	0b	Tiling Disabled (Linear Blit)		1b	Tiling Enabled	[CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.
		Value	Name	Description							
	0b	Tiling Disabled (Linear Blit)									
1b	Tiling Enabled	[CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.									
10:8	<b>Reserved</b>										
	Format:	MBZ									
	7:0	<b>DWord Length</b>									
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0Ah</td> <td></td> </tr> </tbody> </table>	Value	Name	0Ah						
	Value	Name									
0Ah											
10:8	<b>Reserved</b>										
	Format:	MBZ									
1 BR13	31	<b>Reserved</b>									
		Format:	MBZ								
		30	<b>Clipping Enabled</b>								
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	0b	Disabled									
	1b	Enabled									
	29:26	<b>Reserved</b>									
		Format:	MBZ								
	25:24	<b>Color Depth</b>									
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23:16	<b>Raster Operation</b>										
15:0	<b>Destination Pitch in DWords</b> 2's complement For Tiled surfaces (bit_11 enabled) this pitch is of 512Byte granularity for Tile-X, 128B granularity for Tile-Y and can be upto 128Kbytes (or 32KDwords).										
2 BR22	31:16	<b>Destination Y1 Coordinate (Top)</b> 16 bit signed number.									
	15:0	<b>Destination X1 Coordinate (Left)</b> 16 bit signed number.									
3 BR23	31:16	<b>Destination Y2 Coordinate (Bottom)</b> 16 bit signed number.									
	15:0	<b>Destination X2 Coordinate (Right)</b> 16 bit signed number.									
4 BR09	31:0	<b>Destination Base Address</b>									
		Format: GraphicsAddress[31:0]									

<b>XY_SRC_COPY_CHROMA_BLT</b>				
		Base address of the destination surface: X=0, Y=0. Lower 32bits of the 48bit addressing. When Tiling is enabled (Bit_11 enabled), this address is limited to 4Kbytes. When Tiling is not enabled, this address should be CL (64byte) aligned.		
5  BR27	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">MBZ</td> </tr> </table> <p>Should be programmed all 0's for 48bit addressing.</p>	Format:	MBZ
	Format:	MBZ		
15:0	<p><b>Destination Base Address High</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td style="width: 70%;">GraphicsAddress[47:32]</td> </tr> </table> <p>Should be programmed with the upper 16bits of the 48bit addressing.</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			
6  BR26	31:16	<p><b>Source Y1 Coordinate (Top)</b> 16 bit signed number.</p>		
	15:0	<p><b>Source X1 Coordinate (Left)</b> 16 bit signed number.</p>		
7  BR11	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
15:0	<p><b>Source Pitch (double word aligned) and in DWords</b> 2's complement. For Tiled Src (bit 15 enabled) this pitch is of 512Byte granularity for Tile-X, 128B granularity for Tile-Y and can be upto 128Kbytes (or 32KDwords).</p>			
8  BR12	31:0	<p><b>Source Base Address</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td style="width: 70%;">GraphicsAddress[31:0]</td> </tr> </table> <p>Base address of the destination surface: X=0, Y=0. Lower 32bits of the 48bit addressing. When Tiling is enabled (Bit_15 enabled), this address is limited to 4Kbytes. When Tiling is not enabled, this address should be CL (64byte) aligned.</p>	Format:	GraphicsAddress[31:0]
	Format:	GraphicsAddress[31:0]		
15:0	<p><b>Source Base Address High</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td style="width: 70%;">GraphicsAddress[47:32]</td> </tr> </table> <p>Should be programmed with the upper 16bits of the 48bit addressing.</p>	Format:	GraphicsAddress[47:32]	
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9  BR28	31:16	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">MBZ</td> </tr> </table> <p>Should be programmed all 0's for 48bit addressing.</p>	Format:	MBZ
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15:0	<p><b>Source Base Address High</b></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td style="width: 70%;">GraphicsAddress[47:32]</td> </tr> </table> <p>Should be programmed with the upper 16bits of the 48bit addressing.</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			
10  BR18	31:0	<p><b>Transparency Color Low</b> (Chroma-key Low = Pixel Greater or Equal)</p>		
11  BR19	31:0	<p><b>Transparency Color High</b> (Chroma-key High = Pixel Less or Equal)</p>		

## XY\_TEXT\_BLT

XY_TEXT_BLT			
Project:	CHV, BSW		
Source:	BlitterCS		
Length Bias:	2		
<p>All source scan lines and pixels that fall within the ClipRect Y and X coordinates are written. The source address corresponds to Destination X1 and Y1 coordinate.</p> <p>Text is either bit or byte packed. Bit packed means that the next scan line starts 1 pixel after the end of the current scan line with no bit padding. Byte packed means that the next scan line starts on the first bit of the next byte boundary after the last bit of the current line.</p> <p>Source expansion color registers are always in the SETUP_BLT.</p> <p>Negative Stride (= Pitch) is NOT ALLOWED.</p>			
DWord	Bit	Description	
0  BR00	31:29	<b>Client</b>	
		Default Value:	02h 2D Processor
		Format:	Opcode
	28:22	<b>Instruction Target(Opcode)</b>	
		Default Value:	26h
		Format:	Opcode
	21:17	<b>Reserved</b>	
		Format:	MBZ
	16	<b>Bit / Byte Packed</b>	
		Byte packed is for the NT driver.	
<b>Value</b>		<b>Name</b>	
0		<b>Bit</b>	
15:12	<b>Reserved</b>	1	Byte
		<b>Reserved</b>	
		Format:	MBZ
11	<b>Tiling Enable</b>		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0b	Tiling Disabled (Linear Blit)	
	1b	Tiling Enabled	[CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.
10:8	<b>Reserved</b>		
	Format:	MBZ	
7:0	<b>DWord Length</b>		
	Default Value:	03h	
1	31:16	<b>Destination Y1 Coordinate (Top)</b> 16 bit signed number.	

<b>XY_TEXT_BLT</b>				
BR22	15:0	<b>Destination X1 Coordinate (Left)</b> 16 bit signed number.		
2	31:16	<b>Destination Y2 Coordinate (Bottom)</b> 16 bit signed number.		
BR23	15:0	<b>Destination X2 Coordinate (Right)</b> 16 bit signed number.		
3 BR12	31:0	<b>Source Address</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[31:0]</td> </tr> </table> (address of the first byte on scan line corresponding to Dst X1, Y1). Lower 32bits of the 48bit addressing. (Note no NPO2 change here). Since Text data is Monosource data, the Text source Base Address programmed, must always be Cache Line (64byte) aligned.	Format:	GraphicsAddress[31:0]
Format:	GraphicsAddress[31:0]			
4 BR28	31:16	<b>Reserved</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Format:</td> <td>MBZ</td> </tr> </table> Should be programmed with all "0"s for 48bit addressing.	Format:	MBZ
Format:	MBZ			
	15:0	<b>Source Address High</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> Should be programmed with the upper 16bits of the 48bit addressing.	Format:	GraphicsAddress[47:32]
Format:	GraphicsAddress[47:32]			

## XY\_TEXT\_IMMEDIATE\_BLT

### XY\_TEXT\_IMMEDIATE\_BLT

Project: CHV, BSW  
 Source: BlitterCS  
 Length Bias: 2

This instruction allows the Driver to send data through the instruction stream that eliminates the read latency of reading a source from memory.

If an operand is in system cacheable memory and either small or only accessed once, it can be copied directly to the instruction stream versus to graphics accessible memory. The IMMEDIATE\_BLT data MUST transfer an even number of doublewords.

The BLT engine will hang if it does not get an even number of doublewords. All source scan lines and pixels that fall within the ClipRect X and Y coordinates are written. The source data corresponds to Destination X1 and Y1 coordinate.

Source expansion color registers are always in the SETUP\_BLT. NEGATIVE STRIDE (= PITCH) IS NOT ALLOWED.

DWord	Bit	Description								
0  BR00	31:29	<b>Client</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Default Value:</td> <td>02h 2D Processor</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table>	Default Value:	02h 2D Processor	Format:	Opcode				
	Default Value:	02h 2D Processor								
	Format:	Opcode								
	28:22	<b>Instruction Target(Opcode)</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Default Value:</td> <td>31h</td> </tr> <tr> <td>Format:</td> <td>Opcode</td> </tr> </table>	Default Value:	31h	Format:	Opcode				
	Default Value:	31h								
	Format:	Opcode								
	21:17	<b>Reserved</b>								
	16	<b>Bit / Byte Packed</b> Byte packed is for the NT driver. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;"><b>Bit</b></td> </tr> <tr> <td style="text-align: center;">1</td> <td>Byte</td> </tr> </tbody> </table>	Value	Name	0	<b>Bit</b>	1	Byte		
	Value	Name								
	0	<b>Bit</b>								
1	Byte									
15:12	<b>Reserved</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ							
Format:	MBZ									
11	<b>Tiling Enable</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%; text-align: center;">Value</th> <th style="width: 40%; text-align: center;">Name</th> <th style="width: 45%; text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td>Tiling Disabled (Linear Blit)</td> <td></td> </tr> <tr> <td style="text-align: center;">1b</td> <td>Tiling Enabled</td> <td>[CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.</td> </tr> </tbody> </table>	Value	Name	Description	0b	Tiling Disabled (Linear Blit)		1b	Tiling Enabled	[CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.
Value	Name	Description								
0b	Tiling Disabled (Linear Blit)									
1b	Tiling Enabled	[CHV, BSW] [CHV, BSW]: Tile-X or Tile-Y.								
10:8	<b>Reserved</b>									
7:0	<b>DWord Length</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Default Value:</td> <td>01h Excludes DWORD 0,1</td> </tr> </table> 01 + DWL = (Number of Immediate double words)h	Default Value:	01h Excludes DWORD 0,1							
Default Value:	01h Excludes DWORD 0,1									

<b>XY_TEXT_IMMEDIATE_BLT</b>		
1  BR22	31:16	<b>Destination Y1 Coordinate (Top)</b> 16 bit signed number.
	15:0	<b>Destination X1 Coordinate (Left)</b> 16 bit signed number.
2  BR23	31:16	<b>Destination Y2 Coordinate (Bottom)</b> 16 bit signed number.
	15:0	<b>Destination X2 Coordinate (Right)</b> 16 bit signed number.
3..n	31:0	<b>Immediate Data</b>