Intel® Iris™ Plus Graphics and UHD Graphics Open Source

Programmer's Reference Manual

For the 2017 - 2019 Intel Core™ Processors, Pentium® Gold Processors, Celeron® Processors, and Xeon® Processors based on the "Coffee Lake" Platform

Volume 1: Configurations

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Configurations Overview

The Intel "Gen" Graphics Architecture was first introduced to the market in 2004. Since that time, the architecture and implementation have evolved to add many new features, increase performance, and improve power efficiency.

Each product generation has its own configurations chapter. Each chapter has a section for each project, and each project contains the following subsections:

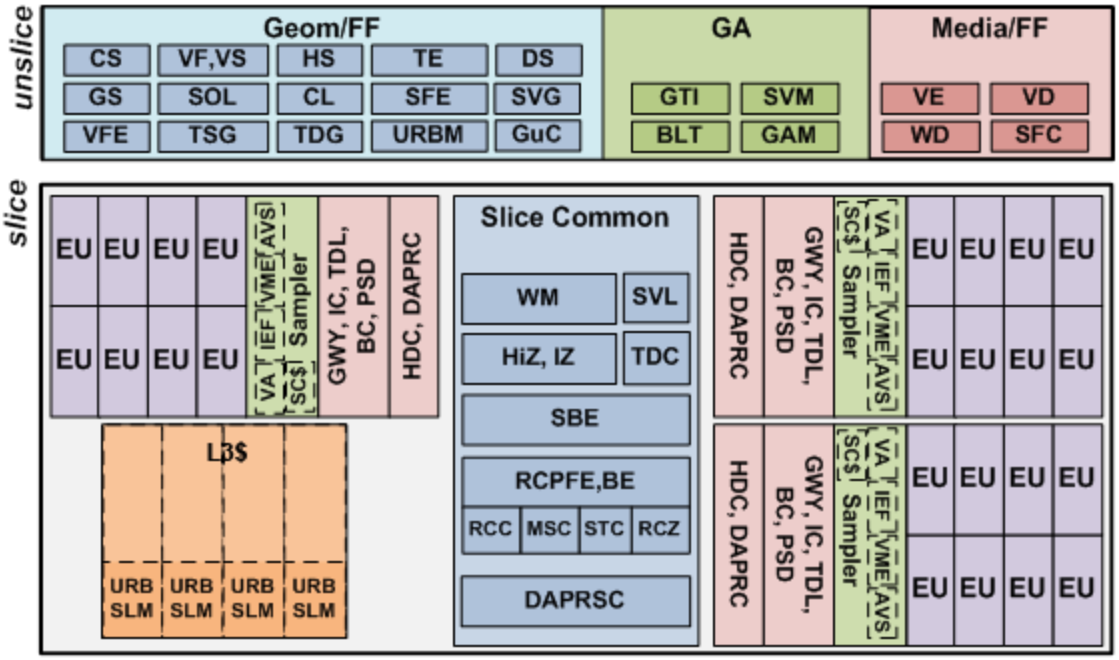
- Top Level Block Diagrams - Shows basic feature blocks of the project's graphics architecture, for GT configurations.
- Device Attributes - Lists details of the graphics configuration options for each project.
- Steppings and Device IDs - Lists all the current unique GT Die / Packages for a specific project.

Top Level Block Diagrams CFL

The diagrams below show basic feature blocks of the Gen9 Coffee Lake (CFL) graphics architecture.

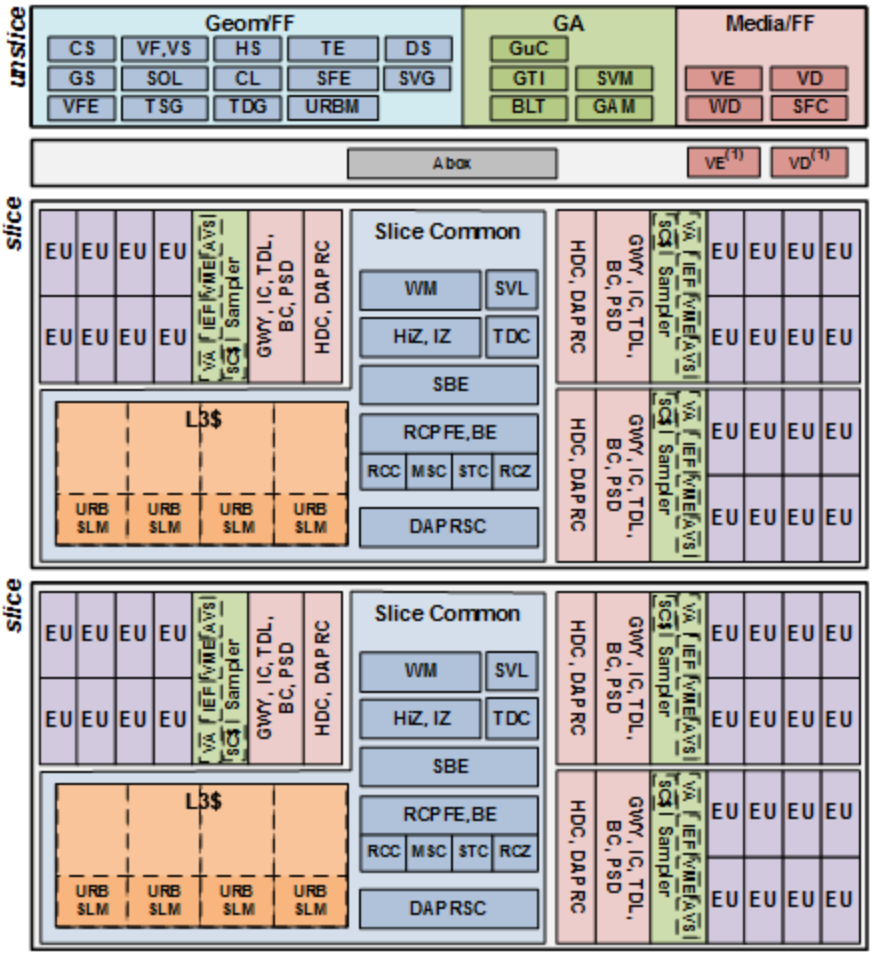
GT2 Configuration

The GT2 configuration contains one Unslice and one Slice with separate power domains for each, although they share a single clock domain.



GT3 Configuration

The GT3 configuration has an identical Unslice to GT2, except that it contains two Slices. Separate clock domains for the Unslice and Slice may be available depending on SKU. The L3 caches of each Slice combine to provide an aggregate L3 cache of twice the size and twice the bandwidth of a single instance. GT3 also has additional media blocks with second instance of VEBox and VDBox each.



This diagram is based on the following functional partitions:

(a) Geometry Fixed Functions (Geom/FF)

(b) Media Fixed Functions (Media/FF)

(c) Global Assets and GT Interface (GA)

(d) One or more Subslices (three shown)

(e) A Slice Common block

(f) An L3 Cache (L3$) block

Note that the combination of (a), (b), and (c) is typically referred to as the "unslice", while a combination of (d), (e), and (f) is referred to as a compute "slice".

The functionality in each of these groupings is further broken down as follows:

- Unslice – Fixed function pipelines for 3D, GPGPU, and Media operations, and interface to the outside world.
    - The 3D Geometry / Fixed Function (Geom/FF) block consisting of:
        - 3D fixed function pipeline (CS, VFVS, HS, TE, DS, GS, SOL, SL, SFE, SVG)

        - Video Front-End unit (VFE)
        - Thread Spawner unit (TSG) and the global Thread Dispatcher unit (TDG)
        - Unified Return Buffer Manager (URBM)
    - Media fixed function assets:
        - Video Decode (VD) Box
        - Video Encode (VE) Box
        - Wireless Display (WD) BOX
        - Scaler & Format Converter (SFC)
    - The Global Assets (GA) block as the primary interface and memory stream gateway to the outside world, consisting of:
        - GT Interface (GTI)
        - State Variable Manager (SVM)
        - Blitter (BLT)
        - Graphics Arbiter (GAM)
- Subslice (three shown) – A compute unit with supporting fixed- or shared-function assets sufficient for the EU capability.
    - A bank of Execution Units (EUs) – eight per subslice shown
    - Sampler, supporting both media and 3D functions
    - Gateway (GWY)
    - Instruction cache (IC)
    - Local Thread Dispatcher (TDL)
    - Barycentric Calculator (BC)
    - Pixel Shader Dispatcher (PSD)
    - Data Cluster (HDC)
    - Dataport Render Cache (DAPRC) - two per subslice
- Slice Common – Scalable fixed function assets which support the compute horsepower provided two or more subslices.
    - 3D Fixed Function:
        - Windower/Mask unit (WM)
        - Hi-Z (HZ) and Intermediate Z (IZ)
        - Setup Backend (SBE)
        - RCPFE, BE
        - 3D stream caches (RCC, MSC, STC, RCZ)
    - Media Fixed Functions:
        - DAPRSC
        - SVL

        - TDC
- L3 Cache – backing L3 cache for certain memory streams emanating from subslices.
    - L3 Data cache with support for data, URB, and shared local memory (SLM)

Device Attributes CFL

The following table lists detailed GT device attributes for proposed Coffee Lake (CFL) SKUs.

NOTE: This information is preliminary, and subject to change.

Product Configuration Attribute Table			
Product Family	**CFL**		
Architectural Name *	**1x2x6**	**1x3x8**	**2x3x8**
SKU Name	**GT1F**	**GT2**	**GT3**
Global Attributes			
Slice count	1	1	2
Subslice Count	2	3	6
EU/Subslice	6	8	8
EU count (total)	12	23 / 24 [b]	47 / 48 [b]
Thread Count	7	7	7
Thread Count (Total)	84	161 / 168	329 / 336
FLOPs/Clk - Half Precision, MAD (peak)	384	736 / 768	1504 / 1536
FLOPs/Clk - Single Precision, MAD (peak)	192	368 / 384	752 / 768
FLOPs/Clk - Double Precision, MAD (peak)	48	92 / 96	188 / 192
Unslice clocking (coupled/decoupled from Cr slice)	coupled	coupled	coupled
GTI / Ring Interfaces	1	1	1
GTI bandwidth (bytes/unslice-clk)	64: R	64: R	64: R
	64: W	64: W	64: W
eDRAM Support	N/A	N/A	0, 64MB
Graphics Virtual Address Range	48 bit	48 bit	48 bit
Graphics Physical Address Range	39 bit	39 bit	39 bit
Caches & Dedicated Memories			
L3 Cache, total size (bytes)	384K	768K	1536K
L3 Cache, bank count	2	4	8
L3 Cache, bandwidth (bytes/clk)	2x 64: R 2x 64: W	4x 64: R 4x 64: W	8x 64: R 8x 64: W
L3 Cache, D$ Size (Kbytes)	192K - 256K	512K	1024K
URB Size (kbytes)	128K - 192K	384K	768K
SLM Size (kbytes)	0, 128K	0, 192K	0, 384K
LLC/L4 size (bytes) [1]	~2MB/CPU core	~2MB/CPU core	~2MB/CPU core

Product Configuration Attribute Table			
Instruction Cache (IC, bytes)	2x 48K	3x 48K	6x 48K
Color Cache (RCC, bytes)	24K	24K	2x 24K
MSC Cache (MSC, bytes)	16K	16K	2x 16K
HiZ Cache (HZC, bytes)	12K	12K	2x 12K
Z Cache (RCZ, bytes)	32K	32K	2x 32K
Stencil Cache (STC, bytes)	8K	8K	2x 8K
Instruction Issue Rates			
FMAD, SP (ops/EU/clk)	8	8	8
FMUL, SP (ops/EU/clk)	8	8	8
FADD, SP (ops/EU/clk)	8	8	8
MIN,MAX, SP (ops/EU/clk)	8	8	8
CMP, SP (ops/EU/clk)	8	8	8
INV, SP (ops/EU/clk)	2	2	2
SQRT, SP (ops/EU/clk)	2	2	2
RSQRT, SP (ops/EU/clk)	2	2	2
LOG, SP (ops/EU/clk)	2	2	2
EXP, SP (ops/EU/clk)	2	2	2
POW, SP (ops/EU/clk)	1	1	1
IDIV, SP (ops/EU/clk)	1-6	1-6	1-6
TRIG, SP (ops/EU/clk)	2	2	2
FDIV, SP (ops/EU/clk)	1	1	1
Load/Store			
Data Ports (HDC)	2	3	6
L3 Load/Store (dwords/clk)	2x 64	3x 64	6x 64
SLM Load/Store (dwords/clk)	2x 64	3x 64	6x 64
Atomic Inc, 32b - sequential addresses (dwords/clk)	2x 64	3x 64	6x 64
Atomic Inc, 32b - same address (dwords/clk)	2x 4	3x 4	6x 4
Atomic CmpWr, 32b - sequential addresses (dwords/clk)	2x 32	3x 32	6x 32
Atomic CmpWr, 32b - same address (dwords/clk)	2x 4	3x 4	6x 4
3D Attributes			
Geometry pipes	1	1	1
Samplers (3D)	2	3	6
Texel Rate, point, 32b (tex/clk)	8	12	24

Product Configuration Attribute Table			
Texel Rate, point, 64b (tex/clk)	8	12	24
Texel Rate, point, 128b (tex/clk)	8	12	24
Texel Rate, bilinear, 32b (tex/clk)	8	12	24
Texel Rate, bilinear, 64b (tex/clk)	8	12	24
Texel Rate, bilinear, 128b (tex/clk)	2	3	6
Texel Rate, trilinear, 32b (tex/clk)	8	12	24
Texel Rate, trilinear, 64b (tex/clk)	4	6	12
Texel Rate, trilinear, 128b (tex/clk)	1	1.5	3
Texel Rate, aniso 2x, MIP Linear,, 32b (tex/clk)	2	3	6
Texel Rate, aniso 4x, MIP Linear,, 32b (tex/clk)	1	1.5	3
Texel Rate, aniso 8x, MIP Linear,, 32b (tex/clk)	0.5	0.75	1.5
Texel Rate, aniso 16x, MIP Linear,, 32b (tex/clk)	0.25	0.375	0.75
HiZ Rate, (ppc)	64	64	2x 64
IZ Rate, (ppc)	16	16	2x 16
Stencil Rate (ppc)	64	64	2x 64
(500 MHz, DDR-2400 or eDRAM; Range depends on dynamic compression ratio)			
Pixel Rate, fill, 32bpp (pix/clk, RCC hit)	8	8	16
Pixel Rate, fill, 32bpp (pix/clk, LLC hit @ 1.0x unslice clk) [2]			
Pixel Rate, fill, 32bpp (pix/clk, LLC hit, @ 1.5x unslice clk) [2]	N/A	N/A	
Pixel Rate, fill, 32bpp (pix/clk, memory, @ 1.0x unslice clk) [2]			
Pixel Rate, fill, 32bpp (pix/clk, memory, @ 1.5x unslice clk) [2]	N/A	N/A	
(500 MHz, DDR-2400 or eDRAM; Range depends on dynamic compression ratio)			
Pixel Rate, blend, 32bpp (p/clk, RCC hit)	8	8	16
Pixel Rate, blend, 32bpp (p/clk, LLC hit, @ 1.0x unslice clk) [2]			

Product Configuration Attribute Table			
Pixel Rate, blend, 32bpp (p/clk, LLC hit, @ 1.5x unslice clk) [2]	N/A	N/A	
Pixel Rate, blend, 32bpp (pix/clk, memory, @ 1.0x unslice clk) [2]			
Pixel Rate, blend, 32bpp (pix/clk, memory, @ 1.5x unslice clk) [2]	N/A	N/A	
Media Attributes			
Samplers (media)	2	3	6
VDBox Instances	1	1	2
VEBox Instances	1	1	2
SFC Instances	1	1	1
WGBox Instances	N/A	N/A	N/A
Display Attributes			
Display Pipes	3	3	3
Display Planes per Pipe	3	3	3
DDI ports	2	2	2
eDP ports	1	1	1

Footnotes:

* Architectural Name = Slice Count x Subslice Count x EUs per Subslice

[a] SKU naming & details has not yet been decided.

[b] One EU reserved for die recovery purposes.

[c] In the GT4 SKU, a decoupled unslice feature is supported, where the slice and unslice may operate on independent voltage planes (if supported by the platform), and may have independent clocking.

Steppings and Device IDs CFL

The following table lists currently proposed variations of GT Die / Packages for Gen9 Coffee Lake (CFL).

This information is preliminary, and subject to change at any time.

Segment	SKU	TDP	EUs	CPU Brand	Brand #	GFX Name	CPU Stepping	GT/Display Version	DID2 Grouping	DID2 8th Gen	Rev ID	POR	Notes
Mobile	U43e R	15	48	Core i7	645	Intel® Iris® Plus Graphics	D0	KBL I0 / KBL C0	1	3EA6	0x0	Y	Recycle for CFL U43e R
Mobile	U43e R	15	48	Core i5	645	Intel® Iris® Plus Graphics	D0	KBL I0 / KBL C0	1	3EA6	0x0	Y	Recycle for CFL U43e R
Mobile	U43e	28	47	Core i3	655	Intel® Iris® Plus Graphics	D0	KBL I0 / KBL C0	3	3EA8	0x0	Y	
Mobile	U43e	28	48	Core i5	655	Intel® Iris® Plus Graphics	D0	KBL I0 / KBL C0	4	3EA5	0x0	Y	Recycle for CFL U43e R
Mobile	U43e	28	48	Core i7	655	Intel® Iris® Plus Graphics	D0	KBL I0 / KBL C0	4	3EA5	0x0	Y	Recycle for CFL U43e R
Mobile	U2f2f	15	23	Core i3	620	Intel® UHD Graphics	D0	KBL I0 / KBL C0	20	3EA9	0x0	Y	Recovery SKUs based on U43e
Mobile	U42f	15	24	Core i5	620	Intel® UHD Graphics	D0	KBL I0/KBL C0	20	3EA9	0x0	Y	Recovery SKUs based on U43e
Mobile	U42f	15	24	Core i7	620	Intel® UHD Graphics	D0	KBL I0/KBL C0	20	3EA9	0x0	Y	Recovery SKUs based on U43e
Mobile	H4f2	35	23	Core i3	630	Intel® UHD Graphics	U0	CFL A0 / KBL C0	5	3E9B	0x0	Y	
Mobile	H4f2	45	23	Core i5	630	Intel® UHD Graphics	U0	CFL A0 / KBL C0	5	3E9B	0x0	Y	
Mobile/IOTG	H4f2	45	24	Core i5	630	Intel® UHD Graphics	U0	CFL A0 / KBL C0	5	3E9B	0x0	Y	
Mobile/IOTG	H62	45/65	24	Core i7	630	Intel® UHD Graphics	U0	CFL A0 / KBL C0	5	3E9B	0x0	Y	

Segment	SKU	TDP	EUs	CPU Brand	Brand #	GFX Name	CPU Stepping	GT/Display Version	DID2 Grouping	DID2 8th Gen	Rev ID	POR	Notes
Mobile/IOTG	H2f1f	45/65	12	Pentium	610	Intel® UHD Graphics	U0	CFL A0 / KBL C0	15	3E9C	0x0	Y	Fused down 6 cores SKUs
Mobile/IOTG	H2f1f	45/65	12	Celeron	610	Intel® UHD Graphics	U0	CFL A0 / KBL C0	15	3E9C	0x0	Y	Fused down 6 cores SKUs
Mobile	H82	45/65	24	Core i9	630	Intel® UHD Graphics	P0	CFL B0 / KBL C0	5	3E9B	0x1	Y	
Mobile	H82	45/65	24	Core i9	630	Intel® UHD Graphics	R0	CFL C0 / KBL C0	5	3E9B	0x2	Y	
Mobile	H6f2	45/65	24	Core i7	630	Intel® UHD Graphics	U0	CFL A0 / KBL C0	5	3E9B	0x0	Y	
Desktop	S2f1f	35/65	12	Celeron	610	Intel® UHD Graphics	B0	KBL F0 / KBL C0	6	3E93	0x0	Y	
Desktop	S2f1f	35/65	12	Pentium	610	Intel® UHD Graphics	B0	KBL F0 / KBL C0	6	3E93	0x0	Y	
Desktop/IOTG	S42	35/65/95	23	Core i3	630	Intel® UHD Graphics	B0	KBL F0 / KBL C0	7	3E91	0x0	Y	
Desktop	S2f2	35/65	23	Pentium	630	Intel® UHD Graphics	B0	KBL F0 / KBL C0	7	3E91	0x0	Y	
Desktop	S2f1f	35/65	12	Pentium	610	Intel® UHD Graphics	U0	CFL A0 / KBL C0	8	3E90	0x0	Y	
Desktop	S62	35/65	23	Core i5	630	Intel® UHD Graphics	U0	CFL A0 / KBL C0	9	3E92	0x0	Y	
Desktop/IOTG	S62	35/65/95	24	Core i5	630	Intel® UHD Graphics	U0	CFL A0 / KBL C0	9	3E92	0x0	Y	
Desktop/IOTG	S62	35/65/95	24	Core i7	630	Intel® UHD Graphics	U0	CFL A0 / KBL C0	9	3E92	0x0	Y	
Mobile WS	H62	45	24	Mobile Xeon	P630	Intel® UHD Graphics	U0	CFL A0 / KBL C0	10	3E94	0x0	Y	
Mobile WS	H82	45/65	24	Mobile Xeon	P630	Intel® UHD Graphics	P0	CFL B0 / KBL C0	10	3E94	0x1	Y	

Segment	SKU	TDP	EUs	CPU Brand	Brand #	GFX Name	CPU Stepping	GT/Display Version	DID2 Grouping	DID2 8th Gen	Rev ID	POR	Notes
Mobile WS	H82	45/65	24	Mobile Xeon	P630	Intel® UHD Graphics	R0	CFL C0 / KBL C0	10	3E94	0x2	Y	
Desktop WS	S62	65/80/95	24	Xeon	P630	Intel® UHD Graphics	U0	CFL A0 / KBL C0	11	3E96	0x0	Y	
Desktop WS	S4f2	65/71/83	24	Xeon	P630	Intel® UHD Graphics	U0	CFL A0 / KBL C0	11	3E96	0x0	Y	
Desktop	S82	95/65/35	24	Core i9	630	Intel® UHD Graphics	P0	CFL B0 / KBL C0	12	3E98	0x1	Y	
Desktop	S82	95/65/35	24	Core i7	630	Intel® UHD Graphics	P0	CFL B0 / KBL C0	12	3E98	0x1	Y	
Desktop	S6f2	95/65/35	24	Core i5	630	Intel® UHD Graphics	P0	CFL B0 / KBL C0	12	3E98	0x1	Y	
Desktop	S6f2	65/35	23	Core i5	630	Intel® UHD Graphics	P0	CFL B0 / KBL C0	12	3E98	0x1	Y	
Desktop	S6f1f	65/35	12	Core i7	610	Intel® UHD Graphics	P0	CFL B0 / KBL C0	13	3E99	0x1	Y	
Desktop	S4f1f	65/35	12	Core i3	610	Intel® UHD Graphics	P0	CFL B0 / KBL C0	13	3E99	0x1	Y	
Desktop	S2f1f	65/35	12	Pentium	610	Intel® UHD Graphics	P0	CFL B0 / KBL C0	13	3E99	0x1	Y	
Desktop WS	S82	95/80	24	Xeon	P630	Intel® UHD Graphics	P0	CFL B0 / KBL C0	14	3E9A	0x1	Y	
Desktop WS	S6f2	95/80	24	Xeon	P630	Intel® UHD Graphics	P0	CFL B0 / KBL C0	14	3E9A	0x1	Y	
Desktop	S82	95/65/35	24	Core i9	630	Intel® UHD Graphics	R0	CFL C0 / KBL C0	12	3E98	0x2	Y	
Desktop	S82	95/65/35	24	Core i7	630	Intel® UHD Graphics	R0	CFL C0 / KBL C0	12	3E98	0x2	Y	
Desktop	S6f2	95/65/35	24	Core i5	630	Intel® UHD Graphics	R0	CFL C0 / KBL C0	12	3E98	0x2	Y	
Desktop	S6f2	65/35	23	Core i5	630	Intel® UHD Graphics	R0	CFL C0 / KBL C0	12	3E98	0x2	Y	

Segment	SKU	TDP	EUs	CPU Brand	Brand #	GFX Name	CPU Stepping	GT/Display Version	DID2 Grouping	DID2 8th Gen	Rev ID	POR	Notes
Desktop	S6f1f	65/35	12	Core i7	610	Intel® UHD Graphics	R0	CFL C0 / KBL C0	13	3E99	0x2	Y	
Desktop	S4f1f	65/35	12	Core i3	610	Intel® UHD Graphics	R0	CFL C0 / KBL C0	13	3E99	0x2	Y	
Desktop	S2f1f	65/35	12	Pentium	610	Intel® UHD Graphics	R0	CFL C0 / KBL C0	13	3E99	0x2	Y	
Desktop WS	S82	95/80	24	Xeon	P630	Intel® UHD Graphics	R0	CFL C0 / KBL C0	14	3E9A	0x2	Y	
Desktop WS	S6f2	95/80	24	Xeon	P630	Intel® UHD Graphics	R0	CFL C0 / KBL C0	14	3E9A	0x2	Y	

Note-

****CFL GT baseline = KBL R G0**, with 4 additional ECOs on A0 stepping, and 1 additional ECO on 4+3e on top of A0 stepping.

Despite CFL4+3e is superset of CFL 6+2 and KBL-R, but in bug_de HSD the fixes for CFL 4+3e are marked as KBL I0, and it also does not have the HW changes to support 6 cores. Hence not being called as CFL B0 stepping but **KBL I0 to align with bug database.