Intel® Open Source HD Graphics Programmers' Reference Manual (PRM)

Volume 10: Display

For the 2014 Intel Atom™ Processors, Celeron™ Processors, and Pentium™ Processors based on the "BayTrail" Platform (ValleyView graphics)

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Introduction and Flows – Register Summary

This volume contains the register descriptions for the display portion of a family of integrated graphics devices. These registers do vary by devices within the family of devices so special attention needs to be paid to which devices use which registers and register fields.

Different devices within the family may add, modify, or delete registers or register fields relative to another device in the same family based on the supported functions of that device. Additional information on the use and programming of these registers can be found in the display chapter. This document covers both desktop and mobile products.

Address Range	Description
30000h–3FFFFh	Overlay Registers
05000h-05FFFh	GMBUS and I/O Control
06000h-06FFFh	Display Clocks and Clock Gating
0A000h–0AFFFh	Display Palette A/B Registers
60000h–600FFh	Display Pipeline A
61000h–610FFh	Display Pipeline B
61100h–611FFh	Display Port Control Registers
61200h-612FFh	Panel Fitting/Power Sequencing/LVDS Control
62000h-62FFFh	HD Audio Control
64000h-64FFFh	DisplayPort Registers
65000h-65FFFh	LPE Audio Registers
70000h–7FFFFh	Display Pipeline, Display Planes, Cursor Planes, and VGA Control Registers

Panel Control Register Summary

Address	Function	Name	NormalAccess	Panel Write Protect
61180h	Port Control	LVDS Port Control	RW	Yes
61200h	Panel Power Sequence	Panel power status	RO	NA
61204h		Panel Power Control	RW	No
61208h		Panel power on sequencing delay	RW	Yes
6120Ch		Panel power off sequencing delay	RW	Yes
61210h		Panel power cycle Delay and Reference	RW	Yes
61254h	Backlight Control	Backlight PWM Control	RW	No
61260h	BLM	Image BLM Control	RW	No
61270h–61284h		BLM Thresholds	RW	No
61290h–612A4h		BLM Accumulators	RO	NA
61300h	Panel Power Sequence - pipeB	Panel power status - pipeB	RO	NA
61304h		Panel Power Control - pipeB	RW	No
61308h		Panel power on sequencing delay - pipeB	RW	Yes
6130Ch		Panel power off sequencing delay - pipeB	RW	Yes
61310h		Panel power cycle Delay and Reference - pipeB	RW	Yes
61350h-61354h	Backlight Control - pipeB	Backlight PWM Control - pipeB	RW	No
61360h	BLM - pipeB	Image BLM Control - pipeB	RW	No
61370h–61384h		BLM Thresholds - pipeB	RW	No
61390h–613A4h		BLM Accumulators - pipeB	RO	NA

Display Pipe and Plane Control Registers

Address Range	Description
70000h – 70027h	Display Pipeline A Control
70028h – 7007Fh	Reserved
70080h – 7009Fh	Display Cursor Plane Registers A
700A0h – 700BFh	Reserved
700C0h – 70FFFh	Reserved
700C0h – 700DFh	Display Cursor Plane Registers B
700E0h – 70FFFh	Reserved
71000h – 7100Ch	Display Pipeline B Control
71010h – 7107Fh	Reserved
70180h – 7018Ch	Display A Plane Control
71090h – 7117Fh	Reserved
71180h – 7119Bh	Display B/Sprite Plane Control
711D0h – 713FFh	Reserved
71400h – 7140Fh	Video BIOS Registers
72010h – 720FFh	Reserved
72100h – 7217Fh	Reserved
72180h – 7219Fh	Sprite A Plane Control
721D0h – 721F7h	Sprite A Color Adjustment
72280h – 7229Fh	Sprite B Plane Control
722D0h – 722F7h	Sprite B Color Adjustment
72380h – 7239Fh	Sprite C Plane Control
723D0h – 723F7h	Sprite C Color Adjustment

72480h – 7249Fh	Sprite D Plane Control
724D0h – 724F7h	Sprite D Color Adjustment
72500h – 72FFFh	Reserved

Terminology

Description	Software Use	Should be implemented as
Reserved write as zero.	Software must always write a zero to these bits. This allows new features to be added using these bits that will be disabled when using old software and as the default case.	These are read only bits that always read as zeros or r/w bits that are default to zero.
Reserved write as one.	Software must always write a one to these bits. This allows new features to be added using these bits that will be disabled when using old software and as the default case.	
Reserved for BIOS Do not change	Driver access to these bits must read these bits that have been set through an initialization operation before writing this register so that the bits can remain unchanged.	According to each specific bit
Reserved for Video BIOS	These register bits will be used only by video BIOS and drivers should not change them.	These are read/write bits that have no hardware function. They are intended for use by the video BIOS for storage.
Reserved for Compatibility	For functions that are no longer needed these bits had old use, but now does nothing. New software should use the new method.	Read write bits that have no functions.
Use for compatibility only	Under specific conditions, these bits functions as in the old part, new software should use the new method.	According to each specific bit
Read Only	This bit is read only. The read value is determined by hardware. Writes to this bit have no effect.	According to each specific bit. The bit value is determined by hardware and not affected by register writes to the actual bit.
Reserved read only	Don't assume a value for these bits. Writes have no effect.	These bits should read as zero.

Reserved read only write as zero	Don't assume a value for these bits, always write a zero.	These bits should read as zero.
Read/Clear	This bit can be read and writes to it with a one cause the bit to clear.	Hardware events cause the bit to be set and the bit will be cleared on a write operation where the corresponding bit has a one for a value.
Read/Write	This bit can be read or written.	
Double Buffered	Write when desired	Takes effect only after a particular event such as a VBLANK.

Register Protection for Panel Protection

During panel on sequence write protect mechanism is enabled and doesn't let the SW configure some registers in order to create atomic turn on process. The process is started by writing register PP_Control[31:16] (61204) different value then 16'hABCD that prohibits and write access to some registers. Cancelling the write protect mode is done by writing 16'hABCD to this register. The write-protected registers are (LVDS and Panel sequencing Registers):

- LVDS – Digital Display Port Control (61180h)
- Panel power on sequencing delays (61208h)
- Panel power off sequencing delays (6120Ch)
- Panel power cycle delay and Reference Divisor (61210h)
- DPLL Control Registers
- HTOTAL—Horizontal Total Register
- HBLANK—Horizontal Blank Register
- HSYNC - Horizontal Sync Register
- VTOTAL -Vertical Total Register
- VBLANK -Vertical Blank Register
- VSYNC - Vertical Sync Register

Display Mode Set Sequence

Pipe register double-buffering

The registers that are double buffered are first stored and only update when the pipe condition allowed it without harming the frames visually. Two types of registers are

- Pipe config registers (0x70008 0x71008):

Contain pipe enable, double wide, gamma mode, interlaced mode, plane enable overrides, frame start delay, force border.

Those registers updates at Vblank or updates if pipe completely off or updates if VGA native and enabled

- Pipe timing registers (60000/4/8/C/10/14/1C 61000/4/8/C/10/14/1C):

Contain horizontal and vertical total, active, blank start/end, sync start/end, source size.

Those registers update at Vblank after pipe config enable written 0 to 1, or updates if DPLL off or pipe completely off and pipe config register written

For pipe disabling, the pipe will not completely turn off until the start of vertical blank after the pipe enable was written to 0. If there will not be vertical blank the pipe will not be able to completely turn off. Double-buffering is bypassed if VGA native display is enabled (0x71400 bits 31,25,24 set to 0), allowing pipe to turn off immediately.

Enabling pipe always occurs instantly.

Display Pixel Rate Limitations

The maximum display pixel rate is limited by factors including the memory bandwidth and latency available to display, maximum watermark values, maximum display PLL frequencies, maximum bandwidth supported by the port technology, and restrictions within the display pipes.

Within a display pipe the restrictions on the maximum pixel rate are based on the planes enabled, the pixel format of those planes, panel fitting scaling. The restriction is found with the following formula:

```
// Find the ratio for each plane
    For each enabled plane with primary and 2 sprites {
        If both sprites and primary planes are enabled {
            If pixel format is 32bpp {Plane Ratio = 16/18}
            Else If pixel format is 64bpp {Plane Ratio = 8/11}
            Else {Plane Ratio = 1/1}
        }
    }
    For each enabled plane with primary and 1 sprite {
        If both sprite and primary planes are enabled {
            If pixel format is 32bpp {Plane Ratio = 16/17}
            Else If pixel format is 64bpp {Plane Ratio = 8/10}
            Else {Plane Ratio = 1/1}
        }
        Else If only a single plane is enabled {
```

```
                If pixel format is 64bpp {Plane Ratio = 8/9}
                Else {Plane Ratio = 1/1}
            }
        }
// Select the worst ratio, Cursor does not contribute to any restrictions on pipe ratio
        Pipe Ratio = Plane Ratio
// Adjust for panel fitter horizontal down-scaling
        If panel fitting is enabled and panel fitter window horizontal size < pipe horizontal source size {
        Pipe Ratio = Pipe Ratio * (panel fitter window horizontal size / pipe horizontal source size)
        }
// Adjust for 90% rule
        Pipe Ratio = Minimum(Pipe Ratio, 9/10)
```

The resulting Pipe Ratio gives the ratio of the maximum allowed pixel rate for this display pipe divided by the core display clock frequency (CDCLK).

On Valleyview, the core display clock frequency is 320 MHz at vnnmin

Example Primary plane 32bpp, sprite plane 16bpp, panel fitting down-scaling 1/1.12:

Primary ratio = 16/17

Pipe ratio = 16/17 * 1/1.12

Maximum pixel rate = 16/17 * 1/1.12 * 320 MHz = 268 MHz

Example Primary plane 64bpp, sprite plane 32bpp, no panel fitting:

Primary ratio = 8/10

Pipe ratio = 8/10

Maximum pixel rate = 8/10 * 320 MHz = 256 MHz

Mode switch programming sequences

Mode switch stands for a flow of pipe that is going to be changed by disabling/enabling it or change its configuration. Those changes need to be done under certain of some rolls as described below:

- DPLL must be enabled and warmed up before pipe or ports are enabled.
- DPLL must be kept enabled until ports are disabled and pipe is completely off.
- DPLL frequency must not be changed until ports are disabled and pipe is completely off, except at ACA mode
- Planes must be disabled before pipe is disabled or pipe timings changed.
- During normal mode set, panelfitter must be enabled or disabled only when pipe is completely off.
- Duiring fast mode set, panelfitter can be enabled or disabled when the pipe is still on

- The internal CRT ports can be left on during a mode switch if DPLL is not touched.
- Ports can be freely enabled or disabled on a running pipe, except when port multiply needs to be changed.
- Wait for pipe off status (using pipe config register bit 30) is the best way to find when pipe is completely off.

Power On Sequence

In order to turn on the DSP the SW should acts using the next sequence:

- In case of after chip power up:
    - Configure the modesel [3:2] and SFR [1] at DPIO_CFG (GVD)
    - Assert the common lane reset [0] of DPIO_CFG (GVD)
- Enable the ref enable for DPLL A/B using DPLLA_CTL/DPLLB_CTL[29] (without enabling it the registers of this DPLL cannot be configured)
- Program corresponding DDI0/DDI1 Tx lane resets set to default
    - DDI0 (0x8200 = 0x00010080; 0x8204 = 0x00600060)
    - DDI1 (0x8400 = 0x00010080; 0x8404 = 0x00600060)
    - VLV HDMI Inter-pair Skew Fix IOSFSB DPIO CRI Write for B0
        - DDI0
            - 0x8230 = 0x00750F00 (stagger settings for tx1/tx2)
            - 0x82AC = 0x00001500 (Latency optim set to -2UI)
            - 0x82B8 = 0x40400000 (Set common rdload mode)
        - DDI1
            - 0x8430 = 0x00750F00 (stagger settings for tx1/tx2)
            - 0x84AC = 0x00001500 (Latency optim set to -2UI)
            - 0x84B8 = 0x40400000 (Set common rdload mode)
- Configure DPLL A/B parameters using DPIO_Packet/Data indirect access registers (GVD)
- Enable DPLL A/B using DPLLA_CTL/DPLLB_CTL[31]
- Wait for DPLL A/B lock (112usec if calibration is required or 42usec if calibration is not required) or pull lock A/B bit at DPLLA_CTL/DPLLB_CTL[15]
- Program pipe timings registers (60000/4/8/C/10/14/1C 61000/4/8/C/10/14/1C) - Can be done before DPLL programming
- Enable panelfitter as needed - Can be done before DPLL and/or pipe timings programming
- Enable ports
- Wait for DPIO phystatus ready in 6014
- Enable pipe A/B
- Enable planes (VGA or hires)

When using Self Refresh mode and one pipe is active while the second pipe is being enabled or disabled, the workaround sequence below needs to be followed. This does not need to done when both pipes are being enabled or disabled at the same time.

When turning on a second pipe:

1. Disable Self Refresh (register 0x20E0 bit 15 set to 0).
2. Wait for vblank from first pipe (frame is ended and the pipe will use only his part at the ddbm during next frames)
3. Enable second pipe using the mode switch enable sequence as normal.

Power Off Sequence

In order to turn off the DSP the SW should acts using the next sequence:

- Disable ports
- Disable planes (VGA or hires)
- Disable pipe
- Disable VGA display in 0x71400 bit 31 (Disable VGA display done after disable pipe to allow pipe to turn off when no vblank is available in native VGA mode)
- Wait for pipe off status (eliminate any wait state in between wait for pipe off and disable DPLL)
- Disable panelfitter
- Assert corresponding TX lane reset for the port B (DDI0) or port C (DDI1)
    - DDI0 (0x8200 = 0x00000000; 0x8204 = 0x00E00060)
    - DDI1 (0x8400 = 0x00000000; 0x8404 = 0x00E00060)
- Disable DPLL

When using Self Refresh mode and one pipe is active while the second pipe is being enabled or disabled, the workaround sequence below needs to be followed. This does not need to done when both pipes are being enabled or disabled at the same time.

When turning off a second pipe:

1. Disable second pipe using the power off sequence as normal.
2. Anytime after the step in the disable sequence where there is a wait for pipe off status, re-enable Self Refresh if desired (register 0x20E0 bit 15 set to 1).

DRRS / ACA / MAX_FIFO modes

At this three modes the frequency of the DPLL is need to change for LVDS monitors but without causing any harm to the viewer (seamless). All those switches are done during vblank (second raw) and need to be done in less than 100usec (due to LVDS panel's restrictions).

DRRS (Dynamic Rate Refresh Switch) – Changing the dot clock frequency without changing the timing in order to reduce power when working on battery and only primary is working and in static/quasi static mode and hence seamless to the viewer. This ability count on better led's at the panel that holds the

luminance for longer time (less refresh rate is required). The refresh rate frequency can be changed from 60Hz (normal) to 50Hz or 40Hz.

ACA (Adaptive Clock Architecture) – Changing the dot clock frequency due to EMI issues with the wireless (LVDS transmitter harmonic influence the wireless quality). This changing can be done only in small steps (up to 1%) in order not to harm the frame.

MAX FIFO – Changing the dot clock when the DSP is moving to MAX FIFO mode (using the entire DDBM for one pipe) when the chip enter to refresh mode.

DRRS/ACA Flow:

- Pipe is active using LVDS port and PIPECONFIG[17:16] (70008h) is written to be 2'b0.
- The SW configures the new dividers of the DPLL (double buffered at the DPIO) using the DPIO packet/data indirect access registers.
- The SW switch bit [8] at DPLLA/B_CTL
- The DSP HW wait to the next vblank and at the start of the second raw disable the DPLL
- The DPIO HW disable the DPLL and stop providing dot and lvds clocks
- The DSP HW stops transmitting bits to the LVDSIO and drive0
- The DSP HW enable the DPLL after 0.5usec
- The DPIO HW enable the DPLL with the new set of dividers
- The DPIO locked after 41.5 usec and provide updated lvds and dot clocks
- The DSP HW continue transmitting pixels from the point it stopped (vblank area)

Pipe switch Sequence

Pipe switch is mode when sprite or overlay is changing position from pipeA to pipeB and vice versa. This switching is done without disabling any of the pipes and seamless to the viewer.

Flow:

- Switch the SP/OV plane (OV – OCONFIG[18], SP – DSPCCNTR[25:24])
- DSP HW wait to VBLANK of current pipe and stop transmitting pixels using SP/OV
- DSP HW wait to VBLANK of the next pipe and start fetching pixels using SP/OV

GMBUS and I/O Control Registers (05000h–05FFFh)

GPIO Pin Usage (By Functions)

GPIO pins allow the support of simple query and control functions such as DDC and I^2C interface protocols. GPIO pins exist in pairs (for the most part) and provide a mechanism to control external devices through a register programming interface. GPIO pins can be set to a level or the value of the pin can be read. This allows for a "bit banging" version of an I2C interface to be implemented. An additional function of using the GMBUS engine to run the I2C protocols is also allowed. Refer to the *CSpec* for GPIO signal descriptions. Refer to the *Philips I2C-BUS SPECIFICATION version 2.1* for a description of the I2C bus and protocol.

The number and names of the GPIO pins vary from device type to device type. Some of the GPIO pins will be muxed with other functions and are only available when the other function is not being used. The following subsections describe the GPIO pin to register mapping for the various devices. OEMs have the ability to remap these functions onto other pins as long as the hardware limitations are observed.

GPIO Pin Usage (By Device)

GPIO Control Reg	Pin Use (Name)	GMBUS Use	Internal Pullup	I^2C	Device	Description
7	Reserved	No	No			
	Reserved					
6	Reserved	No	No			
	Reserved					
5	Reserved	No	No			
	Reserved					
4	HDMIB/DPB CTLDATA	Yes	No – weak pulldown on reset	Yes	All	DDC for HDMI/DP connection via the integrated HDMI/DP display port B.
	HDMIB/DPB CTLCLK			Yes		
3	HDMIC/DPC CTLDATA	Yes	No –weak pulldown on reset	Yes	All	DDC for HDMI/DP connection via the integrated HDMI/DP display port C.
	HDMIC/DPC			Yes		

	CTLCLK					
2	Reserved	No	No			
	Reserved					
1	DDI2 DDC Data	Yes	No - weak pulldown on reset	Yes		DDC for MIPI connection via the integrated MIPI port .
	DDI2 DDC Clock			Yes		
0	DAC DDC Data (DDCADATA)	Yes	No	Yes	All	DDC for Analog monitor (VGA) connection. This cannot be shared with other DDC or I2C pairs due to legacy monitor issues.
	DAC DDC Clock (DDCACLK)			Yes		

GPIO Control Registers

This section describes the GPIO control registers.

GPIOCTL_0—GPIO Control Register 0

Address offset : 05010h

Default value : 00h, 00h, 000U1000b, 000U1000b

Normal Access : Read / Write

Size :32 bit

Description: GPIO I2C register (gmbus_register.v – reg_gpio0, reg_gpio1, reg_gpio2. reg_gpio3, reg_gpio4)

These registers define the control of the sets of the so called “general purpose” I/O pins. Each register controls a pair of pins that while can be used for general purpose control, most are designated for specific functions according to the requirements of the device and the system that the device finds itself in. Each pin of the two pin pair is designated as a clock or data for descriptive purposes. See the table at the beginning of this section to determine for each product which pins/registers are supported and their intended functions. **Board design variations are possible and would affect the usage of these pins.**

Bit	Description
31:13	Reserved

12	**GPIO_Data In—RO:** This is the value that is sampled on the GPIO_Data pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
11	**GPIO Data Value—R/W:** This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if **GPIO DATA MASK** is also asserted. The value will appear on the pin if this data value is actually written to this register and the **GPIO Data DIRECTION VALUE** contains a value that will configure the pin as an output. **Default = 1.** The GPIO default clock data value is programmed to '1' in hardware. The hardware drives a default of '1' since the I2C interface defaults to a '1'. (this mimics the I2C external pull-ups on the bus)
10	**GPIO Data Mask—WO:** This is a mask bit to determine whether the **GPIO DATA VALUE** bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT write GPIO Data Value bit (default). 1 = Write GPIO Data Value bit. AccessType: Write Only
9	**GPIO Data Direction Value—R/W:** This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if **GPIO Data DIRECTION MASK** is also asserted. The value that will appear on the pin is defined by what is in the register for the **GPIO DATA VALUE** bit. 0 = Pin is configured as an input (default) 1 = Pin is configured as an output.
8	**GPIO Data Direction Mask—WO:** This is a mask bit to determine whether the **GPIO DIRECTION VALUE** bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Data Direction Value bit (default). 1 = Write GPIO Data Direction Value bit. AccessType: Write Only
7:5	Reserved: must be written with zeros.
4	**GPIO Clock Data In—RO:** This is the value that is sampled on the GPIO Clock pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only

3	**GPIO Clock Data Value—R/W:** This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if **GPIO Clock DATA MASK** is also asserted. The value will appear on the pin if this data value is actually written to this register and the **GPIO Clock DIRECTION VALUE** contains a value that will configure the pin as an output. **Default = 1.** The GPIO default clock data value is programmed to '1' in hardware. The hardware drives a default of '1' since the I2C interface defaults to a '1'. (this mimics the I2C external pull-ups on the bus)
2	**GPIO Clock Data Mask—WO:** This is a mask bit to determine whether the **GPIO Clock DATA VALUE** bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Clock Data Value bit (default). 1 = Write GPIO Clock Data Value bit. AccessType: Write Only
1	**GPIO Clock Direction Value—R/W:** This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if **GPIO Clock DIRECTION MASK** is also asserted. The value that will appear on the pin is defined by what is in the register for the **GPIO Clock DATA VALUE** bit. 0 = Pin is configured as an input and the output driver is set to tri-state (default) 1 = Pin is configured as an output.
0	**GPIO Clock Direction Mask—WO:** This is a mask bit to determine whether the **GPIO Clock DIRECTION VALUE** bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT update the GPIO Clock Direction Value bit on a write (default). 1 = Update the GPIO Clock Direction Value bit. on a write operation to this register. AccessType: Write Only

GPIOCTL_1—GPIO Control Register 1

Address offset : 05014h

Default value : 00h, 00h, 000U1000b, 000U1000b

Normal Access : Read / Write

Size :32 bit

Description: GPIO I2C register (gmbus_register.v – reg_gpio0, reg_gpio1, reg_gpio2. reg_gpio3, reg_gpio4)

These registers define the control of the sets of the so called "general purpose" I/O pins. Each register controls a pair of pins that while can be used for general purpose control, most are designated for specific functions according to the requirements of the device and the system that the device finds itself in. Each pin of the two pin pair is designated as a clock or data for descriptive purposes. See the table at the beginning of this section to determine for each product which pins/registers are supported and their intended functions. **Board design variations are possible and would affect the usage of these pins.**

Bit	Description
31:13	Reserved:
12	**GPIO_Data In—RO:** This is the value that is sampled on the GPIO_Data pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
11	**GPIO Data Value—R/W:** This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if **GPIO DATA MASK** is also asserted. The value will appear on the pin if this data value is actually written to this register and the **GPIO Data DIRECTION VALUE** contains a value that will configure the pin as an output. **Default = 1.** The GPIO default clock data value is programmed to '1' in hardware. The hardware drives a default of '1' since the I2C interface defaults to a '1'. (this mimics the I2C external pull-ups on the bus)
10	**GPIO Data Mask—WO:** This is a mask bit to determine whether the **GPIO DATA VALUE** bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT write GPIO Data Value bit (default). 1 = Write GPIO Data Value bit. AccessType: Write Only
9	**GPIO Data Direction Value—R/W:** This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if **GPIO Data**

	DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the **GPIO DATA VALUE** bit. 0 = Pin is configured as an input (default) 1 = Pin is configured as an output.
8	**GPIO Data Direction Mask—WO:** This is a mask bit to determine whether the **GPIO DIRECTION VALUE** bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Data Direction Value bit (default). 1 = Write GPIO Data Direction Value bit. AccessType: Write Only
7:5	Reserved: must be written with zeros.
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1	**GPIO Clock Direction Value—R/W:** This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if **GPIO Clock DIRECTION MASK** is also asserted. The value that will appear on the pin is defined by what is in the register for the **GPIO Clock DATA VALUE** bit. 0 = Pin is configured as an input and the output driver is set to tri-state (default) 1 = Pin is configured as an output.

0	**GPIO Clock Direction Mask—WO:** This is a mask bit to determine whether the **GPIO Clock DIRECTION VALUE** bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT update the GPIO Clock Direction Value bit on a write (default). 1 = Update the GPIO Clock Direction Value bit. on a write operation to this register. AccessType: Write Only

GPIOCTL_2—GPIO Control Register 2

Address offset : 05018h

Default value : 00h, 00h, 000U1000b, 000U1000b

Normal Access : Read / Write

Size :32 bit

Description: GPIO I2C register (gmbus_register.v – reg_gpio0, reg_gpio1, reg_gpio2. reg_gpio3, reg_gpio4)

These registers define the control of the sets of the so called “general purpose” I/O pins. Each register controls a pair of pins that while can be used for general purpose control, most are designated for specific functions according to the requirements of the device and the system that the device finds itself in. Each pin of the two pin pair is designated as a clock or data for descriptive purposes. See the table at the beginning of this section to determine for each product which pins/registers are supported and their intended functions. **Board design variations are possible and would affect the usage of these pins.**

Bit	Description
31:13	Reserved:
12	**GPIO_Data In—RO:** This is the value that is sampled on the GPIO_Data pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
11	**GPIO Data Value—R/W:** This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if **GPIO DATA MASK** is also asserted. The value will appear on the pin if this data value is actually written to this register and the **GPIO Data DIRECTION VALUE** contains a value that will configure the pin as an output. **Default = 1.** The GPIO default clock data value is programmed to ‘1’ in hardware. The hardware drives a default of ‘1’ since the I2C interface defaults to a ‘1’. (this mimics the I2C external pull-ups on the bus)
10	**GPIO Data Mask—WO:** This is a mask bit to determine whether the **GPIO DATA VALUE** bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT write GPIO Data Value bit (default).

	1 = Write GPIO Data Value bit. AccessType: Write Only
9	**GPIO Data Direction Value—R/W:** This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if **GPIO Data DIRECTION MASK** is also asserted. The value that will appear on the pin is defined by what is in the register for the **GPIO DATA VALUE** bit. 0 = Pin is configured as an input (default) 1 = Pin is configured as an output.
8	**GPIO Data Direction Mask—WO:** This is a mask bit to determine whether the **GPIO DIRECTION VALUE** bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Data Direction Value bit (default). 1 = Write GPIO Data Direction Value bit. AccessType: Write Only
7:5	Reserved: must be written with zeros.
4	**GPIO Clock Data In—RO:** This is the value that is sampled on the GPIO Clock pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
3	**GPIO Clock Data Value—R/W:** This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if **GPIO Clock DATA MASK** is also asserted. The value will appear on the pin if this data value is actually written to this register and the **GPIO Clock DIRECTION VALUE** contains a value that will configure the pin as an output. **Default = 1.** The GPIO default clock data value is programmed to '1' in hardware. The hardware drives a default of '1' since the I2C interface defaults to a '1'. (this mimics the I2C external pull-ups on the bus)
2	**GPIO Clock Data Mask—WO:** This is a mask bit to determine whether the **GPIO Clock DATA VALUE** bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Clock Data Value bit (default). 1 = Write GPIO Clock Data Value bit. AccessType: Write Only
1	**GPIO Clock Direction Value—R/W:** This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if **GPIO Clock DIRECTION MASK** is also asserted. The value that will appear on the pin is defined by what is in the register for the **GPIO Clock DATA VALUE** bit. 0 = Pin is configured as an input and the output driver is set to tri-state (default) 1 = Pin is configured as an output.
0	**GPIO Clock Direction Mask—WO:** This is a mask bit to determine whether the **GPIO Clock DIRECTION VALUE** bit should be written into the register. This value is not stored and when read returns 0.

	0 = Do NOT update the GPIO Clock Direction Value bit on a write (default). 1 = Update the GPIO Clock Direction Value bit. on a write operation to this register. AccessType: Write Only

GPIOCTL_3—GPIO Control Register 3

Address offset : 0501Ch

Default value : 00h, 00h, 000U1000b, 000U1000b

Normal Access : Read / Write

Size :32 bit

Description: GPIO I2C register (gmbus_register.v – reg_gpio0, reg_gpio1, reg_gpio2. reg_gpio3, reg_gpio4)

These registers define the control of the sets of the so called "general purpose" I/O pins. Each register controls a pair of pins that while can be used for general purpose control, most are designated for specific functions according to the requirements of the device and the system that the device finds itself in. Each pin of the two pin pair is designated as a clock or data for descriptive purposes. See the table at the beginning of this section to determine for each product which pins/registers are supported and their intended functions. **Board design variations are possible and would affect the usage of these pins.**

Bit	Description
31:13	Reserved:
12	**GPIO_Data In—RO:** This is the value that is sampled on the GPIO_Data pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
11	**GPIO Data Value—R/W:** This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if **GPIO DATA MASK** is also asserted. The value will appear on the pin if this data value is actually written to this register and the **GPIO Data DIRECTION VALUE** contains a value that will configure the pin as an output. **Default = 1.** The GPIO default clock data value is programmed to '1' in hardware. The hardware drives a default of '1' since the I2C interface defaults to a '1'. (this mimics the I2C external pull-ups on the bus)
10	**GPIO Data Mask—WO:** This is a mask bit to determine whether the **GPIO DATA VALUE** bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT write GPIO Data Value bit (default). 1 = Write GPIO Data Value bit. AccessType: Write Only
9	**GPIO Data Direction Value—R/W:** This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if **GPIO Data**

	DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the **GPIO DATA VALUE** bit. 0 = Pin is configured as an input (default) 1 = Pin is configured as an output.
8	**GPIO Data Direction Mask—WO:** This is a mask bit to determine whether the **GPIO DIRECTION VALUE** bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Data Direction Value bit (default). 1 = Write GPIO Data Direction Value bit. AccessType: Write Only
7:5	Reserved: must be written with zeros.
4	**GPIO Clock Data In—RO:** This is the value that is sampled on the GPIO Clock pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
3	**GPIO Clock Data Value—R/W:** This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if **GPIO Clock DATA MASK** is also asserted. The value will appear on the pin if this data value is actually written to this register and the **GPIO Clock DIRECTION VALUE** contains a value that will configure the pin as an output. **Default = 1.** The GPIO default clock data value is programmed to '1' in hardware. The hardware drives a default of '1' since the I2C interface defaults to a '1'. (this mimics the I2C external pull-ups on the bus)
2	**GPIO Clock Data Mask—WO:** This is a mask bit to determine whether the **GPIO Clock DATA VALUE** bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Clock Data Value bit (default). 1 = Write GPIO Clock Data Value bit. AccessType: Write Only
1	**GPIO Clock Direction Value—R/W:** This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if **GPIO Clock DIRECTION MASK** is also asserted. The value that will appear on the pin is defined by what is in the register for the **GPIO Clock DATA VALUE** bit. 0 = Pin is configured as an input and the output driver is set to tri-state (default) 1 = Pin is configured as an output.
0	**GPIO Clock Direction Mask—WO:** This is a mask bit to determine whether the **GPIO Clock DIRECTION VALUE** bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT update the GPIO Clock Direction Value bit on a write (default). 1 = Update the GPIO Clock Direction Value bit. on a write operation to this register. AccessType: Write Only

GPIOCTL_4—GPIO Control Register 4

Address offset : 05020h

Default value : 00h, 00h, 000U1000b, 000U1000b

Normal Access : Read / Write

Size :32 bit

Description: GPIO I2C register (gmbus_register.v – reg_gpio0, reg_gpio1, reg_gpio2. reg_gpio3, reg_gpio4)

These registers define the control of the sets of the so called "general purpose" I/O pins. Each register controls a pair of pins that while can be used for general purpose control, most are designated for specific functions according to the requirements of the device and the system that the device finds itself in. Each pin of the two pin pair is designated as a clock or data for descriptive purposes. See the table at the beginning of this section to determine for each product which pins/registers are supported and their intended functions. **Board design variations are possible and would affect the usage of these pins.**

Bit	Description
31:13	Reserved:
12	**GPIO_Data In—RO:** This is the value that is sampled on the GPIO_Data pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
11	**GPIO Data Value—R/W:** This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if **GPIO DATA MASK** is also asserted. The value will appear on the pin if this data value is actually written to this register and the **GPIO Data DIRECTION VALUE** contains a value that will configure the pin as an output. **Default = 1.** The GPIO default clock data value is programmed to '1' in hardware. The hardware drives a default of '1' since the I2C interface defaults to a '1'. (this mimics the I2C external pull-ups on the bus)
10	**GPIO Data Mask—WO:** This is a mask bit to determine whether the **GPIO DATA VALUE** bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT write GPIO Data Value bit (default). 1 = Write GPIO Data Value bit. AccessType: Write Only
9	**GPIO Data Direction Value—R/W:** This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if **GPIO Data DIRECTION MASK** is also asserted. The value that will appear on the pin is defined by what is in the register for the **GPIO DATA VALUE** bit. 0 = Pin is configured as an input (default) 1 = Pin is configured as an output.

8	**GPIO Data Direction Mask—WO:** This is a mask bit to determine whether the **GPIO DIRECTION VALUE** bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Data Direction Value bit (default). 1 = Write GPIO Data Direction Value bit. AccessType: Write Only
7:5	Reserved: must be written with zeros.
4	**GPIO Clock Data In—RO:** This is the value that is sampled on the GPIO Clock pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
3	**GPIO Clock Data Value—R/W:** This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if **GPIO Clock DATA MASK** is also asserted. The value will appear on the pin if this data value is actually written to this register and the **GPIO Clock DIRECTION VALUE** contains a value that will configure the pin as an output. **Default = 1.** The GPIO default clock data value is programmed to '1' in hardware. The hardware drives a default of '1' since the I2C interface defaults to a '1'. (this mimics the I2C external pull-ups on the bus)
2	**GPIO Clock Data Mask—WO:** This is a mask bit to determine whether the **GPIO Clock DATA VALUE** bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Clock Data Value bit (default). 1 = Write GPIO Clock Data Value bit. AccessType: Write Only
1	**GPIO Clock Direction Value—R/W:** This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if **GPIO Clock DIRECTION MASK** is also asserted. The value that will appear on the pin is defined by what is in the register for the **GPIO Clock DATA VALUE** bit. 0 = Pin is configured as an input and the output driver is set to tri-state (default) 1 = Pin is configured as an output.
0	**GPIO Clock Direction Mask—WO:** This is a mask bit to determine whether the **GPIO Clock DIRECTION VALUE** bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT update the GPIO Clock Direction Value bit on a write (default). 1 = Update the GPIO Clock Direction Value bit. on a write operation to this register. AccessType: Write Only

GMBUS Controller Programming Interface

The GMBUS (Graphic Management Bus) can be used to indirectly access/control devices connected to a GMBUS bus as an alternate to bit-wise programming via software. The GMBUS interface is I^2C compatible.

The basic features are listed as follow:

1. Works as the master of a single master bus.
2. The bus clock frequency is selectable by software to be 50KHz, 100KHz, 400KHz , and 1MHz
3. The GMBUS controller can be attached to the selected GPIO pin pairs.
4. 7 or 10-Bit Slave Address and 8- or 16-bit index.
5. Hardware byte counter to track the data transmissions/reception
6. Timing source from 250MHz un-gated PCI-Express clock.
7. There is a double buffered data register and a 9 bit counter to support 0 byte to 256 byte transfers.
8. The slave device can cause a stall by pulling down the clock line (Slave Stall), or delay the slave acknowledges response.
9. The master controller detects and reports time out conditions for a stall from a slave device or delayed or missing slave acknowledge.
10. Interrupt may optionally be generated from a GMBUS Timeout error.

The byte counter register is a read/write register, and in receiving mode, is used to track the data bytes received. There is a status register to indicate the error condition, data buffer busy, time out, and data complete acknowledgement. There is no support for ring buffer based operation of GMBUS. The GMBUS is controlled by a set of memory mapped IO registers. Status is reported through the GMBUS status register.

GMBUS0—GMBUS Clock/Port Select

Address Offset:05100h

Default Value: 0000 0000h

Normal Access: Read/WriteSize: 32 bits

Double Buffered:No

Description: gmbus clock and port select (gmbus_register.v – reg_gmbus0)

The GMBUS0 register will set the clock rate of the serial bus and the device the controller is connected to. The clock rate options are 50 KHz, 100 KHz, 400 KHz, and 1MHz. This register should be set before the first data valid bit is set, because it will be read only at the very first data valid bit, and not read during the period of the transmission until stop is issued and next first data valid bit is set.

Bit	Description
31:16	Reserved:
15	**Hold Time extension:** This bit selects the hold time on the data line driven from the GMCH.0 = Hold time of 0ns 1 = Hold time of 300 ns
14:12	Reserved

11	**Reserved**
10:8	**GMBUS Rate Select:** These two bits select the rate that the GMBUS will run at. It also defines the AC timing parameters used. It should only be changed when between transfers when the GMBUS is idle. 1xx = Reserved. 000 = 100 KHz 001 = 50 KHz 010 = 400 KHz 011 = 1 MHz
7:3	Reserved:
2:0	**Pin Pair Select:** This field selects an GMBUS pin pair for use in the GMBUS communication. Use the table above to determine which pin pairs are available for a particular device and the intended function of that pin pair. Note that it is not a straight forward mapping of port numbers to pair select numbers. 000 = None (disabled) 001 = MIPI I2C use 010 = Dedicated Analog Monitor DDC Pins (DDC1DATA, DDC1CLK) 011 = Reserved 100 = DP/HDMI port C Use 101 = DP/HDMI port B Use 110 = Reserved 111 = D connector control signals

GMBUS1—GMBUS Command and Status

Address Offset:05104h

Default Value: 0000 0000h

Normal Access: Read/Write Size: 32 bits

Double Buffered:no

Description: gmbus command and status (gmbus_register.v – reg_gmbus1)

This register lets the software indicate to the GMBUS controller the slave device address, register index, and indicate when the data write is complete.

When the **SW_CLR_INT** bit is asserted, all writes to the GMBUS2, GMBUS3, and GMBUS4 registers are discarded. The GMBUS1 register writes to any other bit except the **SW_CLR_INT** are also lost. Reads to these registers always work normally regardless of the state of the **SW_CLR_INT** bit.

Bit	Description
31	**Software Clear Interrupt ,SW_CLR_INT:** This bit must be clear for normal operation. Setting the bit , then clearing it acts as local reset to the GMBUS controller. This bit is commonly used by software to clear a BUS_ERROR when a slave device delivers a NACK. 0 = If this bit is written as a zero when its current state is a one, will clear the **HW_RDY** bit and allows register writes to be accepted to the GMBUS registers (Write Protect Off). This bit is cleared to zero when an event causes the HW_RDY bit transition to occur. 1 = Asserted by software after servicing the GMBUS interrupt. Setting this bit causes the INT status bit to be cleared. Setting (1) this bit also asserts the **HW_RDY** bit (until this bit is written with a 0). When this bit is set, no writes to GMBUS registers will cause the contents to change with the exception of this bit which can be written.
30	Software Ready ,SW_RDY: Data handshake bit used in conjunction with **HW_RDY** bit. 0 = De-asserted via the assertion event for **HW_RDY** bit 1 = When asserted by software, results in de-assertion of **HW_RDY** bit
29	Enable Timeout ,ENT: Enables timeout for slave response. When this bit is enabled and the slave device response has exceeded the timeout period, the GMBUS Slave Stall Timeout Error interrupt bit is set. 0 = disable timeout counter 1 = enable timeout counter
28	Reserved:
27:25	Bus Cycle Select 000 = No GMBUS cycle is generated.001 = GMBUS cycle is generated without an INDEX, with no STOP, and ends with a WAIT010 = Reserved011 = GMBUS cycle is generated with an INDEX, with no STOP, and ends with a WAIT100 = Generates a STOP if currently in a WAIT or after the completion of the current byte if active.101 = GMBUS cycle is generated without an INDEX and with a STOP110 = Reserved111 = GMBUS cycle is generated with an INDEX and with a STOP GMBUS cycle will always consist of a START followed by Slave Address, followed by an optional read or write data phase. A read cycle with an index will consist of a START followed by a Slave Address a WRITE indication and the INDEX and then a RESTART with a Slave Address and an optional read data phase. The GMBUS cycle will terminate either with a STOP or by entering a wait state. The WAIT state is exited by generating a STOP or by starting another GMBUS cycle. This can only cause a STOP to be generated if a GMBUS cycle is generated, the GMBUS is

	currently in a data phase, or it is in a WAIT phase: Note that the three bits can be decoded as follows: 27 = STOP generated 26 = INDEX used 25 = cycle ends in a WAIT
24:16	**Total Byte Count.** (9-bits). This determines the total number of bytes to be transferred during the DATA phase of a GMBUS cycle. The DATA phase can be prematurely terminated by generating a STOP while in the DATA phase (see Bus Cycle Select). Do not change the value of this field during GMBUS cycles transactions.
15:8	**8-bit GMBUS Slave Register Index ,INDEX:** This field specifies the 8-bits of index to be used for the generated bus write transaction or the index used for the WRITE portion of the WRITE/READ pair. It only has an effect if the enable Index bit is set. Do not change this field during a GMBUS transaction.
7:1	**7-bit GMBUS Slave Address ,SADDR:** When a GMBUS cycle is to be generated using the Bus Cycle Select field, this field specifies the value of the slave address that is to be sent out. For use with 10-bit slave address devices, set this value to 11110XXb (where the last two bits (xx) are the two MSBs of the 10-bit address) and the slave direction bit to a write. This is followed by the first data byte being the 8 LSBs of the 10-bit slave address. Special Slave Addresses 0000 000R = General Call Address 0000 000W = Start byte 0000 001x = CBUS Address 0000 010x = Reserved 0000 011x = Reserved 0000 1xxx = Reserved 1111 1xxx = Reserved 1111 0xxx = 10-Bit addressing
0	**Slave Direction Bit:** When a GMBUS cycle is to be generated based on the Bus Cycle Select, this bit determines if the operation will be a read or a write. A read operation with the index enabled will perform a write with just the index followed by a re-start and a read. 1 = Indicates that a Read from the slave device operation is to be performed.0 = Indicates that a Write to slave device operation is to be performed.

GMBUS2—GMBUS Status Register

Address Offset:05108h

Default Value: 0000 0800h

Normal Access: Read/WriteSize: 32 bits

Description: gmbus status (gmbus_register.v – reg_gmbus2)

Double Buffered:No

Bit	Description
31:16	Reserved:
15	INUSE 0 = read operation that contains a zero in this bit position indicates that the GMBUS engine is now acquired and the subsequent reads of this register will now have this bit set. Writing a 0 to this bit has no effect. 1 = read operation that contains a one for this bit indicates that the GMBUS is currently allocated to someone else and "In use". Once set, a write of a 1 to this bit indicates that the software has relinquished the GMBUS resource and will reset the value of this bit to a 0. Software wishing to arbitrate for the GMBUS resource can poll this bit until it reads a zero and will then own usage of the GMBUS controller. This bit has no effect on the hardware, and is only used as semaphore among various independent software threads that don't know how to synchronize their use of this resource that may need to use the GMBUS logic. Writing a one to this bit is software's indication that the software use of this resource is now terminated and it is available for other clients. AccessType: One to clear
14	Hardware Wait Phase ,HW_WAIT_PHASE (read only): 0 = The GMBUS engine is not in a wait phase. 1 = Set when GMBUS engine is in wait phase. Wait phase is entered at the end of the current transaction when that transaction is selected not to terminate with a STOP. Once in a WAIT_PHASE, the software can now choose to generate a STOP cycle or a repeated start (RESTART) cycle followed by another GMBUS transaction on the GMBUS. AccessType: Read Only
13	**Slave Stall Timeout Error (read only)**. This bit indicates that a slave stall timeout has occurred. It is tied to the Enable Timeout (ENT) bit. 0 = No slave timeout has occurred. 1 = A slave acknowledge timeout has occurred

	AccessType: Read Only
12	**GMBUS Interrupt Status (read only)**. This bit indicates that an event that causes a GMBUS interrupt has occurred. 0 = The conditions that could cause a GMBUS interrupt have not occurred or this bit has been cleared by software assertion of the **SW_CLR_INT** bit. 1 = GMBUS interrupt event occurred. This interrupt must have been one of the types enabled in the GMBUS4 register. AccessType: Read Only
11	**Hardware Ready ,HW_RDY (read only)**. This provides a method of detecting when the current software client routine can proceed with the next step in a sequence of GMBUS operations. This data handshake bit is used in conjunction with the **SW_RDY** bit. When this bit is changed to asserted by the GMBUS controller, it results in the de-assertion of the **SW_RDY** bit. 0 = Condition required for assertion has not occurred or when this bit was a one and: 0. **SW_RDY** bit has been asserted. 1. During a GMBUS read transaction, after the each read of the data register. 2. During a GMBUS write transaction, after each write of the data register. 3. **SW_CLR_INT** bit has been cleared. 1 = This bit is asserted under the following conditions: a. After a reset or when the transaction is aborted by the setting of the **SW_CLR_INT** bit. b. When an active GMBUS cycle has terminated with a STOP. c. When during a GMBUS write transaction, the data register needs and can accept another four bytes of data. d. During a GMBUS read transaction, this bit is asserted when the data register has four bytes of new data or the read transaction DATA phase is complete and the data register contains the last few bytes of the read data. This bit resumes to normal operation when the **SW_CLR_INT** bit is written to a 0. AccessType: Read Only
10	**NAK Indicator (read only).** Was previously called Slave Acknowledge Timeout Error SATOER. 0 = No bus error has been detected or **SW_CLR_INT** has been written as a zero since the last bus error. 1 = Set by hardware if any expected device acknowledge is not received from the slave within the timeout. AccessType: Read Only
9	**GMBUS Active, GA (read only).** This is a status bit that indicates whether the GMBUS controller is in an IDLE state or not.

	0 = The GMBUS controller is currently IDLE. 1 = This indicates that the bus is in START, ADDRESS, INDEX, DATA, WAIT, or STOP Phase. Set when GMBUS hardware is not IDLE. AccessType: Read Only
8:0	**Current Byte Count (read only).** Can be used to determine the number of bytes currently transmitted/received by the GMBUS controller hardware. Set to zero at the start of a GMBUS transaction data transfer and incremented after the completion of each byte of the data phase. Note that because reads have internal storage, the byte count on a read operation may be ahead of the data that has been accepted from the data register. AccessType: Read Only

GMBUS3—GMBUS Data Buffer

Address Offset:0510Ch

Default Value: 0000 0000h

Normal Access: Read/Write

Description: gmbus data buffer (gmbus_register.v – reg_gmbus3)

Size: 32 bits

This is data read/write register. This register is double buffered. Bit 0 is the first bit sent or read, bit 7 is the 8th bit sent or read, all the way through bit 31 being the 32nd bit sent or read. For GMBUS write operations with a non-zero byte count, this register be written with the data before the GMBUS cycle is initiated. For byte counts that are greater than four bytes, this register will be written with subsequent data only after the HW_RDY status bit is set indicating that the register is now ready for additional data. For GMBUS read operations, software should wait until the HW_RDY bit indicates that the register contains the next set of valid read data before reading this register.

Bit	Description
31:24	Data Byte 3:
23:16	Data Byte 2:
15:8	Data Byte 1:
7:0	Data Byte 0:

GMBUS4—GMBUS Interrupt Mask

Address Offset:05110h

Default Value: 0000 0000h

Normal Access: Read/Write

Description: gmbus interrupt mask (gmbus_register.v – reg_gmbus4)

Size: 32 bits

Bit	Description
31:5	Reserved
4:0	**Interrupt Mask:** This field specifies which GMBUS interrupts events may contribute to the setting of gmbus interrupt status bit in second level interrupt status register PIPEASTAT. Bit 4: GMBUS Slave stall timeout Bit 3: GMBUS NAK Bit 2: GMBUS Idle Bit 1: Hardware wait (GMBUS cycle without a stop has completed) Bit 0: Hardware ready (Data has been transferred) 0 = Disable this type of GMBUS interrupt 1 = Enable this type of GMBUS interrupt

GMBUS5—2 Byte Index Register

Address Offset:05120h

Default Value: 0000h

Normal Access: Read/WriteSize: 32 bits

Description: gmbus index (gmbus_register.v – reg_gmbus5)

Double Buffered:no

This register provides a method for the software indicate to the GMBUS controller the 2 byte device index.

Bit	Description
31	**2 Byte Index Enable:** When this bit is asserted (1), then bits 15:00 are used as the index. Bits 15:8 are used in the first byte which is the most significant index bits. The slave index in the GMBUS1<15:8> are ignored. Bits 7:0 are used in the second byte which is the least significant index bits.
30:16	Reserved
15:00	**2 Byte Slave Index:** This is the 2 byte index used in all GMBUS accesses when bit 31 is asserted (1).

Display Clock Control Registers (06000h–06FFFH)

The clock control registers were reduced only for control and clock disabling since many of the DPLL registers host at the DPIO and accessed through the DPIO Packet/Data indirect access. This chapter describes the clock registers that still host at the DSP controller and some of the DPIO features.

Clocks supported per Port type:

Display Modes	Display Clock Frequency Range (MHz)	Bit Clock Frequency Range (bps)
CRT DAC	20-355 MHz	N/A
HDMI	20-165 MHz	0.2-1.65 Gbs
LVDS (Single Channel)	20-112 MHz	0.14-0.78 Gbs
Display Port	162, 270 MHz	1.62, 2.70 Gbs

In order to configure the DPLL for certain frequency there are few parameters:

- Jitter (the lower the n divider – better jitter, the lower the VCO – better jitter)
- Power (the lower VCO – the smallest power consummation)
- Accuracy of the freq (the higher the VCO – usually the better accuracy)

Reference Frequency:

There are two external differential inputs to the DPIO, where each of the DPLLs can use any of the two as reference clock. These will be connected to CK505 that will supply 2 kinds of clocks – 96MHz and 100MHz (SSC and non SSC). Since the 96MHz is high jitter clock.

- 96MHz for CRT (HDMI/DP has jitter issue)
- 96MHz or 100MHz (usually SSC) for LVDS
- 100MHz for eDP
- 27MHz (XTL) for HDMI/DP

DPLLA_CTRL—DPLL A Control Register

Address Offset:06014h

Default Value: 00002000h

Normal Attribute: R/Wts

Description: DPLL A Control (cpdmmreg.v – reg03_lt)

Size: 32 bits

Bit	Description
31	DPLL A VCO Enable: Disabling the PLLA will cause the display dot clock to stop. 0 = DPLLA is disabled in its lowest power state (default) 1 = DPLLA is enabled and operational (42usec until lock without calibration and 110usec for calibration)
30	DPLLA External Clock Buffer Enable: 0 = Disable DPLLA clock from being driven out 1 = Enable DPLLA clock to be drive out
29	RefA clock enable: : Indicate the reference clock of PLL A is enable 0 – Disable (default) 1 – Enable
28	**VGA Mode Disable:** When in native VGA modes, writes to the VGA MSR register causes the value in the selected (by MSR bits) VGA clock control register to be loaded into the active register. This allows the VGA clock select to select the pixel frequency between the two standard VGA pixel frequencies. 0 = VGA MSR<3:2> Clock Control bits select DPLL A Frequency 1 = Disable VGA Control
27:26	**Enable single DPLLA frequency for both pipes:** When two pipes are enabled for eDP and both pipes can run with the same DP frequency either 162MHz or 270MHz. Setting this mode can allow using only DPLLA to feed both pipes. DPLLB should be shutdown to save power. This control is double buffered. 00 = Disabled 01 = Enabled 10 = Reserved 11 = Reserved
25:24	Reserved: FPA0/FPA1 P2 Clock Divide: 00 = Divide by 10. This is used when Dot Clock =< 270MHz in HDMI or DAC modes 01 = Divide by 5. This is used when Dot Clock >270MHz 10 = Reserved

	11 = Reserved For DPLLA in LVDS mode, BITS(27:26)=10 00 = Divide by 14. This is used in Single-Channel LVDS 01 = Divide by 7. This is used in Dual-Channel LVDS 10 = Reserved 11 = Reserved
23:16	**Reserved**
15	PLLA Lock (RO) 1 - PLLA Lock 0 – PLLA unlock
14	Vcc Voltage Select: This control selects the VCC voltage in DPLL 0 = 1.0 V (default) 1 = voltage for LDO circuit (for TNG use)
13	DPLL A Reference Input Select: This control selects the integrated core refclk or external OSC refclk as the input clock source to DPLL A. 0 = External refclk pad (27MHz) 1 = Integrated core refclk (default is 100 MHz)
12:9	Reserved: **Parallel to Serial Load Pulse phase selection:** Programmable select bits to choose the relative phase of the high speed (10X) DPLL clock used for generating the parallel to serial load pulse for digital display port on PCIe. The relative phase is the number of flop delays (phase 0 represents 1 flop delay) of the 1X parallel data synchronization signal in the 10X clock domain. The earliest selectable clock phase is 4. A phase selection of 10 or greater simply extends the flop delay count to sample delayed data. 0100 = use clock phase-40101 = use clock phase-5**0110 = use clock phase-6 (Default value)**0111 = use clock phase-71000 = use clock phase-81001 = use clock phase-91010 = use clock phase-101011 = use clock phase-111100 = use clock phase-121101 = use clock phase-13 Phases 0 through 3 are not available for Load Pulse selection.
8	Display Rate Switch pipeA: Switching this bit (transition 0 to 1 or 1 to 0) causes the DSP HW to disable and than enable the DPLL during vblank (2 row) in order to switch the frequency at the DPLL (new dividers stored at the DPIO which is double buffered) (This bit is only available when bits 17:16 of the PIPEACONF register are 00)

7:0	DPIO PhyStatus (Read Only): This field contains the two 4-bit ModPhy lane status. One for PortB and one for PortC. This signal is active low. Bit 7:4 = Port C PhyStatus[3:0] Bit 3:0 = Port B PhyStatus[3:0]

DPLLB_CTRL—DPLL B Control Registers

Address Offset:06018h

Default Value: 00006000h

Normal Attribute: R/W

Description: DPLL B Control (cpdmmreg.v – reg04_lt)

Size: 32 bits

Bit	Description
31	DPLL B VCO Enable: Disabling the PLLB will cause the display dot clock to stop. 0 = DPLLB is disabled in its lowest power state (default) 1 = DPLLB is enabled and operational (42usec until lock without calibration and 110usec for calibration)
30	DPLLB External Clock Buffer Enable: 0 = Disable DPLLB clock from being driven out 1 = Enable DPLLB clock to be drive out
29	RefB clock enable: : Indicate the reference clock of PLL A is enable 0 – Disable (default) 1 – Enable
28	**VGA Mode Disable:** When in native VGA modes, writes to the VGA MSR register causes the value in the selected (by MSR bits) VGA clock control register to be loaded into the active register. This allows the VGA clock select to select the pixel frequency between the two standard VGA pixel frequencies. 0 = VGA MSR<3:2> Clock Control bits select DPLL A Frequency 1 = Disable VGA Control
27:26	**Enable single DPLLB frequency for both pipes:** When two pipes are enabled for eDP and both pipes can run with the same DP frequency either 162MHz or 270MHz. Setting this mode

	can allow using only DPLLB to feed both pipes. DPLLA should be shutdown to save power. 00 = Disabled 01 = Enabled 10 = Reserved 11 = Reserved
25:24	Reserved:
23:16	Reserved:
15	**Reserved:** Write as zero
14	DPIO Common Register Interface clock select (criclksel): This bit is to control the clock source for DPIO Common Register Interface 0 = Use external reclk pad 1 = Use integrated core refclk (default)
13	**Reserved**
12:9	Reserved:
8	Display Rate Switch pipeB: Switching this bit (transition 0 to 1 or 1 to 0) causes the DSP HW to disable and than enable the DPLL during vblank (2 row) in order to switch the frequency at the DPLL (new dividers stored at the DPIO which is double buffered) (This bit is only available when bits 17:16 of the PIPEACONF register are 00)
7:0	Reserved

DPLLAMD—DPLL A HDMI Multiplier/Divisor Register

Address Offset:0601Ch

Default Value: 00000003h

Normal Attribute: R/W

Description: Pipe A multiply (cpdmmreg.v – reg15_lt)

Size: 32 bits

Bit	Description
31:30	Reserved

29:24	**DPLL A HDMI Divider Hi-Res:** When the source is high resolution, this field determines the number of pixels to be included in the multiplied packet defined by the HDMI multiplier. For CRT, the only valid setting is 1x. HDMI example: If the pixel clock on the display should be 180MHz and the display PLL is set to 270MHz, two pixels and one fill code must be sent over HDMI (fixed frequency mode only). Therefore, the HDMI divider should be set to 2 and the HDMI multiplier should be set to 3, since 180 MHz (pixel clock) = 2/3*270MHz (link character clock) This divider must be set to 1x for any mode except HDMI fixed frequency mode. Value in this register = number of pixels per packet – 1 Default: 0000 – 1 pixel per packet (Default value, must be set to 1x for any mode except HDMI fixed frequency mode) Range: 0-63 (1 pixel per packet – 64 pixels per packet)
23:22	Reserved
21:16	**DPLL A HDMI Divider VGA:** When the source is VGA, these bits specify the HDMI divider. The format of this field is the same as that of the hi-res divider.
15:14	Reserved
13:8	**DPLL A HDMI multiplier Hi-Res:** This field is applied to CRT. In order to keep the clock rate to a more narrow range of rates, the multipler is set and the Display PLL programmed to a multiple of the display mode's actual clock rate. This is unrelated to the pixel multiply that is selectable per plane. 6x and higher multipliers can only be used for HDMI mode. Value in this register = multiplication factor - 1 Default: 000000 (1X) Range: 0 – 63 (1X – 64X)
7:6	Reserved
5:0	**DPLL A HDMI multiplier VGA:** When the source is VGA, these bits specify the HDMI multiplier. The format of this field is the same as that of the hi-res multiplier. 6x and higher multipliers can only be used for HDMI mode. Value in this register = multiplication factor - 1 Default: 000011 (4X) Range: 0 – 63 (1X – 64X)

DPLLBMD—DPLL B HDMI Multiplier/Divisor Register

Address Offset:06020h

Default Value: 00000003h

Normal Attribute: R/W

Description: Pipe B multiplyer (cpdmmreg.v – reg16_lt)

Size: 32 bits

Bit	Description
31:30	Reserved
29:24	**DPLL B HDMI Divider Hi-Res:** When the source is high resolution, this field determines the number of pixels to be included in the multiplied packet defined by the HDMI multiplier. For CRT, the only valid setting is 1x. HDMI example: If the pixel clock on the display should be 180MHz and the display PLL is set to 270MHz, two pixels and one fill code must be sent over HDMI (fixed frequency mode only). Therefore, the HDMI divider should be set to 2 and the HDMI multiplier should be set to 3, since 180 MHz (pixel clock) = 2/3*270MHz (link character clock) This divider must be set to 1x for any mode except HDMI fixed frequency mode. Value in this register = number of pixels per packet – 1 Default: 0000 – 1 pixel per packet (Default value, must be set to 1x for any mode except HDMI fixed frequency mode) Range: 0-63 (1 pixel per packet – 64 pixels per packet)
23:22	Reserved
21:16	**DPLL B HDMI Divider VGA:** When the source is VGA, these bits specify the HDMI divider. The format of this field is the same as that of the hi-res divider.
15:14	Reserved
13:8	**DPLL B HDMI multiplier Hi-Res:** This field is applied to CRT. In order to keep the clock rate to a more narrow range of rates, the multipler is set and the Display PLL programmed to a multiple of the display mode's actual clock rate. This is unrelated to the pixel multiply that is selectable per plane. 6x and higher multipliers can only be used for HDMI mode. Value in this register = multiplication factor - 1 Default: 000011 (4X) Range: 0 – 63 (1X – 64X)

7:6	Reserved
5:0	**DPLL B HDMI multiplier VGA:** When the source is VGA, these bits specify the HDMI multiplier. The format of this field is the same as that of the hi-res multiplier. 6x and higher multipliers can only be used for HDMI mode. Value in this register = multiplication factor - 1 Default: 000000 (1X) Range: 0 – 63 (1X – 64X)

RAWCLK_FREQ—Rawclk Frequency

RAWCLK_FREQ—Rawclk Frequency	
Register Type:	MMIO
Address Offset:	06024h
Project:	All
Default Value:	0000007Dh
Access:	R/W
Size (in bits):	32

Bit	Description
31:10	Reserved Project: All Format:
9:0	Rawclk frequency Project: All Format: Program this field with rawclk frequency. This is used to generate a divided down clock for miscellaneous timers in display.

D_STATE—D State Function Control Register

Address Offset:06104

Default Value: 20D00400h

Normal Attribute: R/W

Description: Power state behaviour (cpdmmreg.v – reg11_lt)

Size: 32 bits

Bit	Description
31:16	DPLL Lock Time: This is the time required to the DPLL to relock. The counter using the HRAW clk (5nsec) and resolution of 5nsec. (SEG DPLL lock time is 42usec)
15	Reserved: MBZ
14:8	DPLL Min Power Down: This is the minimum time required the DPLL to be power down until it is allowed to turn it on again. The HW counter using HRAW clk (5nsec) and has resolution of 160nsec (SEG DPLL required time is 0.5usec)
7:4	Reserved: MBZ
3	**Dot Clock PLL Power Down in D3:** This bit determines whether the PCI Power State Powers down the Dot Clock PLLs when in D3. A 0 on this bit does not power down the DPLLs, requiring software to gate them if necessary. When this bit is a 1, the dot PLLs are powered down when in D3. The PCI power state is determined by bits 1:0 of the PCI Power Management Control/Status register.
2	Reserved
1	**Graphics Core Clock Gating:** This bit determines whether the PCI Power State gates the Graphics Core clocks when in the D3 state. A 0 on this bit does not gate the clocks, requiring software to gate them if necessary. When this bit is a 1, the graphics core clocks are gated at the outputs of the PLLs when in D3. The PCI power state is determined by bits 1:0 of the PCI Power Management Control/Status register. This register field has no use in current products.
0	**Dot Clock Gating:** This bit determines whether the PCI Power State gates the Dot clocks when in the D3 state. A 0 on this bit does not gate the clocks, requiring software to gate them if necessary. When this bit is a 1, the dot clocks are gated at the outputs of the PLLs when in D3. The PCI power state is determined by bits 1:0 of the PCI Power Management Control/Status register.

Display Palette Registers (0A000h–AFFFh)

DPALETTE_A—Pipe A Display Palette

Address Offset: 0A000h

Default Value: 00000000h

Normal Attributes: R/W

Table 4-1. 8-Bit Mode

31 24	23 16	15 8	7 0
Reserved	Red Palette Entry	Green Palette Entry	Blue Palette Entry

Bit	Description
31:24	Reserved: (read only).
23:16	Pipe A Red Palette Entry:
15:8	Pipe A Green Palette Entry:
7:0	Pipe A Blue Palette Entry:

10-bit Programming Notes:

- The 10-bit gamma correction curve is represented by specifying a set of reference points spaced equally along the curve. Red, Green, and Blue each have 129 reference points. The first 128 reference points are stored in the palette RAM, and the final value is stored in the GCMAX register. The first 128 reference points are 16 bits represented in a 10.6 format with 10 integer and 6 fractional bits. The final reference points are 17 bits represented in a 11.6 format with 11 integer and 6 fractional bits.
- The appropriate reference point pairs (adjacent) are selected for each color, and the output is interpolated between these two reference point values.
- To program the gamma correction reference points calculate the desired gamma curve for inputs from 0 to 1024.
- Every 8th point on the curve (0,8,16...1016,1024) becomes a reference point. Convert the gamma value to the 10.6 format. The first 128 reference points are saved to the palette RAM, where the odd DWords contain the lower 8 bits of the reference point value, and the even DWords contain the upper 8 bits of the reference point value. The final 129th reference point is saved in the GCMAX register in 11.6 format..

- Example equation for gamma curve of 2.2:
- For (X = 0..1024) { gamma = [(X / 1024) ^ 2.2] * 1024 }
- The curve is assumed to be flat or increasing, never decreasing.
- The start and end reference points are not fixed values.

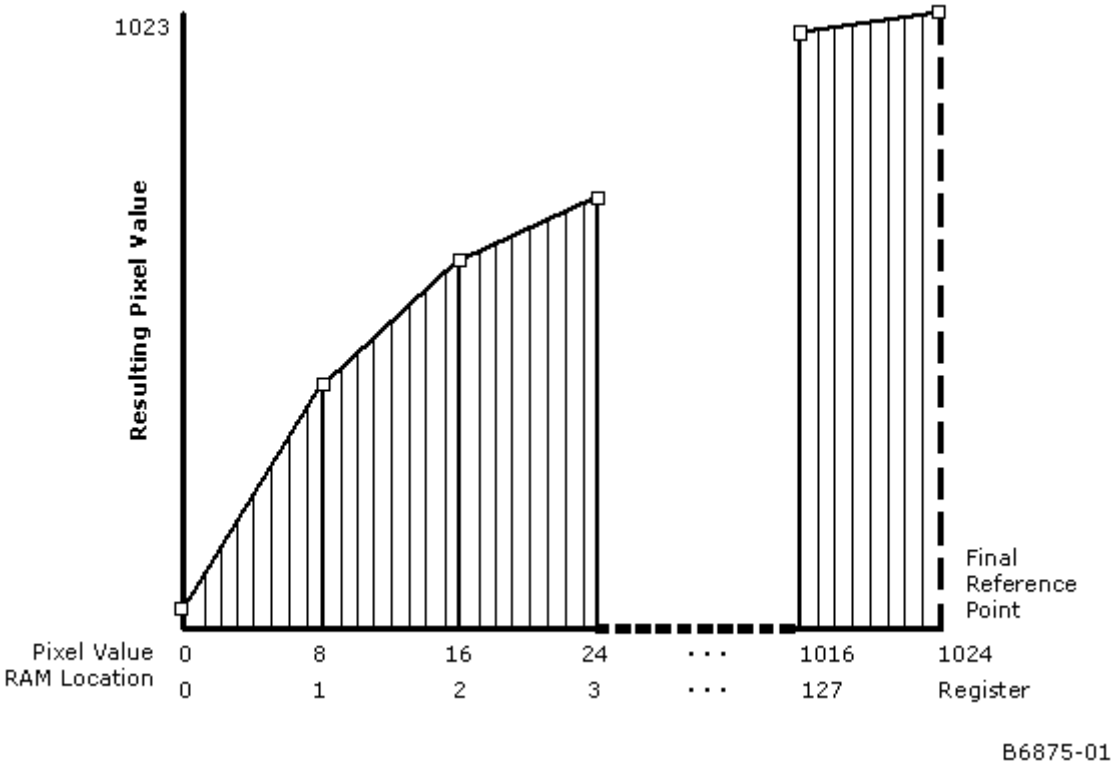

Table 4-2. 10-bit Mode (Even DWord)

31 24	23 22	21 16
Reserved	Red Base[1:0]	Red Fractional Address

15 8	7 0
Green Base[1:0] Green Fractional Address	Blue Base[1:0] Blue Fractional Address

Table 4-3. 10-bit Mode (Odd DWord)

31 24	23 16
Reserved	Red Base [9:2]
15 8	7 0
Green Base[9:2]	Blue Base [9:2]

DPALETTE_B—Pipe B Display Palette

Address Offset: 0A800h

Default Value: 00000000h

Normal Attributes: R/W

8-Bit Mode

Bit	Description
31:24	**Reserved:** Read Only.
23:16	Pipe B Red Palette Entry:
15:8	Pipe B Green Palette Entry:
7:0	Pipe B Blue Palette Entry:

See DPALETTE_A for 10-bit Mode definitions.

Display Pipeline / Port Registers (60000h–6FFFFh)

Display Pipeline A

HTOTAL_A—Pipe A Horizontal Total Register

Address Offset: 60000h

Default Value: 00000000h

Normal Access: R/W

Bit	Description
31:29	**Reserved:** Write as zero.
28:16	**Pipe A Horizontal Total Display Clocks:** This 13-bit field provides Horizontal Total up to 8192 pixels encompassing the Horizontal Active Display period, front/back border and retrace period. Any pending event (HSYNC, ACTIVE, HBLANK) is reset at HTOTAL and the programmed sequence begins again. This field is programmed to the number of clocks desired minus one. This number of clocks needs to be a multiple of two when driving data out the digital port out the LVDS port in two channel mode. This value should always be equal or greater to the sum of the horizontal active and the horizontal blank, and border region sizes.
15: 12	**Reserved:** Write as zero.
11: 0	**Pipe A Horizontal Active Display End Pixels:** This 12-bit field provides Horizontal Active Display resolutions up to 4096 pixels. Note that the first horizontal active display pixel is considered pixel number 0. The value programmed should be the (active pixels/line – 1). The number of active pixels will be limited to multiples of two pixels when driving the integrated LVDS port in two channel mode. For proper results during VGA centering mode this value needs to be large enough to fit the largest VGA mode supported, this should be at least 720/1440 pixels for standard VGA type modes or 640/1280 pixels if the nine-dot disable bit in the VGA control register is set. When using the internal panel fitting logic, the minimum horizontal size allowed will be three pixels.

HBLANK_A—Pipe A Horizontal Blank Register

Address Offset: 60004h

Default Value: 00000000h

Normal Access: R/W

Bit	Description

31:29	**Reserved:** Read Only.
28:16	**Pipe A Horizontal Blank End:** This 13-bit field specifies the position of Horizontal Blank End expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HBLANK End pixel position, where the first active pixel is considered position 0; the second active pixel is considered position 1, etc. Horizontal blank ending at the same point as the horizontal total indicates that there is no left hand border area. HBLANK size has a minimum value of 32 clocks. The number of clocks within blank needs to be a multiple of two when driving data out LVDS in two channel mode. The value loaded in the register would be equal to RightBorder+Active+HBlank-1. If this pipe is connected to the TVout port or Panel Fitter 2 the border must be zero. In that case this register is programmed to the same value as the HTOTAL register.
15:13	**Reserved:** Read Only.
12:0	**Pipe A Horizontal Blank Start:** This 13-bit field specifies the Horizontal Blank Start position expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HBLANK Start pixel position, where the first active pixel is considered position 0; the second active pixel is considered position 1, etc. The number of clocks for both left and right borders need to be a multiple of two when driving data out the LVDS port in two channel mode. Horizontal blank should only start after the end of the horizontal active region. The value loaded in the register would be equal to RightBorder+Active-1. If this pipe is connected to the TVout port or Panel Fitter 2 the border must be zero. In that case this register is programmed to the same value as the HACTIVE register.

HSYNC_A—Pipe A Horizontal Sync Register

Address Offset: 60008h

Default Value: 00000000h

Normal Access: R/W

Bit	Description
31:29	**Reserved:** Write as zero.
28:16	**Pipe A Horizontal Sync End:** This 13-bit field specifies the horizontal Sync End position expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HSYNC End pixel position, where the first active pixel is

	considered position 0; the second active pixel is considered position 1, etc. The number of clocks in the sync period needs to be a multiple of two when driving data out the LVDS port in two channel mode. This value should be greater than the horizontal sync start position and would be loaded with the Active+RightBorder+FrontPorch+Sync-1.
15:13	**Reserved:** Read Only.
12:0	**Pipe A Horizontal Sync Start:** This 13-bit field specifies the horizontal Sync Start position expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HSYNC Start pixel position, where the first active pixel is considered position 0; the second active pixel is considered position 1, etc. Note that when HSYNC Start is programmed equal to HBLANK Start, both HSYNC and HBLANK will be asserted on the same pixel clock. It should never be programmed to less than HBLANK start. The number of cycles from the beginning of the line needs to be a multiple of two when driving data out the LVDS port in two channel mode. This register should not be less than the horizontal active end. This register should be loaded with the Active+RightBorder+FrontPorch-1.

VTOTAL_A—Pipe A Vertical Total Register

Address Offset: 6000Ch

Default Value: 00000000h

Normal Access: R/W

Bit	Description
31:29	**Reserved:** Read Only.
28:16	**Pipe A Vertical Total Display Lines:** This 13 bit field provides Vertical Total up to 8192 lines encompassing the Vertical Active Display Lines, top/bottom border and retrace period. The value programmed should be the number of lines required minus one. Vertical total needs to be large enough to be greater than the sum of the vertical active, vertical border, and the vertical blank regions. The vertical counter is incremented on the leading edge of the horizontal sync. For interlaced display modes, this indicates the total number of lines in both fields. In interlaced modes, hardware automatically divides this number by 2 to get the number of lines in each field.
15:12	**Reserved:** Read Only.
11:0	**Pipe A Vertical Active Display Lines:** This 12-bit field provides vertical active display resolutions up to 4096 lines. It should be programmed with the desired number of lines minus one. When using the internal panel fitting logic, the minimum vertical active area must be three lines. For interlaced display modes, this indicates the total number of lines in both fields. In interlaced modes, hardware automatically divides this number by 2 to get the number of

	lines in each field.

VBLANK_A—Pipe A Vertical Blank Register

Address Offset: 60010h

Default Value: 00000000h

Normal Access: R/W

Bit	Description
31:29	Reserved: Read Only.
28:16	**Pipe A Vertical Blank End:** This 13-bit field specifies the Vertical Blank End position expressed in terms of the absolute Line number relative to the vertical active display start. The value programmed should be the VBLANK End line position, where the first active line is considered line 0, the second active line is considered line 1, etc. The end of vertical blank should be after the start of vertical blank and before or equal to the vertical total. This register should be loaded with the Vactive+BottomBorder+VBlank-1. For interlaced display modes, hardware automatically divides this number by 2 to get the vertical blank end in each field. It does not count the two half lines that get added when operating in modes with half lines. If this pipe is connected to the TVout port or Panel Fitter 2 the border must be zero. In that case this register is programmed to the same value as the VTOTAL register.
15:13	Reserved: Read Only.
12: 0	**Pipe A Vertical Blank Start:** This 13-bit field specifies the Vertical Blank Start expressed in terms of the absolute line number relative to the vertical active display start. The value programmed should be the VBLANK Start line position, where the first active line is considered line 0, the second active line is considered line 1, etc. Minimum vertical blank size is required to be at least three lines. Blank should start after the end of active. This register is loaded with the Vactive+BottomBorder-1. For interlaced display modes, hardware automatically divides this number by 2 to get the vertical blank start in each field. It does not count the two half lines that get added when operating in modes with half lines. If this pipe is connected to the TVout port or Panel Fitter 2 the border must be zero. In that case this register is programmed to the same value as the VACTIVE register.

VSYNC_A—Pipe A Vertical Sync Register

Address Offset: 60014h

Default Value: 00000000h

Normal Access: R/W

Bit	Description
31:29	**Reserved:** Read Only.
28:16	**Pipe A Vertical Sync End:** This 13-bit field specifies the Vertical Sync End position expressed in terms of the absolute Line number relative to the vertical active display start. The value programmed should be the VSYNC End line position, where the first active line is considered line 0, the second active line is considered line 1, etc. This register should be loaded with Vactive+BottomBorder+FrontPorch+Sync-1. For interlaced display modes, hardware automatically divides this number by 2 to get the vertical sync end in each field. It does not count the two half lines that get added when operating in modes with half lines.
15:13	**Reserved:** Read Only.
12:0	**Pipe A Vertical Sync Start:** This 13-bit field specifies the Vertical Sync Start position expressed in terms of the absolute line number relative to the vertical active display start. The value programmed should be the VSYNC Start line position, where the first active line is considered line 0, the second active line is considered line 1, etc. This register would be loaded with Vactive+BottomBorder+FrontPorch-1. For interlaced display modes, hardware automatically divides this number by 2 to get the vertical sync start in each field. It does not count the two half lines that get added when operating in modes with half lines.

PIPESRCA—Pipe A Source Image Size

Address Offset:6001Ch

Default Value: 00000000h

Normal Access: Read/Write

Bit	Description
31:28	**Reserved:** Write as zero
27:16	**Pipe A Horizontal Source Image Size:** This 12-bit field specifies Horizontal source image size up to 4096. This determines the size of the image created by the display planes sent to the blender. The value programmed should be the source image size minus one. The actual source size must be two times the programmed value in the “pixel multiply mode. It must represent a size that is a multiple of two (even numbers) when driving the LVDS port in two channel mode. This implies that for this mode, the value programmed will always be an odd number. Except in the case of panel fitting internal or in an external device, this register field would be programmed to a value identical to the horizontal active. This is the only register of the timing

	registers that is allowed to be programmed while the pipe is enabled.
15:12	**Reserved:** Write as zero
11: 0	**Pipe A Vertical Source Image Size:** This 12-bit field specifies the vertical source image size up to 4096 lines. This determines the size of the image created by the display planes sent to the blender. The value programmed should be the source image size minus one. Note that the actual number of lines needs to be at least twice the planes programmed value when in the pixel multiply mode. Except in the case of panel fitting internal or in an external device, this register field would be programmed to a value identical to the vertical active. For interlaced display modes, hardware automatically divides this number by 2 to get the vertical source image size in each field.

BCLRPAT_A— Pipe A Border Color Pattern Register

Address Offset:60020h

Default Value: 00000000h

Normal Access: Read/Write

This register value determines what color should be sent to the display in the border region, the space between the end of active and the beginning of blank and the end of blank and the beginning of active.

Bit	Description
31:24	Reserved
23:16	Pipe A Border Red Channel Value
15:8	Pipe A Border Green Channel Value
7:0	Pipe A border Blue Channel Value

VSYNCSHIFT_A— Vertical Sync Shift Register

Address Offset:60028h

Default Value: 00000000h

Normal Access: Read/Write

Bit	Description

31:13	**Reserved:** Write as zero.
12:0	**Pipe A Second Field Vertical Sync Shift:** This value specifies the vertical sync alignment for the start of the interlaced second field expressed in terms of the absolute pixel number relative to the horizontal active display start. This value will only be used if the PIPEACONF is programmed to an interlaced mode using vsync shift. Otherwise a legacy value of floor[htotal / 2] will be used. Typically, the interlaced second field vertical sync should start one pixel after the point halfway between successive horizontal syncs, so the value of this register should be programmed to: (horizontal sync start - floor[horizontal total / 2]) (use the actual horizontal sync start and horizontal total values and not the minus one values programmed into registers). This vertical sync shift only occurs during the interlaced second field. In all other cases the vertical sync start position is aligned with horizontal sync start.

Pipe A M/N Values

Calculation of TU, Data M, and Data N is as follows:

For modes that divide into the link frequency evenly,

Active/TU = Payload/Capacity = Data M/N = dot clock * bytes per pixel / ls_clk * number of lanes

Default value to program TU size is "111111" for TU size of 64

Calculation of Link M and Link N is as follows:

Link M/N = dot clock / ls_clk

Please note that in the DisplayPort specifcation, dot clock is referred to as strm_clk.

When switching between two refresh rates, both the M1/N1 data and link values and the M2/N2 link values must be programmed. For dynamic refresh rate control, M1/N1 values are used for higher power, and M2/N2 values are used for lower power. Selection of M1/N1 or M2/N2 is indicated via MSA from the CPU display.

TransADataM1— Pipe A Data M value 1

TransADataM1— Pipe A Data M value 1	
Register Type:	MMIO
Address Offset:	60030h
Project:	All

Default Value:	7E000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of Vblank
Double Buffer Armed By:	Writing the TransADPLinkN1

This is the primary Pipe data M value used for DisplayPort. It is used in conjunction with the data N value 1.

Bit	Description
31	Reserved Project: All Format: MBZ
30:25	TU1_Size Project: All This field is the size of the transfer unit for DP, minus one.
24	Reserved Project: All Format: MBZ
23:0	Pipe_A_Data_M1_value Project: All This field is the M1 value for internal use of the DDA.

TransADataN1— Pipe A Data N value 1

TransADataN1— Pipe A Data N value 1	
Register Type:	MMIO
Address Offset:	60034h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

Double Buffer Update Point:	Start of Vblank
Double Buffer Armed By:	Writing the TransADPLinkN1

This is the primary Pipe data N value used for DisplayPort. It is used in conjunction with the data M value 1.

Bit	Description
31:24	Reserved Project: All Format: MBZ
23:0	Pipe_A_Data_N1_value Project: All This field is the N1 value for internal use of the DDA.

TransADataM2— Pipe A Data M value 2

TransADataM2— Pipe A Data M value 2	
Register Type:	MMIO
Address Offset:	60038h
Project:	All
Default Value:	7E000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of Vblank
Double Buffer Armed By:	Writing the TransADPLinkN2

This is the second Pipe data M value used for DisplayPort. It is used in conjunction with the data N value 2.

Bit	Description
31	Reserved Project: All Format: MBZ

30:25	TU2_Size Project: All Default Value: 111111b 64 This field is the size of the transfer unit for DP, minus one.	
24	Reserved Project: All Format: MBZ	
23:0	Pipe_A_Data_M2_value Project: All This field is the M2 value for internal use of the DDA.	

TransADataN2— Pipe A Data N value 2

TransADataN2— Pipe A Data N value 2	
Register Type:	MMIO
Address Offset:	6003Ch
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of Vblank
Double Buffer Armed By:	Writing the TransADPLinkN2

This is the second Pipe data N value used for DisplayPort. It is used in conjunction with the data M value 2.

Bit	Description
31:24	Reserved Project: All Format: MBZ
23:0	Pipe_A_Data_N2_value Project: All

	This field is the N2 value for internal use of the DDA.

TransADPLinkM1— Pipe A Link M value 1

TransADPLinkM1— Pipe A Link M value 1	
Register Type:	MMIO
Address Offset:	60040h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of Vblank
Double Buffer Armed By:	Writing the TransADPLinkN1

This is the primary link data M value used for DisplayPort. It is used in conjunction with the link N value 1

Bit	Description
31:24	Reserved Project: All Format: MBZ
23:0	Pipe_A_Link_M1_value Project: All This field is the M1 value for external transmission in the Main Stream Attributes.

TransADPLinkN1— Pipe A Link N value 1

TransADPLinkN1— Pipe A Link N value 1	
Register Type:	MMIO
Address Offset:	60044h

Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of Vblank
Double Buffer Armed By:	Writing the TransADPLinkN1

This is the primary link data N value used for DisplayPort. It is used in conjunction with the link M value 1.

Bit	Description
31:24	Reserved Project: All Format: MBZ
23:0	Pipe_A_Link_N1_value Project: All This field is the N1 value for external transmission in the Main Stream Attributes and VB-ID.

TransADPLinkM2— Pipe A Link M value 2

TransADPLinkM2— Pipe A Link M value 2

Register Type:	MMIO
Address Offset:	60048h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of Vblank
Double Buffer Armed By:	Writing the TransADPLinkN2

This is the secondary link data M value used for DisplayPort. It is used in conjunction with the link N value 2.

Bit	Description
31:24	Reserved Project: All Format: MBZ
23:0	Pipe_A_Link_M2_value Project: All This field is the M2 value for external transmission in the Main Stream Attributes.

TransADPLinkN2— Pipe A Link N value 2

TransADPLinkN2— Pipe A Link N value 2

Register Type:	MMIO
Address Offset:	6004Ch
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of Vblank
Double Buffer Armed By:	Writing the TransADPLinkN2

This is the secondary link data N value used for DisplayPort. It is used in conjunction with the link M value 2.

Bit	Description
31:24	Reserved Project: All Format: MBZ
23:0	Pipe_A_Link_N2_value Project: All This field is the N2 value for external transmission in the Main Stream Attributes and VB-ID.

PSR Config Registers

PSRCTLA – Pipe A Panel Self Refresh Control

Memory Offset Address: 60090h

Default Value: 00000000h

Normal Access: Read/Write double buffered

In the vlv platform, when an embedded Displayport panel with panel self-refresh is used the following control register needs to be configured to be properly functional and power-saving.

Bit	Description
	Reserved
	Identical Frame threshold: Number of identical frames that display controller needs to exceed in order to transition to PSR active state in HW timer mode
	DPLLA power down delay: programmable delay from main link powerdown to DPLLA powerdown. The delay is in number of cdclk clocks.
	Double frames in PSR active entry. If asserted, HW will send two frames with same SDP active setting when entry PSR active state. This bit is set if the vertical blanking time is less than 330us.
	Source transmitter state in PSR active. If asserted, HW will keep transmitter active during PSR active state and sends only idle symbols. If deasserted, HW will turn off transmitter during PSR active state. Display driver will keep this bit consistent with “Source transmitter state in PSR active” bit in DPCD register of the sink.
	PSR_active_entry. This bit is only valid in PSR_mode is SW timer mode. If it is asserted, HW will transition into PSR_active state. If it is deasserted, HW will transition to PSR_inactive state. SW should not set or clear this bit more than once within one vblank period.
	PSR_single_frame_update. In PSR SW or HW mode, SW set this bit before writing registers for a flip. After HW finishes signle frame update, it goes back to PSR active – no RFB state. SW driver may send new single frame update request. **Programming note:** Reading this bit is updated at the next vblank. Writing this bit to 1 will cause PSR FSM to perform single frame update automatically, no vblank is required. When single frame update is done, it will automatically go back to PSR active – no RFB update. 60094[2:0] = 3’b011.
	Reserved
	PSR mode: B011-111: reserved. b010: **PSR with HW timer**. HW timer decides PSR active entry point. PSR active state exits upon MMIO write registers that may change the frame buffer. b001: **PSR with SW timer.** In this mode, SW will keep track of idle frames and buffer modification in the driver and explicitly specify the entry and exit PSR active state point.

	PSR reset. If assert all PSR functions are reset back to PSR inactive state. When it needs to resynchronize source and sync, SW writes 0x2 to DPCD register 600h and to this bit to get system back to PSR active states. This bit is self clear.
	PSR enable: Panel Self-refresh is enabled. When it is asserted PSR is enabled and operate in one of the mode that specified by PSR mode.

PSRSTATA – Pipe A PSR status register

Memory Offset Address: 60094h

Default Value: 00000000h

Normal Access: Read Only

Bit	Description
	Display local standby state: 00: D0 idle state, fetch frame buffer from system memory 01: D0i1 – PSR is active, stop fetch frame buffer in system memory 02: D0i2 – PSR is active, display controller is trunk gated 03: D0i3 – Reserved in VLV
	Reserved
	Repeat Frame counter: Number of identical frames has been sent by display controller. Value is not roll over at 255.
	Reserved
	SDP sent: it indicates if SDP packet has been sent in current frame.
	PSR in transition. There is a period that source already committed to PSR active but sink did not. SW should not change the source state at this time but wait until this status bit is clear. The wait time should in the range of 120-250us in the worst case.
	Reserved
	Reserved
	PSR current state: indicate current source state that vlv PSR state machine are in

	000: PSR_disabled **001:** PSR_inactive **010:** PSR_transition_to_active **011:** PSR_active – no RFB update **100:** PSR_active – single frame update **101:** PSR_exit

VSCSDPA – Pipe A VSC SDP register

Memory Offset Address: 600A0h

Default Value: 00000000h

Normal Access: Read/Write

Bit	Description
	SDP send frequency 00: off, not sending 01: send one every frame 10: send once 11: reserved Programming note: This field shall be programmed either send once or send one every frame when SW driver sets PSR active entry bit When PSR is enabling this field is ignored. One SDP is sent in every frame until source is in PSR active state
	Reserved
	DB1: Programmed by display driver in manual mode, auto-generate by display controller in all other modes
	DB0: Bits 7:4: Stereo Interface Method Specific Parameter Bits 3:0: Stereo Interface Method Code. This field is programmed by display driver for stereo display configuration

Pipe A Wide Gamut Color Correction C01_C00 Coefficients

Memory Offset Address: 600B0h

Default Value: 00000000h

Normal Access: Read/Write

When color correction matrix enable bit is set in PIPEACONF register, each of pixels in the pipe is multiplied with this matrix. Color matrix is used to convert pixels from one RGB color space to another RGB color space. There are many applications for the use of this matrix lile gamut mapping between 72 percent color gamut to 92 percent color gamut. Each coefficient is a 12-bit signed fixed-point number. The application of coefficients are as follows:

Bit	Description
	Reserved
	C01 Coefficient: 12-bit 2's complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.
	Reserved
	C00 Coefficient: 12-bit 2's complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

Pipe A Wide Gamut Color Correction C02 Coefficient

Memory Offset Address: 600B4h

Default Value: 00000000h

Normal Access: Read/Write

When color correction matrix enable bit is set in PIPEACONF register, each of pixels in the pipe is multiplied with this matrix. Color matrix is used to convert pixels from one RGB color space to another RGB color space. There are many applications for the use of this matrix lile gamut mapping between 72 percent color gamut to 92 percent color gamut. Each coefficient is a 12-bit signed fixed-point number. The application of coefficients are as follows:

Bit	Description
	Reserved
	C02 Coefficient: 12-bit 2's complement signed value that is programmed for linea. The range of the value can be from -

	1.999 to +1.999.

Pipe A Wide Gamut Color Correction C11_C10 Coefficients

Memory Offset Address: 600B8h

Default Value: 00000000h

Normal Access: Read/Write

When color correction matrix enable bit is set in PIPEACONF register, each of pixels in the pipe is multiplied with this matrix. Color matrix is used to convert pixels from one RGB color space to another RGB color space. There are many applications for the use of this matrix lile gamut mapping between 72 percent color gamut to 92 percent color gamut. Each coefficient is a 12-bit signed fixed-point number. The application of coefficients are as follows:

Bit	Description
	Reserved
	C11 Coefficient: 12-bit 2's complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.
	Reserved
	C10 Coefficient: 12-bit 2's complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

Pipe A Wide Gamut Color Correction C12 Coefficient

Memory Offset Address: 600BCh

Default Value: 00000000h

Normal Access: Read/Write

When color correction matrix enable bit is set in PIPEACONF register, each of pixels in the pipe is multiplied with this matrix. Color matrix is used to convert pixels from one RGB color space to another RGB color space. There are many applications for the use of this matrix lile gamut mapping between 72 percent color gamut to 92 percent color gamut. Each coefficient is a 12-bit signed fixed-point number. The application of coefficients are as follows:

Bit	Description
	Reserved

	C12 Coefficient: 12-bit 2's complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

Pipe A Wide Gamut Color Correction C21_C20 Coefficients

Memory Offset Address: 600C0h

Default Value: 00000000h

Normal Access: Read/Write

When color correction matrix enable bit is set in PIPEACONF register, each of pixels in the pipe is multiplied with this matrix. Color matrix is used to convert pixels from one RGB color space to another RGB color space. There are many applications for the use of this matrix lile gamut mapping between 72 percent color gamut to 92 percent color gamut. Each coefficient is a 12-bit signed fixed-point number. The application of coefficients are as follows:

Bit	Description
	Reserved
	C21 Coefficient: 12-bit 2's complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.
	Reserved
	C20 Coefficient: 12-bit 2's complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

Pipe A Wide Gamut Color Correction C22 Coefficient

Memory Offset Address: 600C4h

Default Value: 00000000h

Normal Access: Read/Write

When color correction matrix enable bit is set in PIPEACONF register, each of pixels in the pipe is multiplied with this matrix. Color matrix is used to convert pixels from one RGB color space to another RGB color space. There are many applications for the use of this matrix lile gamut mapping between 72 percent color gamut to 92 percent color gamut. Each coefficient is a 12-bit signed fixed-point number. The application of coefficients are as follows:

Bit	Description
	Reserved
	C22 Coefficient: 12-bit 2's complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

PSRCTLB – Pipe B Panel Self Refresh Control

Memory Offset Address: 61090h

Default Value: 00000000h

Normal Access: Read/Write double buffered

In the vlv platform, when an embedded Displayport panel with panel self-refresh is used the following control register needs to be configured to be properly functional and power-saving.

Bit	Description
	Reserved
	Identical Frame threshold: Number of identical frames that display controller needs to exceed in order to transition to PSR active state in HW timer mode
	DPLLB power down delay: programmable delay from main link powerdown to DPLLB powerdown. The delay is in number of cdclk clocks.
	Double frames in PSR active entry. If asserted, HW will send two frames with same SDP active setting when entry PSR active state. This bit is set if the vertical blanking time is less than 330us.
	Source transmitter state in PSR active. If asserted, HW will keep transmitter active during PSR active state and sends only idle symbols. If deasserted, HW will turn off transmitter during PSR active state. Display driver will keep this bit consistent with "Source transmitter state in PSR active" bit in DPCD register of the sink.
	PSR_active_entry. This bit is only valid in PSR_mode is SW timer mode. If it is asserted, HW will transition into PSR_active state. If it is deasserted, HW will transition to PSR_inactive state. SW should not set or clear this bit more than once within one vblank period.
	PSR_single_frame_update. In PSR SW or HW mode, SW set this bit before writing registers for a flip. After HW finishes signle frame update, it goes back to PSR active – no RFB state. SW driver may send new single frame update request.

	Programming note: Reading this bit is updated at the next vblank. Writing this bit to 1 will cause PSR FSM to perform single frame update automatically, no vblank is required. When single frame update is done, it will automatically go back to PSR active – no RFB update. 61094[2:0] = 3'b011.
	Reserved
	PSR mode: B011-111: reserved. b010: **PSR with HW timer**. HW timer decides PSR active entry point. PSR active state exits upon MMIO write registers that may change the frame buffer. b001: **PSR with SW timer.** In this mode, SW will keep track of idle frames and buffer modification in the driver and explicitly specify the entry and exit PSR active state point.
	PSR reset. If assert all PSR functions are reset back to PSR inactive state. When it needs to resynchronize source and sync, SW writes 0x2 to DPCD register 600h and to this bit to get system back to PSR active states. This bit is self clear.
	PSR enable: Panel Self-refresh is enabled. When it is asserted PSR is enabled and operate in one of the mode that specified by PSR mode.

PSRSTATB – Pipe B PSR status register

Memory Offset Address: 61094h

Default Value: 00000000h

Normal Access: Read Only

VSCSDPB – Pipe B VSC SDP register

Memory Offset Address: 610A0h

Default Value: 00000000h

Normal Access: Read/Write

Bit	Description
	SDP send frequency 00: off, not sending 01: send one every frame 10: send once 11: reserved Programming note: This field shall be programmed either send once or send one every frame

	when SW driver sets PSR active entry bit When PSR is enabling this field is ignored. One SDP is sent in every frame until source is in PSR active state
	Reserved
	DB1: Programmed by display driver in manual mode, auto-generate by display controller in all other modes
	DB0: Bits 7:4: Stereo Interface Method Specific Parameter Bits 3:0: Stereo Interface Method Code. This field is programmed by display driver for stereo display configuration

Pipe B Wide Gamut Color Correction C01_C00 Coefficients

Memory Offset Address: 610B0h

Default Value: 00000000h

Normal Access: Read/Write

When color correction matrix enable bit is set in PIPEBCONF register, each of pixels in the pipe is multiplied with this matrix. Color matrix is used to convert pixels from one RGB color space to another RGB color space. There are many applications for the use of this matrix lile gamut mapping between 72 percent color gamut to 92 percent color gamut. Each coefficient is a 12-bit signed fixed-point number. The application of coefficients are as follows:

Bit	Description
	Reserved
	C01 Coefficient: 12-bit 2's complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.
	Reserved
	C00 Coefficient: 12-bit 2's complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

Pipe B Wide Gamut Color Correction C02 Coefficient

Memory Offset Address: 610B4h

Default Value: 00000000h

Normal Access: Read/Write

When color correction matrix enable bit is set in PIPEBCONF register, each of pixels in the pipe is multiplied with this matrix. Color matrix is used to convert pixels from one RGB color space to another RGB color space. There are many applications for the use of this matrix lile gamut mapping between 72 percent color gamut to 92 percent color gamut. Each coefficient is a 12-bit signed fixed-point number. The application of coefficients are as follows:

Bit	Description
	Reserved
	C02 Coefficient: 12-bit 2's complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

Pipe B Wide Gamut Color Correction C11_C10 Coefficients

Memory Offset Address: 610B8h

Default Value: 00000000h

Normal Access: Read/Write

When color correction matrix enable bit is set in PIPEBCONF register, each of pixels in the pipe is multiplied with this matrix. Color matrix is used to convert pixels from one RGB color space to another RGB color space. There are many applications for the use of this matrix lile gamut mapping between 72 percent color gamut to 92 percent color gamut. Each coefficient is a 12-bit signed fixed-point number. The application of coefficients are as follows:

Bit	Description
	Reserved
	C11 Coefficient: 12-bit 2's complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.
	Reserved
	C10 Coefficient: 12-bit 2's complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

Pipe B Wide Gamut Color Correction C12 Coefficient

Memory Offset Address: 610BCh

Default Value: 00000000h

Normal Access: Read/Write

When color correction matrix enable bit is set in PIPEBCONF register, each of pixels in the pipe is multiplied with this matrix. Color matrix is used to convert pixels from one RGB color space to another RGB color space. There are many applications for the use of this matrix lile gamut mapping between 72 percent color gamut to 92 percent color gamut. Each coefficient is a 12-bit signed fixed-point number. The application of coefficients are as follows:

Bit	Description
	Reserved
	C12 Coefficient: 12-bit 2's complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

Pipe B Wide Gamut Color Correction C21_C20 Coefficients

Memory Offset Address: 610C0h

Default Value: 00000000h

Normal Access: Read/Write

When the color correction matrix enable bit is set in PIPEBCONF register, each of pixels in the pipe is multiplied with this matrix. Color matrix is used to convert pixels from one RGB color space to another RGB color space. There are many applications for the use of this matrix lile gamut mapping between 72 percent color gamut to 92 percent color gamut. Each coefficient is a 12-bit signed fixed-point number. The application of coefficients are as follows:

Bit	Description
	Reserved
	C21 Coefficient: 12-bit 2's complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.
	Reserved
	C20 Coefficient:

	12-bit 2's complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

Pipe B Wide Gamut Color Correction C22 Coefficient

Memory Offset Address: 610C4h

Default Value: 00000000h

Normal Access: Read/Write

When color correction matrix enable bit is set in PIPEBCONF register, each of pixels in the pipe is multiplied with this matrix. Color matrix is used to convert pixels from one RGB color space to another RGB color space. There are many applications for the use of this matrix lile gamut mapping between 72 percent color gamut to 92 percent color gamut. Each coefficient is a 12-bit signed fixed-point number. The application of coefficients are as follows:

Bit	Description
	Reserved
	C22 Coefficient: 12-bit 2's complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

VIDEO_DIP_CTL_A—Video DIP Control for Pipe A

VIDEO_DIP_CTL_A—Video DIP Control for Pipe A	
Register Type:	MMIO
Address Offset:	60200h
Project:	All
Default Value:	20200900h
Access:	R/W
Size (in bits):	32
Please note that writes to this register take effect immediately. Therefore, it is critical for software to follow the write and read sequences as described in the bit 31 text.	

Bit	Description
31	Enable_Graphics_Data_Island_Packet Project: All Default Value: 0b Data Island Packet (DIP) is a mechanism that allows up to 36 bytes to be sent over digital port during VBLANK, according to the HDMI and DP specifications. This includes header, payload, checksum and ECC information. Each type of DIP can be sent once per vsync, once every other vsync, or once. This data can be transmitted on either Pipe, through any digital port (digital port B, C), but not two simultaneously on one Pipe. Please note that the audio subsystem is also capable of sending Data Island Packets. These packets are programmed by the audio driver and can be read by in MMIO space via the audio control state and audio HDMI widget data island registers, addresses 620B4h and 62054h, respectively. Write sequence: 1. Wait for 1 VSync to ensure completion of any pending DIP transmissions. 2. Disable the DIP type (bits 24:21) and set the DIP buffer index (bits 20:19) for the DIP being written. 3. Set the DIP access address (bits 3:0) to 0, or to the desired DWORD to be written. 4. Write DIP data 1 DWORD at a time. The IF access address autoincrements with each DWORD write, wrapping around to address 0 when the max buffer address size of 0xF has been reached. Please note that software must write an entire DWORD at a time. 5. Enable the DIP type and transmission frequency. Reading sequence: 1. Set the DIP buffer index (bits 20:19) for the DIP being read. 2. Set the DIP access address to 0, or to the desired DWORD to be read. Read DIP data 1 DWORD at a time. The DIP access address autoincrements with each DWORD read, wrapping around to address 0 when the max buffer address size of 0xF has been reached. Value / Name / Description / Project 0b / Disable / Video DIP is disabled / All 1b / Enable / Video DIP is enabled / All

Programming Notes

- Partial DIPs are never sent out while the port is enabled. Disabling the DIP at the same time it is being transferred will result in the DIP being completed before the function is disabled.
- Shutting off the port on which DIP is being transmitted will result in partial transfer of DIP data. There is no need to switch off the DIP enable bit if the port transmitting DIP is disabled.
- When disabling both the DIP port and DIP transmission, first disable the port and then disable DIP.
- Enabling a DIP function at the same time that the DIP would have been sent out (had it already been enabled) will result in the DIP being sent on the following frame.

1. Enabling should only be done after the buffer contents have been written.

- If DIP is enabled but DIP types are all disabled, no DIP is sent. However, a single Null DIP will be sent at the same point in the stream that DIP packets would have been sent. This is done to keep the port in HDMI mode, otherwise it would revert to DVI mode. The "Null packets enabled during vsync" mode (bit #9 of port control register) overrides this behavior.
- After DIP is sent and intend to disable DIP after DIP is sent. Before disable DIP, one shall disable DPIOunit clock gating first and wait for two vblanks and enable DPIO clock gating.

30:29 Port_Select

Project: All

Default Value: 01b Digital Port B

This selects which port is to transmit the data island. This field must not be changed while data island transmission is enabled.

Value	Name	Description	Project
00b	Reserved	Reserved	All
01b	Digital Port B	Digital Port B (Default)	All
10b	Digital Port C	Digital Port C	All

	11b	Reserved	Reserved	All

28:26 Reserved Project: All Format:

25 GCP_DIP_enable

Project: All

Default Value: 0b

This bit enables the output of the General Control Packet. GCP is different from other DIPs in that much of the payload is automatically reflected in the packet, and therefore a DIP buffer for GCP is not needed. Please refer to the GCP payload register for payload details. Writes to this bit take effect immediately.

This bit should not be enabled for 8bpc mode if at least one of the other HDMI ports is enabled in 12bpc mode.

Value	Name	Description	Project
0b	Disable	GCP DIP disabled	All
1b	Enable	GCP DIP enabled	All

24:21 Data_Island_Packet_type_enable

Project: All

Default Value: 0001b Enable AVI DIP

These bits enable the output of a given data island packet (DIP) type. It can be updated while the port is enabled and is immediately updated (not double-buffered). Within 2 vblank periods, the DIP is guaranteed to have been transmitted.

	<table><tr><th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr><tr><td>XXX1b</td><td>Enable AVI</td><td>Enable AVI DIP (Default = enabled)</td><td>All</td></tr><tr><td>XX1Xb</td><td>Enable Vendor</td><td>Enable Vendor-specific DIP (Default = disabled)</td><td>All</td></tr><tr><td>X1XXb</td><td>Enable Gamut</td><td>Enable Gamut Metadata Packet (Default = disabled)</td><td>All</td></tr><tr><td>1XXXb</td><td>Enable Source</td><td>Enable Source Product Description DIP (Default = disabled)</td><td>All</td></tr></table>
20:19	DIP_buffer_index Project: All Default Value: 00b This field is used during programming of different DIPs. These bits are used as an index to their respective DIP buffers. The transmission frequency must also be written when programming the buffer. <table><tr><th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr><tr><td>00b</td><td>AVI</td><td>AVI DIP (31 bytes of space available)</td><td>All</td></tr><tr><td>01b</td><td>Vendor-specific</td><td>Vendor-specific DIP</td><td>All</td></tr><tr><td>10b</td><td>Reserved</td><td>Reserved</td><td>All</td></tr><tr><td>11b</td><td>Source Product</td><td>Source Product Description DIP</td><td>All</td></tr></table>
18	Reserved Project: All Format:

17:16	Video_DIP_transmission_frequency Project: All Default Value: 00b These bits dictate the frequency of Video DIP transmission for the DIP buffer index designated in bits 20:19. When writing Video DIP data, this value is also latched when the first DW of the Video DIP is written. When read, this value reflects the Video DIP transmission frequency for the Video DIP buffer designated in bits 20:19. This field shall be ignored for Gamut Metadata Packet transmission.

Value	Name	Description	Project
00b	Send Once	Send Once	All
01b	Every VSync	Send Every VSync (Default for AVI)	All
10b	Every Other Vsync	Send at least every other VSync	All
11b	Reserved	Reserved	All

15:12	Reserved Project: All Format: MBZ
11:8	Video_DIP_buffer_size Project: All AccessType: Read Only Default Value: 1001b This reflects the buffer size in dwords available for the type of Video DIP being indexed by

	bits 20:19 of this register, including the header. It is hardwired to the maximum size of a Video DIP, 36 bytes. Please note that this count includes ECC bytes, which are not writable by software. These bits are immediately valid after write of the DIP index.
7:4	Reserved Project: All Format: MBZ
3:0	Video_DIP_RAM_access_address Project: All AccessType: Read Only Selects the DWORD address for access to the Video DIP buffers. This value is automatically incremented after each read or write of the Video DIP Data Register. The value wraps back to zero when it autoincrements past the max address value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.

VIDEO_DIP_DATA_A–Video Data Island Packet Data for Pipe A

VIDEO_DIP_DATA_A–Video Data Island Packet Data for Pipe A	
Register Type:	MMIO
Address Offset:	60208h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32
Bit	Description

31:0	Video_DIP_DATA Project: All When read, this returns the current value at the location specified in the Video DIP buffer index select and Video DIP RAM access address fields. The index used to address the RAM is incremented after each read or write of this register. DIP data can be read at any time. Data should be loaded into the RAM before enabling the transmission through the DIP type enable bit. Accesses to this register are on a per-DWORD basis.

Construction of DIP:

MSB				LSB
DW0	DP: Header byte 3 HDMI: ECC header (RO)	Header byte 2	Header byte 1	Header byte 0
DW1	Data byte 3	Data byte 2	Data byte 1: Start of payload	Data byte 0: Checksum for payload
…				
DW8	ECC byte 3 (RO)	ECC byte 2 (RO)	ECC byte 1 (RO)	ECC byte 0 (RO)
DW9	DP: ECC byte 7 (RO) HDMI: Reserved	DP: ECC byte 6 (RO) HDMI: Reserved	DP: ECC byte 5 (RO) HDMI: Reserved	DP: ECC byte 4 (RO) HDMI: Reserved

VIDEO_DIP_GDCP_PAYLOAD_A–Video Data Island Payload for Pipe A

VIDEO_DIP_GDCP_PAYLOAD_A–Video Data Island Payload for Pipe A	
Register Type:	MMIO
Address Offset:	60210h

Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

Bit	Description
31:3	Reserved Project: All Format: MBZ
2	GCP_color_indication Project: All Default Value: 0b This bit must be set when in deep color mode. It may optionally be set for 24-bit mode. It must be set if the sink attached to Pipe A can receive GCP data.

Value	Name	Description	Project
0b	Don't Indicate	Don't indicate color depth. CD and PP bits in GCP set to zero	All
1b	Indicate	Indicate color depth using CD bits in GCP. It will be set depending on programmed pixel depth in port control register	All

1	GCP_default_phase_enable Project: All Default Value: 0b Indicates the video timings meet alignment requirements such that the following conditions are met: 1. Htotal is an even number 2. Hactive is an even number 3. Hsync is an even number 4. Front and back porches for Hsync are even numbers

	5. Vsync always starts on an even-numbered pixel within a line in interlaced modes (starting counting with 0)

Value	Name	Description	Project
0b	Clear	Default phase bit in GCP is cleared	All
1b	Require Met	Default phase bit in GCP is set. All requirements must be met before setting this bit	All

0	GCP_AV_mute Project: All Default Value: 0b Set AV mute bit in GCP

Value	Name	Description	Project
0b	Clear	AV mute bit in GCP is cleared. When this bit transitions to 0, the AV mute clear flag is sent in the next GCP packet	All
1b	Set	AV mute bit in GCP is set. When this bit transitions to 1, the AV mute set flag is sent in the next GCP packet	All

Display Pipeline B

HTOTAL_B—Pipe B Horizontal Total Register

Address Offset: 61000h

Default Value: 00000000h

Normal Access: R/W

Bit	Description
31:29	**Reserved:** Write as zero.
28:16	Pipe B Horizontal Total Display: See pipe A description.

15:12	**Reserved:** Write as zero.
11:0	Pipe B Horizontal Active Display: See pipe A description

HBLANK_B—Pipe B Horizontal Blank Register

Address Offset: 61004h

Default Value: 00000000h

Normal Access: R/W

Bit	Description
31:29	**Reserved**. Write as zero.
28:16	Pipe B Horizontal Blank End: See pipe A description
15:13	**Reserved:** Write as zero.
12:0	Pipe B Horizontal Blank Start: See pipe A description.

HSYNC_B—Pipe B Horizontal Sync Register

Address Offset: 61008h

Default Value: 00000000h

Normal Access: R/W

Bit	Description
31:29	**Reserved:** Write as zero.
28: 16	Pipe B Horizontal Sync End: See pipe A description.
15:13	**Reserved:** Write as zero.
12:0	Pipe B Horizontal Sync Start: See pipe A description

VTOTAL_B—Pipe B Vertical Total Register

Address Offset: 6100Ch

Default Value: 00000000h

Normal Access: R/W

Bit	Description
31:29	**Reserved:** Write as zero.
28:16	Pipe B Vertical Total Display: See pipe A description.
15:12	**Reserved:** Write as zero.
11:0	Pipe B Vertical Active Display: See pipe A description.

VBLANK_B—Pipe B Vertical Blank Register

Address Offset: 61010h

Default Value: 00000000h

Normal Access: R/W

Bit	Description
31:29	**Reserved:** Write as zero.
28:16	Pipe B Vertical Blank End: See pipe A description.
15:13	**Reserved:** Write as zero.
12:0	Pipe B Vertical Blank Start: See pipe A description.

VSYNC_B—Pipe B Vertical Sync Register

Address Offset: 61014h

Default Value: 00000000h

Normal Access: R/W

Bit	Description
31:29	**Reserved:** Write as zero.
28:16	Pipe B Vertical Sync End: See pipe A description.
15:13	**Reserved:** Write as zero.
12:0	Pipe B Vertical Sync Start: See pipe A description.

PIPEBSRC—Pipe B Source Image Size

Address Offset:6101Ch

Default Value: 00000000h

Normal Access: Read/Write

Bit	Description
31:28	**Reserved:** Write as zero
27:16	Pipe B Horizontal Source Image Size: See pipe A description.
15:12	**Reserved:** Write as zero
11:0	Pipe B Vertical Source Image Size: See pipe A description.

BCLRPAT_B—Pipe B Border Color Pattern Register

Address Offset:61020h

Default Value: 00000000h

Normal Access: Read/Write

This register determines the color sent during the border region, the periods between the end of blank and the start of active and the end of active and the start of blank. Also same color will be sent during pseudo border period. VGA border color is determined by the VGA border “overscan” color register.

Bit	Description
31:24	Reserved
23:16	Pipe B Red channel color value
15:8	Pipe B Green channel color value
7:0	Pipe B Blue channel color value

VSYNCSHIFT_B— Vertical Sync Shift Register

Address Offset:61028h

Default Value: 00000000h

Normal Access: Read/Write

Bit	Description
31:13	**Reserved:** Write as zero.
12:0	**Pipe B Second Field Vertical Sync Shift:** This value specifies the vertical sync alignment for the start of the interlaced second field expressed in terms of the absolute pixel number relative to the horizontal active display start. This value will only be used if the PIPEBCONF is programmed to an interlaced mode using vsync shift. Otherwise a legacy value of floor[htotal / 2] will be used. Typically, the interlaced second field vertical sync should start one pixel after the point halfway between successive horizontal syncs, so the value of this register should be programmed to: (horizontal sync start - floor[horizontal total / 2]) (use the actual horizontal sync start and horizontal total values and not the minus one values programmed into registers). This vertical sync shift only occurs during the interlaced second field. In all other cases the vertical sync start position is aligned with horizontal sync start.

Pipe B M/N Values

Calculation of TU, Data M, and Data N is as follows:

For modes that divide into the link frequency evenly,

Active/TU = Payload/Capacity = Data M/N = dot clock * bytes per pixel / ls_clk * number of lanes

Default value to program TU size is "111111" for TU size of 64

Calculation of Link M and Link N is as follows:

Link M/N = dot clock / ls_clk

Please note that in the DisplayPort specifcation, dot clock is referred to as strm_clk.

When switching between two refresh rates, both the M1/N1 data and link values and the M2/N2 link values must be programmed. For dynamic refresh rate control, M1/N1 values are used for higher power, and M2/N2 values are used for lower power. Selection of M1/N1 or M2/N2 is indicated via MSA from the CPU display.

TransBDataM1— Pipe B Data M value 1

TransBDataM1— Pipe B Data M value 1	
Register Type:	MMIO
Address Offset:	61030h

Project:	All
Default Value:	7E000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of Vblank
Double Buffer Armed By:	Writing the TransBDPLinkN1

See Pipe A description

Bit	Description
31	Reserved Project: All Format: MBZ
30:25	TU1_Size Project: All Default Value: 111111b 64 See Pipe A description.
24	Reserved Project: All Format: MBZ
23:0	Pipe_B_Data_M1_value Project: All See Pipe A description.

Pipe B Video DIP

VIDEO_DIP_CTL_B—Video DIP Control for Pipe B

VIDEO_DIP_CTL_B—Video DIP Control for Pipe B	
Register Type:	MMIO
Address Offset:	61170h
Default Value:	20200900h
Access:	R/W

Size (in bits):	32
See Pipe A description.	
Bit	Description
31	Enable_Graphics_Data_Island_Packet Project: All See Pipe A description.
30:29	Port_Select Project: All See Pipe A description.
28:26	Reserved Project: All Format:
25	GCP_DIP_enable Project: All See Pipe A description. This bit should not be enabled for 8bpc mode if at least one of the other HDMI ports is enabled in 12bpc mode.
24:21	Data_Island_Packet_type_enable Project: All See Pipe A description.
20:19	DIP_buffer_index Project: All See Pipe A description.
18	Reserved Project: All Format:
17:16	Video_DIP_transmission_frequency Project: All See Pipe A description.

15:12	Reserved Project: All Format: MBZ
11:8	Video_DIP_buffer_size Project: All AccessType: Read Only Default Value: 1001b See Pipe A description.
7:4	Reserved Project: All Format: MBZ
3:0	Video_DIP_RAM_access_address Project: All AccessType: Read only See Pipe A description.

VIDEO_DIP_DATA_B–Video Data Island Packet Data for Pipe B

VIDEO_DIP_DATA_B–Video Data Island Packet Data for Pipe B
Register Type: MMIO Address Offset:61174h Project: All Default Value: 00000000h Access: R/W

Size (in bits): 32	
Bit	Description
31:0	Video_DIP_DATA Project: All Format: See Pipe A description.

VIDEO_DIP_GDCP_PAYLOAD_B–Video Data Island Payload for Pipe B

VIDEO_DIP_GDCP_PAYLOAD_B–Video Data Island Payload for Pipe B	
Register Type:	MMIO
Address Offset:	61178h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

Bit	Description
31:3	Reserved Project: All Format: MBZ
2	GCP_color_indication Project: All See Pipe A description.
1	GCP_default_phase_enable Project: All See Pipe A description.
0	GCP_AV_mute Project: All See Pipe A description.

Display Port Control

ADPA—Analog Display Port Register

Address Offset:61100h

Default Value: 00040000h

Normal Access: Read/Write

Description: CRT port control (dprrega.v – adp_Q)

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>31</td><td>
Analog_Display-Port_Enable

Project: All

Default Value: 0b

This bit enables or disables the analog port CRT DAC and syncs outputs.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr>
<tr><td>0b</td><td>Disable</td><td>Disable the analog port DAC and disable output of syncs</td><td>All</td></tr>
<tr><td>1b</td><td>Enable</td><td>Enable the analog port DAC and enable output of syncs</td><td>All</td></tr>
</table>
</td></tr>
<tr><td>30</td><td>
Pipe_Select

Project: All

Default Value: 0b

Determines which pipe output will feed this DAC port.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr>
<tr><td>0b</td><td>Pipe A</td><td>Pipe A</td><td>All</td></tr>
<tr><td>1b</td><td>Pipe B</td><td>Pipe B</td><td>All</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><td>29:26</td><td>Reserved Project: All Format:</td></tr>
<tr><td>25:24</td><td>CRT_Hot_Plug_Detection_Channel_Status

Project: All

AccessType: Read Only

Default Value: 00b

These bits are set when a CRT hot plug or unplug event has been detected and indicate which color channels were attached. Write a one to these bits to clear the status. The rising or falling edges of these bits are ORed together to go to the main ISR CRT hot plug register bit.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr>
<tr><td>00b</td><td>None</td><td>No channels attached</td><td>All</td></tr>
<tr><td>01b</td><td>Blue</td><td>Blue channel only is attached</td><td>All</td></tr>
<tr><td>10b</td><td>Green</td><td>Green channel only is attached</td><td>All</td></tr>
<tr><td>11b</td><td>Both</td><td>Both blue and green channel attached</td><td>All</td></tr>
</table></td></tr>
<tr><td>23</td><td>CRT_Hot_Plug_Detection_Enable

Project: All

Default Value: 0b

Hot plug detection is used to set status bits or an interrupt on the connection or disconnection of a CRT to the analog display port.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr>
</table></td></tr>
</table>

	0b	Disable	CRT hot plug detection is disabled	All
	1b	Enable	CRT hot plug detection is enabled	All

22

CRT_Hot_Plug_Circuit_Activation_Period

Project: All

Default Value: 0b

This bit sets the activation period for the CRT hot plug circuit.

Value	Name	Description	Project
0b	64 cdclk	64 cdclk periods	All
1b	128 cdclk	128 cdclk periods	All

21

CRT_Hot_Plug_Detect_Warmup_Time

Project: All

Default Value: 0b

This bit sets the warmup time for the CRT hot plug circuit.

Value	Name	Description	Project
0b	2M pcdclks	2M pcdclks warmup (approximately 5ms)	All
1b	4M pcdclks	4M pcdclks warmup (approximately 10ms)	All

20

CRT_Hot_Plug_Detect_Sampling_Period

Project: All

Default Value: 0b

This bit determines the length of time between sampling periods when the transcoder is disabled.

Value	Name	Description	Project
0b	1G pcdclks	1G pcdclks (approximately 2 seconds)	All
1b	2G pcdclks	2G pcdclks (approximately 4 seconds)	All

19:18

CRT_Hot_Plug_Voltage_Compare_Value

Project: All

Default Value: 01b A0

Compare value for Vref to determine whether the analog port is connected to a CRT.

Value	Name	Description	Project
00b	80	80	All
01b	A0	A0 (Default)	All
10b	C0	C0	All
11b	E0	E0 (bit 17 must be = 1)	All

17

CRT_Hot_Plug_Reference_Voltage

Project: All

Default Value: 0b

Value	Name	Description	Project

	0b	325mv	325mv	All
	1b	475mv	475mv (bits 19:18 must be = 11)	All

16

Force_CRT_Hot_Plug_Detect_Trigger

Project: All

Default Value: 0b

Triggers a CRT hotplug/unplug detection cycle independent of the hot plug detection enable bit. This bit is automatically cleared after the detection is completed. The result of this trigger is reflected in the CRT Hot Plug Detection Status. Software must reset status after a force CRT detect trigger.

Value	Name	Description	Project
0b	No Trigger	No Trigger	All
1b	Force Trigger	Force Trigger	All

15:10

Reserved Project: All Format:

9:5

CRT Full Scale Output Voltage Trimming Control

Project: All

Default Value: 0b

This controls CRT output voltage trimming to ensure the output voltage is withing VESA spec.

4

VSYNC_Polarity_Control

Project: All

Default Value: 0b

The output VSYNC polarity is controlled by this bit. This is used to implement display modes that require inverted polarity syncs and to set the disabled state of the VSYNC signal.

	<table><tr><th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr><tr><td>0b</td><td>Low</td><td>Active Low</td><td>All</td></tr><tr><td>1b</td><td>High</td><td>Active High</td><td>All</td></tr></table>
3	HSYNC_Polarity_Control Project: All Default Value: 0b The output HSYNC polarity is controlled by this bit. This is used to implement display modes that require inverted polarity syncs and to set the disabled state of the HSYNC signal. <table><tr><th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr><tr><td>0b</td><td>Low</td><td>Active Low</td><td>All</td></tr><tr><td>1b</td><td>High</td><td>Active High</td><td>All</td></tr></table>
2	Reserved Project: All Forma
1	Monochrome Enable: If the CRT display is a monochrom type, SW driver shall set this bit to enable the CRT circuit to drive only the green channel to CRT and gate off the red and blue channels. 0 = Monochrome disabled (default) 1 = Monochrome enabled
0	DAC Power Config: this bit controls the voltage for the CRT analog supply voltage 0 = 1.35V is used for analog supply voltage (default) 1 = 1.25V is used for analog supply voltage

PORT_HOTPLUG_EN

Memory Offset Address: 61110h

Default Value: 00000020h

Normal Access: Read/Write

Description: DPD enable control (dprrega.v – ql_hotplugen_Q)

NOTE: For correct operation of display port hot plug detection, the device 2 configuration register GMBUSFREQ at offset 0xCC-0xCD must be programmed correctly.

Bit	Description
31:30	RESERVED: mbz
29	**DisplayPort/HDMI B Hot Plug Interrupt Detect Enable:** This will enable the consideration of the hot plug interrupt status bit for DisplayPort B in the Port Hotplug Status register, offset 61114h. Please note that software must set this bit at boot in order to detect the HPD input buffer live state. Since setting this bit may generate an interrupt, it must not be cleared and reset as part of interrupt processing. 0 = DisplayPort or HDMIB Hot Plug Detect Disabled **(Default)** 1 = DisplayPort or HDMIB Hot Plug Detect Enabled
28	**DisplayPort/HDMI C Hot Plug Interrupt Detect Enable:** This will enable the consideration of the hot plug interrupt status bit for DisplayPort C in the Port Hotplug Status register, offset 61114h. Please note that software must set this bit at boot in order to detect the HPD input buffer live state. Since setting this bit may generate an interrupt, it must not be cleared and reset as part of interrupt processing. 0 = DisplayPort or HDMIC Hot Plug Detect Disabled **(Default)** 1 = DisplayPort or HDMIC Hot Plug Detect Enabled
27	**DisplayPort/HDMI D Hot Plug Interrupt Detect Enable:** This will enable the consideration of the hot plug interrupt status bit for DisplayPort D in the Port Hotplug Status register, offset 61114h. Please note that software must set this bit at boot in order to detect the HPD input buffer live state. Since setting this bit may generate an interrupt, it must not be cleared and reset as part of interrupt processing. 0 = DisplayPort or HDMID Hot Plug Detect Disabled **(Default)** 1 = DisplayPort or HDMID Hot Plug Detect Enabled
26	**Reserved**
25	**Reserved**
24	**Pipe A Audio Interrupt Detect Enable: [vlv]** This bit enables consideration of the pipe A audio interrupt status bit in the Port Hotplug Status Register, offset 61114h. It relates to the HDMI port that has audio enabled and can only be used in combination with TMDS encoding. This bit is only to be used for integrated HDMI. 0 = Audio interrupt detect disabled **(Default)**

	1 = Audio interrupt detect enabled
23	**Pipe B Audio Interrupt Detect Enable: [vlv]** This bit enables consideration of the pipe B audio interrupt status bit in the Port Hotplug Status Register, offset 61114h. It relates to the HDMI port that has audio enabled and can only be used in combination with TMDS encoding. This bit is only to be used for integrated HDMI. 0 = Audio interrupt detect disabled **(Default)** 1 = Audio interrupt detect enabled
22:19	**Reserved:** MBZ
18	Reserved: MBZ **TV Hot Plug Detect Interrupt Enable:** This will enable the consideration of the TV hot plug interrupt status bit. 0 = TV Hot Plug Detect Disabled (bit 10 of the port hotplug status register no longer detects interrupts, **Default**) 1 = TV Hot Plug Detect Enabled
17:16	**DP Hotplug Short Pulse Duration:** These bits define the duration of the pulse defined as a short pulse for DisplayPort ports. Pulse less than this value is detected short pulse. Pulse larger than this value is detected long pulse. For DP, this shall use 2ms as threshold. 00 = 2mS (Default) **01** = 4.5mS **10** = 6mS **11** = 100mS
15:10	RESERVED: mbz
9	Reserved: MBZ. This bit is the same as bit 23 in 61100h
8	Reserved: MBZ. This bit is the same as bit 22 in 61100h
7	Reserved: MBZ. This bit is the same as bit 21 in 61100h
6:5	Reserved: MBZ. This bit is the same as bit 19:18 in 61100h
4	Reserved: MBZ. This bit is the same as bit 20 in 61100h
3	Reserved: MBZ
2	Reserved: MBZ. This bit is the same as bit 17 in 61100h
1:0	Reserved: MBZ

PORT_HOTPLUG_STAT

Memory Offset Address: 61114h

Default Value: 00000000h

Normal Access: Read/Write

Description: CRT port control (dprrega.v – porthotst_aR)

This register is the second level of a two level interrupt and status scheme. Status bits in this register are 'sticky"; once set they can be cleared by writing a one to that bit. A write of a zero does not affect the corresponding Interrupt status bit. The corresponding enable bits determine if the interrupt status bit should be propagated to the first line interrupt status register. When an interrupt occurs, the first line interrupt register indicates the second line source of the interrupt. Reading the second line register will determine the precise source for the interrupt.

- Before clearing a Port-sourced interrupt (e.g., CRT hotplug) in the IIR, the corresponding interrupt (source) status in the PORT_HOTPLUG_STAT must be cleared by writing a '1' to the appropriate bit. In the case where fields are larger than 1 bit wide, all bits in the field must be cleared by writing a '1' to them.

Bit	Descriptions
31:30	RESERVED: mbz
29	**DisplayPort/HDMIB Hot Plug Input Buffer Live State:** This bit is read-only. It reflects the real-time state of the of the hot plug input (HPD pin) on DisplayPort or HDMI B when bit 29 of the hotplug enable register, offset 61110h is set. This pin signal is active high. This does not feed into the first line interrupt status register. This bit should be read to confirm cable connection prior to attempting EDID read. 1 = HPD detected active 0 = HPD detected inactive AccessType: Read Only
28	**DisplayPort/HDMIC Hot Plug Input Buffer Live State:** This bit is read-only. It reflects the real-time state of the of the hot plug input (HPD pin) on DisplayPortC when bit of this register is set. This pin signal is active high. This does not feed into the first line interrupt status register. This bit should be read to confirm cable connection prior to attempting EDID read. 1 = HPD detected high 0 = HPD detected low AccessType: Read Only
27	**DisplayPortD Hot Plug Input Buffer Live State:** This bit is read-only. It reflects the real-time state of the of the hot plug input (HPD pin) on DisplayPortD when bit of this register is set. This pin signal is active high. This does not feed into the first line interrupt status register. Please

	note that port D is intended for LFP use and therefore HPD may not be present. Bit 2 of the DPD control register must therefore be read to determine whether DPD is used in the system. 1 = HPD detected high 0 = HPD detected low AccessType: Read Only
26:24	RESERVED: mbz
23	**Reserved**
22:21	**DisplayPort D Hot Plug Interrupt Detect Status:** This reflects hot plug interrupt status on DisplayPort D. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. This bit feeds into the first line interrupt status register when bit 27 of the hotplug enable status register is set. 00 = DisplayPort D Hot Plug event not detected 1x = DisplayPort D long pulse Hot Plug event detected X1 = DisplayPort D short pulse Hot Plug event detected AccessType: One to Clear
20:19	**DisplayPort C Hot Plug Interrupt Detect Status:** This reflects hot plug interrupt status on DisplayPort or HDMI C. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. This bit feeds into the first line interrupt status register when bit 28 of the hotplug enable status register is set. Please note that these bits should be considered in conjunction with bit 28, the hot plug input buffer live state, when determining further action: if bit 28 = 0, the bits should be cleared and the port must be disabled. 00 = DisplayPort/HDMI C Hot Plug event not detected 1x = DisplayPort/HDMI C long pulse Hot Plug event detected X1 = DisplayPort C short pulse Hot Plug event detected AccessType: One to Clear
18:17	**DisplayPort B Hot Plug Interrupt Detect Status:** This reflects hot plug interrupt status on DisplayPort B. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. This bit feeds into the first line interrupt status register when bit 29 of the hotplug enable status register is set. Please note that these bits should be considered in conjunction with bit 29, the hot plug input buffer live state, when determining further action: if bit 29 = 0, the bits should be cleared and the port must be disabled. 00 = DisplayPort/HDMI B Hot Plug event not detected

	1x = DisplayPort/HDMI B long pulse Hot Plug event detected X1 = DisplayPort B short pulse Hot Plug event detected AccessType: One to Clear
16	**Reserved**
15	**Reserved**
14	**Reserved**
13:12	RESERVED: mbz
11	**CRT Hot Plug Interrupt Status:** This bit is set when a CRT hot plug or unplug event has been detected. A hot plug or unplug event is defined as the change in connection state of the CRT as determined by the hardware CRT detect sequence which is enabled through bit #9 (CRT hot plug interrupt enable) or bit #3 (Force CRT detect trigger) in the Port_HotPlug_En register 0x61110. After reset, the CRT is considered "unconnected" even if physically connected until the first detect sequence occurs. Physically plugging or unplugging the CRT device will also be detected as a change of connection state. Writing a 1 to this bit clears it. 0 =CRT Interrupt has not occurred 1 = CRT Interrupt has occurred AccessType: One to Clear
10	**TV Hot Plug Interrupt Status:** This bit is set when a TV hot plug or unplug event has been detected. Reflects the state of bit 31 of the TV DAC state register, offset 68004-68007h. Software must write a one to these bits to clear the status. 0 =TV Interrupt has not occurred 1 = TV Interrupt has occurred AccessType: One to Clear
9:8	**Reserved:** MBZ. These info are recorded in 61100h ADPA register[25:24]
7	Reserved: mbz
6	**DisplayPort D Aux Interrupt Status:** This bit is set when a transaction on AUX channel D has completed or timed out. This bit feeds into the first line interrupt status register when bit 29 of the AUX channel D control register is set. Writing a 1 to this bit clears it. 0 = AUX channel D Interrupt has not occurred 1 = AUX channel D Interrupt has occurred AccessType: One to Clear

5	**DisplayPort C Aux Interrupt Status:** This bit is set when a transaction on AUX channel C has completed or timed out. This bit feeds into the first line interrupt status register when bit 29 of the AUX channel C control register is set. Writing a 1 to this bit clears it. 0 = AUX channel C Interrupt has not occurred 1 = AUX channel C Interrupt has occurred AccessType: One to Clear
4	**DisplayPort B Aux Interrupt Status:** This bit is set when a transaction on AUX channel B has completed or timed out. This bit feeds into the first line interrupt status register when bit 29 of the AUX channel B control register is set. Writing a 1 to this bit clears it. 0 = AUX channel B Interrupt has not occurred 1 = AUX channel B Interrupt has occurred AccessType: One to Clear
3	**Reserved**
2	**Reserved**
1	**Reserved**
0	**Reserved**

HDMIB—Digital Display Port B Control Register

Address Offset:61140h

Default Value: 00000018h

Normal Access: Read/Write

Size: 32 bits

Description: HDMIB port control

The operating mode of the port is determined by the setting of the encoding register field (bits 11:10).

Bit	Description
31	**HDMIB Enable (Digital Display Port B Enable):** Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written. Both this bit and bit 6 of this register must be enabled to send audio over this port. This port must not be enabled simultaneously with DisplayPort B. 1 = Enable. This bit enables the Digital Display Port B interface for HDMI mode. 0 = Disable and tristates the Digital Display Port B interface for HDMI mode.

30	**Pipe Select:** This bit determines from which display pipe the source data will originate. This only applies to devices with dual display pipes. Pipe selection takes place on the Vblank after being written 0 = Pipe A 1 = Pipe B
29	Reserved
28:26	**Color Format:** This field selects the number of bits per color sent to a receiver device connected to this port. Color format takes place on the Vblank after being written. Color format change must be done as a part of mode set since different color depths require different pixel clock settings. Selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer results in dithering the output stream. 000 = 8 bits per color **(Default, x3 mode)** 001 = RESERVED for 10 bits per color 010 = RESERVED for 6 bits per color 011 = RESERVED 1xx = RESERVED
25:19	Reserved
18	Reserved
17:16	**Symbol Clock Duty Cycle:** These bits control the output clock duty cycle to enable EMI mitigation on the external UDI link. 10/90 cycle has been measured to have ~13dB EMI improvement over a 50/50 duty cycle. 00 = **(Default)** 50/50 duty cycle: Clock output is 0000011111 01 = 10/90 duty cycle: Clock output is 0111111111 followed by 0000000001 10 = 20/80 duty cycle: Clock output is 0011111111 followed by 0000000011 11 = Reserved
15	Reserved: :
14	Reserved
13	Reserved:
12	Reserved:
11:10	**Encoding:** These bits select among encoding types. It is set as part of the display detection process. Control codes for ANSI 8b/10b and TMDS encoding must be programmed using these

	bits. Please note that ANSI 8b/10b and TMDS encoding can only be enabled on one port at a time, as only one HPD pin is available for use between ports B and C. 00 = Reserved 01 = Reserved 10 = TMDS encoding (external link and HDMI only)See the HDMI specification for control codes. In this mode, the external HPD pin is used to generate hotplug. In fixed frequency mode, start of fill and end of fill values for TMDS must be programmed using register 6114C. 11 = Reserved
9	Null packets enabled during Vsync This bit enables a null packet (32 bytes of a value of 0) to be sent when Vsync=1 on this port, required for HDMI operation. It also enables preambles and guardbands prior to the null packets, in accordance with the HDMI specification. It is only valid for modes that use TMDS encoding. 0 = Disable null infoframe packets when Vsync=1 on this port. **(Default)** 1 = Enable null infoframe packets when Vsync=1 on this port.
8	**Color Range Select:** This bit is used to select the color range of RBG outputs in HDMI mode. It is only valid when using TMDS encoding and 8 bit per color mode. 0 = Apply full 0-255 color range to the output **(Default)** 1 = Apply 16-235 color range to the output
7	**Reserved**
6	**Audio Output Enable:** This bit directs audio to this port. When enabled and audio data is available, the audio data will be combined with the video data and sent over this port. The audio unit uses the status of this bit to indicate presence of the HDMI output to the audio driver. 0 = **(Default)** No audio output on this port 1 = Enable audio on this port
5	**Reserved**
4:3	Sync Polarity: Please note that sync polarity does not apply to ANSI coding. Indicates the polarity of Hsync and Vsync. Inverted polarity is transmitted as SYNC-BLANK-SYNC and standard polarity is transmitted as BLANK-SYNC-BLANK. For example, if Vsync is not inverted and Hsync is inverted, an Hsync period transmitted during Vsync would be transmitted as BLANK+VS+HS – BLANK+VS – BLANK+VS+HS. Please note that in native VGA modes, these bits have no effect. In native VGA modes, sync

	polarity is determined by VRshr3c2d76b[7:6], the VGA polarity bits in VGA control. 00 = VS and HS are active low (inverted) 01 = VS is active low (inverted), HS is active high 10 = VS is active high, HS is active low (inverted) 11 = (Default) VS and HS are active high
2	Digital Port B Detected: Read-only bit indicating whether a digital port B was detected during initialization. It signifies the level of the GMBUS port 4 data line at boot. This bit is valid regardless of whether the port is enabled. 0 = Digital Port B not detected during initialization 1 = Digital Port B detected during initialization AccessType: Read Only
1:0	Reserved: MBZ

HDMIC—Digital Display Port C Register

Address Offset:61160h

Default Value: 00000018h

Normal Access: Read/Write

Description: HDMIC port control

The operating mode of the port is determined by the setting of the encoding register field (bits 11:10).

Bit	Description
31	**HDMIC Enable (Digital Display Port C Enable):** Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written. Both this bit and bit 6 of this register must be enabled to send audio over this port in HDMI. This port must not be enabled simultaneously with DisplayPort C. 1 = Enable. This bit enables the Digital Display Port C interface for HDMI or DVI modes. 0 = Disable and tristates the Digital Display Port C interface for HDMI or DVI modes.
30	**Pipe Select:** This bit determines from which display pipe the source data will originate. This only applies to devices with dual display pipes. Pipe selection takes place on the Vblank after being written 0 = Pipe A

	1 = Pipe B
29	**Reserved**
28:26	**Color Format:** This field selects the number of bits per color sent to a receiver device connected to this port. Color format takes place on the Vblank after being written. Color format change must be done as a part of mode set since different color depths require different pixel clock settings. Selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer results in dithering the output stream. 000 = 8 bits per color **(Default)** 001 = RESERVED for 10 bits per color 010 = RESERVED for 6 bits per color 011 = RESERVED 1xx = RESERVED
25:19	Reserved
18	**Reserved**
17:16	**Symbol Clock Duty Cycle:** These bits control the output clock duty cycle to enable EMI mitigation on the external HDMI link. 10/90 cycle has been measured to have ~13dB EMI improvement over a 50/50 duty cycle. 00 = **(Default)** 50/50 duty cycle: Clock output is 0000011111 01 = 10/90 duty cycle: Clock output is 0111111111 followed by 0000000001 **(HDMI only)** 10 = 20/80 duty cycle: Clock output is 0011111111 followed by 0000000011 **(HDMI only)** 11 = Reserved
15	Reserved
14	Reserved
13	Reserved
12	Reserved
11:10	**Encoding:** These bits select among encoding types. It is set as part of the display detection process. Control codes for ANSI 8b/10b and TMDS encoding must be programmed using these bits. Please note that ANSI 8b/10b and TMDS encoding can only be enabled on one port at a time, as only one HPD pin is available for use between ports B and C.

	00 = Reserved 01 = Reserved 10 = TMDS encoding (external link and HDMI only) See the HDMI specification for control codes. In this mode, the external HPD pin is used to generate hotplug. In fixed frequency mode, start of fill and end of fill values for TMDS must be programmed using register 6114C. 11 = Reserved
9	Null packets enabled during Vsync This bit enables a null packet (32 bytes of a value of 0) to be sent when Vsync=1 on this port, required for HDMI operation. It also enables preambles and guardbands prior to the null packets, in accordance with the HDMI specification. It is only valid for modes that use TMDS encoding. 0 = Disable null infoframe packets when Vsync=1 on this port. **(Default)** 1 = Enable null infoframe packets when Vsync=1 on this port.
8	**Color Range Select:** This bit is used to select the color range of RBG outputs in HDMI mode. It is only valid when using TMDS encoding and 8 bit per color mode. 0 = Apply full 0-255 color range to the output **(Default)** 1 = Apply 16-235 color range to the output **(pre-VLV)**
7	**Reserved**
6	**Audio Output Enable: :** This bit directs audio to this port. When enabled and audio data is available, the audio data will be combined with the video data and sent over this port. The audio unit uses the status of this bit to indicate presence of the HDMI output to the audio driver. 0 = **(Default)** No audio output on this port 1 = Enable audio on this port (pre-VLV)
5	**Reserved**
4:3	**Sync Polarity:** Please note that sync polarity does not apply to ANSI coding. Indicates the polarity of Hsync and Vsync. Inverted polarity is transmitted as SYNC-BLANK-SYNC and standard polarity is transmitted as BLANK-SYNC-BLANK. For example, if Vsync is not inverted and Hsync is inverted, an Hsync period transmitted during Vsync would be transmitted as BLANK+VS+HS – BLANK+VS – BLANK+VS+HS. Please note that in native VGA modes, these bits have no effect. In native VGA modes, sync polarity is determined by VRshr3c2d76b[7:6], the VGA polarity bits in VGA control.

	00 = VS and HS are active low (inverted) 01 = VS is active low (inverted), HS is active high 10 = VS is active high, HS is active low (inverted) 11 = (Default) VS and HS are active high
2	**Digital Port C Detected:** Read-only bit indicating whether a digital port C was detected during initialization. It signifies the level of the GMBUS port 3 (port C) data line at boot. This bit is valid regardless of whether the port is enabled. 0 = Digital Port C not detected during initialization 1 = Digital Port C detected during initialization (default) AccessType: Read Only
1	**DDI2 Port Detected:** Read-only bit indicating whether the DDI2 port was detected during initialization. It signifies the level of the GMBUS port 1 data line at boot. This bit is valid regardless of whether the port is enabled. 0 = DDI2 Port not detected during initialization 1 = DDI2 Port detected during initialization (default) AccessType: Read Only
0	Reserved: MBZ

Display Digital Port Hot Plug Control Register

Display Digital Port Hot Plug Control Register	
Register Type:	MMIO
Address Offset:	61164h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

Bit	Description
31:21	Reserved Project: All Format:

20	Reserved. Digital_Port_D_Hot_Plug_Detect_Input_Enable Project: All Default Value: 0b Controls the state of the HPD buffer for the digital port. The buffer state is independent of whether the port is enabled or not. **Value / Name / Description / Project** 0b / Disable / Buffer disabled / All 1b / Enable / Buffer enabled. Hot plugs bit reflect the electrical state of the HPD pin / All
19:18	Reserved. Digital_Port_D_Hot_Plug_Short_Pulse_Duration Project: All Default Value: 0b These bits define the duration of the pulse defined as a short pulse. **Value / Name / Description / Project** 00b / 2ms / 2mS / All 01b / 4.5ms / 4.5mS / All 10b / 6ms / 6mS / All 11b / 100ms / 100mS / All

<table>
<tr><td></td><td></td></tr>
<tr><td>17:16</td><td>
Reserved. Digital_Port_D_Hot_Plug_Interrupt_Detect_Status

Project: All

Default Value: 0b

AccessType: One to Clear

This reflects hot plug detect status on the digital port. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. When either a long or short pulse is detected, one of these bits will set. These bits are ORed together to go to the main ISR hotplug register bit.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr>
<tr><td>00b</td><td>No Detect</td><td>Digital port hot plug event not detected</td><td>All</td></tr>
<tr><td>X1b</td><td>Short Detect</td><td>Digital port short pulse hot plug event detected</td><td>All</td></tr>
<tr><td>1Xb</td><td>Long Detect</td><td>Digital port long pulse hot plug event detected</td><td>All</td></tr>
</table>
</td></tr>
<tr><td>15:13</td><td>Reserved Project: All Format:</td></tr>
</table>

<table>
<tr><td>12</td><td>Reserved. Digital_Port_C_Hot_Plug_Detect_Input_Enable

Project: All

Default Value: 0b

Controls the state of the HPD buffer for the digital port. The buffer state is independent of whether the port is enabled or not.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr>
<tr><td>0b</td><td>Disable</td><td>Buffer disabled</td><td>All</td></tr>
<tr><td>1b</td><td>Enable</td><td>Buffer enabled. Hot plugs bit reflect the electrical state of the HPD pin</td><td>All</td></tr>
</table></td></tr>
<tr><td>11:10</td><td>Reserved. Digital_Port_C_Hot_Plug_Short_Pulse_Duration

Project: All

Default Value: 0b

These bits define the duration of the pulse defined as a short pulse.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr>
<tr><td>00b</td><td>2ms</td><td>2mS</td><td>All</td></tr>
<tr><td>01b</td><td>4.5ms</td><td>4.5mS</td><td>All</td></tr>
<tr><td>10b</td><td>6ms</td><td>6mS</td><td>All</td></tr>
<tr><td>11b</td><td>100ms</td><td>100mS</td><td>All</td></tr>
</table></td></tr>
<tr><td>9:8</td><td>Reserved. Digital_Port_C_Hot_Plug_Interrupt_Detect_Status</td></tr>
</table>

Project: All

Default Value: 0b

AccessType: One to Clear

This reflects hot plug detect status on the digital port. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. When either a long or short pulse is detected, one of these bits will set. These bits are ORed together to go to the main ISR hotplug register bit.

Value	Name	Description	Project
00b	No Detect	Digital port hot plug event not detected	All
X1b	Short Detect	Digital port short pulse hot plug event detected	All
1Xb	Long Detect	Digital port long pulse hot plug event detected	All

7:5

Reserved Project: All Format:

4

Reserved. Digital_PORT_B_Hot_Plug_Detect_Input_Enable

Project: All

Default Value: 0b

Controls the state of the HPD buffer for the digital port. The buffer state is independent of whether the port is enabled or not.

Value	Name	Description	Project
0b	Disable	Buffer disabled	All
1b	Enable	Buffer enabled. Hot plugs bit reflect the electrical state of the HPD pin	All

<table>
<tr><td></td><td></td></tr>
<tr><td>3:2</td><td>
Reserved. Digital_Port_B_Hot_Plug_Short_Pulse_Duration

Project: All

Default Value: 0b

These bits define the duration of the pulse defined as a short pulse.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr>
<tr><td>00b</td><td>2ms</td><td>2mS</td><td>All</td></tr>
<tr><td>01b</td><td>4.5ms</td><td>4.5mS</td><td>All</td></tr>
<tr><td>10b</td><td>6ms</td><td>6mS</td><td>All</td></tr>
<tr><td>11b</td><td>100ms</td><td>100mS</td><td>All</td></tr>
</table>
</td></tr>
<tr><td>1:0</td><td>
Reserved. Digital_Port_B_Hot_Plug_Interrupt_Detect_Status

Project: All

Default Value: 0b

AccessType: One to Clear

This reflects hot plug detect status on the digital port. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. When either a long or short pulse is detected, one of these bits will set. These bits are ORed together to go to the main ISR hotplug register bit.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr>
<tr><td>00b</td><td>No Detect</td><td>Digital port hot plug event not detected</td><td>All</td></tr>
<tr><td>X1b</td><td>Short Detect</td><td>Digital port short pulse hot plug event detected</td><td>All</td></tr>
</table>
</td></tr>
</table>

	1Xb	Long Detect	Digital port long pulse hot plug event detected	All

DP_B—DisplayPort B Control Register

Address Offset:64100h

Default Value: 00000018h

Normal Access: Read/Write

Description: Display Port B control (dprrega_b0.v – ql_displayb1)

Size: 32 bits

Please note that DisplayPort B uses the same lanes as HDMIB. Therefore HDMIB and DisplayPort B cannot be enabled simultaneously. This register is write-protected by the pipe A or pipe B Panel Power Control Register.

Calculation of TU is as follows:

For modes that divide into the link frequency evenly,

Active/TU = payload/capacity

Please note that this is the same ratio as data m/n:

Payload/capacity = dot clk * bytes per pixel / ls_clk * # of lanes

Bit	Description
31	**DisplayPort B Enable:** Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written. 1 = Enable. This bit enables the Display Port B interface. 0 = Disable and tristates the Display Port B interface.
30	**Pipe Select:** This bit determines from which display pipe the source data will originate. Pipe selection takes place on the Vblank after being written 0 = Pipe A 1 = Pipe B
29:28	**Link training pattern enable:** These bits are used for link initialization as defined in the DisplayPort specification. Please note that the link must first be configured prior to sending training patterns.

	00 – Pattern 1 enabled: Repetition of D10.2 characters **Default**. **01 – Pattern 2 enabled:** Repetition of K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2. **10 – Idle Pattern enabled:** Transmit BS followed by VB-ID with NoVideoStream_flag set to 1, five times 11 – Link not in training: Send normal pixels
27:25	Reserved: MBZ
24:22	Reserved: MBZ
21:19	**Port Width Selection:** This bit selects the number of lanes to be enabled on the DisplayPort link. Port width selection takes place on the Vblank after being written. Port width change must be done as a part of mode set. 000 = x1 Mode (Default) 001 = x2 Mode. 010 = RESERVED 011 = x4 Mode. 1xx = RESERVED
18	**Reserved**
17:16	Reserved: MBZ
15	Reserved: MBZ
14:9	Reserved: MBZ
8	ASR enable: : this bit enables the Alternate Scrammbler Reset capability for eDP port to use alternate scrambler reset value of FFFEh 1 - ASR enable 0 – ASR disable
7	Reserved
6	**Audio Output Enable:** This bit enables audio on this output port. It may be enabled or disabled only when the link training is complete and set to “Normal” 0 = Audio output disabled 1 = Audio output enabled

5	**Reserved**
4:3	**Sync Polarity:** Indicates the polarity of Hsync and Vsync. Please note that in native VGA modes, these bits have no effect. In native VGA modes, sync polarity is determined by VRshr3c2d76b[7:6], the VGA polarity bits in VGA control. 00 = VS and HS are active low (inverted) 01 = VS is active low (inverted), HS is active high 10 = VS is active high, HS is active low (inverted) 11 = (Default) VS and HS are active high
2	Digital Display B Detected: Read-only bit indicating whether a digital display was detected during initialization. It signifies the level of the GMBUS port 4 (port B) data line at boot. 0 = digital display not detected during initialization (Default) 1 = digital display detected during initialization AccessType: Read Only
1	Reserved: MBZ
0	Disable framestart window to stall audio sample. This applies to both pipes. 0 = Enable framestart window to stall audio sample (default) 1 = Disable framestart window to stall audio sample

DPB_AUX_CH_CTL—Display Port B AUX Channel Control

Memory Address Offset:64110h

Default Value: 00050000h

Access:Read/Write

Description: AuxB control (dprrega_b0.v – auxb_ctl_rdback)

Programming note: Do not change any fields while Busy bit 31 is asserted.

Bit	Description
31	Send/Busy: Setting this bit to a one initiates the transaction, when read this bit will be a 1 until the transmission completes. The transaction is completed when the response is received or when a

	timeout occurs. Do not write a 1 again until transaction completes. Writes of 0 will be ignored.
30	Done: A sticky bit that indicates the transaction has completed. SW must write a 1 to this bit to clear the event. AccessType: One to Clear
29	Interrupt on Done: Enable an interrupt in the hotplug status register when the transaction completes or times out.
28	Time out error: A sticky bit that indicates the transaction has timed out. SW must write a 1 to this bit to clear the event. AccessType: One to Clear
27:26	Time out timer value: 00: 400us (default)01: 600us10: 800us11: 1600us The time count depends on the 2X bit clock divider (bits 10:0) being programmed for 2MHz.
25	**Receive error:** A sticky bit that indicates that the data received was corrupted, not in multiples of a full byte, or more than 20 bytes. SW must write a 1 to this bit to clear the event. AccessType: One to Clear
24:20	Message Size: This field is used to indicate the total number bytes to transmit (including the header). It also indicates the number of bytes received in a transaction (including the header). This field is valid only only when the done bit is set and timeout or receive error has not occurred. Sync/Stop are not part of the message or the message size. Reads of this field will give the response message size. The read value will not be valid while Busy bit 31 is asserted. Message sizes of 0 or >20 are not allowed.
19:16	Precharge Time: Used to determine the precharge time for the Aux Channel drivers. The value is the number of microseconds times 2. This depends on the 2X bit clock divider (bits 10:0) being programmed for 2MHz. Default is 5 decimal which gives 10us of precharge. Example: For 12us precharge, program 6 (12us/2us).
15	**Reserved**

14	**Reserved**
13	**Reserved**
12	**Reserved**
11	**Reserved**
10:0	2X Bit Clock divider: Used to determine the 2X bit clock the Aux Channel logic runs on. This value divides the input clock frequency down to 2X bit clock rate. The 2X bit clock rate is ideally 2MHz (0.5us). Example: For 300MHz input clock and desired 2MHz 2X bit clock, program 150 (300MHz/2MHz).

DPB_AUX_CH_DATA1—Display Port B AUX Data Register 1

Memory Address Offset:64114h

Default Value: 00000000h

Access:Read/Write

Description : AuxB Data1 (dprrega_b0.v – auxb_dpr_data1, ql_auxb_d1)

The read value will not be valid while Busy bit 31 is asserted.

Bit	Description
31:0	AUX_CH_DATA1[31:0]: The first Dword of the message. The Msbyte is transmitted first. Reads will give the response data after transaction complete.

DPB_AUX_CH_DATA2—Display Port B AUX Data Register 2

Memory Address Offset:64118h

Default Value: 00000000h

Access:Read/Write

Description: AuxB Data2 (dprrega_b0.v – auxb_dpr_data2, ql_auxb_d2)

The read value will not be valid while Busy bit 31 is asserted.

Bit	Description
31:0	AUX_CH_DATA2[31:0]:

	The second Dword of the message. The Msbyte is transmitted first. Only used if the message size is greater than 4. Reads will give the response data after transaction complete.

DPB_AUX_CH_DATA3—Display Port B AUX Data Register 3

Memory Address Offset:6411Ch

Default Value: 00000000h

Access:Read/Write

Description: AuxB Data3 (dprrega_b0.v – auxb_dpr_data3, ql_auxb_d3)

The read value will not be valid while Busy bit 31 is asserted.

Bit	Description
31:0	AUX_CH_DATA3[31:0]: The third Dword of the message. The Msbyte is transmitted first. Only used if the message size is greater than 8. Reads will give the response data after transaction complete.

DPB_AUX_CH_DATA4—Display Port B AUX Data Register 4

Memory Address Offset:64120h

Default Value: 00000000h

Access:Read/Write

Description: AuxB Data4 (dprrega_b0.v – auxb_dpr_data4, ql_auxb_d4)

The read value will not be valid while Busy bit 31 is asserted.

Bit	Description
31:0	AUX_CH_DATA4[31:0]: The fourth Dword of the message. The Msbyte is transmitted first. Only used if the message size is greater than 12. Reads will give the response data after transaction complete.

DPB_AUX_CH_DATA5—Display Port B AUX Data Register 5

Memory Address Offset:64124h

Default Value: 00000000h

Access:Read/Write

Description: AuxB Data5 (dprrega_b0.v – auxb_dpr_data5, ql_auxb_d5)

The read value will not be valid while Busy bit 31 is asserted.

Bit	Description
31:0	AUX_CH_DATA5[31:0]: The fifth Dword of the message. The Msbyte is transmitted first. Only used if the message size is greater than 16. Reads will give the response data after transaction complete.

DP_C—Display Port C Control Register

Address Offset:64200h

Default Value: 00000018h

Normal Access: Read/Write

Description: Display Port C control (dprrega_b0.v – ql_displayc1)

Size: 32 bits

Please note that DisplayPort C uses the same lanes as HDMIC. Therefore HDMIC and DisplayPort C cannot be enabled simultaneously. This register is write-protected by the pipe A or pipe B Panel Power Control Register.

Bit	Description
31	**DisplayPort C Enable:** Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written. Both this bit and bit 6 of this register must be enabled to send audio over this port. 1 = Enable. This bit enables the Display Port C interface. 0 = Disable and tristates the Display Port C interface.
30	**Pipe Select:** This bit determines from which display pipe the source data will originate. Pipe selection takes place on the Vblank after being written 0 = Pipe A 1 = Pipe B
29:28	**Link training pattern enable:** These bits are used for link initialization as defined in the DisplayPort specification. Please note that the link must first be configured prior to sending training patterns. **00 – Pattern 1 enabled:** Repetition of D10.2 characters **Default**. **01 – Pattern 2 enabled:** Repetition of K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2. **10 – Idle Pattern enabled:** Transmit BS followed by VB-ID with NoVideoStream_flag set to 1, five times

	11 – Link not in training: Send normal pixels
27:25	**Reserved**
24:22	**Reserved**
21:19	**Port Width Selection:** This bit selects the number of lanes to be enabled on the DisplayPort link. Port width selection takes place on the Vblank after being written. Port width change must be done as a part of mode set. 000 = x1 Mode (Default) 001 = x2 Mode. 010 = RESERVED 011 = x4 Mode. 1xx = RESERVED
18	**Reserved**
17:16	Reserved: MBZ
15	Reserved: MBZ
14:9	Reserved: MBZ
8	ASR enable: : this bit enables the Alternate Scrambler Reset capability for eDP port to use alternate scrambler reset value of FFFEh 1 - ASR enable 0 – ASR disable
7	Reserved
6	**Audio Output Enable:** This bit enables audio on this output port. It may be enabled or disabled only when the link training is complete and set to “Normal” 0 = Audio output disabled 1 = Audio output enabled
5	**Reserved**
4:3	Sync Polarity: Indicates the polarity of Hsync and Vsync. Please note that in native VGA modes, these bits have no effect. In native VGA modes, sync polarity is determined by VRshr3c2d76b[7:6], the VGA polarity bits in VGA control. 00 = VS and HS are active low (inverted)

	01 = VS is active low (inverted), HS is active high 10 = VS is active high, HS is active low (inverted) 11 = (Default) VS and HS are active high
2	Digital Display C Detected: Read-only bit indicating whether a digital display was detected during initialization. It signifies the level of the GMBUS port data line at boot. 0 = digital display not detected during initialization (Default) 1 = digital display detected during initialization AccessType: Read only
1:0	Reserved: MBZ

DPC_AUX_CH_CTL—Display Port C AUX Channel Control

Memory Address Offset:64210h

Default Value: 00050000h

Access:Read/Write

Description: AuxC Data1 (dprrega_b0.v – auxc_dpr_data1, ql_auxc_d1)

Programming note: Do not change any fields while Busy bit 31 is asserted.

Bit	Description
31	Send/Busy: Setting this bit to a one initiates the transaction, when read this bit will be a 1 until the transmission completes. The transaction is completed when the response is received or when a timeout occurs. Do not write a 1 again until transaction completes. Writes of 0 will be ignored.
30	Done: A sticky bit that indicates the transaction has completed. SW must write a 1 to this bit to clear the event. AccessType: One to Clear
29	Interrupt on Done: Enable an interrupt in the hotplug status register when the transaction completes or times out.
28	Time out error: A sticky bit that indicates the transaction has timed out. SW must write a 1 to this bit to clear

	the event. AccessType: One to Clear
27:26	Time out timer value: 00: 400us (default)01: 600us10: 800us11: 1600us The time count depends on the 2X bit clock divider (bits 10:0) being programmed for 2MHz.
25	**Receive error:** A sticky bit that indicates that the data received was corrupted, not in multiples of a full byte, or more than 20 bytes. SW must write a 1 to this bit to clear the event. AccessType: One to Clear
24:20	Message Size: This field is used to indicate the total number bytes to transmit (including the header). It also indicates the number of bytes received in a transaction (including the header). This field is valid only only when the done bit is set and timeout or receive error has not occurred. Sync/Stop are not part of the message or the message size. Reads of this field will give the response message size. The read value will not be valid while Busy bit 31 is asserted. Message sizes of 0 or >20 are not allowed.
19:16	Precharge Time: Used to determine the precharge time for the Aux Channel drivers. The value is the number of microseconds times 2. This depends on the 2X bit clock divider (bits 10:0) being programmed for 2MHz. Default is 5 decimal which gives 10us of precharge. Example: For 12us precharge, program 6 (12us/2us).
15	**Reserved**
14	**Reserved**
13	**Reserved**
12	**Reserved**
11	**Reserved**
10:0	2X Bit Clock divider: Used to determine the 2X bit clock the Aux Channel logic runs on.

	This value divides the input clock frequency down to 2X bit clock rate. The 2X bit clock rate is ideally 2MHz (0.5us). Example: For 300MHz input clock and desired 2MHz 2X bit clock, program 150 (300MHz/2MHz).

DPC_AUX_CH_DATA1—Display Port C AUX Data Register 1

Memory Address Offset:64214h

Default Value: 00000000h

Access:Read/Write

Description: AuxC Data1 (dprrega_b0.v – auxc_dpr_data1, ql_auxc_d1)

The read value will not be valid while Busy bit 31 is asserted.

Bit	Description
31:0	AUX_CH_DATA1[31:0]: The first DWord of the message. The MSbyte is transmitted first. Reads will give the response data after transaction complete.

DPC_AUX_CH_DATA2—Display Port C AUX Data Register 2

Memory Address Offset:64218h

Default Value: 00000000h

Access:Read/Write

Description: AuxC Data2 (dprrega_b0.v – auxc_dpr_data2, ql_auxc_d2)

The read value will not be valid while Busy bit 31 is asserted.

Bit	Description
31:0	AUX_CH_DATA2[31:0]: The second DWord of the message. The MSbyte is transmitted first. Only used if the message size is greater than 4. Reads will give the response data after transaction complete.

DPC_AUX_CH_DATA3—Display Port C AUX Data Register 3

Memory Address Offset:6421Ch

Default Value: 00000000h

Access:Read/Write

Description: AuxC Data3 (dprrega_b0.v – auxc_dpr_data3, ql_auxc_d3)

The read value will not be valid while Busy bit 31 is asserted.

Bit	Description
31:0	AUX_CH_DATA3[31:0]: The third DWord of the message. The MSbyte is transmitted first. Only used if the message size is greater than 8. Reads will give the response data after transaction complete.

DPC_AUX_CH_DATA4—Display Port C AUX Data Register 4

Memory Address Offset:64220h

Default Value: 00000000h

Access:Read/Write

Description: AuxC Data4 (dprrega_b0.v – auxc_dpr_data4, ql_auxc_d4)

The read value will not be valid while Busy bit 31 is asserted.

Bit	Description
31:0	AUX_CH_DATA4[31:0]: The fourth DWord of the message. The MSbyte is transmitted first. Only used if the message size is greater than 12. Reads will give the response data after transaction complete.

DPC_AUX_CH_DATA5—Display Port C AUX Data Register 5

Memory Address Offset:64224h

Default Value: 00000000h

Access:Read/Write

Description: AuxC Data5 (dprrega_b0.v – auxc_dpr_data5, ql_auxc_d5)

The read value will not be valid while Busy bit 31 is asserted.

Bit	Description
31:0	AUX_CH_DATA5[31:0]: The fifth DWord of the message. The MSbyte is transmitted first. Only used if the message size is greater than 16. Reads will give the response data after transaction complete.

Panel Registers

PipeA Panel Power Sequencing Registers

PipeA_PP_STATUS—PipeA Panel Power Status Register

Address offset:61200h

Default Value: 08000000h

Description: PP Status (dplrreg.v – panel_pwr_sr)

Normal Access: Read only

Bit	Description
31	Panel Power On Status 0 = Indicates that the panel power down sequencing has completed. A power cycle delay may be currently active. It is safe and allowed to program pipe timing and DPLL registers. If this bit is not a zero, it activates the register write protect and writes to those registers will be ignored unless the write protect key value is set in the panel sequencing control register. 1 = In conjunction with bits Power Sequence Progress field and Power Cycle Delay Active, this bit set to a one indicates that the panel is currently powered up or is currently in the power down sequence and it is unsafe to change the pipe timing and DPLL registers for the pipe that is assigned to the embedded panel output. If the embedded panel port is selected as the target for the panel control, Software is responsible for enabling the LCD display by writing a "1" to the port enable bit only after all pipe timing, DPLL registers are properly programmed, and the PLL has locked to the reference signal. This bit is cleared (set to 0) only after the panel power down sequencing is completed.
30	**Require Asset Status:** This bit indicates the status of programming of the display PLL and the selected display port. This a power on cycle will not be allowed unless this status indicates that the required assets are programmed and ready for use. 0 = All required assets are not properly programmed. 1 = All required assets are ready for the driving of a panel. The following conditions determine that the assets are ready: 1) Display Pipe PLL Enabled and frequency locked (bit-31 of DPLL Control Register for the pipe attached to the embedded panel port). 2) Display Pipe Enabled (bit-31 of PIPECONF—Pipe Configuration Register. For the pipe attached to the embedded panel port) 3) Embedded Panel Port is Programmed Enabled

29:28	Power Sequence Progress 00 = Indicates that the panel is not in a power sequence 01 = Indicates that the panel is in a power up sequence (may include power cycle delay) 10 = Indicates that the panel is in a power down sequence 11 = Reserved
27	**Power Cycle Delay Active:** Power cycle delays occur after a panel power down sequence or after a hardware reset. On reset, a power cycle delay will occur using the default value for the timing. 0 = A power cycle delay is not currently active 1 = A power cycle delay (T4) is currently active
26:4	Reserved
3:0	**Reserved**

PipeA_PP_CONTROL—PipeA Panel Power Control Register

Address offset:61204h

Default Value: 000000000h

Normal Access: Read/Write

Description: PP Control (dplrreg.v – pnl_pwr_cntl)

Bit	Description
31:16	Write Protect Key ABCD – Write protect off When this field is programmed to anything except the write protect off setting and the panel is either powered up or in the process of a power up sequence, a set of registers involved in generation of panel timing or control become write-protected. Any write cycles to those write-protected registers, while they will complete as normal, will not change the value of the register when write-protected. When this register field contains the write protect off key value, write protect will be unconditionally disabled. In situations where the embedded panel port is unused, the port should remain powered down and the write protect will be inactive. This field in normal operation should be left to all zeros and never programmed with the key value. It exists only to allow testing and workarounds. List of Write-protected registers: (LVDS and Panel sequencing Registers):

	LVDS – Digital Display Port Control – Address: 61180h–61183h Pipe A Panel power on sequencing delays - Address: 61208-6120Bh Pipe A Panel power off sequencing delays – Address: 6120Ch – 6120Fh Pipe A Panel power cycle delay and Reference Divisor – Address: 61210h – 61213 Display Port B Control Register – Address 64100 (if Display port B is connected to pipe A) Display Port C Control Register – Address 64200 (if Display port C is connected to pipe A) (DPLL registers): DPLL Control Registers FPA0—DPLL Divisor Register FPA1—DPLL Divisor Register 1 FPB0—DPLL Divisor Register FPB1—DPLL Divisor Register 1 (Display Pipe timing registers except source size) HTOTAL—Horizontal Total Register HBLANK—Horizontal Blank Register HSYNC_—Horizontal Sync Register VTOTAL_—Vertical Total Register VBLANK_—Vertical Blank Register VSYNC_—Vertical Sync Register
15:4	Reserved
3	**eDP panel Vdd enable:** Enabling this bit enables the panel vdd if the embedded panel is DisplayPort, as indicated in bits 31:30 of the panel power on sequencing. Software must enable this bit for eDP link training. After eDP link training is done, software must disable it and let the normal panel power sequencing to take control. 0 = eDP panel Vdd disabled 1 = eDP panel Vdd enabled
2	**Backlight Enable::** Enabling this bit enables the panel backlight if the embedded panel is DisplayPort, as indicated in bits 31:30 of the panel power on sequencing. Software must enable this bit after training the link, and disable it when disabling the panel power state target. 0 = Backlight disabled 1 = Backlight enabled
1	**Power Down on Reset:** Enabling this bit causes the panel to power down when a reset warning comes to the GMCH from the ICH. When system reset is initiated, the embedded panel port

	automatically begins the panel power down sequence. If the panel is not on during a reset event, this bit is ignored. 0 = Do not run panel power down sequence when reset is detected1 = Run panel power down sequence when system is reset
0	**Power State Target:** Writing this bit can occur any time, it will only be used at the completion of any current power cycle. 0 = The panel power state target is off, if the panel is either on or in a power on sequence, a power off sequence is started as soon as the panel reaches the power on state. This may include a power cycle delay. If the panel is currently off, there is no change of the power state or sequencing done. 1= The panel power state target is on, if the panel is in either the off state or a power off sequence, if all pre-conditions are met, a power on sequence is started as soon as the panel reaches the power off state. This may include a power cycle delay. If the panel is currently off, there is no change of the power state or sequencing done. While the panel is on or in a power on sequence, the register write lock will be enabled.

PipeA_PP_ON_DELAYS—PipeA Panel Power on Sequencing Delays

Address offset:61208h

Default Value: 00000000h

Normal Access: Read/Write

Description: PP On Delay values (dplrreg.v – DPLRppon_sd)

Write Protect by Panel Power Sequencer on

Bit	Description
31:30	**Panel Control port select:** These bits define to which port the embedded panel is connected. This is used for automatic control of the panel power. If the selected port is disabled or if the port is not on pipe-B, then, the power sequence will not allow a panel power up. 00 = Reserved 01 = Panel is connected to the embedded DisplayPort B 10 = Panel is connected to the embedded DisplayPort C 11 = Reserved The selection of non-existent ports are not allowed. This programming will disable panel power sequencing logic.
29	Reserved

28:16	**Power up delay:** Programmable value of panel power sequencing delay during panel power up. This provides the time delay for the T1+T2 time sequence. The time unit used is the 100us timer.
15:13	Reserved
12:0	**Power on to Backlight enable delay:** Programmable value of panel power sequencing delay during panel power up. This provides the time delay for the T5 (T3 for DisplayPort) time sequence. The time unit used is the 100us timer.

PipeA_PP_OFF_DELAYS—PipeA Panel Power off Sequencing Delays

Address offset:6120Ch

Default Value: 00000000h

Normal Access: Read/Write

Description: PP Delay Off values (dplrreg.v – DPLRppoff_sd)Write Protect by Panel Power Sequencer on Mobile products

Bit	Description
31:29	Reserved
28:16	**Power Down delay:** Programmable value of panel power sequencing delay during power up. This provides the time delay for the T3 (T5 for DisplayPort) time sequence. The time unit used is the 100us timer.
15:13	Reserved
12:0	**Power Backlight off to power down delay:** Programmable value of panel power sequencing delay during power down. This provides the time delay for the Tx (T4 for DisplayPort) time sequence. The time unit used is the 100us timer.

PipeA_PP_DIVISOR—PipeA Panel Power Cycle Delay and Reference Divisor

Address offset:61210h

Default Value: 00270F04h

Normal Access: Read/Write

Description: PP Divisor (dplrreg.v – DPLRrefdiv_pp_cd)Write Protect by Panel Power Sequencer on Mobile Products

This register selects the reference divisor and controls how long the panel must remain in a power off condition once powered down. This has a default value that allows a timer to initiate directly after device reset. If the panel limits how fast we may sequence from up to down to up again. Typically this is .5-1.5 sec. But limited to 400ms in the SPWG specification. This register forces the panel to stay off for a programmed duration. Special care is needed around reset and D3 cold situations to conform to power cycle delay specifications.

Bit	Description
31:8	**Reference divider:** This field provides the value of the divider used for the creation of the panel timer reference clock. The output of the divider is used as the fastest of the three time bases (100us) for all other timers. The other time bases are divided from this frequency. The value of zero should not be used. When it is desired to divide by N, the actual value to be programmed is (N/2)-1. The value should be (100*RefinMHz/2)-1. The default value assumes the default value for the display core clock. The following are examples for various memory speeds. **Display Core FrequencyValue of Field** 233MHz 2D81h 200MHz 270Fh 133MHz 19F9h
7:5	Reserved
4:0	**Power Cycle Delay:** Programmable value of time panel must remain in a powered down state after powering down. For devices coming out of reset, the default values will define how much time must pass before a power on sequence can be started. This field uses the .1 S time base unit from the divider. If the panel power on sequence is attempted during this delay, the power on sequence will commence once the power cycle delay is complete. Writing a value of 0 selects no delay or is used to abort the delay if it is active. During the initial power up reset, a D3 cold power cycle, or a user instigated system reset, the timer will be set to the default value and the count down will begin after the de-assertion of reset. Writing this field to a zero while the count is active will abort this portion of the sequence. This corresponds to the T4 of the SPWG specification. Note: Even if the panel is not enabled, the T4 count happens after reset. This register needs to be programmed to a "+1" value. For instance for meeting the SPWG specification of 400mS, program 5 to achieve at least 400mS delay prior to powerup.

PipeB Panel Power Sequencing Registers ()

PipeB_PP_STATUS—PipeB Panel Power Status Register ()

Address offset:61300h

Default Value: 08000000h

Description: PP Status (dplrreg.v – panel_pwr_sr)

Normal Access: Read only

Bit	Description
31	Panel Power On Status 0 = Indicates that the panel power down sequencing has completed. A power cycle delay may be currently active. It is safe and allowed to program pipe timing and DPLL registers. If this bit is not a zero, it activates the register write protect and writes to those registers will be ignored unless the write protect key value is set in the panel sequencing control register. 1 = In conjunction with bits Power Sequence Progress field and Power Cycle Delay Active, this bit set to a one indicates that the panel is currently powered up or is currently in the power down sequence and it is unsafe to change the pipe timing and DPLL registers for the pipe that is assigned to the embedded panel output. If the embedded panel port is selected as the target for the panel control, Software is responsible for enabling the LCD display by writing a "1" to the port enable bit only after all pipe timing, DPLL registers are properly programmed, and the PLL has locked to the reference signal. This bit is cleared (set to 0) only after the panel power down sequencing is completed.
30	**Require Asset Status:** This bit indicates the status of programming of the display PLL and the selected display port. This a power on cycle will not be allowed unless this status indicates that the required assets are programmed and ready for use. 0 = All required assets are not properly programmed. 1 = All required assets are ready for the driving of a panel. The following conditions determine that the assets are ready: 1) Display Pipe PLL Enabled and frequency locked (bit-31 of DPLL Control Register for the pipe attached to the embedded panel port). 2) Display Pipe Enabled (bit-31 of PIPECONF—Pipe Configuration Register. For the pipe attached to the embedded panel port) 3) Embedded Panel Port is Programmed Enabled
29:28	Power Sequence Progress 00 = Indicates that the panel is not in a power sequence 01 = Indicates that the panel is in a power up sequence (may include power cycle delay) 10 = Indicates that the panel is in a power down sequence 11 = Reserved
27	**Power Cycle Delay Active:** Power cycle delays occur after a panel power down sequence or after a hardware reset. On reset, a power cycle delay will occur using the default value for the

	timing. 0 = A power cycle delay is not currently active 1 = A power cycle delay (T4) is currently active
26:4	Reserved
3:0	**Reserved**

PipeB_PP_CONTROL—PipeB Panel Power Control Register ()

Address offset:61304h

Default Value: 000000000h

Normal Access: Read/Write

Description: PP Control (dplrreg.v – pnl_pwr_cntl)

Bit	Description
31:16	Write Protect Key ABCD – Write protect off When this field is programmed to anything except the write protect off setting and the panel is either powered up or in the process of a power up sequence, a set of registers involved in generation of panel timing or control become write-protected. Any write cycles to those write-protected registers, while they will complete as normal, will not change the value of the register when write-protected. When this register field contains the write protect off key value, write protect will be unconditionally disabled. In situations where the embedded panel port is unused, the port should remain powered down and the write protect will be inactive. This field in normal operation should be left to all zeros and never programmed with the key value. It exists only to allow testing and workarounds. List of Write-protected registers: (Panel sequencing Registers): Pipe B Panel power on sequencing delays - Address: 61308-6130Bh Pipe B Panel power off sequencing delays – Address: 6130Ch – 6130Fh Pipe B Panel power cycle delay and Reference Divisor – Address: 61310h – 61313 Display Port B Control Register – Address 64100 (if Display port B is connected to pipe B) Display Port C Control Register – Address 64200 (if Display port C is connected to pipe B) (DPLL registers): DPLL Control Registers

	FPA0—DPLL Divisor Register FPA1—DPLL Divisor Register 1 FPB0—DPLL Divisor Register FPB1—DPLL Divisor Register 1 (Display Pipe timing registers except source size) HTOTAL—Horizontal Total Register HBLANK—Horizontal Blank Register HSYNC_—Horizontal Sync Register VTOTAL_—Vertical Total Register VBLANK_—Vertical Blank Register VSYNC_—Vertical Sync Register
15:4	Reserved
3	**eDP panel Vdd enable:** Enabling this bit enables the panel vdd if the embedded panel is DisplayPort, as indicated in bits 31:30 of the panel power on sequencing. Software must enable this bit for eDP link training. After eDP link training is done, software must disable it and let the normal panel power sequencing to take control. 0 = eDP panel Vdd disabled 1 = eDP panel Vdd enabled
2	**Backlight Enable::** Enabling this bit enables the panel backlight if the embedded panel is DisplayPort, as indicated in bits 31:30 of the panel power on sequencing. Software must enable this bit after training the link, and disable it when disabling the panel power state target. 0 = Backlight disabled 1 = Backlight enabled
1	**Power Down on Reset:** Enabling this bit causes the panel to power down when a reset warning comes to the GMCH from the ICH. When system reset is initiated, the embedded panel port automatically begins the panel power down sequence. If the panel is not on during a reset event, this bit is ignored. 0 = Do not run panel power down sequence when reset is detected1 = Run panel power down sequence when system is reset
0	**Power State Target:** Writing this bit can occur any time, it will only be used at the completion of any current power cycle. 0 = The panel power state target is off, if the panel is either on or in a power on sequence, a power off sequence is started as soon as the panel reaches the power on state. This may include a power cycle delay. If the panel is currently off, there is no change of the power state

	or sequencing done. 1= The panel power state target is on, if the panel is in either the off state or a power off sequence, if all pre-conditions are met, a power on sequence is started as soon as the panel reaches the power off state. This may include a power cycle delay. If the panel is currently off, there is no change of the power state or sequencing done. While the panel is on or in a power on sequence, the register write lock will be enabled.

PipeB_PP_ON_DELAYS—PipeB Panel Power on Sequencing Delays ()

Address offset:61308h

Default Value: 00000000h

Normal Access: Read/Write

Description: PP On Delay values (dplrreg.v – DPLRppon_sd)Write Protect by Panel Power Sequencer on

Bit	Description
31:30	**Panel Control port select:** These bits define to which port the embedded panel is connected. This is used for automatic control of the panel power. If the selected port is disabled or if the port is not on pipe-B, then, the power sequence will not allow a panel power up. 00 = Reserved 01 = Panel is connected to the embedded DisplayPort B 10 = Panel is connected to the embedded DisplayPort C 11 = Reserved The selection of non-existent ports are not allowed. This programming will disable panel power sequencing logic.
29	Reserved
28:16	**Power up delay:** Programmable value of panel power sequencing delay during panel power up. This provides the time delay for the T1+T2 time sequence. The time unit used is the 100us timer.
15:13	Reserved
12:0	**Power on to Backlight enable delay:** Programmable value of panel power sequencing delay during panel power up. This provides the time delay for the T5 (T3 for DisplayPort) time sequence. The time unit used is the 100us timer.

PipeB_PP_OFF_DELAYS—PipeB Panel Power off Sequencing Delays ()

Address offset:6130Ch

Default Value: 00000000h

Normal Access: Read/Write

Description: PP Delay Off values (dplrreg.v – DPLRppoff_sd)Write Protect by Panel Power Sequencer on Mobile productsBit	Description
31:29	Reserved
28:16	**Power Down delay:** Programmable value of panel power sequencing delay during power up. This provides the time delay for the T3 (T5 for DisplayPort) time sequence. The time unit used is the 100us timer.
15:13	Reserved
12:0	**Power Backlight off to power down delay:** Programmable value of panel power sequencing delay during power down. This provides the time delay for the Tx (T4 for DisplayPort) time sequence. The time unit used is the 100us timer.

PipeB_PP_DIVISOR—PipeB Panel Power Cycle Delay and Reference Divisor ()

Address offset:61310h

Default Value: 00270F04h

Normal Access: Read/Write

Description: PP Divisor (dplrreg.v – DPLRrefdiv_pp_cd)
Write Protect by Panel Power Sequencer on Mobile Products

This register selects the reference divisor and controls how long the panel must remain in a power off condition once powered down. This has a default value that allows a timer to initiate directly after device reset. If the panel limits how fast we may sequence from up to down to up again. Typically this is .5-1.5 sec. But limited to 400ms in the SPWG specification. This register forces the panel to stay off for a programmed duration. Special care is needed around reset and D3 cold situations to conform to power cycle delay specifications.

Bit	Description
31:8	**Reference divider:** This field provides the value of the divider used for the creation of the panel timer reference clock. The output of the divider is used as the fastest of the three time bases (100us) for all other timers. The other time bases are divided from this frequency. The value of zero should not be used. When it is desired to divide by N, the actual value to be programmed is (N/2)-1. The value should be (100*RefinMHz/2)-1. The default value assumes the default value

	for the display core clock. The following are examples for various memory speeds. **Display Core FrequencyValue of Field** 233MHz 2D81h 200MHz 270Fh 133MHz19F9h
7:5	Reserved
4:0	**Power Cycle Delay:** Programmable value of time panel must remain in a powered down state after powering down. For devices coming out of reset, the default values will define how much time must pass before a power on sequence can be started. This field uses the .1 S time base unit from the divider. If the panel power on sequence is attempted during this delay, the power on sequence will commence once the power cycle delay is complete. Writing a value of 0 selects no delay or is used to abort the delay if it is active. During the initial power up reset, a D3 cold power cycle, or a user instigated system reset, the timer will be set to the default value and the count down will begin after the de-assertion of reset. Writing this field to a zero while the count is active will abort this portion of the sequence. This corresponds to the T4 of the SPWG specification. Note: Even if the panel is not enabled, the T4 count happens after reset. This register needs to be programmed to a "+1" value. For instance for meeting the SPWG specification of 400mS, program 5 to achieve at least 400mS delay prior to powerup.

Panel Fitting Registers

PFIT_CONTROL—Panel Fitting Controls

Address offset:61230h

Default Value: 20000000h

Normal Access: Read/Write

The source input pixels are upscaled or downscaled (maximum 12.5%) to fit the selected pipe destination size.

Bit	Description
31	**Panel Fitting Enabled:** Disables the panel fitting function by forcing pixels to bypass. Panel fitting must be disabled when running VGA native modes or interlaced modes on the same pipe. Panel fitting should be enabled or disabled before the pipe is enabled. 0 = Bypass the panel fitting (1:1 ratio)1 = Enable panel fitting (Ratios include 1:1)
30:29	**Pipe Select:** Indicates the pipe attached to the panel fitter

	00 = Panel fitter is attached to Display Pipe A. 01 = Panel fitter is attached to Display Pipe B. **This is the default after reset**. 10 = Reserved for pipe C 11 = Reserved for pipe D
28:26	Scaling Mode 000 = Auto-scale (source and destination should have the same aspect ratios)001 = Programmed scaling: Values in register 61234h will be used for horizontal and vertical scaling factors (This is defeatured in functional mode)010 = Pillarbox (example: 4:3 to 16:9 auto conversion) use only when destination has wider aspect ratio than source 011 = Letterbox (example: 16:9 to 4:3 auto conversion) use only when destination has taller aspect ratio than source 1xx = Reserved
25:24	**Filter Coefficient Select:** Selects the set of predefined filter coefficients to use for panel fitting 00 = Fuzzy filtering01 = Crisp edge enhancing filtering10 = Median between fuzzy and crisp filtering 11 = Reserved
23	**Reserved**
22	**Reserved**
21:19	**Reserved**
18:5	Reserved
4	Reserved:) write as zero
3	Reserved
2:0	Reserved

PFIT_PGM_RATIOS—Programmed Panel Fitting Ratios

Address offset:61234h

Default Value: 00000000h

Normal Access: Read/Write

When programmed scaling mode (Panel Fitting Controls 28:26 = "001") is selected, this determines the vertical and horizontal ratios used for panel fitting scaling. The values should be based on the source sizes and active sizes programmed into the pipe timing registers. The values written into the register

should be rounded to the proper number of bits for the best precision. The value programmed should be [(source size register value +1) / (active size register value + 1)]

When programmed scaling mode is not selected, read back of this register gives the auto-generated vertical and horizontal scaling ratios used for panel fitting scaling. Register writes will be ignored. The ratios are calculated each VBLANK. When in HiRes modes, the values are based on the source sizes and active sizes programmed into the pipe timing registers. When in VGA modes it is determined by the VGA source sizes calculated by the VGA and active sizes from the pipe timing registers. VGA source sizes may have invalid values due to mode change transitions. These will eventually be correct when the mode change is complete. The value read is internally generated [(source size register value +1) / (active size register value + 1)]

For each register field the MSB is the 1 bit integer value and the lower 12 bits are the fractional value. A value of 1.0 will indicate 1:1 scaling. A value greater than 1.0 will indicate downscaling. A value less than 1.0 will indicate upscaling. The vertical and horizontal ratios are usually identical, except for when source and active aspect ratios differ.

Bit	Description
31:29	**Reserved** – Reads as zeros
28:16	**Panel fitting vertical ratio:** Vertical scaling ratio for panel fitting.
15:13	**Reserved** – Reads as zeros
12:0	**Panel fitting horizontal ratio:** Horizontal scaling ratio for panel fitting.

Backlight Control and Modulation Histogram Registers

PipeA_BLC_PWM_CLT2—PipeA Backlight PWM Control Register 2

Address offset:61250h

Default Value: 00000000h

Normal Access: Read/Write

Double Buffered:No

Bit	Description
31	**PWM Enable:** This bit enables the PWM counter logic 0 = PWM disabled (drives 0 always) 1 = PWM enabled
30	Reserved: MBZ

29	Reserved
28	**Backlight Polarity.** This field controls the polarity of the PWM signal. 0 = Active High1 = Active Low
27	Reserved: MBZ
26	Phase-In Interrupt Status: This bit will be set by hardware when a Phase-In interrupt has occurred. Software will clear this bit by writing a '1', which will reset the interrupt generation. AccessType: One to Clear
25	**Phase In Enable:** Setting this bit enables a PWM phase in based on the programming of the Phase In registers below. This bit clears itself when the phase in is completed.
24	**Phase In Interrupt Enable:** Setting this bit enables an interrupt to be generated when the PWM phase in is completed.
23:16	**Phase In time base:** This field determines the number of VBLANK events that pass before one increment occurs. 0 = invalid 1 = 1 vblank 2 = 2 vblanks etc.
15:8	**Phase In Count:** This field determines the number of increment events in this phase in. Writes to this register should only occur when hardware-phase-ins are disabled. Reads to this register can occur any time, where the value in this field indicates the number of increment events remaining to fully apply a phase-in request as hardware automatically decrements this value. A value of 0 is invalid. In order to write the same value to this field for the second time, one must write a dummy value to this field, for example, '0', before writing the real value for the second time.
7:0	**Phase In Increment:** This field indicates the amount to adjust the PWM duty cycle register on each increment event. This is a two's complement number.

PipeA_BLC_PWM_CTL—PipeA Backlight PWM Control Register

Address offset:61254hDefault Value: 00000000hNormal Access: Read/Write

Bit	Description
31:16	**Backlight Modulation Frequency.** This field determines the number of time base events in total for a complete cycle of modulated backlight control. This field is normally set once during initialization based on the frequency of the clock that is being used and the desired PWM frequency. This value represents the period of the PWM stream in display core clocks multiplied by 128, or 25MHz S0IX clocks multipled by 16.
15:0	**Backlight Duty Cycle.** This field determines the number of time base events for the active portion of the PWM backlight control. This should never be larger than the frequency field. A value of zero will turn the backlight off. A value equal to the backlight modulation frequency field will be full on. This field gets updated when it is desired to change the intensity of the backlight, it will take affect at the end of the current PWM cycle. This value represents the active time of the PWM stream in display core clock periods multiplied by 128 or 25MHz S0IX clocks multipled by 16.

PipeB_BLC_PWM_CLT2—PipeB Backlight PWM Control Register 2

Address offset:61350h

Default Value: 00000000h

Normal Access: Read/Write

Double Buffered:No

Bit	Description
31	**PWM Enable:** This bit enables the PWM counter logic 0 = PWM disabled (drives 0 always) 1 = PWM enabled
30	Reserved MBZ
29	Reserved
28	**Backlight Polarity.** This field controls the polarity of the PWM signal. 0 = Active High1 = Active Low
27	Reserved: MBZ

26	Phase-In Interrupt Status: This bit will be set by hardware when a Phase-In interrupt has occurred. Software will clear this bit by writing a '1', which will reset the interrupt generation. AccessType: One to Clear
25	**Phase In Enable:** Setting this bit enables a PWM phase in based on the programming of the Phase In registers below. This bit clears itself when the phase in is completed.
24	**Phase In Interrupt Enable:** Setting this bit enables an interrupt to be generated when the PWM phase in is completed.
23:16	**Phase In time base:** This field determines the number of VBLANK events that pass before one increment occurs. 0 = invalid 1 = 1 vblank 2 = 2 vblanks etc.
15:8	**Phase In Count:** This field determines the number of increment events in this phase in. Writes to this register should only occur when hardware-phase-ins are disabled. Reads to this register can occur any time, where the value in this field indicates the number of increment events remaining to fully apply a phase-in request as hardware automatically decrements this value. A value of 0 is invalid. In order to write the same value to this field for the second time, one must write a dummy value to this field, for example, '0', before writing the real value for the second time.
7:0	**Phase In Increment:** This field indicates the amount to adjust the PWM duty cycle register on each increment event. This is a two's complement number.

PipeB_BLC_PWM_CTL—PipeB Backlight PWM Control Register

Address offset:61354h

Default Value: 00000000h

Normal Access: Read/Write

Bit	Description
31:16	**Backlight Modulation Frequency.** This field determines the number of time base events in total for a complete cycle of modulated backlight control. This field is normally set once during

	initialization based on the frequency of the clock that is being used and the desired PWM frequency. This value represents the period of the PWM stream in display core clocks multiplied by 128 or 25MHz S0IX clocks multipled by 16.
15:0	**Backlight Duty Cycle.** This field determines the number of time base events for the active portion of the PWM backlight control. This should never be larger than the frequency field. A value of zero will turn the backlight off. A value equal to the backlight modulation frequency field will be full on. This field gets updated when it is desired to change the intensity of the backlight, it will take affect at the end of the current PWM cycle. This value represents the active time of the PWM stream in display core clock periods multiplied by 128 or 25MHz S0IX clocks multipled by 16.

PipeB Histogram Threshold Guardband Register

Address offset:61368h

Default Value: 00000000h

Normal Access: Read/Write

Double buffer: Yes

Bit	Description
31	Histogram Interrupt enable: 0 = Disabled 1 = Enabled. This generates a histogram interrupt once a Histogram event occurs.
30	Histogram Event status (Read Only): When a Histogram event has occured, this will get set by the hardware. For any more Histogram events to occur, the software needs to clear this bit by writing a '1'. The default state for this bit is '0'. 0 = Histogram event has not occurred.1 = Histogram event has occurred. AccessType: Read Only
29:22	**Guardband Interrupt Delay:** An interrupt is generated after this many consecutive frames of the guardband threshold being surpassed. This value is double buffered on start of vblank. A value of 0 is invalid.
21:0	**Threshold Guardband:** This value is used to determine the guardband for the threshold interrupt generation. This single value is used for all the segments. This value is double buffered on start of vblank

HD Audio Registers (62000h–62FFFh)

These registers are memory mapped and accessible through normal 32 bit, 16 bit, or 8 bit accesses.

Audio Configuration

The video driver configures the audio operation through the following procedure.

1. Read the Capabilities Written bit in the Audio Configuration register at address offset 0x62000. If this bit is a 1, the video driver does not need to write the audio configuration. If this bit is a 0, continue this procedure to write the audio configuration.
2. Read the EDID and directly write the EDID data into the audio EDID register region at address offset 0x62080
3. Parse the EDID information to determine the monitor's audio capabilities. Then configure the hardware for those capabilities by setting the capability registers.
   - Write the audio capabilities to the Audio PCM Sizes and Rates register at address offset 0x62044
   - Write the compressed audio supported formats to the Audio Stream Formats register at address offset 0x62048
   - Set the presence detect bit to 1 in the Audio Pin Sense register at address offset 0x62074
4. Set the Capabilities Written bit in the Audio Configuration register to 1. This indicates that the hardware can begin processing audio data using the current settings.
5. For DP audio configuration, cdclk frequency shall be set to meet the following requirements:
6.

DP Link Frequency (MHz)	Cdclk frequency (MHz)
270	320 or higher
162	200 or higher

AUD_CONFIG_A—Audio Configuration – Pipe A

AUD_CONFIG_A—Audio Configuration – Pipe A	
Register Type:	MMIO
Address Offset:	62000h
Project:	All

Default Value:	00000000h
Access:	R/W
Size (in bits):	32

This register configures the audio output.

Bit	Description
31:30	Reserved Project: All Format:
29	N_value_Index Project: All Default Value: 0b

Value	Name	Description	Project
0b	HDMI	N value read on bits 27:20 and 15:4 reflects HDMI N value. Bits 27:20 and 15:4 are is programmable to any N value - default h7FA6.	All
1b	DP	N value read on bits 27:20 and 15:4 reflects DP N value. Set this bit to 1 before programming N value register. When this is set to 1, 27:20 and 15:4 will reflect the current N value – default h8000.	All

28	Reserved
27:20	Reserved
19:16	Pixel_Clock(HDMI) Project: All Default Value: 0b This is the target frequency of the CEA/HDMI video mdoe to which the audio stream is added. This value is used for generating N_CTS packets. This refers to only HDMI Pixel clock and does not refer to DP Link clock. DP Link clock does not require this programming.

	Note: The Pipe on which audio is attached must be disabled when changing this field.

Value	Name	Description	Project
0000b	25.2 / 1.001 MHz	25.2 / 1.001 MHz	All
0001b	25.2 MHz	25.2 MHz Program this value for pixel clocks not listed in this field	All
0010b	27 MHz	27 MHz	All
0011b	27 * 1.001 MHz	27 * 1.001 MHz	All
0100b	54 MHz	54 MHz	All
0101b	54 * 1.001 MHz	54 * 1.001 MHz	All
0110b	74.25 / 1.001 MHz	74.25 / 1.001 MHz	All
0111b	74.25 MHz	74.25 MHz	All
1000b	148.5 / 1.001 MHz	148.5 / 1.001 MHz	All
1001b	148.5 MHz	148.5 MHz	All
Others	Reserved	Reserved	All

15:4	Reserved
3	Reserved
2:0	Reserved Project: All Format:

AUD_CONFIG_B—Audio Configuration – Pipe B

AUD_CONFIG_B—Audio Configuration – Pipe B

Register Type:	MMIO
Address Offset:	62100h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

This register configures the audio output.

Bit	Description
31:30	Reserved Project: All Format:
29	N_value_Index Project: All Default Value: 0b

Value	Name	Description	Project
0b	HDMI	N value read on bits 27:20 and 15:4 reflects HDMI N value. Bits 27:20 and 15:4 are is programmable to any N value - default h7FA6.	All
1b	DP	N value read on bits 27:20 and 15:4 reflects DP N value. Set this bit to 1 before programming N value register. When this is set to 1, 27:20 and 15:4 will reflect the current N value – default h8000.	All

28	Reserved
27:20	Reserved
19:16	Pixel_Clock(HDMI) Project: All

Default Value: 0b

See Pipe A description.

Value	Name	Description	Project
0000b	25.2 / 1.001 MHz	25.2 / 1.001 MHz	All
0001b	25.2 MHz	25.2 MHz Program this value for pixel clocks not listed in this field	All
0010b	27 MHz	27 MHz	All
0011b	27 * 1.001 MHz	27 * 1.001 MHz	All
0100b	54 MHz	54 MHz	All
0101b	54 * 1.001 MHz	54 * 1.001 MHz	All
0110b	74.25 / 1.001 MHz	74.25 / 1.001 MHz	All
0111b	74.25 MHz	74.25 MHz	All
1000b	148.5 / 1.001 MHz	148.5 / 1.001 MHz	All
1001b	148.5 MHz	148.5 MHz	All
others	Reserved	Reserved	All

15:4

Lower_N_value(testmode) Project: All Security: Test

See Pipe A description

3

Disable_NCTS Project: All

See Pipe A description

2:0

Reserved Project: All Format:

AUD_MISC_CTRL_A—Audio MISC Control for Pipe A

AUD_MISC_CTRL_A—Audio MISC Control for Pipe A	
Register Type:	MMIO
Address Offset:	62010h
Project:	All
Default Value:	00000044h
Access:	Read/Write
Size (in bits):	32

Bit	Description
31:9	Reserved Project: All Format: MBZ
8	**Reserved**
7:4	Output_Delay Project: All Default Value: 0100b The number of samples between when the sample is received from the HD Audio link and when it appears as an analog signal at the pin.
3	Reserved Project: All Format: MBZ
2	Sample_Fabrication_EN_bit Project: All Access: R/W Default Value: 1b This bit indicates whether internal fabrication of audio samples is enabled during a link underrun.

Value	Name	Description	Project

	0b	Disable	Audio fabrication disabled	All
	1b	Enable	Audio fabrication enabled	All

1 — Pro_Allowed

Project: All

Access: R/W

Default Value: 0b

By default, the audio device is configured to consumer mode and does not allow the mode to be changed to professional mode by an HD Audio verb. When Pro is allowed by setting this configuration bit, the HD Audio codec allows a verb to set the device into professional mode.

Note: Setting this configuration bit does not change the default Pro bit value to be 1. Pro must be set to 1 through the normal process, using a verb.

Value	Name	Description	Project
0b	Consumer	Consumer use only	All
1b	Professional	Professional use allowed	All

0 — Reserved Project: All Format: MBZ

AUD_MISC_CTRL_B—Audio MISC Control for Pipe B

AUD_MISC_CTRL_B—Audio MISC Control for Pipe B	
Register Type:	MMIO
Address Offset:	62110h
Project:	All
Default Value:	00000044h
Access:	Read/Write
Size (in bits):	32

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>31:9</td><td>Reserved Project: All Format: MBZ</td></tr>
<tr><td>8</td><td>Reserved</td></tr>
<tr><td>7:4</td><td>Output_Delay Project: All Default Value: 0100b
See Pipe A description.</td></tr>
<tr><td>3</td><td>Reserved Project: All Format: MBZ</td></tr>
<tr><td>2</td><td>Sample_Fabrication_EN_bit
Project: All
Access: R/W
Default Value: 1b
See Pipe A description.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr>
<tr><td>0b</td><td>Disable</td><td>Audio fabrication disabled</td><td>All</td></tr>
<tr><td>1b</td><td>Enable</td><td>Audio fabrication enabled</td><td>All</td></tr>
</table></td></tr>
<tr><td>1</td><td>Pro_Allowed
Project: All
Access: R/W
Default Value: 0b
See Pipe A description.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr>
<tr><td>0b</td><td>Consumer</td><td>Consumer use only</td><td>All</td></tr>
<tr><td>1b</td><td>Professional</td><td>Professional use allowed</td><td>All</td></tr>
</table></td></tr>
</table>

0	Reserved Project: All Format: MBZ

AUD_VID_DID—Audio Vendor ID / Device ID

AUD_VID_DID—Audio Vendor ID / Device ID	
Register Type:	MMIO
Address Offset:	62020h
Project:	All
Default Value:	80862882h
Access:	Read Only
Size (in bits):	32

These values are returned from the device as the Vendor ID/ Device ID response to a Get Root Node command.

Bit	Description
31:16	Vendor_ID Project: All Format: U16 Used to identify the codec within the PnP system. This field is hardwired within the device. Value = 0x8086
15:0	Device_ID Project: All Format: U16 Constant used to identify the codec within the PnP system. This field is set by the device hardware. Value = 0x2882 [Valleyview2]

AUD_RID—Audio Revision ID

AUD_RID—Audio Revision ID	
Register Type:	MMIO
Address Offset:	62024h
Project:	All
Default Value:	00100000h
Access:	Read Only
Size (in bits):	32

These values are returned from the device as the Revision ID response to a Get Root Node command.

Bit	Description
31:24	Reserved Project: All Format:
23:20	Major_Revision Project: All Default Value: 0001b The major revision number (left of the decimal) of the HD Audio Spec to which the codec is fully compliant. This field is hardwired within the device. Value = 0x1
19:16	Minor_Revision Project: All The minor revision number (rights of the decimal) or “dot number” of the HD Audio Spec to which the codec is fully compliant. This field is hardwired within the device. Value = 0x0
15:8	Revision_ID Project: All The vendor’s revision number for this given Device ID. This field is hardwired within the device. Value = 0x0
7:0	Stepping_ID Project: All

	An optional vendor stepping number within the given Revision ID. This field is hardwired within the device. Value = 0x0	

AUD_PWRST—Audio Power State (Function Group, Convertor, Pin Widget)

Audio Power State Format	
Project:	All
Bit	Description
1:0	Power_State Project: All Default Value: 11b D3

Value	Name	Description	Project
00b	D0	D0	All
01b,10b	Unsupported	Unsupported	All
11b	D3	D3	All

AUD_PINW_CONNLNG_LIST—Audio Connection List

AUD_PINW_CONNLNG_LIST—Audio Connection List	
Register Type:	MMIO
Address Offset:	620A8h
Project:	All
Default Value:	00030202h
Access:	Read Only

Size (in bits):	32
These values are returned from the device as the Connection List Length response to a Get Pin Widget command.	

Bit	Description
31:24	Reserved Project: All Format:
23:8	Connection_List_Entry Project: All Default Value: 0000001100000010b Connection to Convertor Widget Node 0x0302
7	Long_Form Project: All Default Value: 0b This bit indicates whether the items in the connection list are 'long form' or 'short form'. This bit is hardwired to 0 (items in connection list are short form)
6:0	Connection_List_Length Project: All Default Value: 02h This field indicates the number of items in the connection list. If this field is 2, there is only one hardwired input possible, which is read from the Connection List, and there is no Connection Select Control.

AUD_PINW_CONNLNG_SEL—Audio Connection Select

AUD_PINW_CONNLNG_SEL—Audio Connection Select	
Register Type:	MMIO
Address Offset:	620ACh
Project:	All
Default Value:	00000000h
Access:	Read Only
Size (in bits):	32
These values are returned from the device as the Connection List Length response to a Get Pin Widget	

command.	
Bit	Description
31:24	Reserved Project: All Format:
23:16	Connection_select_Control_D Project: All Format: Connection Index Currently Set [Default 0x00], Port D Widget is set to 0x00
15:8	Connection_select_Control_C Project: All Format: Connection Index Currently Set [Default 0x00], Port C Widget is set to 0x00
7:0	Connection_select_Control_B Project: All Format: Connection Index Currently Set [Default 0x00], Port B Widget is set to 0x00

AUD_CNTL_ST_A—Audio Control State Register – Pipe A

AUD_CNTL_ST_A—Audio Control State Register – Pipe A	
Register Type:	MMIO
Address Offset:	620B4h
Project:	All
Default Value:	00005400h
Access:	R/W
Size (in bits):	32
Bit	Description
31	Reserved Project: All Format: MBZ
30:29	DIP_Port_Select Project: All

AccessType: Read Only

Default Value: 00b

This read-only bit reflects which port is used to transmit the DIP data. This can only change when DIP is disabled. If one or more audio-related DIP packets is enabled and audio is enabled on a digital port, these bits will reflect the digital port to which audio is directed.

Value	Name	Description	Project
00b	Reserved	Reserved	All
01b	Digital Port B	Digital Port B	All
10b	Digital Port C	Digital Port C	All
11b	Digital Port D	Digital Port D	All

28:25

Reserved Project: All Format: MBZ

24:21

DIP_type_enable_status

Project: All

AccessType: Read Only

Default Value: 0000b

These bits reflect the DIP types enabled. It can be updated while the port is enabled. Within 2 vblank periods, the DIP is guaranteed to have been transmitted. Disabling a DIP type results in setting the contents of that DIP buffer to zero. A reserved setting reflects a disabled DIP.

Value	Name	Description	Project
XXX0b	Disable	Audio DIP disabled	All
XXX1b	Enable	Audio DIP enabled	All
XX0Xb	Disable	Generic 1 (ACP) DIP disabled	All

	XX1Xb	Enable	Generic 1 (ACP) DIP enabled	All
	X0XXb	Disable	Generic 2 DIP disabled	All
	X1XXb	Enable	Generic 2 DIP enabled, can be used by ISRC1 or ISRC2	All
	1XXXb	Reserved	Reserved	All

20:18

DIP_buffer_index

Project: All

Default Value: 0000b

This field is used during read of different DIPs, and during read or write of ELD data. These bits are used as an index to their respective DIP or ELD buffers. When the index is not valid, the contents of the DIP will return all 0's.

Value	Name	Description	Project
000b	Audio	Audio DIP (31 bytes of address space, 31 bytes of data)	All
001b	Gen 1	Generic 1 (ACP) Data Island Packet (31 bytes of address space, 31 bytes of data)	All
010b	Gen 2	Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data)	All
011b	Gen 3	Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data)	All
1XXb	Reserved	Reserved	All

17:16

DIP_transmission_frequency

Project: All

AccessType: Read Only

Default Value: 00b

These bits reflect the frequency of DIP transmission for the DIP buffer type designated in

bits 20:18. When writing DIP data, this value is also latched when the first DW of the DIP is written.

When read, this value reflects the DIP transmission frequency for the DIP buffer designated in bits 20:18.

Value	Name	Description	Project
00b	Disable	Disabled	All
01b	Reserved	Reserved	All
10b	Send Once	Send Once	All
11b	Best Effort	Best effort (Send at least every other vsync)	All

15	Reserved Project: All Format: MBZ
14:10	ELD_buffer_size Project: All AccessType: Read only 10101 = This field reflects the size of the ELD buffer in DWORDs (84 Bytes of ELD)
9:5	ELD_access_address Project: All Selects the DWORD address for access to the ELD buffer (84 bytes). The value wraps back to zero when incremented past the max addressing value 0x1F. This field change takes effect immediately after being written. The read value indicates the current access address.
4	ELD_ACK Project: All AccessType: Read Only Acknowledgement from the audio driver that ELD read has been completed
3:0	DIP_RAM_access_address Project: All AccessType: Read Only

	Selects the DWORD address for access to the DIP buffers. The value wraps back to zero when it incremented past the max addressing value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.

AUD_CNTL_ST_B—Audio Control State Register – Pipe B

AUD_CNTL_ST_B—Audio Control State Register – Pipe B	
Register Type:	MMIO
Address Offset:	621B4h
Project:	All
Default Value:	00005400h
Access:	R/W
Size (in bits):	32

Bit	Description
31	Reserved Project: All Format: MBZ
30:29	DIP_Port_Select Project: All AccessType: Read Only Default Value: 00b See Pipe A description.

Value	Name	Description	Project
00b	Reserved	Reserved	All
01b	Digital Port B	Digital Port B	All
10b	Digital Port C	Digital Port C	All

	11b	Digital Port D	Digital Port D	All

28:25 Reserved Project: All Format: MBZ

24:21 DIP_type_enable_status

Project: All

AccessType: Read Only

Default Value: 0000b

See Pipe A description.

Value	Name	Description	Project
XXX0b	Disable	Audio DIP disabled (Default)	All
XXX1b	Enable	Audio DIP enabled	All
XX0Xb	Disable	Generic 1 (ACP) DIP disabled	All
XX1Xb	Enable	Generic 1 (ACP) DIP enabled	All
X0XXb	Disable	Generic 2 DIP disabled	All
X1XXb	Enable	Generic 2 DIP enabled, can be used by ISRC1 or ISRC2	All
1XXXb	Reserved	Reserved	All

20:18 DIP_buffer_index

Project: All

Default Value: 000b

See Pipe A description.

Value	Name	Description	Project
000b	Audio	Audio DIP (31 bytes of address space, 31 bytes of data)	All

	001b	Gen 1	Generic 1 (ACP) Data Island Packet (31 bytes of address space, 11 bytes of data)	All
	010b	Gen 2	Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data)	All
	011b	Gen 3	Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data)	All
	1XXb	Reserved	Reserved	All

17:16 DIP_transmission_frequency

Project: All

AccessType: Read Only

Default Value: 00b

See Pipe A description

Value	Name	Description	Project
00b	Disable	Disabled	All
01b	Reserved	Reserved	All
10b	Send Once	Send Once	All
11b	Best Effort	Best effort (Send at least every other vsync)	All

15 Reserved Project: All Format: MBZ

14:10 ELD_buffer_size Project: All AccessType: Read Only

10101 = This field reflects the size of the ELD buffer in DWORDs (84 Bytes of ELD)

9:5 ELD_access_address Project: All

See Pipe A description.

4	ELD_ACK Project: All AccessType: Read Only See Pipe A description.
3:0	DIP_RAM_access_address Project: All AccessType: Read only See Pipe A description.

AUD_CNTL_ST2— Audio Control State 2

AUD_CNTL_ST2— Audio Control State 2	
Register Type:	MMIO
Address Offset:	620C0h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

This register is used for handshaking between the audio and video drivers for interrupt management. For each port, ELD readiness is sent by the display software to the audio software via an unsolicited response when the ELD ready bit is set. Display software sets these bits as part of enabling the respective audio-enabled digital display port.

Bit	Description
31:10	Reserved Project: All Format:
9	Reserved
8	ELD_validD

<table>
<tr><td></td><td>
Project: All

Default Value: 0b

This R/W bit reflects the state of the ELD data written to the ELD RAM. After writing the ELD data, the video software must set this bit to 1 to indicate that the ELD data is valid. At audio codec initialization, or on a hotplug event, this bit is set to 0 by the video software. This bit is reflected in the audio pin complex widget as the ELD valid status bit.
<table>
<tr><td>Value</td><td>Name</td><td>Description</td><td>Project</td></tr>
<tr><td>0b</td><td>Invalid</td><td>ELD data invalid (default, when writing ELD data, set 0 by software)</td><td>All</td></tr>
<tr><td>1b</td><td>Valid</td><td>ELD data valid (Set by video software only)</td><td>All</td></tr>
</table>
</td></tr>
<tr><td>7:6</td><td>Reserved</td></tr>
<tr><td>5</td><td>Reserved</td></tr>
<tr><td>4</td><td>
ELD_validC

Project: All

Default Value: 0b

See ELD_validD descripion.
<table>
<tr><td>Value</td><td>Name</td><td>Description</td><td>Project</td></tr>
<tr><td>0b</td><td>Invalid</td><td>ELD data invalid (default, when writing ELD data, set 0 by software)</td><td>All</td></tr>
<tr><td>1b</td><td>Valid</td><td>ELD data valid (Set by video software only)</td><td>All</td></tr>
</table>
</td></tr>
<tr><td>3:2</td><td>Reserved</td></tr>
<tr><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>
ELD_validB

Project: All
</td></tr>
</table>

Default Value: 0b

See ELD_validD descripion.

Value	Name	Description	Project
0b	Invalid	ELD data invalid (default, when writing ELD data, set 0 by software)	All
1b	Valid	ELD data valid (Set by video software only)	All

AUD_HDMIW_HDMIEDID_A—HDMI Data EDID Block – Pipe A

AUD_HDMIW_HDMIEDID_A—HDMI Data EDID Block – Pipe A

Register Type:	MMIO
Address Offset:	62050h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

These registers contain the HDMI data block from the EDID. The graphics driver reads the EDID and writes the structure to these registers. The vendor specific data block may be longer than 8 bytes, but the driver must not write more than 48 bytes to the buffer. The EDID format is Version 3 within the CEA-861B specification. The HDMI Vendor Specific Data Block is described in version 1.1 of the HDMI specification.

These values are returned from the device as the HDMI Vendor Specific Data Block response to a Get HDMI Widget command.

Writing sequence:

- Video software sets ELD invalid, and sets the ELD access address to 0, or to the desired DWORD to be written.
- Video software writes ELD data 1 DWORD at a time. The ELD access address autoincrements with each DWORD write, wrapping around to address 0 when the max buffer address size of 0xF has been reached. Please note that software must write an entire DWORD at a time.
- Please note that the audio driver checks the valid bit with each byte read of the ELD. This

	means that the video driver can unilaterally write ELD irrespective of audio driver ELD read status. Reading sequence: • Video software sets the ELD access address to 0, or to the desired DWORD to be read. • Video software reads ELD data 1 DWORD at a time. The ELD access address autoincrements with each DWORD read, wrapping around to address 0 when the max buffer address size of 0xF has been reached.
Bit	Description
31:0	EDID_HDMI_Data_Block Project: All Format: Please note that the contents of this buffer are not cleared when ELD is disabled. The contents of this buffer are cleared during gfx reset

AUD_HDMIW_HDMIEDID_B—HDMI Data EDID Block – Pipe B

AUD_HDMIW_HDMIEDID_B—HDMI Data EDID Block – Pipe B	
Register Type:	MMIO
Address Offset:	62150h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32
See Pipe A description.	
Bit	Description
31:0	EDID_HDMI_Data_Block Project: All Format: See Pipe A description

AUD_HDMIW_INFOFR_A—Audio Widget Data Island Packet – Pipe A

AUD_HDMIW_INFOFR_A—Audio Widget Data Island Packet – Pipe A	
Register Type:	MMIO
Address Offset:	62054h
Project:	All
Default Value:	00000000h
Access:	Read Only
Size (in bits):	32

When the IF type or dword index is not valid, the contents of the DIP will return all 0's.

These values are programmed by the audio driver in an HDMI Widget Set command. They are returned one byte at a time from the device on the HD audio bus as the HDMI DIP response to a Get HDMI Widget command. To fetch a specific byte, the audio driver should send an HDMI Widget HDMI DIP Index Pointer Set command to set the index, then fetch the indexed byte using the HDMI DIP get.

Bit	Description
31:0	Data_Island_Packet_Data Project: All Format: This reflects the contents of the DIP indexed by the DIP access address. The contents of this buffer are cleared during function reset or HD audio link reset.

AUD_HDMIW_INFOFR_B—Audio Widget Data Island Packet – Pipe B

AUD_HDMIW_INFOFR_B—Audio Widget Data Island Packet – Pipe B	
Register Type:	MMIO
Address Offset:	62154h
Project:	All
Default Value:	00000000h
Access:	Read Only

Size (in bits):	32
See Pipe A description.	
Bit	Description
31:0	Data_Island_Packet_Data Project: All Format: See Pipe A description.

LPE Audio Registers (65000h–65FFFh)

Audio Configuration Sequence

DP/HDMI audio open:

1. reset the audio function in LPE_AUD_STATUS (not needed if out of reset)
2. HDMI/DP driver read EDID through I2C, include the audio and video latencies, compute the relevant delay
3. write AUD_CONFIG register, except AudioEnable (sets User, Validity, sample flat, block begin, number of channels, format, layout)
4. program ChannelStatus bits
5. unmask the relevant interrupts in PORT_HOTPLUG_EN and PORT_HOTPLUG_STAT
6. get frame rate from video driver
7. program N, CTS (or Maud/Naud) based on information provided by the hardware HAS.
8. program the FIFO threshold in AUD_BUF_CONFIG
9. Program underrun bit (silent stream) if needed (recommended).
10. program channel swaps if needed
11. write Audio Infoframe in local memory (all the 28 bytes need to be written, zero-out reserved bits/bytes)
12. Program 62F38[0] = 1 to enable MMIO register programming
13. Program 62F20[1] = 0 to disable AMP_MUTE_Status for port B or 62F28[1] = 0 MUTE status for port C
14. Enable LPE bit
15. Start sending audio by programming A/B/C/D buffers

Note: if silent stream is active LPE audio unit will send silent audio stream to the monitor to keep the its PLL is synchronize so when new application buffers coming there will start executing from that buffer

1. For DP audio configuration, cdclk frequency shall be set to meet the following requirements:

DP Link Frequency (MHz)	Cdclk frequency (MHz)
270	320 or higher
162	200 or higher

LPE Audio Registers (65000h–65FFFh)

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Note: if silent stream is active LPE audio unit will send silent audio stream to the monitor to keep the its PLL is synchronize so when new application buffers coming there will start executing from that buffer

1. For DP audio configuration, cdclk frequency shall be set to meet the following requirements:

DP Link Frequency (MHz)	Cdclk frequency (MHz)
270	320 or higher
162	200 or higher

STREAM_A_LPE_AUD_CONFIG—LPE Audio Configuration

Memory Offset Address: 65000h

Default Value: 00000280h

Normal Access: Read/Write

This register configures the HDMI audio unit

Bit	Descriptions
31:17	Reserved
16	**LPE Stream A Pause/resume** – DMA pause fetching at the boundary of buffers when this bit is set, and resume fetching when this bit is cleared. 1= DMA stop requesting more audio sample from buffer A,B,C,D after reading and depleting all data from current buffer 0= DMA resume requesting data from the next available buffer (A,B,C,D). Programming note: this bit should not be used by SW driver. When SW driver wants to pause audio, it shall invalidate the two newest allocated audio buffers. When the current audio buffers are processed, silent stream is sent automatically.
15	LPE HDMI/DP mode on stream A 1 = DP mode 0 = HDMI mode (default)
14	**Bogus sample disable for odd channel** – When number of channels in a sample is odd (3, 5, or 7) source application may pad a bogus sample to the next even number of channels. If this bit is set there is no padding in input buffer 1= No bogus sample present in buffer for odd number of channels 0= Bogus sample present in buffer for odd number of channels (default)
13	**Left alignment** When input buffer is in 32-bit container mode. If this bit is set the MSB of audio sample is aligned bit 31 of the container if this bit is clear MSB of audio sample is aligned with bit 23 of the container. 1= MSB is bit 31 of 32-bit container 0= MSB is bit 23 of 32-bit container (default)
12	**16-bit container** When this bit is set 16-bit sample is stored in 16-bit container format. When it is clear container is 32-bit for each sample regardless of valid bits (default) 1= 16-bit container 0= 32-bit container
11	**Underrun packet bit (Silent Stream enable)** Set this bit will enble HW to send valid zero-filled packet with Sample flat bit set when no sample buffer is available, NCTS packets (or Timesstamp

	packet) are sent to keep sink in sync even no audio sound will heard. 1= send underrun packets (silent stream) 0= send null packets (default) Programming note: SW driver shall always set silent stream bit. When SW driver wants to pause audio, it shall invalidate the two newest allocated audio buffers. When the current audio buffers are processed, silent stream is sent automatically.
10	User bit (U) HW will clear this bit ineach sub-frames it sends. 1= sey U bit in sub-frame 0= clear U bit in sub-frame (default)
9	Validity Bit (V) HW will set this bit in both each sub-frames it sends. 1= Set V bit in sub-frame (default) 0= clear V bit in sub-frame.
8	Sample Flat bit When set the sample flat bit will be set in all HDMI sub-packets. 1= flat bit is set for valid sample 0= flat bit is not set for valid sample (default)
7	Set Block begin for all sub-packets Controls the B bit in the header of only the first Audio Packet /frame of a 192 frame 60958 block in Layout 1 mode. This bit only applies to LPE HDMI mode. 0: The B bit will be set only for sub-packet 0 1: The B bit in the Audio sample packet header will be set for all valid sub-packets. (default)
6:4	Num audio Channels 000: 2 channels (stereo) 001: 3 channels 010: 4 channels 011: 5 channels 100: 6 channels 101: 7 channels

	110: 8 channels **Note:** When disable_bogus sample bit is clear HW will always treat odd number of channels similar to the next higher even number. Thus 3 is similar to 4, 5 to 6 and 7 to 8. This is because SW ensures that an even number of samples are packed in the audio buffers. Programming note: Bit 6 of of this field is a write only bit. When reads back, it always returns zero. Ensure to write bit 6 to 1'b1 when programming for 6/7/8 audio channels.
3:2	Format 00: L-PCM or IEC 61937 01: High Bit Rate IEC 61937 stream packet (not supported) 10: One Bit Audio Sample packet (not supported) 11: DST Audio Sample packet (not supported)
1	Layout 0: Layout 0 (2-ch) 1: Layout 1 (3-8 ch) **Note:** Layout bit doesn't matter for HBR
0	**Audio Enable :** Controls generation of N/CTS and transmission of audio sample packets. 0: Audio sample packets are not transmitted, CTS calculation/transmission is disabled 1: Audio sample packets are transmitted & CTS calculation is enabled When enable audio unit will wait until the next vertical blank period before sending out the audio packets. When disable, audio unit may continue to send audio packet until the end of current active video frame before stopping.

STREAM_A_LPE_AUD_CH_STATUS_0 – Audio Channel Status Attributes 0

Memory Offset Address: 65008h

Default Value: 00000000h

Normal Access: Read/Write

Bit	Descriptions
31:0	**Channel status register 0**. These bits are transmitted as attributes of audio packets

Each block has 192 frames so there are 192 bit slots available for transmission. But it is nly the first 40 bits of the channel status are meaningful. Software driver will program these two registers with appropriate values before enabling audio. For each block, the first 40 bits are inserted one at a time in

each frame, the remaining 152 bits are zeroed. Note that the same C bit value is transmitted for each subframe of each sub-packet.

Byte	Consumer format channel status fields							
0	Pro/con = 0	Non-audio = 0	Copyright	Emphasis			Channel status mode = 00	
	bit 0	1	2	3	4	5	6	7
1	Category code							
	bit 8	9	10	11	12	13	14	15
2	Source number				Channel number			
	bit 16	17	18	19	20	21	22	23
3	Sampling frequency				Clock accuracy			
	bit 24	25	26	27	28	29	30	31
4	Word length				(Future original sampling frequency?)			
	bit 32	33	34	35	36	37	38	39
5–23	Reserved							
	bits 40–191							

Table 2. Consumer format channel status fields.

STREAM_A_LPE_AUD_CH_STATUS_1 – Audio Channel Status Attributes 1

Memory Offset Address: 6500Ch

Default Value: 00000000h

Normal Access: Read/Write

Bit	Descriptions
31:8	Reserved
7:0	**Channel status register 1**. These bits are transmitted as attributes of audio packets. There is only 8 bits valid in this register.

STREAM_A_LPE_AUD_HDMI_CTS_DP_Maud – Audio HDMI CTS Register (DP Maud)

Memory Offset Address: 65010h

Default Value: 00000000h

Normal Access: Read/Write

Bit	Descriptions
31:25	Reserved
24	Enable CTS/M Programming 1 = Enable CTS/M programming 0 = Disable CTS/M programming
23:0	HDMI CTS Values These are bits [23:0] of programmable HDMI CTS values (or DP Maud) that is pre-calculated to achieve desired audio sample rates with a particular pixel clocks configuration. Audio function must be disabled when changing this field. Bit 24 also need to write to 1 to enable this field.

STREAM_A_LPE_AUD_HDMI_N_DP_Naud – Audio HDMI N Register (DP Naud)

Memory Offset Address: 65014h

Default Value: 00000000h

Normal Access: Read/Write

Bit	Descriptions
31:25	Reserved
24	Enable N Programming 1 = Enable N programming 0 = Disable N programming
23:0	HDMI N Values These are bits [23:0] of programmable HDMI N (or DP Naud) values that is pre-calculated to

	achieve desired audio sample rates with a particular pixel clocks configuration. Audio function must be disabled when changing this field. Bit 24 also need to write to 1 to enable this field.

STREAM_A_LPE_AUD_Buffer_config – LPE Audio buffer config

Memory Offset Address: 65020h

Default Value: 00000100h

Normal Access: Read/writeThese registers facilliates HDMI audio sample buffer management mechanism between Software and Hardware to fetch the HDMI audio samples from system memory to display controller Hardware provides 4 set of buffers A, B, C, and D. Software will program the address and the length of buffer then set the buffer valid. Hardware will start fectching the audio sample from valid buffers, update remaining bytes, and eventually clear the valid bit when it is done. If the buffer interrupt bit is set Hardware will generate an interrupt to IIR register in the graphics interface and Software will be notified. If there is more than one buffers valida at one time Hardware will srart in alphabetical order and rotate through all 4 buffers.

Bit	Descriptions
31:24	Reserved
23:16	Audio buffer delay This field specifies a delay in number of video frames that the audio controller will count off when audio enable bit is set before start transmitting audio sample.
15:11	Reserved
10:8	DMA FIFO watermark Audio unit has a 8x64 bytes fifo for pre-fetching and staging audio samples. This register provides a watermark value in SWORDs (64B). When enable and sample buffer is available audio unit will fetch samples until this FIFO is full then it waits until HDMI/DP packet assembler drains the samples to a level less or equal the watermark setting then it will start fetching the samples again. Default value is 1 cacheline (SW).
7:0	AUDF FIFO watermark Audio unit has a 96x8 bytes fifo for pre-fetching and staging audio samples. This register provides a watermark value in DWORDs. When enable and sample buffer is available audio unit will fetch samples until this FIFO occupancy is above the watermark then it waits until HDMI packet assembler drains the samples to a level less or equal the watermark setting then it will

	start fetching the samples again

STREAM_A_LPE_AUD_BUF_CH_SWP — Audio Sample Swapping

Memory Offset Address: 65024h

Default Value: 00FAC688h

Normal Access: Read only

Audio sample in input buffer can be rearranged before sending as HDMI subpacket. For each of 32-byte block of audio samples we give them an index from 0 to 7. This index then can be programmed into this register to destinate its location in a subpacket of a HDMI audio packet. Software can take advantage of this register and leave the channel rearrangement in hardware by specified a location of channel in current sample that would like to map to HDMI channel order. In case of less than 8 channel the index of the channel above the valid number will be ignored. This register is only valid for layout 1.

Bit	Descriptions
31:24	Reserved
23:21	**Sample index for Second channel of subpacket 3.** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 3 in a HDMI audio packet
20:18	**Sample index for First channel of subpacket 3.** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 1 in a HDMI audio packet
17:15	**Sample index for Second channel of subpacket 2.** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 0 in a HDMI audio packet
14:12	**Sample index for First channel of subpacket 2.** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 0 in a HDMI audio packet
11:9	**Sample index for Second channel of subpacket 1.** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 1 in a HDMI audio packet
8:6	**Sample index for First channel of subpacket 1.** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 1 in a HDMI audio packet
5:3	**Sample index for Second channel of subpacket 0.** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 0 in a HDMI audio packet
2:0	**Sample index for First channel of subpacket 0.** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 0 in a HDMI audio packet

STREAM_A_LPE_AUD_BUF_A_ADDR – Address for Audio Buffer A

Memory Offset Address: 65040h

Default Value: 00000000h

Normal Access: Read/WriteBit	Descriptions
31:6	**Buffer address**. This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	Reserved
1	**Interrupt enable.** If enable hardware will generate an interrupt when it is done fetching this buffer
0	**Buffer valid**. This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

STREAM_A_LPE_AUD_BUF_A_LENGTH — Length for Audio Buffer A

Memory Offset Address: 65044h

Default Value: 00000000h

Normal Access: Read/Write

Bit	Descriptions
31:20	Reserved
19:0	**Buffer Length** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

STREAM_A_LPE_AUD_BUF_B_ADDR – Address for Audio Buffer B

Memory Offset Address: 65048h

Default Value: 00000000h

Normal Access: Read/Write

Bit	Descriptions

31:6	**Buffer address**. This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	Reserved
1	**Interrupt enable.** If enable hardware will generate an interrupt when it is done fetching this buffer
0	**Buffer valid**. This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

STREAM_A_LPE_AUD_BUF_B_LENGTH — Length for Audio Buffer B

Memory Offset Address: 6504Ch

Default Value: 00000000h

Normal Access: Read/Write

Bit	Descriptions
31:20	Reserved
19:0	**Buffer Length** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

STREAM_A_LPE_AUD_BUF_C_ADDR – Address for Audio Buffer C

Memory Offset Address: 65050h

Default Value: 00000000h

Normal Access: Read/Write

Bit	Descriptions
31:6	**Buffer address**. This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	Reserved
1	**Interrupt enable.** If enable hardware will generate an interrupt when it is done fetching this buffer
0	**Buffer valid**. This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

STREAM_A_LPE_AUD_BUF_C_LENGTH — Length for Audio Buffer C

Memory Offset Address: 65054h

Default Value: 00000000h

Normal Access: Read/Write

Bit	Descriptions
31:20	Reserved
19:0	**Buffer Length** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

STREAM_A_LPE_AUD_BUF_D_ADDR – Address for Audio Buffer D

Memory Offset Address: 65058h

Default Value: 00000000h

Normal Access: Read/Write

Bit	Descriptions
31:6	**Buffer address**. This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	Reserved
1	**Interrupt enable.** If enable hardware will generate an interrupt when it is done fetching this buffer
0	**Buffer valid**. This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

STREAM_A_LPE_AUD_BUF_D_LENGTH — Length for Audio Buffer D

Memory Offset Address: 6505Ch

Default Value: 00000000h

Normal Access: Read/Write

Bit	Descriptions
31:20	Reserved

19:0	**Buffer Length** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

STREAM_A_LPE_AUD_CNTL_ST—LPE Audio Control State Register

Memory Offset Address: 65060h

Default Value: 00000000h

Access:Read/Write

Bit	Description
31	Reserved
30:29	Reserved
28:25	**Reserved** for later DIP type if needed: Must be 0.
24:21	**DIP type enable status (read only):** These bits reflects the DIP types enabled. It can be updated while the port is enabled. Within 2 vblank periods, the DIP is guaranteed to have been transmitted. Disabling an DIP type results in setting the contents of that DIP buffer to zero. A reserved setting reflects a disabled DIP. XXX1 = Audio DIP enable status **(Default = disabled)** XX1X = Generic 1 (ACP) DIP enable status **(Default = disabled)** X1XX = Generic 2 DIP enable status, can be used by ISRC1 or ISRC2 **(Default = disabled)** 1XXX = Reserved
20:18	**DIP buffer index (R/W):** This field is used during read or write of different DIPs, and during read or write of ELD data. These bits are used as an index to their respective DIP or ELD buffers. When the index is not valid, the contents of the DIP will return all 0's. 000 = (Default) Audio DIP (31 bytes of address space, 13 bytes of data) 001 = Generic 1 (ACP) Data Island Packet (31 bytes of address space, 11 bytes of data) 010 = Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data) 011 = Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data) 1XX = reserved
17:16	**DIP transmission frequency (R/W)** These bits reflect the frequency of DIP transmission for the

	DIP buffer type designated in bits 20:18. When writing DIP data, this value is also latched when the first DW of the DIP is written. When read, this value reflects the DIP transmission frequency for the DIP buffer designated in bits 20:18. 00 = Disabled (Default) 01 = once per frame 10 = Send once 11 = Best effort (Send at least every other vsync)
15	**CP Ready:** This **R/W** bit reflects the state of CP request from the audio unit. When an audio CP request has been serviced, it must be reset to 1 by the video software to indicate that the CP request has been serviced. 0 = CP request pending or not ready to receive requests (default) 1 = CP request ready CP_ready bit is programmable through Bit 15
14	**Reserved**
13:9	**Reserved**
8:5	**Reserved**
4	Reserved
3:0	**DIP RAM access address (R/W):** Selects the DWORD address for access to the DIP buffers. The value wraps back to zero when it incremented past the max addressing value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.

STREAM_A_LPE_AUD_HDMI_STATUS—LPE Audio Status

Memory Offset Address: 65064h

Default Value: 00000000h

Normal Access: Read/Write

Bit	Descriptions
31	**Sample Buffer Underrun:** This bit indicates an underrun in the sample buffer to HDMI controller when it needs to send. This bit is set at the last line of active video when there are no

	more sample in any valid buffers and HDMI audio unit has not satisfied number of audio samples intended in that video frame. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO. AccessType: One to Clear
30	**Reserved**
29	**LPE Audio Buffer Done Status:** This bit is set when a LPE audio buffer is completed transferred all of its data to LPE audio unit. This bit is clear when write 1 to it AccessType: One to Clear
28:24	Reserved
23:16	**Reserved**
15	**Sample Buffer Underrun Interrupt Enable:** This bit is to enable the first line buffer underrun interrupt when sample buffer underrun status is detected 0 = LPE sample Buffer Underrun Interrupt Disabled 1 = LPE sample Buffer Underrun Interrupt Enabled
14	**Audio bandwidth Underrun Interrupt Enable:** This bit is to enable the first line bandwidth underrun interrupt when bandwidth underrun status is detected 0 = LPE Bandwidth Underrun Interrupt Disabled 1 = LPE Bandwidth Underrun Interrupt Enabled
13:3	Reserved
2	**Azalia compatible mode:** This bit is to enable the vucp, PR, ECC to be generated in the Azalia way 0 = Disable Azalia compatible mode on vucp, PR, ECC 1 = Enable Azalia compatible mode on vucp, PR, ECC
1	**Reserved**
0	**Function Reset (R/W, only):** Write 1 to this bit will reset hardware within audio unit without needs of reset the full display controller. The FIFO and pointers will be reset and audio

	registers will be reset to default values. Write 0 will put the unit back to idle and ready to be programmed again.

STREAM_A_LPE_AUD_HDMIW_INFOFR—Audio HDMI Data Island Packet Data

Memory Offset Address: 65068h

Default Value: 00000000h

Normal Access: Read/Write

When the IF type or dword index is not valid, the contents of the DIP will return all 0's.

Bit	Descriptions
31:0	**Data Island Packet Data :** When read, this returns the current value at the location specified in the Video DIP buffer index select and Video DIP RAM access address fields. The index used to address the RAM is incremented after each read or write of this register. DIP data can be read at any time. Data should be loaded into the RAM before enabling the transmission through the DIP type enable bit. Accesses to this register are on a per-DWORD basis

Construction of DIP write: MSB LSB

DW0	ECC for header (read only, calculated by HW)	Header byte 2	Header byte 1	Header byte 0
DW1	Data byte 3	Data byte 2	Data byte 1: start of payload	Data byte 0: Checksum for payload
…				
DW8 (read only, calculated by HW)	ECC		ECC for data bytes 7-13	ECC for data bytes 0-6

STREAM_B_LPE_AUD_CONFIG—LPE Audio Configuration

Memory Offset Address: 65800h

Default Value: 00000280h

Normal Access: Read/Write

This register configures the HDMI audio unit

Bit	Descriptions
31:17	Reserved
16	**LPE Stream B Pause/resume** – DMA pause fetching at the boundary of buffers when this bit is set, and resume fetching when this bit is cleared. 1= DMA stop requesting more audio sample from buffer A,B,C,D after reading and depleting all data from current buffer 0= DMA resume requesting data from the next available buffer (A,B,C,D). Programming note: this bit should not be used by SW driver. When SW driver wants to pause audio, it shall invalidate the two newest allocated audio buffers. When the current audio buffers are processed, silent stream is sent automatically.
15	LPE HDMI/DP mode on stream B 1= DP mode 0 = HDMI mode (default)
14	**Bogus sample disable for odd channel** When number of channels in a sample is odd (3, 5, or 7) source application may pad a bogus sample to the next even number of channels. If this bit is set there is no padding in input buffer 1= No bogus sample present in buffer for odd number of channels 0= Bogus sample present in buffer for odd number of channels (default)
13	**Left alignment** When input buffer is in 32-bit container mode. If this bit is set the MSB of audio sample is aligned bit 31 of the container if this bit is clear MSB of audio sample is aligned with bit 23 of the container. 1= MSB is bit 31 of 32-bit container 0= MSB is bit 23 of 32-bit container (default)
12	**16-bit container** When this bit is set 16-bit sample is stored in 16-bit container format. When it is clear container is 32-bit for each sample regardless of valid bits (default) 1= 16-bit container 0= 32-bit container
11	**Underrun packet bit (Silent Stream enable)** Set this bit will enble HW to send valid zero-filled packet with Sample flat bit set when no sample buffer is available, NCTS packets (or Timesstamp packet) are sent to keep sink in sync even no audio sound will heard.

	1= send underrun packets (silent stream) 0= send null packets (default) Programming note: SW driver shall always set silent stream bit. When SW driver wants to pause audio, it shall invalidate the two newest allocated audio buffers. When the current audio buffers are processed, silent stream is sent automatically.
10	User bit (U) HW will clear this bit ineach sub-frames it sends. 1= sey U bit in sub-frame 0= clear U bit in sub-frame (default)
9	Validity Bit (V) HW will set this bit in both each sub-frames it sends. 1= Set V bit in sub-frame (default) Reserved
8	Sample Flat bit When set the sample flat bit will be set in all HDMI sub-packets. 1= flat bit is set for valid sample 0= flat bit is not set for valid sample (default)
7	Set Block begin for all sub-packets Controls the B bit in the header of only the first Audio Packet /frame of a 192 frame 60958 block in Layout 1 mode. This bit only applies to LPE HDMI mode. 0: The B bit will be set only for sub-packet 0 1: The B bit in the Audio sample packet header will be set for all valid sub-packets. (default)
6:4	Num. audio Channels 000: 2 channels (stereo) 001: 3 channels 010: 4 channels 011: 5 channels 100: 6 channels 101: 7 channels 110: 8 channels **Note:** When disable_bogus sample bit is clear HW will always treat odd number of channels similar to the next higher even number. Thus 3 is similar to 4, 5 to 6 and 7 to 8. This is because

	SW ensures that an even number of samples are packed in the audio buffers. Programming note: Bit 6 of of this field is a write only bit. When reads back, it always returns zero. Ensure to write bit 6 to 1'b1 when programming for 6/7/8 audio channels.
3:2	Format 00: L-PCM or IEC 61937 01: High Bit Rate IEC 61937 stream packet (not supported) 10: One Bit Audio Sample packet (not supported) 11: DST Audio Sample packet (not supported)
1	Layout 0: Layout 0 (2-ch) 1: Layout 1 (3-8 ch) **Note:** Layout bit doesn't matter for HBR
0	**Audio Enable :** Controls generation of N/CTS and transmission of audio sample packets. 0: Audio sample packets are not transmitted, CTS calculation/transmission is disabled 1: Audio sample packets are transmitted & CTS calculation is enabled When enable audio unit will wait until the next vertical blank period before sending out the audio packets. When disable, audio unit may continue to send audio packet until the end of current active video frame before stopping.

STREAM_B_LPE_AUD_CH_STATUS_0 – Audio Channel Status Attributes 0

Memory Offset Address: 65808h

Default Value: 00000000h

Normal Access: Read/Write

Bit	Descriptions
31:0	**Channel status register 0**. These bits are transmitted as attributes of audio packets

Each block has 192 frames so there are 192 bit slots available for transmission. But it is nly the first 40 bits of the channel status are meaningful. Software driver will program these two registers with appropriate values before enabling audio. For each block, the first 40 bits are inserted one at a time in each frame, the remaining 152 bits are zeroed. Note that the same C bit value is transmitted for each subframe of each sub-packet.

Byte	Consumer format channel status fields							
0	Pro/con = 0	Non-audio = 0	Copyright	Emphasis			Channel status mode = 00	
	bit 0	1	2	3	4	5	6	7
1	Category code							
	bit 8	9	10	11	12	13	14	15
2	Source number				Channel number			
	bit 16	17	18	19	20	21	22	23
3	Sampling frequency				Clock accuracy			
	bit 24	25	26	27	28	29	30	31
4	Word length				(Future original sampling frequency?)			
	bit 32	33	34	35	36	37	38	39
5–23	Reserved							
	bits 40–191							

Table 2. Consumer format channel status fields.

STREAM_B_LPE_AUD_CH_STATUS_1 – Audio Channel Status Attributes 1

Memory Offset Address: 6580Ch

Default Value: 00000000h

Normal Access: Read/Write

Bit	Descriptions
31:8	Reserved
7:0	**Channel status register 1**. These bits are transmitted as attributes of audio packets. There is only 8 bits valid in this register.

STREAM_B_LPE_AUD_HDMI_CTS_DP_Maud – Audio HDMI CTS Register (DP Maud)

Memory Offset Address: 65810h

Default Value: 00000000h

Normal Access: Read/Write

Bit	Descriptions
31:25	Reserved
24	Enable CTS/M Programming 1 = Enable CTS/M programming 0 = Disable CTS/M programming
23:0	HDMI CTS Values These are bits [23:0] of programmable HDMI CTS values (or DP Maud) that is pre-calculated to achieve desired audio sample rates with a particular pixel clocks configuration. Audio function must be disabled when changing this field. Bit 24 also need to write to 1 to enable this field.

STREAM_B_LPE_AUD_HDMI_N_DP_Naud – Audio HDMI N Register (DP Naud)

Memory Offset Address: 65814h

Default Value: 00000000h

Normal Access: Read/Write

Bit	Descriptions
31:25	Reserved
24	Enable N Programming 1 = Enable N programming 0 = Disable N programming

23:0	HDMI N Values These are bits [23:0] of programmable HDMI N (or DP Naud) values that is pre-calculated to achieve desired audio sample rates with a particular pixel clocks configuration. Audio function must be disabled when changing this field. Bit 24 also need to write to 1 to enable this field.

STREAM_B_LPE_AUD_Buffer_config – LPE Audio buffer config

Memory Offset Address: 65820h

Default Value: 00000100h

Normal Access: Read/write

These registers facilliates HDMI audio sample buffer management mechanism between Software and Hardware to fetch the HDMI audio samples from system memory to display controller Hardware provides 4 set of buffers A, B, C, and D. Software will program the address and the length of buffer then set the buffer valid. Hardware will start fectching the audio sample from valid buffers, update remaining bytes, and eventually clear the valid bit when it is done. If the buffer interrupt bit is set Hardware will generate an interrupt to IIR register in the graphics interface and Software will be notified. If there is more than one buffers valida at one time Hardware will srart in alphabetical order and rotate through all 4 buffers.

Bit	Descriptions
31:24	Reserved
23:16	Audio buffer delay. This field specifies a delay in number of video frames that the audio controller will count off when audio enable bit is set before start transmitting audio sample.
15:11	Reserved.
10:8	DMA FIFO watermark Audio unit has a 8x64 bytes fifo for pre-fetching and staging audio samples. This register provides a watermark value in SWORDs (64B). When enable and sample buffer is available audio unit will fetch samples until this FIFO is full then it waits until HDMI/DP packet assembler drains the samples to a level less or equal the watermark setting then it will start fetching the samples again. Default value is 1 cacheline (SW).
7:0	FIFO watermark.

	Audio unit has a 96x8 bytes fifo for pre-fetching and staging audio samples. This register provides a watermark value in DWORDs. When enable and sample buffer is available audio unit will fetch samples until this FIFO occupancy is above the watermark then it waits until HDMI packet assembler drains the samples to a level less or equal the watermark setting then it will start fetching the samples again

STREAM_B_LPE_AUD_BUF_CH_SWP — Audio Sample Swapping

Memory Offset Address: 65824h

Default Value: 00FAC688h

Normal Access: Read only

Audio sample in input buffer can be rearranged before sending as HDMI subpacket. For each of 32-byte block of audio samples we give them an index from 0 to 7. This index then can be programmed into this register to destinate its location in a subpacket of a HDMI audio packet. Software can take advantage of this register and leave the channel rearrangement in hardware by specified a location of channel in current sample that would like to map to HDMI channel order. In case of less than 8 channel the index of the channel above the valid number will be ignored. This register is only valid for layout 1.

Bit	Descriptions
31:24	Reserved
23:21	**Sample index for Second channel of subpacket 3.** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 3 in a HDMI audio packet
20:18	**Sample index for First channel of subpacket 3.** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 1 in a HDMI audio packet
17:15	**Sample index for Second channel of subpacket 2.** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 0 in a HDMI audio packet
14:12	**Sample index for First channel of subpacket 2.** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 0 in a HDMI audio packet
11:9	**Sample index for Second channel of subpacket 1.** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 1 in a HDMI audio packet
8:6	**Sample index for First channel of subpacket 1.** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 1 in a HDMI audio packet
5:3	**Sample index for Second channel of subpacket 0.** This field has the index of 32-byte buffer

	block that will be send out as the second channel sample of subpacket 0 in a HDMI audio packet
2:0	**Sample index for First channel of subpacket 0.** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 0 in a HDMI audio packet

STREAM_B_LPE_AUD_BUF_A_ADDR – Address for Audio Buffer A

Memory Offset Address: 65840h

Default Value: 00000000h

Normal Access: Read/Write

Bit	Descriptions
31:6	**Buffer address**. This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	Reserved
1	**Interrupt enable.** If enable hardware will generate an interrupt when it is done fetching this buffer
0	**Buffer valid**. This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

STREAM_B_LPE_AUD_BUF_A_LENGTH — Length for Audio Buffer A

Memory Offset Address: 65844h

Default Value: 00000000h

Normal Access: Read/Write

Bit	Descriptions
31:20	Reserved
19:0	**Buffer Length** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

STREAM_B_LPE_AUD_BUF_B_ADDR – Address for Audio Buffer B

Memory Offset Address: 65848h

Default Value: 00000000h

Normal Access: Read/Write

Bit	Descriptions
31:6	**Buffer address**. This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	Reserved
1	**Interrupt enable.** If enable hardware will generate an interrupt when it is done fetching this buffer
0	**Buffer valid**. This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

STREAM_B_LPE_AUD_BUF_B_LENGTH — Length for Audio Buffer B

Memory Offset Address: 6584Ch

Default Value: 00000000h

Normal Access: Read/Write

Bit	Descriptions
31:20	Reserved
19:0	**Buffer Length** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

STREAM_B_LPE_AUD_BUF_C_ADDR – Address for Audio Buffer C

Memory Offset Address: 65850h

Default Value: 00000000h

Normal Access: Read/Write

Bit	Descriptions
31:6	**Buffer address**. This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	Reserved

1	**Interrupt enable.** If enable hardware will generate an interrupt when it is done fetching this buffer
0	**Buffer valid**. This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

STREAM_B_LPE_AUD_BUF_C_LENGTH — Length for Audio Buffer C

Memory Offset Address: 65854h

Default Value: 00000000h

Normal Access: Read/Write

Bit	Descriptions
31:20	Reserved
19:0	**Buffer Length** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

STREAM_B_LPE_AUD_BUF_D_ADDR – Address for Audio Buffer D

Memory Offset Address: 65858h

Default Value: 00000000h

Normal Access: Read/Write

Bit	Descriptions
31:6	**Buffer address**. This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	Reserved
1	**Interrupt enable.** If enable hardware will generate an interrupt when it is done fetching this buffer
0	**Buffer valid**. This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

STREAM_B_LPE_AUD_BUF_D_LENGTH — Length for Audio Buffer D

Memory Offset Address: 6585Ch

Default Value: 00000000h

Normal Access: Read/Write

Bit	Descriptions
31:20	Reserved
19:0	**Buffer Length** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

STREAM_B_LPE_AUD_CNTL_ST—LPE Audio Control State Register

Memory Offset Address: 65860h

Default Value: 00000000h

Access:Read/Write

Bit	Description
31	Reserved
30:29	Reserved.
28:25	Reserved for later DIP type if needed: Must be 0.
24:21	**DIP type enable status (read only):** These bits reflects the DIP types enabled. It can be updated while the port is enabled. Within 2 vblank periods, the DIP is guaranteed to have been transmitted. Disabling an DIP type results in setting the contents of that DIP buffer to zero. A reserved setting reflects a disabled DIP. XXX1 = Audio DIP enable status **(Default = disabled)** XX1X = Generic 1 (ACP) DIP enable status **(Default = disabled)** X1XX = Generic 2 DIP enable status, can be used by ISRC1 or ISRC2 **(Default = disabled)** 1XXX = Reserved AccessType: Read Only
20:18	**DIP buffer index (R/W):** This field is used during read or write of different DIPs, and during read or write of ELD data. These bits are used as an index to their respective DIP or ELD buffers. When the index is not valid, the contents of the DIP will return all 0's.

	000 = (Default) Audio DIP (31 bytes of address space, 13 bytes of data) 001 = Generic 1 (ACP) Data Island Packet (31 bytes of address space, 11 bytes of data) 010 = Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data) 011 = Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data) 1XX = reserved
17:16	**DIP transmission frequency (R/W)** These bits reflect the frequency of DIP transmission for the DIP buffer type designated in bits 20:18. When writing DIP data, this value is also latched when the first DW of the DIP is written. When read, this value reflects the DIP transmission frequency for the DIP buffer designated in bits 20:18. 00 = Disabled (Default) 01 = once per frame 10 = Send once 11 = Best effort (Send at least every other vsync)
15	**CP Ready:** This **R/W** bit reflects the state of CP request from the audio unit. When an audio CP request has been serviced, it must be reset to 1 by the video software to indicate that the CP request has been serviced. 0 = CP request pending or not ready to receive requests (default) 1 = CP request ready
14	**Reserved**
13:9	**Reserved**
8:5	**Reserved**
4	**Reserved**
3:0	**DIP RAM access address (R/W):** Selects the DWORD address for access to the DIP buffers. The value wraps back to zero when it incremented past the max addressing value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.

STREAM_B_LPE_AUD_HDMI_STATUS—LPE Audio Status

Memory Offset Address: 65864h

Default Value: 00000000h

Normal Access: Read/Write

Bit	Descriptions
31	**Sample Buffer Underrun Status:** This bit indicates an underrun in the sample buffer to HDMI/DP controller when it needs to send. This bit is set at the last line of active video when there are no more sample in any valid buffers and HDMI/DP audio unit has not satisfied number of audio samples intended in that video frame. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO. AccessType: One to Clear
30	**Reserved**
29	**LPE Audio Buffer Done Status:** This bit is set when a LPE audio buffer is completed transferred all of its data to LPE audio unit. This bit is clear when write 1 to it AccessType: One to Clear
28:24	Reserved
23:16	**Reserved**
15	**Sample Buffer Underrun Interrupt Enable:** This bit is to enable the first line buffer underrun interrupt when sample buffer underrun status is detected 0 = LPE sample Buffer Underrun Interrupt Disabled 1 = LPE sample Buffer Underrun Interrupt Enabled
14	**Audio bandwidth Underrun Interrupt Enable:** This bit is to enable the first line bandwidth underrun interrupt when bandwidth underrun status is detected 0 = LPE Bandwidth Underrun Interrupt Disabled 1 = LPE Bandwidth Underrun Interrupt Enabled
13:1	Reserved
2	**Azalia compatible mode:** This bit is to enable the vucp, PR, ECC to be generated in the Azalia way 0 = Disable Azalia compatible mode on vucp, PR, ECC 1 = Enable Azalia compatible mode on vucp, PR, ECC
1	**Reserved**

0	**Function Reset (R/W, only):** Write 1 to this bit will reset hardware within audio unit without needs of reset the full display controller. The FIFO and pointers will be reset and audio registers will be reset to default values. Write 0 will put the unit back to idle and ready to be programmed again.

STREAM_B_LPE_AUD_HDMIW_INFOFR—Audio HDMI Data Island Packet Data

Memory Offset Address: 65868h

Default Value: 00000000h

Normal Access: Read/Write

When the IF type or dword index is not valid, the contents of the DIP will return all 0's.

Bit	Descriptions
31:0	**Data Island Packet Data :** When read, this returns the current value at the location specified in the Video DIP buffer index select and Video DIP RAM access address fields. The index used to address the RAM is incremented after each read or write of this register. DIP data can be read at any time. Data should be loaded into the RAM before enabling the transmission through the DIP type enable bit. Accesses to this register are on a per-DWORD basis

Construction of DIP write: MSB LSB

DW0	ECC for header (read only, calculated by HW)	Header byte 2	Header byte 1	Header byte 0
DW1	Data byte 3	Data byte 2	Data byte 1: start of payload	Data byte 0: Checksum for payload
…				
DW8 (read only, calculated by HW)	ECC		ECC for data bytes 7-13	ECC for data bytes 0-6

Display and Cursor Registers (70000h–7FFFFh)

These registers are memory mapped and accessible through normal 32 bit, 16 bit, or 8 bit accesses.

Display Pipeline A

PIPEA_DSL—Pipe A Display Scan Line

Memory Offset Address: 70000h

Default Value: 00000000h

Normal Access: Read only

This register enables the read back of the display pipe vertical "line counter". The display line value is from the display pipe A timing generator and is reset to zero at the beginning of a scan. The value increments at the leading edge of HSYNC and can be safely read any time. For normal operation, scan line zero is the first active line of the display. When in VGA centering mode, the scan line 0 is the 1st active scan line of the pseudo border not the centered active VGA image. In interlaced display timings, the scan line counter provides the current line in the field. One field will have a total number of lines that is one greater than the other field.

Programming Note: In order to cause the scan line logic to report the correct Line Counter value, the corresponding Display Pipeline timing registers must be programmed to valid, non-zero (e.g., 640x480 @ 60Hz) values before enabling the Pipe or programming VGA timing and enabling native VGA.

Bit	Descriptions
31	**Current Field:** Provides read back of the current field being displayed on display pipe A. Non-TV mode: 0 = first field (odd field) 1 = second field (even field) TV mode: 1 = first field (odd field) 0 = second field (even field)
30:13	**Reserved:** Read only.
12:0	**Line Counter for Display [12:0]:** Provides read back of the display pipe A vertical line counter. This is an indication of the current display scan line to be used by software to synchronize with the display.

PIPEA_SLC—Pipe A Display Scan Line Count Range Compare

Memory Offset Address: 70004h

Default Value: 00000000h

Normal Access: Read/Write

This register can be written via the command stream processor using the MI_LOAD_SCAN_LINES_INCL or MI_LOAD_SCAN_LINES_EXCL commands. They can safely be accessed at any time.

The Top and Bottom Line Count Compare registers are compared with the display line values from display A timing generator. The Top compare register operator is a less than or equal, while the Bottom compare register operator is a greater than or equal. The results of these 2 comparisons are communicated to the command stream controller for generating interrupts, status, and command stream flow control ("wait for within range" and "wait for not within range"). For range check, the value programmed should be the (**desired value – 1)**, so for line 0, the value programmed is VTOTAL, and for line 1, the value programmed is 0.

Bit	Descriptions
31	Inclusive / Exclusive: 1 = Inclusive: within the range. 0 = Exclusive: outside of the range.
30:29	**Reserved:** Read only.
28:16	**Start Scan Line Number:** This field specifies the starting scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0,Display Buffer height in lines-1].
15:13	**Reserved:** Read only.
12:0	**End Scan Line Number:** This field specifies the ending scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0, Display Buffer height in lines-1].

PIPEACONF—Pipe A Configuration Register

Memory Offset Address: 70008h

Default Value: 00000000h

Normal Access: Read/Write double buffered

Bit	Descriptions
31	**Pipe A Enable:** Setting this bit to the value of one, turns on pipe A. This must be done before any planes are enabled on this pipe. Changing it to a zero should only be done when all planes that are assigned to this pipe have been disabled. Turning the pipe enable bit off disables the

	timing generator in this pipe. Plane disable occurs after the next VBLANK event after the plane is disabled. Synchronization pulses to the display are not maintained if the timing generator is disabled. Power consumption will be at it's lowest state when disabled. A separate bit controls the DPLL enable for this pipe. Pipe timing registers should contain valid values before this bit is enabled. 0 = Disable 1 = Enable
30	**Pipe State:** This bit indicates the actual state of the pipe. Since there can be some delay between disabling the pipe and the pipe actually shutting off, this bit indicates the true current state of the pipe. 0 = Disabled1 = Enabled AccessType: Read Only
29	DSI PLL Lock (lock): This bit indicates the clocks from DSI PLL are locked. 0 = Unlocked 1 = Locked AccessType: Read only
28:27	**Reserved**
26	**Display Port Audio Only Mode:** Setting this bit to 1 indicates the DisplayPort will output audio only. 0 = DisplayPort will output Video or Video and Audio 1 = DisplayPort will output Audio only
25	**Reserved**
24	**Pipe A Gamma Unit Mode:** This bit selects which mode the pipe gamma correction logic works in. In the palette mode, it behaves as a 3X256x8 RAM lookup. VGA and indexed mode operation should use the palette in 8-bit mode. In the 10-bit gamma mode, it will act as a piecewise linear interpolation. Other gamma units such as in the overlay or sprite are unaffected by this bit. 0 = 8-bit Palette Mode 1 = 10-bit Gamma Mode

23:21	Interlaced Mode These bits are used for software control of interlaced behavior. They are updated immediately if the pipe is off, or in the vertical blank after programming if pipe is enabled. 0xx = Progressive 100 = Interlaced embedded panel using programmable vertical sync shift. (2x) 101 = Interlaced using vertical sync shift. Backup option to 110 setting. (2x) 110 = Interlaced with VSYNC/HSYNC Field Indication using legacy vertical sync shift. 111 = Interlaced with Field 0 Only using legacy vertical sync shift. Not used Note: VGA display modes and Panel fitting do not work while in interlaced modes Setting the Interlaced embedded panel mode causes hardware to automatically modify the output to match the specifications of panels that support interlaced mode.
20	**MIPI Display Self-refresh mode for MIPI A (refresh):** 0 = Normal Operation, display controller generate timing and refresh display panel at refresh rate 1 = Display self-refresh mode. Display controller update frame buffer in display module on demand only
19	**Display/Overlay Planes Off:** This bit when set will cause all enabled Display and overlay planes that are assigned to this pipe to be disabled by overriding the current setting of the plane enable bit, at the next VBLANK. Timing signals continue as they were but the screen becomes blank. Setting the bit back to a zero will then allow the display and overlay planes to resume on the following VBLANK. 0 = Normal Operation 1 = Planes assigned to this pipe are disabled.
18	**Cursor Planes Off:** This bit when set will cause all enabled cursor planes that are assigned to this pipe to be disabled by overriding the current setting of the plane enable bit, at the next VBLANK. Timing signals continue as they were but the cursor(s) no longer appear on the screen. Setting the bit back to a zero will then allow the cursor planes to resume on the following VBLANK. 0 = Normal Operation 1 = Planes assigned to this pipe are disabled.
17:16	Refresh Rate CxSR Mode Association These bits select how refresh rates are tied to big FIFO mode on pipe A. When they are set to anything other than 00, bits 23:21 of this register must be programmed to 0xx. Switching between 01 and 10 settings directly is not allowed. Software must program this field to 00 before switching. Software is responsible for enabling this mode only for integrated dispay panels that support corresponding mode. 00 – **Default** – no dynamic refresh rate change enabled. Software control only.

	01 – Progressive-to-progressive refresh rate change enabled and tied to big FIFO mode. Pixel clock values set in FPA0/FPA1 settings in the DPLLA control register and FPA0/FPA1 divider registers. FPA0 is tied to non-big-FIFO mode 10 – Progressive-to-interlaced refresh rate change enabled and tied to big FIFO mode. Pixel clock value does not change in this case. Scaling must be disabled in this mode. Uses programmable VS shift 11 – Reserved
15	Color Correction Matrix Enable on Pipe A 1 = Color Correction Coefficients are enabled to perform color correction 0 = Color Correction Coefficients are disabled
14	**DisplayPort Power Mode Switch :** This bit selects the software controlled progressive to progressive power saving mode (software controlled DRRS). Hardware Controlled Refresh Rate Select must be disabled when enabling this. Link and data M/N 1 values are used for normal settings, M/N 2 values are used for low power settings. 0 – Normal progressive refresh rate (default) 1 – Low Power progressive refresh rate
13	Reserved
12	**Reserved**
11:10	**Reserved**
9:8	**Reserved**
7:5	**Bits Per Color: :** This field selects the number of bits per color sent to a receiver device connected to this port. Color format takes place on the Vblank after being written. Color format change can be done independent of a pixel clock change in DisplayPort. Selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer results in dithering the output stream. For further details on Display Port fixed frequency programming to accommodate these formats refer to "DP Frequency Programming" in DPLL section of Bspec. 000 = 8 bits per color **(Default)** 001 = 10 bits per color 010 = 6 bits per color 011 = RESERVED 1xx = RESERVED

4	**Dithering enable:** This bit enables dithering for DisplayPort 6bpc or 8bpc modes **0 –** Dithering disabled (Default) **1 –** Dithering enabled Programming note: Dithering should only be enabled for 8 bpc or 6 bpc.
3:2	**Dithering type:** This bit selects dithering type for DisplayPort 6bpc or 8bpc modes **00 -** Spatial only (default) **01-** Spatio-Temporal 1 **10-** Reserved **11-** Reserved
1	**Reserved**
0	**Reserved:** Write as zero

PIPEAGCMAXRED—Pipe A Gamma Correction Max Red

Memory Offset Address: 70010h

Default Value: 00010000h

Normal Access: Read/Write

Bit	Descriptions
31:17	Reserved
16:0	**Max Red Gamma Correction Point:** 129th reference point for red channel of the pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 1024.0. Format: 11.6 Default: 0x10000

PIPEAGCMAXGREEN—Pipe A Gamma Correction Max Green

Memory Offset Address: 70014h

Default Value: 00010000h

Normal Access: Read/Write

Bit	Descriptions
31:17	Reserved

16:0	**Max Green Gamma Correction Point:** 129th reference point for green channel of the pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 1024.0. Format: 11.6 Default: 0x10000

PIPEAGCMAXBLUE—Pipe A Gamma Correction Max Blue

Memory Offset Address: 70018h

Default Value: 00010000h

Normal Access: Read/Write

Bit	Descriptions
31:17	Reserved
16:0	**Max Blue Gamma Correction Point:** 129th reference point for blue channel of the pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 1024.0. Format: 11.6 Default: 0x10000

PIPEASTAT—Pipe A Display Status

Memory Offset Address: 70024h

Default Value: 00000000h

Normal Access: Read/Write

This register is the second level of a two level interrupt and status scheme. A single bit in the first line interrupt status register represents the state of this register which is equal to the AND of a status bits with their corresponding enable bits OR'ed together. First line interrupt status bits can cause interrupts or writes of the status register to cacheable memory. Bits in this register indicate the status of the display pipe A and can cause interrupt status bit changes in the first level interrupt and status register. Status bits in this register as 'sticky" and once they are set will be cleared by writing a one to that bit. A write of a zero will not have an effect on the corresponding Interrupt status bit. The corresponding enable bits will determine if the interrupt status bit should be used in the first line interrupt status register. When an interrupt occurs, the first line interrupt register indicates the second line source of the interrupt. Reading the second line register will determine the precise source for the interrupt.

Programming:

1. Prior to clearing a Display Pipe-sourced interrupt (e.g., Display Pipe A VBLANK) in the IIR, the corresponding interrupt (source) status in the PIPEASTAT or PIPEBSTAT register (e.g., Pipe A VBLANK

Interrupt Status bit of PIPEASTAT) must first be cleared. Note that clearing these status bits requires writing a '1' to the appropriate bit position.

2.

Bit	Descriptions
31	**FIFO A Under-run Status:** Set when a pipe A FIFO under-run occurs, cleared by a write of a 1. An underrun has occurred on an attempt to pop an empty FIFO. This does not feed into the first line interrupt status register. This will occur naturally during mode changes, to be useful, it should be cleared after a mode change has occurred. This bit is only valid after Pipe A has been completely configured. 1 = FIFO A Underflow occurred 0 = FIFO A Underflow did not occur AccessType: One to Clear
30	**Sprite B Flip Done Interrupt Enable:** This will enable the consideration of the Sprite B flip done interrupt status bit in the first line interrupt logic 0 = Sprite B Flip Done Interrupt Disabled 1 = Sprite B Flip Done Interrupt Enabled
29	**Reserved**
28	**Reserved**
27	**GMBUS Event Enable:** This will enable the use of the GMBUS interrupt status bit in the first line interrupt/status logic. 0 = No GMBUS event enabled 1 = GMBUS event enabled
26	**Plane A Flip Done Interrupt Enable:** This will enable the consideration of the Plane A flip done interrupt status bit in the first line interrupt logic 0 = Plane A flip done Interrupt/Status Disabled 1 = Plane A flip done Interrupt/Status Enabled
25	**Vertical Sync Interrupt Enable:** This will enable the consideration of the vertical sync interrupt status bit in the first line interrupt logic. 0 = Vertical Sync Interrupt/Status Disabled 1 = Vertical Sync Interrupt/Status Enabled
24	**Display Line Compare Enable:** This will enable the consideration of the line compare interrupt status bit in the first line interrupt/status logic. 0 = Display Line Compare Interrupt/Status Disabled 1 = Display Line Compare Interrupt/Status Enabled
23	**DPST Event Enable:** This interrupt is generated by the DPST logic. 0 = No DPST event enabled 1 = DPST event enabled
22	**Sprite A Flip Done Interrupt Enable:** This will enable the consideration of the Sprite A flip done interrupt status bit in the first line interrupt logic

	0 = Sprite A Flip Done Interrupt Disabled 1 = Sprite A Flip Done Interrupt Enabled
21	**Odd Field Interrupt Event Enable:** This bit should only be used when this pipe is in an interlaced display timing. 0 = Odd Field Event disable 1 = Odd Field Event enable
20	**Even Field Interrupt Event Enable:** This bit should only be used when this pipe is in an interlaced display timing. 0 = Even field Event disable 1 = Even field Event enable
19	Performance Counter Event Enable
18	**Start of Vertical Blank Interrupt Enable:** This will enable the consideration of the start of vertical blank interrupt status bit in the first line interrupt/status logic. 0 = Start of Vertical Blank Interrupt/Status Disabled 1 = Start of Vertical Blank Interrupt/Status Enabled
17	**Framestart Interrupt Enable:** This will enable the consideration of the vertical blank interrupt status bit in the first line interrupt/status logic. 0 = Vertical Blank Interrupt/Status Disabled 1 = Vertical Blank Interrupt/Status Enabled
16	**Pipe A Horizontal Blank Interrupt Enable**: This will enable the consideration of the start of horizontal blank interrupt status bit in the first line interrupt/status logic 0 = Start of Horizontal Blank Interrupt/Status Disabled 1 = Start of Horizontal Blank Interrupt/Status Enabled
15	**Sprite B Flip Done Interrupt Status:** MMIO Flip Event is completed on Sprite B 0 = Sprite B Flip Not Done 1 = Sprite B Flip Done AccessType: One to Clear
14	**Sprite A Flip Done Interrupt Status:** MMIO Flip Event is completed on Sprite A 0 = Sprite A Flip Not Done 1 = Sprite A Flip Done AccessType: One to Clear
13	**Reserved**
12	**Reserved**
11	**GMBUS Interrupt Status:** This status bit will be set on a GMBUS event. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. 0 = GMBUS event has not occurred 1 = GMBUS event has occurred AccessType: One to Clear

10	**Plane A Flip Done Interrupt Status:** Async/Sync Flip Event is completed on Display Plane A 0 = Plane A Flip Not Done 1 = Plane A Flip Done AccessType: One to Clear
9	**Vertical Sync Interrupt Status:** This bit provides a sticky status that is set when a pipe A vertical sync occurs, cleared by a write of a 1. For interlaced timing modes, this occurs once per field, when in progressive, it occurs once per frame. For this bit to be meaningful, the pipe and pixel clock should be enabled and running. 0 = Vertical Sync has not occurred 1 = Vertical Sync has occurred AccessType: One to Clear
8	**Display Line Compare Interrupt Status:** Set when a pipe A compare match occurs, cleared by a write of a 1. 0 = Display Line Compare has not been satisfied 1 = Display Line Compare has been satisfied AccessType: One to Clear
7	**DPST Event Status:** This bit is cleared when a write to this register occurs with this bit as a one. Writes with this bit as a zero has no effect on the value of the bit. Multiple DPST events (Histogram or Phase In) can cause this bit to be asserted, determination of which event occurred is done in the DPST registers. 0 = DPST Interrupt has not occurred on pipe A 1 = DPST Interrupt has occurred on pipe A AccessType: One to Clear
6	**Pipe A Panel Self Refresh Status:** This bit indicates interrupt is generated by the PSR controller and intends to send interrupt to SW driver when the PSR interrupt enable bit (70028h bit 22) is set. This is cleared when a write to this register occurs with this bit as a one. Write with this bit as a zero has no effect on the value of the bit. 0 = PSR Interrupt has not occurred on pipe A 1 = PSR interrupt has occurred on pipe A AccessType: One to Clear
5	**Odd Field Interrupt Status:** This status bit will be set on a Odd field VBLANK event. This bit should only be used when this pipe is in an interlaced display timing. For synchronization with register updates, the actual event will occur one line after the start of VBLANK. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. Note: This bit will not be set when pipe is in "Interlaced with Field 0 Only using legacy vertical sync shift" mode. 0 = Odd Field Vertical Blank has not occurred 1 = Odd Field Vertical Blank has occurred AccessType: One to Clear
4	**Even Field Interrupt Status:** This status bit will be set on a even field VBLANK event. This bit

	should only be used when this pipe is in an interlaced display timing. For synchronization with register updates, the actual event will occur one line after the start of VBLANK. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. Note: This bit will not be set when pipe is in "Interlaced with Field 0 Only using legacy vertical sync shift" mode. 0 = Even Field Vertical Blank has not occurred 1 = Even Field Vertical Blank has occurred AccessType: One to Clear
3	Performance Monitor Event interrupt AccessType: One to Clear
2	**Start of Vertical Blank Interrupt Status:** This status bit will be set at the beginning of a VBLANK event. At this point, the double buffered display registers flip, taking their new values. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. In MIPI DSR mode, GPIO TE trigger sets the Vblank Interrupt status 0 = Start of Vertical Blank has not occurred 1 = Start of Vertical Blank has occurred AccessType: One to Clear
1	**Framestart Interrupt Status:** This status bit will be set on a VBLANK event, when the frame start occurs. The display registers are updated at the start of vertical blank, but the new register data is not utilized by the display pipeline until the point in the vertical blank period when the frame start occurs, which is the event that triggers this bit. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. 0 = Vertical Blank has not occurred 1 = Vertical Blank has occurred AccessType: One to Clear
0	Pipe A Horizontal Blank Status: 0 = Pipe A Horizontal Blank has not occurred 1 = Pipe A Horizontal Blank has occurred AccessType: One to Clear

DPFLIPSTAT—Display FLIP Status Register

Memory Offset Address: 70028h

Default Value: 00000000h

Normal Access: Read/Write

This register is the first level render flip event status/interrupt enable bits. When a flip event occurs and the corresponding status/interrupt enable bit is set, the corresponding pulse interrupt is generated to the graphics interface and sent to GT.

The render flip event status bits are not persistence. An event will set the appropriate status bit for 1 clock. When an flip status event happens and the corresponding status enable bit it set, it generates a wire pulse to the graphics interface. First line interrupt status bits can cause the associated event wire to pulse.

The corresponding enable bits will determine if the interrupt status bit pulse should be used to pulse the associated wire to the graphics interface. This register is used ONLY for display to GT flip response communication. The register does NOT affect MMIO flip usage model via the driver.

Bit	Descriptions
31:30	Reserved: MBZ
29	Display pipe B Line Compare Interrupt Status Enable 0 = Display Pipe B Line Compare Interrupt Disabled 1 = Display Pipe B Line Compare Interrupt Enabled
28	Pipe B Horizontal Blank Interrupt Enable 0 = Pipe B Horizontal Blank Interrupt Disabled 1 = Pipe B Horizontal Blank Interrupt Enabled
27	Pipe B Vertical Blank Interrupt Enable 0 = Pipe B Vertical Blank Interrupt Disabled 1 = Pipe B Vertical Blank Interrupt Enabled
26	Sprite D Flip Done Interrupt Enable 0 = Sprite D Flip Done Interrupt Disabled 1 = Sprite D Flip Done Interrupt Enabled
25	Sprite C Flip Done Interrupt Enable 0 = Sprite C Flip Done Interrupt Disabled 1 = Sprite C Flip Done Interrupt Enabled
24	Plane B Flip Done Interrupt Enable 0 = Plane B Flip Done Interrupt Disabled 1 = Plane B Flip Done Interrupt Enabled
23	Reserved
22	Panel Self Refresh (PSR) Interrupt Enable on Pipe A 0 = PSR interrupt Disabled on Pipe A

	1 = PSR Interrupt Enabled on Pipe A
21	Display pipe A Line Compare Interrupt Status Enable 0 = Display Pipe A Line Compare Interrupt Disabled 1 = Display Pipe A Line Compare Interrupt Enabled
20	Pipe A Horizontal Blank Interrupt Enable 0 = Pipe A Horizontal Blank Interrupt Disabled 1 = Pipe A Horizontal Blank Interrupt Enabled
19	Pipe A Vertical Blank Interrupt Enable 0 = Pipe A Vertical Blank Interrupt Disabled 1 = Pipe A Vertical Blank Interrupt Enabled
18	Sprite B Flip Done Interrupt Enable 0 = Sprite B Flip Done Interrupt Disabled 1 = Sprite B Flip Done Interrupt Enabled
17	Sprite A Flip Done Interrupt Enable 0 = Sprite A Flip Done Interrupt Disabled 1 = Sprite A Flip Done Interrupt Enabled
16	Plane A Flip Done Interrupt Enable 0 = Plane A Flip Done Interrupt Disabled 1 = Plane A Flip Done Interrupt Enabled
15:0	Reserved: MBZ

DPINVGTT—Display Invalid GTT PTE Status Register

Memory Offset Address: 7002Ch

Default Value: 00000000h

Normal Access: Read/Write

This register is the second level of a two level interrupt and status scheme. A single bit in the first line interrupt status register represents the state of this register which is equal to the AND of a status bits with their corresponding enable bits OR'ed together. First line interrupt status bits can cause interrupts or writes of the status register to cacheable memory. Bits in this register indicate the status of the display flips on pipe A and pipe B and can cause interrupt status bit changes in the first level interrupt and status register. Status bits in this register as 'sticky" and once they are set will be cleared by writing

a one to that bit. A write of a zero will not have an effect on the corresponding Interrupt status bit. The corresponding enable bits will determine if the interrupt status bit should be used in the first line interrupt status register. When an interrupt occurs, the first line interrupt register indicates the second line source of the interrupt. Reading the second line register will determine the precise source for the interrupt.

Bit	Descriptions
31:24	Reserved: MBZ
23	Cursor B Invalid GTT PTE Interrupt Enable 0 = Cursor B Invalid GTT PTE Interrupt Disabled 1 = Cursor B Invalid GTT PTE Interrupt Enabled
22	Cursor A Invalid GTT PTE Interrupt Enable 0 = Cursor A Invalid GTT PTE Interrupt Disabled 1 = Cursor A Invalid GTT PTE Interrupt Enabled
21	Sprite D Invalid GTT PTE Interrupt Enable 0 = Sprite D Invalid GTT PTE Interrupt Disabled 1 = Sprite D Invalid GTT PTE Interrupt Enabled
20	Sprite C Invalid GTT PTE Interrupt Enable 0 = Sprite C Invalid GTT PTE Interrupt Disabled 1 = Sprite C Invalid GTT PTE Interrupt Enabled
19	Plane B Invalid GTT PTE Interrupt Enable 0 = Plane B Invalid GTT PTE Interrupt Disabled 1 = Plane B Invalid GTT PTE Interrupt Enabled
18	Sprite B Invalid GTT PTE Interrupt Enable 0 = Sprite B Invalid GTT PTE Interrupt Disabled 1 = Sprite B Invalid GTT PTE Interrupt Enabled
17	Sprite A Invalid GTT PTE Interrupt Enable 0 = Sprite A Invalid GTT PTE Interrupt Disabled 1 = Sprite A Invalid GTT PTE Interrupt Enabled
16	Plane A Invalid GTT PTE Interrupt Enable 0 = Plane A Invalid GTT PTE Interrupt Disabled

	1 = Plane A Invalid GTT PTE Interrupt Enabled
15:8	Reserved: MBZ
7	Cursor B Invalid GTT PTE Status 0 = Cursor B encountered an invalid GTT PTE has not occurred 1 = Cursor B encountered an invalid GTT PTE has occurred AccessType: One to Clear
6	Cursor A Invalid GTT PTE Status 0 = Cursor A encountered an invalid GTT PTE has not occurred 1 = Cursor A encountered an invalid GTT PTE has occurred AccessType: One to Clear
5	Sprite D Invalid GTT PTE Status 0 = Sprite D encountered an invalid GTT PTE has not occurred 1 = Sprite D encountered an invalid GTT PTE has occurred. AccessType: One to Clear
4	Sprite C Invalid GTT PTE Status 0 = Sprite C encountered an invalid GTT PTE has not occurred 1 = Sprite C encountered an invalid GTT PTE has occurred. AccessType: One to Clear
3	Plane B Invalid GTT PTE Status 0 = Plane B encountered an invalid GTT PTE has not occurred 1 = Plane B encountered an invalid GTT PTE has occurred. AccessType: One to Clear
2	Sprite B Invalid GTT PTE Status 0 = Sprite B encountered an invalid GTT PTE has not occurred 1 = Sprite B encountered an invalid GTT PTE has occurred. AccessType: One to Clear
1	Sprite A Invalid GTT PTE Status 0 = Sprite A encountered an invalid GTT PTE has not occurred 1 = Sprite A encountered an invalid GTT PTE has occurred.

	AccessType: One to Clear
0	Plane A Invalid GTT PTE Status 0 = Plane A encountered an invalid GTT PTE has not occurred 1 = Plane A encountered an invalid GTT PTE has occurred. AccessType: One to Clear

DSPARB—Display Arbitration Control

Memory Offset Address: 70030h

Default Value: 80008000h

Normal Access: Read/Write

Reset value is for [vlv-32KB]

Default:C080C080h

Default [vlv-16KB]:C080C080h

Notes: Each active display plane A, B, sprite A, B, C, D requires a FIFO to cover for memory latency. There are two FIFOs, one for each pipe. The FIFO all come from a single RAM that is divided into areas for each display plane, and 2 sprites. Plane A, and sprite A, B share one FIFO. Plane B, and sprite C, D share another FIFO. The amount of the RAM used by each display plane is defined by this register. The two fields in the register split the display RAM into three portions, allocated between display plane A, sprite A, B for pipe A, and display planeB, sprite C, D for pipe B. This register is double buffered and updated on the leading edge of Vertical Blank of the pipe. It takes effect on the next VBLANK for whichever pipe is currently active. Each display plane needs a minimum FIFO size that is at least MaxLatencyForPlane * PixelRate * PixelSize + 512. All values should be rounded up to the next unit of 64B.

Notes: A special C3 mode can occur when a single display (of Display A and Display B) is active and the overlay and Display C are disabled. In that mode, when C3 is entered, the values in the BSTART and CSTART fields are ignored and the entire RAM is allocated to the single active display plane.

Notes: The control granularity of FIFO size is 64-bytes and the total size of the RAM is 2048*16 bytes making TOTALSIZE equal to 512. The range of values for sprite ASTART and sprite BSTART is 0-511. Similarly, the range of values for sprite CSTART and sprite DSTART is 0-511.

Notes: [VLV] FIFO Sizes PA=128, SA=64, SB=64; PB=128, SC=64, SD=64

Notes: [vlv-16KB setting] FIFO Sizes PA=128, SA=64, SB=64; PB=128, SC=64, SD=64

Notes: [vlv-32KB setting] FIFO Sizes PA=256, SA=128, SB=128; PB=256, SC=128, SD=128

Notes: The display dot clock frequency or pixel rate must not exceed 90% of the core display clock. When a primary plane is enabled with 64bpp format and sprite is also enabled on the same pipe, the dot clock frequency or pixel rate must be less than 80% of the core display clock.

FW1—Display FIFO Watermark Control 1

Memory Offset Address: 70034h

Default Value: 3F8F0F0Fh

Normal Access: Read/Write

These control values only apply to high-resolution (non-VGA) modes of operation. The hardware depends on these registers being set properly since it is possible to set the watermarks to states causing starvation of the sync FIFO.

Bit	Description
31:23	**Display FIFO Self Refresh Watermark**. This register defines the value of the watermark used by the Display streamer in case the CPU is in C2/C3/C4 and the memory has entered self refresh. Number in 64Bs of space in FIFO above which the Display Stream will generate requests to Memory.
22	Reserved – MBZ
21:16	**Reserved**
15:8	**Display Plane B FIFO Watermark:** Number in 64Bs of space in FIFO above which the Display B Stream will generate requests to Memory.
7:0	**Display Plane A FIFO Watermark:** Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory.

FW2—Display FIFO Watermark Control 2

Memory Offset Address: 70038h

Default Value: 0b0f0f0fh

Normal Access: Read/Write

These control values only apply to high-resolution (non-VGA) modes of operation. The hardware depends on these registers being set properly since it is possible to set the watermarks to states causing starvation of the sync FIFO.

Bit	Description
31	Reserved: MBZ
30:28	Reserved: MBZ
27:24	Reserved: MBZ

23:16	Reserved: MBZ
15:14	Reserved: MBZ
13:8	**Reserved**
7:0	**Display Plane Sprite A FIFO Watermark**. Number in 64Bs of space in FIFO above which the Display Sprite A Stream will generate requests to Memory

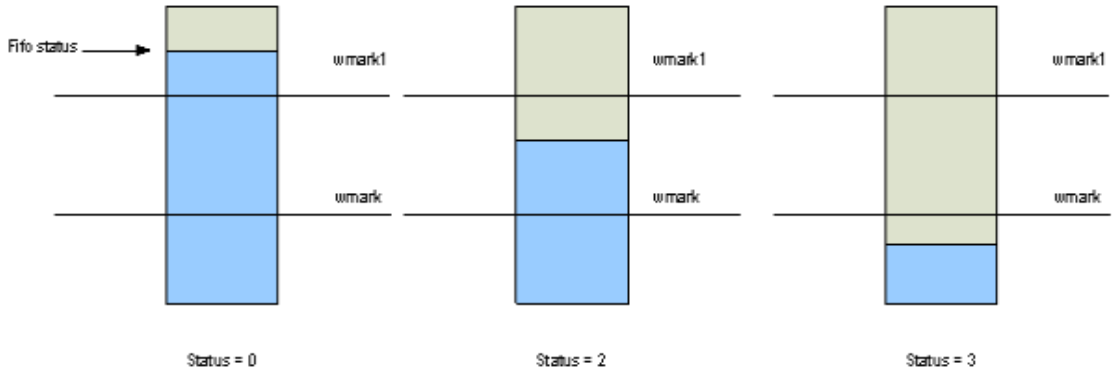
FW4—Display FIFO Watermark1 Control 4

Memory Offset Address: 70070h

Default Value: 00040404h

Normal Access: Read/Write

These control values only apply to high resolution (non-VGA) modes of operation. The hardware depends on these registers being set properly since it is possible to set the watermarks to states causing starvation of the sync FIFO. These values control the second watermark level. For each FIFO, there are two watermarks, wmark1 and wmark. When fifo status is above wmark1, hardware generates a status of 0. When fifo status is between wmark1 and wmark, it generates a status of 2. When fifo status is below wmark, it generates a status of 3. The fifo status is indicated by the blue color. When the FIFO is full, its fifo status is 0. The two wmark levels are shown below:



Bit	Description
31:24	Reserved: MBZ
23:16	**Display Sprite B FIFO Watermark1:** Number in 64Bs of space in FIFO above which the Display Sprite B Stream will generate request with status 2
15:14	Reserved: MBZ
13:8	**Reserved**

7:0	**Display Sprite A FIFO Watermark1**: Number in 64Bs of space in FIFO above which the Display Sprite A Stream will generate request with status 2 (Value should be as recommended in the high priority bandwidth analysis spreadsheet).

FW5—Display FIFO Watermark1 Control 5

Memory Offset Address: 70074h

Default Value: 04040404h

Normal Access: Read/Write

These control values only apply to high resolution (non-VGA) modes of operation. The hardware depends on these registers being set properly since it is possible to set the watermarks to states causing starvation of the sync FIFO. These values control the second watermark level.

Bit	Description
31:24	**Display B FIFO Watermark1:** Number in 64Bs of space in FIFO above which the Display B Stream will generate request with status 2
23:16	**Display A FIFO Watermark1:** Number in 64Bs of space in FIFO above which the Display A Stream will generate request with status 2
15:14	Reserved: MBZ
13:8	**Reserved**
7:6	Reserved: MBZ
5:0	**CursorFIFO Self Refresh Watermark1:** Number in 64Bs of space in FIFO above which the Display Cursor Stream will generate request with status 2 during memory SR (Value should be as recommended in the high priority bandwidth analysis spreadsheet).

FW6—Display FIFO Watermark1 Control 6

Memory Offset Address: 70078h

Default Value: 00000078h

Normal Access: Read/Write

These control values only apply to high resolution (non-VGA) modes of operation. The hardware depends on these registers being set properly since it is possible to set the watermarks to states causing starvation of the sync FIFO. These values control the second watermark level.

Bit	Description

31:9	Reserved: MBZ
8:0	**Display FIFO Self Refresh Watermark1:** Number in 64Bs of space in FIFO above which the Display A/B Streamer will generate request with status 2 during max fifo mode (Value should be as recommended in the high priority bandwidth analysis spreadsheet).

FW7-Display FIFO Watermark Control 7

Memory Offset Address: 7007Ch

Default Value: 040f040fh

Normal Access: Read/Write

These control values only apply to high resolution (non-VGA) modes of operation. The hardware depends on these registers being set properly since it is possible to set the watermarks to states causing starvation of the sync FIFO. These values control the second watermark level. For each FIFO, there are two watermarks, wmark1 and wmark. When fifo status is above wmark1, hardware generates a status of 0. When fifo status is between wmark1 and wmark, it generates a status of 2. When fifo status is below wmark, it generates a status of 3. The fifo status is indicated by the blue color. When the FIFO is full, its fifo status is 0. The two wmark levels are shown below:

Bit	Description
31:24	**Display Sprite D FIFO Watermark1:** Number in 64Bs of space in FIFO above which the Display Sprite D Stream will generate request with status 2
23:16	**Display Sprite D FIFO Watermark:** Number in 64Bs of space in FIFO above which the Display Sprite D Stream will generate request with status 2
15:8	**Display Sprite C FIFO Watermark1**. Number in 64Bs of space in FIFO above which the Display Sprite C Stream will generate request with status 2
7:0	**Display Sprite C FIFO Watermark**. Number in 64Bs of space in FIFO above which the Display Sprite C Stream will generate request with status 2

DDL1 - Display FIFO Drain Latency 1

Memory Offset Address: 70050h

Default Value: 00000000h

Normal Access: Read/Write

For each plane, it has its associated programmable drain latency value. It is calculated based on the pixel drain rate and pixel size format. The plane display drain latency is a 7-bit value calculated using the following equation:

PROGRAMMABLE_DRAIN_LATENCY_REG[6:0] = TRUNC[(64 * PRECISION * 4)/(ACTUAL_DRAIN_RATE *BPP)

Actual drain rate depends on the pixel clock frequency.

BPP is the framebuffer pixel size format measured in bytes per pixel

Precision is either 32 or 64 and is used to maximize the programmable drain latency value to be fitted in a 7-bit count of 127

Bit	Description
31	Display Cursor A drain latency precision select: 1 – use 64 as precision multipler to increase precision to be stored in 7-bit Cursor A drain latency value 0 – use 32 as precision multipler to increase percision to be stored in 7-bit Cursor A drain latency value
30:24	Cursor A Drain Latency Value: For cursor latency, 4 BPP is assumed for all cursor formats. : Programmable drain latency value in time ticks per 64B FIFO entry
23	Display Sprite B drain latency precision select: 1 – use 64 as precision multipler to increase precision to be stored in 7-bit Sprite B drain latency value 0 – use 32 as precision multipler to increase percision to be stored in 7-bit Sprite B drain latency value
22:16	Sprite B Drain Latency Value: Programmable drain latency value in time ticks per 64B FIFO entry
15	Display Sprite A drain latency precision select: 1 – use 64 as precision multipler to increase precision to be stored in 7-bit Sprite A drain latency value 0 – use 32 as precision multipler to increase percision to be stored in 7-bit Sprite A drain latency value
14:8	Sprite A Drain Latency Value: Programmable drain latency value in time ticks per 64B FIFO entry
7	Display Plane A drain latency precision select: 1 – use 64 as precision multipler to increase precision to be stored in 7-bit Plane A drain

	latency value 0 – use 32 as precision multipler to increase percision to be stored in 7-bit Plane A drain latency value
6:0	Display plane A Drain Latency Value: Programmable drain latency value in time ticks per 64B FIFO entry

DDL2 - Display FIFO Drain Latency 2

Memory Offset Address: 70054h

Default Value: 00000000h

Normal Access: Read/Write

For each plane, it has its associated programmable drain latency value. It is calculated based on the pixel drain rate and pixel size format. The plane display drain latency is a 7-bit value calculated using the following equation:

PROGRAMMABLE_DRAIN_LATENCY_REG[6:0] = TRUNC[(64 * PRECISION * 4)/(ACTUAL_DRAIN_RATE *BPP)

Actual drain rate depends on the pixel clock frequency.

BPP is the framebuffer pixel size format measured in bytes per pixel

Precision is either 32 or 64 and is used to maximize the programmable drain latency value to be fitted in a 7-bit count of 127

Bit	Description
31	Display Cursor B drain latency precision select: 1 – use 64 as precision multipler to increase precision to be stored in 7-bit Cursor B drain latency value 0 – use 32 as precision multipler to increase percision to be stored in 7-bit Cursor B drain latency value
30:24	Cursor B Drain Latency Value: For cursor latency, 4 BPP is assumed for all cursor formats
23	Display Sprite D drain latency precision select: 1 – use 64 as precision multipler to increase precision to be stored in 7-bit Sprite D drain latency value 0 – use 32 as precision multipler to increase percision to be stored in 7-bit Sprite D drain latency value
22:16	Sprite D Drain Latency Value:

15	Display Sprite C drain latency precision select: 1 – use 64 as precision multipler to increase precision to be stored in 7-bit Sprite C drain latency value 0 – use 32 as precision multipler to increase percision to be stored in 7-bit Sprite C drain latency value
14:8	Sprite C Drain Latency Value:
7	Display Plane B drain latency precision select: 1 – use 64 as precision multipler to increase precision to be stored in 7-bit Plane B drain latency value 0 – use 32 as precision multipler to increase percision to be stored in 7-bit Plane B drain latency value
6:0	Display plane B Drain Latency Value:

DSPARB2—Display Arbitration Control 2

Memory Offset Address: 70060h

Default Value: 00001111h

Normal Access: Read/Write

Reset Value is for [32KB]

Notes: Each active display plane A, B, sprite A, B, C, D requires a FIFO to cover for memory latency. There are two FIFOs, one for each pipe. The FIFO all come from a single RAM that is divided into areas for each display plane, and 2 sprites. Plane A, and sprite A, B share one FIFO. Plane B, and sprite C, D share another FIFO. The amount of the RAM used by each display plane is defined by this register. The two fields in the register split the display RAM into three portions, allocated between display plane A, sprite A, B for pipe A, and display planeB, sprite C, D for pipe B. This register is double buffered and updated on the leading edge of Vertical Blank of the pipe. It takes effect on the next VBLANK for whichever pipe is currently active. Each display plane needs a minimum FIFO size that is at least MaxLatencyForPlane * PixelRate * PixelSize + 512. All values should be rounded up to the next unit of 64B.

Notes: A special C3 mode can occur when a single display (of Display A and Display B) is active and the overlay and Display C are disabled. In that mode, when C3 is entered, the values in the BSTART and CSTART fields are ignored and the entire RAM is allocated to the single active display plane.

Notes: The control granularity of FIFO size is 64-bytes and the total size of the RAM is 2048*16 bytes making TOTALSIZE equal to 512. The range of values for sprite ASTART and sprite BSTART is 0-511. Similarly, the range of values for sprite CSTART and sprite DSTART is 0-511.

Notes: [vlv-16KB setting] FIFO Sizes PA=128, SA=64, SB=64; PB=128, SC=64, SD=64

Notes: [vlv-32KB setting] FIFO Sizes PA=256, SA=128, SB=128; PB=256, SC=128, SD=128

Notes: The display dot clock frequency or pixel rate must not exceed 90% of the core display clock. When a primary plane is enabled with 64bpp format and sprite is also enabled on the same pipe, the dot clock frequency or pixel rate must be less than 80% of the core display clock.

DSPHOWM — Display FIFO WM High Order

Memory Offset Address: 70064h

Default Value: 00000000h

Normal Access: Read/Write

Bit	Descriptions
31:25	Reserved
24	**Display FIFO Self Refresh Watermark High Order**. This field is the high order bit for the SR WM pointer . Combined with the lower order 9-bit SR FIFO WM pointer, it forms a 10-bit SR FIFO WM pointer. This register defines the value of the watermark used by the Display streamer in case the CPU is in C2/C3/C4 and the memory has entered self refresh. Number in 64Bs of space in FIFO above which the Display Stream will generate requests to Memory.
23:21	Reserved
20	**Sprite D FIFO Watermark High Order:** This field is the high order bit for Sprite D FIFO WM. Combined with lower order 8-bit Sprite D FIFO WM, it forms a 9-bit Sprite D FIFO WM pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory.
19:17	Reserved
16	**Sprite C FIFO Watermark High Order:** This field is the high order bit for Sprite C FIFO WM. Combined with lower order 8-bit Sprite C FIFO WM, it forms a 9-bit Sprite C FIFO WM pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory.
15:13	Reserved
12	**Display Plane B FIFO Watermark High Order:** This field is the high order bit for Display B FIFO WM. Combined with lower order 8-bit Display B FIFO WM, it forms a 9-bit Display B FIFO WM pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory.
11:9	Reserved
8	**Sprite B FIFO Watermark High Order:** This field is the high order bit for Sprite B FIFO WM. Combined with lower order 8-bit Sprite B FIFO WM, it forms a 9-bit Sprite B FIFO WM pointer.

	Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory.
7:5	Reserved: MBZ
4	**Sprite A FIFO Watermark High Order:** This field is the high order bit for Sprite A FIFO WM. Combined with lower order 8-bit Sprite A FIFO WM, it forms a 9-bit Sprite A FIFO WM pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory.
3:1	Reserved: MBZ
0	**Display Plane A FIFO Watermark High Order:** This field is the high order bit for Display A FIFO WM. Combined with lower order 8-bit Display A FIFO WM, it forms a 9-bit Display A FIFO WM pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory.

DSPHOWM1 — Display FIFO WM1 High Order

Memory Offset Address: 70068h

Default Value: 00000000h

Normal Access: Read/Write

Bit	Descriptions
31:25	Reserved
24	**Display FIFO Self Refresh Watermark1 High Order**. This field is the high order bit for the SR WM1 pointer . Combined with the lower order 9-bit SR FIFO WM1 pointer, it forms a 10-bit SR FIFO WM1 pointer. This register defines the value of the watermark used by the Display streamer in case the CPU is in C2/C3/C4 and the memory has entered self refresh. Number in 64Bs of space in FIFO above which the Display Stream will generate requests to Memory.
23:21	Reserved
20	**Sprite D FIFO Watermark1 High Order:** This field is the high order bit for Sprite D FIFO WM1. Combined with lower order 8-bit Sprite D FIFO WM1, it forms a 9-bit Sprite D FIFO WM1 pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory.
19:17	Reserved
16	**Sprite C FIFO Watermark1 High Order:** This field is the high order bit for Sprite C FIFO WM1. Combined with lower order 8-bit Sprite C FIFO WM1, it forms a 9-bit Sprite C FIFO WM1 pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory.
15:13	Reserved
12	**Display Plane B FIFO Watermark1 High Order:** This field is the high order bit for Display B FIFO WM1. Combined with lower order 8-bit Display B FIFO WM1, it forms a 9-bit Display B FIFO WM1 pointer. Number in 64Bs of space in FIFO above which the Display A Stream will

	generate requests to Memory.
11:9	Reserved
8	**Sprite B FIFO Watermark1 High Order:** This field is the high order bit for Sprite B FIFO WM1. Combined with lower order 8-bit Sprite B FIFO WM1, it forms a 9-bit Sprite B FIFO WM1 pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory.
7:5	Reserved: MBZ
4	**Sprite A FIFO Watermark1 High Order:** This field is the high order bit for Sprite A FIFO WM1. Combined with lower order 8-bit Sprite A FIFO WM1, it forms a 9-bit Sprite A FIFO WM1 pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory.
3:1	Reserved: MBZ
0	**Display Plane A FIFO Watermark1 High Order:** This field is the high order bit for Display A FIFO WM1. Combined with lower order 8-bit Display A FIFO WM1, it forms a 9-bit Display A FIFO WM1 pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory.

PipeAFrameCOUNT— Pipe A Frame Counter

Memory Offset Address: 70040h

Default Value: 00000000h

Normal Access: Read Only

Requires that this pipe's PLL is running

Bit	Descriptions
31:0	**Pipe A Frame Count**. Provides read back of the display pipe frame counter. This counter increments on every start of vertical blank and rolls over back to 0 after 2^32 frames.

PipeAFLIPCOUNT— Pipe A Flip Counter

Memory Offset Address: 70044h

Default Value: 00000000h

Normal Access: Read Only

Requires that this pipe's PLL be running

Bit	Descriptions
31:0	**Pipe A Flip Counter** Provides read back of the display pipe flip counter. This counter increments on each flip of the surface of the primary plane on this pipe. This includes command streamer asynchronous and synchronous flips and any MMIO writes to the primary plane surface

	address. It rolls over back to 0 after 2^32 flips.

Cursor A Plane Control Registers

The hardware cursor registers are memory mapped and accessible through 32 bit, 16 bit, or 8 bit accesses. They are all double-buffered, including the palette registers. Writes to cursor registers are performed to a holding register. The actual register update will occur based on the associated pipe's Vertical Blank signal only after a write cycle to the base address register (setting the trigger) has occurred. Writes to any register other than the trigger register will disable an active trigger if that occurs before the vertical blank.

CURACNTR—Cursor A Control Register

Memory Offset Address: 70080h

Default Value: 00000000h

Normal Access: Read/Write

This register, and all other cursor registers will remain in their holding register (readable) after a write. The holding registers are transferred into the active registers on the asserting edge of Vertical Blank only after a write cycle to the base address register has completed.

Bit	Description
31:30	**Reserved:** Write as zero.
29:28	**Reserved: Write as zero.**
27	**Reserved**
26	**Cursor Gamma Enable:** This bit only has an effect when using the cursor in a non-VGA mode. In VGA pop-up operation, the cursor data will always bypass the gamma (palette) unit. 0 = Cursor pixel data bypasses gamma correction or palette (default). 1 = Cursor pixel data is gamma to be corrected in the pipe.
25:16	**Reserved:** Write as zero
15	**180° Rotation:** This mode causes the cursor to be rotated 180°. In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image. Only 32 bits per pixel cursors can be rotated. This field must be zero when the cursor format is 2 bits per pixel. 0 = No rotation 1 = 180° Rotation of 32 bit per pixel cursors
14:6	**Reserved**
5	Cursor Mode Select bit: See following table.
4	**Reserved**
3	**Reserved**
2:0	**Cursor Mode Select:** These three bits together with bit 5 select the mode for cursor as shown in the following table.

CURABASE—Cursor A Base Address Register

Memory Offset Address: 70084h

Default Value: 00000000h

Normal Access: Read/Write

This register specifies the graphics memory address at which the cursor image data is located. Writes to this register acts like a trigger that enables atomic updates of the cursor registers. When updating the cursor registers, this register should be written last in the sequence. This register should be written even if the actual contents did not change to allow the holding registers to move to the active registers on the next VBLANK.

For legacy cursor modes, this register is sufficient to specify the address of the entire cursor. For ARGB modes, this register specifies the address of the first page of the cursor data.

Bit	Description
31:6	**Cursor Base Address**. This field specifies bits 31:6 of the graphics address of the base of the cursor. Popup cursor mode is selected within the CURACNTR register. The cursor surface address must be 4K byte aligned. The cursor must be in linear memory, it cannot be tiled. When performing 180° rotation, this offset must be the difference between the last pixel of the last line of the cursor data in its unrotated orientation and the cursor surface address. A write to this register also acts as a trigger event to force the update of active registers from the staging registers on the next display event. Each cursor register is double-buffered. The CPU writes to a set of holding registers. The active registers are updated from the holding registers following the leading edge of the vertical blank pulse. The update is postponed until the next vblank if a write cycle is active to any of the cursor registers at the time of the vblank. The update is also postponed if a write sequence is in progress. It is assumed that if the cursor mode is changed, the cursor image will also be changed. To prevent the cursor from appearing when it is only partially programmed, the active registers will not be updated until both the cursor control and base address registers have been programmed. If the cursor control register is written, the cursor base address must also be written before the change will be effective. However, the base address register may be changed (e.g., to change the shape of the cursor) without also writing to the control register. If both are to be written, the control register must be written first.
5	**Reserved: MBZ**
4	**Reserved**
3:0	**Reserved**

CURAPOS—Cursor A Position Register

Memory Offset Address: 70088h

Default Value: 00000000h

Normal Access: Read/Write

This register specifies the screen position of the cursor. The origin of the cursor position is always the upper left corner of the active image for the display pipe that the cursor is assigned. This register can be loaded atomically (requires that the base address be written) and is double buffered.

Bit	Description
31	**Cursor Y-Position Sign Bit:** This bit provides the sign bit of a signed 13-bit value that specifies the horizontal position of cursor. (default is 0). For normal high resolution display modes, the cursor must have at least a single pixel positioned over the active screen. For use as a VGA Popup, the entire cursor must be positioned over the active area of the VGA image.
30:28	**Reserved:** Write as zero.
27:16	**Cursor Y-Position Magnitude Bits 11:0:** This register provides the magnitude bits of a signed 12-bit value that specifies the vertical position of cursor. The sign bit of this value is provided by bit 31of this register. (default is 0). For use as a VGA Popup, the entire cursor must be positioned over the active area of the VGA image. Enabling the border in VGA (VGA Border Enable bit in the VGA sliip register) includes the border in what is considered the “active area”. For HDMI modes where the vertical zoom is greater than 1x, the position is specified using the zoomed grid. When performing 180° rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation.
15	**Cursor X-Position Sign Bit:** This bit provides the sign bit of a signed 13-bit value that specifies the horizontal position of cursor. (default is 0).). For normal high resolution display modes, the cursor must have at least a single pixel positioned over the active screen. For use as a VGA Popup, the entire cursor must be positioned over the active area of the VGA image. Enabling the border in VGA (VGA Border Enable bit in the VGA Config register) includes the border in what is considered the “active area”.
14:12	**Reserved:** Write as zero.
11:0	**Cursor X-Position Magnitude Bits 11:0:** These 12 bits provide the signed 13-bit value that specifies the horizontal position of cursor. The sign bit is provided by bit 15 of this register. (default is 0) For HDMI modes where the horizontal zoom is greater than 1x, the position is specified using the zoomed grid. When performing 180° rotation, this field specifies the horizontal position of the lower right

	corner relative to the end of the active video area in the unrotated orientation.

CURALIVEBASE—Cursor A Live Base Address Register

Memory Offset Address: 700ACh

Default Value: 00000000h

Normal Access: Read Only

Bit	Description
31:6	**Cursor A Live Base Address** This gives the live value of the surface base address as being currently used for the plane.
5	Reserved: MBZ
4	**Reserved**
3:0	**Reserved**

CURAPALET[0:3]—Cursor A Palette registers (4 Registers)

Memory Offset Address: 70090–7009Fh

CURAPALET0: 70090–70093h

CURAPALET1: 70094–70097h

CURAPALET2: 70098–7009Bh

CURAPALET3: 7009C–7009Fh

Default Value: 00000000h

Normal Access: Read/Write

These palette registers can be accessed through this MMIO interface register locations combined with an enable bit. This is the preferred method. The cursor palette provides color information when using one of the indexed modes. The two-bit index selects one of the four colors or two of the colors when in the AND/XOR cursor mode. The cursor palette provides color information when using one of the indexed modes. The two-bit index selects one of the four colors or two of the colors when in the AND/XOR cursor mode.

Bit	Descriptions
31:24	**Reserved:** Write as zero.
23:16	**Red or Y Value:** These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the Y and excess 128 notation for the UV values. The

	data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
15:8	Green or U Value:
7:0	Blue or V Value:

The table below describes the palette usage for different cursor modes and indexes.

Index	2 color	3color	4color
00	palette 0	palette 0	palette 0
01	palette 1	palette 1	palette 1
10	transparent	Transparent	palette 2
11	invert destination	palette 3	palette 3

Cursor B Plane Control Registers

CURBCNTR—Cursor B Control Register

Memory Offset Address: 700C0h

Default Value: 00000000h

Normal Access: Read/Write

The hardware cursor registers are memory mapped and accessible through 32 bit, 16 bit, or 8 bit accesses. They are all, including the palette registers double buffered. Writes to cursor registers are done to a holding register. The actual register update will occur based on the assigned pipes VBLANK. It is recommended that the base register be accessed through a 32-bit write only. To update all cursor registers atomically, a sequence that ends with a base address register write should be used.

Bit	Descriptions
31:30	**Reserved:** Write as zero.
29:28	**Reserved**
27	**Reserved:** Write as zero.
26	Cursor Gamma Enable: 0 = Cursor pixel data bypasses gamma correction (default). 1 = Cursor pixel data is gamma to be corrected.

25:16	Reserved:
15	**180° Rotation:** This mode causes the cursor to be rotated 180°. In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image. Only 32 bits per pixel cursors can be rotated. This field must be zero when the cursor format is 2 bits per pixel. 0 = No rotation 1 = 180° Rotation of 32 bit per pixel cursors
14:6	**Reserved:** Write as zero
5	Cursor Mode Select bit: See following table.
4:3	Reserved:
2:0	**Cursor Mode Select:** These three bits together with bit 5 select the mode for cursor as shown in the following table.

CURBBASE—Cursor B Base Address Register

Memory Offset Address: 700C4h

Default Value: 00000000h

Normal Access: Read/Write

This register specifies the memory address at which the cursor data is located. Writes to this register should be done with 32-bit accesses and acts as a trigger to atomically update the cursor register set. For legacy cursor modes, this register is sufficient to specify the address of the entire cursor. The address is the graphics address. For ARGB modes, this register specifies the address of the first page of the cursor data.

Bit	Description
31:6	**Cursor Base Address:** This register specifies the graphics address of the entire cursor. It also acts as a trigger event to force the update of active registers on the next display event. The cursor surface address must be 4K byte aligned. The cursor must be in linear memory, it cannot be tiled. When performing 180° rotation, this offset must be the difference between the last pixel of the last line of the cursor data in its unrotated orientation and the cursor surface address. A write to this register also acts as a trigger event to force the update of active registers from the staging registers on the next display event. Each cursor register is double-buffered. The CPU writes to a set of holding registers. The active registers are updated from the holding registers following the leading edge of the vertical blank pulse. The update is postponed until the next vblank if a write cycle is active to any of the cursor registers at the time of the vblank. The update

	is also postponed if a write sequence is in progress. It is assumed that if the cursor mode is changed, the cursor image will also be changed. To prevent the cursor from appearing when it is only partially programmed, the active registers will not be updated until both the cursor control and base address registers have been programmed. If the cursor control register is written, the cursor base address must also be written before the change will be effective. However, the base address register may be changed (e.g., to change the shape of the cursor) without also writing to the control register. If both are to be written, the control register must be written first.
5	Reserved: MBZ
4	**Reserved**
3:0	**Reserved**

CURBPOS—Cursor B Position Register

Memory Offset Address: 700C8h

Default Value: 00000000h

Normal Access: Read/Write

This register specifies the screen position of the cursor. The origin of the cursor position is always the upper left corner of the active image for the display pipe that the cursor is assigned. This register can be loaded atomically and is double buffered. The load register is transferred into the active register on the leading edge of Vertical Blank of the pipe cursor is currently assigned after the trigger has been set.

Bit	Descriptions
31	**Cursor Y-Position Sign Bit:** This bit provides the sign bit of a signed 13-bit value that specifies the horizontal position of cursor. (default is 0).). For normal high resolution display modes, the cursor must have at least a single pixel positioned over the active screen.
30:28	**Reserved:** Write as zero.
27:16	**Cursor Y-Position Magnitude Bits 11:0:** This register provides the magnitude bits of a signed 13-bit value that specifies the vertical position of cursor. The sign bit of this value is provided by bit 31of this register. (default is 0) When performing 180° rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation.
15	**Cursor X-Position Sign Bit:** This bit provides the sign bit of a signed 13-bit value that specifies the horizontal position of cursor. (default is 0).). For normal high resolution display modes, the cursor must have at least a single pixel positioned over the active screen.

	For HDMI modes where the vertical zoom is greater than 1x, the position is specified using the zoomed grid.
14:12	**Reserved:** Write as zero.
11:0	**Cursor X-Position Magnitude Bits 11:0:** These 12 bits provide the signed 13-bit value that specifies the horizontal position of cursor. The sign bit is provided by bit 15 of this register. (default is 0) For HDMI modes where the horizontal zoom is greater than 1x, the position is specified using the zoomed grid. When performing 180° rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation.

CURBLIVEBASE—Cursor B Live Base Address Register

Memory Offset Address: 700ECh

Default Value: 00000000h

Normal Access: Read Only

Bit	Description
31:6	**Cursor B Live Base Address:** This gives the live value of the surface base address as being currently used for Cursor B plane.
5	Reserved: MBZ
4	**Reserved**
3:0	**Reserved**

CURB PALET[0:3]—Cursor B Palette registers (4 Registers)

Memory Offset Address: 700D0–700DCh

CURBPALET0: 700D0–700D3h

CURBPALET1: 700D4–700D7h

CURBPALET2: 700D8–700DBh

CURBPALET3: 700DC–700DFh

Default Value: 00000000h

Normal Access: Read/Write

These palette registers can be accessed through this MMIO interface or through a legacy mode using the VGA palette register locations combined with an enable bit. This is the preferred method. The cursor palette provides color information when using one of the indexed modes. In the two-bit

AND/XOR cursor modes, the two-bit index selects one of the four colors or two of the colors when in the mode. RGB data is full range unsigned numbers. YUV data will be unsigned for the Y and excess 128 notation for the UV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.

Bit	Descriptions
31:24	**Reserved:** Write as zero.
23:16	Red or Y:
15:8	Green or U Value:
7:0	Blue or V Value:

Display Pipeline B

PIPEB_DSL—Display Scan Line

Memory Address Offset: 71000h

Default Value: 00h

Normal Access: Read only

This register enables the read back of the display pipe vertical "line counter". The display line value is from the display pipe B timing generator and is reset to zero at the beginning of a scan. The value increments at the leading edge of HSYNC and can be safely read any time. For normal operation, scan line zero is the first active line of the display. When in VGA centering mode, the scan line 0 is the 1st active scan line of the pseudo border not the centered active VGA image display area. In interlaced display timings, the scan line counter provides the current line in the field. One field will have a total number of lines that is one greater than the other field.

Programming Note: In order to cause the scan line logic to report the correct Line Counter value, the corresponding Display Pipeline timing registers must be programmed to valid, non-zero (e.g., 640x480 @ 60Hz) values before enabling the Pipe or programming VGA timing and enabling native VGA.

Bit	Description
31	**Current Field:** Provides read back of the current field being displayed on display pipe B. Non-TV mode: 0 = first field (odd field) 1 = second field (even field) TV mode:

	1 = first field (odd field) 0 = second field (even field)
30:13	**Reserved:** Read only.
12: 0	**Pipe B Display Line Counter:** This register enables the read back of the display vertical "line counter". The display line values are from the pipe B timing generator. They change at the leading edge of HSYNC, and can be safely read at any time.

PIPEB_SLC—Pipe B Display Scan Line Range Compare Register

Memory Address Offset:71004h

Default Value: 00h

Normal Access: Read/Write

The Start and End Line Count Compare registers are compared with the display line values from the timing generator. They change at the leading edge of HSYNC. They can safely be accessed at any time. The End compare register operator is a less than or equal, while the Start compare register operator is a greater than or equal. The results of these 2 comparisons are communicated to the command stream controller for generating interrupts, status, and command stream flow control ("wait for within range" and "wait for not within range").

For range check, the value programmed should be the desired value - 1. So for line 0, the value programmed is VTOTAL and for line 1, the value programmed is 0.

This register can be written via the command stream processor using the MI_LOAD_SCAN_LINES_INCL or MI_LOAD_SCAN_LINES_EXCL commands.

Bit	Description
31	Inclusive/Exclusive: 1 = Inclusive Within Range,0 = Exclusive Out of Range
30: 29	**Reserved:** Read only.
28:16	**Start Scan Line Number:** This field specifies the starting scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0,Display Buffer height in lines-1].
15:13	**Reserved:** Read only.
12:0	**End Scan Line Number:** This field specifies the ending scan line number of the Scan Line

	Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0, Display Buffer height in lines-1].

PIPEBCONF—Pipe B Configuration Register

Memory Offset Address: 71008h

Default Value: 00000000h

Normal Access: Read/Write double buffered

Bit	Descriptions
31	**Pipe B Enable:** Setting this bit to the value of one, turns on pipe B. This must be done before any planes are enabled on this pipe. Changing it to a zero should only be done when all planes that are assigned to this pipe have been disabled. Turning the pipe enable bit off disables the timing generator in this pipe. Plane disable occurs after the next VBLANK event after the plane is disabled. Synchronization pulses to the display are not maintained if the timing generator is disabled. Power consumption will be at its lowest state when disabled. A separate bit controls the DPLL enable for this pipe. Pipe timing registers should contain valid values before this bit is enabled. Disabling the Pipe and changing the timing registers and re-enabling the pipe before the next VBLANK will cause the mode change to occur at the end of the current frame. This requires no wait on the software's part. On the other hand, if this is the disabling of the pipe, that does require a software wait for VBLANK to occur. Synchronization pulses to the display are not maintained if the timing generator is disabled. Power consumption is at it's lowest state. 1 = Enable 0 = Disable
30	**Pipe State:** This bit indicates the actual state of the pipe. Since there can be some delay between disabling the pipe and the pipe actually shutting off, this bit indicates the true current state of the pipe. 0 = Disabled1 = Enabled AccessType: Read Only
29	**Reserved:** Write as zero.
28:27	**Reserved**
26	**Display Port Audio Only Mode:** Setting this bit to 1 indicates the DisplayPort will output

	audio only. 0 = DisplayPort will output Video or Video and Audio 1 = DisplayPort will output Audio only
25	**Reserved**
24	**Pipe B Gamma Unit Mode**. This bit selects which mode the pipe gamma correction logic works in. In the palette mode, it behaves as a 3X256x8 RAM lookup. VGA and indexed mode operation should use the palette in 8-bit mode. In the 10-bit gamma mode, it will act as a piecewise linear interpolation. Other gamma units such as in the overlay and sprite are unaffected by this bit. 0 = 8-bit Palette Mode 1 = 10-bit Gamma Mode
23:21	Interlaced Mode These bits are used for software control of interlaced behavior. They are updated immediately if the pipe is off, or in the vertical blank after programming if pipe is enabled. 0xx = Progressive 100 = Interlaced embedded panel using programmable vertical sync shift (2x) 101 = Interlaced using vertical sync shift. Backup option to setting 110. (2x)110 = Interlaced with VSYNC/HSYNC Field Indication using legacy vertical sync shift. 111 = Interlaced with Field 0 Only using legacy vertical sync shift. Not used. Note: VGA display modes and Panel fitting do not work while in interlaced modes Setting the Interlaced embedded panel mode causes hardware to automatically modify the output to match the specifications of panels that support interlaced mode.
20	**MIPI Display Self-refresh mode for MIPI B:** 0 = Normal Operation, display controller generate timing and refresh display panel at refresh rate 1 = Display self-refresh mode. Display controller update frame buffer in display module on demand only
19	**Display/Overlay Planes Off**. This bit when set will cause all enabled Display and overlay planes that are assigned to this pipe to be disabled by overriding the current setting of the plane enable bit, at the next VBLANK. Timing signals continue as they were but the screen becomes blank. Setting the bit back to a zero will then allow the display and overlay planes to resume on the following VBLANK. 0 = Normal Operation 1 = Planes assigned to this pipe are disabled.

18	**Cursor Planes Off**. This bit when set will cause all enabled cursor planes that are assigned to this pipe to be disabled by overriding the current setting of the plane enable bit, at the next VBLANK. Timing signals continue as they were but the screen becomes blank. Setting the bit back to a zero will then allow the cursor planes to resume on the following VBLANK. 0 = Normal Operation 1 = Planes assigned to this pipe are disabled.
17:16	Refresh Rate CxSR Mode Association These bits select how refresh rates are tied to CxSR on pipe B. When they are set to anything other than 00, bits 23:21 of this register must be programmed to 0xx. Switching between 01 and 10 settings directly is not allowed. Software must program this field to 00 before switching. Software is responsible for enabling this mode only for integrated dispay panels that support corresponding mode. 00 – **Default** – no dynamic refresh rate change enabled. Software control only. 01 – Progressive-to-progressive refresh rate change enabled and tied to CxSR. Pixel clock values set in FPB0/FPB1 settings in the DPLLB control register and FPB0/FPB1 divider registers. 10 – Progressive-to-interlaced refresh rate change enabled and tied to CxSR. Pixel clock value does not change in this case. Scaling must be disabled in this mode. Uses programmable VS shift 11 – Reserved
15	Color Correction Matrix Enable on Pipe B: 1 = Color Correction Coefficients are enabled to perform color correction 0 = Color Correction Coefficients are disabled
14	**DisplayPort Power Mode Switch :** This bit selects the software controlled progressive to progressive power saving mode (software controlled DRRS). Hardware Controlled Refresh Rate Select must be disabled when enabling this. Link and data M/N 1 values are used for normal settings, M/N 2 values are used for low power settings. 0 – Normal progressive refresh rate (default) 1 – Low Power progressive refresh rate
13	Reserved **Color Range Select: :** This bit is used to select the color range of RBG outputs. 0 = Apply full 0-255 color range to the output **(Default)** 1 = Apply 16-235 color range to the output
12	**Reserved**

11:10	**Reserved**
9:8	**Reserved: MBZ**
7:5	**Bits Per Color: :** This field selects the number of bits per color sent to a receiver device connected to this port. Color format takes place on the Vblank after being written. Color format change can be done independent of a pixel clock change. Selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer results in dithering the output stream. For further details on Display Port fixed frequency programming to accommodate these formats refer to “DP Frequency Programming” in DPLL section of Bspec. 000 = 8 bits per color **(Default)** 001 = 10 bits per color 010 = 6 bits per color 011 = RESERVED 1xx = RESERVED
4	**Dithering enable:** This bit enables dithering for DisplayPort 6bpc or 8bpc modes **0 –** Dithering disabled (Default) **1 –** Dithering enabled Programming Note: Dithering should only be enabled for 8bpc or 6bpc.
3:2	**Dithering type:** This bit selects dithering type for DisplayPort 6bpc or 8bpc modes **00 -** Spatial only (default) **01-** Spatio-Temporal 1 **10-** Reserved **11-** Reserved
1	**Reserved**
0	**Reserved: Write as zero**

PIPEBGCMAXRED—Pipe B Gamma Correction Max Red

Memory Offset Address: 71010h

Default Value: 00010000h

Normal Access: Read/Write

Bit	Descriptions
31:17	Reserved
16:0	**Max Red Gamma Correction Point**. 129th reference point for red channel of the pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 1024.0. Format: 11.6 Default: 0x10000

PIPEBGCMAXGREEN—Pipe B Gamma Correction Max Green

Memory Offset Address: 71014h

Default Value: 00010000h

Normal Access: Read/Write

Bit	Descriptions
31:17	Reserved
16:0	**Max Green Gamma Correction Point**. 129th reference point for green channel of the pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 1024.0. Format: 11.6 Default: 0x10000

PIPEBGCMAXBLUE—Pipe B Gamma Correction Max Blue

Memory Offset Address: 71018h

Default Value: 00010000h

Normal Access: Read/Write

Bit	Descriptions
31:17	Reserved
16:0	**Max Blue Gamma Correction Point**. 129th reference point for blue channel of the pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 1024.0. Format: 11.6 Default: 0x10000

PIPEBSTAT—Pipe B Status

Memory Offset Address: 71024h

Default Value: 00000000h

Normal Access: Read/Write

Programming:

Prior to clearing a Display Pipe-sourced interrupt (e.g., Display Pipe A VBLANK) in the IIR, the corresponding interrupt (source) status in the PIPEASTAT or PIPEBSTAT register (e.g., Pipe A VBLANK Interrupt Status bit of PIPEASTAT) must first be cleared. Note that clearing these status bits requires writing a '1' to the appropriate bit position.

Bit	Descriptions
31	**Pipe B Underflow Status:** This bit is set when an underflow occurs at the display pipe B. It is cleared by writing a one to this bit. This event will occur naturally during mode changes, to be effective, it should be cleared after a mode change. This bit is only valid after Pipe B has been completely configured. 1 = FIFO B Underflow occurred 0 = FIFO B Underflow did not occur AccessType: One to Clear
30	**Sprite D Flip Done Interrupt Enable:** This will enable the consideration of the Sprite D flip done interrupt status bit in the first line interrupt logic 0 = Sprite D Flip Done Interrupt Disabled 1 = Sprite D Flip Done Interrupt Enabled
29	**Reserved**
28	**Reserved**
27	Performance Counter2 Interrupt Enable: This bit enables the second performance counter interrupt. 0 = Second Performance Counter2 Interrupt Status Disabled 1 = Second Performance Counter2 interrupt Status Enabled
26	**Plane B Flip Done Interrupt Enable:** This will enable the consideration of the Plane B flip done interrupt status bit in the first line interrupt logic 0 = Plane B flip done Interrupt/Status Disabled 1 = Plane B flip done Interrupt/Status Enabled
25	Vertical Sync Interrupt Enable:

	0 = Vertical Sync Interrupt/Status Disabled 1 = Vertical Sync Interrupt/Status Enabled
24	Display Line Compare Enable: 0 = Pipe B Display Line Compare Status Report Disabled 1 = Pipe B Display Line Compare Status report Enabled
23	**BLM Event Enable:** This interrupt is generated by the image brightness segment comparators. Which segment cause an interrupt are controlled by the BLM Histogram control register. 0 = No BLM event enabled 1 = BLM event enabled
22	**Sprite C Flip Done Interrupt Enable:** This will enable the consideration of the Sprite C flip done interrupt status bit in the first line interrupt logic 0 = Sprite C Flip Done Interrupt Disabled 1 = Sprite C Flip Done Interrupt Enabled
21	**Odd Field Interrupt Event Enable**. This bit should only be used when this pipe is in an interlaced display timing. 0 = Odd Field Event disable 1 = Odd Field Event enable
20	**Even Field Interrupt Event Enable**. This bit should only be used when this pipe is in an interlaced display timing. 0 = Even field Event disable 1 = Even field Event enable
19	Panel Self Refresh (PSR) Interrupt Enable on Pipe B: 0 = PSR interrupt Disabled on Pipe B 1 = PSR Interrupt Enabled on Pipe B
18	**Start of Vertical Blank Interrupt Enable:** This will enable the consideration of the start of vertical blank interrupt status bit in the first line interrupt/status logic. 0 = Start of Vertical Blank Interrupt/Status Disabled 1 = Start of Vertical Blank Interrupt/Status Enabled
17	**Pipe B Framestart Interrupt Enable:** This will enable the consideration of the vertical blank interrupt status bit in the first line interrupt/status logic. 0 = Pipe B Framestart Interrupt/Status Disabled

	1 = Pipe B Framestart Interrupt/Status Enabled
16	**Pipe B Horizontal Blank Interrupt Enable**: This will enable the consideration of the start of horizontal blank interrupt status bit in the first line interrupt/status logic 0 = Start of Horizontal Blank Interrupt/Status Disabled 1 = Start of Horizontal Blank Interrupt/Status Enabled
15	**Sprite D Flip Done Interrupt Status:** MMIO Flip Event is completed on Sprite D 0 = Sprite D Flip Not Done 1 = Sprite D Flip Done AccessType: One to Clear
14	**Sprite C Flip Done Interrupt Status:** MMIO Flip Event is completed on Sprite C 0 = Sprite C Flip Not Done 1 = Sprite C Flip Done AccessType: One to Clear
13	**Reserved**
12	**Reserved**
11	**Second Performance Counter2 Interrupt Status:** This bit is set when the second performance counter2 generates an interrupt. It is cleared by a write of a one. 0 = Second performance counter interrupt event not asserted 1 = Second performance counter interrtup event asserted AccessType: One to Clear
10	**Plane B Flip Done Interrupt Status:** Async/Sync Flip Event is completed on Display Plane B 0 = Plane B Flip Not Done 1 = Plane B Flip Done AccessType: One to Clear
9	Pipe B Vertical Sync Status: 0 = Vertical Sync not asserted 1 = Vertical Sync asserted AccessType: One to Clear
8	**Pipe B Display Line Compare Status:** This bit is cleared when a write to this register occurs with this bit as a one. Writes with this bit as a zero has no effect on the value of the bit.

	0 = Display Line Compare Status not asserted 1 = Display Line Compare Status asserted AccessType: One to Clear
7	**BLM Image Brightness Status:** This bit is cleared when a write to this register occurs with this bit as a one. Writes with this bit as a zero has no effect on the value of the bit. 0 =DPST Interrupt has not occurred on pipe B 1 = DPST Interrupt has occurred on pipe B AccessType: One to Clear
6	Reserved: MBZ
5	**Odd Field Interrupt Status**. This status bit will be set on a Odd field VBLANK event. This bit should only be used when this pipe is in an interlaced display timing. For synchronization with register updates, the actual event will occur one line after the start of VBLANK. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. Note: This bit will not be set when pipe is in "Interlaced with Field 0 Only using legacy vertical sync shift" mode. 0 = Odd Field Vertical Blank has not occurred 1 = Odd Field Vertical Blank has occurred AccessType: One to Clear
4	**Even Field Interrupt Status**. This status bit will be set on a even filed VBLANK event. This bit should only be used when this pipe is in an interlaced display timing. For synchronization with register updates, the actual event will occur one line after the start of VBLANK. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. Note: This bit will not be set when pipe is in "Interlaced with Field 0 Only using legacy vertical sync shift" mode. 0 = Even Field Vertical Blank has not occurred 1 = Even Field Vertical Blank has occurred AccessType: One to Clear
3	**Pipe B Panel Self Refresh Status:** This bit indicates interrupt is generated by the PSR controller and intends to send interrupt to SW driver when the PSR interrupt enable bit (70028h bit 22) is set. This is cleared when a write to this register occurs with this bit as a one. Write with this bit as a zero has no effect on the value of the bit. 0 = PSR Interrupt has not occurred on pipe B

	1 = PSR interrupt has occurred on pipe B AccessType: One to Clear
2	**Start of Vertical Blank Interrupt Status:** This status bit will be set at the beginning of a VBLANK event. At this point, the double buffered display registers flip, taking their new values. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. In MIPI DSR mode, GPIO TE trigger sets the Vblank Interrupt status 0 = Start of Vertical Blank has not occurred 1 = Start of Vertical Blank has occurred AccessType: One to Clear
1	**Pipe B Framestart Interrupt Status:** This status bit will be set on a VBLANK event, when the frame start occurs. The display registers are updated at the start of vertical blank, but the new register data is not utilized by the display pipeline until the point in the vertical blank period when the frame start occurs, which is the event that triggers this bit. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. 0 = Pipe B Framestart Status has not occurred 1 = Pipe B Framestart Status has occurred AccessType: One to Clear
0	Pipe B Horizontal Blank Status: 0 = Pipe B Horizontal Blank has not occurred 1 = Pipe B Horizontal Blank has occurred AccessType: One to Clear

PipeBFrameCount— Pipe B Frame Counter

Memory Offset Address: 71040h

Default Value: 00000000h

Normal Access: Read Only

Bit	Descriptions
31:0	Pipe B Frame Count See PipeAFrameCount description.

PipeBFlipCount — Pipe B Flip Counter

Memory Offset Address: 71044h

Default Value: 00000000h

Normal Access: Read Only

Bit	Descriptions
31:0	Pipe B Flip Count. See PipeAFlipCount description.

PipeBMSAMISC— Pipe B MSA MISC

Memory Offset Address: 71048h

Default Value: 00000000h

Normal Access: Read/Write

Bit	Descriptions
31	**Reserved**
30:3	Reserved
2:0	**Reserved**

Display A (Primary) Plane Control

DSPAADDR—Display A Async flip Start Address Register

Memory Offset Address: 7017Ch

Default Value: 00000000h

Normal Access: Read/Write Double buffered

Bit	Descriptions
31:12	**Display A Start Address Bits.** This register provides the start address of the display A plane or the first eye when running in stereo mode. This address must be at least pixel aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. This address must be 4K aligned. When performing asynchronous flips and the display surface is in tiled memory, this address must be 256K aligned. This register can be written directly

<table>
<tr><td></td><td>through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT.
Write to this register triggers async flip. The async flip address is written into the Display A Base Address register 0x7019C</td></tr>
<tr><td>11:4</td><td>Reserved: MBZ</td></tr>
<tr><td>3</td><td>Flip_Source
Project: All
Default Value: 0b
This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr>
<tr><td>0b</td><td>CS</td><td>Flip source is CS</td><td>All</td></tr>
<tr><td>1b</td><td>BCS</td><td>Flip source is BCS</td><td>All</td></tr>
</table></td></tr>
<tr><td>2</td><td></td></tr>
<tr><td>1:0</td><td>Reserved: MBZ</td></tr>
</table>

DSPACNTR—Display A Plane Control Register

Memory Offset Address: 70180h

Default Value: 00000000h

Normal Access: Read/Write Double buffered

Notes: The active set of registers will be updated on the VBlank (of the currently selected pipe) after the "trigger" register (the Start Address register or the Control register when plane enable bit transitioning from a zero to a one) is written – thus providing an atomic update of all display controls. If the currently selected pipe is disabled, the update is immediate.

Bit	Descriptions
31	**Display Plane A (Primary A) Enable:** When this bit is set, the primary plane will generate pixels for display. When set to zero, display plane A memory fetches cease and display is blanked (from this plane) at the next VBLANK event from the pipe that display A is assigned. The display pipe must be enabled to enable this plane. There is an override for the enable of this

	plane in the Pipe Configuration register. During maxfifo mode, there is only one display plane. Plane enable is protected from updated at vblank. Any mode changes requires CPU exits to C0 and trigger maxfifo mode exit. 1 = Enable 0 = Disable
30	**Display A Gamma Enable:** This bit should only be changed after the plane has been disabled. It controls the bypassing of the display pipe gamma unit for this display plane's pixel data only. For 8-bit indexed display data, this bit should be set to a one. 0 = Display A pixel data bypasses the display pipe gamma correction logic (default). 1 = Display A pixel data is gamma corrected in the display pipe gamma correction logic.
29:26	**Display A Source Pixel Format:** These bits should only be changed after the plane has been disabled. Pixel formats with an alpha channel (8:8:8:8) should not use source keying. Pixel format of 8-bit indexed uses the palette. Before entering the blender, each source format is converted to 10 bits per pixel (details are described in the intermediate precision for the blender section of the Display Functions chapter). 000x = Reserved. 0010 = 8-bpp Indexed. 0011 = Reserved. 0100 = Reserved. 0101 = 16-bit BGRX (5:6:5:0) pixel format (XGA compatible). 0110 = 32-bit BGRX (8:8:8:8) pixel format. Ignore alpha. 0111 = 32-bit BGRA (8:8:8:8) pixel format. (with pre-multiplied alpha color format) 1000 = 32-bit RGBX (10:10:10:2) pixel format. Ignore alpha. 1001 = 32-bit RGBA (10:10:10:2) pixel format. (with pre-multiplied alpha color format) 1010 = 32-bit BGRX (10:10:10:2) pixel format Ignore alpha 1011 = 32-bit BGRA (10:10:10:2) pixel format (with pre-multiplied alpha color format) 1100 = 64-bit RGBX (16:16:16:16) 16 bit floating point pixel format. Ignore alpha. 1101 = 64-bit RGBA (16:16:16:16) 16-bit floating point pixel format (with pre-multiplied color format) 1110 = 32-bit RGBX (8:8:8:8) pixel format. Ignore alpha. 1111 = 32-bit RGBA (8:8:8:8) pixel format (with pre-multiplied color format)
25:24	Reserved
23	**Key Window Enable**. This bit applies only to devices with a display plane C. This bit is set to one when the color key is used as a destination key for display C. Display plane C must be

	enabled on the same pipe and it's Z-order should be programmed to be behind display A for this to be set to a one. 0 = Source Key applies to entire display plane A 1 = Source Key applies to only pixels within the intersection between Display A and Display C
22	**Key Enable**. This bit enables source keying for display A. Source keying allows a plane that is behind (below) this plane to show through where the display A key matches the display A data. This function is overloaded to provide display C destination keying when combined with the key window enable bit. Setting this bit is not allowed when the display pixel format includes an alpha channel. 0 = Source key is disabled 1 = Source key is enabled
21:20	**Pixel Multiply:** This cause the display plane to duplicate lines and pixels sent to the assigned pipe. In the pixel multiply mode, the horizontal pixels are doubled and lines are sent twice. Asynchronous flips are not used in this mode. Programming Notes: • Asynchronous flips are not permitted when pixel multiply is enabled. 00 = No duplication 01 = Line/pixel Doubling 10 = Reserved 11 = Pixel Doubling only
19	**Reserved:** Software must preserve the contents of this bit.
18	**Reserved:** Write as zero
17:16	**Reserved:** Software must preserve the contents of this bit.
15	**180° Display Rotation:** This mode causes the display plane to be rotated 180°. In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image. 0 = No rotation 1 = 180° rotation
14	Display A Trickle Feed Enable: 0 = Trickle Feed Enabled - Display A data requests are sent whenever there is space in the Display Data Buffer. 1 = Trickle Feed Disabled - Display A data requests are sent in bursts. Note: On mobile products this bit will be ignored such that Trickle Feed is always disabled.

13	Display A Data Buffer Partitioning Control: 0 = Display A Data Buffer will encompass Sprite A buffer space when Sprite A is disabled. 1 = Display A Data Buffer will not use Sprite A buffer space when Sprite A is disabled. Note: When in C3xR Max FIFO mode, this bit will be ignored.
12:11	Reserved
10	**Tiled Surface**. This bit indicates that the display A surface data is in tiled memory. The tile pitch is specified in bytes in the DSPASTRIDE register. Only X tiling is supported for display surfaces. When this bit is set, it affects the hardware interpretation of the DSPATILEOFF, DSPALINOFF, and DSPASURF registers. 0 = Display A surface uses linear memory 1 = Display A surface uses X-tiled memory
9	**Asynchronous Surface Address Update Enable:** This bit will enable asynchronous updates of the surface address when written by MMIO. The surface address will change with the next TLB request or when start of vertical blank is reached. Updates during vertical blank may not complete until after the first few active lines are displayed. Restrictions: No command streamer initiated surface address updates are allowed when this bit is enabled. Only one asynchronous update may be made per frame. Must wait for vertical blank before again writing the surface address register. 0 = DSPASURF MMIO writes will update synchronous to start of vertical blank (default) 1 = DSPASURF MMIO writes will update asynchronously
8:1	**Reserved:** Write as zero
0	Reserved

DSPALINOFF—Display A Linear Offset Register

Memory Offset Address: 70184h

Default Value: 00000000h

Normal Access: Read/Write Double buffered

This register specifies the panning for the display surface. The surface base address is specified in the DSPASURF register, and this register is used to describe an offset from that base address. Bit 10 of DSPACNTR specifies whether the display A surface is in linear or tiled memory. When the surface is in linear memory, this field contains the byte offset of the plane data in graphics memory. When the surface is tiled, the contents of this register are ignored.

This register can be written directly through software or by load register immediate command packets in the command stream.

This register is double buffered by VSYNC only. A change to this register will take affect on the next vsync following the write.

Bit	Descriptions
31:0	**Display A Offset:** This register provides the panning offset into the display A plane. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset must be at least pixel aligned. This offset is the difference between the address of the upper left pixel to be displayed and the display surface address. When performing 180° rotation, this offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address.

DSPASTRIDE—Display A Stride Register

Memory Offset Address: 70188h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

Bit	Descriptions
31:6	**Display A Stride:** This is the stride for display A in bytes. When using linear memory, this must be 64 byte aligned. When using tiled memory, this must be 512 byte aligned. This value is used to determine the line to line increment for the display. This register is updated either through a command packet passed through the command stream or writes to this register. When it is desired to update both this and the start register, the stride register must be written first because the write to the start register is the trigger that causes the update of both registers on the next VBLANK event. When using tiled memory, the actual memory buffer stride is limited to a maximum of 16K bytes.

DSPAKEYVAL—Sprite Color Key Value Register

Memory Offset Address: 70194h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

This register specifies the key color to be used with the mask bits to determine if the display source data matches the key. This register will only have an effect when the display color key is enabled. The overlay destination key value is used for overlay keying when Display A is being used as a primary display with overlay destination keying enabled. This key can be used as a Display C destination key onto Display A.

Bit	Descriptions
31:24	Reserved
23:16	**Red Key Value:** Specifies the color key value for the sprite red/Cr channel.
15:8	**Green Key Value:** Specifies the color key value for the sprite green/Y channel.
7:0	**Blue Key Value:** Specifies the color key value for the sprite blue/Cb channel.

DSPAKEYMSK—Sprite Color Key Mask Register

Memory Offset Address: 70198h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

This register specifies the key mask to be used with the color value bits to determine if the display source data matches the key when enabled. A zero bit in the mask indicates that the corresponding bit match failure should be ignored when determining if the pixel matches.

Bit	Descriptions
31:24	Reserved
23:16	**Red mask Value:** Specifies the color key mask for the sprite red/Cr channel.
15:8	**Green mask Value:** Specifies the color key mask for the sprite green/Y channel.
7:0	**Blue mask Value:** Specifies the color key mask for the sprite blue/Cb channel.

DSPASURF—Display A Surface Base Address Register

Memory Offset Address: 7019Ch

Default Value: 00000000h

Normal Access: Read/Write Double buffered

Bit	Descriptions
31:12	**Display A Surface Base Address**. This address specifies the surface base address. When the surface is tiled, panning is specified using (x, y) offsets in the DSPATILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DSPALINOFF register.

<table>
<tr><td></td><td>This address must be 4K aligned. When performing asynchronous flips and the display surface is in tiled memory, this address must be 256K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT.</td></tr>
<tr><td>11:4</td><td>Reserved</td></tr>
<tr><td>3</td><td>Flip_Source

Project: All

Default Value: 0b

This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination.
<table>
<tr><td>Value</td><td>Name</td><td>Description</td><td>Project</td></tr>
<tr><td>0b</td><td>CS</td><td>Flip source is CS</td><td>All</td></tr>
<tr><td>1b</td><td>BCS</td><td>Flip source is BCS</td><td>All</td></tr>
</table></td></tr>
<tr><td>2</td><td>Reserved</td></tr>
<tr><td>1:0</td><td>Reserved: MBZ</td></tr>
</table>

DSPATILEOFF—Display A Tiled Offset Register

Memory Offset Address: 701A4h

Default Value: 00000000h

Normal Access: Read/Write Double buffered

This register specifies the panning for the display surface. The surface base address is specified in the DSPASURF register, and this register is used to describe an offset from that base address. Bit 10 of DSPACNTR specifies whether the display A surface is in linear or tiled memory. When the surface is in linear memory, the offset is specified in the DSPALINOFF register and the contents of this register are ignored. When the surface is tiled, the start position is specified in this register as an (x, y) offset from the beginning of the surface.

This register can be written directly through software or by load register immediate command packets in the command stream.

This register is double buffered by VBLANK only. A change to this register will take affect on the next vblank following the write.

Bit	Descriptions
31:28	**Reserved:** Write as zero
27:16	**Plane Start Y-Position:** These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180° rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.
15:12	**Reserved:** Write as zero
11:0	**Plane Start X-Position:** These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180° rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the unrotated orientation.

DSPASURFLIVE—Display A Live Surface Base Address Register

Memory Offset Address: 701ACh

Default Value: 00000000h

Normal Access: Read Only

Bit	Descriptions
31:0	**Display A Live Surface Base Address**. This gives the live value of the surface base address as being currently used for the plane.

Display B (Second Primary or Sprite) Control

All Display B/Sprite registers are double buffered. The active set of registers will be updated on the VBlank (of the currently selected pipe) after the "trigger" register (the Start Address register or the Control register when plane enable bit transitioning from a zero to a one) is written – thus providing an atomic update of all display controls. If the currently selected pipe is disabled, the update is immediate.

DSPBADDR—Display B Async flip Start Address Register

Memory Offset Address: 7117Ch

Default Value: 00000000h

Normal Access: Read/Write Double buffered

<table>
<tr><th>Bit</th><th>Descriptions</th></tr>
<tr><td>31:12</td><td>Display B Start Address Bits. This register provides the start address of the display B plane or the first eye when running in stereo mode. This address must be at least pixel aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT.

This address must be 4K aligned. When performing asynchronous flips and the display surface is in tiled memory, this address must be 256K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT.

Write to this register triggers async flip The async flip address is written into the Display B Base Address register 0x7119C</td></tr>
<tr><td>11:4</td><td>Reserved: MBZ</td></tr>
<tr><td>3</td><td>Flip_Source

Project: All

Default Value: 0b

This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination.

<table><tr><th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr><tr><td>0b</td><td>CS</td><td>Flip source is CS</td><td>All</td></tr><tr><td>1b</td><td>BCS</td><td>Flip source is BCS</td><td>All</td></tr></table></td></tr>
<tr><td>2</td><td></td></tr>
<tr><td>1:0</td><td>Reserved: MBZ</td></tr>
</table>

DSPBCNTR—Display B/Sprite Plane Control Register

Memory Offset Address: 71180h

Default Value: 01000000h

Normal Access: Read/Write Double Buffered

The active set of registers will be updated on the VBlank (of the currently selected pipe) after the "trigger" register (the Start Address register or the Control register when plane enable bit transitioning from a zero to a one) is written – thus providing an atomic update of all display controls. If the currently selected pipe is disabled, the update is immediate.

Bit	Descriptions
31	**Display B/Sprite (Primary B) Enable:** This bit will enable or disable the display B/sprite. When this bit is set, the plane will generate pixels for display. When set to zero, memory fetches cease and display is blanked (from this plane) at the next VBLANK event from the pipe that this plane is assigned. At least one of the display pipes must be enabled to enable this plane. There is an override for the enable of this plane in the Pipe Configuration register. During maxfifo mode, there is only one display plane. Plane enable is protected from updated at vblank. Any mode changes requires CPU exits to C0 and trigger maxfifo mode exit. 1 = Enable 0 = Disable
30	**Display B/Sprite Gamma Enable:** This bit should only be changed after the plane has been disabled. It controls the bypassing of the display pipe gamma unit for this display plane pixel data only. For 8-bit indexed display data, this bit should be set to a one. 0 = Display B pixel data bypasses the pipe gamma correction logic (default). 1 = Display B pixel data is gamma corrected in the pipe gamma correction logic
29:26	**Display B Source Pixel Format:** This field selects the pixel format for the sprite/display B. Pixel formats with an alpha channel (8:8:8:8) should not use source keying. Before entering the blender, each source format is converted to 10 bits per pixel (details are described in the intermediate precision for the blender section of the Display Functions chapter). 000x = Reserved. 0010 = 8-bpp Indexed. 0011 = Reserved.0100 = Reserved. 0101 = 16-bit BGRX (5:6:5:0) pixel format (XGA compatible). 0110 = 32-bit BGRX (8:8:8:8) pixel format. Ignore alpha. 0111 = 32-bit BGRA (8:8:8:8) pixel format. (with pre-multiplied alpha color format) 1000 = 32-bit RGBX (10:10:10:2) pixel format. Ignore alpha. 1001 = 32-bit RGBA (10:10:10:2) pixel format. (with pre-multiplied alpha color format) 1010 = 32-bit BGRX (10:10:10:2) pixel format Ignore alpha 1011 = 32-bit BGRA (10:10:10:2) pixel format (with pre-multiplied alpha color format) 1100 = 64-bit RGBX (16:16:16:16) 16 bit floating point pixel format. Ignore alpha. 1101 = 64-bit RGBA (16:16:16:16) 16-bit floating point pixel format (with pre-multiplied color

	format) 1110 = 32-bit RGBX (8:8:8:8) pixel format. Ignore alpha. 1111 = 32-bit RGBA (8:8:8:8) pixel format (with pre-multiplied color format)
25:24	Reserved AccessType: Read Only
23	**Key Window Enable: This applies only to devices with a Display Plane C**. It determines what area of the screen the source key compare should be applied. This bit is set to one when the color key is used as a destination key for display C. Display plane C must be enabled on the same pipe and display A should not be enabled on this pipe for this to be used. The function is only effective when display C is enabled and defined by Z-order to be behind display B. 0 = If keying is enabled, it applies to the entire display B plane 1 = If keying is enabled, it applies only to the intersection between display B and display C
22	**Source Key Enable:** When used as a sprite or a secondary this enables source color keying. Sprite pixel values that match the key will become transparent. Source keying allows a plane that is behind (below) this plane to show through where the display B data matches the display B key. This function is overloaded to provide display C destination keying when combined with the key window enable bit.. Setting this bit is not allowed when the display pixel format includes an alpha channel. 0 = Sprite source key is disabled (default) 1 = Sprite source key is enabled.
21:20	**Pixel Multiply:** This cause the display plane to duplicate lines and pixels sent to the assigned pipe. In the line/pixel doubling mode, the horizontal pixels are doubled and lines are sent twice. Asynchronous flips are not used in this mode. Programming Notes: • Asynchronous flips are not permitted when pixel multiply is enabled. 00 = No duplication 01 = Line/pixel Doubling 10 = Reserved 11 = Pixel Doubling only
19:16	**Reserved:** Write as zero
15	**180° Display Rotation:** This mode causes the display plane to be rotated 180°. In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image. 0 = No rotation

	1 = 180° rotation
14	**Display B Trickle Feed Enable:** 0 = Trickle Feed Enabled - Display B data requests are sent whenever there is space in the Display Data Buffer. 1 = Trickle Feed Disabled - Display B data requests are sent in bursts. Note: On mobile products this bit will be ignored such that Trickle Feed is always disabled.
13	**Display B Data Buffer Partitioning Control:** 0 = Display B Data Buffer will encompass Sprite B buffer space when Sprite B is disabled. 1 = Display B Data Buffer will not use Sprite B buffer space when Sprite B is disabled. Note: When in C3xR Max FIFO mode, this bit will be ignored.
12:11	Reserved
10	**Tiled Surface:** This bit indicates that the display B surface data is in tiled memory. The tile pitch is specified in bytes in the DSPBSTRIDE register. Only X tiling is supported for display surfaces. When this bit is set, it affects the hardware interpretation of the DSPBLINOFF, DSPBTILEOFF, and DSPBSURF registers. 0 = Display B surface uses linear memory 1 = Display B surface uses X-tiled memory
9	**Asynchronous Surface Address Update Enable:** This bit will enable asynchronous updates of the surface address when written by MMIO. The surface address will change with the next TLB request or when start of vertical blank is reached. Updates during vertical blank may not complete until after the first few active lines are displayed. Restrictions: No command streamer initiated surface address updates are allowed when this bit is enabled. Only one asynchronous update may be made per frame. Must wait for vertical blank before again writing the surface address register. 0 = DSPBSURF MMIO writes will update synchronous to start of vertical blank (default) 1 = DSPBSURF MMIO writes will update asynchronously
8:1	**Reserved:** Write as zero
0	Reserved

DSPBLINOFFSET —Display B/Sprite Linear Offset Register

Memory Offset Address: 71184h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

This register specifies the panning for the display surface. The surface base address is specified in the DSPBSURF register, and this register is used to describe an offset from that base address. Bit 10 of DSPBCNTR specifies whether the display B surface is in linear or tiled memory. When the surface is in linear memory, this field contains the byte offset of the plane data in graphics memory. When the surface is tiled, the contents of this register are ignored.

This register can be written directly through software or by load register immediate command packets in the command stream.

This register is double buffered by VSYNC only. A change to this register will take affect on the next vsync following the write.

Bit	Descriptions
31:0	**Display B Offset:** This register provides the panning offset into the display B plane. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset must be at least pixel aligned. This offset is the difference between the address of the upper left pixel to be displayed and the display surface address. When performing 180° rotation, this offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address.

DSPBSTRIDE—Display B/Sprite Stride Register

Memory Offset Address: 71188h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

Bit	Descriptions
31:6	**Display B/Sprite Stride:** This is the stride for display B/Sprite in bytes. When using linear memory, this must be 64 byte aligned. When using tiled memory, this must be 512 byte aligned. The maximum value for this register is fixed. This register is updated through a command packet passed through the command stream or writes to this register. When it is desired to update both this and the start register, the stride register must be written first because the write to the start register is the trigger that causes the update of both registers on the next VBLANK event. When using tiled memory, the actual memory buffer stride is limited to a maximum of 16K bytes. The value in this register is updated through the command streamer during a synchronous flip.
5:0	Reserved

DSPBKEYVAL—Sprite Color Key Value Register

Memory Offset Address: 71194h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

This register specifies the key color to be used with the mask bits to determine if the sprite source data matches the key. This register will only have an effect when the sprite color key is enabled. The overlay destination key value is used for overlay keying when Display B is being used as a secondary display with overlay destination keying enabled.

Bit	Descriptions
31:24	Reserved
23:16	**Red Key Value:** Specifies the color key value for the sprite red/Cr channel.
15:8	**Green Key Value:** Specifies the color key value for the sprite green/Y channel.
7:0	**Blue Key Value:** Specifies the color key value for the sprite blue/Cb channel.

DSPBKEYMSK—Sprite Color Key Mask Register

Memory Offset Address: 71198h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

This register specifies the key mask to be used with the color value bits to determine if the sprite source data matches the key when enabled. A zero bit in the mask indicates that the corresponding bit match failure should be ignored when determining if the pixel matches.

Bit	Descriptions
31:24	Reserved
23:16	**Red Mask Value:** Specifies the color key mask for the sprite red/Cr channel.
15:8	**Green Mask Value:** Specifies the color key mask for the sprite green/Y channel.
7:0	**Blue Mask Value:** Specifies the color key mask for the sprite blue/Cb channel.

DSPBSURF—Display B Surface Address Register

Memory Offset Address: 7119Ch

Default Value: 00000000h

Normal Access: Read/Write Double buffered

Writing to this register triggers the display plane flip. When it is desired to change multiple display B registers, this register should be written last as a write to this register will cause all new register values to take effect.

<table>
<tr><td>Bit</td><td>Descriptions</td></tr>
<tr><td>31:12</td><td>Display B Surface Base Address: This address specifies the surface base address. When the surface is tiled, panning is specified using (x, y) offsets in the DSPBTILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DSPBLINOFF register.
This address must be 4K aligned. When performing asynchronous flips and the display surface is in tiled memory, this address must be 256K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT.</td></tr>
<tr><td>11:4</td><td>Reserved: MBZ</td></tr>
<tr><td>3</td><td>Flip_Source
Project: All
Default Value: 0b
This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination.
<table><tr><td>Value</td><td>Name</td><td>Description</td><td>Project</td></tr><tr><td>0b</td><td>CS</td><td>Flip source is CS</td><td>All</td></tr><tr><td>1b</td><td>BCS</td><td>Flip source is BCS</td><td>All</td></tr></table></td></tr>
<tr><td>2</td><td></td></tr>
<tr><td>1:0</td><td>Reserved: MBZ</td></tr>
</table>

DSPBTILEOFF—Display B Tiled Offset Register

Memory Offset Address: 711A4h

Default Value: 00000000h

Normal Access: Read/Write Double buffered

This register specifies the panning for the display surface. The surface base address is specified in the DSPBSURF register, and this register is used to describe an offset from that base address. Bit 10 of DSPBCNTR specifies whether the display B surface is in linear or tiled memory. When the surface is in linear memory, the offset is specified in the DSPBLINOFF register and the contents of this register are ignored. When the surface is tiled, the start position is specified in this register as an (x, y) offset from the beginning of the surface.

This register can be written directly through software or by load register immediate command packets in the command stream.

This register is double buffered by VBLANK only. A change to this register will take affect on the next vblank following the write.

Bit	Descriptions
31:28	**Reserved:** Write as zero
27:16	**Plane Start Y-Position:** These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180° rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.
15:12	**Reserved:** Write as zero
11:0	**Plane Start X-Position:** These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180° rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the unrotated orientation.

DSPBSURFLIVE—Display B Live Surface Base Address Register

Memory Offset Address: 711ACh

Default Value: 00000000h

Normal Access: Read Only

Bit	Descriptions
31:0	**Display B Live Surface Base Address**. This gives the live value of the surface base address as being currently used for the plane.

DSPBFLPQSTAT—Flip Queue Status Register

Memory Offset Address: 71200h

Default Value: 00000000h

Normal Access: Read Only

Bit	Descriptions
31:16	**Reserved:** Write as zero (RO)
15:8	**Queue Free Entry Count (RO):** This value indicates the number of free entries in the queue at the time that the register was read. The total number of entries in the queue is the sum of the occupied entry count and the free entry count.
7:0	**Queue Occupied Entry Count (RO):** This value indicates the number of occupied entries in the queue at the time that the register was read. The total number of entries in the queue is the sum of the occupied entry count and the free entry count.

Video BIOS Registers (71400h- 714FFh)

VGACNTRL—VGA Display Plane Control Register

Memory Offset Address: 71400h

Default Value: 00000000h

Normal Access: Read/Write

This register provides support for VGA compatibility modes. This register is used by video BIOS only.

Bit	Descriptions
31	**VGA Display Disable:** This bit will disable the VGA compatible display mode. It has no effect on VGA register or A0000-BFFFF memory aperture accesses which are controlled by the PCI configuration and VGA register settings. VGA display should only be enabled if all display planes other than VGA are disabled. After enabling the VGA, most display planes need to stay disabled, only the VGA popup (cursor A) can be enabled. The VGA display is never trusted. No secrets are allowed in the pre-allocated memory and VGA is limited to access only that memory. VGA 132 Column text mode is not supported. 0 = VGA Display Enabled 1 = VGA Display Disabled
30	**VGA/Pop-up 2X Centered Mode Scaling:** When this bit is set to a one, the VGA and pop-up data is scaled using pixel doubling in both the horizontal and vertical direction for use on un-scaled flat panel displays. Setting this bit allows the VGA to run at higher dot clock frequencies and creates a larger (4x the size) image for better quality on larger displays. It is intended for use in one of the centering modes when not using the internal panel fitting. Do not use it for native VGA modes or when internal panel fitting is used to scale VGA. In the situations where it is used, for 1280 wide or larger panels this bit should be set. For exactly 1280 wide panels, the Nine-dot disable bit should also be set. This operation is in addition to the VGA functions that double the pixels and lines. 0 = VGA display is normal size 1 = VGA and VGA popup data is doubled in the horizontal and vertical direction.
29	**VGA Pipe Select:** This bit only applies to devices with dual pipe support. For devices with a single display pipe, this bit will be ignored. For dual pipe devices, this bit determines which pipe is to receive the VGA display data. This must be changed only when the VGA display is in the disabled state via the VGA display disable bit or during the write to enable VGA display. 0 = Selects Assigns the VGA display to Pipe A 1 = Selects Assigns the VGA display to Pipe B
28:27	**Reserved** – Software must preserve the contents of these bits.
26	**VGA Border Enable:** This bit determines if the VGA border areas during VGA centering modes are included in the active display area and do or do not appear on integrated TV encoder

	output and devices that use centering such as on DVO connected flat panel, TV displays, or integrated panels. For use with the internal panel fitting logic, the border if enabled will be scaled along with the pixel data. Setting this bit allows the popup to be positioned overlapping the border area of the image. 0 = VGA Border areas are not included in the image size calculations for centering only active area.1 = VGA Border areas are enabled and is passed to the display pipe for display and used in the image size calculation for centering modes
25:24	**VGA Centering Enable:** VGA centering modes use the pipe timing generators to determine the actual display timings. This would normally correspond to the display panel size and timings. The VGA registers determine the centered VGA image height and width. The VGA border may or may not be considered in the calculation selected by the VGA Border Enable bit. For a proper image, the VGA image size should not exceed the pipe timing generator active rectangle. When using the internal panel fitting logic, the horizontal image size needs to be less than or equal to 2048 pixels to generate a proper image. The VGA image will either be centered within the pipe timing rectangle or appear in the upper left corner. Upper left corner centered mode is generally used for external panel scaling where the DVO stall signal is used and is always used for internal panel fitting operation. When panel fitter is enabled on the same pipe as VGA this register setting is ignored and upper left corner centered mode is always selected. When centering is disabled, the VGA CRTC registers determine the display timing compatible with legacy VGA devices for driving CRT like devices. 00 = VGA centering is disabled, VGA operates in Native VGA mode or when driving integrated TV01 = VGA centering is enabled, VGA image appears in the center of the larger rectangle 10 = VGA centering is enabled, VGA image appears in the upper left corner of the larger rectangle 11 = VGA centering is enabled, VGA image appears in the upper left corner of the larger rectangle
23	**VGA Palette Read Select:** This bit only applies to dual display pipe devices and determines which palette VGA palette read accesses will occur from. 0 = VGA palette reads will access Palette A (default). 1 = VGA palette reads will access Palette B VGA palette reads are reads from I/O address 0x3c9.
22	VGA Palette A Write Disable: This determines which palette the VGA palette writes will have as a destination. One or both palettes can be the destination. If both are disabled, writes will not affect the palette RAM contents. 0 = VGA palette writes will update Palette A (default).1 = VGA palette writes will not update Palette A VGA palette writes are writes to I/O address 0x3C9h.
21	Dual Pipe VGA Palette B Write Disable: This determines which palette the VGA palette writes will have as a destination. One or both

	palettes can be the destination. If both are disabled, writes will not affect the palette RAM contents. 0 = VGA palette writes will update Palette B (default).1 = VGA palette writes will not update Palette B VGA palette writes are writes to I/O address 0x3C9h.
20	**Legacy VGA 8-Bit Palette Enable:** This bit only affects reads and writes to the palette through VGA I/O addresses. In the 6-bit mode, the 8-bits of data are shifted up two bits on the write (upper two bits are lost) and shifted two bits down on the read. It provides backward compatibility for original VGA programs (in it's default state) as well as VESA VBE support for 8-bit palette. It does not affect palette accesses through the palette register MMIO path. 0 = 6-bit DAC (default).1 = 8-bit DAC.
19	**Reserved**
18	**Nine Dot Disable:** Prevents DOS applications from setting the VGA display into a real 9-dot per character operation mode, instead the device emulates that using 8-dots per character. This is intended to provide VGA compatibility on DVI type connectors and integrated panels where there would otherwise not be room for the 720 horizontal pixels or 1440 pixels when horizontally doubled. The VGA register bit SR01<0> functionality is disabled. VGA panning control handles the pseudo 9-dot mode when both this bit is set and SR01<0> is clear. 0 = Enable use of 9-dot enable bit in VGA registers1 = Ignore the 9-dot per character bit and always use 8
17	Reserved
16:8	**Reserved** – Software must preserve the contents of these bits.
7:6	**Blink Duty Cycle:** Controls the VGA text mode blink duty cycle relative to the cursor blink duty cycle. 00 = 100% Duty Cycle, Full Cursor Rate (Default)01 = 25% Duty Cycle, ½ Cursor Rate10 = 50% Duty Cycle, ½ Cursor Rate11 = 75% Duty Cycle, ½ Cursor Rate
5:0	**VSYNC Blink Rate:** Controls the VGA blink rate in terms of the number of VSYNCs per on/off cycle. These bits are programmed with the (VSYNCs/cycle)/2-1. The proper programming of this register is determined by the VSYNC rate that the display requires when in a VGA display mode.

Software Flag Registers

SWF00—Software Flag 00

Memory Offset Address: 70410h

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions
31:0	**Reserved** – for Video BIOS and Drivers

SWF01—Software Flag 01

Memory Offset Address: 70414h

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions
31:0	**Reserved** – for Video BIOS and Drivers

SWF02—Software Flag 02

Memory Offset Address: 70418h

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions
31:0	**Reserved** – for Video BIOS and Drivers

SWF03—Software Flag 03

Memory Offset Address: 7041Ch

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions

31:0	**Reserved** – for Video BIOS and Drivers

SWF04—Software Flag 04

Memory Offset Address: 70420h

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions
31:0	**Reserved** – for Video BIOS and Drivers

SWF05—Software Flag 05

Memory Offset Address: 70424h

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions
31:0	**Reserved** – for Video BIOS and Drivers

SWF06—Software Flag 06

Memory Offset Address: 70428h

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions
31:0	**Reserved** – for Video BIOS and Drivers

SWF07—Software Flag 07

Memory Offset Address: 7042Ch

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions
31:0	**Reserved** – for Video BIOS and Drivers

SWF08—Software Flag 08

Memory Offset Address: 70430h

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions
31:0	**Reserved** – for Video BIOS and Drivers

SWF09—Software Flag 09

Memory Offset Address: 70434h

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions
31:0	**Reserved** – for Video BIOS and Drivers

SWF0A—Software Flag 0A

Memory Offset Address: 70438h

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions

31:0	**Reserved** – for Video BIOS and Drivers

SWF0B—Software Flag 0B

Memory Offset Address: 7043Ch

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions
31:0	**Reserved** – for Video BIOS and Drivers

SWF0C—Software Flag 0C

Memory Offset Address: 70440h

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions
31:0	**Reserved** – for Video BIOS and Drivers

SWF0D—Software Flag 0D

Memory Offset Address: 70444h

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions
31:0	**Reserved** – for Video BIOS and Drivers

SWF0E—Software Flag 0E

Memory Offset Address: 70448h

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions
31:0	**Reserved** – for Video BIOS and Drivers

SWF0F—Software Flag 0F

Memory Offset Address: 7044Ch

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions
31:0	**Reserved** – for Video BIOS and Drivers

SWF10—Software Flag 10

Memory Offset Address: 71410h

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions
31:0	**Reserved** – for Video BIOS and Drivers

SWF11—Software Flag 11

Memory Offset Address: 71414h

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions

31:0	**Reserved** – for Video BIOS and Drivers

SWF12—Software Flag 12

Memory Offset Address: 71418h

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions
31:0	**Reserved** – for Video BIOS and Drivers

SWF13—Software Flag 13

Memory Offset Address: 7141Ch

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions
31:0	**Reserved** – for Video BIOS and Drivers

SWF14—Software Flag 14

Memory Offset Address: 71420h

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions
31:0	**Reserved** – for Video BIOS and Drivers

SWF15—Software Flag 15

Memory Offset Address: 71424h

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions
31:0	**Reserved** – for Video BIOS and Drivers

SWF16—Software Flag 16

Memory Offset Address: 71428h

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions
31:0	**Reserved** – for Video BIOS and Drivers

SWF17—Software Flag 17

Memory Offset Address: 7142Ch

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions
31:0	**Reserved** – for Video BIOS and Drivers

SWF18—Software Flag 18

Memory Offset Address: 71430h

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions

31:0	**Reserved** – for Video BIOS and Drivers

SWF19—Software Flag 19

Memory Offset Address: 71434h

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions
31:0	**Reserved** – for Video BIOS and Drivers

SWF1A—Software Flag 1A

Memory Offset Address: 71438h

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions
31:0	**Reserved** – for Video BIOS and Drivers

SWF1B—Software Flag 1B

Memory Offset Address: 7143Ch

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions
31:0	**Reserved** – for Video BIOS and Drivers

SWF1C—Software Flag 1C

Memory Offset Address: 71440h

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions
31:0	**Reserved** – for Video BIOS and Drivers

SWF1D—Software Flag 1D

Memory Offset Address: 71444h

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions
31:0	**Reserved** – for Video BIOS and Drivers

SWF1E—Software Flag 1E

Memory Offset Address: 71448h

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions
31:0	**Reserved** – for Video BIOS and Drivers

SWF1F—Software Flag 1F

Memory Offset Address: 7144Ch

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions

31:0	**Reserved** – for Video BIOS and Drivers

SWF30—Software Flag 30

Memory Offset Address: 72414h

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions
31:0	**Reserved** – for Video BIOS and Drivers

SWF31—Software Flag 31

Memory Offset Address: 72418h

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions
31:0	**Reserved** – for Video BIOS and Drivers

SWF32—Software Flag 32

Memory Offset Address: 7241Ch

Default Value: 00000000h

Normal Access: Read/Write

These 32-bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Descriptions
31:0	**Reserved** – for Video BIOS and Drivers

Sprite A Control Registers

All of the basic control Sprite A, Sprite B, Sprite C, Sprite D registers are double buffered. The active set is updated after the trigger register is written followed by a VBLANK event. Sprite A, Sprite B are always assigned to pipe A. Sprite C, Sprite D are always assigned to pipe B The Sprite color adjustment registers are not double buffered and take effect immediately.

SPACNTR—Sprite A Control Register

Memory Offset Address: 72180h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

The active set of basic control registers will be updated on the VBlank (of the currently selected pipe) after the "trigger" register (the Start Address register or the Control register when plane enable bit transitioning from a zero to a one) is written – thus providing an atomic update of all display controls with the exception of the Sprite A color control registers. If the currently selected pipe is disabled, the VBLANK of the active pipe is used. At least one pipe must be enabled and running for the display plane to be enabled.

Bit	Descriptions
31	**Sprite A Enable:** This bit will enable or disable the Sprite A. When this bit is set, the plane will generate pixels for display to be combined by the blender for the target pipe. When set to zero, memory fetches cease and display is blanked (from this plane) at the next VBLANK event from the pipe that this plane is assigned. At least one of the display pipes must be enabled to enable this plane. There is an override for the enable of this plane in the Pipe Configuration register. This bit only has an effect when the plane is not trusted. When the plane is marked trusted, this bit will be overridden and the display disabled when the registers are unlocked. 1 = Enable0 = Disable
30	**Sprite A Gamma Enable:** There are two gamma adjustments possible in the Sprite A data path. This bit controls the gamma correction in the display pipe not the gamma control in this plane. It affects only the pixel data from this display plane. For pixel format of 8-bit indexed, this bit should be set to a one. Gamma correction logic that is contained in the Sprite A logic is disabled by loading the default values into those registers. When this plane is marked as trusted, this bit should always be set to zero to force the pipe gamma to be always be bypassed. 0 = Sprite A pixel data bypasses the display pipe gamma correction logic (default). 1 = Sprite A pixel data is gamma corrected in the pipe gamma correction logic
29:26	**Sprite A Source Pixel Format:** This field selects the pixel format for the sprite/Sprite A. Pixel formats with an alpha channel should not use source keying. Before entering the blender, each source format is converted to 10 bits per pixel (details are described in the intermediate

	precision for the blender section of the Display Functions chapter). 0000 = YUV 4:2:2 packed (see byte order below). 0001 = Reserved 0010 = 8-bpp Indexed. 0011 = Reserved. 0100 = Reserved. 0101 = 16-bit BGRX (5:6:5:0) pixel format (XGA compatible). 0110 = 32-bit BGRX (8:8:8:8) pixel format. Ignore alpha. 0111 = 32-bit BGRA (8:8:8:8) pixel format with pre-multiplied alpha channel. 1000 = 32-bit RGBX (10:10:10:2) pixel format. Ignore alpha. 1001 = 32-bit RGBA (10:10:10:2) pixel format 1010 = Reserved. 1011 = Reserved. 1100 = Reserved. 1101 = Reserved. 1110 = 32-bit RGBX (8:8:8:8) pixel format. Ignore alpha. 1111 = 32-bit RGBA (8:8:8:8)
25:24	Sprite A Pipe Select: Sprite A always ties to pipe A. Reserved.
23	Reserved:
22	**Sprite Source Key Enable:** When used as a sprite in the 16/32-bpp modes without alpha this enables source color keying. Sprite pixel values that match (within range) the key will become transparent. Setting this bit is not allowed when the Sprite A pixel format includes an alpha channel. 0 = Sprite source key is disabled (default) 1 = Sprite source key is enabled. Each sprite has built in source keying enabled/disabled. If the source keying is disabled and no alpha blending is enabled, the pixels are tagged as opaque. If sprite source keying is enabled and no alpha blending is enabled, it works as follows: For YUV sprite data, each yuv channel data is compared with the corresponding channel's key color Low and High (each channel inrange can be masked out). If all three channels are in range between the low and high key values, it is considered source compared. For RGB sprite data, each 24-bit RGB pixel data is compared with the 24-bit key value (note it

	only uses the 24-bit Low key value for comparison). Each 24-bit has to be equal (each bit comparison can also be masked out) for the source compared. If the sprite source data compare and matches, then the sprite data will be tagged as transparent when blending with its destination pixel. If the sprite source data does not compare, then the sprite data will be tagged as opaque when blending with its destination pixel.
21:20	**Pixel Multiply:** This cause the display plane to duplicate lines and pixels sent to the assigned pipe. In the line/pixel doubling mode, the horizontal pixels are doubled and lines are sent twice. This is a method of scaling the source image by two (both H and V). 00 = No line/Pixel duplication 01 = Line/Pixel Doubling 10 = Line Doubling only 11 = Pixel Doubling only
19	**Color Conversion Disabled:** This bit enables or disables the color conversion logic. Color conversion is intended to be used with the formats that support YUV formats such as the YUV 4:2:2 packed format and x:8:8:8 and 8:8:8:8 formats. Formats such as RGB5:5:5 and 5:6:5 do not have YUV versions. 0 = Pixel data is sent through the conversion logic (only applies to YUV formats) 1 = Pixel data is not sent through the YUV->RGB conversion logic.
18	**YUV Format:** This bit specifies the source YUV format for the YUV to RGB color conversion operation. This field is ignored when source data is RGB. 0 = ITU-R Recommendation BT.601 1 = ITU-R Recommendation BT.709
17:16	**YUV byte Order:** This field is used to select the byte order when using YUV 4:2:2 data formats. For other formats, this field is ignored. 00 = YUYV01 = UYVY10 = YVYU11 = VYUY
15	**180° Display Rotation:** This mode causes the display plane to be rotated 180°. In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image and calculate the x, y offset as relative to the lower right corner. 0 = No rotation 1 = 180° rotation
14:11	Reserved
10	**Tiled Surface:** This bit indicates that the Sprite A surface data is in tiled memory. The tile pitch is specified in bytes in the DSPCSTRIDE register. Only X tiling is supported for display surfaces.

<table>
<tr><td></td><td>When this bit is set, it affects the hardware interpretation of the DSPCTILEOFF, DSPCLINOFF, and DSPCSURFADDR registers.
0 = Sprite A surface uses linear memory
1 = Sprite A surface uses X-tiled memory</td></tr>
<tr><td>9:3</td><td>Reserved: Write as zero</td></tr>
<tr><td>2</td><td>Sprite A Bottom: This bit will force the Sprite A plane to be on the bottom of the Z order. If the plane is marked as trusted, it only applies to the Z order of the trusted planes.0 = Sprite A Z order is determined by the other control bits1 = Sprite A is forced to be on the bottom of the Z order.</td></tr>
<tr><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>Sprite A Z-order: With Sprite A and B z-order, bottom control bits, Sprite A plane is placed in a specific z-order among other planes.
<table>
<tr><td colspan="6">Display Pipe A Z-orders</td></tr>
<tr><td>SAzorder</td><td>SAbottom</td><td>SBzorder</td><td>SBbottom</td><td>Resulting Pipe Z-order (from bottom to top)</td><td>Source Keying</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>PA SA SB CA</td><td>PA in Black</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>PA SB SA CA</td><td>PA in Black</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>SB PA SA CA</td><td>use src keying on SB</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>SB PA SA CA</td><td>use src keying on SB</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>SB SA PA CA</td><td>use src keying on SA</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>SB SA PA CA</td><td>use src keying on SA</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>SA PA SB CA</td><td>use src keying on SA</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>SA PA SB CA</td><td>use src keying on SA</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>SA SB PA CA</td><td>use src keying on SB</td></tr>
</table>
</td></tr>
</table>

	1	1	1	0	SA SB PA CA	use src keying on SB
	0: Sprite A z-order is disabled 1: Sprite A z-order is enabled					

SPALINOFF —Sprite A Linear Offset Register

Memory Offset Address: 72184h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

This register specifies the panning for the display surface. The surface base address is specified in the DSPCSURFADDR register, and this register is used to describe an offset from that base address. Bit 10 of DSPCCNTR specifies whether the display A surface is in linear or tiled memory. When the surface is in linear memory, this field contains the byte offset of the plane data in graphics memory. When the surface is tiled, the contents of this register are ignored. For YUV422 format, the linear offset value should be of even value.

This register can be written directly through software or by load register immediate command packets in the command stream.

This register is double buffered by VSYNC only. A change to this register will take affect on the next vsync following the write.

Bit	Descriptions
31:0	**Sprite A Offset:** This register provides the panning offset into the Sprite A plane. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset must be at least pixel aligned. This offset is the difference between the address of the upper left pixel to be displayed and the display surface address. When performing 180° rotation, this offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address.

SPASTRIDE—Sprite A Stride Register

Memory Offset Address: 72188h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

Bit	Descriptions
31:6	**Sprite A Stride:** This is the stride for Sprite A in bytes. When using linear memory, this must be

	64 byte aligned. When using tiled memory, this must be 256 byte aligned. This register is updated through a command packet passed through the command stream or writes to this register. When it is desired to update both this and the start register, the stride register must be written first because the write to the start register is the trigger that causes the update of both registers on the next VBLANK event. When using tiled memory, the actual memory buffer stride is limited to a maximum of 16K bytes.
5:0	Reserved

SPAPOS—Sprite Position Register

Memory Offset Address: 7218Ch

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

These registers specify the screen position and size of the sprite. This register is double buffered. The load register is transferred into the active register on the asserting edge of Vertical Blank for the pipe that the display is assigned. When using the sprite as a secondary display, this should be set to the entire display rectangle.

Bit	Descriptions
31:28	**Reserved:** Write as zero
27:16	**SpriteY-Position:** These 12 bits specify the vertical position in lines of the sprite (upper left corner) relative to the beginning of the active video area. When performing 180° rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	**Reserved:** Write as zero
11:0	**Sprite X-Position:** These 12 bits specify the horizontal position in pixels of the sprite (upper left corner) relative the beginning of the active video area. When performing 180° rotation, this field specifies the horizontal position of the original lower right corner relative to the original end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.

SPASIZE—Sprite Height and Width Register

Memory Offset Address: 72190h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

This register specifies the height and width of the sprite in pixels and lines. The rectangle defined by the size and position should never exceed the boundaries of the display rectangle that the sprite is assigned to.

Bit	Descriptions
31:28	**Reserved:** Write as zero
27:16	**Sprite Height:** This register field is used to specify the height of the sprite in lines. The value in the register is the height minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	**Reserved:** Write as zero
11:0	**Sprite Width:** This register field is used to specify the width of the sprite in pixels. This does not have to be the same as the stride but should be less than or equal to the stride (converted to pixels). The value in the register is the width minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image. The sprite width is limited to even values when YUV source pixel format is used (actual width, not the width minus one value).

SPAKEYMINVAL—Sprite Color Key Min Value Register

Memory Offset Address: 72194h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

This register specifies the key color to be used with the mask bits to determine if the sprite source data matches the key. This register will only have an effect when the sprite color key is enabled. The unused bits of the 5:5:5 or 5:6:5 formats must be filled with duplicates of the three or two MSBs of the pixel value.

For YUV sprite data, each yuv channel data is compared with the corresponding channel's key color Low and High (each channel inrange can be masked out). If all three channels are in range between the low and high key values, it is considered source compared.

For RGB sprite data, each 24-bit RGB pixel data is compared with the 24-bit key value (note it only uses the 24-bit Low key value for comparison). Each 24-bit has to be equal (each bit comparison can also be masked out) for the source compared.

Bit	Descriptions
31:24	**Reserved:** Write as zero
23:16	**Red Key Min Value:** Specifies the color key minimum value for the sprite red/Cr channel.

15:8	**Green Key Min Value:** Specifies the color key minimum value for the sprite green/Y channel.
7:0	**Blue Key Min Value:** Specifies the color key minimum value for the sprite blue/Cb channel.

SPAKEYMSK—Sprite Color Key Mask Register

Memory Offset Address: 72198h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

Bit	Descriptions
31:3	**Reserved:** Write as zero
2	**Red Channel Enable:** Specifies the source color key enable for the red/Cr channel.
1	**Green Channel Enable:** Specifies the source color key enable for the green/Y channel.
0	**Blue Channel Enable:** Specifies the source color key enable for the blue/Cb channel

SPASURF—Sprite A Surface Address Register

Memory Offset Address: 7219Ch

Default Value: 00000000h

Normal Access: Read/Write Double buffered

Writing to this register triggers the display plane flip. When it is desired to change multiple Sprite A registers, this register should be written last as a write to this register will cause all new register values to take effect.

Bit	Descriptions
31:12	**Sprite A Surface Base Address:** This address specifies the surface base address. When the surface is tiled, panning is specified using (x, y) offsets in the DSPCTILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DSPCLINOFF register. This address must be 4K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. The value in this register is updated through the command streamer during synchronous flips.
11:4	Reserved: MBZ
3	Flip_Source

<table>
<tr><td></td><td>
Project: All

Default Value: 0b

This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr>
<tr><td>0b</td><td>CS</td><td>Flip source is CS</td><td>All</td></tr>
<tr><td>1b</td><td>BCS</td><td>Flip source is BCS</td><td>All</td></tr>
</table>
</td></tr>
<tr><td>2</td><td></td></tr>
<tr><td>1:0</td><td>Reserved: MBZ</td></tr>
</table>

SPAKEYMAXVAL—Sprite Color Key Max Value Register

Memory Offset Address: 721A0h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

This register specifies the key color to be used with the mask bits to determine if the sprite source data matches the key. This register will only have an effect when the sprite color key is enabled.

For YUV sprite data, each yuv channel data is compared with the corresponding channel's key color Low and High (each channel inrange can be masked out). If all three channels are in range between the low and high key values, it is considered source compared.

For RGB sprite data, each 24-bit RGB pixel data is compared with the 24-bit key value (note it only uses the 24-bit Low key value for comparison). Each 24-bit has to be equal (each bit comparison can also be masked out) for the source compared.

Bit	Descriptions
31:24	**Reserved:** Write as zero
23:16	**Red Key Max Value:** Specifies the color key value for the sprite red/Cr channel.
15:8	**Green Key Max Value:** Specifies the color key value for the sprite green/Y channel.

7:0	**Blue Key Max Value:** Specifies the color key value for the sprite blue/Cb channel.

SPATILEOFF—Sprite A Tiled Offset Register

Memory Offset Address: 721A4h

Default Value: 00000000h

Normal Access: Read/Write Double buffered

This register specifies the panning for the display surface. The surface base address is specified in the DSPCSURFADDR register, and this register is used to describe an offset from that base address. Bit 10 of DSPCCNTR specifies whether the display A surface is in linear or tiled memory. When the surface is in linear memory, the offset is specified in the DSPCLINOFF register and the contents of this register are ignored. When the surface is tiled, the start position is specified in this register as an (x, y) offset from the beginning of the surface.

This register can be written directly through software or by load register immediate command packets in the command stream.

This register is double buffered by VSYNC only. A change to this register will take affect on the next vsync following the write.

Bit	Descriptions
31:28	**Reserved:** Write as zero
27:16	**Plane Start Y-Position:** These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180° rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.
15:12	**Reserved:** Write as zero
11:0	**Plane Start X-Position:** These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180° rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the unrotated orientation.

SPAContAlpha—Sprite A Constant Alpha Register

Memory Offset Address: 721A8h

Default Value: 00000000h

Normal Access: Read/Write Double buffered

Bit	Description
31	**Enable Constant Alpha:** Sprite A Sprite constant alpha provides a way to apply an alpha value to all video sprite pixels. Each pixel color channel is multiplied by the constant alpha before proceeding to the blender. This can be used to create fade out effects. This is intended for CE device use where the video sprite might still be used to generate video output. 0 – Sprite A Sprite Constant Alpha is disabled 1 – Sprite A Sprite Constant Alpha is enabled
30:8	Reserved: MBZ
7:0	**Sprite A Constant Alpha Value:** This field provides the alpha value when constant alpha is enabled. A value of FF means fully opaque and a value of zero means fully transparent. Values in between those values allow for a blending of sprite with other surfaces.

SPALIVESURF—Sprite A Live Surface Address Register

Memory Offset Address: 721ACh

Default Value: 00000000h

Normal Access: Read

Bit	Descriptions
31:12	**Sprite A Live Surface Base Address:** This gives the live value of the surface base address as being currently used for the Sprite A plane.
11:4	**Reserved: MBZ**
3	Flip_Source Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination.

Value	Name	Description	Project
0b	CS	Flip source is CS	All
1b	BCS	Flip source is BCS	All

2	**Reserved**
1:0	**Reserved: MBZ**

Sprite A Color Adjustment

These functions provide mechanisms for control of image colors generated from Sprite A sources. These functions are mainly intended for use for YUV color format sources. Adjustments are made before the YUV to RGB conversion. They take effect even when the Conversion Bypass bit is set. For display source input data in RGB format, software must set all the color correction registers to their default values (equivalent to a bypass mode). **These registers are not double buffered, take effect immediately after loading.**

SPACLRC0 —Sprite A Color Correction 0 Register

Address Offset:721D0h

Default Value: 01000000h

Normal Access: RW

Size: 32 bits

Bit	Description
31:27	Reserved
26:18	**Contrast:** Contrast adjustment applies to YUV data. The Y channel is multiplied by the value contained in the register field. This signed fixed-point number is in 3i.6f format with the first 3 MSBs as the integer value and the last 6 LSBs as the fraction value. The allowed contrast value ranges from 0 to 7.53125 decimal. Bypassing Contrast, for YUV modes and for source data in RGB format, is accomplished by programming this field to a field value that represents 1.0 decimal or 001.000000 binary .
17:8	Reserved
7:0	**Brightness:** This field provides the brightness adjustment with a 8-bit 2's compliment value ranging [-128, +127]. This value is added to the Y value after contrast multiply and before YUV to RGB conversion. A value of zero disables this adjustment affect. This 8-bit signed value provides half of the achievable brightness adjustment dynamic range. A full range brightness value would have a programmable range of [-255, +255]. Bypassing Brightness for YUV formats and for source data in RGB format, is accomplished by programming this field to 0.

SPAGAMC0— Sprite A Gamma Correction Registers

Address Offset:721F4h

Default Value: 00080808h

Normal Access: R/W

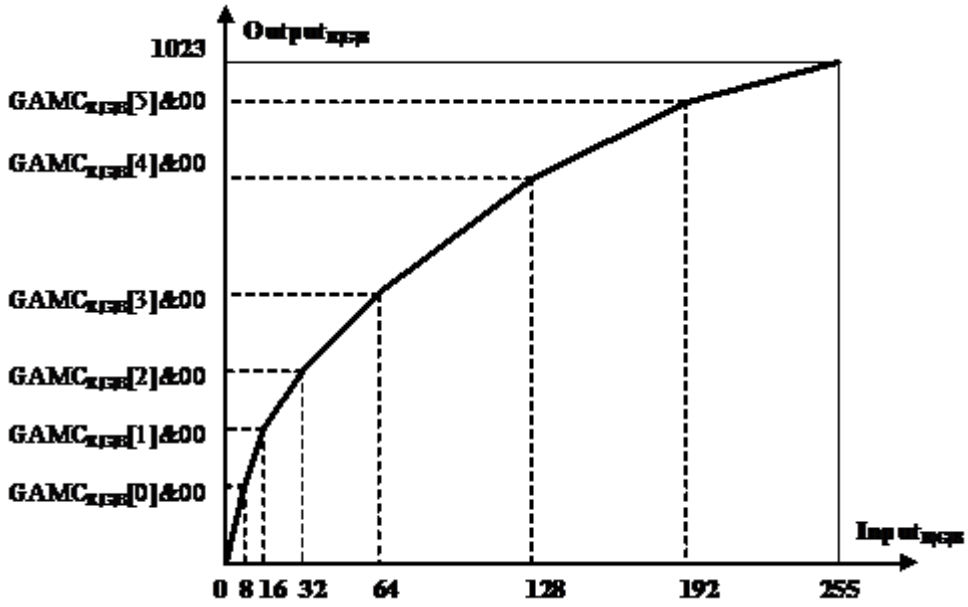
Size: 32 bits

These registers are used to determine the characteristics of the gamma correction for the Sprite A pixel data pre-blending. Additional gamma correction can be done in the display pipe gamma if desired. The pixels input to the gamma correction are 8 bit per channel pixels, and the output of the gamma correction is 10 bit per channel pixels. The gamma curve is represented by specifying a set of points along the curve. Each register has 32 bits, which are written to and read from together when accessed by the software. They are the six individual breakpoints on a logarithmically spaced color intensity space as shown in the following figure. The 8 bit values in the register are extended to 10 bit values in hardware by concatenating two zeroes onto the LSBs. The two end points (0 and 1023) have fixed values 0 and 1023, respectively. The appropriate Gamma breakpoint pairs (adjacent) are selected for each color component (Red, Green and Blue), and the output is interpolated between these two breakpoint values. The Gamma Correction registers (GAMC0 to GAMC5) are not double-buffered. They should be updated when the overlay is off. Otherwise, screen artifacts may show.

When the output from overlay is set in YUV format by programming CSC bypass, normally software should also bypass this gamma unit. However, since this gamma unit can also be viewed as a nonlinear transformation, it can be used, for whatever reason, in YUV output mode. In this case, the mapping of the three sets of piecewise linear map are as the following:

Bit	Description
31:24	Reserved
23:16	Red (V/Cr):
15:8	Green (Y):
7:0	Blue (U/Cb):

Figure 11-1. Programming of the Piecewise-linear Estimation of Gamma Correction Curve



SPAGAMC1— Sprite A Gamma Correction Registers

Address Offset:721F0h

Default Value: 00101010h

Normal Access: R/W

Size: 32 bits

Same as previous register.

Bit	Description
31:24	Reserved
23:16	Red (V/Cr):
15:8	Green (Y):
7:0	Blue (U/Cb):

SPAGAMC2— Sprite A Gamma Correction Registers

Address Offset:721ECh

Default Value: 00202020h

Normal Access: R/W

Size: 32 bits

Same as previous register.

Bit	Description
31:24	Reserved
23:16	Red (V/Cr):
15:8	Green (Y):
7:0	Blue (U/Cb):

SPAGAMC3— Sprite A Gamma Correction Registers

Address Offset:721E8h

Default Value: 00404040h

Normal Access: R/W

Size: 32 bits

Same as previous register.

Bit	Description
31:24	Reserved
23:16	Red (V/Cr):
15:8	Green (Y):
7:0	Blue (U/Cb):

SPAGAMC4— Sprite A Gamma Correction Registers

Address Offset:721E4h

Default Value: 00808080h

Normal Access: R/W

Size: 32 bits

Same as previous register.

Bit	Description
31:24	Reserved

23:16	Red (V/Cr):
15:8	Green (Y):
7:0	Blue (U/Cb):

SPAGAMC5— Sprite A Gamma Correction Registers

Address Offset:721E0h

Default Value: 00C0C0C0h

Normal Access: R/W

Size: 32 bits

Same as previous register.

Bit	Description
31:24	Reserved
23:16	Red (V/Cr):
15:8	Green (Y):
7:0	Blue (U/Cb):

Sprite B Control Registers

All of the basic control Sprite A, Sprite B, Sprite C, Sprite D registers are double buffered. The active set is updated after the trigger register is written followed by a VBLANK event. Sprite A, Sprite B are always assigned to pipe A. Sprite C, Sprite D are always assigned to pipe B The Sprite color adjustment registers are not double buffered and take effect immediately.

SPBCNTR—Sprite B Control Register

Memory Offset Address: 72280h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

The active set of basic control registers will be updated on the VBlank (of the currently selected pipe) after the "trigger" register (the Start Address register or the Control register when plane enable bit transitioning from a zero to a one) is written – thus providing an atomic update of all display controls with the exception of the Sprite B color control registers. If the currently selected pipe is disabled, the VBLANK of the active pipe is used. At least one pipe must be enabled and running for the display plane to be enabled.

Bit	Descriptions
31	**Sprite B Enable:** This bit will enable or disable the Sprite B. When this bit is set, the plane will generate pixels for display to be combined by the blender for the target pipe. When set to zero, memory fetches cease and display is blanked (from this plane) at the next VBLANK event from the pipe that this plane is assigned. At least one of the display pipes must be enabled to enable this plane. There is an override for the enable of this plane in the Pipe Configuration register. This bit only has an effect when the plane is not trusted. When the plane is marked trusted, this bit will be overridden and the display disabled when the registers are unlocked. 1 = Enable0 = Disable
30	**Sprite B Gamma Enable:** There are two gamma adjustments possible in the Sprite B data path. This bit controls the gamma correction in the display pipe not the gamma control in this plane. It affects only the pixel data from this display plane. For pixel format of 8-bit indexed, this bit should be set to a one. Gamma correction logic that is contained in the Sprite B logic is disabled by loading the default values into those registers. When this plane is marked as trusted, this bit should always be set to zero to force the pipe gamma to be always be bypassed. 0 = Sprite B pixel data bypasses the display pipe gamma correction logic (default). 1 = Sprite B pixel data is gamma corrected in the pipe gamma correction logic
29:26	**Sprite B Source Pixel Format:** This field selects the pixel format for the sprite/Sprite B. Pixel formats with an alpha channel should not use source keying. Before entering the blender, each source format is converted to 10 bits per pixel (details are described in the intermediate precision for the blender section of the Display Functions chapter). 0000 = YUV 4:2:2 packed (see byte order below). 0001 = Reserved0010 = 8-bpp Indexed. 0011 = Reserved. 0100 = Reserved. 0101 = 16-bit BGRX (5:6:5:0) pixel format (XGA compatible). 0110 = 32-bit BGRX (8:8:8:8) pixel format. Ignore alpha. 0111 = 32-bit BGRA (8:8:8:8) pixel format with pre-multiplied alpha channel. 1000 = 32-bit RGBX (10:10:10:2) pixel format. Ignore alpha. 1001 = 32-bit RGBA (10:10:10:2) pixel format 1010 = Reserved.1011 = Reserved. 1100 = Reserved.1101 = Reserved. 1110 = 32-bit RGBX (8:8:8:8) pixel format. Ignore alpha. 1111 = 32-bit RGBA (8:8:8:8)

25:24	Reserved
23	Reserved
22	**Sprite Source Key Enable:** When used as a sprite in the 16/32-bpp modes without alpha this enables source color keying. Sprite pixel values that match (within range) the key will become transparent. Setting this bit is not allowed when the Sprite B pixel format includes an alpha channel. 0 = Sprite source key is disabled (default) 1 = Sprite source key is enabled.
21:20	**Pixel Multiply:** This cause the display plane to duplicate lines and pixels sent to the assigned pipe. In the line/pixel doubling mode, the horizontal pixels are doubled and lines are sent twice. This is a method of scaling the source image by two (both H and V). 00 = No line/Pixel duplication 01 = Line/Pixel Doubling 10 = Line Doubling only 11 = Pixel Doubling only
19	**Color Conversion Disabled:** This bit enables or disables the color conversion logic. Color conversion is intended to be used with the formats that support YUV formats such as the YUV 4:2:2 packed format and x:8:8:8 and 8:8:8:8 formats. Formats such as RGB5:5:5 and 5:6:5 do not have YUV versions. 0 = Pixel data is sent through the conversion logic (only applies to YUV formats) 1 = Pixel data is not sent through the YUV->RGB conversion logic.
18	**YUV Format:** This bit specifies the source YUV format for the YUV to RGB color conversion operation. This field is ignored when source data is RGB. 0 = ITU-R Recommendation BT.601 1 = ITU-R Recommendation BT.709
17:16	**YUV byte Order:** This field is used to select the byte order when using YUV 4:2:2 data formats. For other formats, this field is ignored. 00 = YUYV01 = UYVY10 = YVYU11 = VYUY
15	**180° Display Rotation:** This mode causes the display plane to be rotated 180°. In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image and calculate the x, y offset as relative to the lower right corner. 0 = No rotation 1 = 180° rotation

<table>
<tr><td>14:11</td><td>Reserved</td></tr>
<tr><td>10</td><td>Tiled Surface: This bit indicates that the Sprite B surface data is in tiled memory. The tile pitch is specified in bytes in the DSPCSTRIDE register. Only X tiling is supported for display surfaces.
When this bit is set, it affects the hardware interpretation of the DSPCTILEOFF, DSPCLINOFF, and DSPCSURFADDR registers.
0 = Sprite B surface uses linear memory
1 = Sprite B surface uses X-tiled memory</td></tr>
<tr><td>9:3</td><td>Reserved: Write as zero</td></tr>
<tr><td>2</td><td>Sprite B Bottom: This bit will force the Sprite B plane to be on the bottom of the Z order. If the plane is marked as trusted, it only applies to the Z order of the trusted planes.0 = Sprite B Z order is determined by the other control bits1 = Sprite B is forced to be on the bottom of the Z order.</td></tr>
<tr><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>Sprite B Z-order: With Sprite A and B z-order, bottom control bits, Sprite B plane is placed in a specific z-order among other planes in pipe A.
<table>
<tr><td colspan="6">Display Pipe A Z-orders</td></tr>
<tr><td>SAzorder</td><td>SAbottom</td><td>SBzorder</td><td>SBbottom</td><td>Resulting Pipe Z-order (from bottom to top)</td><td>Source Keying</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>PA SA SB CA</td><td>PA in Black</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>PA SB SA CA</td><td>PA in Black</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>SB PA SA CA</td><td>use src keying on SB</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>SB PA SA CA</td><td>use src keying on SB</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>SB SA PA CA</td><td>use src keying on SA</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>SB SA PA CA</td><td>use src keying on SA</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>SA PA SB CA</td><td>use src keying on SA</td></tr>
</table></td></tr>
</table>

	1	1	0	0	SA PA SB CA	use src keying on SA
	0	1	1	0	SA SB PA CA	use src keying on SB
	1	1	1	0	SA SB PA CA	use src keying on SB
	0: Sprite B z-order is disabled 1: Sprite B z-order is enabled					

SPBLINOFF —Sprite B Linear Offset Register

Memory Offset Address: 72284h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

This register specifies the panning for the display surface. The surface base address is specified in the DSPCSURFADDR register, and this register is used to describe an offset from that base address. Bit 10 of DSPCCNTR specifies whether the display A surface is in linear or tiled memory. When the surface is in linear memory, this field contains the byte offset of the plane data in graphics memory. When the surface is tiled, the contents of this register are ignored. For YUV422 format, the linear offset value should be of even value.

This register can be written directly through software or by load register immediate command packets in the command stream.

This register is double buffered by VSYNC only. A change to this register will take affect on the next vsync following the write.

Bit	Descriptions
31:0	**Sprite B Offset:** This register provides the panning offset into the Sprite B plane. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset must be at least pixel aligned. This offset is the difference between the address of the upper left pixel to be displayed and the display surface address. When performing 180° rotation, this offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address.

SPBSTRIDE—Sprite B Stride Register

Memory Offset Address: 72288h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

Bit	Descriptions
31:6	**Sprite B Stride:** This is the stride for Sprite B in bytes. When using linear memory, this must be 64 byte aligned. When using tiled memory, this must be 256 byte aligned. This register is updated through a command packet passed through the command stream or writes to this register. When it is desired to update both this and the start register, the stride register must be written first because the write to the start register is the trigger that causes the update of both registers on the next VBLANK event. When using tiled memory, the actual memory buffer stride is limited to a maximum of 16K bytes.
5:0	Reserved

SPBPOS—Sprite Position Register

Memory Offset Address: 7228Ch

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

These registers specify the screen position and size of the sprite. This register is double buffered. The load register is transferred into the active register on the asserting edge of Vertical Blank for the pipe that the display is assigned. When using the sprite as a secondary display, this should be set to the entire display rectangle.

Bit	Descriptions
31:28	**Reserved:** Write as zero
27:16	**SpriteY-Position:** These 12 bits specify the vertical position in lines of the sprite (upper left corner) relative to the beginning of the active video area. When performing 180° rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	**Reserved:** Write as zero
11:0	**Sprite X-Position:** These 12 bits specify the horizontal position in pixels of the sprite (upper left corner) relative the beginning of the active video area. When performing 180° rotation, this field

	specifies the horizontal position of the original lower right corner relative to the original end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.

SPBSIZE—Sprite Height and Width Register

Memory Offset Address: 72290h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

This register specifies the height and width of the sprite in pixels and lines. The rectangle defined by the size and position should never exceed the boundaries of the display rectangle that the sprite is assigned to.

Bit	Descriptions
31:28	**Reserved:** Write as zero
27:16	**Sprite Height:** This register field is used to specify the height of the sprite in lines. The value in the register is the height minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	**Reserved:** Write as zero
11:0	**Sprite Width:** This register field is used to specify the width of the sprite in pixels. This does not have to be the same as the stride but should be less than or equal to the stride (converted to pixels). The value in the register is the width minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image. The sprite width is limited to even values when YUV source pixel format is used (actual width, not the width minus one value).

SPBKEYMINVAL—Sprite Color Key Min Value Register

Memory Offset Address: 72294h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

This register specifies the key color to be used with the mask bits to determine if the sprite source data matches the key. This register will only have an effect when the sprite color key is enabled. The unused bits of the 5:5:5 or 5:6:5 formats must be filled with duplicates of the three or two MSBs of the pixel value.

For YUV sprite data, each yuv channel data is compared with the corresponding channel's key color Low and High (each channel inrange can be masked out). If all three channels are in range between the low and high key values, it is considered source compared.

For RGB sprite data, each 24-bit RGB pixel data is compared with the 24-bit key value (note it only uses the 24-bit Low key value for comparison). Each 24-bit has to be equal (each bit comparison can also be masked out) for the source compared.

Bit	Descriptions
31:24	**Reserved:** Write as zero
23:16	**Red Key Min Value:** Specifies the color key minimum value for the sprite red/Cr channel.
15:8	**Green Key Min Value:** Specifies the color key minimum value for the sprite green/Y channel.
7:0	**Blue Key Min Value:** Specifies the color key minimum value for the sprite blue/Cb channel.

SPBKEYMSK—Sprite Color Key Mask Register

Memory Offset Address: 72298h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

Bit	Descriptions
31:3	**Reserved:** Write as zero
2	**Red Channel Enable:** Specifies the source color key enable for the red/Cr channel.
1	**Green Channel Enable:** Specifies the source color key enable for the green/Y channel.
0	**Blue Channel Enable:** Specifies the source color key enable for the blue/Cb channel

SPBSURF—Sprite B Surface Address Register

Memory Offset Address: 7229Ch

Default Value: 00000000h

Normal Access: Read/Write Double buffered

Writing to this register triggers the display plane flip. When it is desired to change multiple Sprite B registers, this register should be written last as a write to this register will cause all new register values to take effect.

<table>
<tr><th>Bit</th><th>Descriptions</th></tr>
<tr><td>31:12</td><td>Sprite B Surface Base Address: This address specifies the surface base address. When the surface is tiled, panning is specified using (x, y) offsets in the DSPCTILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DSPCLINOFF register.

This address must be 4K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT.

The value in this register is updated through the command streamer during synchronous flips.</td></tr>
<tr><td>11:4</td><td>Reserved: MBZ</td></tr>
<tr><td>3</td><td>Flip_Source

Project: All

Default Value: 0b

This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination.

<table>
<tr><th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr>
<tr><td>0b</td><td>CS</td><td>Flip source is CS</td><td>All</td></tr>
<tr><td>1b</td><td>BCS</td><td>Flip source is BCS</td><td>All</td></tr>
</table></td></tr>
<tr><td>2</td><td>Reserved</td></tr>
<tr><td>1:0</td><td>Reserved: MBZ</td></tr>
</table>

SPBKEYMAXVAL—Sprite Color Key Max Value Register

Memory Offset Address: 722A0h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

This register specifies the key color to be used with the mask bits to determine if the sprite source data matches the key. This register will only have an effect when the sprite color key is enabled.

Bit	Descriptions
31:24	**Reserved:** Write as zero
23:16	**Red Key Max Value:** Specifies the color key value for the sprite red/Cr channel.
15:8	**Green Key Max Value:** Specifies the color key value for the sprite green/Y channel.
7:0	**Blue Key Max Value:** Specifies the color key value for the sprite blue/Cb channel.

SPBTILEOFF—Sprite B Tiled Offset Register

Memory Offset Address: 722A4h

Default Value: 00000000h

Normal Access: Read/Write Double buffered

This register specifies the panning for the display surface. The surface base address is specified in the DSPCSURFADDR register, and this register is used to describe an offset from that base address. Bit 10 of DSPCCNTR specifies whether the display A surface is in linear or tiled memory. When the surface is in linear memory, the offset is specified in the DSPCLINOFF register and the contents of this register are ignored. When the surface is tiled, the start position is specified in this register as an (x, y) offset from the beginning of the surface.

This register can be written directly through software or by load register immediate command packets in the command stream.

This register is double buffered by VSYNC only. A change to this register will take affect on the next vsync following the write.

Bit	Descriptions
31:28	**Reserved:** Write as zero
27:16	**Plane Start Y-Position:** These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180° rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.
15:12	**Reserved:** Write as zero
11:0	**Plane Start X-Position:** These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180° rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the unrotated orientation.

SPBContAlpha—Sprite B Constant Alpha Register

Memory Offset Address: 722A8h

Default Value: 00000000h

Normal Access: Read/Write Double buffered

Bit	Description
31	**Enable Constant Alpha:** Sprite B Sprite constant alpha provides a way to apply an alpha value to all video sprite pixels. Each pixel color channel is multiplied by the constant alpha before proceeding to the blender. This can be used to create fade out effects. This is intended for CE device use where the video sprite might still be used to generate video output. 0 – Sprite B Sprite Constant Alpha is disabled 1 – Sprite B Sprite Constant Alpha is enabled
30:8	Reserved: MBZ
7:0	**Sprite B Constant Alpha Value:** This field provides the alpha value when constant alpha is enabled. A value of FF means fully opaque and a value of zero means fully transparent. Values in between those values allow for a blending of sprite with other surfaces.

SPBLIVESURF—Sprite B Live Surface Address Register

Memory Offset Address: 722ACh

Default Value: 00000000h

Normal Access: Read Only

Bit	Descriptions
31:12	**Sprite B Live Surface Base Address:** This gives the live value of the surface base address as being currently used for Sprite B plane.
11:4	**Reserved: MBZ**
3	Flip_Source Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination.

	Value	Name	Description	Project
	0b	CS	Flip source is CS	All
	1b	BCS	Flip source is BCS	All
2	**Reserved**			
1:0	**Reserved: MBZ**			

Sprite B Color Adjustment

These functions provide mechanisms for control of image colors generated from Sprite B sources. These functions are mainly intended for use for YUV color format sources. Adjustments are made before the YUV to RGB conversion. They take effect even when the Conversion Bypass bit is set. For display source input data in RGB format, software must set all the color correction registers to their default values (equivalent to a bypass mode). **These registers are not double buffered, take effect immediately after loading.**

SPBCLRC0—Sprite B Color Correction 0 Register

Address Offset:722D0h

Default Value: 01000000h

Normal Access: RW

Size: 32 bits

Bit	Description
31:27	Reserved:
26:18	**Contrast:** Contrast adjustment applies to YUV data. The Y channel is multiplied by the value contained in the register field. This signed fixed-point number is in 3i.6f format with the first 3 MSBs as the integer value and the last 6 LSBs as the fraction value. The allowed contrast value ranges from 0 to 7.53125 decimal. Bypassing Contrast, for YUV modes and for source data in RGB format, is accomplished by programming this field to a field value that represents 1.0 decimal or 001.000000 binary .
17:8	Reserved:
7:0	**Brightness:** This field provides the brightness adjustment with a 8-bit 2's compliment value ranging [-128, +127]. This value is added to the Y value after contrast multiply and before YUV to RGB conversion. A value of zero disables this adjustment affect. This 8-bit signed value provides half of the achievable brightness adjustment dynamic range. A full range brightness value would have a programmable range of [-255, +255].

	Bypassing Brightness for YUV formats and for source data in RGB format, is accomplished by programming this field to 0.

SPBGAMC0— Sprite B Gamma Correction Registers

Address Offset:722F4h

Default Value: 00080808h

Normal Access: R/W

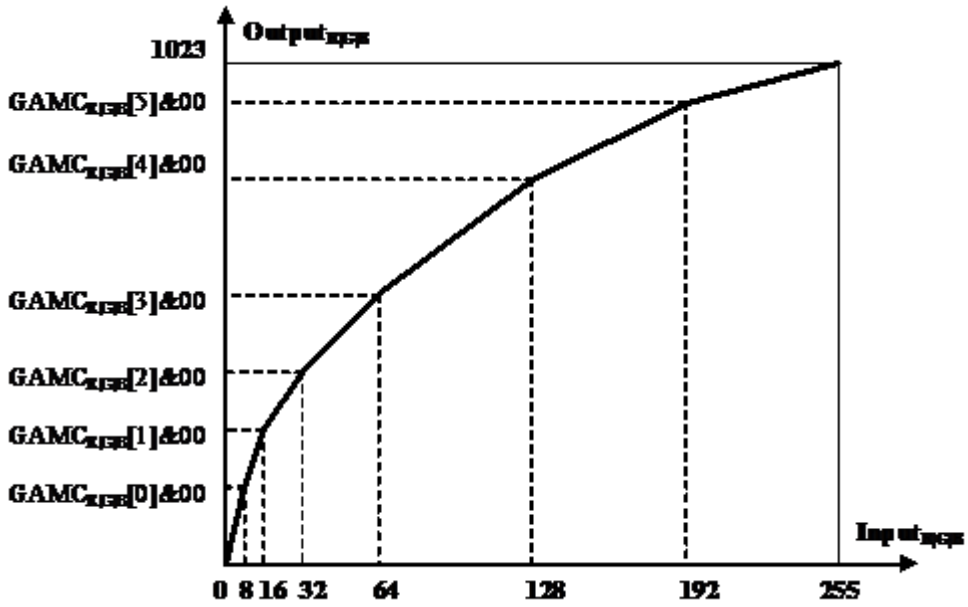
Size: 32 bits

These registers are used to determine the characteristics of the gamma correction for the Sprite B pixel data pre-blending. Additional gamma correction can be done in the display pipe gamma if desired. The pixels input to the gamma correction are 8 bit per channel pixels, and the output of the gamma correction is 10 bit per channel pixels. The gamma curve is represented by specifying a set of points along the curve. Each register has 32 bits, which are written to and read from together when accessed by the software. They are the six individual breakpoints on a logarithmically spaced color intensity space as shown in the following figure. The 8 bit values in the register are extended to 10 bit values in hardware by concatenating two zeroes onto the LSBs. The two end points (0 and 1023) have fixed values 0 and 1023, respectively. The appropriate Gamma breakpoint pairs (adjacent) are selected for each color component (Red, Green and Blue), and the output is interpolated between these two breakpoint values. The Gamma Correction registers (GAMC0 to GAMC5) are not double-buffered. They should be updated when the overlay is off. Otherwise, screen artifacts may show.

When the output from overlay is set in YUV format by programming CSC bypass, normally software should also bypass this gamma unit. However, since this gamma unit can also be viewed as a nonlinear transformation, it can be used, for whatever reason, in YUV output mode. In this case, the mapping of the three sets of piecewise linear map are as the following:

Bit	Description
31:24	Reserved:
23:16	Red (V/Cr):
15:8	Green (Y):
7:0	Blue (U/Cb):

Figure 11-2. Programming of the Piecewise-linear Estimation of Gamma Correction Curve



SPBGAMC1— Sprite B Gamma Correction Registers

Address Offset:722F0h

Default Value: 00101010h

Normal Access: R/W

Size: 32 bits

Same as previous register.

Bit	Description
31:24	Reserved:
23:16	Red (V/Cr):
15:8	Green (Y):
7:0	Blue (U/Cb):

SPBGAMC2— Sprite B Gamma Correction Registers

Address Offset:722ECh

Default Value: 00202020h

Normal Access: R/W

Size: 32 bits

Same as previous register.

Bit	Description
31:24	Reserved:
23:16	Red (V/Cr):
15:8	Green (Y):
7:0	Blue (U/Cb):

SPBGAMC3— Sprite B Gamma Correction Registers

Address Offset:722E8h

Default Value: 00404040h

Normal Access: R/W

Size: 32 bits

Same as previous register.

Bit	Description
31:24	Reserved:
23:16	Red (V/Cr):
15:8	Green (Y):
7:0	Blue (U/Cb):

SPBGAMC4— Sprite B Gamma Correction Registers

Address Offset:722E4h

Default Value: 00808080h

Normal Access: R/W

Size: 32 bits

Same as previous register.

Bit	Description
31:24	Reserved:
23:16	Red (V/Cr):
15:8	Green (Y):

7:0	Blue (U/Cb):

SPBGAMC5— Sprite B Gamma Correction Registers

Address Offset:722E0h

Default Value: 00C0C0C0h

Normal Access: R/W

Size: 32 bits

Same as previous register.

Bit	Description
31:24	Reserved:
23:16	Red (V/Cr):
15:8	Green (Y):
7:0	Blue (U/Cb):

Sprite C Control Registers

All of the basic control Sprite A, Sprite B, Sprite C, Sprite D registers are double buffered. The active set is updated after the trigger register is written followed by a VBLANK event. Sprite A, Sprite B are always assigned to pipe A. Sprite C, Sprite D are always assigned to pipe B The Sprite color adjustment registers are not double buffered and take effect immediately.

SPCCNTR—Sprite C Control Register

Memory Offset Address: 72380h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

The active set of basic control registers will be updated on the VBlank (of the currently selected pipe) after the "trigger" register (the Start Address register or the Control register when plane enable bit transitioning from a zero to a one) is written – thus providing an atomic update of all display controls with the exception of the Sprite C color control registers. If the currently selected pipe is disabled, the VBLANK of the active pipe is used. At least one pipe must be enabled and running for the display plane to be enabled.

Bit	Descriptions
31	**Sprite C Enable:** This bit will enable or disable the Sprite C. When this bit is set, the plane will

	generate pixels for display to be combined by the blender for the target pipe. When set to zero, memory fetches cease and display is blanked (from this plane) at the next VBLANK event from the pipe that this plane is assigned. At least one of the display pipes must be enabled to enable this plane. There is an override for the enable of this plane in the Pipe Configuration register. This bit only has an effect when the plane is not trusted. When the plane is marked trusted, this bit will be overridden and the display disabled when the registers are unlocked. 1 = Enable0 = Disable
30	**Sprite C Gamma Enable:** There are two gamma adjustments possible in the Sprite C data path. This bit controls the gamma correction in the display pipe not the gamma control in this plane. It affects only the pixel data from this display plane. For pixel format of 8-bit indexed, this bit should be set to a one. Gamma correction logic that is contained in the Sprite C logic is disabled by loading the default values into those registers. When this plane is marked as trusted, this bit should always be set to zero to force the pipe gamma to be always be bypassed. 0 = Sprite C pixel data bypasses the display pipe gamma correction logic (default). 1 = Sprite C pixel data is gamma corrected in the pipe gamma correction logic
29:26	**Sprite C Source Pixel Format:** This field selects the pixel format for the sprite/Sprite C. Pixel formats with an alpha channel should not use source keying. Before entering the blender, each source format is converted to 10 bits per pixel (details are described in the intermediate precision for the blender section of the Display Functions chapter). 0000 = YUV 4:2:2 packed (see byte order below). 0001 = Reserved0010 = 8-bpp Indexed. 0011 = Reserved.0100 = Reserved. 0101 = 16-bit BGRX (5:6:5:0) pixel format (XGA compatible). 0110 = 32-bit BGRX (8:8:8:8) pixel format. Ignore alpha. 0111 = 32-bit BGRA (8:8:8:8) pixel format with pre-multiplied alpha channel. 1000 = 32-bit RGBX (10:10:10:2) pixel format. Ignore alpha. 1001 = 32-bit RGBA (10:10:10:2) pixel format 1010 = Reserved. 1011 = Reserved. 1100 = Reserved. 1101 = Reserved. 1110 = 32-bit RGBX (8:8:8:8) pixel format. Ignore alpha. 1111 = 32-bit RGBA (8:8:8:8)
25:24	Sprite C Pipe Select: Sprite C always ties to Pipe B

	Reserved.
23	Reserved:
22	**Sprite Source Key Enable:** When used as a sprite in the 16/32-bpp modes without alpha this enables source color keying. Sprite pixel values that match (within range) the key will become transparent. Setting this bit is not allowed when the Sprite C pixel format includes an alpha channel. 0 = Sprite source key is disabled (default) 1 = Sprite source key is enabled.
21:20	**Pixel Multiply:** This cause the display plane to duplicate lines and pixels sent to the assigned pipe. In the line/pixel doubling mode, the horizontal pixels are doubled and lines are sent twice. This is a method of scaling the source image by two (both H and V). 00 = No line/Pixel duplication 01 = Line/Pixel Doubling 10 = Line Doubling only 11 = Pixel Doubling only
19	**Color Conversion Disabled:** This bit enables or disables the color conversion logic. Color conversion is intended to be used with the formats that support YUV formats such as the YUV 4:2:2 packed format and x:8:8:8 and 8:8:8:8 formats. Formats such as RGB5:5:5 and 5:6:5 do not have YUV versions. 0 = Pixel data is sent through the conversion logic (only applies to YUV formats) 1 = Pixel data is not sent through the YUV->RGB conversion logic.
18	**YUV Format:** This bit specifies the source YUV format for the YUV to RGB color conversion operation. This field is ignored when source data is RGB. 0 = ITU-R Recommendation BT.601 1 = ITU-R Recommendation BT.709
17:16	**YUV byte Order:** This field is used to select the byte order when using YUV 4:2:2 data formats. For other formats, this field is ignored. 00 = YUYV01 = UYVY10 = YVYU11 = VYUY
15	**180° Display Rotation:** This mode causes the display plane to be rotated 180°. In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image and calculate the x, y offset as relative to the lower right corner. 0 = No rotation 1 = 180° rotation

<table>
<tr><td>14:11</td><td>Reserved</td></tr>
<tr><td>10</td><td>Tiled Surface: This bit indicates that the Sprite C surface data is in tiled memory. The tile pitch is specified in bytes in the DSPCSTRIDE register. Only X tiling is supported for display surfaces.
When this bit is set, it affects the hardware interpretation of the DSPCTILEOFF, DSPCLINOFF, and DSPCSURFADDR registers.
0 = Sprite C surface uses linear memory
1 = Sprite C surface uses X-tiled memory</td></tr>
<tr><td>9:3</td><td>Reserved: Write as zero</td></tr>
<tr><td>2</td><td>Sprite C Bottom: This bit will force the Sprite C plane to be on the bottom of the Z order. If the plane is marked as trusted, it only applies to the Z order of the trusted planes.0 = Sprite C Z order is determined by the other control bits1 = Sprite C is forced to be on the bottom of the Z order.</td></tr>
<tr><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>Sprite C Z-order: With Sprite C and D z-order, bottom control bits, Sprite C plane is placed in a specific z-order among other planes in pipe B.
<table>
<tr><td colspan="6">Display Pipe B Z-orders</td></tr>
<tr><td>SCzorder</td><td>SCbottom</td><td>SDzorder</td><td>SDbottom</td><td>Resulting Pipe Z-order (from bottom to top)</td><td>Source Keying</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>PB SC SD CB</td><td>PB in Black</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>PB SD SC CB</td><td>PB in Black</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>SD PB SC CB</td><td>use src keying on SD</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>SD PB SC CB</td><td>use src keying on SD</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>SD SC PB CB</td><td>use src keying on SC</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>SD SC PB CB</td><td>use src keying on SC</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>SC PB SD CB</td><td>use src keying on SC</td></tr>
</table></td></tr>
</table>

	1	1	0	0	SC PB SD CB	use src keying on SC
	0	1	1	0	SC SD PB CB	use src keying on SD
	1	1	1	0	SC SD PB CB	use src keying on SD
	0	1	0	1	Not Allowed	
	0	1	1	1	Not Allowed	
	1	1	0	1	Not Allowed	
	1	1	1	1	Not Allowed	
	1	0	1	0	Not Allowed	
	1	0	1	1	Not Allowed	
	0: Sprite C z-order is disabled 1: Sprite C z-order is enabled					

SPCLINOFF —Sprite C Linear Offset Register

Memory Offset Address: 72384h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

This register specifies the panning for the display surface. The surface base address is specified in the DSPCSURFADDR register, and this register is used to describe an offset from that base address. Bit 10 of DSPCCNTR specifies whether the display A surface is in linear or tiled memory. When the surface is in linear memory, this field contains the byte offset of the plane data in graphics memory. When the surface is tiled, the contents of this register are ignored. For YUV422 format, the linear offset value should be of even value.

This register can be written directly through software or by load register immediate command packets in the command stream.

This register is double buffered by VSYNC only. A change to this register will take affect on the next vsync following the write.

Bit	Descriptions

31:0	**Sprite C Offset:** This register provides the panning offset into the Sprite C plane. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset must be at least pixel aligned. This offset is the difference between the address of the upper left pixel to be displayed and the display surface address. When performing 180° rotation, this offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address.

SPCSTRIDE—Sprite C Stride Register

Memory Offset Address: 72388h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

Bit	Descriptions
31:6	**Sprite C Stride:** This is the stride for Sprite C in bytes. When using linear memory, this must be 64 byte aligned. When using tiled memory, this must be 256 byte aligned. This register is updated through a command packet passed through the command stream or writes to this register. When it is desired to update both this and the start register, the stride register must be written first because the write to the start register is the trigger that causes the update of both registers on the next VBLANK event. When using tiled memory, the actual memory buffer stride is limited to a maximum of 16K bytes.
5:0	Reserved

SPCPOS—Sprite C Position Register

Memory Offset Address: 7238Ch

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

These registers specify the screen position and size of the sprite. This register is double buffered. The load register is transferred into the active register on the asserting edge of Vertical Blank for the pipe that the display is assigned. When using the sprite as a secondary display, this should be set to the entire display rectangle.

Bit	Descriptions
31:28	**Reserved:** Write as zero
27:16	**SpriteY-Position:** These 12 bits specify the vertical position in lines of the sprite (upper left corner) relative to the beginning of the active video area. When performing 180° rotation, this

	field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	**Reserved:** Write as zero
11:0	**Sprite X-Position:** These 12 bits specify the horizontal position in pixels of the sprite (upper left corner) relative the beginning of the active video area. When performing 180° rotation, this field specifies the horizontal position of the original lower right corner relative to the original end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.

SPCSIZE—Sprite C Height and Width Register

Memory Offset Address: 72390h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

This register specifies the height and width of the sprite in pixels and lines. The rectangle defined by the size and position should never exceed the boundaries of the display rectangle that the sprite is assigned to.

Bit	Descriptions
31:28	**Reserved:** Write as zero
27:16	**Sprite Height:** This register field is used to specify the height of the sprite in lines. The value in the register is the height minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	**Reserved:** Write as zero
11:0	**Sprite Width:** This register field is used to specify the width of the sprite in pixels. This does not have to be the same as the stride but should be less than or equal to the stride (converted to pixels). The value in the register is the width minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image. The sprite width is limited to even values when YUV source pixel format is used (actual width, not the width minus one value).

SPCKEYMINVAL—Sprite C Color Key Min Value Register

Memory Offset Address: 72394h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

This register specifies the key color to be used with the mask bits to determine if the sprite source data matches the key. This register will only have an effect when the sprite color key is enabled. The unused bits of the 5:5:5 or 5:6:5 formats must be filled with duplicates of the three or two MSBs of the pixel value.

For YUV sprite data, each yuv channel data is compared with the corresponding channel's key color Low and High (each channel inrange can be masked out). If all three channels are in range between the low and high key values, it is considered source compared.

For RGB sprite data, each 24-bit RGB pixel data is compared with the 24-bit key value (note it only uses the 24-bit Low key value for comparison). Each 24-bit has to be equal (each bit comparison can also be masked out) for the source compared.

Bit	Descriptions
31:24	**Reserved:** Write as zero
23:16	**Red Key Min Value:** Specifies the color key minimum value for the sprite red/Cr channel.
15:8	**Green Key Min Value:** Specifies the color key minimum value for the sprite green/Y channel.
7:0	**Blue Key Min Value:** Specifies the color key minimum value for the sprite blue/Cb channel.

SPCKEYMSK—Sprite C Color Key Mask Register

Memory Offset Address: 72398h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

Bit	Descriptions
31:3	**Reserved:** Write as zero
2	**Red Channel Enable:** Specifies the source color key enable for the red/Cr channel.
1	**Green Channel Enable:** Specifies the source color key enable for the green/Y channel.
0	**Blue Channel Enable:** Specifies the source color key enable for the blue/Cb channel

SPCSURF—Sprite C Surface Address Register

Memory Offset Address: 7239Ch

Default Value: 00000000h

Normal Access: Read/Write Double buffered

Writing to this register triggers the display plane flip. When it is desired to change multiple Sprite C registers, this register should be written last as a write to this register will cause all new register values to take effect.

<table>
<tr><th>Bit</th><th>Descriptions</th></tr>
<tr><td>31:12</td><td>Sprite C Surface Base Address: This address specifies the surface base address. When the surface is tiled, panning is specified using (x, y) offsets in the DSPCTILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DSPCLINOFF register.
This address must be 4K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT.
The value in this register is updated through the command streamer during synchronous flips.</td></tr>
<tr><td>11:4</td><td>Reserved: MBZ</td></tr>
<tr><td>3</td><td>Flip_Source
Project: All
Default Value: 0b
This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr>
<tr><td>0b</td><td>CS</td><td>Flip source is CS</td><td>All</td></tr>
<tr><td>1b</td><td>BCS</td><td>Flip source is BCS</td><td>All</td></tr>
</table></td></tr>
<tr><td>2</td><td>Reserved</td></tr>
<tr><td>1:0</td><td>Reserved: MBZ</td></tr>
</table>

SPCKEYMAXVAL—Sprite C Color Key Max Value Register

Memory Offset Address: 723A0h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

This register specifies the key color to be used with the mask bits to determine if the sprite source data matches the key. This register will only have an effect when the sprite color key is enabled.

Bit	Descriptions
31:24	**Reserved:** Write as zero
23:16	**Red Key Max Value:** Specifies the color key value for the sprite red/Cr channel.
15:8	**Green Key Max Value:** Specifies the color key value for the sprite green/Y channel.
7:0	**Blue Key Max Value:** Specifies the color key value for the Sprite Clue/Cb channel.

SPCTILEOFF—Sprite C Tiled Offset Register

Memory Offset Address: 723A4h

Default Value: 00000000h

Normal Access: Read/Write Double buffered

This register specifies the panning for the display surface. The surface base address is specified in the DSPCSURFADDR register, and this register is used to describe an offset from that base address. Bit 10 of DSPCCNTR specifies whether the display A surface is in linear or tiled memory. When the surface is in linear memory, the offset is specified in the DSPCLINOFF register and the contents of this register are ignored. When the surface is tiled, the start position is specified in this register as an (x, y) offset from the beginning of the surface.

This register can be written directly through software or by load register immediate command packets in the command stream.

This register is double buffered by VSYNC only. A change to this register will take affect on the next vsync following the write.

Bit	Descriptions
31:28	**Reserved:** Write as zero
27:16	**Plane Start Y-Position:** These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180° rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.
15:12	**Reserved:** Write as zero
11:0	**Plane Start X-Position:** These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180° rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active

	display plane in the unrotated orientation.

SPCContAlpha—Sprite C Constant Alpha Register

Memory Offset Address: 723A8h

Default Value: 00000000h

Normal Access: Read/Write Double buffered

Bit	Description
31	**Enable Constant Alpha:** Sprite C Sprite constant alpha provides a way to apply an alpha value to all video sprite pixels. Each pixel color channel is multiplied by the constant alpha before proceeding to the blender. This can be used to create fade out effects. This is intended for CE device use where the video sprite might still be used to generate video output. 0 – Sprite C Sprite Constant Alpha is disabled 1 – Sprite C Sprite Constant Alpha is enabled
30:8	Reserved: MBZ
7:0	**Sprite C Constant Alpha Value:** This field provides the alpha value when constant alpha is enabled. A value of FF means fully opaque and a value of zero means fully transparent. Values in between those values allow for a blending of sprite with other surfaces.

SPCLIVESURF—Sprite C Live Surface Address Register

Memory Offset Address: 723ACh

Default Value: 00000000h

Normal Access: Read Only

Bit	**Descriptions**
31:12	**Sprite C Live Surface Base Address:** This gives the live value of the surface base address as being currently used for Sprite C.
11:4	Reserved: MBZ
3	Flip_Source Project: All

	Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. Value / Name / Description / Project 0b / CS / Flip source is CS / All 1b / BCS / Flip source is BCS / All
2	**Reserved**
1:0	**Reserved: MBZ**

Sprite C Color Adjustment

These functions provide mechanisms for control of image colors generated from Sprite C sources. These functions are mainly intended for use for YUV color format sources. Adjustments are made before the YUV to RGB conversion. They take effect even when the Conversion Bypass bit is set. For display source input data in RGB format, software must set all the color correction registers to their default values (equivalent to a bypass mode). **These registers are not double buffered, take effect immediately after loading.**

SPCCLRC0—Sprite C Color Correction 0 Register

Address Offset:723D0h

Default Value: 01000000h

Normal Access: RW

Size: 32 bits

Bit	Description
31:27	Reserved:
26:18	**Contrast:** Contrast adjustment applies to YUV data. The Y channel is multiplied by the value contained in the register field. This signed fixed-point number is in 3i.6f format with the first 3 MSBs as the integer value and the last 6 LSBs as the fraction value. The allowed contrast value ranges from 0 to 7.53125 decimal. Bypassing Contrast, for YUV modes and for source data in RGB format, is accomplished by programming this field to a field value that represents 1.0 decimal or 001.000000 binary .
17:8	Reserved:

7:0	**Brightness:** This field provides the brightness adjustment with a 8-bit 2's compliment value ranging [-128, +127]. This value is added to the Y value after contrast multiply and before YUV to RGB conversion. A value of zero disables this adjustment affect. This 8-bit signed value provides half of the achievable brightness adjustment dynamic range. A full range brightness value would have a programmable range of [-255, +255]. Bypassing Brightness for YUV formats and for source data in RGB format, is accomplished by programming this field to 0.

SPCGAMC0— Sprite C Gamma Correction Registers

Address Offset:723F4h

Default Value: 00080808h

Normal Access: R/W

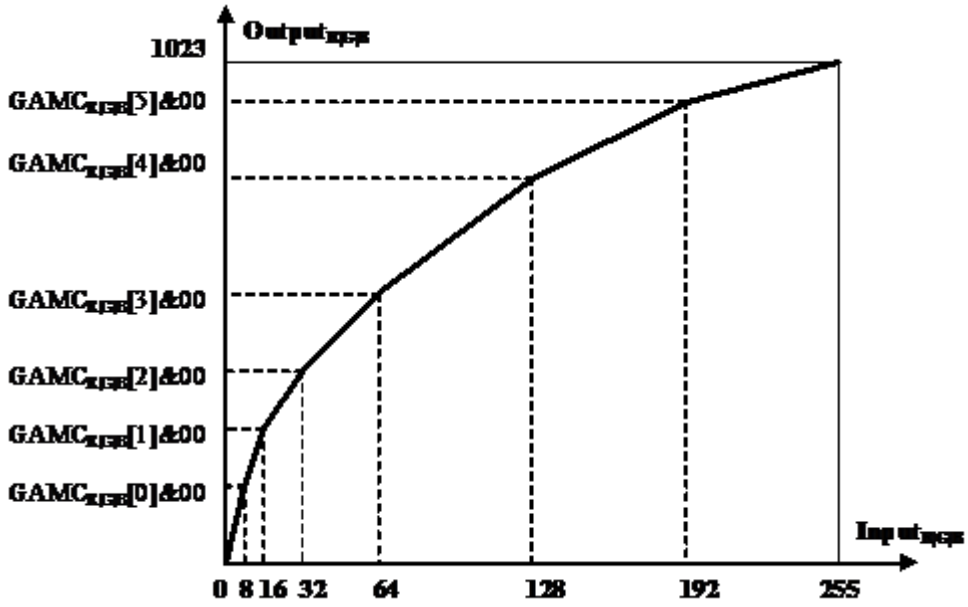
Size: 32 bits

These registers are used to determine the characteristics of the gamma correction for the Sprite C pixel data pre-blending. Additional gamma correction can be done in the display pipe gamma if desired. The pixels input to the gamma correction are 8 bit per channel pixels, and the output of the gamma correction is 10 bit per channel pixels. The gamma curve is represented by specifying a set of points along the curve. Each register has 32 bits, which are written to and read from together when accessed by the software. They are the six individual breakpoints on a logarithmically spaced color intensity space as shown in the following figure. The 8 bit values in the register are extended to 10 bit values in hardware by concatenating two zeroes onto the LSBs. The two end points (0 and 1023) have fixed values 0 and 1023, respectively. The appropriate Gamma breakpoint pairs (adjacent) are selected for each color component (Red, Green and Blue), and the output is interpolated between these two breakpoint values. The Gamma Correction registers (GAMC0 to GAMC5) are not double-buffered. They should be updated when the overlay is off. Otherwise, screen artifacts may show.

When the output from overlay is set in YUV format by programming CSC bypass, normally software should also bypass this gamma unit. However, since this gamma unit can also be viewed as a nonlinear transformation, it can be used, for whatever reason, in YUV output mode. In this case, the mapping of the three sets of piecewise linear map are as the following:

Bit	Description
31:24	Reserved:
23:16	Red (V/Cr):
15:8	Green (Y):
7:0	Blue (U/Cb):

Figure 11-3. Programming of the Piecewise-linear Estimation of Gamma Correction Curve



SPCGAMC1— Sprite C Gamma Correction Registers

Address Offset:723F0h

Default Value: 00101010h

Normal Access: R/W

Size: 32 bits

Same as previous register.

Bit	Description
31:24	Reserved:
23:16	Red (V/Cr):
15:8	Green (Y):
7:0	Blue (U/Cb):

SPCGAMC2— Sprite C Gamma Correction Registers

Address Offset:723ECh

Default Value: 00202020h

Normal Access: R/W

Size: 32 bits

Same as previous register.

Bit	Description
31:24	Reserved:
23:16	Red (V/Cr):
15:8	Green (Y):
7:0	Blue (U/Cb):

SPCGAMC3— Sprite C Gamma Correction Registers

Address Offset:723E8h

Default Value: 00404040h

Normal Access: R/W

Size: 32 bits

Same as previous register.

Bit	Description
31:24	Reserved:
23:16	Red (V/Cr):
15:8	Green (Y):
7:0	Blue (U/Cb):

SPCGAMC4— Sprite C Gamma Correction Registers

Address Offset:723E4h

Default Value: 00808080h

Normal Access: R/W

Size: 32 bits

Same as previous register.

Bit	Description
31:24	Reserved:
23:16	Red (V/Cr):
15:8	Green (Y):

7:0	Blue (U/Cb):

SPCGAMC5— Sprite C Gamma Correction Registers

Address Offset:723E0h

Default Value: 00C0C0C0h

Normal Access: R/W

Size: 32 bits

Same as previous register.

Bit	Description
31:24	Reserved:
23:16	Red (V/Cr):
15:8	Green (Y):
7:0	Blue (U/Cb):

Sprite D Control Registers

All of the basic control Sprite A, Sprite B, Sprite C, Sprite D registers are double buffered. The active set is updated after the trigger register is written followed by a VBLANK event. Sprite A, Sprite B are always assigned to pipe A. Sprite C, Sprite D are always assigned to pipe B The Sprite color adjustment registers are not double buffered and take effect immediately.

SPDCNTR—Sprite D Control Register

Memory Offset Address: 72480h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

The active set of basic control registers will be updated on the VBlank (of the currently selected pipe) after the “trigger” register (the Start Address register or the Control register when plane enable bit transitioning from a zero to a one) is written – thus providing an atomic update of all display controls with the exception of the Sprite D color control registers. If the currently selected pipe is disabled, the VBLANK of the active pipe is used. At least one pipe must be enabled and running for the display plane to be enabled.

Bit	Descriptions

31	**Sprite D Enable:** This bit will enable or disable the Sprite D. When this bit is set, the plane will generate pixels for display to be combined by the blender for the target pipe. When set to zero, memory fetches cease and display is blanked (from this plane) at the next VBLANK event from the pipe that this plane is assigned. At least one of the display pipes must be enabled to enable this plane. There is an override for the enable of this plane in the Pipe Configuration register. This bit only has an effect when the plane is not trusted. When the plane is marked trusted, this bit will be overridden and the display disabled when the registers are unlocked. 1 = Enable0 = Disable
30	**Sprite D Gamma Enable:** There are two gamma adjustments possible in the Sprite D data path. This bit controls the gamma correction in the display pipe not the gamma control in this plane. It affects only the pixel data from this display plane. For pixel format of 8-bit indexed, this bit should be set to a one. Gamma correction logic that is contained in the Sprite D logic is disabled by loading the default values into those registers. When this plane is marked as trusted, this bit should always be set to zero to force the pipe gamma to be always be bypassed. 0 = Sprite D pixel data bypasses the display pipe gamma correction logic (default). 1 = Sprite D pixel data is gamma corrected in the pipe gamma correction logic
29:26	**Sprite D Source Pixel Format:** This field selects the pixel format for the sprite/Sprite D. Pixel formats with an alpha channel should not use source keying. Before entering the blender, each source format is converted to 10 bits per pixel (details are described in the intermediate precision for the blender section of the Display Functions chapter). 0000 = YUV 4:2:2 packed (see byte order below). 0001 = Reserved 0010 = 8-bpp Indexed. 0011 = Reserved. 0100 = Reserved. 0101 = 16-bit BGRX (5:6:5:0) pixel format (XGA compatible). 0110 = 32-bit BGRX (8:8:8:8) pixel format. Ignore alpha. 0111 = 32-bit BGRA (8:8:8:8) pixel format with pre-multiplied alpha channel. 1000 = 32-bit RGBX (10:10:10:2) pixel format. Ignore alpha. 1001 = 32-bit RGBA (10:10:10:2) pixel format 1010 = Reserved. 1011 = Reserved. 1100 = Reserved. 1101 = Reserved.

	1110 = 32-bit RGBX (8:8:8:8) pixel format. Ignore alpha. 1111 = 32-bit RGBA (8:8:8:8)
25:24	Reserved.
23	Reserved:
22	**Sprite Source Key Enable:** When used as a sprite in the 16/32-bpp modes without alpha this enables source color keying. Sprite pixel values that match (within range) the key will become transparent. Setting this bit is not allowed when the Sprite D pixel format includes an alpha channel. 0 = Sprite source key is disabled (default) 1 = Sprite source key is enabled.
21:20	**Pixel Multiply:** This cause the display plane to duplicate lines and pixels sent to the assigned pipe. In the line/pixel doubling mode, the horizontal pixels are doubled and lines are sent twice. This is a method of scaling the source image by two (both H and V). 00 = No line/Pixel duplication 01 = Line/Pixel Doubling 10 = Line Doubling only 11 = Pixel Doubling only
19	**Color Conversion Disabled:** This bit enables or disables the color conversion logic. Color conversion is intended to be used with the formats that support YUV formats such as the YUV 4:2:2 packed format and x:8:8:8 and 8:8:8:8 formats. Formats such as RGB5:5:5 and 5:6:5 do not have YUV versions. 0 = Pixel data is sent through the conversion logic (only applies to YUV formats) 1 = Pixel data is not sent through the YUV->RGB conversion logic.
18	**YUV Format:** This bit specifies the source YUV format for the YUV to RGB color conversion operation. This field is ignored when source data is RGB. 0 = ITU-R Recommendation BT.601 1 = ITU-R Recommendation BT.709
17:16	**YUV byte Order:** This field is used to select the byte order when using YUV 4:2:2 data formats. For other formats, this field is ignored. 00 = YUYV01 = UYVY10 = YVYU11 = VYUY
15	**180° Display Rotation:** This mode causes the display plane to be rotated 180°. In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image and calculate the x, y offset as relative to the lower right corner.

<table>
<tr><td></td><td>0 = No rotation
1 = 180° rotation</td></tr>
<tr><td>14:11</td><td>Reserved</td></tr>
<tr><td>10</td><td>Tiled Surface: This bit indicates that the Sprite D surface data is in tiled memory. The tile pitch is specified in bytes in the DSPCSTRIDE register. Only X tiling is supported for display surfaces.
When this bit is set, it affects the hardware interpretation of the DSPCTILEOFF, DSPCLINOFF, and DSPCSURFADDR registers.
0 = Sprite D surface uses linear memory
1 = Sprite D surface uses X-tiled memory</td></tr>
<tr><td>9:3</td><td>Reserved: Write as zero</td></tr>
<tr><td>2</td><td>Sprite D Bottom: This bit will force the Sprite D plane to be on the bottom of the Z order. If the plane is marked as trusted, it only applies to the Z order of the trusted planes.0 = Sprite D Z order is determined by the other control bits1 = Sprite D is forced to be on the bottom of the Z order.</td></tr>
<tr><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>Sprite D Z-order: With Sprite C and D z-order, bottom control bits, Sprite D plane is placed in a specific z-order among other planes in pipe B.
<table>
<tr><td colspan="6">Display Pipe B Z-orders</td></tr>
<tr><td>SCzorder</td><td>SCbottom</td><td>SDzorder</td><td>SDbottom</td><td>Resulting Pipe Z-order (from bottom to top)</td><td>Source Keying</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>PB SC SD CB</td><td>PB in Black</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>PB SD SC CB</td><td>PB in Black</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>SD PB SC CB</td><td>use src keying on SD</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>SD PB SC CB</td><td>use src keying on SD</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>SD SC PB CB</td><td>use src keying on SC</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>SD SC PB CB</td><td>use src keying on SC</td></tr>
</table></td></tr>
</table>

0	1	0	0	SC PB SD CB	use src keying on SC
1	1	0	0	SC PB SD CB	use src keying on SC
0	1	1	0	SC SD PB CB	use src keying on SD
1	1	1	0	SC SD PB CB	use src keying on SD
0	1	0	1	Not Allowed	
0	1	1	1	Not Allowed	
1	1	0	1	Not Allowed	
1	1	1	1	Not Allowed	
1	0	1	0	Not Allowed	
1	0	1	1	Not Allowed	

0: Sprite D z-order is disabled

1: Sprite D z-order is enabled

SPDLINOFF —Sprite D Linear Offset Register

Memory Offset Address: 72484h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

This register specifies the panning for the display surface. The surface base address is specified in the DSPCSURFADDR register, and this register is used to describe an offset from that base address. Bit 10 of DSPCCNTR specifies whether the display A surface is in linear or tiled memory. When the surface is in linear memory, this field contains the byte offset of the plane data in graphics memory. When the surface is tiled, the contents of this register are ignored. For YUV422 format, the linear offset value should be of even value.

This register can be written directly through software or by load register immediate command packets in the command stream.

This register is double buffered by VSYNC only. A change to this register will take affect on the next vsync following the write.

Bit	Descriptions
31:0	**Sprite D Offset:** This register provides the panning offset into the Sprite D plane. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset must be at least pixel aligned. This offset is the difference between the address of the upper left pixel to be displayed and the display surface address. When performing 180° rotation, this offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address.

SPDSTRIDE—Sprite D Stride Register

Memory Offset Address: 72488h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

Bit	Descriptions
31:6	**Sprite D Stride:** This is the stride for Sprite D in bytes. When using linear memory, this must be 64 byte aligned. When using tiled memory, this must be 256 byte aligned. This register is updated through a command packet passed through the command stream or writes to this register. When it is desired to update both this and the start register, the stride register must be written first because the write to the start register is the trigger that causes the update of both registers on the next VBLANK event. When using tiled memory, the actual memory buffer stride is limited to a maximum of 16K bytes.
5:0	Reserved

SPDPOS—Sprite D Position Register

Memory Offset Address: 7248Ch

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

These registers specify the screen position and size of the sprite. This register is double buffered. The load register is transferred into the active register on the asserting edge of Vertical Blank for the pipe that the display is assigned. When using the sprite as a secondary display, this should be set to the entire display rectangle.

Bit	Descriptions
31:28	**Reserved:** Write as zero
27:16	**SpriteY-Position:** These 12 bits specify the vertical position in lines of the sprite (upper left corner) relative to the beginning of the active video area. When performing 180° rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	**Reserved:** Write as zero
11:0	**Sprite X-Position:** These 12 bits specify the horizontal position in pixels of the sprite (upper left corner) relative the beginning of the active video area. When performing 180° rotation, this field specifies the horizontal position of the original lower right corner relative to the original end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.

SPDSIZE—Sprite D Height and Width Register

Memory Offset Address: 72490h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

This register specifies the height and width of the sprite in pixels and lines. The rectangle defined by the size and position should never exceed the boundaries of the display rectangle that the sprite is assigned to.

Bit	Descriptions
31:28	**Reserved:** Write as zero
27:16	**Sprite Height:** This register field is used to specify the height of the sprite in lines. The value in the register is the height minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	**Reserved:** Write as zero
11:0	**Sprite Width:** This register field is used to specify the width of the sprite in pixels. This does not have to be the same as the stride but should be less than or equal to the stride (converted to pixels). The value in the register is the width minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image. The sprite width is limited to even values when YUV source pixel format is used (actual width, not the width minus one value).

SPDKEYMINVAL—Sprite D Color Key Min Value Register

Memory Offset Address: 72494h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

This register specifies the key color to be used with the mask bits to determine if the sprite source data matches the key. This register will only have an effect when the sprite color key is enabled. The unused bits of the 5:5:5 or 5:6:5 formats must be filled with duplicates of the three or two MSBs of the pixel value.

For YUV sprite data, each yuv channel data is compared with the corresponding channel's key color Low and High (each channel inrange can be masked out). If all three channels are in range between the low and high key values, it is considered source compared.

For RGB sprite data, each 24-bit RGB pixel data is compared with the 24-bit key value (note it only uses the 24-bit Low key value for comparison). Each 24-bit has to be equal (each bit comparison can also be masked out) for the source compared.

Bit	Descriptions
31:24	**Reserved:** Write as zero
23:16	**Red Key Min Value:** Specifies the color key minimum value for the sprite red/Cr channel.
15:8	**Green Key Min Value:** Specifies the color key minimum value for the sprite green/Y channel.
7:0	**Blue Key Min Value:** Specifies the color key minimum value for the sprite blue/Cb channel.

SPDKEYMSK—Sprite D Color Key Mask Register

Memory Offset Address: 72498h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

Bit	Descriptions
31:3	**Reserved:** Write as zero
2	**Red Channel Enable:** Specifies the source color key enable for the red/Cr channel.
1	**Green Channel Enable:** Specifies the source color key enable for the green/Y channel.
0	**Blue Channel Enable:** Specifies the source color key enable for the blue/Cb channel

SPDSURF—Sprite D Surface Address Register

Memory Offset Address: 7249Ch

Default Value: 00000000h

Normal Access: Read/Write Double buffered

Writing to this register triggers the display plane flip. When it is desired to change multiple Sprite D registers, this register should be written last as a write to this register will cause all new register values to take effect.

<table>
<tr><th>Bit</th><th>Descriptions</th></tr>
<tr><td>31:12</td><td>Sprite D Surface Base Address: This address specifies the surface base address. When the surface is tiled, panning is specified using (x, y) offsets in the DSPCTILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DSPCLINOFF register.
This address must be 4K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT.
The value in this register is updated through the command streamer during synchronous flips.</td></tr>
<tr><td>11:4</td><td>Reserved: MBZ</td></tr>
<tr><td>3</td><td>Flip_Source
Project: All
Default Value: 0b
This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination.
<table><tr><th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr><tr><td>0b</td><td>CS</td><td>Flip source is CS</td><td>All</td></tr><tr><td>1b</td><td>BCS</td><td>Flip source is BCS</td><td>All</td></tr></table></td></tr>
<tr><td>2</td><td>Reserved</td></tr>
<tr><td>1:0</td><td>Reserved: MBZ</td></tr>
</table>

SPDKEYMAXVAL—Sprite D Color Key Max Value Register

Memory Offset Address: 724A0h

Default Value: 00000000h

Normal Access: Read/Write Double Buffered

This register specifies the key color to be used with the mask bits to determine if the sprite source data matches the key. This register will only have an effect when the sprite color key is enabled.

Bit	Descriptions
31:24	**Reserved:** Write as zero
23:16	**Red Key Max Value:** Specifies the color key value for the sprite red/Cr channel.
15:8	**Green Key Max Value:** Specifies the color key value for the sprite green/Y channel.
7:0	**Blue Key Max Value:** Specifies the color key value for the Sprite blue/Cb channel.

SPDTILEOFF—Sprite D Tiled Offset Register

Memory Offset Address: 724A4h

Default Value: 00000000h

Normal Access: Read/Write Double buffered

This register specifies the panning for the display surface. The surface base address is specified in the DSPCSURFADDR register, and this register is used to describe an offset from that base address. Bit 10 of DSPCCNTR specifies whether the display A surface is in linear or tiled memory. When the surface is in linear memory, the offset is specified in the DSPCLINOFF register and the contents of this register are ignored. When the surface is tiled, the start position is specified in this register as an (x, y) offset from the beginning of the surface.

This register can be written directly through software or by load register immediate command packets in the command stream.

This register is double buffered by VSYNC only. A change to this register will take affect on the next vsync following the write.

Bit	Descriptions
31:28	**Reserved:** Write as zero
27:16	**Plane Start Y-Position:** These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180° rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.
15:12	**Reserved:** Write as zero
11:0	**Plane Start X-Position:** These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180° rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active

	display plane in the unrotated orientation.

SPDContAlpha—Sprite D Constant Alpha Register

Memory Offset Address: 724A8h

Default Value: 00000000h

Normal Access: Read/Write Double buffered

Bit	Description
31	**Enable Constant Alpha:** Sprite D Sprite constant alpha provides a way to apply an alpha value to all video sprite pixels. Each pixel color channel is multiplied by the constant alpha before proceeding to the blender. This can be used to create fade out effects. This is intended for CE device use where the video sprite might still be used to generate video output. 0 – Sprite D Constant Alpha is disabled 1 – Sprite D Constant Alpha is enabled
30:8	Reserved: MBZ
7:0	**Sprite D Constant Alpha Value:** This field provides the alpha value when constant alpha is enabled. A value of FF means fully opaque and a value of zero means fully transparent. Values in between those values allow for a blending of sprite with other surfaces.

SPDLIVESURF—Sprite D Live Surface Address Register

Memory Offset Address: 724ACh

Default Value: 00000000h

Normal Access: Read Only

Bit	**Descriptions**
31:12	**Sprite D Live Surface Base Address:** This gives the live value of the surface base address as being currently used for Sprite D
11:4	**Reserved: MBZ**
3	Flip_Source Project: All

	Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. Value / Name / Description / Project 0b / CS / Flip source is CS / All 1b / BCS / Flip source is BCS / All
2	**Reserved**
1:0	**Reserved: MBZ**

Sprite D Color Adjustment

These functions provide mechanisms for control of image colors generated from Sprite D sources. These functions are mainly intended for use for YUV color format sources. Adjustments are made before the YUV to RGB conversion. They take effect even when the Conversion Bypass bit is set. For display source input data in RGB format, software must set all the color correction registers to their default values (equivalent to a bypass mode). **These registers are not double buffered, take effect immediately after loading.**

SPDCLRC0—Sprite D Color Correction 0 Register

Address Offset:724D0h

Default Value: 01000000h

Normal Access: RW

Size: 32 bits

Bit	Description
31:27	Reserved:
26:18	**Contrast:** Contrast adjustment applies to YUV data. The Y channel is multiplied by the value contained in the register field. This signed fixed-point number is in 3i.6f format with the first 3 MSBs as the integer value and the last 6 LSBs as the fraction value. The allowed contrast value ranges from 0 to 7.53125 decimal. Bypassing Contrast, for YUV modes and for source data in RGB format, is accomplished by programming this field to a field value that represents 1.0 decimal or 001.000000 binary .
17:8	Reserved:

7:0	**Brightness:** This field provides the brightness adjustment with a 8-bit 2's compliment value ranging [-128, +127]. This value is added to the Y value after contrast multiply and before YUV to RGB conversion. A value of zero disables this adjustment affect. This 8-bit signed value provides half of the achievable brightness adjustment dynamic range. A full range brightness value would have a programmable range of [-255, +255]. Bypassing Brightness for YUV formats and for source data in RGB format, is accomplished by programming this field to 0.

SPDGAMC0— Sprite D Gamma Correction Registers

Address Offset:724F4h

Default Value: 00080808h

Normal Access: R/W

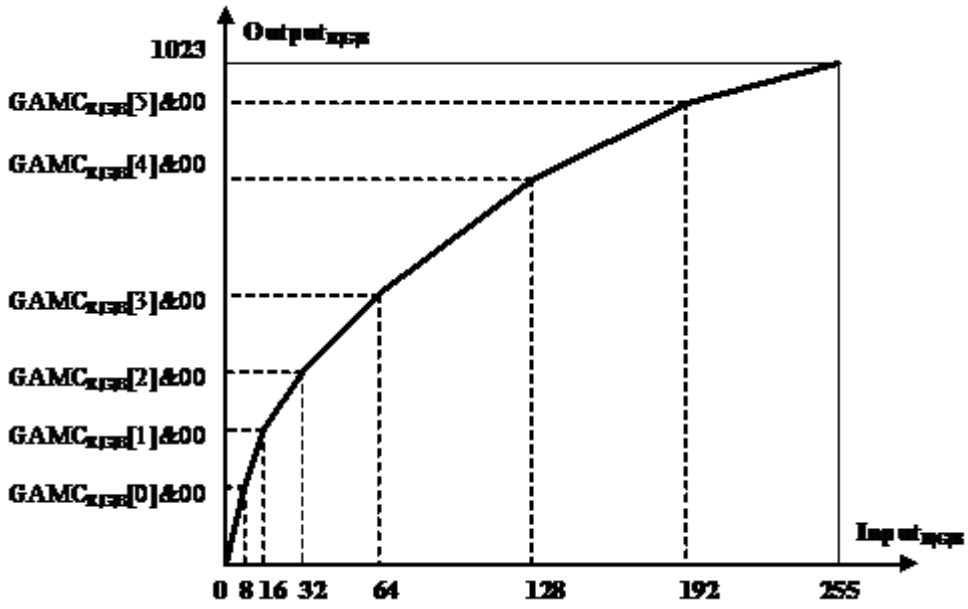
Size: 32 bits

These registers are used to determine the characteristics of the gamma correction for the Sprite D pixel data pre-blending. Additional gamma correction can be done in the display pipe gamma if desired. The pixels input to the gamma correction are 8 bit per channel pixels, and the output of the gamma correction is 10 bit per channel pixels. The gamma curve is represented by specifying a set of points along the curve. Each register has 32 bits, which are written to and read from together when accessed by the software. They are the six individual breakpoints on a logarithmically spaced color intensity space as shown in the following figure. The 8 bit values in the register are extended to 10 bit values in hardware by concatenating two zeroes onto the LSBs. The two end points (0 and 1023) have fixed values 0 and 1023, respectively. The appropriate Gamma breakpoint pairs (adjacent) are selected for each color component (Red, Green and Blue), and the output is interpolated between these two breakpoint values. The Gamma Correction registers (GAMC0 to GAMC5) are not double-buffered. They should be updated when the overlay is off. Otherwise, screen artifacts may show.

When the output from overlay is set in YUV format by programming CSC bypass, normally software should also bypass this gamma unit. However, since this gamma unit can also be viewed as a nonlinear transformation, it can be used, for whatever reason, in YUV output mode. In this case, the mapping of the three sets of piecewise linear map are as the following:

Bit	Description
31:24	Reserved:
23:16	Red (V/Cr):
15:8	Green (Y):
7:0	Blue (U/Cb):

Figure 11-4. Programming of the Piecewise-linear Estimation of Gamma Correction Curve



SPDGAMC1— Sprite D Gamma Correction Registers

Address Offset:724F0h

Default Value: 00101010h

Normal Access: R/W

Size: 32 bits

Same as previous register.

Bit	Description
31:24	Reserved:
23:16	Red (V/Cr):
15:8	Green (Y):
7:0	Blue (U/Cb):

SPDGAMC2— Sprite D Gamma Correction Registers

Address Offset:724ECh

Default Value: 00202020h

Normal Access: R/W

Size: 32 bits

Same as previous register.

Bit	Description
31:24	Reserved:
23:16	Red (V/Cr):
15:8	Green (Y):
7:0	Blue (U/Cb):

SPDGAMC3— Sprite D Gamma Correction Registers

Address Offset:724E8h

Default Value: 00404040h

Normal Access: R/W

Size: 32 bits

Same as previous register.

Bit	Description
31:24	Reserved:
23:16	Red (V/Cr):
15:8	Green (Y):
7:0	Blue (U/Cb):

SPDGAMC4— Sprite D Gamma Correction Registers

Address Offset:724E4h

Default Value: 00808080h

Normal Access: R/W

Size: 32 bits

Same as previous register.

Bit	Description
31:24	Reserved:
23:16	Red (V/Cr):

15:8	Green (Y):
7:0	Blue (U/Cb):

SPDGAMC5— Sprite D Gamma Correction Registers

Address Offset:724E0h

Default Value: 00C0C0C0h

Normal Access: R/W

Size: 32 bits

Same as previous register.

Bit	Description
31:24	Reserved:
23:16	Red (V/Cr):
15:8	Green (Y):
7:0	Blue (U/Cb):

GCI Registers

These registers are configuration for the Display arbiter and gci controller

FW_BLC_SELF

Address Packet:06500h

Default Value: 00000000h

Normal Attribute: R/W

Description: Display FIFO Watermark

Size: 32 bits

Bit	Description
31:16	Reserved
15	CSPWRDWNEN 1 = Dispaly FIFO can go into max_fifo configuration if only one plane A/B is enabled and all other planes, including overlay, are off. Another criteria that allow maxfifo mode entry is that CPU has to be in non C0 state. If CPU enters C0 state, maxfifo mode will exit in the next vblank. 0 = Dont put display FIFO in max_fifo configuration
14:0	Reserved

MI_ARB

Address Packet:06504h

Default Value: 00000000h

Normal Attribute: R/W

Description: Display Arbiter

Size: 32 bits

Bit	Description
31:3	Reserved
2	DISPLAY_TRICKLE_FEED_DISABLE 1 – Disable (Turn off trickle feed Display request). During maxfifo mode, display tricklefeed shall be disabled to improve power saving 0 – Enable (Default)

1:0	Reserved

CZCLK_CDCLK_FREQ_RATIO

Address Packet:06508h

Default Value: 00000077h

Normal Attribute: RO

Description: Display CZCLK/CDCLK FREQ Ratio for RMBUS sync

Size: 32 bits

Bit	Description
31:9	Reserved
8:4	Display CDCLK FREQUENCY ENCODING (Only highlighted frequencies are POR)

CDCLK Frequency encoding	CDCLK Divide Ratio	CD Register Encoding (Decimal)	SKU200 VCO 800 (MHz)	SKU266 VCO 1600 (MHz)	SKU333 VCO 2000 (MHz)	CD Qual Gen Ratio
5'b00001	1	1	800	1600	2000	1
5'b00010	1.5	2	533	1067	1333	2
5'b00011	2	3	400	800	1000	3
5'b00100	2.5	4	320	640	800	4
5'b00101	3	5	267	533	667	5
5'b00111	4	7	200	400	500	7
5'b01000	4.5	8	178	356	444	8
5'b01001	5	9	160	320	400	9
5'b01011	6	11	133	267	333	11
5'b01110	7.5	14	107	213	267	14
5'b01111	8	15	100	200	250	15

	5'b10001	9	17	89	178	222	17
	5'b10011	10	19	80	160	200	19
	5'b10111	12	23	67	133	167	23
	5'b11101	15	29	53	107	133	29
	5'b11111	16	31	50	100	125	31

3:0 CORE CLOCK (CZCLK) FREQUENCY ENCODING

CZCLK Frequency encoding	CZCLK Divide Ratio	CZ Register Encoding (Decimal)	SKU200 VCO 800 (MHz)	SKU266 VCO 1600 (MHz)	SKU333 VCO 2000 (MHz)	CZ Qual Gen Ratio
4'b0001	1	1	800	1600	2000	1
4'b0010	1.5	2	533	1067	1333	2
4'b0011	2	3	400	800	1000	3
4'b0100	2.5	4	320	640	800	4
4'b0101	3	5	267	533	667	5
4'b0111	4	7	200	400	500	7
4'b1000	4.5	8	178	356	444	8
4'b1001	5	9	160	320	400	9

	4'b1011	6	11	133	267	333	11
	4'b1110	7.5	14	107	213	267	14
	4'b1111	8	15	100	200	250	15

GCI_Control

Address Packet:0650Ch

Default Value: 00004000h

Normal Attribute: R/W

Description: GCI Control Register.

Size: 32 bits

Bit	Description
31:28	PFI Credit info to be sent to Pondicherry PFI: Others = reserved 0111 = 15 credits 0110 = 14 credits 0101 = 13 credits 0100 = 12 credits 0011 = 11 credits 0010 = 10 credits 0001 = 9 credits 0000 = 8 credits available to PND (default) Based on the czclk/cdclk ratio, display driver has to determine the appropriate PFI credits to be used
27	Force PFI Credit Resend to SSA 0 = Disable PFI credit to resend to SSA. Hardware is responsible to clear this bit after the PFI credit initialization request is sent. 1 = Enable PFI credit to resend to SSA. When driver sets this bit, Display PFI request engine will resend the new PFI credit bit [31:28] to SSA. Hardware is responsible to clear this bit after the PFI credit initialization request is sent.
26:25	Reserved

24	Reserved
23:15	Reserved
14	VGA_FAST_MODE_DISABLE 0 = Fast Mode enabled. The Gfx mem arbiter can accept a vga display read request every clock. Note that the HP Address (G_HP_CONTROL[28:24]) and ID (G_HP_CONTROL[21:16]) FIFO depths must be set to a value greater than 1 when Fast Mode is enabled. 1 = Fast Mode disabled. (default) The Gfx mem arbiter can accept a vga display read request every other clock Programming note: VGA FAST MODE is not supported in vlv.
13:4	Request Latency Override If bit 3 of this register is set, the 10-btt Request Latency Override value programmed here is used as the latency offset from the global timer for requests that win arbitration. If bit 3 is not set, normal request latency from streamers is used. Programming note: This value should not be larger than the actual required request latency. Otherwise, it will cause underrun. The guidline is to use latency corresponds to low watermark level or even smaller. When this field is used, the actual request latency is defeatured, either zero or a small value is used but still not causing underrun.
3	Request Latency Override Enable: 1 = Request Latency Override values in bit[13:4] is used as the latency offset from global timer 0 = Request Latency Override values is disabled. Normal request latency from streamer is used. (default)
2	Reserved
1	Reserved
0	HP_ARBITRATION_MODE : 0 = Select hierarchical arbiter 1 = Select backup round robin arbiter

GMBUSFREQ — GMBUS frequency binary encoding

Address Offset:06510h

Default Value: 000000A0h

Normal Attribute: R/W

Description: GMBUS Frequency Binary Encoding Register.

Size: 32 bits

Bit	Description
31:10	Reserved
9:0	CMBUS CDCLK frequency (cdfreq): Programmng note: bit[9:2] should be programmed to the number of cdclk that generates 4MHz reference clock freq which is used to generate GMBus clock. This will vary with the cdclk freq. Programming note: For hot plug detect on exact 100ms as long pulse, driver shall program [9:0] = cdclk/1.01

MIPI Registers

MIPIA_DEVICE_READY_REG – MIPI A Device Ready Register

Address Offset:00B000h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:4	Reserved
3	BUS Possession
2:1	ULPS State 2'b10 = ULPS entry 2'b01 = ULPS exit 2'b00 = Normal operation S/W needs to ensure that there is a minimum of 1ms time available before clearing the UPLS exit State.
0	**Device Ready** Set by the processor to inform that device is ready

MIPIA_INTR_STAT_REG

Address Offset:00B004h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31	Tearing Effect Set to indicate that tearing effect trigger message is Received
30	SPL PKT Sent Interrupt Set to confirm the transmission of the DPI event specific commands set in the dpi control and dpi data register

29	Gen Read Data Avail Set to indicate that the requested data for a Generic Read request is available in the buffer i.e., generic read response data is available in the read FIFO
28	LP Generic WR FIFO Full Set to indicate that the LP generic write fifo is full
27	HS Generic WR Fifo Full Set to indicate that the HS generic write fifo is full
26	RX Prot Violation Set if DSI protocol violation error is reported in the acknowledge packet by the display device
25	RX Invalid TX Length Set if invalid transmission length error is reported in the acknowledge packet by the display device
24	ACK With No Error Set if acknowledge trigger message is received with out any error
23	Turn Around Ack Timeout Set if a turn around acknowledgement sequence is not received from the display device
22	LP RX Timeout Set if a low power reception count expires this interrupt is generated
21	HS TX Timeout Set if a high speed transmission prevails for more than the expected count value this interrupt is raised
20	DPI FIFO Underrun Set to '1' if there is no data in the dpi fifo to make a in time delivery of the pixel data to the DSI receiver
19	Low Contention Set to '1' if a LP low fault is registered by at the D-PHY contention detector
18	High Contention Set to '1' if a LP high fault is registered by at the D-PHY contention detector
17	TXDSI VC ID Invalid Set to '1' if the received virtual channel ID is invalid

16	TXDSI Data Type Not Recognised Set to '1' if the received data type is not recognised
15	Reserved
14	TXECC Multibit Error Set to '1' if there is no ECC correction for the packet or there are more than 2 bit errors in the packet received by Arasan_DSI_host
13	TXECC Single Bit Error Set to '1' if ECC syndrome was computed and is corrected for one bit error during the reception of packets by the Arasan_DSI_host
12	TXFalse Control Error Set to '1' if a control error is observed on the lanes by the Arasan_DSI_host
11	RXDSI VC ID Invalid Set to '1' if the virtual channel ID is invalid by the display device is reported in the Acknowledge packet by the display device
10	RXDSI Data Type Not Recognised Set to '1' if the data type is not recognised by the display device is reported in the Acknowledge packet by the display device
9	Reserved
8	RXECC Multibit Error Set to '1' if there is no ECC correction for the packet or there are more than 2 bit errors in the packet is reported in the Acknowledge packet by the display device
7	RXECC Single Bit Error Set to '1' if ECC syndrome was computed and corrected for one bit error is reported in the Acknowledge packet by the display device
6	RXFalse Control Error Set to '1' if a control error is reported in the Acknowledge packet by the display device
5	RXHS Receive Timeout Error Set to '1' if the high speed receive timer value expires and data transfer lasts on the data lane is reported in the Acknowledge packet by the display device
4	RX LP TX Sync Error

	Set to '1' if Low power transmission sync error occurs in the display device and is reported in the Acknowledge packet by the display device
3	RXEscape Mode Entry Error Set to '1' if Escape Mode Entry command is not understandable by the display device and is reported in the Acknowledge packet by the display device
2	RXEOTSyncError
1	RXSOTSyncError Set to '1' if a start of transmission synchronisation error is reported in the Acknowledge packet by the display device
0	RXSOTError Set to '1' if a start of transmission error is reported in the Acknowledge packet by the display device

MIPIA_INTR_EN_REG

Address Offset:00B008h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31	Tearing effect Set to enable tearing effect interrupt
30	SPL Pkt Sent Interrupt Set to enable the confirmation of transmission of the DPI event specific commands set in the dpi control and dpi data register
29	Gen Read Data Avail Set to enable Generic Read available interrupt
28	LP Generic WR FIFO Full Set to indicate that the LP generic write fifo is full
27	HS Generic WR FIFO Full Set to indicate that the HS generic write fifo is full

26	RX Prot Violation Set to enable protocol violation error
25	RX Invalid TX Length Set to enable invalid transmission length error
24	ACK With No Error Set to enable acknowledge trigger message reception with out any error
23	Turn Around ACK Timeout Set to enable turn around acknowledgement ,sequence timeout
22	LP RX Timeout Set to enable low power reception count timeouts
21	HS TX Timeout Set to enable a high speed transmission timeout
20	DPI FIFO Underrun Set to enable if there is no data in the dpi fifo to make a in time delivery of the pixel data to the DSI receiver
19	Low Contention Set to enable a LP low fault interrupt
18	High Contention Set to enable a LP high fault interrupt
17	TXDSI VC ID Invalid Set to enable the interrupt if the received packets virtual channel ID is invalid
16	TXDSI Data Type Not Recognised Set to enable the interrupt if the received packets data type is not recognised
15	Reserved
14	TXECC Multibit Error Set to enable the interrupt if there is no ECC correction for the packet or there are more than 2 bit errors in the packet received by Arasan DSI host
13	TXECC Single bit Error

	Set to enable the interrupt if ECC syndrome was computed and is corrected for one bit error during the reception of packets by the Arasan DSIhost
12	TXFalse Control Error Set to enable the interrupt for the control error.,observed on the lanes by the Arasan_DSI_host
11	RXDSI VC ID Invalid Set to enable the interrupt for invalid virtual channel ID in the acknowledgment packet reports
10	RXDSI Data Type Not Recognised Set to enable the interrupt for the un recognised data type in the acknowledgment packet reports
9	Reserved
8	RXECC Multibit Error Set to enable the interrupt for no ECC correction for the packet or there are more than 2 bit errors reported in the acknowledgment packet
7	RXECC Single bit Error Set to enable the interrupt for ECC syndrome computation and one bit error correction for the acknowledgment packet
6	RXFalse Control Error Set to enable the interrupt for control error in the acknowledgment packet reports
5	RXHS Receive Timeout Error Set to enable the interrupt for the high speed receive timeout Error in the acknowledgment packet reports
4	RX LP TX Sync Error Set to enable the interrupt for Low power transmission sync error in the acknowledgment packet reports
3	RXEscape Mode Entry Error Set to enable the interrupt for Escape Mode Entry command error in the acknowledgment packet reports
2	RXEOTSync Error Set to enable the interrupt for End of transmission synchronisation Error in the acknowledgement packet reports
1	RXSOTSync Error

	Set to enable the interrupt for start of transmission synchronisation error in the acknowledgement packet reports
0	RXSOT Error Set to enable the interrupt for start of transmission error in the acknowledgment packet reports

MIPIA_DSI_FUNC_PRG__REG

Address Offset:00B00Ch

Default Value: 00000001h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:16	Reserved
15:13	Supported Data Width in Command Mode 000 --> Reserved, 001 --> 16 bit data , 010 --> 9 bit data , 011 --> 8 bit data , 100 --> option 1 : 101 --> option 2 : 110 to 111 --> Reserved
12:11	Reserved
10:7	Supported Format In Video Mode Supported colour format, 0001 --> RGB565, 0010 --> RGB666, 0011 --> RGB 666 loosely packed format, 0100 --> RGB888
6:5	Channel Number For Command Mode Virtual channel number for command mode is programmed by the processor

4:3	Channel Number for Video Mode Virtual channel number for command mode is programmed by the processor
2:0	Data Lanes PRG REG Number of data lanes to be supported is programmed by the processor Programming note: For VLV C0, when driver programs this field, it shall program the number of data lanes and txrequesths_0 enable sel in IOSF MIPI RCOMP register Port ID=1B and offset = 0x3 bit[31:28]

MIPIA_HS_TX_TIMEOUT_REG

Address Offset:00B010h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:24	Reserved
23:0	High Speed TX Timeout Counter The maximum duration allowed for the DSI host ,to remain in high speed mode for a transmission. If the counter expires, HS mode is terminated with EOT and the lanes enter stop state

MIPIA_LP_RX_TIMEOUT_REG

Address Offset:00B014h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:24	Reserved
23:0	Low Power Reception Timeout Counter Timeout value to be checked for received short packets .If the timer expires the DSI Host enters stop state

MIPIA_TURN_AROUND_TIMEOUT_REG

Address Offset:00B018h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:6	Reserved
5:0	Turn Around Timeout Register Timeout value to be checked after the DSI host makes a turn around in the direction of transfers. If the timer expires the DSI Host enters stop state

MIPIA_DEVICE_RESET_TIMER

Address Offset:00B01Ch

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:16	Reserved
15:0	Device Reset Timer Timeout value to be checked for device to be reset after issuing reset entry command. If the timer expires the DSI Host enters normal operation

MIPIA_DPI_RESOLUTION_REG

Address Offset:00B020h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:16	Vertical Address Shows the vertical address count in lines

15:0	Horizontal Address Shows the horizontal address count in pixels

MIPIA_DBI_RESOLUTION_REG

Address Offset:00B024h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:2	Reserved
1:0	DBI FIFO Thrtl DBI FIFO's watermark can be set using the following bits so as to enable dbi_stall de-assertion whenever the below FIFO condition is reached: 00 - (1/2) DBI fifo empty 01 - (1/4) DBI fifo empty 10 - 7 locations are empty 11 - Reserved

MIPIA_HORIZ_SYNC_PADDING_COUNT

Address Offset:00B028h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:16	Reserved
15:0	Horizontal Sync Padding Count Shows the horizontal sync padding value in terms of txbyteclkhs

MIPIA_HORIZ_BACK_PORCH_COUNT

Address Offset:00B02Ch

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:16	Reserved
15:0	Horizontal Back Porch Count Shows the horizontal back porch value in terms of txbyteclkhs

MIPIA_HORIZ_FRONT_PORCH_COUNT

Address Offset:00B030h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:16	Reserved
15:0	Horizontal Front Porch Count Shows the horizontal front porch value in terms of txbyteclkhs

MIPIA_HORIZ_ACTIVE_AREA_COUNT

Address Offset:00B034h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:16	Reserved
15:0	Horizontal Active Area Count Shows the horizontal active area value in terms of txbyteclkhs

MIPIA_VERT_SYNC_PADDING_COUNT

Address Offset:00B038h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:16	Reserved
15:0	Vertical Sync Padding Count Shows the vertical sync padding value in terms of lines

MIPIA_VERT_BACK_PORCH_COUNT

Address Offset:00B03Ch

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:16	Reserved
15:0	Vertical Back Porch Count Shows the vertical back porch value in terms of lines

MIPIA_VERT_FRONT_PORCH_COUNT

Address Offset:00B040h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:16	Reserved
15:0	Vertical Front Porch Count Shows the vertical front porch value in terms of lines

MIPIA_HIGH_LOW_SWITCH_COUNT

Address Offset:00B044h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:16	Reserved High speed to low power or Low power to high speed switching time in terms of txbyteclkhs
15:0	High Speed to Low Power or Low Power to High Speed Switch Count High speed to low power or Low power to high speed switching time in terms of txbyteclkhs

MIPIA_DPI_CTRL_REG

Address Offset:00B048h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:8	Reserved
7	RSTTRG
6	HS LP Set to '0' to indicate the special packets are sent through the DSI link using HS transmission and set to '1' to indicate that the special packets are sent through the DSI link using low power mode
5	Back Light Off Set to '1' to indicate a backlight OFF short packet has to be packetised for the DPI's virtual channel
4	Back Light on Set to '1' to indicate a backlight ON short packet has to be packetised for the DPI's virtual channel
3	Color Mode Off Set to '1' to indicate a color mode OFF short packet has to be packetised for the DPI's virtual channel
2	Color Mode On Set to '1' to indicate a color mode ON short packet has to be packetised for the DPI's virtual channel
1	Turn On Set to '1' to indicate a turn on short packet has to be packetised for the DPI's virtual channel

0	Shut Down Set to '1' to indicate a shut down short packet has to be packetised for the DPI's virtual channel

MIPIA_DPI_DATA_REGISTER

Address Offset:00B04Ch

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:6	Reserved
5:0	Command Byte Command Byte to represent the new or not defined command bytes usage for special features representation. [Like backlight ON and OFF]. This register should be programmed before the DPI control register is being programmed for backlight ON/OFF

MIPIA_INIT_COUNT_REGISTER

Address Offset:00B050h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:16	Reserved
15:0	Master Init Timer Counter value in terms of low power clock to initialise the DSI Host IP [TINT] that drives a stop state on the mipi's D-PHY bus

MIPIA_MAX_RETURN_PKT_SIZE_REGISTER

Address Offset:00B054h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:10	Reserved
9:0	Max Return Pkt Size Set the count value in bytes to collect the return data packet for reverse direction data flow in data lane0 in response to a DBI read operation

MIPIA_VIDEO_MODE_FORMAT_REGISTER

Address Offset:00B058h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:5	Reserved
4	Ramdom DPI Display Resolution Defeature Set by the processor to support random DPI display resolution 0 – random DPI display resolution support disabled 1 – random DPI display resolution support enabled
3	Disable video BTA Set by the processor to inform the DSI controller to disable the BTA sent at the last blanking line of VFP. By default, this bit is set to 0. 0 – BTA sending at the last blanking line of VFP is enabled. 1 – BTA sending at the last blanking line of VFP is disabled
2	IP TG Config Set by the processor to inform that the DSI controller should discontinue the DPI transfer after the last line of the VFP after ip_tg_enable deassertion. By default, this bit is set to 0. 0 - After ip_tg_enable deassertion, DSI Tx controller stops the DPI transfer immediately after the

	current packet is transmitted. 1 - After ip_tg_enable deassertion, DSI Tx controller discontinues the DPI transfer after the last line of the VFP
1:0	Video Mode FMT Sets the Video mode format (packet sequence) to be supported in DSI. In Non Burst Mode, in addition to programming this register the horizontal active area count register value should also be programmed equal to RGB word count value In Burst Mode, in addition to programming this register the horizontal active area count register value should also be programmed greater than the RGB word count value, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link. 00 – Reserved 01 - Non Burst Mode with Sync Pulse 10 - Non Burst Mode with Sync events 11 - Burst Mode

MIPIA_EOT_DISABLE_REGISTER

Address Offset:00B05Ch

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:8	Reserved
7	LP RX Timeout Error Recovery Disable Set by the processor to enable or disable the LP_Rx_timeout error recovery if the processor clears LP_Rx_timeout error interrupt. 0 - LP_Rx_timeout error recovery action will be taken by the DSI Tx controller if the processor clears the LP_Rx_timeout error interrupt. 1 - If the processor clears the LP_Rx_timeout error interrupt, LP_Rx_timeout error recovery action will not happen in DSI Tx contorller. LP Rx timeout error interrupt will act as an informative interrupt
6	HS TX Timeout Error Recovery Disable Set by the processor to enable or disable the HS_Tx_timeout error recovery if the processor clears HS_Tx_timeout interrupt. 0 - HS_Tx_timeout error recovery action will be taken by the DSI Tx controller if the processor

	clears the HS_Tx_timeout error interrupt. 1 - If the processor clears the HS_Tx_timeout error interrupt, HS_Tx_timeout error recovery action will not happen in DSI Tx contorller. HS Tx timeout error interrupt will act as an informative interrupt
5	Low Contention Recovery Disable Set by the processor to enable or disable the contention recovery procedure if the processor clears Low contention interrupt. 0 - Contention recovery will happen if the processor clears Low contention interrupt. 1 - If the processor clears the low contention interrupt, contention recovery procedure will not be initiated by the DSI Tx contorller. Low contention interrupt will act as an informative interrupt
4	High Contention Recovery Disable Set by the processor to enable or disable the contention recovery procedure if the processor clears High contention interrupt. 0 - Contention recovery will happen if the processor clears High contention interrupt. 1 - If the processor clears the high contention interrupt, contention recovery procedure will not be initiated by the DSI Tx contorller. Ignore the High Contention Interrupt in MIPI_INTR_STAT_REG
3	TXDSI Type Not Recognised Error Recovery Disable Set by the processor to enable or disable the error recovery action to be taken by the DSI Tx controller if TxDSI data type not recognised error interrupt is cleared by the processor. 0 - Error recovery action will be taken if TxDSI data type not recognised error interrupt is cleared by the processor. 1 - If TxDSI data type not recognised error interrupt is cleared by the processor, error recovery action will not be taken by the DSI TX controller. Tx DSI data type not recognized error interrupt will act as an informative interrupt
2	TXECC Multibit Err Recovery Disable Set by the processor to enable or disable the error recovery action to be taken by the DSI Tx controller if Tx ECC multibit error interrupt is cleared by the processor. 0 - Error recovery action will be taken if Tx ECC multibit error interrupt is cleared by the processor. 1 - If Tx ECC multibit error interrupt is cleared by the processor, error recovery action will not be taken by the DSI TX controller. Tx multibit error interrupt will act as an informative interrupt
1	ClockStop Set by the processor to enable or disable clock stopping feature during BLLP timing in a DPI transfer in dual channel mode or during DPI only mode and also when there is no traffic in the

	DBI interface in DBI only enabled mode. By default this register value is 0. 0 - clock stopping disabled 1 - clock stopping enabled
0	EOT Dis Set by the processor to enable or disable EOT short packet transmission. By default this register value is 0. For backward comapatibility of earlier DSI systems, EOT short packet transmission can be disabled. 0 - EOT short packet transmission enabled 1 - EOT short packet transmission disabled

MIPIA_LP_BYTECLK_REGISTER

Address Offset:00B060h

Default Value: 00000000h

Normal Attribute: RW

vlv

Size: 32 bits

Bit	Description
31:16	Reserved
15:0	LP Byteclk Low power clock equivalence in terms of byte clock. The value programmed in this register is equal to the number of byte clocks occupied in one low power clock. This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc)

MIPIA_LP_GEN_DATA_REGISTER

Address Offset:00B064h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:0	LP Gen Data Data port register used for generic data transfers in low power mode

MIPIA_HS_GEN_DATA_REGISTER

Address Offset:00B068h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:0	HS Gen Data Data port register used for generic data transfers in low power mode

MIPIA_LP_GEN_CTRL_REGISTER

Address Offset:00B06Ch

Default Value: 00000000h

Normal Attribute:WO

Size: 32 bits

Bit	Description
31:24	Reserved
23:8	Word Count Specifies the word count for generic long packet Specifies the accompanied parameters for generic short packets. Note: Invalid parameters must be set to 00h
7:6	Virtual Channel Used to specify the virtual channel for which the generic data transmission is intended
5:0	Data type Used to specify the generic data types 03h - Generic short write, no parameters 13h - Generic short write, 1 parameter 23h - Generic short write, 2 parameters 04h - Generic read, no parameters 14h - Generic read, 1 parameter 24h - Generic read 2 parameter

	29h - Generic long write 05h – Manufacturer DCS short write, no parameter 15h – Manufacturer DCS short write, one parameter 06h – Manufacturer DCS read, no parameter 39h – Manufacturer DCS long write

MIPIA_HS_GEN_CTRL_REGISTER

Address Offset:00B070h

Default Value: 00000000h

Normal Attribute:WO

Size: 32 bits

Bit	Description
31:24	Reserved
23:8	Word Count Specifies the word count for generic long packet Specifies the accompanied parameters for generic short packets. Note: Invalid parameters must be set to 00h
7:6	Virtual Channel Used to specify the virtual channel for which the generic data transmission is intended
5:0	Data type Used to specify the generic data types 03h - Generic short write, no parameters 13h - Generic short write, 1 parameter 23h - Generic short write, 2 parameters 04h - Generic read, no parameters 14h - Generic read, 1 parameter 24h - Generic read 2 parameter 29h - Generic long write 05h – Manufacturer DCS short write, no parameter 15h – Manufacturer DCS short write, one parameter 06h – Manufacturer DCS read, no parameter

	39h – Manufacturer DCS long write

MIPIA_GEN_FIFO_STAT_REGISTER

Address Offset:00B074h

Default Value: 1E060606h

Normal Attribute: RO

Size: 32 bits

Bit	Description
31:29	Reserved
28	DPI FIFO Empty Default 1
27	DBI FIFO Empty Default 1
26	LP Ctrl FIFO Empty Default 1
25	LP Ctrl FIFO Half Empty Default 1
24	LP Ctrl FIFO Full Default 0
23:19	Reserved
18	HS Ctrl FIFO Empty Default 1
17	HS Ctrl FIFO Half Empty Default 1
16	HS Ctrl FIFO Full Default 0
15:11	Reserved
10	LP Data FIFO Empty Default 1
9	LP Data FIFO Half Empty Default 1
8	LP Data FIFO Full Default 0
7:3	Reserved
2	HS Data FIFO Empty Default 1
1	HS Data FIFO Half Empty

	Default 1
0	HS Data FIFO Full Default 0

MIPIA_HS_LS_DBI_ENABLE_REG

Address Offset:00B078h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Description:Note : dbi_hs_lp_switch_reg has to be written only if DBI FIFO is empty

Bit	Description
31:1	Reserved
0	DBI HS LS Switch Re Set to 1 if DBI packets have to be transmitted in Low power mode Set to 0 if DBI packets have to be transmitted in High speed mode

MIPIA_RESERVED

Address Offset:00B07Ch

Default Value: 00000000h

Normal Attribute: RO

Size: 32 bits

Bit	Description
31:0	Reserved

MIPIA_DPHY_PARAM_REG

Address Offset:00B080h

Default Value: 0B061A04h

Normal Attribute: RW

Size: 32 bits

Bit	Description

31:30	Reserved
29:24	Exit Zero Count THS_0_TIM_UI_CNT and THS_EXIT_TIM_UI_CNT for dphy are programmed as exit zero count by the processor
23:21	Reserved
20:16	Trail Count TCLK_POST_TIM_UI_CNT and TCLK_TRAIL_TIM_UI_CNT for dphy are programmed as trail count by the processor
15:8	CLK Zero Count TCLK_0_TIM_UI_CNT for dphy is programmed as clk zero count by the processor
7:6	Reserved
5:0	Prepare Count TCLK_PREP_TIM_UI_CNT and THS_PREP_TIM_UI_CNT for dphy are programmed as prepare count by the processor

MIPIA_DBI_BW_CTRL_REG

Address Offset:00B084h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:0	Bandwidth Timer DBI Bandwidth control Register. The bandwidth essential for transmitting 16 long packets containing 252 bytes meant for DCS write memory command is programmed in this register in terms of byte clocks. Based on the DSI transfer rate and the number of lanes configured the time taken to transmit 16 long packets in a DSI stream varies. Note: The value programmed in this timer must be greater than the actual time taken to carryout 16 long packets transmission in DSI stream plus the time taken to transmit two blanking packets

MIPIA_CLK_LANE_SWITCHING_TIME_CNT

Address Offset:00B088h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:16	LS HS SSW Cnt Low power to high speed switching time in terms byte clock (txbyteclkhs). This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc). Typical value - Number of byte clocks required to switch from low power mode to high speed mode after txrequesths_clk is asserted. Current Value is ah = 10 txbyteclkhs
15:0	HS LS Pwr SW Cnt High speed to low power switching time in terms byte clock (txbyteclkhs). This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc). Typical value - Number of byte clocks request to switch from high speed mode to low power mode after txrequesths_clk is de-asserted. Current Value is 14h = 20 txbyteclkhs

MIPIA_STOP_STATE_STALL

Address Offset:00B08Ch

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:8	Reserved
7:0	STOP STATE STALL COUNTER Delay between (stall the stop state signal) the data transfer is increased based on this counter value. This counter is calculated from txclkesc. Note: If processor programs this register then it needs to reprogram the high_low_ switch counter in B044h and lp_equivalent_byteclk reg in B060h to compensate this delay. High_low_switch_count B044h: High to low switch counter = Actual High to low switch + stop_sta_stall_reg value * Low power clock equivalence value in terms of byte clock LP equivalent byteclk register B060h:

	LP equivalent byteclk value = txclkesc time/ txbyteclk time * (105 + stop_sta_stall_reg value) / 105 Minimum time of Low Power short packet transfer = 105 txclkesc

MIPIA_INTR_STAT_REG_1

Address Offset:00B090h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:1	Reserved
0	RX Contention Detected Set to 1'b1 if the contention detected in the display device and is reported in the Acknowledge packet by the display device

MIPIA_INTR_EN_REG_1

Address Offset:00B094h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:1	Reserved
0	Enable RX Contention Detected Set to enable the interrupt for contention detected error in the acknowledgement packet reports

MIPIA_DBI_TYPEC_CTRL

Address Offset:00B100h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31	VAL 0= disable DBI TYPE-C interface (default) 1= enable DBI TYPE-C interface Driver to make sure that the command and data buffers are cleared before this bit is changed
30	Status command and data buffer empty & link completed sending out all serialized data and IDLE 0 = IDLE 1 = work in progress
29:28	Option TYPE-C option selection 00 option 1 01 option 2 10 option 3 11 no defined functionality
27:24	Freq Type-C clock frequency ; A counter based onczclk is used to generate the TYPE-C Clock. So based on the czclk, a frequency close to the specified below will be generated. Not the exact frequency. 0000 1Mhz (default) 0001 1Mhz 0010 2Mhz 1111 15Mhz
23:9	Reserved
8	Override Use override counter value to derive the TYPE-C clock frequency
7:0	Override Counter Override counter value to generate the TYPE-C clock

MIPIA_CTRL

Address Offset:00B104h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

MIPI adapter has a control register with options to control width of the dbi bus and the divide value of the clock that needs to be supplied to the Clocks module so that a 2x divided clock can be provided to

the MIPI D-PHY IP.Self refresh capability is in DCS commands. The other 3 controls bits (SD, CM and back light control) are now moved to MIPI IP registers

Bit	Description
31:7	Reserved
6:5	Escape Clock Divider Escape clock divider select for Pipe A and Pipe C Escape clock is shared by both Pipe A and Pipe C so it cant be set different. 00= 1 X (20 Mhz) (default) 01= ½ X (10Mhz) 10= ¼ X (5Mhz) Changing this register can only be done when the MIPI device_ready is turned OFF
4:3	Status 2'b00: low priority on read requests to G-unit 2'b11 : high priority
2	RGB Flip 1'b0 : RGB data from disp2d is reverted to BGR 1'b1 : RGB data from disp2d is passed as is to MIPI IP
1:0	Reserved

MIPIA_DATA_ADD

Address Offset:00B108h

Default Value: 00000000h

Normal Attribute: RW

vlv

Size: 32 bits

Bit	Description
31:5	Data Mem Addr When there is updated data for the display panel, S/W programs this register with the memory address to read from

4:1	Reserved
0	Data Valid This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

MIPIA_DATA_LEN

Address Offset:00B10Ch

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:20	Reserved
19:0	Data Length This field shows the remaining length of data that needs to be read from memory, Initially set by S/W and is decremented by H/W as reads are issued

MIPIA_CMD_ADD

Address Offset:00B110h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:5	Command Mem Addr When there are new commands that need to be sent to the display panel, S/W programs this register with the memory address to read the commands from
4:3	Reserved MBZ
2	MIPIA Auto PWG Enable Idle state: SW driver writes to this bit to enable auto power gating for MIPIA controller 0: default

	1: auto power gate is enabled
1	Command Data Mode 0: data for memory write command from system buffer that is specified by MIPI data address register 1: data for memory write command from pipe A rendering
0	Command Valid This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

MIPIA_CMD_LEN

Address Offset:00B114h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:24	Command 3 This is command 3 length (command + parameters) in bytes
23:16	Command 2 This is command 2 length (command + parameters) in bytes
15:8	Command 1 This is command 1 length (command + parameters) in bytes
7:0	Command 0 This is command 0 length (command + parameters) in bytes

MIPIA_RD_DATA_RETURN0

Address Offset:00B118h

Default Value: 00000000h

Normal Attribute: RO

Size: 32 bits

In addition to the command and data registers, adapter provides 8 read only registers for S/W to read the return data from the panel. At this time the usage case for the read path from the panel is for configuration reads only. Hence, more than 4 bytes of read are not allowed. Maximum read return size in the MIPI IP should be no greater than 32 bytes

Bit	Description
31:0	RD Data Return Panel This is the configuration data returned from the panel

MIPIA_RD_DATA_RETURN1

Address Offset:00B11Ch

Default Value: 00000000h

Normal Attribute: RO

Size: 32 bits

In addition to the command and data registers, adapter provides 8 read only registers for S/W to read the return data from the panel. At this time the usage case for the read path from the panel is for configuration reads only. Hence, more than 4 bytes of read are not allowed. Maximum read return size in the MIPI IP should be no greater than 32 bytes

Bit	Description
31:0	RD Data Return Panel This is the configuration data returned from the panel

MIPIA_RD_DATA_RETURN2

Address Offset:00B120h

Default Value: 00000000h

Normal Attribute: RO

Size: 32 bits

In addition to the command and data registers, adapter provides 8 read only registers for S/W to read the return data from the panel. At this time the usage case for the read path from the panel is for configuration reads only. Hence, more than 4 bytes of read are not allowed. Maximum read return size in the MIPI IP should be no greater than 32 bytes

Bit	Description
31:0	RD Data Return Panel

	This is the configuration data returned from the panel

MIPIA_RD_DATA_RETURN3

Address Offset:00B124h

Default Value: 00000000h

Normal Attribute: RO

Size: 32 bits

In addition to the command and data registers, adapter provides 8 read only registers for S/W to read the return data from the panel. At this time the usage case for the read path from the panel is for configuration reads only. Hence, more than 4 bytes of read are not allowed. Maximum read return size in the MIPI IP should be no greater than 32 bytes

Bit	Description
31:0	RD Data Return Panel This is the configuration data returned from the panel

MIPIA_RD_DATA_RETURN4

Address Offset:00B128h

Default Value: 00000000h

Normal Attribute: RO

Size: 32 bits

In addition to the command and data registers, adapter provides 8 read only registers for S/W to read the return data from the panel. At this time the usage case for the read path from the panel is for configuration reads only. Hence, more than 4 bytes of read are not allowed. Maximum read return size in the MIPI IP should be no greater than 32 bytes

Bit	Description
31:0	RD Data Return Panel This is the configuration data returned from the panel

MIPIA_RD_DATA_RETURN5

Address Offset:00B12Ch

Default Value: 00000000h

Normal Attribute: RO

Size: 32 bits

In addition to the command and data registers, adapter provides 8 read only registers for S/W to read the return data from the panel. At this time the usage case for the read path from the panel is for configuration reads only. Hence, more than 4 bytes of read are not allowed. Maximum read return size in the MIPI IP should be no greater than 32 bytes

Bit	Description
31:0	RD Data Return Panel This is the configuration data returned from the panel

MIPIA_RD_DATA_RETURN6

Address Offset:00B130h

Default Value: 00000000h

Normal Attribute: RO

Size: 32 bits

In addition to the command and data registers, adapter provides 8 read only registers for S/W to read the return data from the panel. At this time the usage case for the read path from the panel is for configuration reads only. Hence, more than 4 bytes of read are not allowed. Maximum read return size in the MIPI IP should be no greater than 32 bytes

Bit	Description
31:0	RD Data Return Panel This is the configuration data returned from the panel

MIPIA_RD_DATA_RETURN7

Address Offset:00B134h

Default Value: 00000000h

Normal Attribute: RO

Size: 32 bits

In addition to the command and data registers, adapter provides 8 read only registers for S/W to read the return data from the panel. At this time the usage case for the read path from the panel is for configuration reads only. Hence, more than 4 bytes of read are not allowed. Maximum read return size in the MIPI IP should be no greater than 32 bytes

Bit	Description

31:0	RD Data Return Panel This is the configuration data returned from the panel

MIPIA_RD_DATA_VALID

Address Offset:00B138h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:8	Reserved
7:0	Read Data Valid Each bit corresponds to presence of valid data in the registers above. When data is returned from the panel, H/W will write into these registers in sequence, and set the corresponding valid bit. When S/W issues a write '1 to the registers, this bit is cleared

MIPIA_PORT_CTRL

Address Offset:061190h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31	EN When this bit is disabled the MIPI DPI (video mode) is inactive and in it's low power state. When it is enable it starts to generate timing for this MIPI port 0 = The port is disabled and all MIPI DPI interface are disable (timing generator is off) 1 = The port is enabled
30:27	MIPI4DPHY AdjDly HSTX MIPI A These four bits act as an encoded count of the number of buffer delays to insert on the ckdsi2x clock going to the six flops that are storing the HS TX data and clock signals. Default is 4'b0000 which is the equivalent of 1 buffer delay. Will need to set these bits to a

	value determined by clock timing team before using the MIPI DSI HS TX feature
26	MIPI Dual-link mode (applicable only if MIPI dual-link mode is enabled through MIPI Lanes configuration bits) 0 = Front-Back mode (default. Supported only in video mode) 1 = Pixel alternative mode (Supported in both video and command mode)
25	MIPI A Dither Enable MIPI is supported only in video mode for vlv C0 only This bit enables or disables (bypassing) 8-6-bit color dithering function. The usage of this bit would be on for 18-bpp panels and off for 24-bpp panels. 0 = disabled 1 = enabled
24	Reserved
23	SelFlopped HSTX A This bit will be used to mux between the flopped (new) and unflopped (original) versions of the TX HS clock and data. Default 0 = pass through new flopped version of these signals, if set to 1 = pass through the original unflopped version.
22	Reserved
21:18	FLISDSI AdjDly HSTX MIPI A These four bits act as an encoded count of the number of buffer delays to insert on the ckdsi2x clock going to the six flops that are storing the HS TX data and clock signals. Default is 4'b0000 which is the equivalent of 1 buffer delay. Will need to set these bits to a value determined by clock timing team before using the MIPI DSI HS TX feature
17	AFE Latchout This bit reflect the value of the output latch of CLK A lane in DSI AFE b1 = current value of output latch is 1 (D-PHY is in LP11 state) b0 = current value of output latch is 0 (D-PHY is in LP00 state) The software driver can read this bit to see if the hold value (LP11 or LP00) to initialize from a sleep state (s0i1 or S0i3) correctly
16	LPOutput Hold

	0= disable transparent latche inside DSI AFE. Output are driven by latch value. 1= enable transparent latch inside DSI AFE so data are driven by DSI DPHY
15	FLISDSI AdjDly HSTX MIPI C high order The fourth bit of four bits act as an encoded count of the number of buffer delays to insert on the ckdsi2x clock going to the six flops that are storing the HS TX data and clock signals. Default is 4'b0000 which is the equivalent of 1 buffer delay. Will need to set these bits to a value determined by clock timing team before using the MIPI DSI HS TX feature
14:11	MIPI4DPHY AdjDly HSTX MIPI C These four bits act as an encoded count of the number of buffer delays to insert on the ckdsi2x clock going to the six flops that are storing the HS TX data and clock signals. Default is 4'b0000 which is the equivalent of 1 buffer delay. Will need to set these bits to a value determined by clock timing team before using the MIPI DSI HS TX feature
10:9	CSB Clock input for bandgap voltage sample and hold circuit. Final setting will be based silicon characterization. 00b = 20mhz clock 01b = 10mhz clock 10b = 40mhz clock 11b = reserved
8	**Reserved**
7:5	FLISDSI AdjDly HSTX MIPI C lower order The lower 3-bit of four bits act as an encoded count of the number of buffer delays to insert on the ckdsi2x clock going to the six flops that are storing the HS TX data and clock signals. Default is 4'b0000 which is the equivalent of 1 buffer delay. Will need to set these bits to a value determined by clock timing team before using the MIPI DSI HS TX feature
4	Delay When set, the TE counter will be count down until
3:2	Effect 00: No tearing effect required - memory write start as soon as write data is available 01: TE trigger by MIPI DPHY and DSI protocol 10: TE trigger by GPIO pin

	11: Reserved
1:0	MIPI Lanes Configuration 00: All 4 MIPI A lanes are assigned to pipe A. All 4 MIPI C lanes are assigned to pipe B. 01: MIPI dual-link mode with data from pipe A 10: MIPI dual-link mode with data from pipe B 11: Reserved Programming note: when MIPI dual-link mode is enabled, the port enable bits in both MIPI A control register and MIPI C control register shall be enabled.

MIPIA_TEARING_CTR

Address Offset:061194h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:16	Reserved
15:0	TE Number of delay clocks from TE trigger to start sending data to DSI controller

MIPIA_AUTOPWG

Address Offset:0611A0h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:0	Reserved

MIPIC_DEVICE_READY_REG – MIPI C Device Ready Register

Address Offset:00B800h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:4	Reserved
3	BUS Possession
2:1	ULPS State 2'b10 = ULPS entry 2'b01 = ULPS exit 2'b00 = Normal operation S/W needs to ensure that there is a minimum of 1ms time available before clearing the UPLS exit State
0	**Device Ready** Set by the processor to inform that device is ready

MIPIC_INTR_STAT_REG

Address Offset:00B804h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31	Tearing Effect Set to indicate that tearing effect trigger message is received
30	SPL PKT Sent Interrupt Set to confirm the transmission of the DPI event specific commands set in the dpi control and dpi data register
29	Gen Read Data Avail Set to indicate that the requested data for a Generic Read request is available in the buffer i.e., generic read response data is available in the read FIFO

28	LP Generic WR FIFO Full Set to indicate that the LP generic write fifo is full
27	HS Generic WR Fifo Full Set to indicate that the HS generic write fifo is full
26	RX Prot Violation Set if DSI protocol violation error is reported in the acknowledge packet by the display device
25	RX Invalid TX Length Set if invalid transmission length error is reported in the acknowledge packet by the display device
24	ACK With No Error Set if acknowledge trigger message is received with out any error
23	Turn Around Ack Timeout Set if a turn around acknowledgement sequence is not received from the display device
22	LP RX Timeout Set if a low power reception count expires this interrupt is generated
21	HS TX Timeout Set if a high speed transmission prevails for more than the expected count value this interrupt is raised
20	DPI FIFO Underrun Set to '1' if there is no data in the dpi fifo to make a in time delivery of the pixel data to the DSI receiver
19	Low Contention Set to '1' if a LP low fault is registered by at the D-PHY contention detector
18	High Contention Set to '1' if a LP high fault is registered by at the D-PHY contention detector
17	TXDSI VC ID Invalid Set to '1' if the received virtual channel ID is invalid
16	TXDSI Data Type Not Recognised Set to '1' if the received data type is not recognised

15	Reserved
14	TXECC Multibit Error Set to '1' if there is no ECC correction for the packet or there are more than 2 bit errors in the packet received by Arasan_DSI_host
13	TXECC Single Bit Error Set to '1' if ECC syndrome was computed and is corrected for one bit error during the reception of packets by the Arasan_DSI_host
12	TXFalse Control Error Set to '1' if a control error is observed on the lanes by the Arasan_DSI_host
11	RXDSI VC ID Invalid Set to '1' if the virtual channel ID is invalid by the display device is reported in the Acknowledge packet by the display device
10	RXDSI Data Type Not Recognised Set to '1' if the data type is not recognised by the display device is reported in the Acknowledge packet by the display device
9	Reserved
8	RXECC Multibit Error Set to '1' if there is no ECC correction for the packet or there are more than 2 bit errors in the packet is reported in the Acknowledge packet by the display device
7	RXECC Single Bit Error Set to '1' if ECC syndrome was computed and corrected for one bit error is reported in the Acknowledge packet by the display device
6	RXFalse Control Error Set to '1' if a control error is reported in the Acknowledge packet by the display device
5	RXHS Receive Timeout Error Set to '1' if the high speed receive timer value expires and data transfer lasts on the data lane is reported in the Acknowledge packet by the display device
4	RX LP TX Sync Error Set to '1' if Low power transmission sync error occurs in the display device and is reported in the Acknowledge packet by the display device

3	RXEscape Mode Entry Error Set to '1' if Escape Mode Entry command is not understandable by the display device and is reported in the Acknowledge packet by the display device
2	RXEOTSyncError
1	RXSOTSyncError Set to '1' if a start of transmission synchronisation error is reported in the Acknowledge packet by the display device
0	RXSOTError Set to '1' if a start of transmission error is reported in the Acknowledge packet by the display device

MIPIC_INTR_EN_REG

Address Offset:00B808h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31	Tearing effect Set to enable tearing effect interrupt
30	SPL Pkt Sent Interrupt Set to enable the confirmation of transmission of the DPI event specific commands set in the dpi control and dpi data register
29	Gen Read Data Avail Set to enable Generic Read available interrupt
28	LP Generic WR FIFO Full Set to indicate that the LP generic write fifo is full
27	HS Generic WR FIFO Full Set to indicate that the HS generic write fifo is full

26	RX Prot Violation Set to enable protocol violation error
25	RX Invalid TX Length Set to enable invalid transmission length error
24	ACK With No Error Set to enable acknowledge trigger message reception with out any error
23	Turn Around ACK Timeout Set to enable turn around acknowledgement ,sequence timeout
22	LP RX Timeout Set to enable low power reception count timeouts
21	HS TX Timeout Set to enable a high speed transmission timeout
20	DPI FIFO Underrun Set to enable if there is no data in the dpi fifo to make a in time delivery of the pixel data to the DSI receiver
19	Low Contention Set to enable a LP low fault interrupt
18	High Contention Set to enable a LP high fault interrupt
17	TXDSI VC ID Invalid Set to enable the interrupt if the received packets virtual channel ID is invalid
16	TXDSI Data Type Not Recognised Set to enable the interrupt if the received packets data type is not recognised
15	Reserved
14	TXECC Multibit Error Set to enable the interrupt if there is no ECC correction for the packet or there are more than 2 bit errors in the packet received by Arasan DSI host
13	TXECC Single bit Error

	Set to enable the interrupt if ECC syndrome was computed and is corrected for one bit error during the reception of packets by the Arasan DSIhost
12	TXFalse Control Error Set to enable the interrupt for the control error.,observed on the lanes by the Arasan_DSI_host
11	RXDSI VC ID Invalid Set to enable the interrupt for invalid virtual channel ID in the acknowledgment packet reports
10	RXDSI Data Type Not Recognised Set to enable the interrupt for the un recognised data type in the acknowledgment packet reports
9	Reserved
8	RXECC Multibit Error Set to enable the interrupt for no ECC correction for the packet or there are more than 2 bit errors reported in the acknowledgment packet
7	RXECC Single bit Error Set to enable the interrupt for ECC syndrome computation and one bit error correction for the acknowledgment packet
6	RXFalse Control Error Set to enable the interrupt for control error in the acknowledgment packet reports
5	RXHS Receive Timeout Error Set to enable the interrupt for the high speed receive timeout Error in the acknowledgment packet reports
4	RX LP TX Sync Error Set to enable the interrupt for Low power transmission sync error in the acknowledgment packet reports
3	RXEscape Mode Entry Error Set to enable the interrupt for Escape Mode Entry command error in the acknowledgment packet reports
2	RXEOTSync Error Set to enable the interrupt for End of transmission synchronisation Error in the acknowledgement packet reports
1	RXSOTSync Error

	Set to enable the interrupt for start of transmission synchronisation error in the acknowledgement packet reports
0	RXSOT Error Set to enable the interrupt for start of transmission error in the acknowledgment packet reports

MIPIC_DSI_FUNC_PRG__REG

Address Offset:00B80Ch

Default Value: 00000001h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:16	Reserved
15:13	Supported Data Width in Command Mode 000 --> Reserved, 001 --> 16 bit data , 010 --> 9 bit data , 011 --> 8 bit data , 100 --> option 1 : 101 --> option 2 : 110 to 111 --> Reserved
12:11	Reserved
10:7	Supported Format In Video Mode Supported colour format, 0001 --> RGB565, 0010 --> RGB666, 0011 --> RGB 666 loosely packed format, 0100 --> RGB888
6:5	Channel Number For Command Mode Virtual channel number for command mode is programmed by the processor

4:3	Channel Number for Video Mode Virtual channel number for command mode is programmed by the processor
2:0	Data Lanes PRG REG Number of data lanes to be supported is programmed by the processor Programming note: For VLV C0, when driver programs this field, it shall program the number of data lanes and txrequesths_0 enable sel in IOSF MIPI RCOMP register Port ID=1B and offset = 0x3 bit[27:24]

MIPIC_HS_TX_TIMEOUT_REG

Address Offset:00B810h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:24	Reserved
23:0	High Speed TX Timeout Counter The maximum duration allowed for the DSI host ,to remain in high speed mode for a transmission. If the counter expires, HS mode is terminated with EOT and the lanes enter stop state

MIPIC_LP_RX_TIMEOUT_REG

Address Offset:00B814h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:24	Reserved
23:0	Low Power Reception Timeout Counter Timeout value to be checked for received short packets .If the timer expires the DSI Host enters stop state

MIPIC_TURN_AROUND_TIMEOUT_REG

Address Offset:00B818h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:6	Reserved
5:0	Turn Around Timeout Register Timeout value to be checked after the DSI host makes a turn around in the direction of transfers. If the timer expires the DSI Host enters stop state

MIPIC_DEVICE_RESET_TIMER

Address Offset:00B81Ch

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:16	Reserved
15:0	Device Reset Timer Timeout value to be checked for device to be reset after issuing reset entry command. If the timer expires the DSI Host enters normal operation

MIPIC_DPI_RESOLUTION_REG

Address Offset:00B820h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:16	Vertical Address

	Shows the vertical address count in lines
15:0	Horizontal Address Shows the horizontal address count in pixels

MIPIC_DBI_RESOLUTION_REG

Address Offset:00B824h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:2	Reserved
1:0	DBI FIFO Thrtl DBI FIFO's watermark can be set using the following bits so as to enable dbi_stall de-assertion whenever the below FIFO condition is reached: 00 - (1/2) DBI fifo empty 01 - (1/4) DBI fifo empty 10 - 7 locations are empty 11 - Reserved

MIPIC_HORIZ_SYNC_PADDING_COUNT

Address Offset:00B828h

Default Value: 00000000h

Normal Attribute: RW

vlv

Size: 32 bits

Bit	Description
31:16	Reserved
15:0	Horizontal Sync Padding Count Shows the horizontal sync padding value in terms of txbyteclkhs

MIPIC_HORIZ_BACK_PORCH_COUNT

Address Offset:00B82Ch

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:16	Reserved
15:0	Horizontal Back Porch Count Shows the horizontal back porch value in terms of txbyteclkhs

MIPIC_HORIZ_FRONT_PORCH_COUNT

Address Offset:00B830h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:16	Reserved
15:0	Horizontal Front Porch Count Shows the horizontal front porch value in terms of txbyteclkhs

MIPIC_HORIZ_ACTIVE_AREA_COUNT

Address Offset:00B834h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:16	Reserved
15:0	Horizontal Active Area Count

	Shows the horizontal active area value in terms of txbyteclkhs

MIPIC_VERT_SYNC_PADDING_COUNT

Address Offset:00B838h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:16	Reserved
15:0	Vertical Sync Padding Count Shows the vertical sync padding value in terms of lines

MIPIC_VERT_BACK_PORCH_COUNT

Address Offset:00B83Ch

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:16	Reserved
15:0	Vertical Back Porch Count Shows the vertical back porch value in terms of lines

MIPIC_VERT_FRONT_PORCH_COUNT

Address Offset:00B840h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:16	Reserved

15:0	Vertical Front Porch Count Shows the vertical front porch value in terms of lines

MIPIC_HIGH_LOW_SWITCH_COUNT

Address Offset:00B844h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:16	Reserved High speed to low power or Low power to high speed switching time in terms of txbyteclkhs
15:0	High Speed to Low Power or Low Power to High Speed Switch Count High speed to low power or Low power to high speed switching time in terms of txbyteclkhs

MIPIC_DPI_CTRL_REG

Address Offset:00B848h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:8	Reserved
7	RSTTRG
6	HS LP Set to '0' to indicate the special packets are sent through the DSI link using HS transmission and set to '1' to indicate that the special packets are sent through the DSI link using low power mode
5	Back Light Off Set to '1' to indicate a backlight OFF short packet has to be packetised for the DPI's virtual channel
4	Back Light on

	Set to '1' to indicate a backlight ON short packet has to be packetised for the DPI's virtual channel
3	Color Mode Off Set to '1' to indicate a color mode OFF short packet has to be packetised for the DPI's virtual channel
2	Color Mode On Set to '1' to indicate a color mode ON short packet has to be packetised for the DPI's virtual channel
1	Turn On Set to '1' to indicate a turn on short packet has to be packetised for the DPI's virtual channel
0	Shut Down Set to '1' to indicate a shut down short packet has to be packetised for the DPI's virtual channel

MIPIC_DPI_DATA_REGISTER

Address Offset:00B84Ch

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:6	Reserved
5:0	Command Byte Command Byte to represent the new or not defined command bytes usage for special features representation. [Like backlight ON and OFF]. This register should be programmed before the DPI control register is being programmed for backlight ON/OFF

MIPIC_INIT_COUNT_REGISTER

Address Offset:00B850h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:16	Reserved
15:0	Master Init Timer Counter value in terms of low power clock to initialise the DSI Host IP [TINT] that drives a stop state on the mipi's D-PHY bus

MIPIC_MAX_RETURN_PKT_SIZE_REGISTER

Address Offset:00B854h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:10	Reserved
9:0	Max Return Pkt Size Set the count value in bytes to collect the return data packet for reverse direction data flow in data lane0 in response to a DBI read operation

MIPIC_VIDEO_MODE_FORMAT_REGISTER

Address Offset:00B858h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:5	Reserved
4	Ramdom DPI Display Resolution Defeature Set by the processor to support random DPI display resolution 0 – random DPI display resolution support disabled 1 – random DPI display resolution support enabled
3	Disable video BTA Set by the processor to inform the DSI controller to disable the BTA sent at the last blanking line of VFP.

	By default, this bit is set to 0. 0 – BTA sending at the last blanking line of VFP is enabled. 1 – BTA sending at the last blanking line of VFP is disabled
2	IP TG Config Set by the processor to inform that the DSI controller should discontinue the DPI transfer after the last line of the VFP after ip_tg_enable deassertion. By default, this bit is set to 0. 0 - After ip_tg_enable deassertion, DSI Tx controller stops the DPI transfer immediately after the current packet is transmitted. 1 - After ip_tg_enable deassertion, DSI Tx controller discontinues the DPI transfer after the last line of the VFP
1:0	Video Mode FMT Sets the Video mode format (packet sequence) to be supported in DSI. In Non Burst Mode, in addition to programming this register the horizontal active area count register value should also be programmed equal to RGB word count value In Burst Mode, in addition to programming this register the horizontal active area count register value should also be programmed greater than the RGB word count value, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link. 00 – Reserved 01 - Non Burst Mode with Sync Pulse 10 - Non Burst Mode with Sync events 11 - Burst Mode

MIPIC_EOT_DISABLE_REGISTER

Address Offset:00B85Ch

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:8	Reserved
7	LP RX Timeout Error Recovery Disable Set by the processor to enable or disable the LP_Rx_timeout error recovery if the processor clears LP_Rx_timeout error interrupt. 0 - LP_Rx_timeout error recovery action will be taken by the DSI Tx controller if the processor clears the LP_Rx_timeout error interrupt. 1 - If the processor clears the LP_Rx_timeout error interrupt, LP_Rx_timeout error recovery action will not happen in DSI Tx contorller. LP Rx timeout error interrupt will act as an informative

	interrupt
6	HS TX Timeout Error Recovery Disable Set by the processor to enable or disable the HS_Tx_timeout error recovery if the processor clears HS_Tx_timeout interrupt. 0 - HS_Tx_timeout error recovery action will be taken by the DSI Tx controller if the processor clears the HS_Tx_timeout error interrupt. 1 - If the processor clears the HS_Tx_timeout error interrupt, HS_Tx_timeout error recovery action will not happen in DSI Tx contorller. HS Tx timeout error interrupt will act as an informative interrupt
5	Low Contention Recovery Disable Set by the processor to enable or disable the contention recovery procedure if the processor clears Low contention interrupt. 0 - Contention recovery will happen if the processor clears Low contention interrupt. 1 - If the processor clears the low contention interrupt, contention recovery procedure will not be initiated by the DSI Tx contorller. Low contention interrupt will act as an informative interrupt
4	High Contention Recovery Disable Set by the processor to enable or disable the contention recovery procedure if the processor clears High contention interrupt. 0 - Contention recovery will happen if the processor clears High contention interrupt. 1 - If the processor clears the high contention interrupt, contention recovery procedure will not be initiated by the DSI Tx contorller. Ignore the High Contention Interrupt in MIPI_INTR_STAT_REG
3	TXDSI Type Not Recognised Error Recovery Disable Set by the processor to enable or disable the error recovery action to be taken by the DSI Tx controller if TxDSI data type not recognised error interrupt is cleared by the processor. 0 - Error recovery action will be taken if TxDSI data type not recognised error interrupt is cleared by the processor. 1 - If TxDSI data type not recognised error interrupt is cleared by the processor, error recovery action will not be taken by the DSI TX controller. Tx DSI data type not recognized error interrupt will act as an informative interrupt
2	TXECC Multibit Err Recovery Disable Set by the processor to enable or disable the error recovery action to be taken by the DSI Tx controller if Tx ECC multibit error interrupt is cleared by the processor. 0 - Error recovery action will be taken if Tx ECC multibit error interrupt is cleared by the processor.

	1 - If Tx ECC multibit error interrupt is cleared by the processor, error recovery action will not be taken by the DSI TX controller. Tx multibit error interrupt will act as an informative interrupt
1	ClockStop Set by the processor to enable or disable clock stopping feature during BLLP timing in a DPI transfer in dual channel mode or during DPI only mode and also when there is no traffic in the DBI interface in DBI only enabled mode. By default this register value is 0. 0 - clock stopping disabled 1 - clock stopping enabled
0	EOT Dis Set by the processor to enable or disable EOT short packet transmission. By default this register value is 0. For backward comapatibility of earlier DSI systems, EOT short packet transmission can be disabled. 0 - EOT short packet transmission enabled 1 - EOT short packet transmission disabled

MIPIC_LP_BYTECLK_REGISTER

Address Offset:00B860h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:16	Reserved
15:0	LP Byteclk Low power clock equivalence in terms of byte clock. The value programmed in this register is equal to the number of byte clocks occupied in one low power clock. This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc)

MIPIC_LP_GEN_DATA_REGISTER

Address Offset:00B864h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:0	LP Gen Data Data port register used for generic data transfers in low power mode

MIPIC_HS_GEN_DATA_REGISTER

Address Offset:00B868h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:0	HS Gen Data Data port register used for generic data transfers in low power mode

MIPIC_LP_GEN_CTRL_REGISTER

Address Offset:00B86Ch

Default Value: 00000000h

Normal Attribute:WO

Size: 32 bits

Bit	Description
31:24	Reserved
23:8	Word Count Specifies the word count for generic long packet Specifies the accompanied parameters for generic short packets. Note: Invalid parameters must be set to 00h
7:6	Virtual Channel Used to specify the virtual channel for which the generic data transmission is intended
5:0	Data type Used to specify the generic data types 03h - Generic short write, no parameters

	13h - Generic short write, 1 parameter 23h - Generic short write, 2 parameters 04h - Generic read, no parameters 14h - Generic read, 1 parameter 24h - Generic read 2 parameter 29h - Generic long write 05h – Manufacturer DCS short write, no parameter 15h – Manufacturer DCS short write, one parameter 06h – Manufacturer DCS read, no parameter 39h – Manufacturer DCS long write

MIPIC_HS_GEN_CTRL_REGISTER

Address Offset:00B870h

Default Value: 00000000h

Normal Attribute:WO

Size: 32 bits

Bit	Description
31:24	Reserved
23:8	Word Count Specifies the word count for generic long packet Specifies the accompanied parameters for generic short packets. Note: Invalid parameters must be set to 00h
7:6	Virtual Channel Used to specify the virtual channel for which the generic data transmission is intended
5:0	Data type Used to specify the generic data types 03h - Generic short write, no parameters 13h - Generic short write, 1 parameter 23h - Generic short write, 2 parameters 04h - Generic read, no parameters

	14h - Generic read, 1 parameter 24h - Generic read 2 parameter 29h - Generic long write 05h – Manufacturer DCS short write, no parameter 15h – Manufacturer DCS short write, one parameter 06h – Manufacturer DCS read, no parameter 39h – Manufacturer DCS long write

MIPIC_GEN_FIFO_STAT_REGISTER

Address Offset:00B874h

Default Value: 1E060606h

Normal Attribute: RO

Size: 32 bits

Bit	Description
31:29	Reserved
28	DPI FIFO Empty Default 1
27	DBI FIFO Empty Default 1
26	LP Ctrl FIFO Empty Default 1
25	LP Ctrl FIFO Half Empty Default 1
24	LP Ctrl FIFO Full Default 0
23:19	Reserved
18	HS Ctrl FIFO Empty Default 1

17	HS Ctrl FIFO Half Empty Default 1
16	HS Ctrl FIFO Full Default 0
15:11	Reserved
10	LP Data FIFO Empty Default 1
9	LP Data FIFO Half Empty Default 1
8	LP Data FIFO Full Default 0
7:3	Reserved
2	HS Data FIFO Empty Default 1
1	HS Data FIFO Half Empty Default 1
0	HS Data FIFO Full Default 0

MIPIC_HS_LS_DBI_ENABLE_REG

Address Offset:00B878h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Description:Note: dbi_hs_lp_switch_reg has to be written only if DBI FIFO is empty

Bit	Description
31:1	Reserved
0	DBI HS LS Switch Re

	Set to 1 if DBI packets have to be transmitted in Low power mode Set to 0 if DBI packets have to be transmitted in High speed mode

MIPIC_RESERVED

Address Offset:00B87Ch

Default Value: 00000000h

Normal Attribute: RO

Size: 32 bits

Bit	Description
31:0	Reserved

MIPIC_DPHY_PARAM_REG

Address Offset:00B880h

Default Value: 0B061A04h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:30	Reserved
29:24	Exit Zero Count THS_0_TIM_UI_CNT and THS_EXIT_TIM_UI_CNT for dphy are programmed as exit zero count by the processor
23:21	Reserved
20:16	Trail Count TCLK_POST_TIM_UI_CNT and TCLK_TRAIL_TIM_UI_CNT for dphy are programmed as trail count by the processor
15:8	CLK Zero Count TCLK_0_TIM_UI_CNT for dphy is programmed as clk zero count by the processor
7:6	Reserved
5:0	Prepare Count

	TCLK_PREP_TIM_UI_CNT and THS_PREP_TIM_UI_CNT for dphy are programmed as prepare count by the processor

MIPIC_DBI_BW_CTRL_REG

Address Offset:00B884h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:0	Bandwidth Timer DBI Bandwidth control Register. The bandwidth essential for transmitting 16 long packets containing 252 bytes meant for DCS write memory command is programmed in this register in terms of byte clocks. Based on the DSI transfer rate and the number of lanes configured the time taken to transmit 16 long packets in a DSI stream varies. Note: The value programmed in this timer must be greater than the actual time taken to carryout 16 long packets transmission in DSI stream plus the time taken to transmit two blanking packets

MIPIC_CLK_LANE_SWITCHING_TIME_CNT

Address Offset:00B888h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:16	LS HS SSW Cnt Low power to high speed switching time in terms byte clock (txbyteclkhs). This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc). Typical value - Number of byte clocks required to switch from low power mode to high speed mode after txrequesths_clk is asserted. Current Value is ah = 10 txbyteclkhs
15:0	HS LS Pwr SW Cnt High speed to low power switching time in terms byte clock (txbyteclkhs). This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc). Typical value - Number of byte clocks request to switch from high speed mode to low power mode after txrequesths_clk is

	de-asserted. Current Value is 14h = 20 txbyteclkhs

MIPIA_CLK_LANE_SWITCHING_TIME_CNT

Address Offset:00B088h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:16	LS HS SSW Cnt Low power to high speed switching time in terms byte clock (txbyteclkhs). This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc). Typical value - Number of byte clocks required to switch from low power mode to high speed mode after txrequesths_clk is asserted. Current Value is ah = 10 txbyteclkhs
15:0	HS LS Pwr SW Cnt High speed to low power switching time in terms byte clock (txbyteclkhs). This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc). Typical value - Number of byte clocks request to switch from high speed mode to low power mode after txrequesths_clk is de-asserted. Current Value is 14h = 20 txbyteclkhs

MIPIC_STOP_STATE_STALL

Address Offset:00B88Ch

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:8	Reserved
7:0	STOP STATE STALL COUNTER Delay between (stall the stop state signal) the data transfer is increased based on this counter

	value. This counter is calculated from txclkesc. Note: If processor programs this register then it needs to reprogram the high_low_ switch counter in B844h and lp_equivalent_byteclk reg in B860h to compensate this delay. High_low_switch_count B844h: High to low switch counter = Actual High to low switch + stop_sta_stall_reg value * Low power clock equivalence value in terms of byte clock LP equivalent byteclk register B860h: LP equivalent byteclk value = txclkesc time/ txbyteclk time * (105 + stop_sta_stall_reg value) / 105 Minimum time of Low Power short packet transfer = 105 txclkesc

MIPIC_INTR_STAT_REG_1

Address Offset:00B890h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:1	Reserved
0	RX Contention Detected Set to 1'b1 if the contention detected in the display device and is reported in the Acknowledge packet by the display device

MIPIC_INTR_EN_REG_1

Address Offset:00B894h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:1	Reserved
0	Enable RX Contention Detected

	Set to enable the interrupt for contention detected error in the acknowledgement packet reports

MIPIC_CTRL

Address Offset:00B904h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

MIPI adapter has a control register with options to control width of the dbi bus and the divide value of the clock that needs to be supplied to the Clocks module so that a 2x divided clock can be provided to the MIPI D-PHY IP.Self refresh capability is in DCS commands. The other 3 controls bits (SD, CM and back light control) are now moved to MIPI IP registers

Bit	Description
31:5	Reserved
4:3	Status 2'b00: low priority on read requests to G-unit 2'b11 : high priority
2	RGB Flip 1'b0 : RGB data from disp2d is reverted to BGR 1'b1 : RGB data from disp2d is passed as is to MIPI IP
1:0	Reserved

MIPIC_DATA_ADD

Address Offset:00B908h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:5	Data Mem Addr When there is updated data for the display panel, S/W programs this register with the memory

	address to read from
4:1	Reserved
0	Data Valid This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

MIPIC_DATA_LEN

Address Offset:00B90Ch

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:20	Reserved
19:0	Data Length This field shows the remaining length of data that needs to be read from memory, Initially set by S/W and is decremented by H/W as reads are issued

MIPIC_CMD_ADD

Address Offset:00B910h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:5	Command Mem Addr When there are new commands that need to be sent to the display panel, S/W programs this register with the memory address to read the commands from
4:3	Reserved MBZ
2	MIPIC Auto PWG Enable

	Idle state: SW driver writes to this bit to enable auto power gating for MIPIC controller 0: default 1: auto power gate is enabled
1	Command Data Mode 0: data for memory write command from system buffer that is specified by MIPI data address register 1: data for memory write command from pipe A rendering
0	Command Valid This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

MIPIC_CMD_LEN

Address Offset:00B914h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:24	Command 3 This is command 3 length (command + parameters) in bytes
23:16	Command 2 This is command 2 length (command + parameters) in bytes
15:8	Command 1 This is command 1 length (command + parameters) in bytes
7:0	Command 0 This is command 0 length (command + parameters) in bytes

MIPIC_RD_DATA_RETURN0

Address Offset:00B918h

Default Value: 00000000h

Normal Attribute: RO

Size: 32 bits

In addition to the command and data registers, adapter provides 8 read only registers for S/W to read the return data from the panel. At this time the usage case for the read path from the panel is for configuration reads only. Hence, more than 4 bytes of read are not allowed. Maximum read return size in the MIPI IP should be no greater than 32 bytes

Bit	Description
31:0	RD Data Return Panel This is the configuration data returned from the panel

MIPIC_RD_DATA_RETURN1

Address Offset:00B91Ch

Default Value: 00000000h

Normal Attribute: RO

Size: 32 bits

In addition to the command and data registers, adapter provides 8 read only registers for S/W to read the return data from the panel. At this time the usage case for the read path from the panel is for configuration reads only. Hence, more than 4 bytes of read are not allowed. Maximum read return size in the MIPI IP should be no greater than 32 bytes

Bit	Description
31:0	RD Data Return Panel This is the configuration data returned from the panel

MIPIC_RD_DATA_RETURN2

Address Offset:00B920h

Default Value: 00000000h

Normal Attribute: RO

Size: 32 bits

In addition to the command and data registers, adapter provides 8 read only registers for S/W to read the return data from the panel. At this time the usage case for the read path from the panel is for configuration reads only. Hence, more than 4 bytes of read are not allowed. Maximum read return size in the MIPI IP should be no greater than 32 bytes

Bit	Description
31:0	RD Data Return Panel This is the configuration data returned from the panel

MIPIC_RD_DATA_RETURN3

Address Offset:00B924h

Default Value: 00000000h

Normal Attribute: RO

Size: 32 bits

In addition to the command and data registers, adapter provides 8 read only registers for S/W to read the return data from the panel. At this time the usage case for the read path from the panel is for configuration reads only. Hence, more than 4 bytes of read are not allowed. Maximum read return size in the MIPI IP should be no greater than 32 bytes

Bit	Description
31:0	RD Data Return Panel This is the configuration data returned from the panel

MIPIC_RD_DATA_RETURN4

Address Offset:00B928h

Default Value: 00000000h

Normal Attribute: RO

Size: 32 bits

In addition to the command and data registers, adapter provides 8 read only registers for S/W to read the return data from the panel. At this time the usage case for the read path from the panel is for configuration reads only. Hence, more than 4 bytes of read are not allowed. Maximum read return size in the MIPI IP should be no greater than 32 bytes

Bit	Description
31:0	RD Data Return Panel This is the configuration data returned from the panel

MIPIC_RD_DATA_RETURN5

Address Offset:00B92Ch

Default Value: 00000000h

Normal Attribute: RO

Size: 32 bits

In addition to the command and data registers, adapter provides 8 read only registers for S/W to read the return data from the panel. At this time the usage case for the read path from the panel is for configuration reads only. Hence, more than 4 bytes of read are not allowed. Maximum read return size in the MIPI IP should be no greater than 32 bytes

Bit	Description
31:0	RD Data Return Panel This is the configuration data returned from the panel

MIPIC_RD_DATA_RETURN6

Address Offset:00B930h

Default Value: 00000000h

Normal Attribute: RO

Size: 32 bits

In addition to the command and data registers, adapter provides 8 read only registers for S/W to read the return data from the panel. At this time the usage case for the read path from the panel is for configuration reads only. Hence, more than 4 bytes of read are not allowed. Maximum read return size in the MIPI IP should be no greater than 32 bytes

Bit	Description
31:0	RD Data Return Panel This is the configuration data returned from the panel

MIPIC_RD_DATA_RETURN7

Address Offset:00B934h

Default Value: 00000000h

Normal Attribute: RO

Size: 32 bits

In addition to the command and data registers, adapter provides 8 read only registers for S/W to read the return data from the panel. At this time the usage case for the read path from the panel is for configuration reads only. Hence, more than 4 bytes of read are not allowed. Maximum read return size in the MIPI IP should be no greater than 32 bytes

Bit	Description
31:0	RD Data Return Panel This is the configuration data returned from the panel

MIPIC_RD_DATA_VALID

Address Offset:00B938h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:8	Reserved
7:0	Read Data Valid Each bit corresponds to presence of valid data in the registers above. When data is returned from the panel, H/W will write into these registers in sequence, and set the corresponding valid bit. When S/W issues a write '1 to the registers, this bit is cleared

MIPIC_PORT_CTRL

Address Offset:061700h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31	EN When this bit is disabled the MIPI DPI (video mode) is inactive and in it's low power state. When it is enable it starts to generate timing for this MIPI port 0 = The port is disabled and all MIPI DPI interface are disable (timing generator is off) 1 = The port is enabled
30:26	Reserved

25	MIPI C Dithering Enable MIPI dithering is supported only in video mode for VLV C0 This bit enables or disables (bypassing) 8-6-bit color dithering function. The usage of this bit would be on for 18-bpp panels and off for 24-bpp panels. 0 = disabled 1 = enabled
24:22	Reserved
21	Reserved
20	Reserved
19	Reserved
18:16	Reserved
15	Reserved
14:5	Reserved
4	Delay When set, the TE counter will be count down until
3:2	Effect 00: No tearing effect required - memory write start as soon as write data is available 01: TE trigger by MIPI DPHY and DSI protocol 10: TE trigger by GPIO pin 11: Reserved
1:0	Reserved

MIPIC_TEARING_CTR

Address Offset:061704h

Default Value: 00000000h

Normal Attribute: RW

Size: 32 bits

Bit	Description
31:16	Reserved
15:0	TE Number of delay clocks from TE trigger to start sending data to DSI controller