Intel® Open Source HD Graphics

Programmer's Reference Manual

For the 2016 Intel Atom™ Processors, Celeron™ Processors, and Pentium™ Processors based on the "Apollo Lake" Platform (Broxton Graphics)

Volume 3: Configurations

May 2017, Revision 1.0

Creative Commons License

Notices and Disclaimers

Table of Contents

Configurations Overview

The Intel "Gen" Graphics Architecture was first introduced to the market in 2004. Since that time, the architecture and implementation have evolved to add many new features, increase performance, and improve power efficiency.

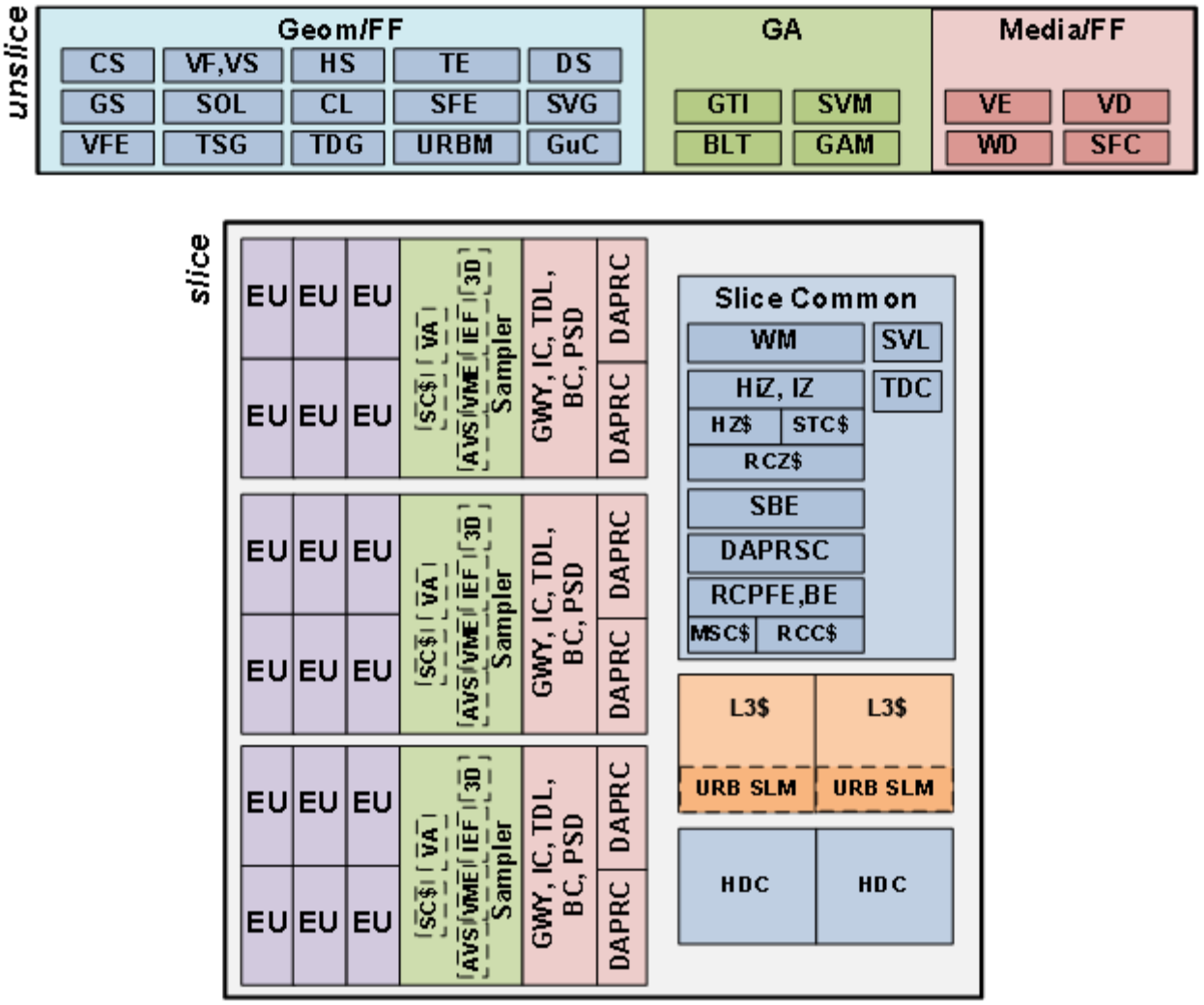
Each product generation has its own configurations chapter. Each chapter has a section for each project, and each project contains the following subsections:

- Top Level Block Diagrams - Show basic feature blocks of the project's graphics architecture, for GT configurations.
- Device Attributes - List details of the graphics configuration options for each project.
- Steppings and Device IDs - Lists all of the current unique GT Die / Packages for a specific project.

Top Level Block Diagrams

This topic shows basic feature blocks of the Broxton (BXT) graphics architecture.

3x6 Configuration



This diagram is based on the following functional partitions:

(a) Geometry Fixed Functions (Geom/FF)

(b) Media Fixed Functions (Media/FF)

(c) Global Assets and GT Interface (GA)

(d) One or more Subslices (three shown)

(e) A Slice Common block

(f) An L3 Cache (L3$) block

Note that the combination of (a), (b), and (c) is typically referred to as the “unslice”, while a combination of (d), (e), and (f) is referred to as a compute “slice”.

The functionality in each of these groupings is further broken down as follows:

- Unslice – Fixed function pipelines for 3D, GPGPU, and Media operations, and interface to the outside world.
    - The 3D Geometry / Fixed Function (Geom/FF) block consisting of:
        - 3D fixed function pipeline (Command Stream-CS, Vertex Fetch-VF, Vertex Shader-VS, Hull Shader-HS, Tessellation Engine-TE, Domain Shader-DS, Geometry Shader-GS, Stream Output Logic-SOL, Clipper-CL, Strip/Fan Engine-SF, State Variable Global-SVG)
        - Video Front-End unit (VFE)
        - Thread Spawner unit (TSG) and the global Thread Dispatcher unit (TDG)
        - Unified Return Buffer Manager (URBM)
    - Media fixed function assets:
        - Video Decode (VD) Box
        - Video Encode (VE) Box
        - Wireless Display (WD) BOX
        - SFC
    - The Global Assets (GA) block as the primary interface and memory stream gateway to the outside world, consisting of:
        - GT Interface (GTI)
        - State Variable Manager (SVM)
        - Blitter (BLT)
        - Graphics Arbiter (GAM)
- Subslice (three shown) – A compute unit with supporting fixed- or shared-function assets sufficient for the EU capability.
    - A bank of Execution Units (EUs) – eight per subslice shown
    - Sampler, supporting both media and 3D functions
    - Gateway (GWY)
    - Instruction cache (IC)
    - Local Thread Dispatcher (TDL)
    - Barycentric Calculator (BC)
    - Pixel Shader Dispatcher (PSD)
    - Data Cluster (HDC)
    - Dataport Render Cache (DAPRC) - two per subslice
- Slice Common – Scalable fixed function assets which support the compute horsepower provided two or more subslices.
    - 3D Fixed Function:

        - Windower/Mask unit (WM)
        - Hi-Z (HZ) and Intermediate Z (IZ)
        - Setup Backend (SBE)
        - RCPFE, BE
        - 3D stream caches (RCC$, MSC$, HZ$, STC$, RCZ$)
    - Media Fixed Functions:
        - DAPRSC
        - SVL
        - TDC
- L3 Cache – backing L3 cache for certain memory streams emanating from subslices.
    - L3 Data cache with support for data, URB, and shared local memory (SLM)

Device Attributes

The following table lists detailed GT device attributes for proposed BXT SKUs.

Product Configuration Attribute Table

Product Family	**BXT**
Architectural Name *	**3x6**
SKU Name	
Slice count	1
Subslice Count	3
EU/Subslice	6
EU count (total)	18
Thread Count	6
Thread Count (Total)	108
FLOPs/Clk - Half Precision, MAD (peak)	576
FLOPs/Clk - Single Precision, MAD (peak)	288
FLOPs/Clk - Double Precision, MAD (peak) [a]	36
Unslice clocking (coupled/decoupled from Cr slice) [b]	coupled
GTI / Ring Interfaces	1
GTI bandwidth (bytes/unslice-clk)	64: R
	64: W
Graphics Virtual Address Range	48 bit
Graphics Physical Address Range	39 bit
L3 Cache, total size (bytes)	384K
L3 Cache, bank count	2
L3 Cache, bandwidth (bytes/clk)	4x 64: R|W
L3 Cache, D$ Size (Kbytes)	192K-256K
URB Size (kbytes)	128K-192K
SLM Size (kbytes)	0, 128K
LLC/L4 size (bytes)	N/A
Instruction Cache (IC, bytes)	3x 48K
Color Cache (RCC, bytes)	24K
MSC Cache (MSC, bytes)	16K
HiZ Cache (HZC, bytes)	8K
Z Cache (RCZ, bytes)	32K
Stencil Cache (STC, bytes)	8K
FMAD, SP (ops/EU/clk)	8
FMUL, SP (ops/EU/clk)	8

FADD, SP (ops/EU/clk)	8
MIN,MAX, SP (ops/EU/clk)	8
CMP, SP (ops/EU/clk)	8
INV, SP (ops/EU/clk)	2
SQRT, SP (ops/EU/clk)	2
RSQRT, SP (ops/EU/clk)	2
LOG, SP (ops/EU/clk)	2
EXP, SP (ops/EU/clk)	2
POW, SP (ops/EU/clk)	1
IDIV, SP (ops/EU/clk)	1-6
TRIG, SP (ops/EU/clk)	2
FDIV, SP (ops/EU/clk)	1
Data Ports (HDC) [c]	2
L3 Load/Store - same addresses within msg (dwords/clk)	2x 32
L3 Load/Store - unique addresses within msg (dwords/clk)	
SLM Load//Store - same addresses within msg (dwords/clk)	
SLM Load//Store - unique addresses within msg (dwords/clk)	
Atomic, Local 32b - same addresses within msg (dwords/clk)	
Atomic, Global 32b - unique addresses within msg (dwords/clk)	
Geometry pipes	1
Samplers (3D)	3
Texel Rate, point, 32b (tex/clk)	12
Texel Rate, point, 64b (tex/clk)	12
Texel Rate, point, 128b (tex/clk)	12
Texel Rate, bilinear, 32b (tex/clk)	12
Texel Rate, bilinear, 64b (tex/clk)	12
Texel Rate, bilinear, 128b (tex/clk)	6
Texel Rate, trilinear, 32b (tex/clk)	12
Texel Rate, trilinear, 64b (tex/clk)	6
Texel Rate, trilinear, 128b (tex/clk)	1.5
Texel Rate, aniso 2x, MIP Linear, 32b (tex/clk)	3
Texel Rate, aniso 4x, MIP Linear,32b (tex/clk)	1.5
Texel Rate, ansio 8x, MIP Linear,32b (tex/clk)	0.75
Texel Rate, ansio 16x, MIP Linear,32b (tex/clk)	0.375
HiZ Rate, (ppc)	32
IZ Rate, (ppc)	16
Stencil Rate (ppc)	32

(500 MHz, DDR-2400 or eDRAM; Range depends on dynamic compression ratio)	
Pixel Rate, fill, 32bpp (pix/clk, RCC hit)	8
Pixel Rate, fill, 32bpp (pix/clk, LLC hit @ 1.0x unslice clk)	N/A
Pixel Rate, fill, 32bpp (pix/clk, LLC hit, @ 1.5x unslice clk)	N/A
Pixel Rate, fill, 32bpp (pix/clk, memory, @ 1.0x unslice clk)	8
Pixel Rate, fill, 32bpp (pix/clk, memory, @ 1.5x unslice clk)	N/A
(500 MHz, DDR-2400 or eDRAM; Range depends on dynamic compression ratio)	
Pixel Rate, blend, 32bpp (p/clk, RCC hit)	8
Pixel Rate, blend, 32bpp (p/clk, LLC hit, @ 1.0x unslice clk)	N/A
Pixel Rate, blend, 32bpp (p/clk, LLC hit, @ 1.5x unslice clk)	N/A
Pixel Rate, blend, 32bpp (pix/clk, memory, @ 1.0x unslice clk)	8
Pixel Rate, blend, 32bpp (pix/clk, memory, @ 1.5x unslice clk)	N/A
Samplers (media)	3
VDBox Instances	1
VEBox Instances	1
SFC Instances	1
WGBox Instances	1
Display Pipes	3
Display Planes per Pipe	4+4+3

Notes:

* Architectural Name = Subslice Count x EUs per Subslice

A brief explanation of the listed SKUs is as follows:

- 3x6 has three subslices, with six EUs each for a total of 3 x 6 = 18 EUs.

Programming Note	
Context:	Device Attributes
Double precision support in hardware is TBD.	

Programming Note	
Context:	Device Attributes
Unslice clock and slice clock are coupled; independent frequency control is not supported.	

Programming Note	
Context:	Device Attributes
Unlike other Gen variants, this version shares HDCs units across subslices.	

Steppings and Device IDs

Broxton GT Unique Devices

The following table lists current unique GT Die / Packages steppings for BXT. Prior to manufacturing, this information is subject to change at any time.

SOC SKU	GT SKU	SOC Stepping	GT/Disp Stepping	Native Device2 ID	GT Device2 Revision ID	Comments	Project
BXT	3x6	C0	D0	0x1A84 (18EU) 0x1A85 (12EU)	0x0C	PRQ Base Candidate	BXT:3x6
APL	3x6	B1	C0	0x5A84 (18 EU) 0x5A85 (12 EU)	0x0A	ApolloLake PRQ Base Candidate	BXT:3x6
APL	3x6	B2	C0	0x5A84 (18 EU) 0x5A85 (12 EU)	0x0B	ApolloLake PRQ for CCG	BXT:3x6
APL	3x6	E0	D0	0x5A84 (18 EU) 0x5A85 (12 EU)	0x0C	ApolloLake PRQ stepping for IOTG	BXT:3x6