Intel® Open Source HD Graphics

Programmer's Reference Manual

For the 2016 Intel Atom™ Processors, Celeron™ Processors, and Pentium™ Processors based on the "Apollo Lake" Platform (Broxton Graphics)

Volume 2b: Command Reference: Registers

May 2017, Revision 1.0

Creative Commons License

You are free to Share - to copy, distribute, display, and perform the work under the following conditions:

- **Attribution.** You must attribute the work in the manner specified by the author or licensor (but not in any way that suggests that they endorse you or your use of the work).
- **No Derivative Works.** You may not alter, transform, or build upon this work.

Notices and Disclaimers

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

A "Mission Critical Application" is any application in which failure of the Intel Product could result, directly or indirectly, in personal injury or death. SHOULD YOU PURCHASE OR USE INTEL'S PRODUCTS FOR ANY SUCH MISSION CRITICAL APPLICATION, YOU SHALL INDEMNIFY AND HOLD INTEL AND ITS SUBSIDIARIES, SUBCONTRACTORS AND AFFILIATES, AND THE DIRECTORS, OFFICERS, AND EMPLOYEES OF EACH, HARMLESS AGAINST ALL CLAIMS COSTS, DAMAGES, AND EXPENSES AND REASONABLE ATTORNEYS' FEES ARISING OUT OF, DIRECTLY OR INDIRECTLY, ANY CLAIM OF PRODUCT LIABILITY, PERSONAL INJURY, OR DEATH ARISING IN ANY WAY OUT OF SUCH MISSION CRITICAL APPLICATION, WHETHER OR NOT INTEL OR ITS SUBCONTRACTOR WAS NEGLIGENT IN THE DESIGN, MANUFACTURE, OR WARNING OF THE INTEL PRODUCT OR ANY OF ITS PARTS.

Intel may make changes to specifications and product descriptions at any time, without notice. Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined". Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. The information here is subject to change without notice. Do not finalize a design with this information.

The products described in this document may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Implementations of the I2C bus/protocol may require licenses from various entities, including Philips Electronics N.V. and North American Philips Corporation.

Intel and the Intel logo are trademarks of Intel Corporation in the U.S. and other countries.

* Other names and brands may be claimed as the property of others.

Table of Contents

Arbiter Control Register

GARBCNTLREG - Arbiter Control Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x29124100
Size (in bits):	32
Address:	0B004h

DWord	Bit	Description
0	31	**Reserved**
	30	**Disables hashing function** Access: R/W Disables hashing function to generate bank_id[1:0] for L3$ bank accessing, and forces the use of address[7:6] for bank_id[1:0]. 0: (default) Hash function enabled to generate L3$ bank IDs. 1: L3$ address[7:6] used as L3$ bank IDs. lncf_csr_l3bankidhashdis. (This bit needs to set corresponding bit lpfcon_csr_l3bankidhashdis in LPFC.)
	29:28	**Arbitration priority order between RCC and MSC** Default Value: 10b Access: R/W Arbitration priority order between RCC and MSC. 00b/11b: Invalid; default setting used. 10b: Default setting; RCC MSC (i.e., MSC has higher priority). 01b: RCC MSC (i.e., RCC has higher priority). lncf_csr_rcc_msc_pri[1:0].
	27:22	**Arbitration priority order between RCZ, STC, and HIZ** Default Value: 100100b Access: R/W Arbitration priority order between RCZ, STC, and HIZ. 100100b: Default setting; RCZ STC HIZ. (i.e., RCZ has lowest priority; HIZ has highest priority). 100001b: RCZ ; HIZ ; STC. 011000b: STC ; RCZ ; HIZ. 010010b: STC ; HIZ ; RCZ. 001001b: HIZ ; RCZ ; STC. 000110b: HIZ ; STC ; RCZ. Note: Others settings are invalid, and result in use of default. lncf_csr_rcz_stc_hiz_pri[5:0].

GARBCNTLREG - Arbiter Control Register

	21:19	**Write data port arbitration priority between Z client writes and L3$ evictions** Default Value: 010b Access: R/W Z Max Write Request Limit Count (GFXC_MRLC). This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (both Slice 0 and 1). Minimum count value must be = 1. Incf_csr_wdpagapz[2:0].
	18:16	**Write data port arbitration priority between C client writes and Z/L3$ writes/evictions** Default Value: 010b Access: R/W C Max Request Limit Count (GFXZ_MRLC). This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (both Slice 0 and 1). Minimum count value must be = 1. Incf_csr_wdpagapc[2:0].
	15	**Reserved** Access: RO
	14:12	**L3 Max Write Request Limit Count** Default Value: 100b Access: R/W L3 Max Write Request Limit Count (GFXL3_MRLC). This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1. Incf_csr_wdpagapl3[2:0].
	11:9	**Reserved** Access: RO
	8	**GAPs_fixarb_en** Default Value: 1b Access: R/W Incf_csr_gaps_fixarb_en.
	7	**Reserved1** Access: RO
	6:0	**Reserved** Access: RO

ASL Storage

ASLS_0_2_0_PCI - ASL Storage	
Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	000FCh

This is a software scratch register. The exact bit register usage must be worked out in common between System BIOS and driver software.
For each device, the ASL control method requires two bits for DOD (BIOS detectable yes or no, VGA/NonVGA), one bit for DGS (enable/disable requested), and two bits for DCS (enabled now/disabled now, connected or not).

DWord	Bit	Description
0	31:0	**Device Switching Storage** Default Value: 00000000000000000000000000000000b Access: R/W Software controlled usage to support device switching.

ATS Capability

ATS_CAP_0_2_0_PCI - ATS Capability

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000020
Size (in bits):	16
Address:	00204h

ATS Capability reports support for Device-TLBs on Device-2, compliant to PCI Express ATS specification.

DWord	Bit	Description
0	15:6	**RESERVED** Access: RO Reserved Value: 000b — Name: **[Default]**
	5	**Page Aligned Request** Default Value: 1b Access: RO Hardwired to 1, the Untranslated Address is always aligned to a 4096 byte boundary. Processor Graphics reports value of 1b indicating all VT-d and SVM translations are page-aligned.
	4:0	**Invalidate Queue Depth** Default Value: 00000b Access: RO The number of Invalidate Requests that the endpoint can accept before putting back pressure on the upstream connection. Hardwired to 0h, the function can accept 32 Invalidate Requests.

ATS Control

ATS_CTRL_0_2_0_PCI - ATS Control

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	16
Address:	00206h

DWord	Bit	Description
0	15	**ATS Enable** Default Value: 0b Access: R/W When Set, the function is enabled to cache translations. Processor graphics ignores this field, as GT uses GTLB as IOTLB and only pretends to software that it has a Device-TLB. Software is expected to Set this field before configuring extended context-entry for Device2 with Page Request Enable field Set. For compatibility, this field is implemented as RW as software can read it to determine ATS enable status.
	14:5	**RESERVED** Default Value: 000b Access: RO Reserved
	4:0	**Smallest Translation Unit** Default Value: 00000b Access: R/W This value indicates to the Endpoint the minimum number of 4096-byte blocks that is indicated in a Translation Completion or Invalidate Request. This is a power of 2 multiple and the number of blocks is 2^STU. A value of 0 indicates one block and value 1F indicates 2^31 blocks. For IGD this must be programmed to 0h for 4KB as smallest translation unit.

ATS Extended Capability Header

ATS_EXTCAP_0_2_0_PCI - ATS Extended Capability Header

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x3001000F
Size (in bits):	32
Address:	00200h

ATS Capability reports support for Device-TLBs on Device-2, compliant to PCI Express ats specification.

DWord	Bit	Description
0	31:20	**Next Capability Offset** Default Value: 001100000000b Access: RO This is a hardwired pointer to the next item in the capabilities list. Value 300h in this field provides the offset for Page-Request Capability.
	19:16	**Version** Default Value: 0001b Access: RO Hardwired to capability version 1.
	15:0	**Capability ID** Default Value: 0000000000001111b Access: RO Hardwired to the ATS Extended Capability ID

Base Data of Stolen Memory

BDSM_0_0_0_PCI - Base Data of Stolen Memory

Register Space:	PCI: 0/0/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	000B0h

This register contains the base address of graphics data stolen DRAM memory.

DWord	Bit	Description
0	31:20	**Graphics Base of Stolen Memory** Default Value: 000000000000b Access: R/W Lock This register contains bits 31 to 20 of the base address of stolen DRAM memory. BIOS determines the base of graphics stolen memory by subtracting the graphics stolen memory size (PCI device 0 offset 50 bits 15:8) from TOLUD (PCI Device 0 offset BC bits 31:20).
	19:1	**RESERVED** Default Value: 000b Access: RO Reserved
	0	**Lock** Default Value: 0b Access: R/W Key Lock This bit will lock all writeable settings in this register, including itself.

Base of GTT Stolen Memory

BGSM_0_0_0_PCI - Base of GTT Stolen Memory

Register Space:	PCI: 0/0/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	000B4h

This register contains the base address of stolen DRAM memory for the GTT.

DWord	Bit	Description
0	31:20	**Graphics Base of GTT Stolen Memory** Default Value: 000000000000b Access: R/W Lock This register contains the base address of stolen DRAM memory for the GTT. BIOS determines the base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI Device 0 offset 50 bits 7:6) from the Graphics Base of Data Stolen Memory (PCI Device 0 offset B0 bits 31:20).
	19:1	**RESERVED** Default Value: 000b Access: RO Reserved
	0	**Lock** Default Value: 0b Access: R/W Key Lock This bit will lock all writeable settings in this register, including itself.

Batch Buffer Per Context Pointer

BB_PER_CTX_PTR - Batch Buffer Per Context Pointer

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1

This register is used to program the batch buffer address to be executed between context restore and execution of ring/execution list if enabled. This will only get executed due to regular context save/restore and not during power restore. This register is part of the execution list context and will be executed per context. Only supported if execution list is enabled. There is no preempting workloads within the Per Context Batch Buffer.

Programming Notes	Source
BlitterCS/VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be programmed for these command streamers.	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS
Render CS: Per Context Batch Buffer execution must not look at the MI_RS_CONTROL or Wait For Event status that are restored for the corresponding context. Ex: A context with MI_RS_CONTROL status with RS disabled doesn't stop Render CS from triggering Resource Streamer to execute Per Context Batch Buffer when "**RS Enabled Batch Buffer Per Context**" is set.	RenderCS
RenderCS: The following commands are not supported within a Per Context Batch Buffer:	RenderCS

Command Name
MI_WAIT_FOR_EVENT
MI_ARB_CHECK
MI_RS_CONTROL
MI_REPORT_HEAD
MI_URB_ATOMIC_ALLOC
MI_SUSPEND_FLUSH
MI_TOPOLOGY_FILTER
MI_RS_CONTEXT
MI_SET_CONTEXT
MI_URB_CLEAR
MI_SEMAPHORE_WAIT (Memory Poll Mode).Note: MI_SEMAPHORE_WAIT in register poll mode is supported.
MI_SEMAPHORE_SIGNAL

BB_PER_CTX_PTR - Batch Buffer Per Context Pointer

MI_BATCH_BUFFER_START
MI_CONDITIONAL_BATCH_BUFFER_END
MEDIA_OBJECT_WALKER
GPGPU_WALKER
3DPRIMITIVE
3DSTATE_BINDING_TABLE_POINTERS_VS
3DSTATE_BINDING_TABLE_POINTERS_HS
3DSTATE_BINDING_TABLE_POINTERS_DS
3DSTATE_BINDING_TABLE_POINTERS_GS
3DSTATE_BINDING_TABLE_POINTERS_PS
3DSTATE_GATHER_CONSTANT_VS
3DSTATE_GATHER_CONSTANT_GS
3DSTATE_GATHER_CONSTANT_HS
3DSTATE_GATHER_CONSTANT_DS
3DSTATE_GATHER_CONSTANT_PS
3DSTATE_DX9_CONSTANTF_VS
3DSTATE_DX9_CONSTANTF_HS
3DSTATE_DX9_CONSTANTF_DS
3DSTATE_DX9_CONSTANTF_GS
3DSTATE_DX9_CONSTANTF_PS
3DSTATE_DX9_CONSTANTI_VS
3DSTATE_DX9_CONSTANTI_HS
3DSTATE_DX9_CONSTANTI_DS
3DSTATE_DX9_CONSTANTI_GS
3DSTATE_DX9_CONSTANTI_PS
3DSTATE_DX9_CONSTANTB_VS
3DSTATE_DX9_CONSTANTB_HS
3DSTATE_DX9_CONSTANTB_DS
3DSTATE_DX9_CONSTANTB_GS
3DSTATE_DX9_CONSTANTB_PS
3DSTATE_DX9_LOCAL_VALID_VS
3DSTATE_DX9_LOCAL_VALID_DS
3DSTATE_DX9_LOCAL_VALID_HS
3DSTATE_DX9_LOCAL_VALID_GS
3DSTATE_DX9_LOCAL_VALID_PS

BB_PER_CTX_PTR - Batch Buffer Per Context Pointer

3DSTATE_DX9_GENERATE_ACTIVE_VS
3DSTATE_DX9_GENERATE_ACTIVE_HS
3DSTATE_DX9_GENERATE_ACTIVE_DS
3DSTATE_DX9_GENERATE_ACTIVE_GS
3DSTATE_DX9_GENERATE_ACTIVE_PS
3DSTATE_BINDING_TABLE_EDIT_VS
3DSTATE_BINDING_TABLE_EDIT_GS
3DSTATE_BINDING_TABLE_EDIT_HS
3DSTATE_BINDING_TABLE_EDIT_DS
3DSTATE_BINDING_TABLE_EDIT_PS
3DSTATE_CONSTANT_VS
3DSTATE_CONSTANT_GS
3DSTATE_CONSTANT_PS
3DSTATE_CONSTANT_HS
3DSTATE_CONSTANT_DS
PIPECONTROL

Workaround	Source
Workaround: [Render CS Only][Execlist Mode of Scheduling] SW must ensure arbitration is switched off while context restore is in progress for any given context. This is achieved by disabling arbitration by programming MI_ARB_ON_OFF to "Arbitration Disable" in RCS_INDIRECT_CTX buffer and by enabling back the arbitration by programming MI_ARB_ON_OFF to "Arbitration Enable" as the last command prior to MI_BATCH_END in the BB_PER_CTX_PTR buffer of every context submitted. Note that RCS_INDIRECT_CTX_OFFSET could be set to default value or any other legitimate value as per the programming notes of the register definition. Arbitration disable by programming MI_ARB_ON_OFF (Arbitration Disabled) in RCS_INDIRECT_CTX buffer. Arbitration enabled by programming MI_ARB_ON_OFF (Arbitration Enabled) as the last command prior to MI_BATCH_BUFFER_END in BB_PER_CTX_PTR buffer. Additional Note: This WA need not be applied when it is guaranteed for no preemption to occur during execution of GPGPU workload. Preemption of GPGPU workload can be avoided by Bracketing the GPGPU workload with MI_ARB_ON_OFF (Arbitration Disable) and MI_ARB_ON_OFF (Arbitration Enable) command. MI_ARB_ON_OFF is a privileged command and can only be programmed in ring buffer or in privileged batch buffer (batch buffer in GGTT memory). Pending execlist submitted must not trigger preemption of the ongoing GPGPU workload due to following reasons First context of the pending execlist submitted is not the same as the ongoing GPGPU context. Force restore bit set for the submitted pending execlist.	
Workaround:On BXT “RS enabled Batch Buffer Per Context” can be programmed with MI_SEMAPHORE_WAIT command in register poll mode. Resource streamer stops executing the “RS enabled Batch Buffer Per Context” on encountering MI_SEMAPHORE_WAIT command. SW must ensure all the commands meant to be executed by Resource Streamer from “RS enabled Batch Buffer Per Context” must be programmed prior to programming the MI_SEMAPHORE_WAIT	RenderCS

BB_PER_CTX_PTR - Batch Buffer Per Context Pointer

command.

DWord	Bit	Description
0	31:12	**Batch Buffer Per Context Address** Format: U20 Pointer to the Context in memory to be executed as a batch.
	11:3	**Reserved** Format: MBZ
	2	**Reserved**
	1	**RS Enabled Batch Buffer Per Context** Format: U1 If set, the command stream will enable the RS to parse commands. **Programming Notes** This must be set when programming the resource streamer pool commands (3DSTATE_BINDING_TABLE_POOL_ALLOC, 3DSTATE_GATHER_POOL_ALLOC, and 3DSTATE_DX9_CONSTANT_BUFFER_POOL_ALLOC) in order for the pool alloc fields to be valid in both the render engine and resource streamer.
	0	**Batch Buffer Per Context Valid** Format: U1 If set, the command stream will execute the context from the **Batch Buffer Per Context Address** prior to the execution of actual submitted workloads.

BLC_PWM_CTL

BLC_PWM_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	C8250h-C8253h
Name:	Backlight 1 PWM Control
ShortName:	BLC_PWM_CTL_1
Power:	PG0
Reset:	soft
Address:	C8350h-C8353h
Name:	Backlight 2 PWM Control
ShortName:	BLC_PWM_CTL_2
Power:	PG0
Reset:	soft

DWord	Bit	Description
0	31	**PWM Enable** This bit enables the PWM. A disabled PWM will drive 0, which can be inverted to 1 with the polarity control. Value: 0b = Disable; 1b = Enable
	30	**Reserved** Format: MBZ
	29	**PWM Polarity** This field controls the polarity of the PWM signal. Value: 0b = Active High; 1b = Active Low
	28:0	**Reserved** Format: MBZ

BLC_PWM_DUTY

BLC_PWM_DUTY	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	C8258h-C825Bh
Name:	Backlight 1 PWM Duty Cycle
ShortName:	BLC_PWM_DUTY_1
Power:	PG0
Reset:	soft
Address:	C8358h-C835Bh
Name:	Backlight 2 PWM Duty Cycle
ShortName:	BLC_PWM_DUTY_2
Power:	PG0
Reset:	soft

DWord	Bit	Description
0	31:0	**Duty Cycle** This field controls the active portion of the backlight PWM duty cycle. The value should be programmed to (BLC_PWM_FREQ Frequency * desired duty cycle percentage / 100). A value of zero will give a 0% active duty cycle. A value equal to BLC_PWM_FREQ Frequency will give a 100% active duty cycle. When written, the new value will take affect at the end of the current PWM cycle. **Restriction** Restriction: This should never be larger than BLC_PWM_FREQ Frequency.

BLC_PWM_FREQ

BLC_PWM_FREQ		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	C8254h-C8257h	
Name:	Backlight 1 PWM Frequency	
ShortName:	BLC_PWM_FREQ_1	
Power:	PG0	
Reset:	soft	
Address:	C8354h-C8357h	
Name:	Backlight 2 PWM Frequency	
ShortName:	BLC_PWM_FREQ_2	
Power:	PG0	
Reset:	soft	
DWord	**Bit**	**Description**
0	31:0	**Frequency** This field controls the backlight PWM frequency. The value should be programmed to (PWM clock frequency / desired PWM frequency). The Backlight page gives the PWM clock frequency.

Blitter MOCS Register0

BLT_MOCS_0 - Blitter MOCS Register0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030
Size (in bits):	32
Address:	0CC00h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_0 - Blitter MOCS Register0

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register1

BLT_MOCS_1 - Blitter MOCS Register1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034
Size (in bits):	32
Address:	0CC04h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_1 - Blitter MOCS Register1

7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register2

BLT_MOCS_2 - Blitter MOCS Register2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038
Size (in bits):	32
Address:	0CC08h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_2 - Blitter MOCS Register2

7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register3

BLT_MOCS_3 - Blitter MOCS Register3

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031
Size (in bits):	32
Address:	0CC0Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_3 - Blitter MOCS Register3

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register4

BLT_MOCS_4 - Blitter MOCS Register4

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CC10h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_4 - Blitter MOCS Register4

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register5

BLT_MOCS_5 - Blitter MOCS Register5

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CC14h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_5 - Blitter MOCS Register5

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register6

BLT_MOCS_6 - Blitter MOCS Register6

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CC18h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_6 - Blitter MOCS Register6

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register7

LT_MOCS_7 - Blitter MOCS Register7

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CC1Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

LT_MOCS_7 - Blitter MOCS Register7

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register8

BLT_MOCS_8 - Blitter MOCS Register8

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CC20h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_8 - Blitter MOCS Register8

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register9

BLT_MOCS_9 - Blitter MOCS Register9

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CC24h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_9 - Blitter MOCS Register9

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register10

BLT_MOCS_10 - Blitter MOCS Register10

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CC28h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_10 - Blitter MOCS Register10

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register11

BLT_MOCS_11 - Blitter MOCS Register11

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CC2Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_11 - Blitter MOCS Register11

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register12

BLT_MOCS_12 - Blitter MOCS Register12

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CC30h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_12 - Blitter MOCS Register12

7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register13

BLT_MOCS_13 - Blitter MOCS Register13

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CC34h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_13 - Blitter MOCS Register13

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register14

BLT_MOCS_14 - Blitter MOCS Register14

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CC38h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_14 - Blitter MOCS Register14

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register15

BLT_MOCS_15 - Blitter MOCS Register15

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CC3Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_15 - Blitter MOCS Register15

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register16

BLT_MOCS_16 - Blitter MOCS Register16

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030
Size (in bits):	32
Address:	0CC40h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_16 - Blitter MOCS Register16

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register17

BLT_MOCS_17 - Blitter MOCS Register17

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034
Size (in bits):	32
Address:	0CC44h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_17 - Blitter MOCS Register17

7 — Enable Skip Caching

Default Value:	0b
Access:	R/W

Enable for the Skip cache mechanism
0: Not enabled
1: Enabled for LLC

6 — Dont allocate on miss

Default Value:	0b
Access:	R/W

Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM).
0: Allocate on MISS (normal cache behavior)
1: Do NOT allocate on MISS

5:4 — LRU management

Default Value:	11b
Access:	R/W

This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches.
11: Good chance of generating hits.
10: Poor chance of generating hits
01: Don't change the LRU if it is a HIT
00: Reserved

3:2 — Target Cache

Default Value:	01b
Access:	R/W

This field allows the choice of LLC vs eLLC for caching
00: eLLC Only
01: LLC Only
10: LLC/eLLC Allowed
11: LLC/eLLC Allowed

1:0 — LLC/eDRAM cacheability control

Default Value:	00b
Access:	R/W

Memory type information used in LLC/eDRAM.
00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)
01: Uncacheable (UC) - non-cacheable
10: Writethrough (WT)
11: Writeback (WB)

Blitter MOCS Register18

BLT_MOCS_18 - Blitter MOCS Register18

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038
Size (in bits):	32
Address:	0CC48h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_18 - Blitter MOCS Register18

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register19

BLT_MOCS_19 - Blitter MOCS Register19

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031
Size (in bits):	32
Address:	0CC4Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_19 - Blitter MOCS Register19

7 — Enable Skip Caching

Default Value:	0b
Access:	R/W

Enable for the Skip cache mechanism
0: Not enabled
1: Enabled for LLC

6 — Dont allocate on miss

Default Value:	0b
Access:	R/W

Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM).
0: Allocate on MISS (normal cache behavior)
1: Do NOT allocate on MISS

5:4 — LRU management

Default Value:	11b
Access:	R/W

This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches.
11: Good chance of generating hits.
10: Poor chance of generating hits
01: Don't change the LRU if it is a HIT
00: Reserved

3:2 — Target Cache

Default Value:	00b
Access:	R/W

This field allows the choice of LLC vs eLLC for caching
00: eLLC Only
01: LLC Only
10: LLC/eLLC Allowed
11: LLC/eLLC Allowed

1:0 — LLC/eDRAM cacheability control

Default Value:	01b
Access:	R/W

Memory type information used in LLC/eDRAM.
00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)
01: Uncacheable (UC) - non-cacheable
10: Writethrough (WT)
11: Writeback (WB)

Blitter MOCS Register20

BLT_MOCS_20 - Blitter MOCS Register20

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CC50h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_20 - Blitter MOCS Register20

7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register21

BLT_MOCS_21 - Blitter MOCS Register21

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CC54h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_21 - Blitter MOCS Register21

7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register22

BLT_MOCS_22 - Blitter MOCS Register22

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CC58h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_22 - Blitter MOCS Register22

7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register23

BLT_MOCS_23 - Blitter MOCS Register23

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CC5Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_23 - Blitter MOCS Register23

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register24

BLT_MOCS_24 - Blitter MOCS Register24

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CC60h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_24 - Blitter MOCS Register24

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register25

BLT_MOCS_25 - Blitter MOCS Register25

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CC64h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_25 - Blitter MOCS Register25

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register26

BLT_MOCS_26 - Blitter MOCS Register26

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CC68h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_26 - Blitter MOCS Register26

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register27

BLT_MOCS_27 - Blitter MOCS Register27

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CC6Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_27 - Blitter MOCS Register27

7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register28

BLT_MOCS_28 - Blitter MOCS Register28

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CC70h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_28 - Blitter MOCS Register28

7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register29

BLT_MOCS_29 - Blitter MOCS Register29

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CC74h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_29 - Blitter MOCS Register29

7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register30

BLT_MOCS_30 - Blitter MOCS Register30

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CC78h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_30 - Blitter MOCS Register30

7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register31

BLT_MOCS_31 - Blitter MOCS Register31

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CC7Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_31 - Blitter MOCS Register31

7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register32

BLT_MOCS_32 - Blitter MOCS Register32

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030
Size (in bits):	32
Address:	0CC80h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_32 - Blitter MOCS Register32

7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register33

BLT_MOCS_33 - Blitter MOCS Register33

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034
Size (in bits):	32
Address:	0CC84h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_33 - Blitter MOCS Register33

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register34

BLT_MOCS_34 - Blitter MOCS Register34

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038
Size (in bits):	32
Address:	0CC88h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_34 - Blitter MOCS Register34

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register35

BLT_MOCS_35 - Blitter MOCS Register35

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031
Size (in bits):	32
Address:	0CC8Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_35 - Blitter MOCS Register35

7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register36

BLT_MOCS_36 - Blitter MOCS Register36

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CC90h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_36 - Blitter MOCS Register36

7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register37

BLT_MOCS_37 - Blitter MOCS Register37

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CC94h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_37 - Blitter MOCS Register37

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register38

BLT_MOCS_38 - Blitter MOCS Register38

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CC98h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_38 - Blitter MOCS Register38

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register39

BLT_MOCS_39 - Blitter MOCS Register39

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CC9Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_39 - Blitter MOCS Register39

7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register40

BLT_MOCS_40 - Blitter MOCS Register40

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CCA0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_40 - Blitter MOCS Register40

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register41

BLT_MOCS_41 - Blitter MOCS Register41

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CCA4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_41 - Blitter MOCS Register41

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register42

BLT_MOCS_42 - Blitter MOCS Register42

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CCA8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_42 - Blitter MOCS Register42

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register43

BLT_MOCS_43 - Blitter MOCS Register43

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CCACh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_43 - Blitter MOCS Register43

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register44

BLT_MOCS_44 - Blitter MOCS Register44

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CCB0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_44 - Blitter MOCS Register44

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register45

BLT_MOCS_45 - Blitter MOCS Register45

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CCB4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_45 - Blitter MOCS Register45

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register46

BLT_MOCS_46 - Blitter MOCS Register46

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CCB8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_46 - Blitter MOCS Register46

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register47

BLT_MOCS_47 - Blitter MOCS Register47

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CCBCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_47 - Blitter MOCS Register47

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register48

BLT_MOCS_48 - Blitter MOCS Register48

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030
Size (in bits):	32
Address:	0CCC0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_48 - Blitter MOCS Register48

7 — Enable Skip Caching

Default Value:	0b
Access:	R/W

Enable for the Skip cache mechanism
0: Not enabled
1: Enabled for LLC

6 — Dont allocate on miss

Default Value:	0b
Access:	R/W

Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM).
0: Allocate on MISS (normal cache behavior)
1: Do NOT allocate on MISS

5:4 — LRU management

Default Value:	11b
Access:	R/W

This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches.
11: Good chance of generating hits.
10: Poor chance of generating hits
01: Don't change the LRU if it is a HIT
00: Reserved

3:2 — Target Cache

Default Value:	00b
Access:	R/W

This field allows the choice of LLC vs eLLC for caching
00: eLLC Only
01: LLC Only
10: LLC/eLLC Allowed
11: LLC/eLLC Allowed

1:0 — LLC/eDRAM cacheability control

Default Value:	00b
Access:	R/W

Memory type information used in LLC/eDRAM.
00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)
01: Uncacheable (UC) - non-cacheable
10: Writethrough (WT)
11: Writeback (WB)

Blitter MOCS Register49

BLT_MOCS_49 - Blitter MOCS Register49

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034
Size (in bits):	32
Address:	0CCC4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_49 - Blitter MOCS Register49

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register50

BLT_MOCS_50 - Blitter MOCS Register50

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038
Size (in bits):	32
Address:	0CCC8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_50 - Blitter MOCS Register50

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register51

BLT_MOCS_51 - Blitter MOCS Register51

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031
Size (in bits):	32
Address:	0CCCCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_51 - Blitter MOCS Register51

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register52

BLT_MOCS_52 - Blitter MOCS Register52

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CCD0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_52 - Blitter MOCS Register52

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register53

BLT_MOCS_53 - Blitter MOCS Register53

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CCD4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_53 - Blitter MOCS Register53

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register54

BLT_MOCS_54 - Blitter MOCS Register54

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CCD8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_54 - Blitter MOCS Register54

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register55

BLT_MOCS_55 - Blitter MOCS Register55

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CCDCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_55 - Blitter MOCS Register55

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register56

BLT_MOCS_56 - Blitter MOCS Register56

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CCE0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_56 - Blitter MOCS Register56

7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register57

BLT_MOCS_57 - Blitter MOCS Register57

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CCE4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_57 - Blitter MOCS Register57

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register58

BLT_MOCS_58 - Blitter MOCS Register58

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CCE8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_58 - Blitter MOCS Register58

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register59

BLT_MOCS_59 - Blitter MOCS Register59

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CCECh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_59 - Blitter MOCS Register59

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register60

BLT_MOCS_60 - Blitter MOCS Register60

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CCF0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_60 - Blitter MOCS Register60

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register61

BLT_MOCS_61 - Blitter MOCS Register61

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CCF4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_61 - Blitter MOCS Register61

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register62

BLT_MOCS_62 - Blitter MOCS Register62

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CCF8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_62 - Blitter MOCS Register62

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Blitter MOCS Register63

BLT_MOCS_63 - Blitter MOCS Register63

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CCFCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

BLT_MOCS_63 - Blitter MOCS Register63

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Built In Self Test

BIST_0_2_0_PCI - Built In Self Test			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	8		
Address:	0000Fh		
This register is used for control and status of Built In Self Test (BIST).			
DWord	**Bit**	**Description**	
0	7	**BIST Supported**	
		Default Value:	0b
		Access:	RO
		BIST is not supported. This bit is hardwired to 0.	
	6:0	**Reserved**	
		Default Value:	0000000b
		Access:	RO
		Reserved	

Cache Line Size

CLS_0_2_0_PCI - Cache Line Size		
Register Space:	PCI: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	8	
Address:	0000Ch	
DWord	**Bit**	**Description**
0	7:0	**Cache Line Size Value** Default Value: 00000000b Access: R/W This field is implemented by PCI Express devices as a read-write field for legacy compatibility purposes but has no effect on any PCI Express device behavior.

Capabilities Control

CAPCTRL0_0_2_0_PCI - Capabilities Control

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x0000010C
Size (in bits):	16
Address:	00042h

DWord	Bit	Description
0	15:12	**Reserved** Default Value: 0000000b Access: RO Reserved
	11:8	**CAPID Version** Default Value: 0001b Access: RO This field is hardwired to the value 1h to identify the first revision of the CAPID register definition.
	7:0	**CAPID Length** Default Value: 00001100b Access: RO This field is hardwired to the value 0Ch to indicate the structure length (12 bytes).

Capabilities Pointer

CAPPOINT_0_2_0_PCI - Capabilities Pointer

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000040
Size (in bits):	8
Address:	00034h

This register points to a linked list of capabilities implemented by this device.

DWord	Bit	Description
0	7:0	**Capabilities Pointer Value** Default Value: 01000000b Access: RO This field contains an offset into the function's PCI Configuration Space for the first item in the New Capabilities Linked List, the CAPID0 register at offset 40h.

Capability Identifier

CAPID0_0_2_0_PCI - Capability Identifier

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00007009
Size (in bits):	16
Address:	00040h

DWord	Bit	Description
0	15:8	**Next Capability Pointer** Default Value: 01110000b Access: RO This field is hardwired to point to the next PCI Capability structure, the PCIe Capabilities structure at 70h.
	7:0	**Capability Identifier** Default Value: 00001001b Access: RO This field is hardwired to the value 09h to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.

CDCLK_CTL

CDCLK_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x000002A1
Access:	R/W
Size (in bits):	32
Address:	46000h-46003h
Name:	CD Clock Control
ShortName:	CDCLK_CTL
Power:	PG0
Reset:	global

This register is not reset by the device 2 FLR.

Restriction

Restriction : These fields should only be changed as part of the Display Sequences for Changing CD Clock Frequency.

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:22	**DE CD2X Divider Select** Access: Double Buffered Double Buffer Update Point: Pipe off or start of vertical blank This field selects how the DE PLL CD2X clock output is divided before driving the display CD2X clock. This field is double buffered to align with the pipe from DE CD2X Pipe Select. It will update at the start of vertical blank of the selected pipe, or immediately if the selected pipe is disabled or no pipe is selected.

Value	Name	Description
00b	Divide by 1	If DE PLL output is 1248 MHz: CD2X 1248 MHz, CD 624 MHz. If DE PLL output is 1152 MHz: CD2X 1152 MHz, CD 576 MHz. DE PLL CD2X output must be configured to 1152 MHz or 1248 MHz when using this divider.
01b	Divide by 1.5	CD2X 768 MHz, CD 384 MHz DE PLL CD2X output must be configured to 1152 MHz when using this divider.
10b	Divide by 2	CD2X 576 MHz, CD 288 MHz DE PLL CD2X output must be configured to 1152 MHz when using this divider.

CDCLK_CTL

11b	Divide by 4	CD2X 288 MHz, CD 144 MHz DE PLL CD2X output must be configured to 1152 MHz when using this divider.

Restriction
Restriction : DE CD2X Divider Select must not be changed while more than one pipe is enabled. When one pipe is enabled, the DE CD2X Pipe Select must be set to that pipe before changing DE CD2X Divider Select.

21:20 **DE CD2X Pipe Select**

This field selects the pipe enable and vertical blank to be used for double buffering the DE CD2X Divider Select and SSA Precharge Enable.

Value	Name	Description
00b	Pipe A	
01b	Pipe B	
10b	Pipe C	
11b	None	Double buffer enable is tied to 1 so that writes to the DE CD2X Divider Select and SSA Precharge Enable will take effect immediately.

19 **Reserved**

18 **Reserved**

17 **Reserved**

Format:	MBZ

16 **SSA Precharge Enable**

Access:	Double Buffered
Double Buffer Update Point:	Pipe off or start of vertical blank

This field enables the Low Speed Small Signal Array Pre-charge.
This field is double buffered to align with the pipe from DE CD2X Pipe Select. It will update at the start of vertical blank of the selected pipe, or immediately if the selected pipe is disabled or no pipe is selected.

Value	Name
0b	Disable
1b	Enable

Restriction

CDCLK_CTL

Restriction :
This field must be disabled when CD clock frequency is < 500 MHz and enabled when CD clock frequency is >= 500 MHz.
This field must not be changed while more than one pipe is enabled. When one pipe is enabled, the DE CD2X Pipe Select must be set to that pipe before changing DE CD2X Divider Select.

15:11 Reserved

Format:	MBZ

10:0 CD Frequency Decimal

Format:	U10.1

This field selects the decimal value of the frequency for CD clock, which is used to generate divided down clocks for some display engine timers.
This value is represented in a 10.1 format with 10 integer bits and 1 fractional bit.

Program this field to select the pre-defined value that matches the CD frequency chosen by the DE PLL and CD2X Divider. If no value is defined, program this field with the CD frequency, rounded to the closest 0.5, then minus one.

Value	Name
00 1000 1111 0b	144 MHz CD
01 0001 1111 0b	288 MHz CD
01 0111 1111 0b	384 MHz CD
10 0011 1111 0b	576 MHz CD
10 0110 1111 0b	624 MHz CD
01 0101 0000 1b	337.5 MHz CD **[Default]**

Class Code

CC_0_2_0_PCI - Class Code

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00030000
Size (in bits):	24
Address:	00009h

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

DWord	Bit	Description
0	23:16	**Base Class Code** Default Value: 00000011b Access: RO Variant This is an 8-bit value that indicates the base class code. When MGGC0[VAMEN] is 0 this code has the value 03h, indicating a Display Controller. When MGGC0[VAMEN] is 1 this code has the value 04h, indicating a Multimedia Device.
	15:8	**Sub-Class Code** Default Value: 00000000b Access: RO Variant When MGGC0[VAMEN] is 0 this value will be determined based on Device 0 GGC register, GMS and IVD fields. 00h: VGA compatible 80h: Non VGA (GMS = "00h" or IVD = "1b") When MGGC0[VAMEN] is 1, this value is 80h, indicating other multimedia device.
	7:0	**Programming Interface** Default Value: 00000000b Access: RO When MGGC0[VAMEN] is 0 this value is 00h, indicating a Display Controller. When MGGC0[VAMEN] is 1 this value is 00h, indicating a NOP.

Configuration Register1 for RPMunit

CONFIG1 - Configuration Register1 for RPMunit

Register Space:	MMIO: 0/2/0
Default Value:	0x0000001E
Size (in bits):	32
Address:	00D04h

Lock bit LOCK applies to all RW/L fields in this register. Lock is overridden during context restore.

DWord	Bit	Description
0	31	**Lock for RW/L Fields in this Register** Access: R/W Lock 0 = Bits of CONFIG0 register are R/W. 1 = All bits of CONFIG0 register are RO (including this lock bit). Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). Lock is reset on a restore after context is captured.
	30:9	**Placeholder Bits BF** Access: R/W Lock Placeholder bits for implementation or ECO loops.
	8:0	**RCP L3 FREQ DETECT** Default Value: 000011110b Access: R/W Lock This is control signal needed from clock unit that can be set at 1 when 2X clock frequency is less than or equal to 1GHz. It needs to be at 0 when 2X clock frequency is >1GHz. Without this circuit changes, the GT L3 cache will not be functional at lower frequency due to Vcc is less than Vccmin of 0.9V for the array. default value: low2xthresh=0x01Eh corresponding to a 1x frequency of 500Mhz.

DC_STATE_EN

DC_STATE_EN	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	45504h-45507h
Name:	Display C State Enable
ShortName:	DC_STATE_EN
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:10	**Reserved**
	9	**In CSR Flow** Value / Name: 0b – Not In CSR 1b – In CSR Restriction : This field is used for hardware communication. Software must not change this field.
	8	**Block Outbound Traffic** Access is read/write, but hardware can also clear the value based on the PM Request. Value / Name: 0b – Do Not Block 1b – Block Restriction : This field is used for hardware communication. Software must not change this field.
	7:5	**Reserved**

DC_STATE_EN

	4	**Mask Poke** This field masks the poke signal that would otherwise be generated by a write to the DC_STATE_SEL register. **Value** / **Name** 0b – Unmask 1b – Mask **Restriction** Restriction : This field is used for hardware communication. Software must not change this field.
	3	**DC9 Allow** This field indicates software allows Display C9. When allowed, the PCU can save the display PCI Config context and power down display **Value** / **Name** 0b – Do not allow 1b – Allow
	2	**Reserved**
	1:0	**Dynamic DC State Enable** This field enables hardware to dynamically enter and exit Display C states. **Value** / **Name** 00b – Disable 01b – Enable up to DC5 10b – Enable up to DC6 **Restriction** Restriction : The Display CSR code must be loaded before this field is enabled.

DDI_BUF_CTL

DDI_BUF_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	64000h-64003h
Name:	DDI A Buffer Control
ShortName:	DDI_BUF_CTL_A
Power:	PG1
Reset:	soft
Address:	64100h-64103h
Name:	DDI B Buffer Control
ShortName:	DDI_BUF_CTL_B
Power:	PG1
Reset:	soft
Address:	64200h-64203h
Name:	DDI C Buffer Control
ShortName:	DDI_BUF_CTL_C
Power:	PG1
Reset:	soft
Address:	64300h-64303h
Name:	DDI D Buffer Control
ShortName:	DDI_BUF_CTL_D
Power:	PG1
Reset:	soft
Address:	64400h-64403h
Name:	DDI E Buffer Control
ShortName:	DDI_BUF_CTL_E
Power:	PG1
Reset:	soft

Do not read or write the register when the associated power well is disabled.

DWord	Bit	Description
0	31	**DDI Buffer Enable** This bit enables the DDI buffer.

DDI_BUF_CTL

Value	Name
0b	Disable
1b	Enable

30 **Reserved**

Format:	MBZ

29:28 **Reserved**

27:24 **DP Vswing Emp Sel**

Description
This field is ignored on Broxton. Voltage swing and emphasis programming is done through the PHY registers.
These bits are used to select the voltage swing and emphasis for DisplayPort.
This field is ignored for HDMI and DVI. The values programmed in DDI_BUF_TRANS determine the voltage swing and emphasis for each selection.

Value	Name	Description
0000b-1000b	Select 0 - Select 8	Select from buffer translations 0 through 8. Valid with all DDIs.
1001b	Select 9	Select buffer translation 9. Valid only with DDIA and DDIE.

23:17 **Reserved**

Format:	MBZ

16 **Port Reversal**

This field enables lane reversal within the port. Lane reversal swaps the data on the lanes as they are output from the port.

Value	Name
0b	Not reversed
1b	Reversed

Programming Notes
DDI B, C, D, and F reversal always swaps the four lanes, so lane 0 is swapped with lane 3, and lane 1 is swapped with lane 2. If DDIA Lane Capability Control selects DDIA x2, then DDI A reversal swaps the two lanes, so lane 0 is swapped with lane 1. If DDIA Lane Capability Control selects DDIA x4, then DDI A reversal swaps the four lanes, so lane 0 is swapped with lane 3, and lane 1 is swapped with lane 2.

Restriction
Restriction : This field must not be changed while the DDI is enabled. DDI E does not support reversal.

DDI_BUF_CTL

15:8 Reserved

Format:	MBZ

7 DDI Idle Status

Access:	RO

This bit indicates when the DDI buffer is idle.

Value	Name
0b	Buffer Not Idle
1b	Buffer Idle

Restriction
Restriction : On BXT this status can be incorrect. Follow the fixed delay in the mode set sequence instead of using this field.

6:5 Reserved

Format:	MBZ

4 DDIA Lane Capability Control

This bit selects how lanes are shared between DDI A and DDI E.
This field is only used in the DDI A instance of this register.
See the DDI A and DDI E lane mapping table in the Introduction section.

Value	Name	Description	Programming Notes
0b	DDIA x2	DDI A supports 2 lanes and DDI E supports 2 lanes	Restriction : Not supported on Broxton.
1b	DDIA x4	DDI A supports 4 lanes and DDI E is not used	

Restriction
Restriction : This field must be programmed at system boot based on board configuration and may not be changed afterwards.

3:1 DP Port Width Selection

Description
This bit selects the number of lanes to be enabled on the DDI link for DisplayPort.

Value	Name	Description
000b	x1	x1 Mode
001b	x2	x2 Mode
011b	x4	x4 Mode Not allowed with DDI E, some restrictions with DDI A
Others	Reserved	Reserved

Programming Notes

DDI_BUF_CTL

DDI E only supports x1 and x2 when DDI_BUF_CTL_A DDIA Lane Capability Control is set to DDIA x2, otherwise DDI E is not supported. DDI A (EDP) supports x1, x2, and x4 when DDI_BUF_CTL_A DDIA Lane Capability Control is set to DDIA x4, otherwise DDI A only supports x1 and x2.

Restriction
Restriction : When in DisplayPort mode the value selected here must match the value selected in TRANS_DDI_FUNC_CTL attached to this DDI.
Restriction : This field must not be changed while the DDI is enabled.

0 **Init Display Detected**

Access:	RO

Description
Strap indicating whether a display was detected on this port during initialization. It signifies the level of the port detect pin at boot. This bit is only informative. It does not prevent this port from being enabled in hardware. This field only indicates the DDIA detection. Detection for other ports is read from SFUSE_STRAP.
There are no port presence straps on Broxton. Software should use alternate means to determine port presence.

Value	Name	Description
0b	Not Detected	Digital display not detected during initialization
1b	Detected	Digital display detected during initialization

DE_PIPE_INTERRUPT

DE_PIPE_INTERRUPT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	44400h-4440Fh
Name:	Display Engine Pipe A Interrupts
ShortName:	DE_PIPE_INTERRUPT_A
Power:	PG1
Reset:	soft
Address:	44410h-4441Fh
Name:	Display Engine Pipe B Interrupts
ShortName:	DE_PIPE_INTERRUPT_B
Power:	PG2
Reset:	soft
Address:	44420h-4442Fh
Name:	Display Engine Pipe C Interrupts
ShortName:	DE_PIPE_INTERRUPT_C
Power:	PG2
Reset:	soft

Description

This table indicates which events are mapped to each bit of the Display Engine Pipe Interrupt registers.
The IER enabled Display Engine Pipe Interrupt IIR (sticky) bits are ORed together to generate the DE_Pipe Interrupts Pending bit in the Master Interrupt Control register.
There is one full set of Display Engine Pipe interrupts per display pipes A/B/C.
The STEREO3D_EVENT_MASK selects between left eye and right eye reporting of vertical blank, vertical sync, and scanline events in stereo 3D modes.

0x44400 = ISR A, 0x44410 = ISR B, 0x44420 = ISR C
0x44404 = IMR A, 0x44414 = IMR B, 0x44424 = IMR C
0x44408 = IIR A, 0x44418 = IIR B, 0x44428 = IIR C
0x4440C = IER A, 0x4441C = IER B, 0x4442C = IER C

DWord	Bit	Description
0	31	**Underrun** The ISR is an active high pulse when there is an underrun on the transcoder attached to this pipe.
	30	**Unused_Int_30** These interrupts are currently unused.

DE_PIPE_INTERRUPT		
	29	**Reserved**
	28	**Reserved**
	27:20	**Unused_Int_27_20** These interrupts are currently unused.
	19	**Reserved**
	18	**Reserved**
	17	**Reserved**
	16	**Reserved**
	15:13	**Unused_Int_15_13** These interrupts are currently unused.
	12	**DPST_Histogram_event** The ISR is an active high pulse on the DPST Histogram event on this pipe.
	11	**Cursor_GTT_Fault_Status** The ISR is an active high pulse when a GTT fault is detected for the cursor on this pipe.
	10	**Plane4_GTT_Fault_Status** **Description** The ISR is an active high pulse when a GTT fault is detected for plane 4 on this pipe. Not all pipes a have plane 4.
	9	**Plane3_GTT_Fault_Status** **Description** The ISR is an active high pulse when a GTT fault is detected for plane 3 on this pipe. Not all pipes a have plane 3.
	8	**Plane2_GTT_Fault_Status** The ISR is an active high pulse when a GTT fault is detected for plane 2 on this pipe.
	7	**Plane1_GTT_Fault_Status** The ISR is an active high pulse when a GTT fault is detected for plane 1 on this pipe.
	6	**Plane4_Flip_Done** **Description** The ISR is an active high pulse when the flip is done for plane 4 on this pipe. Not all pipes have a plane 4.
	5	**Plane3_Flip_Done** **Description** The ISR is an active high pulse when the flip is done for plane 3 on this pipe. Not all pipes have a plane 3.
	4	**Plane2_Flip_Done** The ISR is an active high pulse when the flip is done for plane 2 on this pipe.

DE_PIPE_INTERRUPT		
	3	**Plane1_Flip_Done** The ISR is an active high pulse when the flip is done for plane 1 on this pipe.
	2	**Scan_Line_Event** The ISR is an active high pulse on the scan line event of the transcoder attached to this pipe. **Restriction** Restriction : Not supported with MIPI DSI.
	1	**Vsync** The ISR is an active high level for the duration of the vertical sync of the transcoder attached to this pipe. **Restriction** Restriction : Not supported with MIPI DSI.
	0	**Vblank** The ISR is an active high level for the duration of the vertical blank of the transcoder attached to this pipe.

DE_PLL_CTL

DE_PLL_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000064
Access:	R/W
Size (in bits):	32

Address:	6D000h-6D003h
Name:	DE PLL Control
ShortName:	DE_PLL_CTL
Power:	PG0
Reset:	global

The register is used to control the frequency of the outputs from the DE PLL.
The DE_PLL_ENABLE register controls the PLL enable.

Restriction
Restriction : The fields must not be changed while the PLL is enabled.

DWord	Bit	Description
0	31:25	**Reserved** Format: MBZ
	24:18	**Output Ratio** Set the output clock ratio. Restriction : Display software must not change this field.
	17:16	**PVD Ratio** Set the post VCO divider ratio. 00b: 1 01b: 2 10b: 4 11b: 8 Restriction : Display software must not change this field.
	15:14	**Ref Ratio** Set the refclk ratio. 00b: Ref

DE_PLL_CTL

		01b: Ref/2 10b: Ref/4 11b: Ref/8 **Restriction** Restriction : Display software must not change this field.
	13	**Force On** Force the PLL on. 0b: No Force 1b: Force On **Restriction** Restriction : Display software must not change this field.
	12	**Force Off** Force the PLL off. 0b: No Force 1b: Force Off **Restriction** Restriction : Display software must not change this field.
	11:10	**Freq Sel C** Frequency Select for DSI C clock 00b: 16X: Non DSI **Restriction** Restriction : Display software must not change this field.
	9:8	**Freq Sel A** Frequency Select for DSI A clock 00b: 16X: Non DSI **Restriction** Restriction : Display software must not change this field.

DE_PLL_CTL

	7:0	**PLL Ratio**

Value	Name	Description
3Ch	60	DE PLL 1152 MHz before post divider
41h	65	DE PLL 1248 MHz before post divider
21h	33	DE PLL 633.6 MHz before post divider
64h	100 **[Default]**	
Others	Reserved	

DE_PLL_ENABLE

DE_PLL_ENABLE

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	46070h-46073h
Name:	DE PLL Enable
ShortName:	DE_PLL_ENABLE
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31	**PLL Enable** This field enables or disables the DE PLL. Value / Name: 0b – Disable 1b – Enable
	30	**PLL Lock** Access: RO This fields indicates the status of the DE PLL Lock. Value / Name: 0b – Not locked or not enabled 1b – Locked
	29:0	**Reserved** Format: MBZ

DE Misc Interrupt Definition

DE Misc Interrupt Definition	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	44460h-4446Fh
Name:	Display Engine Miscellaneous Interrupts
ShortName:	DE_MISC_INTERRUPT
Power:	PG0
Reset:	soft

This table indicates which events are mapped to each bit of the Display Engine Miscellaneous Interrupt registers.
0x44460 = ISR
0x44464 = IMR
0x44468 = IIR
0x4446C = IER

DWord	Bit	Description
0	31	**Poison** The ISR is an active high pulse on receiving the poison response to a memory transaction.
	30	**ECC_Double_Error** The ISR is an active high level while any of the ECC Double Error status bits are set.
	29	**Invalid_GTT_page_table_entry** The ISR is an active high pulse on receiving the iMPH invalid GTT page table entry indication.
	28	**Invalid_page_table_entry_data** Description The ISR is an active high pulse on receiving the iMPH invalid page table entry data indication. This interrupt is not supported.
	27	**GSE** The ISR is an active high pulse on the GSE system level event.
	26	**Camera Interrupt Event** This interrupt is not supported.
	25	**Reserved**
	24	**Reserved**
	23	**WD0_Interrupts_Combined** The ISR is an active high level while any of the WD0_IIR bits are set.
	22	**SVM Device Mode PRQ Event** The ISR is an active high pulse on receiving the iMPH SVM Device Mode PRQ event indication. This event indicates that a GT advanced context encountered a recoverable page fault.

DE Misc Interrupt Definition

	21	**SVM Device Mode VTD Fault** The ISR is an active high pulse on receiving the iMPH SVM Device Mode VT-d fault indication. This event indicates GT encountered a non-recoverable translation fault.
	20	**SVM Device Mode Wait Descriptor Completion** The ISR is an active high pulse on receiving the iMPH SVM Device Mode Wait Descriptor Completion indication. This event indicates that IMPH completed Invalidation Wait Descriptor.
	19	**SRD_Interrupts_Combined** The ISR is an active high level while any of the SRD_IIR bits are set.
	18	**Reserved** Format: MBZ
	17:16	**Reserved** Format: MBZ
	15	**GTC_Interrupts_Combined** The ISR is an active high level while any of the GTC_IIR bits are set.
	14:9	**Reserved** Format: MBZ
	8	**Reserved** Format: MBZ
	7:4	**Reserved** Format: MBZ
	3:1	**Reserved** Format: MBZ
	0	**Reserved** Format: MBZ

DE Port Interrupt Definition

DE Port Interrupt Definition	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	44440h-4444Fh
Name:	Display Engine Port Interrupts
ShortName:	DE_PORT_INTERRUPT
Power:	PG0
Reset:	soft

This table indicates which events are mapped to each bit of the Display Engine Port Interrupt registers.
0x44440 = ISR
0x44444 = IMR
0x44448 = IIR
0x4444C = IER

DWord	Bit	Description
0	31	**MIPI C** The ISR is an active high level indicating an interrupt is set in MIPIC_INTR_STAT_REG or MIPIC_INTR_STAT_REG_1.
	30	**MIPI A** The ISR is an active high level indicating an interrupt is set in MIPIA_INTR_STAT_REG or MIPIA_INTR_STAT_REG_1.
	29	**Reserved**
	28	**Reserved**
	27	**AUX Channel D** The ISR is an active high pulse on the AUX DDI D done event. This event will not occur for SRD AUX done.
	26	**AUX Channel C** The ISR is an active high pulse on the AUX DDI C done event. This event will not occur for SRD AUX done.
	25	**AUX Channel B** The ISR is an active high pulse on the AUX DDI B done event. This event will not occur for SRD AUX done.
	24	**MIPI C TE** The ISR is an active high level indicating a TE interrupt is set in MIPIC_STATUS.
	23	**MIPI A TE** The ISR is an active high level indicating a TE interrupt is set in MIPIA_STATUS.
	22:12	**Reserved**

DE Port Interrupt Definition		
	11:10	**Reserved**
	9:8	**Reserved**
	7:6	**Reserved**
	5	**DDI C Hotplug** The ISR gives the live state of the DDI HPD pin when the HPD input is enabled. The IIR is set if a short or long pulse is detected when HPD input is enabled. This field is unused in projects that have a PCH.
	4	**DDI B Hotplug** The ISR gives the live state of the DDI HPD pin when the HPD input is enabled. The IIR is set if a short or long pulse is detected when HPD input is enabled. This field is unused in projects that have a PCH.
	3	**DDI A Hotplug** The ISR gives the live state of the DDI HPD pin when the HPD input is enabled. The IIR is set if a short or long pulse is detected when HPD input is enabled. This field is unused in projects that have a PCH.
	2	**Reserved**
	1	**GMbus** The ISR is an active high pulse when any of the unmasked events in GMBUS4 Interrupt Mask register occur. This field is only used on projects that have GMBUS integrated into the north display. Projects that have GMBUS in the south display have the GMBUS interrupt in the south display interrupts.
	0	**AUX_Channel_A** The ISR is an active high pulse on the AUX DDI A done event. This event will not occur for SRD AUX done.

Device 0 Capabilities A

CAPID0_A_0_0_0_PCI - Device 0 Capabilities A

Register Space:	PCI: 0/0/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	000E4h

DWord	Bit	Description
0	31	**Display HD Audio Disable** Default Value: 0b Access: R/W Key Firmware Only Unused - Bit field not relevant for the current project
	30	**PEG12 Disable** Default Value: 0b Access: R/W Key Firmware Only Unused - Bit field not relevant for the current project
	29	**PEG11 Disable** Default Value: 0b Access: R/W Key Firmware Only Unused - Bit field not relevant for the current project
	28	**PEG10 Disable** Default Value: 0b Access: R/W Key Firmware Only Unused - Bit field not relevant for the current project
	27	**PCI Express Link Width Upconfig Disable** Default Value: 0b Access: R/W Firmware Only Unused - Bit field not relevant for the current project
	26	**DMI Width** Default Value: 0b Access: R/W Firmware Only Unused - Bit field not relevant for the current project
	25	**ECC Disable** Default Value: 0b Access: R/W Firmware Only Unused - Bit field not relevant for the current project

CAPID0_A_0_0_0_PCI - Device 0 Capabilities A

	24	**Force DRAM ECC Enabled** Default Value: 0b Access: R/W Firmware Only Unused - Bit field not relevant for the current project
	23	**VTd Disable** Default Value: 0b Access: R/W Firmware Only 0: Enable VTd 1: Disable VTd
	22	**DMI Gen 2 Disable** Default Value: 0b Access: R/W Firmware Only Unused - Bit field not relevant for the current project
	21	**PEG Gen 2 Disable** Default Value: 0b Access: R/W Firmware Only Unused - Bit field not relevant for the current project
	20:19	**DDR Size** Default Value: 00b Access: R/W Firmware Only Unused - Bit field not relevant for the current project
	18	**Bclk overclocking disable** Default Value: 0b Access: R/W Firmware Only Unused - Bit field not relevant for the current project
	17	**Disable 1N Mode** Default Value: 0b Access: R/W Firmware Only Unused - Bit field not relevant for the current project
	16	**Full ULT Fuse Read Disable** Default Value: 0b Access: R/W Firmware Only Unused - Bit field not relevant for the current project
	15	**Camarillo Device Disable** Default Value: 0b Access: R/W Firmware Only 0: DPTF (Camarillo) associated memory spaces are accessible. 1: DPTF (Camarillo) associated memory and IO spaces are disabled. DEVEN_0_0_0_PCI field for

CAPID0_A_0_0_0_PCI - Device 0 Capabilities A

		DPTF can not be set.
	14	**2 DIMMS per Channel Disable** Default Value: 0b Access: R/W Firmware Only Unused - Bit field not relevant for the current project
	13	**X2APIC Enabled** Default Value: 0b Access: R/W Firmware Only Unused - Bit field not relevant for the current project
	12	**Performance Dual Channel Disable** Default Value: 0b Access: R/W Firmware Only Unused - Bit field not relevant for the current project
	11	**Internal Graphics Disable** Default Value: 0b Access: R/W Key Firmware Only 0b: There is a graphics engine within this CPU. Internal Graphics Device (Device 2) is enabled and all of its memory and I/O spaces are accessable. Configuration cycles to Device 2 will be completed within the CPU. All non-SMM memory and IO accesses to VGA will be handled based on Memory and IO enables of Device 2 and IO registers within Device 2 and VGA Enable of the PCI to PCI bridge control (If PCI Express GFX attach is supported). A selected amount of Graphics Memory space is pre-allocated from the main memory based on Graphics Mode Select (GMS in the GGC Register). Graphics Memory is pre-allocated above TSEG Memory. 1b: There is no graphics engine within this CPU. Internal Graphics Device (Device 2) and all of its memory and I/O functions are disabled. Configuration cycle targeted to Device 2 will be passed on. All non-SMM memory and IO accesses to VGA will be handled based on VGA Enable of the PCI to PCI bridge control. Device 2 is disabled and hidden.
	10	**Reserved**
	9:8	**Capability Device ID** Default Value: 00b Access: R/W Firmware Only
	7:4	**Compatibility Rev ID** Default Value: 0000b Access: R/W Firmware Only Unused - Bit field not relevant for the current project
	3	**DDR Overclocking** Default Value: 0b Access: R/W Firmware Only Unused - Bit field not relevant for the current project

CAPID0_A_0_0_0_PCI - Device 0 Capabilities A

	2	**IA Overclocking Enabled by DSKU** Default Value: 0b Access: R/W Firmware Only Unused - Bit field not relevant for the current project
	1	**DDR Write VRef Enable** Default Value: 0b Access: R/W Firmware Only Unused - Bit field not relevant for the current project
	0	**DDR3L Enable** Default Value: 0b Access: R/W Firmware Only Unused - Bit field not relevant for the current project

Device 0 Capabilities B

CAPID0_B_0_0_0_PCI - Device 0 Capabilities B

Register Space:	PCI: 0/0/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	000E8h

DWord	Bit	Description
0	31	**Reserved_31** Default Value: 0b Access: R/W Firmware Only Unused - Bit field not relevant for the current project
	30	**IA Overclocking DSKU Control Disable** Default Value: 0b Access: R/W Firmware Only Unused - Bit field not relevant for the current project
	29	**IA Overclocking Enable** Default Value: 0b Access: R/W Firmware Only Unused - Bit field not relevant for the current project
	28	**SMT Capability** Default Value: 0b Access: R/W Firmware Only Unused - Bit field not relevant for the current project
	27:25	**Cache Size Capability** Default Value: 000b Access: R/W Firmware Only Unused - Bit field not relevant for the current project
	24	**SVMDIS** Access: R/W Firmware Only Value 0b: SVM mode enabled **[Default]** Value 1b: SVM mode disabled
	23:21	**DDR3 Maximum Frequency Capability with 100 Memory** Access: R/W Firmware Only Unused - Bit field not relevant for the current project

CAPID0_B_0_0_0_PCI - Device 0 Capabilities B

	20	**Gen3 Disable Fuse for PCIe PEG Controllers** Default Value: 0b Access: R/W Firmware Only Unused - Bit field not relevant for the current project
	19	**Package Type** Default Value: 0b Access: R/W Firmware Only Unused - Bit field not relevant for the current project
	18	**Additive Graphics Enabled** Default Value: 0b Access: R/W Firmware Only Unused - Bit field not relevant for the current project
	17	**Additive Graphics Capable** Default Value: 0b Access: R/W Firmware Only Unused - Bit field not relevant for the current project
	16	**Primary PEG Port x16 Disable** Default Value: 0b Access: R/W Firmware Only Unused - Bit field not relevant for the current project
	15:12	**Reserved_15_12** Default Value: 0000b Access: R/W Firmware Only Unused - Bit field not relevant for the current project
	11	**Reserved**
	10:8	**Reserved_10_8** Default Value: 000b Access: R/W Firmware Only Unused - Bit field not relevant for the current project
	7	**Reserved**
	6:4	**DDR3 Maximum Frequency Capability** Default Value: 000b Access: R/W Firmware Only Unused - Bit field not relevant for the current project

CAPID0_B_0_0_0_PCI - Device 0 Capabilities B

	3	**Reserved_3** Default Value: 0b Access: R/W Firmware Only Unused - Bit field not relevant for the current project
	2	**DDR4 DSKU Enable** Default Value: 0b Access: R/W Firmware Only Unused - Bit field not relevant for the current project
	1	**Dual PEG Force x1 when VGA Enabled** Default Value: 0b Access: R/W Firmware Only Unused - Bit field not relevant for the current project
	0	**Single PEG Force x1 when VGA Enabled** Default Value: 0b Access: R/W Firmware Only Unused - Bit field not relevant for the current project

Device 2 Control

DEV2CTL_0_2_0_PCI - Device 2 Control			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	8		
Address:	00058h		
This register implements a control bit to disable and hide the IOBAR register in systems that do not require legacy IOBAR access to Gfx MMIO registers.			
DWord	**Bit**	**Description**	
0	7:1	**Reserved**	
		Default Value:	0000000b
		Access:	RO
		Reserved	
	0	**Reserved**	

Device Capabilities

DEVICECAP_0_2_0_PCI - Device Capabilities

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x10008000
Size (in bits):	32
Address:	00074h

PCI Express Device Capabilities

DWord	Bit	Description
0	31:29	**Reserved** Default Value: 000b Access: RO Reserved
	28	**Functional Level Reset Capability** Default Value: 1b Access: RO Hardwired to 1b to indicate the Function supports the optional Function Level Reset mechanism.
	27:26	**Captured Slot Power Limit Scale** Default Value: 00b Access: RO Not applicable for a Root Complex Integrated Endpoint with no Link or Slot. Hardwired to 00b
	25:18	**Captured Slot Power Limit Value** Default Value: 00000000h Access: RO Not applicable for a Root Complex Integrated Endpoint with no Link or Slot. Hardwired to 00h
	17:16	**Reserved** Default Value: 00b Access: RO Reserved
	15	**Role-Based Error Reporting** Default Value: 1b Access: RO

DEVICECAP_0_2_0_PCI - Device Capabilities

When Set, this bit indicates that the Function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1.
Hardwired to 1b as this bit must be Set by all Functions conforming to the ECN, PCI Express Base Specification, Revision 1.1, or subsequent PCI Express Base Specification revisions.

14:12 RESERVED

Default Value:	000b
Access:	RO

Reserved

11:9 Endpoint L1 Acceptable Latency

Default Value:	000b
Access:	RO

This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from the L1 state to the L0 state.
This does not apply to the integrated graphics device, so it is hardwired to 000b (Maximum of 1 us).

8:6 Endpoint L0s Acceptable Latency

Default Value:	000b
Access:	RO

This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from the L0s state to the L0 state.
This does not apply to the integrated graphics device, so it is hardwired to 000b (Maximum of 64 ns).

5 Extended Tag Field Supported

Default Value:	0b
Access:	RO

This bit indicates the maximum supported size of the Tag field as a Requester.
This does not apply to the integrated graphics device, so it is hardwired to 0b (5-bit Tag field supported).

4:3 Phantom Functions Supported

Default Value:	00b
Access:	RO

This field indicates the support for use of unclaimed Function Numbers to extend the number of outstanding transactions for PCIe devices.
This does not apply to the integrated graphics device, so it is hardwired to 00b to indicate no Function Number bits are used for Phantom Functions.

DEVICECAP_0_2_0_PCI - Device Capabilities

	2:0	**Max Payload Size Supported** Default Value: 000b Access: RO This field indicates the maximum payload size that the Function can support for TLPs. Hardwired to 000b to represents 128 bytes, the minimum allowed value.

Device Enable

DEVEN_0_0_0_PCI - Device Enable

Register Space:	PCI: 0/0/0
Source:	BSpec
Default Value:	0x000000BF
Size (in bits):	32
Address:	00054h

Allows for enabling/disabling of PCI devices and functions that are within the CPU package.

DWord	Bit	Description
0	31:15	**RESERVED** Default Value: 000b Access: RO
	14	**Chap Enable** Default Value: 0b Access: R/W Unused - Bit field not relevant for the current project
	13	**Device 6 Enable** Default Value: 0b Access: R/W Unused - Bit field not relevant for the current project
	12:11	**RESERVED** Default Value: 000b Access: RO
	10	**Device 5 Enable** Default Value: 0b Access: R/W Lock Unused - Bit field not relevant for the current project
	9:8	**RESERVED** Default Value: 000b Access: RO
	7	**Device 4 Enable** Default Value: 1b Access: R/W Lock Unused - Bit field not relevant for the current project

DEVEN_0_0_0_PCI - Device Enable

	6	**RESERVED** Default Value: 000b Access: RO
	5	**Device 3 enable for Display HD Audio** Default Value: 1b Access: R/W Lock
	4	**Internal Graphics Engine** Default Value: 1b Access: R/W Lock 0: Bus 0 Device 2 is disabled and hidden 1: Bus 0 Device 2 is enabled and visible This bit will be set to 0b and remain 0b if Device 2 capability is disabled.
	3	**PEG10 Enable** Default Value: 1b Access: R/W Lock Unused - Bit field not relevant for the current project
	2	**PEG11 Enable** Default Value: 1b Access: R/W Lock Unused - Bit field not relevant for the current project
	1	**PEG12 Enable** Default Value: 1b Access: R/W Lock
	0	**Host Bridge** Default Value: 1b Access: RO

Device Identification

DID2_0_2_0_PCI - Device Identification

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000A84
Size (in bits):	16
Address:	00002h

This register combined with the Vendor Identification register uniquely identifies any PCI device.

DWord	Bit	Description
0	15:7	**Device Identification Number MSB** Default Value: 000010101b Access: RO Variant Firmware Only This is the upper part of a 16 bit value assigned to the device.
	6:2	**Device Identification Number STRAPS** Default Value: 00001b Access: RO Variant These are bits 6:2 of the 16 bit value, updated from straps.
	1:0	**Device Identification Number SKU** Default Value: 00b Access: RO Variant This is the lower part of a 16 bit value assigned to the device.

DFSM

DFSM

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	51000h-51003h
Name:	Display Fuse
ShortName:	DFSM
Power:	PG0
Reset:	global

This register contains fuse and strap settings for display.
This register is not reset by FLR.

DWord	Bit	Description
0	31	**Internal Graphics Disable** This bit indicates whether internal graphics capability is disabled. Value: 0b – Name: Enable – Description: Internal Graphics Enabled Value: 1b – Name: Disable – Description: Internal Graphics Disabled
	30	**Internal Display Disable** This bit indicates whether the display pipe A (first pipe) capability is disabled. Value: 0b – Name: Enable – Description: Pipe A Capability Enabled Value: 1b – Name: Disable – Description: Pipe A Capability Disabled
	29	**Reserved**
	28	**Display PipeC Disable** This bit indicates whether the display pipe C (third pipe) capability is disabled. Value: 0b – Name: Enable – Description: Pipe C Capability Enabled Value: 1b – Name: Disable – Description: Pipe C Capability Disabled
	27	**Display PM Disable** This bit indicates whether the display power management FBC and DPST capabilities are disabled. Value: 0b – Name: Enable – Description: PM Capability Enabled Value: 1b – Name: Disable – Description: PM Capability Disabled

DFSM

26 Display eDP Disable

Description
This bit indicates whether the display embedded DisplayPort eDP DDIA capability is disabled.

Value	Name	Description
0b	Enable	eDP Capability Enabled
1b	Disable	eDP Capability Disabled

25 Reserved

24:23 Display CDCLK Limit

This field indicates the maximum allowed CD clock frequency.

Value	Name	Description
00b	675 MHz	Maximum frequency is 675 MHz. All frequencies are allowed.
01b	540 MHz	Maximum frequency is 540 MHz.
10b	450 MHz	Maximum frequency is 450 MHz.
11b	337.5 MHz	Maximum frequency is 337.5 MHz.

Programming Notes
This field is unused on BXT. Any CD clock frequency limitation must be done in software.

Restriction
Restriction : Display software should not select any frequency higher than the maximum that is allowed. If software incorrectly selects a higher frequency, display hardware will internally override the selection to the lowest frequency.

22 Display Spare

21 Spare 21

This bit indicates whether the display pipe B (second pipe) capability is disabled.

Value	Name
0b	Pipe B Capability Enabled
1b	Pipe B Capability Disabled

20 Display WD Disable

This bit indicates whether the display WD capability is disabled.

Value	Name	Description
0b	Enable	WD Capability Enabled
1b	Disable	WD Capability Disabled

19 Spare 19

18 Spare 18

17 Spare 17

DFSM

		Description Device ID bit 1
	16	**Spare 16** **Description** Device ID bit 0
	15	**Spare 15**
	14	**Spare 14**
	13	**Spare 13**
	12	**Spare 12**
	11	**Spare 11**
	10	**Spare 10**
	9	**Spare 9**
	8	**Spare 8**
	7	**Spare 7** **Description** This field indicates whether the DSC feature is disabled. **Value** / **Name** 0b – DSC Capability Enabled 1b – DSC Capability Disabled
	6	**Display RSB Enable** This bit indicates whether the remote screen blanking feature is enabled in the display engine. **Value** / **Name** / **Description** 0b – Disable – RSB Capability Disabled 1b – Enable – RSB Capability Enabled
	5	**Spare 5**
	4	**Spare 4**
	3	**Spare 3**
	2	**Spare 2**
	1	**Reserved**
	0	**Display Audio Codec Disable** This bit indicates whether the display audio codec capability is disabled. **Value** / **Name** / **Description** 0b – Enable – Audio Codec Capability Enabled 1b – Disable – Audio Codec Capability Disabled

DISPLAY_DEADLINE_CONTROL

DISPLAY_DEADLINE_CONTROL - DISPLAY_DEADLINE_CONTROL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	10102Ch

Deadline latency override control

DWord	Bit	Description
0	31:11	**Reserved** Default Value: 0000000h Access: R/W Reserved
	10:1	**Latency_Override_Offset** Default Value: 000h Access: R/W When enable, provides a fixed latency offset override for display VC1 requests. For example, value of 0 would sent every VC1 request with the current global time value .. effectively making every VC1 request access "urgent".
	0	**Latency_Override_Enable** Default Value: 0b Access: R/W 0 (default) : Hardware determined deadlines. 1 : Latency override enabled. Deadline latency offsets are no longer hardware determined. Instead, deadline latency offsets are taken from the "latency_override_offset" bits

DMA Protected Range

DPR_0_0_0_PCI - DMA Protected Range

Register Space:	PCI: 0/0/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	0005Ch

DMA protected range register.

DWord	Bit	Description
0	31:20	**Top of DPR** Default Value: 000000000000b Access: RO Variant Firmware Only Top address + 1 of DPR. This is the base of TSEG. Bits 19:0 of the BASE reported here are 0x0_0000.
	19:12	**RESERVED** Default Value: 000b Access: RO Reserved
	11:4	**DPRSIZE** Default Value: 00000000b Access: R/W Lock This is the size of memory, in MB, that will be protected from DMA accesses. A value of 0x00 in this field means no additional memory is protected. The maximum amount of memory that will be protected is 255MB. The amount of memory reported in this field will be protected from all DMA accesses, including translated CPU accesses and graphics. The top of the protected range is the BASE of TSEG -1. Note: If TSEG is not enabled, then the top of this range becomes the base of stolen graphics, or ME stolen space or TOLUD, whichever would have been the location of TSEG, assuming it had been enabled. The DPR range works independently of any other range, including the NoDMA.TABLE protection or the PMRC checks in VTd, and is done post any VTd translation or LT NoDMA lookup. Therefore incomming cycles are checked against this range after the VTd translation and faulted if they hit this protected range, even if they passed the VTd translation or were clean in the NoDMA lookup. All the memory checks are OR'ed with respect to NOT being allowed to go to memory. So if either PMRC, DPR, NoDMA table lookup, NoDMA.TABLE.PROTECT OR a VTd translation disallows the cycle, then the cycle is not allowed to go to memory. Or in other words, all of the above checks must pass before a cycle is allowed to DRAM.

DPR_0_0_0_PCI - DMA Protected Range

	3	**RESERVED** Default Value: 000b Access: RO Reserved
	2	**EPM** Default Value: 0b Access: R/W Lock This field controls DMA accesses to the DMA Protected Range (DPR) region. 0: DPR is disabled. 1: DPR is enabled. All DMA requests accessing DPR region are blocked. Dev 0 HW reports the status of DPR enable/disabled through the PRS field in this register.
	1	**Protected Range Status** Default Value: 0b Access: RO Variant Firmware Only This field indicated the status of DPR. 0: DPR protection disabled. 1: DPR protection enabled.
	0	**Lock** Default Value: 0b Access: R/W Key Lock All bits which may be updated by SW in this register are locked down when this bit is set.

DPFC_CONTROL_SA

DPFC_CTL_SA - DPFC_CONTROL_SA

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	100100h

This register contains control bits related to Display Frame Buffer Compression Host Invalidation in System Agent.

DWord	Bit	Description
0	31:30	**Reserved** Default Value: 00b Access: R/W Reserved
	29	**CPUFNCEN** Default Value: 0b Access: R/W 0: Display Buffer is not in a CPU fence. No modifications are allowed from CPU to the Display Buffer. 1: Display Buffer exists in a CPU fence.
	28:5	**Reserved** Default Value: 000000h Access: R/W Reserved
	4:0	**CPUFNCNUM** Default Value: 00h Access: R/W This field specifies the CPU visible FENCE number corresponding to the placement of the uncompressed frame buffer.

DPFC_CPU_FENCE_OFFSET

DPFC_CFO - DPFC_CPU_FENCE_OFFSET

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	100104h

This register contains control bits related to Display Frame Buffer Compression Host Invalidation in System Agent.

DWord	Bit	Description
0	31:22	**Reserved** Default Value: 000h Access: R/W Reserved
	21:0	**YFNCDISP** Default Value: 000000h Access: R/W Y offset from the CPU fence to the Display Buffer base

DSC_CRC_CTL

DSC_CRC_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B284h-6B287h
Name:	DSC_CRC_CTL_A
ShortName:	DSC_CRC_CTL_A
Power:	PG1
Reset:	soft
Address:	6BA84h-6BA87h
Name:	DSC_CRC_CTL_C
ShortName:	DSC_CRC_CTL_C
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31	**Enable CRC** Access: R/W Enables the CRC calculations. The CRC will give a done indication and a new result at the end of each frame. Value: 0b — Name: Disable Value: 1b — Name: Enable
	30	**CRC Done** Access: R/WC This bit is set on the rising edge of the CRC done indication. This is a sticky bit, cleared by writing 1b to it. Value: 0b — Name: Not Done Value: 1b — Name: Done
	29	**CRC Change** Access: R/WC This bit is set if the CRC result value changes from the previous value. This is a sticky bit, cleared by writing 1b to it.

DSC_CRC_CTL

		Value	Name
		0b	No Change
		1b	Change
	28:0	**Reserved**	
		Format:	MBZ

DSC_CRC_RES

DSC_CRC_RES	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	6B288h-6B28Bh
Name:	DSC_CRC_RES_A
ShortName:	DSC_CRC_RES_A
Power:	PG1
Reset:	soft
Address:	6BA88h-6BA8Bh
Name:	DSC_CRC_RES_C
ShortName:	DSC_CRC_RES_C
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:0	**CRC Result Value** This field contains the CRC result at the end of a CRC frame. The CRC done bit indicates when the result is valid.

DSC_PICTURE_PARAMETER_SET_0

DSC_PICTURE_PARAMETER_SET_0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B200h-6B203h
Name:	DSCA_PICTURE_PARAMETER_SET_0
ShortName:	DSCA_PICTURE_PARAMETER_SET_0
Power:	PG1
Reset:	soft
Address:	6BA00h-6BA03h
Name:	DSCC_PICTURE_PARAMETER_SET_0
ShortName:	DSCC_PICTURE_PARAMETER_SET_0
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:20	**Reserved** Format: MBZ
	19	**vbr_enable** Access: R/W

Value	Name	Description
0b	disable **[Default]**	"0" padding bits are stuffed at the end of a slice to ensure that the total number of bits within the slice is equal to the slice bit budget.
1b	Enable	Bit stuffing is bypassed

	18	**enable_422** Access: R/W

Value	Name	Description
0b	444 **[Default]**	Input uses 4:4:4 sampling
1b	422	Input uses 4:2:2 sampling

	17	**convert_rgb** Access: R/W Indicates whether DSC color space conversion is active.

DSC_PICTURE_PARAMETER_SET_0

Value	Name	Description
0b	YCbCr	Color space is YCbCr
1b	convert_rgb	Encoder converts RGB to YCoCg-R, and decoder converts YCoCg-R to RGB.

16 **block_pred_enable**

Access:	R/W

Value	Name	Description
0b	disable	BP is not used to code any groups within the picture
1b	enable	Decoder must select between BP and MMAP

15:12 **linebuf_depth**

Access:	R/W

Contains the line buffer bit depth used to generate the bitstream. If a component's bit depth (after color space conversion) is greater than this value, the line storage rounds the reconstructed values to this number of bits.
0x8 = 8 bits
0x9 = 9 bits
0xA = 10 bits
0xB = 11 bits
0xC = 12 bits
0xD = 13 bits
All other encodings are RESERVED

11:8 **bits_per_component**

Access:	R/W

Indicates the number of bits per component for the original pixels of the encoded picture.
0x8 = 8bpc
0xA = 10bpc
0xC = 12bpc
All other encodings are RESERVED

7:4 **dsc_version_minor**

Access:	R/W

Contains the major version of DSC.
0x1 = Encoder implements DSC

3:0 **dsc_version_major**

Access:	R/W

Contains the major version of DSC.
0x1 = Encoder implements DSC

DSC_PICTURE_PARAMETER_SET_1

DSC_PICTURE_PARAMETER_SET_1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B204h-6B207h
Name:	DSCA_PICTURE_PARAMETER_SET_1
ShortName:	DSCA_PICTURE_PARAMETER_SET_1
Power:	PG1
Reset:	soft
Address:	6BA04h-6BA07h
Name:	DSCC_PICTURE_PARAMETER_SET_1
ShortName:	DSCC_PICTURE_PARAMETER_SET_1
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:10	**RESERVED** Format: MBZ
	9:0	**bits_per_pixel** Access: R/W

DSC_PICTURE_PARAMETER_SET_2

DSC_PICTURE_PARAMETER_SET_2	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B208h-6B20Bh
Name:	DSCA_PICTURE_PARAMETER_SET_2
ShortName:	DSCA_PICTURE_PARAMETER_SET_2
Power:	PG1
Reset:	soft
Address:	6BA08h-6BA0Bh
Name:	DSCC_PICTURE_PARAMETER_SET_2
ShortName:	DSCC_PICTURE_PARAMETER_SET_2
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:16	**pic_width** Access: R/W
	15:0	**pic_height** Access: R/W

DSC_PICTURE_PARAMETER_SET_3

DSC_PICTURE_PARAMETER_SET_3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B20Ch-6B20Fh
Name:	DSCA_PICTURE_PARAMETER_SET_3
ShortName:	DSCA_PICTURE_PARAMETER_SET_3
Power:	PG1
Reset:	soft
Address:	6BA0Ch-6BA0Fh
Name:	DSCC_PICTURE_PARAMETER_SET_3
ShortName:	DSCC_PICTURE_PARAMETER_SET_3
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:16	**slice_width** Access: R/W This defines the width of the slice in number of pixels.
	15:0	**slice_height** Access: R/W This defines the height of the slice in number of pixels.

DSC_PICTURE_PARAMETER_SET_4

DSC_PICTURE_PARAMETER_SET_4	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B210h-6B213h
Name:	DSCA_PICTURE_PARAMETER_SET_4
ShortName:	DSCA_PICTURE_PARAMETER_SET_4
Power:	PG1
Reset:	soft
Address:	6BA10h-6BA13h
Name:	DSCC_PICTURE_PARAMETER_SET_4
ShortName:	DSCC_PICTURE_PARAMETER_SET_4
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:16	**initial_dec_delay** Access: R/W
	15:10	**RESERVED** Format: MBZ
	9:0	**initial_xmit_delay** Access: R/W

DSC_PICTURE_PARAMETER_SET_5

DSC_PICTURE_PARAMETER_SET_5	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B214h-6B217h
Name:	DSCA_PICTURE_PARAMETER_SET_5
ShortName:	DSCA_PICTURE_PARAMETER_SET_5
Power:	PG1
Reset:	soft
Address:	6BA14h-6BA17h
Name:	DSCC_PICTURE_PARAMETER_SET_5
ShortName:	DSCC_PICTURE_PARAMETER_SET_5
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:28	**RESERVED** Format: MBZ
	27:16	**scale_decrement_interval** Access: R/W
	15:0	**scale_increment_interval** Access: R/W

DSC_PICTURE_PARAMETER_SET_6

DSC_PICTURE_PARAMETER_SET_6	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B218h-6B21Bh
Name:	DSCA_PICTURE_PARAMETER_SET_6
ShortName:	DSCA_PICTURE_PARAMETER_SET_6
Power:	PG1
Reset:	soft
Address:	6BA18h-6BA1Bh
Name:	DSCC_PICTURE_PARAMETER_SET_6
ShortName:	DSCC_PICTURE_PARAMETER_SET_6
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:29	**RESERVED** Format: MBZ
	28:24	**flatness_max_qp** Access: R/W
	23:21	**RESERVED** Format: MBZ
	20:16	**flatness_min_qp** Access: R/W
	15:13	**RESERVED** Format: MBZ
	12:8	**first_line_bpg_offset** Access: R/W
	7:6	**RESERVED** Format: MBZ
	5:0	**initial_scale_value** Access: R/W

DSC_PICTURE_PARAMETER_SET_7

DSC_PICTURE_PARAMETER_SET_7	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B21Ch-6B21Fh
Name:	DSCA_PICTURE_PARAMETER_SET_7
ShortName:	DSCA_PICTURE_PARAMETER_SET_7
Power:	PG1
Reset:	soft
Address:	6BA1Ch-6BA1Fh
Name:	DSCC_PICTURE_PARAMETER_SET_7
ShortName:	DSCC_PICTURE_PARAMETER_SET_7
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:16	**nfl_bpg_offset** Access: R/W
	15:0	**slice_bpg_offset** Access: R/W

DSC_PICTURE_PARAMETER_SET_8

DSC_PICTURE_PARAMETER_SET_8	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B220h-6B223h
Name:	DSCA_PICTURE_PARAMETER_SET_8
ShortName:	DSCA_PICTURE_PARAMETER_SET_8
Power:	PG1
Reset:	soft
Address:	6BA20h-6BA23h
Name:	DSCC_PICTURE_PARAMETER_SET_8
ShortName:	DSCC_PICTURE_PARAMETER_SET_8
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:16	**initial_offset** Access: R/W
	15:0	**final_offset** Access: R/W

DSC_PICTURE_PARAMETER_SET_9

DSC_PICTURE_PARAMETER_SET_9	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B224h-6B227h
Name:	DSCA_PICTURE_PARAMETER_SET_9
ShortName:	DSCA_PICTURE_PARAMETER_SET_9
Power:	PG1
Reset:	soft
Address:	6BA24h-6BA27h
Name:	DSCC_PICTURE_PARAMETER_SET_9
ShortName:	DSCC_PICTURE_PARAMETER_SET_9
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:20	**RESERVED** Format: MBZ
	19:16	**rc_edge_factor** Access: R/W
	15:0	**rc_model_Size** Access: R/W

DSC_PICTURE_PARAMETER_SET_10

DSC_PICTURE_PARAMETER_SET_10	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B228h-6B22Bh
Name:	DSCA_PICTURE_PARAMETER_SET_10
ShortName:	DSCA_PICTURE_PARAMETER_SET_10
Power:	PG1
Reset:	soft
Address:	6BA28h-6BA2Bh
Name:	DSCC_PICTURE_PARAMETER_SET_10
ShortName:	DSCC_PICTURE_PARAMETER_SET_10
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:24	**RESERVED** Format: MBZ
	23:20	**rc_tgt_offset_lo** Access: R/W
	19:16	**rc_tgt_offset_hi** Access: R/W
	15:13	**RESERVED** Format: MBZ
	12:8	**rc_quant_incr_limit1** Access: R/W
	7:5	**RESERVED** Format: MBZ
	4:0	**rc_quant_incr_limit0** Access: R/W

DSC_PICTURE_PARAMETER_SET_11

DSC_PICTURE_PARAMETER_SET_11	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B22Ch-6B22Fh
Name:	DSCA_PICTURE_PARAMETER_SET_11
ShortName:	DSCA_PICTURE_PARAMETER_SET_11
Power:	PG1
Reset:	soft
Address:	6BA2Ch-6BA2Fh
Name:	DSCC_PICTURE_PARAMETER_SET_11
ShortName:	DSCC_PICTURE_PARAMETER_SET_11
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:0	**RESERVED** Format: MBZ

DSC_PICTURE_PARAMETER_SET_12

DSC_PICTURE_PARAMETER_SET_12	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B260h-6B263h
Name:	DSCA_PICTURE_PARAMETER_SET_12
ShortName:	DSCA_PICTURE_PARAMETER_SET_12
Power:	PG1
Reset:	soft
Address:	6BA60h-6BA63h
Name:	DSCC_PICTURE_PARAMETER_SET_12
ShortName:	DSCC_PICTURE_PARAMETER_SET_12
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:0	**RESERVED** Format: MBZ

DSC_PICTURE_PARAMETER_SET_13

DSC_PICTURE_PARAMETER_SET_13	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B264h-6B267h
Name:	DSCA_PICTURE_PARAMETER_SET_13
ShortName:	DSCA_PICTURE_PARAMETER_SET_13
Power:	PG1
Reset:	soft
Address:	6BA64h-6BA67h
Name:	DSCC_PICTURE_PARAMETER_SET_13
ShortName:	DSCC_PICTURE_PARAMETER_SET_13
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:0	**RESERVED** Format: MBZ

DSC_PICTURE_PARAMETER_SET_14

DSC_PICTURE_PARAMETER_SET_14	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B268h-6B26Bh
Name:	DSCA_PICTURE_PARAMETER_SET_14
ShortName:	DSCA_PICTURE_PARAMETER_SET_14
Power:	PG1
Reset:	soft
Address:	6BA68h-6BA6Bh
Name:	DSCC_PICTURE_PARAMETER_SET_14
ShortName:	DSCC_PICTURE_PARAMETER_SET_14
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:0	**RESERVED** Format: MBZ

DSC_PICTURE_PARAMETER_SET_15

DSC_PICTURE_PARAMETER_SET_15	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B26Ch-6B26Fh
Name:	DSCA_PICTURE_PARAMETER_SET_15
ShortName:	DSCA_PICTURE_PARAMETER_SET_15
Power:	PG1
Reset:	soft
Address:	6BA6Ch-6BA6Fh
Name:	DSCC_PICTURE_PARAMETER_SET_15
ShortName:	DSCC_PICTURE_PARAMETER_SET_15
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:0	**RESERVED** Format: MBZ

DSC_PICTURE_PARAMETER_SET_16

DSC_PICTURE_PARAMETER_SET_16	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B270h-6B273h
Name:	DSCA_PICTURE_PARAMETER_SET_16
ShortName:	DSCA_PICTURE_PARAMETER_SET_16
Power:	PG1
Reset:	soft
Address:	6BA70h-6BA73h
Name:	DSCC_PICTURE_PARAMETER_SET_16
ShortName:	DSCC_PICTURE_PARAMETER_SET_16
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:20	**slice_row_per_frame** Access: R/W
	19	**RESERVED** Format: MBZ
	18:16	**slice_per_line** Access: R/W
	15:0	**slice_chunk_size** Access: R/W

DSC_RC_BUF_THRESH_0

DSC_RC_BUF_THRESH_0	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	6B230h-6B237h
Name:	DSCA_RC_BUF_THRESH_0
ShortName:	DSCA_RC_BUF_THRESH_0
Power:	PG1
Reset:	soft
Address:	6BA30h-6BA37h
Name:	DSCC_RC_BUF_THRESH_0
ShortName:	DSCC_RC_BUF_THRESH_0
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:24	**rc_buf_thresh_3** Access: R/W
	23:16	**rc_buf_thresh_2** Access: R/W
	15:8	**rc_buf_thresh_1** Access: R/W
	7:0	**rc_buf_thresh_0** Access: R/W
1	31:24	**rc_buf_thresh_7** Access: R/W
	23:16	**rc_buf_thresh_6** Access: R/W
	15:8	**rc_buf_thresh_5** Access: R/W
	7:0	**rc_buf_thresh_4** Access: R/W

DSC_RC_BUF_THRESH_1

DSC_RC_BUF_THRESH_1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	6B238h-6B23Fh
Name:	DSCA_RC_BUF_THRESH_1
ShortName:	DSCA_RC_BUF_THRESH_1
Power:	PG1
Reset:	soft
Address:	6BA38h-6BA3Fh
Name:	DSCC_RC_BUF_THRESH_1
ShortName:	DSCC_RC_BUF_THRESH_1
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:24	**rc_buf_thresh_11** Access: R/W
	23:16	**rc_buf_thresh_10** Access: R/W
	15:8	**rc_buf_thresh_9** Access: R/W
	7:0	**rc_buf_thresh_8** Access: R/W
1	31:16	**RESERVED** Format: MBZ
	15:8	**rc_buf_thresh_13** Access: R/W
	7:0	**rc_buf_thresh_12** Access: R/W

DSC_RC_RANGE_PARAMETERS_0

DSC_RC_RANGE_PARAMETERS_0	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	6B240h-6B247h
Name:	DSCA_RC_RANGE_PARAMETERS_0
ShortName:	DSCA_RC_RANGE_PARAMETERS_0
Power:	PG1
Reset:	soft
Address:	6BA40h-6BA47h
Name:	DSCC_RC_RANGE_PARAMETERS_0
ShortName:	DSCC_RC_RANGE_PARAMETERS_0
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:26	**rc_bpg_offset_1** Access: R/W
	25:21	**rc_max_qp_1**
	20:16	**rc_min_qp_1**
	15:10	**rc_bpg_offset_0** Access: R/W
	9:5	**rc_max_qp_0**
	4:0	**rc_min_qp_0**
1	31:26	**rc_bpg_offset_3** Access: R/W
	25:21	**rc_max_qp_3**
	20:16	**rc_min_qp_3**
	15:10	**rc_bpg_offset_2** Access: R/W
	9:5	**rc_max_qp_2**
	4:0	**rc_min_qp_2**

DSC_RC_RANGE_PARAMETERS_1

DSC_RC_RANGE_PARAMETERS_1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	6B248h-6B24Fh
Name:	DSCA_RC_RANGE_PARAMETERS_1
ShortName:	DSCA_RC_RANGE_PARAMETERS_1
Power:	PG1
Reset:	soft
Address:	6BA48h-6BA4Fh
Name:	DSCC_RC_RANGE_PARAMETERS_1
ShortName:	DSCC_RC_RANGE_PARAMETERS_1
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:26	**rc_bpg_offset_5** Access: R/W
	25:21	**rc_max_qp_5**
	20:16	**rc_min_qp_5**
	15:10	**rc_bpg_offset_4** Access: R/W
	9:5	**rc_max_qp_4**
	4:0	**rc_min_qp_4**
1	31:26	**rc_bpg_offset_7** Access: R/W
	25:21	**rc_max_qp_7**
	20:16	**rc_min_qp_7**
	15:10	**rc_bpg_offset_6** Access: R/W
	9:5	**rc_max_qp_6**
	4:0	**rc_min_qp_6**

DSC_RC_RANGE_PARAMETERS_2

DSC_RC_RANGE_PARAMETERS_2	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	6B250h-6B257h
Name:	DSCA_RC_RANGE_PARAMETERS_2
ShortName:	DSCA_RC_RANGE_PARAMETERS_2
Power:	PG1
Reset:	soft
Address:	6BA50h-6BA57h
Name:	DSCC_RC_RANGE_PARAMETERS_2
ShortName:	DSCC_RC_RANGE_PARAMETERS_2
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:26	**rc_bpg_offset_9** Access: R/W
	25:21	**rc_max_qp_9**
	20:16	**rc_min_qp_9**
	15:10	**rc_bpg_offset_8** Access: R/W
	9:5	**rc_max_qp_8**
	4:0	**rc_min_qp_8**
1	31:26	**rc_bpg_offset_11** Access: R/W
	25:21	**rc_max_qp_11**
	20:16	**rc_min_qp_11**
	15:10	**rc_bpg_offset_10** Access: R/W
	9:5	**rc_max_qp_10**
	4:0	**rc_min_qp_10**

DSC_RC_RANGE_PARAMETERS_3

DSC_RC_RANGE_PARAMETERS_3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	6B258h-6B25Fh
Name:	DSCA_RC_RANGE_PARAMETERS_3
ShortName:	DSCA_RC_RANGE_PARAMETERS_3
Power:	PG1
Reset:	soft
Address:	6BA58h-6BA5Fh
Name:	DSCC_RC_RANGE_PARAMETERS_3
ShortName:	DSCC_RC_RANGE_PARAMETERS_3
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:26	**rc_bpg_offset_13** Access: R/W
	25:21	**rc_max_qp_13**
	20:16	**rc_min_qp_13**
	15:10	**rc_bpg_offset_12** Access: R/W
	9:5	**rc_max_qp_12**
	4:0	**rc_min_qp_12**
1	31:26	**Reserved**
	25:21	**Reserved**
	20:16	**Reserved**
	15:10	**rc_bpg_offset_14** Access: R/W
	9:5	**rc_max_qp_14**
	4:0	**rc_min_qp_14**

DSI_PHY_DW6

DSI_PHY_DW6

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000001
Access:	R/W
Size (in bits):	32
Address:	160018h-16001Bh
Name:	DSI_PHY_DW6
ShortName:	DSI_PHY_DW6
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:23	**Reserved** Format: MBZ
	22	**FORCE_HS_UPDATE** Forced update mode for HS ; Does not wait for any device state
	21	**DSI_HS_RCOMP_UPDATE** LNC clock lane update bit. When this bit is set RCOMP will update Clock lane with calibrated value when its data lane is in stop state. When it is clear it updates when clock lane itself in LP states
	20:19	**DSI_HS_TOGGLE_LIMIT_CREG_ENC** HS state machine toggle limit. Number of times RCOMP state machine will toggle before exiting. 00b: 6 toggles 01b: 4 toggles 10b: 8 toggles 11b: 10 toggles
	18:16	**DSI_HS_CALIB_LOOP_DELAY** Delay after applying a new RCOMP value to the AFE, before sampling the count up/down input from the AFE. At the start of each RCOMP calibration cycle, the state machine waits for 8x this delay before starting to sample the count up/down signal. 0h: 50-53ns 1h: 60ns 2h: 70-72s 3h: 80-83ns

DSI_PHY_DW6

		4h: 90ns 5h: 100-102ns 6h: 125-128ns 7h: 159ns
	15:9	**Reserved** Format: MBZ
	8	**HS_OVR_EN** HS override enable
	7:6	**Reserved** Format: MBZ
	5:1	**HS_OVR_VALUE** HS override values
	0	**HS_CALIB_EN** Enable HS calibration 1b: **[Default]** 0b:

DSI_PLL_CTL

DSI_PLL_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32

Address:	161000h-161003h
Name:	DSI PLL Control
ShortName:	DSI_PLL_CTL
Power:	PG0
Reset:	global

The register is used to control the frequency of the outputs from the MIPI DSI PLL.
The DSI_PLL_ENABLE register controls the MIPI DSI PLL enable.
The MIPI_CLOCK_CTL register controls additional dividers.

Restriction
Restriction : The fields must not be changed while the PLL is enabled.

DWord	Bit	Description
0	31:25	**Reserved** Format: MBZ
	24:18	**Output Ratio** Set the output clock ratio. Restriction : Display software must not change this field.
	17:16	**PVD Ratio** Set the post VCO divider ratio. 00b = 1 01b = 2 10b = 4 11b = 8 Restriction : Display software must not change this field.

DSI_PLL_CTL

15:14 Ref Ratio

Set the refclk ratio.

Value	Name
00b	Ref
01b	Ref/2
10b	Ref/4
11b	Ref/8

Restriction
Restriction : Display software must not change this field.

13 Force On

Force the PLL on.

Value	Name
0b	No Force
1b	Force On

Restriction
Restriction : Display software must not change this field.

12 Force Off

Force the PLL off.

Value	Name
0b	No Force
1b	Force Off

Restriction
Restriction : Display software must not change this field.

11:10 Freq Sel C

Frequency Select for DSI C clock

Value	Name	Description	Programming Notes
00b	16X	Non DSI	Restriction : This value must not be used when the PLL is enabled.
01b	8X	Divide 16X PLL output by 2	
10b	16X/3	Divide 16X PLL output by 3	
11b	4X	Divide 16X PLL output by 4	

DSI_PLL_CTL

	9:8	**Freq Sel A** Frequency Select for DSI A clock

Value	Name	Description	Programming Notes
00b	16X	Non DSI	Restriction : This value must not be used when the PLL is enabled.
01b	8X	Divide 16X PLL output by 2	
10b	16X/3	Divide 16X PLL output by 3	
11b	4X	Divide 16X PLL output by 4	

	7:0	**PLL Ratio**

Description
This field provides the feedback ratio for the PLL.
Values from 34d (22h) to 125d (7Dh) are allowed.

DSI_PLL_ENABLE

DSI_PLL_ENABLE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	46080h-46083h
Name:	DSI PLL Enable
ShortName:	DSI_PLL_ENABLE
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31	**PLL Enable** This field enables or disables the DSI PLL. Value / Name: 0b Disable; 1b Enable
	30	**PLL Lock** Access: RO This fields indicates the status of the DSI PLL lock. Value / Name: 0b Not locked or not enabled; 1b Locked
	29:0	**Reserved** Format: MBZ

DSI_RCOMP_CFG1

DSI_RCOMP_CFG1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32

Address:	16000Ch-16000Fh
Name:	DSI_RCOMP_CFG1
ShortName:	DSI_RCOMP_CFG1
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31	**mipA_dphy_defeature_en** This field must be set to 0x1 when enabling MIPI port A.
	30:28	**mipA_lane_count** This field specifies the number of lanes to be used for MIPI port A. This field is only used on BXT A0.

Value	Name
000b	0 lanes
001b	1 lane
010b	2 lanes
011b	3 lanes
100b	4 lanes

	27	**mipC_dphy_defeature_en** This field must be set to 0x1 when enabling MIPI port C.
	26:24	**mipC_lane_count** This field specifies the number of lanes to be used for MIPI port C. This field is only used on BXT A0.

Value	Name
000b	0 lanes
001b	1 lane
010b	2 lanes
011b	3 lanes
100b	4 lanes

	23:16	**Reserved**

Format:	MBZ

DSI_RCOMP_CFG1		
	15:13	**CZCLK_CLK_FREQ** C
	12:11	**RCOMP_CLK_FREQ**
	10	**Reserved** Format: MBZ
	9:6	**LP_P_RCOMP_OVR_SLEW**
	5	**Reserved** Format: MBZ
	4:1	**LP_N_RCOMP_OVR_SLEW**
	0	**LP_RCOMP_SLEW_OVR_EN**

DSSM

DSSM	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	51004h-51007h
Name:	Display Strap State
ShortName:	DSSM
Power:	PG0
Reset:	global

This register contains fuse and strap settings for display.
This register is not reset by FLR.

DWord	Bit	Description
0	31	**Spare 31**
	30	**Spare 30**
	29	**Spare 29**
	28	**Spare 28**
	27	**Spare 27**
	26	**Spare 26**
	25	**Spare 25**
	24	**Spare 24**
	23	**Spare 23**
	22	**Spare 22**
	21	**Spare 21**
	20	**Spare 20**
	19	**Spare 19**
	18	**Spare 18**
	17	**Spare 17**
	16	**Spare 16**
	15	**Spare 15**
	14	**Spare 14**
	13	**Spare 13**
	12	**Spare 12**
	11	**Spare 11**

DSSM

10	**Spare 10**
9	**Spare 9**
8	**Spare 8**
7	**Spare 7**
6	**Spare 6**
5	**Spare 5**
4	**Spare 4**
3	**Spare 3**
2	**LCPLL Unavail** This bit specifies the availability of some LCPLL output frequencies. **Value** / **Name** / **Description** 0b / Available / LCPLL available 1b / Not available / LCPLL not available
1	**Spare 1**
0	**DisplayPort A Present** **Description** This bit specifies whether the port was present during initalization. This strap state can also be read in the DDI_BUF_CTL_A 0x64000 register bit 0. There are no port presence straps on Broxton. Software should use alternate means to determine port presence. **Value** / **Name** / **Description** 0b / Not Present / Port not present 1b / Present / Port present

EU PAIR 1 PFET control register with lock

PFETCTL - EU PAIR 1 PFET control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0003000A
Size (in bits):	32
Address:	24688h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of EU PAIR 1 PFETCTL register are R/W 1 = All bits of EU PAIR 1 PFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:21	**Reserved** Access: RO Reserved
	20	**Power Well Status** Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	19	**Powergood timer error** Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	18:16	**Delay from enabling secondary PFETs to power good.** Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 320ns

PFETCTL - EU PAIR 1 PFET control register with lock

3'b100: 640ns
3'b101: 1280ns
3'b110: 2560ns
3'b111: 5120ns

Value	Name
011b	**[Default]**

15:13 **Time period last primay pfet strobe to secondary pfet strobe**

Access:	R/W Lock

Time period last primay pfet strobe to secondary pfet strobe
3'b000: 10ns (or 1 bclk)
3'b001: 20ns (or 2 bclk)
3'b010: 30ns (or 3 bclk)
3'b111: 80ns (or 8 bclk)

12:10 **Time period b/w two adjacent strobes**

Access:	R/W Lock

Time period b/w two adjacent strobes to the primary FETs
3'b000: 10ns (or 1 bclk)
3'b001: 20ns (or 2 bclk)
3'b010: 30ns (or 3 bclk)
3'b111: 80ns (or 8 bclk)

9:7 **FET setup margin from enable to strobe**

Access:	R/W Lock

Setup margin in design before sampling enable event at the first pre-charge sequencer/shift register flop
3'b000: 10ns (or 1 bclk)
3'b001: 20ns (or 2 bclk)
3'b010: 30ns (or 3 bclk)
3'b111: 80ns (or 8 bclk)

6:0 **Number of flops to enable primary FETs**

Default Value:	0001010b
Access:	R/W Lock

Number of flops to enable primary FETs. For a setting of N there will be N+1 total strobes generated
7'b0000000: 10 Flops to be strobed
7'b0000001: 11 Flops to be strobed
7'b0000010: 12 Flops to be strobed
7'b0001111: 26 Flops to be strobed

EU PAIR 2 PGFET control register with lock

PFETCTL - EU PAIR 2 PGFET control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0003000A
Size (in bits):	32
Address:	24708h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of EU PAIR 2 PGFETCTL register are R/W 1 = All bits of EU PAIR 2 PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (that is, writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:21	**Reserved** Access: RO Reserved
	20	**Power Well Status** Access: R/WC 0 = Well is powered Down 1 = Well is powered Up Once written to 1, the lock is set and cannot be cleared (that is, writing a 0 will not clear the lock). These bits are not reset on FLR.
	19	**Powergood timer error** Access: R/WC 0 = Well is powered Down 1 = Well is powered Up Once written to 1, the lock is set and cannot be cleared (that is, writing a 0 will not clear the lock). These bits are not reset on FLR.
	18:16	**Delay from enabling secondary PFETs to power good** Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 320ns 3'b100: 640ns

PFETCTL - EU PAIR 2 PGFET control register with lock

3'b101: 1280ns
3'b110: 2560ns
3'b111: 5120ns

Value	Name
011b	**[Default]**

15:13 **Time period last primay pfet strobe to secondary pfet strobe**

Access:	R/W Lock

Time period last primay pfet strobe to secondary pfet strobe
3'b000: 10ns (or 1 bclk)
3'b001: 20ns (or 2 bclk)
3'b010: 30ns (or 3 bclk)
3'b111: 80ns (or 8 bclk)

12:10 **Time period b/w two adjacent strobes**

Access:	R/W Lock

Time period b/w two adjacent strobes to the primary FETs
3'b000: 10ns (or 1 bclk)
3'b001: 20ns (or 2 bclk)
3'b010: 30ns (or 3 bclk)
3'b111: 80ns (or 8 bclk)

9:7 **FET setup margin from enable to strobe**

Access:	R/W Lock

Setup margin in design before sampling enable event at the first pre-charge sequencer/shift register flop
3'b000: 10ns (or 1 bclk)
3'b001: 20ns (or 2 bclk)
3'b010: 30ns (or 3 bclk)
3'b111: 80ns (or 8 bclk)

6:0 **Number of flops to enable primary FETs**

Default Value:	0001010b
Access:	R/W Lock

Number of flops to enable primary FETs. For a setting of N, there will be N+1 total strobes generated.
7'b0000000: 10 Flops to be strobed
7'b0000001: 11 Flops to be strobed
7'b0000010: 12 Flops to be strobed
7'b0001111: 26 Flops to be strobed

FENCE_LSB

FENCE_LSB	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	100000h
Name:	FENCE0_LSB
ShortName:	FENCE0_LSB
Address:	100008h
Name:	FENCE1_LSB
ShortName:	FENCE1_LSB
Address:	100010h
Name:	FENCE2_LSB
ShortName:	FENCE2_LSB
Address:	100018h
Name:	FENCE3_LSB
ShortName:	FENCE3_LSB
Address:	100020h
Name:	FENCE4_LSB
ShortName:	FENCE4_LSB
Address:	100028h
Name:	FENCE5_LSB
ShortName:	FENCE5_LSB
Address:	100030h
Name:	FENCE6_LSB
ShortName:	FENCE6_LSB
Address:	100038h
Name:	FENCE7_LSB
ShortName:	FENCE7_LSB
Address:	100040h
Name:	FENCE8_LSB
ShortName:	FENCE8_LSB
Address:	100048h
Name:	FENCE9_LSB

FENCE_LSB	
ShortName:	FENCE9_LSB
Address:	100050h
Name:	FENCE10_LSB
ShortName:	FENCE10_LSB
Address:	100058h
Name:	FENCE11_LSB
ShortName:	FENCE11_LSB
Address:	100060h
Name:	FENCE12_LSB
ShortName:	FENCE12_LSB
Address:	100068h
Name:	FENCE13_LSB
ShortName:	FENCE13_LSB
Address:	100070h
Name:	FENCE14_LSB
ShortName:	FENCE14_LSB
Address:	100078h
Name:	FENCE15_LSB
ShortName:	FENCE15_LSB
Address:	100080h
Name:	FENCE16_LSB
ShortName:	FENCE16_LSB
Address:	100088h
Name:	FENCE17_LSB
ShortName:	FENCE17_LSB
Address:	100090h
Name:	FENCE18_LSB
ShortName:	FENCE18_LSB
Address:	100098h
Name:	FENCE19_LSB
ShortName:	FENCE19_LSB
Address:	1000A0h
Name:	FENCE20_LSB
ShortName:	FENCE20_LSB

FENCE_LSB	
Address:	1000A8h
Name:	FENCE21_LSB
ShortName:	FENCE21_LSB
Address:	1000B0h
Name:	FENCE22_LSB
ShortName:	FENCE22_LSB
Address:	1000B8h
Name:	FENCE23_LSB
ShortName:	FENCE23_LSB
Address:	1000C0h
Name:	FENCE24_LSB
ShortName:	FENCE24_LSB
Address:	1000C8h
Name:	FENCE25_LSB
ShortName:	FENCE25_LSB
Address:	1000D0h
Name:	FENCE26_LSB
ShortName:	FENCE26_LSB
Address:	1000D8h
Name:	FENCE27_LSB
ShortName:	FENCE27_LSB
Address:	1000E0h
Name:	FENCE28_LSB
ShortName:	FENCE28_LSB
Address:	1000E8h
Name:	FENCE29_LSB
ShortName:	FENCE29_LSB
Address:	1000F0h
Name:	FENCE30_LSB
ShortName:	FENCE30_LSB
Address:	1000F8h
Name:	FENCE31_LSB
ShortName:	FENCE31_LSB
Fence Registers LSBs	

DWord	Bit	Description

FENCE_LSB

0	31:12	**FENCELO** Default Value: 000000h Access: R/W Bits 31:12 of the ending Graphics Address of the fence region. Fence regions must be aligned to a 4KB page. This address represents the last 4KB page of the fence region (Lower Bound is included in the fence region). Graphics Address is the offset within GMADR space.
	11:2	**RESERVED** Default Value: 000h Access: RO Reserved
	1	**TILE** Default Value: 0b Access: R/W This field specifies the spatial ordering of QW within tiles. 0b - Consecutive SWords (32B) sequenced in the X direction 1b - Consecutive OWords (16B) sequenced in the Y direction
	0	**FENCEVAL** Default Value: 0b Access: R/W This field specifies whether or not this fence register defines a fence region. 0b - FENCE INVALID 1b - FENCE VALID

FENCE_MSB

FENCE_MSB	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	100004h
Name:	FENCE0_MSB
ShortName:	FENCE0_MSB
Address:	10000Ch
Name:	FENCE1_MSB
ShortName:	FENCE1_MSB
Address:	100014h
Name:	FENCE2_MSB
ShortName:	FENCE2_MSB
Address:	10001Ch
Name:	FENCE3_MSB
ShortName:	FENCE3_MSB
Address:	100024h
Name:	FENCE4_MSB
ShortName:	FENCE4_MSB
Address:	10002Ch
Name:	FENCE5_MSB
ShortName:	FENCE5_MSB
Address:	100034h
Name:	FENCE6_MSB
ShortName:	FENCE6_MSB
Address:	10003Ch
Name:	FENCE7_MSB
ShortName:	FENCE7_MSB
Address:	100044h
Name:	FENCE8_MSB
ShortName:	FENCE8_MSB
Address:	10004Ch
Name:	FENCE9_MSB

FENCE_MSB	
ShortName:	FENCE9_MSB
Address:	100054h
Name:	FENCE10_MSB
ShortName:	FENCE10_MSB
Address:	10005Ch
Name:	FENCE11_MSB
ShortName:	FENCE11_MSB
Address:	100064h
Name:	FENCE12_MSB
ShortName:	FENCE12_MSB
Address:	10006Ch
Name:	FENCE13_MSB
ShortName:	FENCE13_MSB
Address:	100074h
Name:	FENCE14_MSB
ShortName:	FENCE14_MSB
Address:	10007Ch
Name:	FENCE15_MSB
ShortName:	FENCE15_MSB
Address:	100084h
Name:	FENCE16_MSB
ShortName:	FENCE16_MSB
Address:	10008Ch
Name:	FENCE17_MSB
ShortName:	FENCE17_MSB
Address:	100094h
Name:	FENCE18_MSB
ShortName:	FENCE18_MSB
Address:	10009Ch
Name:	FENCE19_MSB
ShortName:	FENCE19_MSB
Address:	1000A4h
Name:	FENCE20_MSB
ShortName:	FENCE20_MSB

FENCE_MSB

Address:	1000ACh
Name:	FENCE21_MSB
ShortName:	FENCE21_MSB
Address:	1000B4h
Name:	FENCE22_MSB
ShortName:	FENCE22_MSB
Address:	1000BCh
Name:	FENCE23_MSB
ShortName:	FENCE23_MSB
Address:	1000C4h
Name:	FENCE24_MSB
ShortName:	FENCE24_MSB
Address:	1000CCh
Name:	FENCE25_MSB
ShortName:	FENCE25_MSB
Address:	1000D4h
Name:	FENCE26_MSB
ShortName:	FENCE26_MSB
Address:	1000DCh
Name:	FENCE27_MSB
ShortName:	FENCE27_MSB
Address:	1000E4h
Name:	FENCE28_MSB
ShortName:	FENCE28_MSB
Address:	1000ECh
Name:	FENCE29_MSB
ShortName:	FENCE29_MSB
Address:	1000F4h
Name:	FENCE30_MSB
ShortName:	FENCE30_MSB
Address:	1000FCh
Name:	FENCE31_MSB
ShortName:	FENCE31_MSB

Fence Registers MSBs

DWord	Bit	Description

FENCE_MSB

0	31:12	**FENCEUP** Default Value: 00000000h Access: R/W Bits 31:12 of the ending Graphics Address of the fence region. Fence regions must be aligned to a 4KB page. This address represents the last 4KB page of the fence region (Upper Bound is included in the fence region). Graphics Address is the offset within GMADR space.
	11	**Reserved** Default Value: 0b Access: RO Reserved
	10:0	**Pitch** Default Value: 000h Access: R/W This field specifies the width (pitch) of the fence region in multiple of tile widths. For Tile X this field must be programmed to a multiple of 512B (003 is the minimum value) and for Tile Y this field must be programmed to a multiple of 128B (000 is the minimum value). 000h = 128B 001h = 256B 002h = 384B 003h = 512B 004h = 640B 005h = 768B 006h = 896B 007h = 1024B ... 3FFh = 128KB 4FFh = 160KB 5FFh = 192KB 6FFh = 224KB 7FFh = 256KB

FLT_RPT0

FLT_RPT0 - FLT_RPT0	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	124810h

GT uses this register to post VT-d faults

DWord	Bit	Description
0	31:12	**FI** Default Value: 00000h Access: R/W Fault Info.
	11:0	**RESERVED** Default Value: 000h Access: RO

FLT_RPT1

FLT_RPT1 - FLT_RPT1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	124814h
GT uses this register to post VT-d faults	

DWord	Bit	Description
0	31:0	**FI** Default Value: 00000000h Access: R/W Fault Info.

FLT_RPT2

FLT_RPT2 - FLT_RPT2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000010
Size (in bits):	32
Address:	124818h

GT uses this register to post VT-d faults

DWord	Bit	Description
0	31	**PP** Default Value: 0h Access: R/W PASID Present.
	30	**EXE** Default Value: 0h Access: R/W Execute Permission Requested.
	29	**PRIV** Default Value: 0h Access: R/W Privilege Mode Requested .
	28:16	**RESERVED** Default Value: 0000h Access: RO Reserved
	15:0	**Source ID** Default Value: 0010h Access: RO Source ID.

FLT_RPT3

FLT_RPT3 - FLT_RPT3		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	12481Ch	
GT uses this register to post VT-d faults		

DWord	Bit	Description
0	31	**F** Default Value: 0h Access: R/W Fault
	30	**T** Default Value: 0h Access: R/W Type
	29:28	**AT** Default Value: 0h Access: R/W Address Type
	27:8	**PN** Default Value: 00000h Access: R/W PASID Number
	7:0	**FR** Default Value: 0h Access: R/W Fault Reason

GFX_FLSH_CNT

GFX_FLSH_CNT - GFX_FLSH_CNT

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	101008h

Used to flush Gunit TLB

DWord	Bit	Description
0	31:1	**RESERVED** Default Value: 00000000h Access: RO Reserved
	0	**GfxFlshCntl** Default Value: 0b Access: WO Access type of this register is WO. A write to this bit flushes the Gfx TLB in GUNIT. The data associated with the write is discarded and a read return all 0s.

GMBUS0

GMBUS0	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	C5100h-C5103h
Name:	GMBUS0 Clock/Port Select
ShortName:	GMBUS0
Power:	PG1
Reset:	global

This register controls the clock rate of the serial bus and the device the controller is connected to.
This register should be configured before the first data valid bit is set.

DWord	Bit	Description
0	31:12	**Reserved** Format: MBZ
	11	**Reserved**
	10:8	**GMBUS Rate Select** This field selects the rate that the GMBUS will run at. It also defines the AC timing parameters used. Value / Name: 000b: 100 KHz 001b: 50 KHz Others: Reserved Restriction : It should only be changed between transfers when the GMBUS is idle.
	7	**Reserved** Format: MBZ
	6	**Reserved** Format: MBZ
	6	**Reserved** Format: MBZ
	5:3	**Reserved** Format: MBZ

<table>
<tr><th colspan="3">GMBUS0</th></tr>
<tr><td></td><td>2:0</td><td>Pin Pair Select
This field selects a GMBUS pin pair for use in the GMBUS communication.
See the table at the beginning of this section to determine which pin pairs are supported and their intended functions.
<table>
<tr><th>Value</th><th>Name</th></tr>
<tr><td>000b</td><td>None (Disabled)</td></tr>
<tr><td>001b</td><td>Pin Pair 1</td></tr>
<tr><td>010b</td><td>Pin Pair 2</td></tr>
<tr><td>011b</td><td>Pin Pair 3</td></tr>
</table></td></tr>
</table>

GMBUS1

GMBUS1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W Protect
Size (in bits):	32

Address:	C5104h-C5107h
Name:	GMBUS1 Command/Status
ShortName:	GMBUS1
Power:	PG1
Reset:	global

This register indicates the slave device address, register index, and when the data write is complete.
When the SW_CLR_INT bit is asserted, all writes to the GMBUS2, GMBUS3, and GMBUS4 registers are discarded. The GMBUS1 register writes to any other bit except the SW_CLR_INT are also lost.
Reads to these registers always work normally, regardless of the state of the SW_CLR_INT bit.

DWord	Bit	Description
0	31	**Software Clear Interrupt** Access: R/W (SW_CLR_INT) This bit must be clear for normal operation. Setting the bit then clearing it acts as local reset to the GMBUS controller. This bit is commonly used by software to clear a BUS_ERROR when a slave device delivers a NACK. **Value / Name / Description** 0b / Clear HW_RDY / If this bit is written as a zero when its current state is a one, will clear the HW_RDY bit and allows register writes to be accepted to the GMBUS registers (Write Protect Off). This bit is cleared to zero when an event causes the HW_RDY bit transition to occur. 1b / Assert HW_RDY / Asserted by software after servicing the GMBUS interrupt. Setting this bit causes the INT status bit to be cleared and asserts the HW_RDY bit (until this bit is written with a 0). When this bit is set, no writes to GMBUS registers will cause the contents to change with the exception of this bit which can be written.
	30	**Software Ready** (SW_RDY) Data handshake bit used in conjunction with HW_RDY bit. **Value / Name / Description** 0b / De-Assert / De-asserted via the assertion event for HW_RDY bit 1b / SW Assert / When asserted by software, results in de-assertion of HW_RDY bit

GMBUS1

29 Enable Timeout

(ENT) Enables timeout for slave response.

When this bit is enabled and the slave device response has exceeded the timeout period, the GMBUS Slave Stall Timeout Error interrupt bit is set.

Value	Name
0b	Disable
1b	Enable

28 Reserved

Format:	MBZ

27:25 Bus Cycle Select

GMBUS cycle will always consist of a START followed by Slave Address, followed by an optional read or write data phase.

A read cycle with an index will consist of a START followed by a Slave Address a WRITE indication and the INDEX and then a RESTART with a Slave Address and an optional read data phase.

The GMBUS cycle will terminate either with a STOP or by entering a wait state. The WAIT state is exited by generating a STOP or by starting another GMBUS cycle.

This can only cause a STOP to be generated if a GMBUS cycle is generated, the GMBUS is currently in a data phase, or it is in a WAIT phase.

The three bits can be decoded as follows:

27 = STOP generated

26 = INDEX used

25 = Cycle ends in a WAIT

Value	Name	Description
000b	No cycle	No GMBUS cycle is generated
001b	No Index, No Stop, Wait	GMBUS cycle is generated without an INDEX, with no STOP, and ends with a WAIT
010b	Reserved	Reserved
011b	Index, No Stop, Wait	GMBUS cycle is generated with an INDEX, with no STOP, and ends with a WAIT
100b	Gen Stop	Generates a STOP if currently in a WAIT or after the completion of the current byte if active
101b	No Index, Stop	GMBUS cycle is generated without an INDEX and with a STOP
110b	Reserved	Reserved
111b	Index, Stop	GMBUS cycle is generated with an INDEX and with a STOP

24:16 Total Byte Count

This determines the total number of bytes to be transferred during the DATA phase of a GMBUS cycle.

The DATA phase can be prematurely terminated by generating a STOP while in the DATA phase (see Bus Cycle Select).

Restriction

GMBUS1

	Restriction : Do not change the value of this field during GMBUS cycles transactions. The byte count must not be zero.
15:8	**8 bit Slave Register Index** (INDEX) This field specifies the 8-bits of index to be used for the generated bus write transaction or the index used for the WRITE portion of the WRITE/READ pair. It only has an effect if the enable Index bit is set. **Restriction** Restriction : Do not change the value of this field during GMBUS cycles transactions.
7:0	**Slave Address And Direction** Bits 7:1 = 7-bit GMBUS Slave Address: When a GMBUS cycle is to be generated using the Bus Cycle Select field, this field specifies the value of the slave address that is to be sent out. Bit 0 = Slave Direction Bit: When a GMBUS cycle is to be generated based on the Bus Cycle Select, this bit determines if the operation will be a read or a write. A read operation with the index enabled will perform a write with just the index followed by a re-start and a read. A 1 indicates that a Read from the slave device operation is to be performed. A 0 indicates that a Write to the slave device operation is to be performed.

Value	Name
00000001b	General Call Address
00000000b	Start Byte
0000001Xb	CBUS Address
11110XXXb	10-Bit Addressing
Others	Reserved

Programming Notes

For 10-bit slave address devices, set this field to 11110XXb (where the last two bits (XX) are the two MSBs of the 10-bit address) and the slave direction bit to a write, and set the first data byte to be the 8 LSBs of the 10-bit address.

GMBUS2

GMBUS2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000800
Access:	R/W Protect
Size (in bits):	32

Address:	C5108h-C510Bh
Name:	GMBUS2 Status
ShortName:	GMBUS2
Power:	PG1
Reset:	global

When the SW_CLR_INT bit is asserted, all writes to this register are discarded. Reads to this register always work normally regardless of the state of the SW_CLR_INT bit.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15	**INUSE** Software wishing to arbitrate for the GMBUS resource can poll this bit until it reads a zero and will then own usage of the GMBUS controller. This bit has no effect on the hardware, and is only used as semaphore among various independent software threads. **Value** / **Name** / **Description** 0b / GMBUS is Acquired / Reading a 0 indicates that GMBUS is now acquired and subsequent reads will now have this bit set. Writing a 0 has no effect. 1b / GMBUS in Use / Reading a 1 indicates that GMBUS is currently allocated to someone else and "In use". Writing a 1 indicates that the software has relinquished the GMBUS resource, which will reset the value to a 0.
	14	**Hardware Wait Phase** Access: RO Once in a WAIT_PHASE, the software can now choose to generate a STOP cycle or a repeated start (RESTART) cycle followed by another GMBUS transaction. Wait phase is entered at the end of the current transaction when that transaction is selected not to terminate with a STOP. **Value** / **Name** 0b / Not in a wait phase 1b / In wait phase

GMBUS2

13 Slave Stall Timeout Error

Access:	RO

This bit indicates that a slave stall timeout has occurred. It is tied to the Enable Timeout (ENT) bit.

Value	Name
0b	No Slave Timeout
1b	Slave Timeout

12 GMBUS Interrupt Status

Access:	RO

This bit indicates that an event that causes a GMBUS interrupt has occurred. The interrupt can be caused by one of the interrupt types enabled in the GMBUS4 register.

Value	Name
0b	No Interrupt
1b	Interrupt

11 Hardware Ready

Access:	RO

(HW_RDY) This provides a method of detecting when software can proceed with the next step in a sequence of GMBUS operations.
This data handshake bit is used in conjunction with the SW_RDY bit.
When this bit is asserted by the GMBUS controller, it results in the de-assertion of the SW_RDY bit.
This bit resumes to normal operation when the SW_CLR_INT bit is written to a 0.

Value	Name	Description
0b	0	Condition required for assertion has not occurred, or when this bit is a one and: - SW_RDY bit has been asserted - During a GMBUS read transaction, after the each read of the data register - During a GMBUS write transaction, after each write of the data register - SW_CLR_INT bit has been cleared
1b	1 **[Default]**	This bit is asserted under the following conditions: - After a reset or when the transaction is aborted by the setting of the SW_CLR_INT bit - When an active GMBUS cycle has terminated with a STOP - When during a GMBUS write transaction, the data register needs and can accept another four bytes of data - During a GMBUS read transaction, this bit is asserted when the data register has four bytes of new data or the read transaction DATA phase is complete and the data register contains the last few bytes of the read data

GMBUS2

10 NAK Indicator

Access:	RO

MAK is indicated by hardware if any expected device acknowledge is not received from the slave within the timeout.

Value	Name
0b	No bus error
1b	NAK occurred

9 GMBUS Active

Access:	RO

This is a status bit that indicates whether the GMBUS controller is in an IDLE state or not. Active states are the START, ADDRESS, INDEX, DATA, WAIT, or STOP Phase.

Value	Name
0b	Idle
1b	Active

8:0 Current Byte Count

Access:	RO

Can be used to determine the number of bytes currently transmitted/received by the GMBUS controller hardware.
Hardware sets it to zero at the start of a GMBUS transaction data transfer and increments it after the completion of each byte of the data phase.

Restriction
Restriction: Because reads have internal storage, the byte count on a read operation may be ahead of the data that has been accepted from the data register.

GMBUS3

GMBUS3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W Protect
Size (in bits):	32
Double Buffer Update Point:	HW_RDY
Address:	C510Ch-C510Fh
Name:	GMBUS3 Data Buffer
ShortName:	GMBUS3
Power:	PG1
Reset:	global

This is the data read/write register. This register is double buffered.
Bit 0 is the first bit sent or read, bit 7 is the 8th bit sent or read, all the way through bit 31 being the 32nd bit sent or read.
For GMBUS write operations with a non-zero byte count, this register should be written with the data before the GMBUS cycle is initiated.
For byte counts that are greater than four bytes, this register will be written with subsequent data only after the HW_RDY status bit is set indicating that the register is now ready for additional data.
When the SW_CLR_INT bit is asserted, all writes to this register are discarded.
For GMBUS read operations, software should wait until the HW_RDY bit indicates that the register contains the next set of valid read data before reading this register.

DWord	Bit	Description
0	31:24	**Data Byte 3**
	23:16	**Data Byte 2**
	15:8	**Data Byte 1**
	7:0	**Data Byte 0**

GMBUS4

GMBUS4

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W Protect
Size (in bits):	32
Address:	C5110h-C5113h
Name:	GMBUS4 Interrupt Mask
ShortName:	GMBUS4
Power:	PG1
Reset:	global

When the SW_CLR_INT bit is asserted, all writes to this register are discarded. Reads to this register always work normally regardless of the state of the SW_CLR_INT bit.

DWord	Bit	Description
0	31:5	**Reserved** Format: MBZ
	4:0	**Interrupt Mask** This field specifies which GMBUS interrupts events may contribute to the setting of GMBUS interrupt status bit in the second level interrupt status register. For writes, the HW Ready interrupt indicates that software can write the next DWORD. It does NOT mean that the transfer of data to the slave device has completed. The HW Ready interrupt may be used for gmbus write cycles only to detect when to write the next DWORD after the first two DWORDs have been written to GMBUS3. The IDLE or HW wait interrupt may be used to detect the end of writing data to the slave device. For reads, the HWRDY interrupt indicates the arrival of the next dword.

Value	Name
0XXXXb	Slave Stall Timeout Interrupt Disable
1XXXXb	Slave Stall Timeout Interrupt Enable
X0XXXb	NAK Interrupt Disable
X1XXXb	NAK Interrupt Enable
XX0XXb	Idle Interrupt Disable
XX1XXb	Idle Interrupt Enable
XXX0Xb	HW Wait Interrupt (cycle without a stop has completed) Disable
XXX1Xb	HW Wait Interrupt (cycle without a stop has completed) Enable
XXXX0b	HW Ready (Data transferred) Interrupt Disable
XXXX1b	HW Ready (Data transferred) Interrupt Enable

GMBUS5

GMBUS5		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	C5120h-C5123h	
Name:	GMBUS5 2 Byte Index	
ShortName:	GMBUS5	
Power:	PG1	
Reset:	global	

This register provides a method for the software indicate to the GMBUS controller the 2 byte device index.

DWord	Bit	Description
0	31	**2 Byte Index Enable** When this bit is set to 1, then bits 15:0 are used as the index. Bits 15:8 are used in the first byte which is the most significant index bits. The slave index in the GMBUS1<15:8> are ignored. Bits 7:0 are used in the second byte which is the least significant index bits.
	30:16	**Reserved** Format: MBZ
	15:0	**2 Byte Slave Index** This is the 2 byte index used in all GMBUS accesses when 2 Byte Index Enable is set to 1.

GMCH Graphics Control

GGC_0_0_0_PCI - GMCH Graphics Control

Register Space:	PCI: 0/0/0
Source:	BSpec
Default Value:	0x00000500
Size (in bits):	16
Address:	00050h

GMCH Graphics Control Register.

DWord	Bit	Description
0	15:8	**Graphics Mode Select** Default Value: 00000101b Access: R/W Lock This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled. BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0. BIOS Requirement: Given new sizes allow down to 8MB allocation, BIOS has to ensure there is sufficient space for WOPCM and basic GFX Stolen functions. 00h:0MB 01h:32MB 02h:64MB 03h:96MB 04h:128MB 05h:160MB (default) 06h:192MB 07h:224MB 08h:256MB 09h:288MB 0Ah:320MB 0Bh:352MB 0Ch:384MB 0Dh:416MB 0Eh:448MB 0Fh:480MB 10h:512MB 11h - 1Fh: Reserved 20h:1024MB 21h - 2Fh: Reserved 30h:1536MB 31h - 3Fh: Reserved 40h: 2048MB

GGC_0_0_0_PCI - GMCH Graphics Control

		41h - EFh: Reserved F0h: 4MB F1h: 8MB F2h: 12MB F3h: 16MB F4h: 20MB F5h: 24MB F6h: 28MB F7h: 32MB F8h: 36MB F9h: 40MB FAh: 44MB FBh: 48MB FCh: 52MB FDh: 56MB FEh: 60MB FFh: Reserved Hardware functionality in case of programming this value to Reserved is not guaranteed.
	7:6	**GTT Graphics Memory Size** Default Value: 00b Access: R/W Lock This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware will derive the base of GSM from DSM only using the GSM size programmed in the register. Hardware functionality in case of programming this value to Reserved is not guaranteed. 0x0: No Preallocated Memory 0x1: 2MB of Preallocated Memory 0x2: 4MB of Preallocated Memory 0x3: 8MB of Preallocated Memory
	5:3	**RESERVED** Default Value: 000b Access: RO Reserved
	2	**Versatile Acceleration Mode Enable** Default Value: 0b Access: R/W Lock Enables the use of the iGFX engines for Versatile Acceleration. 0 - iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h.

GGC_0_0_0_PCI - GMCH Graphics Control

		1 - iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 048000h.
	1	**IGD VGA Disable** Default Value: 0b Access: R/W Lock 0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub- Class Code field within Device 2 function 0 Class Code register is 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field pre-allocates no memory. This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override (CAPID0_A[IGD] = 1) or via a register (DEVEN[3] = 0).
	0	**GGC Lock** Default Value: 0b Access: R/W Key Lock When set to 1b, this bit will lock all bits in this register.

GPIO_CTL

GPIO_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000808
Access:	R/W
Size (in bits):	32
Address:	C5014h-C5017h
Name:	GPIO Control 1
ShortName:	GPIO_CTL_1
Power:	PG1
Reset:	global
Address:	C5018h-C501Bh
Name:	GPIO Control 2
ShortName:	GPIO_CTL_2
Power:	PG1
Reset:	global
Address:	C501Ch-C501Fh
Name:	GPIO Control 3
ShortName:	GPIO_CTL_3
Power:	PG1
Reset:	global

The register controls a pair of pins that can be used for general purpose control, but usually is designated for specific functions according to the requirements of the device and the system that the device is in. Each pin of the two pin pair is designated as a clock or data for descriptive purposes. See the table at the beginning of this section to determine which pin pairs are supported and their intended functions. Board design variations are possible and would affect the usage of these pins. There are multiple instances of this register to support each of the GPIO pin pairs.

DWord	Bit	Description
0	31:13	**Reserved** Format: MBZ
	12	**GPIO Data In** Default Value: Ub Undefined (read only, depends on I/O pin) Access: RO This is the value that is sampled on the GPIO_Data pin as an input.

GPIO_CTL

11 GPIO Data Value

Default Value:	1b
Access:	R/W

This is the value that should be place on the GPIO Data pin as an output.
This value is only written into the register if GPIO DATA MASK is also asserted.
The value will appear on the pin if this data value is actually written to this register and the GPIO Data DIRECTION VALUE contains a value that will configure the pin as an output.
The default of '1' mimics the I2C external pull-ups.

10 GPIO Data Mask

Access:	WO

This is a mask bit to determine whether the GPIO DATA VALUE bit should be written into the register.

Value	Name
0b	Dot not write
1b	Write

9 GPIO Data Direction Value

Access:	R/W

This is the value that should be used to define the output enable of the GPIO Data pin.
This value is only written into the register if GPIO Data DIRECTION MASK is also asserted.
The value that will appear on the pin is defined by what is in the register for the GPIO DATA VALUE bit.

Value	Name
0b	Input
1b	Output

8 GPIO Data Direction Mask

Access:	WO

This is a mask bit to determine whether the GPIO Data DIRECTION VALUE bit should be written into the register.

Value	Name
0b	Dot not write
1b	Write

7:5 Reserved

Format:	MBZ

4 GPIO Clock Data In

Default Value:	Ub Undefined (read only, depends on I/O pin)
Access:	RO

This is the value that is sampled on the GPIO Clock pin as an input.

GPIO_CTL

	3	**GPIO Clock Data Value** Default Value: 1b Access: R/W This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if GPIO Clock DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Clock DIRECTION VALUE contains a value that will configure the pin as an output. The default of '1' mimics the I2C external pull-ups.
	2	**GPIO Clock Data Mask** Access: WO This is a mask bit to determine whether the GPIO Clock DATA VALUE bit should be written into the register. **Value** / **Name** 0b / Dot not write 1b / Write
	1	**GPIO Clock Direction Value** Access: R/W This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if GPIO Clock DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO Clock DATA VALUE bit. **Value** / **Name** 0b / Input 1b / Output
	0	**GPIO Clock Direction Mask** Access: WO This is a mask bit to determine whether the GPIO Clock DIRECTION VALUE bit should be written into the register. **Value** / **Name** 0b / Dot not write 1b / Write

Graphics Memory Range Address

GMADR_0_2_0_PCI - Graphics Memory Range Address

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x0000000C, 0x00000000
Size (in bits):	64
Address:	00018h

GMADR is the PCI aperture used by S/W to access tiled GFX surfaces in a linear fashion.

DWord	Bit	Description
0	63:39	**Reserved for Memory Base Address** Default Value: 0000000000000000000000000b Access: R/W Must be set to 0 since addressing above 512GB is not supported.
	38:32	**Memory Base Address** Default Value: 0000000b Access: R/W Set by the OS, these bits correspond to address signals [38:32].
	31	**4096 MB Address Mask** Default Value: 0b Access: R/W Lock This bit is either part of the Memory Base Address (R/W) or part of Address Mask (RO) depending on the value of MSAC.APSZ. RO and forced to 0 when MSAC.APSZ >= 4096MB. (i.e. MSAC.APSZ[4]=1)
	30	**2048 MB Address Mask** Default Value: 0b Access: R/W Lock This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ. RO and forced to 0 when MSAC.APSZ >= 2048MB. (i.e. MSAC.APSZ[3]=1)
	29	**1024 MB Address Mask** Default Value: 0b Access: R/W Lock This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ. RO and forced to 0 when MSAC.APSZ >= 1024MB. (i.e. MSAC.APSZ[2]=1)

GMADR_0_2_0_PCI - Graphics Memory Range Address

28	**512MB Address Mask** Default Value: 0b Access: R/W Lock This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ. RO and forced to 0 when MSAC.APSZ >= 512MB. (i.e. MSAC.APSZ[1]=1)
27	**256 MB Address Mask** Default Value: 0b Access: R/W Lock This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ. RO and forced to 0 when MSAC.APSZ >= 256MB. (i.e. MSAC.APSZ[0]=1)
26:4	**Address Mask** Default Value: 00000000000000000000000b Access: RO Hardwired to 0s to indicate at least 128MB address range.
3	**Prefetchable Memory** Default Value: 1b Access: RO Hardwired to 1 to enable prefetching.
2:1	**Memory Type** Default Value: 10b Access: RO Hardwired to 2h to indicate 64 bit base address.
0	**Memory/IO Space** Default Value: 0b Access: RO Hardwired to 0 to indicate memory space.

Graphics MOCS Register0

GFX_MOCS_0 - Graphics MOCS Register0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030
Size (in bits):	32
Address:	0C800h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

GFX_MOCS_0 - Graphics MOCS Register0

7 — Enable Skip Caching

Default Value:	0b
Access:	R/W

Enable for the Skip cache mechanism
0: Not enabled
1: Enabled for LLC

6 — Dont allocate on miss

Default Value:	0b
Access:	R/W

Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM).
0: Allocate on MISS (normal cache behavior)
1: Do NOT allocate on MISS

5:4 — LRU management

Default Value:	11b
Access:	R/W

This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2,1, or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches.
11: Good chance of generating hits.
10: Poor chance of generating hits
01: Don't change the LRU if it is a HIT
00: Reserved

3:2 — Target Cache

Default Value:	00b
Access:	R/W

This field allows the choice of LLC vs eLLC for caching
00: eLLC Only
01: LLC Only
10: LLC/eLLC Allowed
11: LLC/eLLC Allowed

1:0 — LLC/eDRAM cacheability control

Default Value:	00b
Access:	R/W

Memory type information used in LLC/eDRAM.
00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)
01: Uncacheable (UC) - non-cacheable
10: Writethrough (WT)
11: Writeback (WB)

Graphics MOCS Register1

GFX_MOCS_1 - Graphics MOCS Register1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034
Size (in bits):	32
Address:	0C804h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target

GFX_MOCS_1 - Graphics MOCS Register1

	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2,1, or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register2

GFX_MOCS_2 - Graphics MOCS Register2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038
Size (in bits):	32
Address:	0C808h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target

GFX_MOCS_2 - Graphics MOCS Register2

		Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2,1, or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_2 - Graphics MOCS Register2		
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register3

GFX_MOCS_3 - Graphics MOCS Register3

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031
Size (in bits):	32
Address:	0C80Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target

GFX_MOCS_3 - Graphics MOCS Register3

		Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_3 - Graphics MOCS Register3		
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register4

GFX_MOCS_4 - Graphics MOCS Register4

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0C810h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target

GFX_MOCS_4 - Graphics MOCS Register4

		Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_4 - Graphics MOCS Register4		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register5

GFX_MOCS_5 - Graphics MOCS Register5

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0C814h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_5 - Graphics MOCS Register5

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_5 - Graphics MOCS Register5

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register6

GFX_MOCS_6 - Graphics MOCS Register6

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0C818h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved

GFX_MOCS_6 - Graphics MOCS Register6

10:8 Skip Caching control

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is don't care
Bit[8]=1: address bit[9] needs to be "0" to cache in target
Bit[9]=1: address bit[10] needs to be "0" to cache in target
Bit[10]=1: address bit[11] needs to be "0" to cache in target

7 Enable Skip Caching

Default Value:	0b
Access:	R/W

Enable for the Skip cache mechanism
0: Not enabled
1: Enabled for LLC

6 Dont allocate on miss

Default Value:	0b
Access:	R/W

Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM).
0: Allocate on MISS (normal cache behavior)
1: Do NOT allocate on MISS

5:4 LRU management

Default Value:	11b
Access:	R/W

This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches.
11: Good chance of generating hits.
10: Poor chance of generating hits
01: Don't change the LRU if it is a HIT
00: Reserved

GFX_MOCS_6 - Graphics MOCS Register6

	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register7

GFX_MOCS_7 - Graphics MOCS Register7

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0C81Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_7 - Graphics MOCS Register7

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_7 - Graphics MOCS Register7

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register8

GFX_MOCS_8 - Graphics MOCS Register8

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0C820h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved

GFX_MOCS_8 - Graphics MOCS Register8

10:8 Skip Caching control

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is don't care
Bit[8]=1: address bit[9] needs to be "0" to cache in target
Bit[9]=1: address bit[10] needs to be "0" to cache in target
Bit[10]=1: address bit[11] needs to be "0" to cache in target

7 Enable Skip Caching

Default Value:	0b
Access:	R/W

Enable for the Skip cache mechanism
0: Not enabled
1: Enabled for LLC

6 Dont allocate on miss

Default Value:	0b
Access:	R/W

Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM).
0: Allocate on MISS (normal cache behavior)
1: Do NOT allocate on MISS

5:4 LRU management

Default Value:	11b
Access:	R/W

This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches.
11: Good chance of generating hits.
10: Poor chance of generating hits
01: Don't change the LRU if it is a HIT
00: Reserved

GFX_MOCS_8 - Graphics MOCS Register8

	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register9

GFX_MOCS_9 - Graphics MOCS Register9

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0C824h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_9 - Graphics MOCS Register9

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_9 - Graphics MOCS Register9

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register10

GFX_MOCS_10 - Graphics MOCS Register10

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0C828h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved

GFX_MOCS_10 - Graphics MOCS Register10

	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved

GFX_MOCS_10 - Graphics MOCS Register10

	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register11

GFX_MOCS_11 - Graphics MOCS Register11

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0C82Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_11 - Graphics MOCS Register11

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_11 - Graphics MOCS Register11		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register12

GFX_MOCS_12 - Graphics MOCS Register12

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0C830h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved

GFX_MOCS_12 - Graphics MOCS Register12

	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved

GFX_MOCS_12 - Graphics MOCS Register12

	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register13

GFX_MOCS_13 - Graphics MOCS Register13

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0C834h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_13 - Graphics MOCS Register13

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_13 - Graphics MOCS Register13		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register14

GFX_MOCS_14 - Graphics MOCS Register14

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0C838h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_14 - Graphics MOCS Register14

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_14 - Graphics MOCS Register14

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register15

GFX_MOCS_15 - Graphics MOCS Register15

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0C83Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_15 - Graphics MOCS Register15

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_15 - Graphics MOCS Register15		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register16

GFX_MOCS_16 - Graphics MOCS Register16

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030
Size (in bits):	32
Address:	0C840h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_16 - Graphics MOCS Register16

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_16 - Graphics MOCS Register16

	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register17

GFX_MOCS_17 - Graphics MOCS Register17

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034
Size (in bits):	32
Address:	0C844h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_17 - Graphics MOCS Register17

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_17 - Graphics MOCS Register17

	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register18

GFX_MOCS_18 - Graphics MOCS Register18

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038
Size (in bits):	32
Address:	0C848h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_18 - Graphics MOCS Register18

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_18 - Graphics MOCS Register18		
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register19

GFX_MOCS_19 - Graphics MOCS Register19

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031
Size (in bits):	32
Address:	0C84Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_19 - Graphics MOCS Register19

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_19 - Graphics MOCS Register19		
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register20

GFX_MOCS_20 - Graphics MOCS Register20

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0C850h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_20 - Graphics MOCS Register20

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_20 - Graphics MOCS Register20		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register21

GFX_MOCS_21 - Graphics MOCS Register21

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0C854h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_21 - Graphics MOCS Register21

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_21 - Graphics MOCS Register21

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register22

GFX_MOCS_22 - Graphics MOCS Register22

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0C858h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_22 - Graphics MOCS Register22

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_22 - Graphics MOCS Register22

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register23

GFX_MOCS_23 - Graphics MOCS Register23

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0C85Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_23 - Graphics MOCS Register23

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_23 - Graphics MOCS Register23		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register24

GFX_MOCS_24 - Graphics MOCS Register24

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0C860h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_24 - Graphics MOCS Register24

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_24 - Graphics MOCS Register24

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register25

GFX_MOCS_25 - Graphics MOCS Register25

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0C864h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_25 - Graphics MOCS Register25

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_25 - Graphics MOCS Register25		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register26

GFX_MOCS_26 - Graphics MOCS Register26

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0C868h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_26 - Graphics MOCS Register26

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_26 - Graphics MOCS Register26

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register27

GFX_MOCS_27 - Graphics MOCS Register27

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0C86Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_27 - Graphics MOCS Register27

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_27 - Graphics MOCS Register27		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register28

GFX_MOCS_28 - Graphics MOCS Register28

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0C870h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_28 - Graphics MOCS Register28

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_28 - Graphics MOCS Register28		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register29

GFX_MOCS_29 - Graphics MOCS Register29

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0C874h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_29 - Graphics MOCS Register29

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_29 - Graphics MOCS Register29		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register30

GFX_MOCS_30 - Graphics MOCS Register30

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0C878h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_30 - Graphics MOCS Register30

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_30 - Graphics MOCS Register30		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register31

GFX_MOCS_31 - Graphics MOCS Register31

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0C87Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_31 - Graphics MOCS Register31

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_31 - Graphics MOCS Register31		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register32

GFX_MOCS_32 - Graphics MOCS Register32

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030
Size (in bits):	32
Address:	0C880h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_32 - Graphics MOCS Register32

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_32 - Graphics MOCS Register32		
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register33

GFX_MOCS_33 - Graphics MOCS Register33

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034
Size (in bits):	32
Address:	0C884h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_33 - Graphics MOCS Register33

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_33 - Graphics MOCS Register33		
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register34

GFX_MOCS_34 - Graphics MOCS Register34

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038
Size (in bits):	32
Address:	0C888h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_34 - Graphics MOCS Register34

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_34 - Graphics MOCS Register34

	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register35

GFX_MOCS_35 - Graphics MOCS Register35

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031
Size (in bits):	32
Address:	0C88Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_35 - Graphics MOCS Register35

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_35 - Graphics MOCS Register35		
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register36

GFX_MOCS_36 - Graphics MOCS Register36

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0C890h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_36 - Graphics MOCS Register36

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_36 - Graphics MOCS Register36

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register37

GFX_MOCS_37 - Graphics MOCS Register37

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0C894h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_37 - Graphics MOCS Register37

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_37 - Graphics MOCS Register37		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register38

GFX_MOCS_38 - Graphics MOCS Register38

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0C898h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_38 - Graphics MOCS Register38

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_38 - Graphics MOCS Register38		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register39

GFX_MOCS_39 - Graphics MOCS Register39

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0C89Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_39 - Graphics MOCS Register39

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_39 - Graphics MOCS Register39		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register40

GFX_MOCS_40 - Graphics MOCS Register40

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0C8A0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_40 - Graphics MOCS Register40

Bit[8]=1: address bit[9] needs to be "0" to cache in target
Bit[9]=1: address bit[10] needs to be "0" to cache in target
Bit[10]=1: address bit[11] needs to be "0" to cache in target

7 Enable Skip Caching

Default Value:	0b
Access:	R/W

Enable for the Skip cache mechanism
0: Not enabled
1: Enabled for LLC

6 Dont allocate on miss

Default Value:	0b
Access:	R/W

Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM).
0: Allocate on MISS (normal cache behavior)
1: Do NOT allocate on MISS

5:4 LRU management

Default Value:	11b
Access:	R/W

This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches.
11: Good chance of generating hits.
10: Poor chance of generating hits
01: Don't change the LRU if it is a HIT
00: Reserved

3:2 Target Cache

Default Value:	01b
Access:	R/W

This field allows the choice of LLC vs eLLC for caching
00: eLLC Only
01: LLC Only
10: LLC/eLLC Allowed
11: LLC/eLLC Allowed

GFX_MOCS_40 - Graphics MOCS Register40

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register41

GFX_MOCS_41 - Graphics MOCS Register41

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0C8A4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_41 - Graphics MOCS Register41

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_41 - Graphics MOCS Register41		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register42

GFX_MOCS_42 - Graphics MOCS Register42

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0C8A8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_42 - Graphics MOCS Register42

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_42 - Graphics MOCS Register42

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register43

GFX_MOCS_43 - Graphics MOCS Register43

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0C8ACh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_43 - Graphics MOCS Register43

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_43 - Graphics MOCS Register43		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register44

GFX_MOCS_44 - Graphics MOCS Register44

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0C8B0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_44 - Graphics MOCS Register44

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_44 - Graphics MOCS Register44		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register45

GFX_MOCS_45 - Graphics MOCS Register45

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0C8B4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_45 - Graphics MOCS Register45

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_45 - Graphics MOCS Register45		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register46

GFX_MOCS_46 - Graphics MOCS Register46

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0C8B8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_46 - Graphics MOCS Register46

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_46 - Graphics MOCS Register46

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register47

GFX_MOCS_47 - Graphics MOCS Register47

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0C8BCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_47 - Graphics MOCS Register47

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_47 - Graphics MOCS Register47		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register48

GFX_MOCS_48 - Graphics MOCS Register48

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030
Size (in bits):	32
Address:	0C8C0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_48 - Graphics MOCS Register48

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_48 - Graphics MOCS Register48

	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register49

GFX_MOCS_49 - Graphics MOCS Register49

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034
Size (in bits):	32
Address:	0C8C4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_49 - Graphics MOCS Register49

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_49 - Graphics MOCS Register49		
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register50

GFX_MOCS_50 - Graphics MOCS Register50

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038
Size (in bits):	32
Address:	0C8C8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_50 - Graphics MOCS Register50

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_50 - Graphics MOCS Register50

	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register51

GFX_MOCS_51 - Graphics MOCS Register51

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031
Size (in bits):	32
Address:	0C8CCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_51 - Graphics MOCS Register51

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_51 - Graphics MOCS Register51

	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register52

GFX_MOCS_52 - Graphics MOCS Register52

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0C8D0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_52 - Graphics MOCS Register52

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_52 - Graphics MOCS Register52		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register53

GFX_MOCS_53 - Graphics MOCS Register53

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0C8D4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_53 - Graphics MOCS Register53

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_53 - Graphics MOCS Register53

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register54

GFX_MOCS_54 - Graphics MOCS Register54

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0C8D8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_54 - Graphics MOCS Register54

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_54 - Graphics MOCS Register54

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register55

GFX_MOCS_55 - Graphics MOCS Register55

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0C8DCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_55 - Graphics MOCS Register55

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_55 - Graphics MOCS Register55		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register56

GFX_MOCS_56 - Graphics MOCS Register56

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0C8E0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_56 - Graphics MOCS Register56

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_56 - Graphics MOCS Register56

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register57

GFX_MOCS_57 - Graphics MOCS Register57

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0C8E4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_57 - Graphics MOCS Register57

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_57 - Graphics MOCS Register57		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register58

GFX_MOCS_58 - Graphics MOCS Register58

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0C8E8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_58 - Graphics MOCS Register58

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_58 - Graphics MOCS Register58

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register59

GFX_MOCS_59 - Graphics MOCS Register59

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0C8ECh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_59 - Graphics MOCS Register59

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_59 - Graphics MOCS Register59

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register60

GFX_MOCS_60 - Graphics MOCS Register60

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0C8F0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_60 - Graphics MOCS Register60

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_60 - Graphics MOCS Register60

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register61

GFX_MOCS_61 - Graphics MOCS Register61

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0C8F4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_61 - Graphics MOCS Register61

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_61 - Graphics MOCS Register61

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register62

GFX_MOCS_62 - Graphics MOCS Register62

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0C8F8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_62 - Graphics MOCS Register62

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_62 - Graphics MOCS Register62

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics MOCS Register63

GFX_MOCS_63 - Graphics MOCS Register63

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0C8FCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

GFX_MOCS_63 - Graphics MOCS Register63

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

GFX_MOCS_63 - Graphics MOCS Register63

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Graphics System Event

GSE_0_2_0_PCI - Graphics System Event			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	000E4h		
This register can be accessed by either Byte, Word, or Dword PCI config cycles. A write to this register will cause the Graphics System Event display interrupt if it is enabled and unmasked in the display interrupt registers.			
DWord	**Bit**	**Description**	
0	31:24	**GSE Scratch Trigger 3**	
		Default Value:	00000000b
		Access:	R/W
	23:16	**GSE Scratch Trigger 2**	
		Default Value:	00000000b
		Access:	R/W
	15:8	**GSE Scratch Trigger 1**	
		Default Value:	00000000b
		Access:	R/W
	7:0	**GSE Scratch Trigger 0**	
		Default Value:	00000000b
		Access:	R/W

Graphics Translation Table Memory Mapped Range Address

GTTMMADR_0_2_0_PCI - Graphics Translation Table Memory Mapped Range Address

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000004, 0x00000000
Size (in bits):	64
Address:	00010h

This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. The range requires 16 MB combined for MMIO and Global GTT aperture, with 2MB of that used by MMIO, 6MB reserved, and 8MB used by GTT. GTTADR will begin at (GTTMMADR + 8 MB) while the MMIO base address will be the same as GTTMMADR. The region between (GTTMMADR + 2MB) - (GTTMMADR + 8MB) is reserved. For the Global GTT, this range is defined as a memory BAR in graphics device config space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT memory area. The device snoops writes to this region in order to invalidate any cached translations within the various TLB's implemented on-chip. The allocation is for 16MB and the base address is defined by bits [38:24].

DWord	Bit	Description
0	63:39	**Reserved for Memory Base Address** Default Value: 0000000000000000000000000b Access: R/W Must be set to 0 since addressing above 512GB is not supported.
	38:24	**Memory Base Address** Default Value: 000000000000000b Access: R/W Set by the OS, these bits correspond to address signals [38:24].
	23:4	**Address Mask** Default Value: 00000000000000000000b Access: RO Hardwired to 0s to indicate at least 16MB address range.
	3	**Prefetchable Memory** Default Value: 0b Access: RO Hardwired to 0 to prevent prefetching.

GTTMMADR_0_2_0_PCI - Graphics Translation Table Memory Mapped Range Address

	2:1	**Memory Type** Default Value: 10b Access: RO Hardwired to 2h to indicate 64 bit base address.
	0	**Memory/IO Space** Default Value: 0b Access: RO Hardwired to 0 to indicate memory space.

GT_FLUSH_BCLD_ACK

GT_FLUSH_BCLD_ACK - GT_FLUSH_BCLD_ACK

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	030C0h

GT writes a '1 to this bit to acknowledge PRMRR range registers are loaded into GT.
This register is a LOCAL CR register and not an MMIO register

DWord	Bit	Description
0	31:1	**RESERVED** Default Value: 00000000h Access: RO Reserved
	0	**ACK** Default Value: 0b Access: R/W GT Boot Context Load Ack

GT_RELOAD_FLUSH

GT_RELOAD_FLUSH - GT_RELOAD_FLUSH

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	030B0h

Ucode writes a '1 to bits 0 which triggers GT to flush and re-load PRMRR range registers.
This register is a LOCAL CR register and not an MMIO register

DWord	Bit	Description
0	31:1	**RESERVED** Default Value: 00000000h Access: RO Reserved
	0	**BCLD_REQ** Default Value: 0b Access: R/W GT Boot Context Load Request. Write to this bit will initiate ?Mcheck Complete Routine? (PPPE flow).

GTACK

GTACK - GTACK

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	120004h

This register is written to by GT for various device 2 sequencer flows.

DWord	Bit	Description
0	31:5	**RESERVED** Default Value: 0000000h Access: R/W Reserved
	4	**RTPACK** Default Value: 0h Access: R/W GT indicates that the set root table pointer flow is complete from its point of view by writing a 1b to this field. Once SW is notified with the appropriate status bit, this bit is cleared by the HW.
	3	**DESCRACK** Default Value: 0h Access: R/W GT indicates that the generic descriptor flow is complete from its point of view by writing a 1b to this field Once SW is notified with the appropriate status bit, this bit is cleared by the HW.
	2	**VTDACK** Default Value: 0h Access: R/W GT indicates that the Translation Enable/Disable or IOTLB Invalidation flow is complete from its point of view by writing a 1b to this field. Once SW is notified with the appropriate status bit, this bit is cleared by the HW.

GTACK - GTACK

	1	**DPRACK** Default Value: 0h Access: R/W GT indicates that DPR Update flow is complete from its point of view by writing a 1b to this field. Once SW is notified with the appropriate status bit, this bit is cleared by the HW.
	0	**PMRACK** Default Value: 0h Access: R/W GT indicates that PMR Enable/Disable flow is complete from its point of view by writing a 1b to this field. Once SW is notified with the appropriate status bit, this bit is cleared by the HW.

GTI PFET control register with lock

PFETCTL - GTI PFET control register with lock		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x0005000A	
Size (in bits):	32	
Address:	24008h	
DWord	**Bit**	**Description**
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of GTI PFETCTL register are R/W 1 = All bits of GTI PFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (that is, writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:23	**Reserved** Access: RO Reserved
	22	**Leave firewall disabled** Access: R/W Lock When this bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM. Encodings: 0 = Default mode, that is, firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, that is, don't firewall the gated domain, but complete logical flow
	21	**Leave FET On** Access: R/W Lock When This bit is set SPC will not turn off the PFET eventhough it will complete the flow with PM Encodings: 0 = Default mode, that is, power off fets during power down flows 1 = Leave ON mode, that is, don't power off pfet, but complete logical flow **Programming Notes** This bit should be programmed before the powerup sequence is initiated for GTI.
	20	**Power Well Status** Access: R/WC 0 = Well is powered Down 1 = Well is powered Up Once written to 1, the lock is set and cannot be cleared (that is, writing a 0 will not clear the lock). These bits are not reset on FLR.

PFETCTL - GTI PFET control register with lock

	19	**Powergood timer error** Access: R/WC 0 = Well is powered Down 1 = Well is powered Up Once written to 1, the lock is set and cannot be cleared (that is, writing a 0 will not clear the lock). These bits are not reset on FLR.
	18:16	**Delay from enabling secondary PFETs to power good** Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: BXT - 60ns 3'b001: BXT - 120ns 3'b010: BXT - 240ns 3'b011: BXT - 480ns 3'b100: BXT - 960ns 3'b101: BXT - 1920ns 3'b110: BXT - 3840ns 3'b111: BXT - 7680ns Value: 101b — Name: **[Default]**
	15:13	**Time period last primay pfet strobe to secondary pfet strobe** Access: R/W Lock Time period last primary pfet strobe to secondary pfet strobe 3'b000: BXT - 60ns (or 6 bclks) 3'b001: BXT - 120ns (or 12 bclks) 3'b010: BXT - 180ns (or 18 bclks) 3'b111: BXT - 480ns (or 48 bclks)
	12:10	**Time period b/w two adjacent strobes** Access: R/W Lock Time period b/w two adjacent strobes to the primary FETs 3'b000: BXT - 60ns (or 6 bclks) 3'b001: BXT - 120ns (or 12 bclks) 3'b010: BXT - 180ns (or 18 bclks) 3'b111: BXT - 480ns (or 48 bclks)
	9:7	**FET setup margin from enable to strobe** Access: R/W Lock Setup margin in design before sampling enable event at the first pre-charge sequencer/shift register flop 3'b000: BXT - 60ns (or 6 bclks) 3'b001: BXT - 120ns (or 12 bclks)

PFETCTL - GTI PFET control register with lock

		3'b010: BXT - 180ns (or 18 bclks) 3'b111: BXT - 480ns (or 48 bclks)
	6:0	**Number of flops to enable primary FETs** Access: R/W Lock Number of flops to enable primary FETs. For a setting of N there will be N+1 total strobes generated 7'b0000000: 10 Flops to be strobed 7'b0000001: 11 Flops to be strobed 7'b0000010: 12 Flops to be strobed 7'b0001111: 26 Flops to be strobed

Value	Name
0001010b	**[Default]**

GT Mode Register

GT_MODE - GT Mode Register

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	07008h

This Register is used to control the 6EU and 12EU configuration for GT.
Writing 0x01FF01FF to this register enables the 6EU mode.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15	**EU Local Thread Checking Enable** Access: r/w This field configures the EU local thread checking. If enable the stateless access will be checked against the local thread's scratch space size and start address. 0h – Disable **[Default]** – EU local thread checking is disabled. 1h – Enable – EU local thread checking is enabled. **Restriction** Restriction : BXT configuration do not properly support Per-Thread Scratch Space checking when headerless Data Port messages are used. The workaround is either to disable this control, or not use SFID_DP_DC0 or SFID_DP_DC2 headerless messages.
	14:13	**SFR mode** Access: r/w Format: U2 This field must be zero when not in GT4(SFR) configuration i.e GTB_rendermode fuse set to SFR.
	12:11	**Cross Slice Hashing Mode** Access: r/w Format: U2

GT_MODE - GT Mode Register

Value	Name	Description	Programming Notes
0h	Normal Mode **[Default]**	GT3: 16x16 Hashing enabled GT2 or lower modes: No cross slice hashing	
1h	Cross Slice Hashing Disable	Disables the cross slice hashing	
2h	32x16 Hahsing	32x16 Pixel hashing across slices	
3h	32X32 hashing	32X32 pixel hashing across slices	This setting must be used when sub-slice hashing mode is 16x16.

Programming Notes
Normal mode of operation in GT3 mode will be to use either 16x16 Hashing or 32x32 Hashing.

10 **Reserved**

Access:	r/w
Format:	PBC

9:8 **Subslice Hashing Mode**

Access:	r/w
Format:	U2

This field defines hashing modes across subslices.

Value	Name	Description
0h	**[Default]**	8X8 hashing
1h		16x4 hashing
2h		8x4 hashing
3h		16x16 hashing

7 **Reserved**

Access:	r/w
Format:	PBC

7 **Bindless Surface Base Address Select**

Access:	r/w
Format:	Enable

This field selects Bindless_Surface_State_Base_Addr versus Dynamic_State_Base_Addr for sampler state heap base address. It only applies when Bindless Surfaces are being enabled via the BTI encoding. It is intended to allow support for bindless samplers in BXT by sharing the Bindless Surface heap, and using the Bindless Surface Base Addr.

Value	Name	Description
0h	Disable **[Default]**	Selects Dynanmic State Base Addr for Sampler State.

GT_MODE - GT Mode Register

1h	Enable	Selects Bindless Surface Base Address for Sampler State

6 Reserved

Access:	r/w
Format:	PBC

5:4 Slice2 IZ Hashing: 7 EU subslice encoding

Access:	r/w

These bits control 3-way sub-slice hashing by conveying which sub-slice has 7 EUs.

Value	Name	Description
0h	**[Default]**	All subslices have equal number of EUs.
1h		Subslice 2 has 7 EUs.
2h		Subslice 1 has 7 EU.
3h		Subslice 0 has 7 EUs.

Programming Notes
SW must program these bits based on EU Disable Fuses in Slice 2.

3:2 Slice1 IZ Hashing: 7 EU subslice encoding

Access:	r/w

These bits control 3-way sub-slice hashing by conveying which sub-slice has 7 EUs.

Value	Name	Description
0h	**[Default]**	All subslices have equal number of EUs.
1h		Subslice 2 has 7 EUs.
2h		Subslice 1 has 7 EUs.
3h		Subslice 0 has 7 EUs.

Programming Notes
SW must program these bits based on EU Disable Fuses in Slice 1.

1:0 Slice 0 IZ Hashing: 7 EU subslice encoding

Access:	r/w

These bits control 3-way sub-slice hashing by conveying which sub-slice has 7 EUs.

Value	Name	Description
0h	**[Default]**	All subslices have equal number of EUs.
1h		Subslice 2 has 7 EUs.
2h		Subslice 1 has 7 EUs.
3h		Subslice 0 has 7 EUs.

Programming Notes
SW must program these bits based on EU Disable Fuses in Slice 0.

Hardware Scratch Read Write

HSRW_0_2_0_PCI - Hardware Scratch Read Write

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	16
Address:	00060h

This register is reserved as a HW scratchpad.

DWord	Bit	Description
0	15:0	**Reserved R/W** Default Value: 0000000000000000b Access: R/W Reserved for future usage.

HDPORT_STATE

HDPORT_STATE

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	45050h-45053h
Name:	HDPORT State
ShortName:	HDPORT_STATE
Power:	PG0
Reset:	soft

This register is used to indicate when display resources have been pre-empted by hardware for the HDPORT feature. The usage is set during boot, before BIOS or software is active.
The list of DPLLs and DDIs in this register many not accurately reflect the total number of DPLLs and DDIs supported by display engine. HDPORT will not use any DPLL or DDI not listed here. It will not use any DPLL or DDI that is listed here, but not supported by the particular product or SKU.

Programming Notes

HDPORT is not used on Broxton, so all bits will always be 0.

Restriction

Restriction : Display software must not use resources that are marked as being used by HDPORT.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15	**DPLL2 Used** This field indicates whether DPLL 2 is being used by HDPORT. 0b – Not used 1b – Used
	14	**DPLL3 Used** This field indicates whether DPLL 3 is being used by HDPORT. 0b – Not used 1b – Used
	13	**DPLL1 Used** This field indicates whether DPLL 1 is being used by HDPORT.

HDPORT_STATE

		Value: 0b — Name: Not used Value: 1b — Name: Used
	12	**DPLL0 Used** This field indicates whether DPLL 0 is being used by HDPORT. Value: 0b — Name: Not used Value: 1b — Name: Used
	11	**Spare 11**
	10	**Spare 10**
	9	**Spare 9**
	8	**DDI3 Type** This field indicates whether DDI 3 (DDI D) is being used in HDMI or DP mode by HDPORT. Value: 0b — Name: DP Value: 1b — Name: HDMI
	7	**DDI3 Used** This field indicates whether DDI 3 (DDI D) is being used by HDPORT. Value: 0b — Name: Not used Value: 1b — Name: Used
	6	**DDI2 Type** This field indicates whether DDI 2 (DDI C) is being used in HDMI or DP mode by HDPORT. Value: 0b — Name: DP Value: 1b — Name: HDMI
	5	**DDI2 Used** This field indicates whether DDI 2 (DDI C) is being used by HDPORT. Value: 0b — Name: Not used Value: 1b — Name: Used
	4	**DDI1 Type** This field indicates whether DDI 1 (DDI B) is being used by the HDPORT in HDMI or DP mode. Value — Name

HDPORT_STATE

		0b: DP 1b: HDMI
	3	**DDI1 Used** This field indicates whether DDI 1 (DDI B) is being used by HDPORT. Value: 0b – Not used; 1b – Used
	2	**DDI0 Type** This field indicates whether DDI 0 (DDI A and DDI E) is being used in HDMI or DP mode by HDPORT. Value: 0b – DP; 1b – HDMI
	1	**DDI0 Used** This field indicates whether DDI 0 (DDI A and DDI E) is being used by HDPORT. Value: 0b – Not used; 1b – Used
	0	**HDPORT Enabled** This field indicates whether HDPORT is enabled. Value: 0b – Disabled; 1b – Enabled

Header Type

HDR2_0_2_0_PCI - Header Type		
Register Space:	PCI: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	8	
Address:	0000Eh	
This register contains the Header Type of the IGD.		
DWord	**Bit**	**Description**
0	7	**Multi Function Status** Default Value: 0b Access: RO Indicates if the device is a Multi-Function Device. The Value of this register is hardwired to 0, internal graphics is a single function.
	6:0	**Header Code** Default Value: 0000000b Access: RO This is a 7-bit value that indicates the Header Code for the IGD. This code is hardwired to the value 00h, indicating a type 0 configuration space format.

HOTPLUG_CTL

HOTPLUG_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	C4030h-C4033h
Name:	Hot Plug Control
ShortName:	HOTPLUG_CTL
Power:	PG0
Reset:	soft

Hot plug detect (HPD) is used for notification of plug, unplug, and other sink events.
The short pulse durations are programmed in HPD_PULSE_CNT.
The hotplug ISR gives the live states of the HPD pins.

Programming Notes

Due to the possibility of back to back HPD events it is recommended that software filters the value read from the ISR.

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28	**DDI A HPD Input Enable** This field enables the HPD buffer for digital port A. 0b – Disable 1b – Enable
	27	**DDI A HPD Invert** This field inverts the HPD sense for digital port A. 1b – Invert 0b – Do not invert
	26	**Reserved** Format: MBZ
	25:24	**DDI A HPD Status** Access: R/WC This field indicates the hot plug detect status on port A.

HOTPLUG_CTL

When HPD input is enabled and either a long or short pulse is detected, one of these bits will set and the hotplug IIR will be set (if unmasked in the IMR).
These are sticky bits, cleared by writing 1s to both of them.

Value	Name
00b	Hot plug event not detected
01b	Short pulse detected
10b	Long pulse detected
11b	Short and long pulses detected

23:13 Reserved

Format:	MBZ

12 DDI C HPD Input Enable

This field enables the HPD buffer for digital port C.

Value	Name
0b	Disable
1b	Enable

11 DDI C HPD Invert

This field inverts the HPD sense for digital port C.

Value	Name
1b	Invert
0b	Do not invert

10 Reserved

Format:	MBZ

9:8 DDI C HPD Status

Access:	R/WC

This field indicates the hot plug detect status on port C.
When HPD input is enabled and either a long or short pulse is detected, one of these bits will set and the hotplug IIR will be set (if unmasked in the IMR).
These are sticky bits, cleared by writing 1s to both of them.

Value	Name
00b	Hot plug event not detected
01b	Short pulse detected
10b	Long pulse detected
11b	Short and long pulses detected

7:5 Reserved

Format:	MBZ

HOTPLUG_CTL

	4	**DDI B HPD Input Enable** This field enables the HPD buffer for digital port B. **Value** / **Name** 0b – Disable 1b – Enable
	3	**DDI B HPD Invert** This field inverts the HPD sense for digital port B. **Value** / **Name** 1b – Invert 0b – Do not invert
	2	**Reserved** Format: MBZ
	1:0	**DDI B HPD Status** Access: R/WC This field indicates the hot plug detect status on port B. When HPD input is enabled and either a long or short pulse is detected, one of these bits will set and the hotplug IIR will be set (if unmasked in the IMR). These are sticky bits, cleared by writing 1s to both of them. **Value** / **Name** 00b – Hot plug event not detected 01b – Short pulse detected 10b – Long pulse detected 11b – Short and long pulses detected

HPD_FILTER_CNT

HPD_FILTER_CNT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x000001F2
Access:	R/W
Size (in bits):	32
Address:	C4038h-C403Bh
Name:	HPD Filter Count
ShortName:	HPD_FILTER_CNT
Power:	PG0
Reset:	global

This register is on the chip reset, not the FLR.

Restriction
Restriction : This register must be programmed properly before enabling DDI HPD detection.

DWord	Bit	Description
0	31:17	**Reserved** Format: MBZ
	16:0	**HPD Filter Count** Default Value: 001F2h 500 microseconds These bits define the duration of the filter for DDI HPD. The value is the number of microseconds minus 2.

HPD_PULSE_CNT

HPD_PULSE_CNT

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x000007CE
Access:	R/W
Size (in bits):	32
Address:	C4034h-C4037h
Name:	HPD Pulse Count DDI B
ShortName:	HPD_PULSE_CNT_B
Power:	PG0
Reset:	global
Address:	C4044h-C4047h
Name:	HPD Pulse Count DDI C
ShortName:	HPD_PULSE_CNT_C
Power:	PG0
Reset:	global
Address:	C404Ch-C404Fh
Name:	HPD Pulse Count DDI A
ShortName:	HPD_PULSE_CNT_A
Power:	PG0
Reset:	global

There is one instance of this register per DDI.
This register is on the chip reset, not the FLR.

Restriction
Restriction : This register must be programmed properly before enabling DDI HPD detection.

DWord	Bit	Description
0	31:17	**Reserved** Format: MBZ
	16:0	**ShortPulse Count** These bits define the duration of the pulse defined as a short pulse for DDI HPD. The value is the number of microseconds minus 2. Value: 007CEh — Name: 2,000 microseconds for DisplayPort **[Default]** Value: 1869Eh — Name: 100,000 microseconds for HDMI and DVI

Indirect Context Pointer

INDIRECT_CTX - Indirect Context Pointer

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1

This register is used to program the indirect address to be executed between CS and SVG engine context if enabled. This will only get executed due to regular context save/restore and not during power restore. This register is part of the execution list context and will be executed per context. Only supported if execution list is enabled. There is no preempting workloads within this context.

Programming Notes	Source
BlitterCS/VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be programmed for these command streamers.	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS
The following commands are not supported within Render CS indirect context:	RenderCS

Command Name
MI_WAIT_FOR_EVENT
MI_SEMAPHORE_SIGNAL
MI_ARB_CHECK
MI_RS_CONTROL
MI_REPORT_HEAD
MI_URB_ATOMIC_ALLOC
MI_SUSPEND_FLUSH
MI_TOPOLOGY_FILTER
MI_RS_CONTEXT
MI_SET_CONTEXT
MI_URB_CLEAR
MI_SEMAPHORE_WAIT in Memory Poll Mode is not supported. [BXT]: MI_SEMAPHORE_WAIT in register poll mode is supported.
MI_BATCH_BUFFER_START
MI_CONDITIONAL_BATCH_BUFFER_END
MEDIA_OBJECT_WALKER
GPGPU_WALKER
3DPRIMITIVE
3DSTATE_BINDING_TABLE_POINTERS_VS

INDIRECT_CTX - Indirect Context Pointer

3DSTATE_BINDING_TABLE_POINTERS_HS	
3DSTATE_BINDING_TABLE_POINTERS_DS	
3DSTATE_BINDING_TABLE_POINTERS_GS	
3DSTATE_BINDING_TABLE_POINTERS_PS	
3DSTATE_GATHER_CONSTANT_VS	
3DSTATE_GATHER_CONSTANT_GS	
3DSTATE_GATHER_CONSTANT_HS	
3DSTATE_GATHER_CONSTANT_DS	
3DSTATE_GATHER_CONSTANT_PS	
3DSTATE_DX9_CONSTANTF_VS	
3DSTATE_DX9_CONSTANTF_HS	
3DSTATE_DX9_CONSTANTF_DS	
3DSTATE_DX9_CONSTANTF_GS	
3DSTATE_DX9_CONSTANTF_PS	
3DSTATE_DX9_CONSTANTI_VS	
3DSTATE_DX9_CONSTANTI_HS	
3DSTATE_DX9_CONSTANTI_DS	
3DSTATE_DX9_CONSTANTI_GS	
3DSTATE_DX9_CONSTANTI_PS	
3DSTATE_DX9_CONSTANTB_VS	
3DSTATE_DX9_CONSTANTB_HS	
3DSTATE_DX9_CONSTANTB_DS	
3DSTATE_DX9_CONSTANTB_GS	
3DSTATE_DX9_CONSTANTB_PS	
3DSTATE_DX9_LOCAL_VALID_VS	
3DSTATE_DX9_LOCAL_VALID_DS	
3DSTATE_DX9_LOCAL_VALID_HS	
3DSTATE_DX9_LOCAL_VALID_GS	
3DSTATE_DX9_LOCAL_VALID_PS	
3DSTATE_DX9_GENERATE_ACTIVE_VS	
3DSTATE_DX9_GENERATE_ACTIVE_HS	
3DSTATE_DX9_GENERATE_ACTIVE_DS	
3DSTATE_DX9_GENERATE_ACTIVE_GS	
3DSTATE_DX9_GENERATE_ACTIVE_PS	
3DSTATE_BINDING_TABLE_EDIT_VS	

INDIRECT_CTX - Indirect Context Pointer

3DSTATE_BINDING_TABLE_EDIT_GS
3DSTATE_BINDING_TABLE_EDIT_HS
3DSTATE_BINDING_TABLE_EDIT_DS
3DSTATE_BINDING_TABLE_EDIT_PS
3DSTATE_CONSTANT_VS
3DSTATE_CONSTANT_GS
3DSTATE_CONSTANT_PS
3DSTATE_CONSTANT_HS
3DSTATE_CONSTANT_DS
MI_BATCH_BUFFER_END

Workaround

[Render CS Only][Execlist Mode of Scheduling]: SW must ensure arbitration is switched off while context restore is in progress for any given context. This is achieved by disabling arbitration by programming MI_ARB_ON_OFF to "Arbitration Disable" in RCS_INDIRECT_CTX buffer and by enabling back the arbitration by programming MI_ARB_ON_OFF to "Arbitration Enable" as the last command prior to MI_BATCH_END in the BB_PER_CTX_PTR buffer of every context submitted. Note that RCS_INDIRECT_CTX_OFFSET could be set to default value or any other legitimate value as per the programming notes of the register definition. Arbitration disable by programming MI_ARB_ON_OFF (Arbitration Disabled) in RCS_INDIRECT_CTX buffer. Arbitration enabled by programming MI_ARB_ON_OFF (Arbitration Enabled) as the last command prior to MI_BATCH_BUFFER_END in BB_PER_CTX_PTR buffer. Additional Note: This WA need not be applied when it is guaranteed for no preemption to occur during execution of GPGPU workload. Preemption of GPGPU workload can be avoided by Bracketing the GPGPU workload with MI_ARB_ON_OFF (Arbitration Disable) and MI_ARB_ON_OFF (Arbitration Enable) command. MI_ARB_ON_OFF is a privileged command and can only be programmed in ring buffer or in privileged batch buffer (batch buffer in GGTT memory). Pending execlist submitted must not trigger preemption of the ongoing GPGPU workload due to following reasons First context of the pending execlist submitted is not the same as the ongoing GPGPU context. Force restore bit set for the submitted pending execlist.

DWord	Bit	Description
0	31:6	**Indirect CS Context Address** Format: GraphicsAddress[31:6] Pointer to the Context in memory to be executed as a batch.
	5:0	**Size of Indirect CS Context** Format: U6 This is the size of the Indirect Context for CS. This size supports up to 63 cache lines worth of commands where a cache line is 64B. If programmed to zero then the indirect fetch of the CS context is disabled. Value: [0,63] Name:

Interrupt Line

INTRLINE_0_2_0_PCI - Interrupt Line	
Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	8
Address:	0003Ch

This register is used to communicate interrupt line routing information. The device itself does not use this value, rather it is used by device drivers and operating systems to determine priority and vector information.

DWord	Bit	Description
0	7:0	**Interrupt Connection** Default Value: 00000000b Access: R/W Used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates to which input of the system interrupt controller the device's interrupt pin is connected.

Interrupt Pin

INTRPIN_0_2_0_PCI - Interrupt Pin			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00000001		
Size (in bits):	8		
Address:	0003Dh		
This register tells which interrupt pin the device uses.			
DWord	**Bit**	**Description**	
0	7:0	**Interrupt Pin Value**	
		Default Value:	00000001b
		Access:	RO
		As a single function device, the IGD specifies INTA# as its interrupt pin. Hardwired to 01h = INTA#.	

I/O Base Address

IOBAR_0_2_0_PCI - I/O Base Address

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000001
Size (in bits):	32
Address:	00020h

This register provides the Base offset of the I/O registers within Device #2. Bits 15:6 are programmable allowing the I/O Base to be located anywhere in 16bit I/O Address Space. Bits 2:1 are fixed and return zero; bit 0 is hardwired to a one indicating that 8 bytes of I/O space are decoded. Access to the 8Bs of IO space is allowed in PM state D0 when IO Enable (PCICMD bit 0) set. Access is disallowed in PM states D1-D3 or if IO Enable is clear or if Device #2 is turned off or if Internal graphics is disabled through the fuse or fuse override mechanisms.
Note that access to this IO BAR is independent of VGA functionality within Device #2.
If accesses to this IO bar is allowed then all 8, 16 or 32 bit IO cycles from IA cores that falls within the 8B are claimed.

DWord	Bit	Description
0	31:16	**Reserved** Default Value: 0000000b Access: RO Reserved
	15:6	**IO Base Address** Default Value: 0000000000b Access: R/W Set by the OS, these bits correspond to address signals [15:6].
	5:3	**Reserved** Default Value: 0000000b Access: RO Reserved
	2:1	**Memory Type** Default Value: 00b Access: RO Hardwired to 0s to indicate 32-bit address.

IOBAR_0_2_0_PCI - I/O Base Address

	0	**Memory/IO Space** Default Value: 1b Access: RO Hardwired to "1" to indicate IO space.

IOMMU_DEFEATURE_CAPECAPDIS

IOMMU_DEFEATURE_CAPECAPDIS - IOMMU_DEFEATURE_CAPECAPDIS

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	03000h

Description

Capability/Extended Capability Disable Register. Register providing control of various IOMMU functionality. This register is a LOCAL CR register and not an MMIO register

DWord	Bit	Description
0	31:25	**RSVD** Default Value: 0b Access: RO RSVD
	24	**EAFSCAPDIS** Default Value: 0b Access: R/W 1: Hardware does not support the extended-accessed (EA) bit in first-level paging-structure entries. 0: Hardware supports the extendedaccessed (EA) bit in first-level paging-structure entries.
	23	**NWFSCAPDIS** Default Value: 0b Access: R/W 1: Hardware ignores the "No Write" (NW) flag in Device-TLB translationrequests, and behaves as if NW is always 0. 0: Hardware supports the "No Write" (NW) flag in Device-TLB translationrequests.
	22	**POT** Default Value: 0b Access: R/W 1: Hardware does not support PASID-only Translation Type in extended-context-entries. 0: Hardware supports PASID-only Translation Type in extended-context-entries.

IOMMU_DEFEATURE_CAPECAPDIS - IOMMU_DEFEATURE_CAPECAPDIS

21 SRS

Default Value:	0b
Access:	R/W

1: H/W does not support requests-with-PASID seeking supervisor privilege.
0: H/W supports requests-with-PASID seeking supervisor privilege.

20 ERS

Default Value:	0b
Access:	R/W

1: H/W does not support requests seeking execute permission.
0: H/W supports requests seeking execute permission.

19 PRSCAPDIS

Default Value:	0b
Access:	R/W

1: Hardware does not support Page Requests.
0: Hardware supports Page Requests.

18 PASIDCAPDIS

Access:	R/W

1: Hardware does not support process address space IDs.
0: Hardware supports Process Address Space IDs.

Value	Name
0b	

17 DISCAPDIS

Default Value:	0b
Access:	R/W

1: Hardware does not support deferred invalidations of IOTLB and Device-TLB.
0: Hardware supports deferred invalidations of IOTLB and Device-TLB.

16 NESTCAPDIS

Default Value:	0b
Access:	R/W

1: Hardware does not support nested translations.
0: Hardware supports nested translations.

IOMMU_DEFEATURE_CAPECAPDIS - IOMMU_DEFEATURE_CAPECAPDIS

	15	**MTSCAPDIS** Default Value: 0b Access: R/W 1: Hardware does not support Memory Type in first-level translation and Extended in second-level. 0: Hardware supports Memory Type in first-level translation and Extended mem type in second-level.
	14	**ECSCAPDIS** Default Value: 0b Access: R/W 1: Hardware does not support extended-root-entries and Extended Context-Entries 0: Hardware supports extended-root-entries and Extended Context-Entries
	13	**SCCAPDIS** Default Value: 0b Access: R/W 1: Hardware does not support 1-setting of the SNP field in the page-table entries. 0: Hardware supports the 1-setting of the SNP field in the page-table entries.
	12	**PTCAPDIS** Default Value: 0b Access: R/W 1: Hardware does not support pass-through translation type in context entries. 0: Hardware supports pass-through translation type in context entries.
	11	**EIM** Default Value: 0b Access: R/W 1: On Intelx64 platforms, hardware supports only 8-bit APIC-IDs (xAPIC mode). 0: On Intelx64 platforms, hardware supports 32-bit APIC-IDs (x2APIC mode).
	10	**IRCAPDIS** Default Value: 0b Access: R/W 1: Hardware does not support interrupt remapping. 0: Hardware supports interrupt remapping.

IOMMU_DEFEATURE_CAPECAPDIS - IOMMU_DEFEATURE_CAPECAPDIS

	9	**DTCAPDIS** Default Value: 0b Access: R/W 1: Hardware does not support device-IOTLBs. 0: Hardware supports Device-IOTLBs.
	8	**QICAPDIS** Default Value: 0b Access: R/W 1: Hardware does not support queued invalidations. 0: Hardware supports queued invalidations.
	7	**C** Default Value: 0b Access: R/W This field indicates if hardware access to the root, context, page-table and interrupt-remap structures are coherent (snooped) or not. 1: Indicates hardware accesses to remapping structures are non-coherent. 0: Indicates hardware accesses to remapping structures are coherent.
	6	**FL1GPCAPDIS** Default Value: 0b Access: R/W A value of 1 in this field indicates 1-GByte page size is disabled for first-level translation.
	5	**PSI** Default Value: 0b Access: R/W Page Selective Invalidation. 1: Hardware supports only domain and global invalidates for IOTLB 0: Hardware supports page selective, domain and global invalidates for IOTLB
	4:1	**SLLPSCAPCTRL** Default Value: 0h Access: R/W This field indicates the super page sizes supported by hardware. A value of 1 in any of these bits indicates the corresponding super-page size is supported. The super-page sizes corresponding to various bit positions within this field are: 0: 21-bit offset to page frame (2MB)

IOMMU_DEFEATURE_CAPECAPDIS - IOMMU_DEFEATURE_CAPECAPDIS

		1: 30-bit offset to page frame (1GB) 2: 39-bit offset to page frame (512GB) 3: 48-bit offset to page frame (1TB) Hardware implementations supporting a specific super-page size must support all smaller super-page sizes, i.e. only valid values for this field are 0000b, 0001b, 0011b, 0111b, 1111b.SLLPSCAPCTRL
	0	**ZLR** Default Value: 0b Access: R/W 1: Indicates the remapping hardware unit blocks (and treats as fault) zero length DMA read requests to write-only pages. 0: Indicates the remapping hardware unit supports zero length DMA read requests to write-only pages.

IOMMU_DEFEATURE_MISCDIS

IOMMU_DEFEATURE_MISCDIS - IOMMU_DEFEATURE_MISCDIS

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	0300Ch

Description

Miscellaneous Disable Register. Register to disable certain functionality of IOMMU. This register is a LOCAL CR register and not an MMIO register

DWord	Bit	Description
0	31	**Reserved**
	30:23	**Reserved**
	22:10	**SPARE** Default Value: 000h Access: R/W Reserved bit
	9	**PRQCOHDIS** Default Value: 0b Access: R/W PRQ Coherency Disability
	8	**QICOHDIS** Default Value: 0b Access: R/W QI Coherency Disability
	7	**H2PDIS** Default Value: 0b Access: R/W Hit2pend Disability
	6	**DMA_RSRV_CTL** Default Value: 0b Access: R/W Reserved bit check Disability

IOMMU_DEFEATURE_MISCDIS - IOMMU_DEFEATURE_MISCDIS

	5:4	**COLORLIMDIS** Default Value: 00b Access: R/W Disable color limit
	3	**STALLFETCHFIFODIS** Default Value: 0b Access: R/W Stall Fetch FIFO
	2	**STALLCBFIFODIS** Default Value: 0b Access: R/W Stall CB FIFO
	1	**CTXPARTINVDIS** Default Value: 0b Access: R/W Convert Context function/domain invalidations to global
	0	**IOTLBPARTINVDIS** Default Value: 0b Access: R/W Convert IOTLB page/domain invalidations to global

IOMMU_DEFEATURE_PWRDNOVRD

IOMMU_DEFEATURE_PWRDNOVRD - IOMMU_DEFEATURE_PWRDNOVRD

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	03010h

Description

Power Down Override Register. Power Down Override for individual IOMMU component. This register is a LOCAL CR register and not an MMIO register

DWord	Bit	Description
0	31:20	**RSVD** Default Value: 000h Access: RO RSVD
	19	**PDO_Spare** Default Value: 0b Access: R/W Spare Powerdown override.
	18	**PDO_FAULTCAP** Default Value: 0b Access: R/W Powerdown override for Fault Handling Module.
	17	**PDO_QINV** Default Value: 0b Access: R/W Powerdown override for QI Module.
	16	**PDO_MSG** Default Value: 0b Access: R/W Powerdown override for Message Interface.

IOMMU_DEFEATURE_PWRDNOVRD - IOMMU_DEFEATURE_PWRDNOVRD

	15	**PDO_INV** Default Value: 0b Access: R/W Powerdown override for Invalidation Engine.
	14	**PDO_SEQ** Default Value: 0b Access: R/W Powerdown override for Sequencer.
	13	**PDO_CREG** Default Value: 0b Access: R/W Powerdown override for CREG Module.
	12	**PDO_FETCH_RET** Default Value: 0b Access: R/W Powerdown override for fetch return.
	11	**PDO_FETCH_FIFO** Default Value: 0b Access: R/W Powerdown override for fetch fifo.
	10	**PDO_L4_TLB** Default Value: 0b Access: R/W Powerdown override for L4 TLB.
	9	**PDO_RC_TLB** Default Value: 0b Access: R/W Powerdown override for RC TLB.
	8	**PDO_PQ_FSM** Default Value: 0b

IOMMU_DEFEATURE_PWRDNOVRD - IOMMU_DEFEATURE_PWRDNOVRD

		Access: R/W Powerdown override for PQ FSM.
	7	**PDO_FILL_FSM** Default Value: 0b Access: R/W Powerdown override for Fill FSM.
	6	**PDO_L4_FSM** Default Value: 0b Access: R/W Powerdown override for L4 FSM.
	5	**PDO_RC_FSM** Default Value: 0b Access: R/W Powerdown override for RC FSM.
	4	**PDO_IR_FSM** Default Value: 0b Access: R/W Powerdown override for IR FSM.
	3	**PDO_PWT_ARB** Default Value: 0b Access: R/W Powerdown override for PWT Arbiter.
	2	**PDO_PWT_PQ_ALLOC** Default Value: 0b Access: R/W Powerdown override for Pending Queue Allocation.
	1	**PDO_TLB** Default Value: 0b Access: R/W Powerdown override for TLB.

IOMMU_DEFEATURE_PWRDNOVRD - IOMMU_DEFEATURE_PWRDNOVRD		
	0	**PDO_CB** Default Value: 0b Access: R/W Powerdown override for Credit Buffer.

IOMMU_DEFEATURE_PWSWTRDIS

IOMMU_DEFEATURE_PWSWTRDIS - IOMMU_DEFEATURE_PWSWTRDIS

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	03008h

Description

Page Walk Structure Disable Register.Disable Page Walk ways. This register is a LOCAL CR register and not an MMIO register

DWord	Bit	Description
0	31:14	**RSVD** Default Value: 00000h Access: RO RSVD
	13:12	**PQDIS** Default Value: 0h Access: R/W Disable # of PQ entries. 11 : All but one entry/priority, 10 : 1/2, 01 : 1/4, 00 : none
	11:10	**PWTDIS** Default Value: 0h Access: R/W Disable # of PWT entries. 11 : All but one entry/priority, 10 : 1/2, 01 : 1/4, 00 : none
	9:8	**RCCDIS** Default Value: 0h Access: R/W Per TLBID, disable RCC. 11 : full, 10 : 1/2, 01 : 1/4, 00 : none.
	7:6	**SL5DIS** Default Value: 0h Access: R/W Per TLBID, disable TLB. 11 : full, 10 : 1/2, 01 : 1/4, 00 : none.

IOMMU_DEFEATURE_PWSWTRDIS - IOMMU_DEFEATURE_PWSWTRDIS		
	5:4	**SL4DIS** Default Value: 0h Access: R/W Per TLBID, disable TLB. 11 : full, 10 : 1/2, 01 : 1/4, 00 : none.
	3:2	**SL3DIS** Default Value: 0h Access: R/W Per TLBID, disable TLB. 11 : full, 10 : 1/2, 01 : 1/4, 00 : none.
	1:0	**SL2DIS** Default Value: 0h Access: R/W Per TLBID, disable TLB 11 : full, 10 : 1/2, 01 : 1/4, 00 : none.

IOMMU_DEFEATURE_TLBDIS

IOMMU_DEFEATURE_TLBDIS - IOMMU_DEFEATURE_TLBDIS	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	03004h

Description
IOTLB Disable Register. Per TLBID, disable TLB ways. This register is a LOCAL CR register and not an MMIO register

DWord	Bit	Description
0	31:0	**IOTLBDIS** Default Value: 00000000h Access: R/W Per TLBID, disable TLB 11:full, 10:1/2, 01: 1/4, 00:none.

L3 Control Register

L3CNTLREG - L3 Control Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	07034h

Programming Notes

The L3 allocation programming should assign all ways of the cache with no left over ways. Refer to L3 section for the recommended settings.

Any L3 configuration change that reduces the data cache allocation when strong IA coherency is used requires the full flush of L3 prior to the programming update.
An explicit or implicit flush of L3 (DC Flush) through the command streamerdoesn't result in flushing/invalidating the IA Coherent lines from L3. However this can be achieved by setting the "**Pipe line flush Coherent lines**" control bitin the "L3SQCREG4" register.

DWord	Bit	Description
0	31:25	**All L3 Client Pool** Access: R/W Number of ways allocated for the all client pool. This is a combined pool for all clients. [0h,40h] — Increments of 4KB 30h — **[Default]** **Programming Notes** When this field is non-zero, **DC Way Assignment** and **Read Only Client Pool** should be 0KB.
	24:18	**DC Way Assignment** Access: R/W Number of ways allocated for DC. Note this allocation is only for DC data types. [0h,40h] — 0KB-256KB — Increments of 4KB **Programming Notes** Note: This field must be 0KB if All L3 Client Pool is non-zero. **Please refer to L3 HAS for valid programming values**

L3CNTLREG - L3 Control Register

17:11 Read Only Client Pool

Access:	R/W

Number of ways allocated for Read Only L3 clients. This is a combined pool for all Read Only clients.

Value	Name	Description
[0h,40h]	0KB-256KB	Increments of 4KB

Programming Notes
Note: This field must be 0KB if All L3 Client Pool is non-zero. **Please refer to L3 HAS for valid programming values**

10 Reserved

Access:	R/W
Format:	PBC

9 Error Detection Behavior Control

Access:	R/W
Format:	Enable

The L3 error detection can be enabled to hang the GPU on a non-recoverable error due to SER type events. Such option will be used when corresponding context has data consistency requirements.

Once error detection is enabled, s/w has to initialize URB or SLM to all 0's (based on usage model) prior to execution of the workload. Initialization is required to clean up the error detection logic and syndrome tracking.

Value	Name	Description
0h	**[Default]**	RTL does not hang on parity errors or double bit error
1h		RTL enforces a hang on parity errors or double bit error

8 GPGPU L3 Credit Mode Enable

Access:	R/W
Format:	Enable

This bit is required to be enabled under GPGPU workloads to provide the MAX latency coverage from L3 cache. It will override the registers 0xB100[18:14] and 0xB100[23:19], to 0 and the maximum value respectively.

7:1 URB Allocation

Access:	R/W

Number of ways allocated for URB usage

Value	Name	Description
[0h,40h]		Increments of 4KB
30h	**[Default]**	

L3CNTLREG - L3 Control Register

		Programming Notes **Please refer to L3 HAS for valid programming values. At least one way needs to be programmed in L3 space.**
	0	**SLM Mode Enable** Access: R/W Format: Enable When enabled, a 64KB (per bank) region of L3 is reserved for SLM.

L3 Control Register1

L3CNTLREG1 - L3 Control Register1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0xD007FFFF
Size (in bits):	32
Address:	0B10Ch

DWord	Bit	Description
0	31:28	**Data Fifo Depth Control** Access: R/W Data Fifo Depth Control (TS mode). Value cannot be zero for normal operation. lbcf_csr_lc_datafifo_depth[3:0]. Value: 1101b — Name: **[Default]**
	27:24	**Data Clock off time** Access: R/W Description: Data Clock off time (DATACLKOFF): Data Clock off time - Data block is shut off after these many number of clocks programmed in this register bits. lbcf_csr_lc_dataclkoff_time[3:0]. Min value to be 4'h0100. It should be between 4'h4 : 4'hf. Value: 1100b — Name: **[Default]**
	23:20	**TAG CLK OFF TIME** Access: R/W Description: TAG CLK OFF TIME (TAGCLKOFF): TAG Clock Off time. This is the time, which Clock gating Logic checks before it turns off the clock. lbcf_csr_lc_tagclkoff_time[3:0]. Value can be between 4'h4 - 4'hf.

L3CNTLREG1 - L3 Control Register1

Value	Name
0100b	**[Default]**

19 **L3 Aging Disable Bit**

Default Value:	0b
Access:	R/W

L3 Aging Disable Bit (L3AGDIS):
Aging Disable.
lbcf_csr_lc_agingdis.

18:15 **Fill aging**

Default Value:	1111b
Access:	R/W

Fill aging (L3AGF):
Aging Counter for Fill.
lbcf_csr_lc_fill_aging_cnt[3:0].
If bit B103.19 is 0 then this register value has to be nonzero.

14:11 **Aging Counter for Read 1 Port**

Default Value:	1111b
Access:	R/W

Aging Counter for Read 1 Port (L3AGR1):
Aging Counter for Read 1 Port.
lbcf_csr_lc_r1_aging_cnt[3:0].
If bit B103.19 is 0 then this register value has to be nonzero.

10:7 **L3 Aging Counter for R0**

Default Value:	1111b
Access:	R/W

L3 Aging Counter for R0 (L3AGR0):
Aging Counter for R0 Port.
lbcf_csr_lc_r0_aging_cnt[3:0].
If bit B103.19 is 0 then this register value has to be nonzero.

6:4 **L3 Aging Counter for SNOOP**

Default Value:	111b
Access:	R/W

L3 Aging Counter for SNOOP:
Aging Counter for Snoop Port.
lbcf_csr_lc_snp_aging_cnt[3:0].

L3CNTLREG1 - L3 Control Register1

	3:0	**Fill aging for port1** Default Value: 1111b Access: R/W Fill aging (L3AGF): Aging Counter for Fill port 1. lbcf_csr_lc_fill1_aging_cnt[3:0]. If bit B103.19 is 0 then this register value has to be nonzero.

L3 LRA 0 GPGPU

L3_LRA_0_GPGPU - L3 LRA 0 GPGPU		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x0400FC00	
Size (in bits):	32	
Address:	04DD0h	
DWord	**Bit**	**Description**
0	31:30	**L3 GPGPU** Default Value: 00b Access: R/W Which LRA should L3 use.
	29:20	**L3 LRA1 Min GPGPU** Default Value: 0001000000b Access: R/W Minimum value of programmable LRA1.
	19:10	**L3 LRA0 Max GPGPU** Default Value: 0000111111b Access: R/W Maximum value of programmable LRA0.
	9:0	**L3 LRA0 Min GPGPU** Default Value: 0000000000b Access: R/W Minimum value of programmable LRA0.

L3 LRA 1 GPGPU

L3_LRA_1_GPGPU - L3 LRA 1 GPGPU		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x5FF6C1AF	
Size (in bits):	32	
Address:	04DD4h	
DWord	**Bit**	**Description**
0	31:30	**DC GPGPU** Default Value: 01b Access: R/W Which LRA should DC use.
	29:20	**L3 LRA2 Max GPGPU** Default Value: 0111111111b Access: R/W Maximum value of programmable LRA2.
	19:10	**L3 LRA2 Min GPGPU** Default Value: 0110110000b Access: R/W Minimum value of programmable LRA2.
	9:0	**L3 LRA1 Max GPGPU** Default Value: 0110101111b Access: R/W Maximum value of programmable LRA1.

L3 LRA 0 3D

L3_LRA_0_3D - L3 LRA 0 3D

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0400FC00
Size (in bits):	32
Address:	04A10h

DWord	Bit	Description
0	31:30	**L3 3D** Default Value: 00b Access: R/W Which LRA should L3 use.
	29:20	**L3 LRA1 Min 3D** Default Value: 0001000000b Access: R/W Minimum value of programmable LRA1.
	19:10	**L3 LRA0 Max 3D** Default Value: 0000111111b Access: R/W Maximum value of programmable LRA0.
	9:0	**L3 LRA0 Min 3D** Default Value: 0000000000b Access: R/W Minimum value of programmable LRA0.

L3 LRA 1 3D

L3_LRA_1_3D - L3 LRA 1 3D

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x5EF2408F
Size (in bits):	32
Address:	04A14h

DWord	Bit	Description
0	31:30	**DC 3D** Default Value: 01b Access: R/W Which LRA should DC use.
	29:20	**L3 LRA2 Max 3D** Access: R/W Maximum value of programmable LRA2. Value: 0111101111b — Name: **[Default]**
	19:10	**L3 LRA2 Min 3D** Default Value: 0010010000b Access: R/W Minimum value of programmable LRA2.
	9:0	**L3 LRA1 Max 3D** Default Value: 0010001111b Access: R/W Maximum value of programmable LRA1.

L3 LRA 2 3D

L3_LRA_2_3D - L3 LRA 2 3D

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x007FDF0E
Size (in bits):	32
Address:	04A18h

DWord	Bit	Description
0	31:24	**Reserved** Default Value: 00000000b Access: RO
	23:14	**L3 LRA3 Max 3D** Default Value: 0111111111b Access: R/W Maximum value of programmable LRA2. If L3LRA3Min_3D == L3LRA3Max_3D , GATR LRA is disabled, GATR cycles are mapped to L3LRA0 If L3LRA3Min_3D == L3LRA3Max_3D , GATR LRA is disabled, L3LRA2Max_3D will default to L3LRA3Max_3D to reuse GATR entries
	13:4	**L3 LRA3 Min 3D** Default Value: 0111110000b Access: R/W Minimum value of programmable LRA3.
	3:2	**GATR_3D** Default Value: 11b Access: R/W Which LRA should GATR use.
	1:0	**Texture 3D** Default Value: 10b Access: R/W Which LRA should Texture use.

L3 SQC register 4

L3SQCREG4 - L3 SQC register 4		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x40400000	
Size (in bits):	32	
Address:	0B118h	

DWord	Bit	Description
0	31	**Reserved**
	30	**L3SQ URB Read CAM Match Disable** Default Value: 1b Access: R/W L3SQ URB Read CAM Match Disable (SQURBRDCAMDIS): Disables the L3SQ Cam Match ability for URB Reads. By disabling, this allows a performance mode where URB reads are not dependent upon one another but only on any previous URB writes to the same address. This allows many URB reads to the same cacheline at any given time instead of serializing the requests. 1 = URB Read CAM matching is disabled; multiple URB reads to the same cacheline are allowed to be concurrent (default). 0 = URB Read CAM matching is enabled; multiple URB reads to the same cacheline are serialized. lbcf_csr_lsqc_urbrdcam_dis.
	29:28	**Traffic regulation in LSQC for URB lookup traffic** Default Value: 00b Access: R/W Traffic regulation in LSQC for URB lookup traffic (URB lookups are issued to ltcc these many clocks apart). 00b - Continuous. 01b - 4 clocks apart. 10b - 8 clocks apart. 11b - 16 clocks apart. lbcf_lsqc_urb_traffic.
	27	**LQSC RO PERF DIS** Default Value: 0b Access: R/W Default: 0. when set, RO performance mode is disabled and all Reads proceed only after Parent recycles. lbcf_csr_lsqc_roperf_dis.

L3SQCREG4 - L3 SQC register 4

	26	**Order Cam Snp Reject** Default Value: 0b Access: R/W Default: 0. when set, all slots resulting in matches to snp addr result in snprsp as REJECT instead of MISS. lbcf_csr_lsqc_ordercam_snpreject.
	25	**LQSC RW PERF DIS** Default Value: 0b Access: R/W Default: 0. 0: Performance mode is enabled. when set, Rd to RW performance mode is disabled and all cycles proceed only after Parent recycles. lbcf_csr_lsqc_rwperf_dis.
	24	**LSQC read rtrn local crdt pre-consume disable** Default Value: 0b Access: R/W 0 - Default, LSQD consumes the LNE local slicecredit when read return pending. 1 - LSQD consumes read rtrn credit in the clock it is ready to send read return data. lbcf_csr_lsqd_rdtrn_precrdt_dis.
	23	**LSQC Mem Write sqcam HITM response disable** Default Value: 0b Access: R/W 0 - Default. 1 - This disables any Memory Write from cache with HitM tag response to respond for SQCAMs. lbcf_csr_lsqc_sqcam_l3tagrsphitm_dis.
	22	**Non-IA coherent atomics enable** Default Value: 1b Access: R/W 0: Atomics in GTI. 1: Atomics in L3 (non-IA atomic) (default). lbcf_csr_lsqc_glblatmcs_l3. Value of this bit should be same as LNCF register bit 0xb008[0]. Value of this bit should be same as LBCF register bit 0xb11c[8].

L3SQCREG4 - L3 SQC register 4

	21	**Pipe line flush Coherent lines** Default Value: 0b Access: R/W 1: Treat pipeline flush as invalidating even coherent lines along with non coherent lines . 0: Flush invalidates non coherent lines only. lbcf_csr_lsqc_pipeflush_coh.
	20:6	**Reserved** Access: RO
	5	**ltcd b2b 2x dis** Default Value: 0b Access: R/W 0-ltcd b2b 2x feature enabled 1-ltcd b2b 2x feature disabled ltcd_ltcd_b2b_2x_dis
	4	**lslm b2b 2x dis** Default Value: 0b Access: R/W 0-lslm b2b 2x feature enabled 1-lslm b2b 2x feature disabled lbcf_lslm_b2b_2x_dis
	3	**lslm flush denorm** Default Value: 0b Access: R/W lbcf_csr_lslm_flush_denorm_to_zero When this bit is enabled (1b), Floating Point SLM atomics output will be flushed to zero if it is a De-Norm.
	2	**lsqc disable sla coh** Default Value: 0b Access: R/W lbcf_lsqc_disable_sla_coh If this bit is set to 1b, it will disable Short loop atomics access for Coherent atomics.
	1	**lsqc disable sla** Default Value: 0b Access: R/W lbcf_lsqc_disable_sla

L3SQCREG4 - L3 SQC register 4

		If this bit is set to 1b, it will disable Short loop atomics access for Coherent and non-coherent atomics. In BXT, if L3SQCREG4[LTCD_B2B_2X_DIS] (B118[5]) is set to 1, then this bit needs to be set to 1
	0	**lsqd flush denorm** Default Value: 0b Access: R/W lbcf_csr_lsqd_flush_denorm_to_zero When this bit is enabled (1b), Floating Point atomics output will be flushed to zero if it is a De-Norm.

L3 SQC registers 1

L3SQCREG1 - L3 SQC registers 1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00E10000
Size (in bits):	32
Address:	0B100h

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Reserved.
	23:19	**L3SQ General Priority Credit Initialization** Default Value: 11100b Access: R/W L3SQ General Priority Credit Initialization (SQGPCI): Number of general and high priority credits that SQ presents to L3 Arbiter blocks This inherently also determines the depth of the SQ; reduce the number of credits and SQ uses fewer slots. This field can be programmed only after a stalling flush (HSD:2133794/2133796/2134058) Any value not listed here is considered Reserved. Gen priority credits is always greater than high priority credits. Value # General Credits 00000b 0 00001b 2 00010b 4 00011b 6 00100b 8 00101b 10 00110b 12 00111b 14 01000b 16 01001b

L3SQCREG1 - L3 SQC registers 1

		18 01010b 20 01011b 22 01100b 24 01101b 26 01110b 28 01111b 30 10000b 32 ... 11100b 56 (default) Other values are not possible. Can go up to 62 credits. lbcf_csr_lsqc_gen_credit_init[4:0].
	18:14	**L3SQ High Priority Credit Initialization** Default Value: 00100b Access: R/W L3SQ High Priority Credit Initialization (SQHPCI): Number of general and high priority credits that SQ presents to L3 Arbiter blocks. This inherently also determines the depth of the SQ; reduce the number of credits and SQ uses fewer slots. This field can be programmed only after a stalling flush (HSD:2133794/2133796/2134058) Any value not listed here is considered Reserved. gen priority credits is always greater than high priority credits. Value # High Pri Credits 00000b 0 00001b 2 00010b 4 00011b 6 00100b 8 (default) 00101b 10

L3SQCREG1 - L3 SQC registers 1

		00110b 12 00111b 14 01000b 16 01001b 18 01010b 20 01011b 22 01100b 24 01101b 26 01110b 28 01111b 30 10000b 32 ... 11111b 62 Can to go up to 62 credits for BXT-SOC_BIG. lbcf_csr_lsqc_hp_credit_init[4:0] + lbcf_csr_lsqc_gen_credit_init[4:0] should always be less than or equal to 62(BXT-SOC_BIG). lbcf_csr_lsqc_hp_credit_init[4:0].
	13:10	**Reserved** Access: RO Reserved.
	9	**L3SQ Read Once Enable for Sampler Client** Access: R/W L3SQ Read Once Enable for Sampler Client (SQROE): Enables Read Once indications to L3 Cache from SQ. Once enabled, any reads from Sampler client (MT) are sent as Read Once. 0 = (default) Reads from Sampler clients issue Read to L3 Cache. 1 = Reads from Sampler clients issue Read Once to L3 Cache. lbcf_csr_sampler_readonce_en.

L3SQCREG1 - L3 SQC registers 1

	8:6	**Reserved** Access: RO Reserved.
	5:3	**L3SQ Outstanding L3 Fills** Access: R/W L3SQ Outstanding L3 Fills (SQOUTSL3F): Identifies the number of L3 Fills that can be outstanding before SQ throttles the fill requests to L3 Cache. This is not an exact limit, but instead it is used as a threshold to throttling. Once the fill count is greater than or equal to the threshold, then no fills are issued until the fill responses are received to bring the outstanding count back below the threshold. 000b = (default) No limit. 001b = 1 fill. 010b = 2 fills. 011b = 4 fills. 100b = 8 fills. 101b = 16 fills. 11Xb = Reserved. lbcf_csr_lsqc_outs_fill[2:0].
	2:0	**L3SQ Outstanding L3 Lookups** Access: R/W L3SQ Outstanding L3 Lookups (SQOUTSL3L): Identifies the number of L3 lookups that can be outstanding before SQ throttles the lookup requests to L3 Cache. This is not an exact limit, but instead it is used as a threshold to throttling. once the lookup count is greater than or equal to the threshold, then no lookups are issued until the lookup responses are received to bring the outstanding count back below the threshold. 000b = (default) No limit. 001b = 1 lookup. 010b = 2 lookups. 011b = 4 lookups. 100b = 8 lookups. 101b = 16 lookups. 11Xb = Reserved. lbcf_csr_lsqc_outs_lookup[2:0].

MAILBOX0

MAILBOX0 - MAILBOX0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	120800h	
This register contains bits 31:0 of the generic descriptor, fetched from the invalidate queue for GT.		
DWord	**Bit**	**Description**
0	31:0	**DATA** Default Value: 00000000h Access: R/W This field contains bits 31:0 of the generic descriptor, fetched from the invalidate queue for GT.

MAILBOX1

MAILBOX1 - MAILBOX1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	120804h

This register contains bits 63:32 of the generic descriptor, fetched from the invalidate queue for GT.

DWord	Bit	Description
0	31:0	**DATA** Default Value: 00000000h Access: R/W This field contains bits 63:32 of the generic descriptor, fetched from the invalidate queue for GT.

MAILBOX2

MAILBOX2 - MAILBOX2		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	120808h	
This register contains bits 95:64 of the generic descriptor, fetched from the invalidate queue for GT.		
DWord	**Bit**	**Description**
0	31:0	**DATA** Default Value: 00000000h Access: R/W This field contains bits 95:64 of the generic descriptor, fetched from the invalidate queue for GT.

MAILBOX3

MAILBOX3 - MAILBOX3

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	12080Ch

This register contains bits 127:96 of the generic descriptor, fetched from the invalidate queue for GT.

DWord	Bit	Description
0	31:0	**DATA** Default Value: 00000000h Access: R/W This field contains bits 127:96 of the generic descriptor, fetched from the invalidate queue for GT.

Master Latency Timer

MLT2_0_2_0_PCI - Master Latency Timer		
Register Space:	PCI: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	8	
Address:	0000Dh	
The IGD does not support the programmability of the master latency timer because it does not perform bursts.		
DWord	**Bit**	**Description**
0	7:0	**Master Latency Timer Count Value** Default Value: 00000000b Access: RO Hardwired to 0s.

Maximum Latency

MAXLAT_0_2_0_PCI - Maximum Latency		
Register Space:	PCI: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	8	
Address:	0003Fh	
The Integrated Graphics Device has no requirement for the settings of Latency Timers.		
DWord	**Bit**	**Description**
0	7:0	**Maximum Latency Value** Default Value: 00000000b Access: RO Hardwired to 0s because the IGD has no specific requirements for how often it needs to access the PCI bus.

MBDSM

MBDSM - MBDSM

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	1080C0h

This register contains the base address of graphics data stolen DRAM memory. BIOS determines the base of graphics data stolen memory by subtracting the graphics data stolen memory size (PCI Device 0 offset 52 bits 7:4) from TOLUD (PCI Device 0 offset BC bits 31:20).

DWord	Bit	Description
0	31:20	**BDSM** Default Value: 000h Access: RO This BitField contains bits 31 to 20 of the base address of stolen DRAM memory. BIOS determines the base of graphics stolen memory by subtracting the graphics stolen memory size (PCI Device 0 offset 50 bits 15:8) from TOLUD (PCI Device 0 offset BC bits 31:20).
	19:1	**RESERVED** Default Value: 000h Access: RO Reserved
	0	**LOCK** Default Value: 0b Access: RO This bit will lock all writeable settings in this register, including itself.

MBGSM

MBGSM - MBGSM

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00100000
Size (in bits):	32
Address:	108100h

This register contains the base address of stolen DRAM memory for the GTT. BIOS determines the base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI Device 0 offset 52 bits 9:8) from the Graphics Base of Data Stolen Memory (PCI Device 0 offset B0 bits 31:20).

DWord	Bit	Description
0	31:20	**BGSM** Default Value: 001h Access: RO This register contains the base address of stolen DRAM memory for the GTT. BIOS determines the base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI Device 0 offset 50 bits 7:6) from the Graphics Base of Data Stolen Memory (PCI Device 0 offset B0 bits 31:20).
	19:1	**RESERVED** Default Value: 000h Access: RO Reserved
	0	**LOCK** Default Value: 0b Access: RO This bit will lock all writeable settings in this register, including itself.

MCHBAR_LSB

MCHBAR_LSB - MCHBAR_LSB

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	06C88h

This is the base address for the Graphics VT configuration space.
There is no physical memory within this 4KB window that can be addressed.
The 4KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space.
On reset, the GFX-VT configuration space is disabled and must be enabled by writing a 1 to GFX-VTBAREN.
All the bits in this register are locked in Intel TXT mode.
BIOS programs this register after which the register cannot be altered.

DWord	Bit	Description
0	31:12	**GFXVTBAR** Default Value: 000000h Access: R/W Lock This field corresponds to bits 38 to 12 of the base address GFX-VT configuration space. BIOS will program this register resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within the first 512GB of addressable memory space. System Software uses this base address to program the GFX-VT register set. All the Bits in this register are locked in Intel TXT mode.
	11:2	**RESERVED** Default Value: 000h Access: RO Reserved
	1	**LOCK** Default Value: 000h Access: R/W Lock Lock
	0	**GFXVTBAREN** Default Value: 0b Access: R/W Lock 0: GFX-VTBAR is disabled and does not claim any memory. 1: GFX-VTBAR memory mapped accesses are claimed and decoded appropriately This bit will remain 0 if VTd capability is disabled.

MCHBAR_MSB

MCHBAR_MSB - MCHBAR_MSB

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	06C8Ch

This is the base address for the Graphics VT configuration space. There is no physical memory within this 4KB window that can be addressed. The 4KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the GFX-VT configuration space is disabled and must be enabled by writing a 1 to GFX-VTBAREN. All the bits in this register are locked in Intel TXT mode. BIOS programs this register after which the register cannot be altered.

DWord	Bit	Description
0	31:7	**RESERVED** Default Value: 0000000h Access: RO Reserved
	6:0	**GFXVTBAR** Default Value: 00h Access: R/W Lock This field corresponds to bits 38 to 12 of the base address GFX-VT configuration space. BIOS will program this register resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within the first 512GB of addressable memory space. System Software uses this base address to program the GFX-VT register set. All the Bits in this register are locked in Intel TXT mode.

Media0 MOCS Register0

MFX0_MOCS_0 - Media0 MOCS Register0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030
Size (in bits):	32
Address:	0C900h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target

MFX0_MOCS_0 - Media0 MOCS Register0

		Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_0 - Media0 MOCS Register0		
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register1

MFX0_MOCS_1 - Media0 MOCS Register1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034
Size (in bits):	32
Address:	0C904h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target

MFX0_MOCS_1 - Media0 MOCS Register1

		Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_1 - Media0 MOCS Register1		
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register2

MFX0_MOCS_2 - Media0 MOCS Register2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038
Size (in bits):	32
Address:	0C908h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_2 - Media0 MOCS Register2

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_2 - Media0 MOCS Register2		
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register3

MFX0_MOCS_3 - Media0 MOCS Register3

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031
Size (in bits):	32
Address:	0C90Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_3 - Media0 MOCS Register3

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_3 - Media0 MOCS Register3		
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register4

MFX0_MOCS_4 - Media0 MOCS Register4

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0C910h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_4 - Media0 MOCS Register4

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_4 - Media0 MOCS Register4		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register5

MFX0_MOCS_5 - Media0 MOCS Register5

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0C914h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_5 - Media0 MOCS Register5

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_5 - Media0 MOCS Register5		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register6

MFX0_MOCS_6 - Media0 MOCS Register6

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0C918h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_6 - Media0 MOCS Register6

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_6 - Media0 MOCS Register6		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register7

MFX0_MOCS_7 - Media0 MOCS Register7

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0C91Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_7 - Media0 MOCS Register7

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_7 - Media0 MOCS Register7

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register8

MFX0_MOCS_8 - Media0 MOCS Register8

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0C920h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_8 - Media0 MOCS Register8

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_8 - Media0 MOCS Register8		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register9

MFX0_MOCS_9 - Media0 MOCS Register9

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0C924h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_9 - Media0 MOCS Register9

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_9 - Media0 MOCS Register9

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register10

MFX0_MOCS_10 - Media0 MOCS Register10

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0C928h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_10 - Media0 MOCS Register10

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_10 - Media0 MOCS Register10		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register11

MFX0_MOCS_11 - Media0 MOCS Register11

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0C92Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_11 - Media0 MOCS Register11

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_11 - Media0 MOCS Register11

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register12

MFX0_MOCS_12 - Media0 MOCS Register12

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0C930h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_12 - Media0 MOCS Register12

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_12 - Media0 MOCS Register12		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register13

MFX0_MOCS_13 - Media0 MOCS Register13

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0C934h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_13 - Media0 MOCS Register13

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_13 - Media0 MOCS Register13

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register14

MFX0_MOCS_14 - Media0 MOCS Register14

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0C938h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_14 - Media0 MOCS Register14

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_14 - Media0 MOCS Register14

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register15

MFX0_MOCS_15 - Media0 MOCS Register15

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0C93Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_15 - Media0 MOCS Register15

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_15 - Media0 MOCS Register15		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register16

MFX0_MOCS_16 - Media0 MOCS Register16

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030
Size (in bits):	32
Address:	0C940h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_16 - Media0 MOCS Register16

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_16 - Media0 MOCS Register16		
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register17

MFX0_MOCS_17 - Media0 MOCS Register17

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034
Size (in bits):	32
Address:	0C944h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_17 - Media0 MOCS Register17

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_17 - Media0 MOCS Register17

	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register18

MFX0_MOCS_18 - Media0 MOCS Register18

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038
Size (in bits):	32
Address:	0C948h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_18 - Media0 MOCS Register18

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_18 - Media0 MOCS Register18		
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register19

MFX0_MOCS_19 - Media0 MOCS Register19

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031
Size (in bits):	32
Address:	0C94Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_19 - Media0 MOCS Register19

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_19 - Media0 MOCS Register19

	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register20

MFX0_MOCS_20 - Media0 MOCS Register20

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0C950h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_20 - Media0 MOCS Register20

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_20 - Media0 MOCS Register20		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register21

MFX0_MOCS_21 - Media0 MOCS Register21

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0C954h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_21 - Media0 MOCS Register21

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_21 - Media0 MOCS Register21

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register22

MFX0_MOCS_22 - Media0 MOCS Register22

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0C958h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_22 - Media0 MOCS Register22

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_22 - Media0 MOCS Register22		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register23

MFX0_MOCS_23 - Media0 MOCS Register23

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0C95Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_23 - Media0 MOCS Register23

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_23 - Media0 MOCS Register23

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register24

MFX0_MOCS_24 - Media0 MOCS Register24

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0C960h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_24 - Media0 MOCS Register24

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_24 - Media0 MOCS Register24		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register25

MFX0_MOCS_25 - Media0 MOCS Register25

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0C964h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_25 - Media0 MOCS Register25

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_25 - Media0 MOCS Register25

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register26

MFX0_MOCS_26 - Media0 MOCS Register26

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0C968h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_26 - Media0 MOCS Register26

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_26 - Media0 MOCS Register26		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register27

MFX0_MOCS_27 - Media0 MOCS Register27

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0C96Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_27 - Media0 MOCS Register27

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_27 - Media0 MOCS Register27

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register28

MFX0_MOCS_28 - Media0 MOCS Register28

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0C970h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_28 - Media0 MOCS Register28

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_28 - Media0 MOCS Register28		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register29

MFX0_MOCS_29 - Media0 MOCS Register29

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0C974h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_29 - Media0 MOCS Register29

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_29 - Media0 MOCS Register29

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register30

MFX0_MOCS_30 - Media0 MOCS Register30

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0C978h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_30 - Media0 MOCS Register30

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_30 - Media0 MOCS Register30		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register31

MFX0_MOCS_31 - Media0 MOCS Register31

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0C97Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_31 - Media0 MOCS Register31

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_31 - Media0 MOCS Register31

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register32

MFX0_MOCS_32 - Media0 MOCS Register32

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030
Size (in bits):	32
Address:	0C980h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_32 - Media0 MOCS Register32

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_32 - Media0 MOCS Register32		
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register33

MFX0_MOCS_33 - Media0 MOCS Register33

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034
Size (in bits):	32
Address:	0C984h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_33 - Media0 MOCS Register33

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_33 - Media0 MOCS Register33

	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register34

MFX0_MOCS_34 - Media0 MOCS Register34

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038
Size (in bits):	32
Address:	0C988h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_34 - Media0 MOCS Register34

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_34 - Media0 MOCS Register34		
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register35

MFX0_MOCS_35 - Media0 MOCS Register35

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031
Size (in bits):	32
Address:	0C98Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_35 - Media0 MOCS Register35

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_35 - Media0 MOCS Register35

	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register36

MFX0_MOCS_36 - Media0 MOCS Register36

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0C990h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_36 - Media0 MOCS Register36

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_36 - Media0 MOCS Register36		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register37

MFX0_MOCS_37 - Media0 MOCS Register37

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0C994h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_37 - Media0 MOCS Register37

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_37 - Media0 MOCS Register37

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register38

MFX0_MOCS_38 - Media0 MOCS Register38

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0C998h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_38 - Media0 MOCS Register38

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_38 - Media0 MOCS Register38		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register39

MFX0_MOCS_39 - Media0 MOCS Register39

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0C99Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_39 - Media0 MOCS Register39

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_39 - Media0 MOCS Register39

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register40

MFX0_MOCS_40 - Media0 MOCS Register40

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0C9A0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_40 - Media0 MOCS Register40

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_40 - Media0 MOCS Register40		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register41

MFX0_MOCS_41 - Media0 MOCS Register41

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0C9A4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_41 - Media0 MOCS Register41

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_41 - Media0 MOCS Register41

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register42

MFX0_MOCS_42 - Media0 MOCS Register42

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0C9A8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_42 - Media0 MOCS Register42

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_42 - Media0 MOCS Register42		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register43

MFX0_MOCS_43 - Media0 MOCS Register43

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0C9ACh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_43 - Media0 MOCS Register43

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_43 - Media0 MOCS Register43		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register44

MFX0_MOCS_44 - Media0 MOCS Register44

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0C9B0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_44 - Media0 MOCS Register44

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_44 - Media0 MOCS Register44		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register45

MFX0_MOCS_45 - Media0 MOCS Register45

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0C9B4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_45 - Media0 MOCS Register45

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_45 - Media0 MOCS Register45		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register46

MFX0_MOCS_46 - Media0 MOCS Register46

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0C9B8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_46 - Media0 MOCS Register46

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_46 - Media0 MOCS Register46		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register47

MFX0_MOCS_47 - Media0 MOCS Register47

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0C9BCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_47 - Media0 MOCS Register47

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_47 - Media0 MOCS Register47

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register48

MFX0_MOCS_48 - Media0 MOCS Register48

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030
Size (in bits):	32
Address:	0C9C0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_48 - Media0 MOCS Register48

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_48 - Media0 MOCS Register48		
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register49

MFX0_MOCS_49 - Media0 MOCS Register49

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034
Size (in bits):	32
Address:	0C9C4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_49 - Media0 MOCS Register49

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_49 - Media0 MOCS Register49

	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register50

MFX0_MOCS_50 - Media0 MOCS Register50

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038
Size (in bits):	32
Address:	0C9C8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_50 - Media0 MOCS Register50

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_50 - Media0 MOCS Register50		
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register51

MFX0_MOCS_51 - Media0 MOCS Register51

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031
Size (in bits):	32
Address:	0C9CCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_51 - Media0 MOCS Register51

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_51 - Media0 MOCS Register51

	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register52

MFX0_MOCS_52 - Media0 MOCS Register52

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0C9D0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_52 - Media0 MOCS Register52

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_52 - Media0 MOCS Register52		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register53

MFX0_MOCS_53 - Media0 MOCS Register53

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0C9D4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_53 - Media0 MOCS Register53

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_53 - Media0 MOCS Register53

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register54

MFX0_MOCS_54 - Media0 MOCS Register54

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0C9D8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_54 - Media0 MOCS Register54

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_54 - Media0 MOCS Register54		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register55

MFX0_MOCS_55 - Media0 MOCS Register55

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0C9DCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_55 - Media0 MOCS Register55

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_55 - Media0 MOCS Register55		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register56

MFX0_MOCS_56 - Media0 MOCS Register56

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0C9E0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_56 - Media0 MOCS Register56

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_56 - Media0 MOCS Register56		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register57

MFX0_MOCS_57 - Media0 MOCS Register57

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0C9E4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_57 - Media0 MOCS Register57

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_57 - Media0 MOCS Register57

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register58

MFX0_MOCS_58 - Media0 MOCS Register58

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0C9E8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_58 - Media0 MOCS Register58

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_58 - Media0 MOCS Register58		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register59

MFX0_MOCS_59 - Media0 MOCS Register59

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0C9ECh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_59 - Media0 MOCS Register59

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_59 - Media0 MOCS Register59		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register60

MFX0_MOCS_60 - Media0 MOCS Register60

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0C9F0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_60 - Media0 MOCS Register60

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_60 - Media0 MOCS Register60		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register61

MFX0_MOCS_61 - Media0 MOCS Register61

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0C9F4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_61 - Media0 MOCS Register61

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_61 - Media0 MOCS Register61

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register62

MFX0_MOCS_62 - Media0 MOCS Register62

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0C9F8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_62 - Media0 MOCS Register62

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_62 - Media0 MOCS Register62		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register63

MFX0_MOCS_63 - Media0 MOCS Register63

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0C9FCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX0_MOCS_63 - Media0 MOCS Register63

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX0_MOCS_63 - Media0 MOCS Register63		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register0

MFX1_MOCS_0 - Media1 MOCS Register0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030
Size (in bits):	32
Address:	0CA00h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_0 - Media1 MOCS Register0

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_0 - Media1 MOCS Register0		
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register1

MFX1_MOCS_1 - Media1 MOCS Register1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034
Size (in bits):	32
Address:	0CA04h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_1 - Media1 MOCS Register1

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_1 - Media1 MOCS Register1		
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register2

MFX1_MOCS_2 - Media1 MOCS Register2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038
Size (in bits):	32
Address:	0CA08h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_2 - Media1 MOCS Register2

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_2 - Media1 MOCS Register2		
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register3

MFX1_MOCS_3 - Media1 MOCS Register3

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031
Size (in bits):	32
Address:	0CA0Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_3 - Media1 MOCS Register3

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_3 - Media1 MOCS Register3		
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register4

MFX1_MOCS_4 - Media1 MOCS Register4

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CA10h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_4 - Media1 MOCS Register4

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_4 - Media1 MOCS Register4		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register5

MFX1_MOCS_5 - Media1 MOCS Register5

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CA14h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_5 - Media1 MOCS Register5

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_5 - Media1 MOCS Register5		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register6

MFX1_MOCS_6 - Media1 MOCS Register6

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CA18h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_6 - Media1 MOCS Register6

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_6 - Media1 MOCS Register6		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register7

MFX1_MOCS_7 - Media1 MOCS Register7

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CA1Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_7 - Media1 MOCS Register7

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_7 - Media1 MOCS Register7		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register8

MFX1_MOCS_8 - Media1 MOCS Register8

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CA20h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_8 - Media1 MOCS Register8

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_8 - Media1 MOCS Register8

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register9

MFX1_MOCS_9 - Media1 MOCS Register9

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CA24h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_9 - Media1 MOCS Register9

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_9 - Media1 MOCS Register9		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register10

MFX1_MOCS_10 - Media1 MOCS Register10

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CA28h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_10 - Media1 MOCS Register10

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_10 - Media1 MOCS Register10		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register11

MFX1_MOCS_11 - Media1 MOCS Register11

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CA2Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_11 - Media1 MOCS Register11

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_11 - Media1 MOCS Register11

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register12

MFX1_MOCS_12 - Media1 MOCS Register12

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CA30h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_12 - Media1 MOCS Register12

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_12 - Media1 MOCS Register12		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register13

MFX1_MOCS_13 - Media1 MOCS Register13

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CA34h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_13 - Media1 MOCS Register13

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_13 - Media1 MOCS Register13

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register14

MFX1_MOCS_14 - Media1 MOCS Register14

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CA38h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_14 - Media1 MOCS Register14

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_14 - Media1 MOCS Register14		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register15

MFX1_MOCS_15 - Media1 MOCS Register15

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CA3Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_15 - Media1 MOCS Register15

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_15 - Media1 MOCS Register15

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register16

MFX1_MOCS_16 - Media1 MOCS Register16

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030
Size (in bits):	32
Address:	0CA40h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_16 - Media1 MOCS Register16

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_16 - Media1 MOCS Register16		
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register17

MFX1_MOCS_17 - Media1 MOCS Register17

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034
Size (in bits):	32
Address:	0CA44h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_17 - Media1 MOCS Register17

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_17 - Media1 MOCS Register17

	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register18

MFX1_MOCS_18 - Media1 MOCS Register18

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038
Size (in bits):	32
Address:	0CA48h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_18 - Media1 MOCS Register18

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_18 - Media1 MOCS Register18		
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register19

MFX1_MOCS_19 - Media1 MOCS Register19

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031
Size (in bits):	32
Address:	0CA4Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_19 - Media1 MOCS Register19

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_19 - Media1 MOCS Register19

	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register20

MFX1_MOCS_20 - Media1 MOCS Register20

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CA50h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_20 - Media1 MOCS Register20

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_20 - Media1 MOCS Register20		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register21

MFX1_MOCS_21 - Media1 MOCS Register21

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CA54h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_21 - Media1 MOCS Register21

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_21 - Media1 MOCS Register21

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register22

MFX1_MOCS_22 - Media1 MOCS Register22

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CA58h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_22 - Media1 MOCS Register22

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_22 - Media1 MOCS Register22		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register23

MFX1_MOCS_23 - Media1 MOCS Register23

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CA5Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_23 - Media1 MOCS Register23

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_23 - Media1 MOCS Register23

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register24

MFX1_MOCS_24 - Media1 MOCS Register24

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CA60h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_24 - Media1 MOCS Register24

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_24 - Media1 MOCS Register24		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register25

MFX1_MOCS_25 - Media1 MOCS Register25

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CA64h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_25 - Media1 MOCS Register25

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_25 - Media1 MOCS Register25		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register26

MFX1_MOCS_26 - Media1 MOCS Register26

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CA68h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_26 - Media1 MOCS Register26

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_26 - Media1 MOCS Register26		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register27

MFX1_MOCS_27 - Media1 MOCS Register27

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CA6Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_27 - Media1 MOCS Register27

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_27 - Media1 MOCS Register27

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register28

MFX1_MOCS_28 - Media1 MOCS Register28

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CA70h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_28 - Media1 MOCS Register28

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_28 - Media1 MOCS Register28		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register29

MFX1_MOCS_29 - Media1 MOCS Register29

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CA74h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_29 - Media1 MOCS Register29

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_29 - Media1 MOCS Register29

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register30

MFX1_MOCS_30 - Media1 MOCS Register30

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CA78h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_30 - Media1 MOCS Register30

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_30 - Media1 MOCS Register30		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register31

MFX1_MOCS_31 - Media1 MOCS Register31

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CA7Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_31 - Media1 MOCS Register31

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_31 - Media1 MOCS Register31		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register32

MFX1_MOCS_32 - Media1 MOCS Register32

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030
Size (in bits):	32
Address:	0CA80h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_32 - Media1 MOCS Register32

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_32 - Media1 MOCS Register32		
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register33

MFX1_MOCS_33 - Media1 MOCS Register33

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034
Size (in bits):	32
Address:	0CA84h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_33 - Media1 MOCS Register33

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_33 - Media1 MOCS Register33

	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register34

MFX1_MOCS_34 - Media1 MOCS Register34

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038
Size (in bits):	32
Address:	0CA88h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_34 - Media1 MOCS Register34

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_34 - Media1 MOCS Register34		
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register35

MFX1_MOCS_35 - Media1 MOCS Register35

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031
Size (in bits):	32
Address:	0CA8Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_35 - Media1 MOCS Register35

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_35 - Media1 MOCS Register35

	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register36

MFX1_MOCS_36 - Media1 MOCS Register36

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CA90h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_36 - Media1 MOCS Register36

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_36 - Media1 MOCS Register36		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register37

MFX1_MOCS_37 - Media1 MOCS Register37

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CA94h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_37 - Media1 MOCS Register37

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_37 - Media1 MOCS Register37

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register38

MFX1_MOCS_38 - Media1 MOCS Register38

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CA98h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_38 - Media1 MOCS Register38

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_38 - Media1 MOCS Register38		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register39

MFX1_MOCS_39 - Media1 MOCS Register39

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CA9Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_39 - Media1 MOCS Register39

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_39 - Media1 MOCS Register39

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register40

MFX1_MOCS_40 - Media1 MOCS Register40

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CAA0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_40 - Media1 MOCS Register40

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_40 - Media1 MOCS Register40		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register41

MFX1_MOCS_41 - Media1 MOCS Register41

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CAA4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_41 - Media1 MOCS Register41

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_41 - Media1 MOCS Register41		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register42

MFX1_MOCS_42 - Media1 MOCS Register42

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CAA8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_42 - Media1 MOCS Register42

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_42 - Media1 MOCS Register42		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register43

MFX1_MOCS_43 - Media1 MOCS Register43

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CAACh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_43 - Media1 MOCS Register43

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_43 - Media1 MOCS Register43

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register44

MFX1_MOCS_44 - Media1 MOCS Register44

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CAB0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_44 - Media1 MOCS Register44

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_44 - Media1 MOCS Register44		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register45

MFX1_MOCS_45 - Media1 MOCS Register45

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CAB4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_45 - Media1 MOCS Register45

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_45 - Media1 MOCS Register45

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register46

MFX1_MOCS_46 - Media1 MOCS Register46

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CAB8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_46 - Media1 MOCS Register46

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_46 - Media1 MOCS Register46		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register47

MFX1_MOCS_47 - Media1 MOCS Register47

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CABCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_47 - Media1 MOCS Register47

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_47 - Media1 MOCS Register47

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register48

MFX1_MOCS_48 - Media1 MOCS Register48

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030
Size (in bits):	32
Address:	0CAC0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_48 - Media1 MOCS Register48

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_48 - Media1 MOCS Register48		
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register49

MFX1_MOCS_49 - Media1 MOCS Register49

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034
Size (in bits):	32
Address:	0CAC4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_49 - Media1 MOCS Register49

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_49 - Media1 MOCS Register49

	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register50

MFX1_MOCS_50 - Media1 MOCS Register50

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038
Size (in bits):	32
Address:	0CAC8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_50 - Media1 MOCS Register50

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_50 - Media1 MOCS Register50		
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register51

MFX1_MOCS_51 - Media1 MOCS Register51

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031
Size (in bits):	32
Address:	0CACCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_51 - Media1 MOCS Register51

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_51 - Media1 MOCS Register51		
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register52

MFX1_MOCS_52 - Media1 MOCS Register52

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CAD0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_52 - Media1 MOCS Register52

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_52 - Media1 MOCS Register52		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register53

MFX1_MOCS_53 - Media1 MOCS Register53

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CAD4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_53 - Media1 MOCS Register53

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_53 - Media1 MOCS Register53

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register54

MFX1_MOCS_54 - Media1 MOCS Register54

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CAD8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_54 - Media1 MOCS Register54

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_54 - Media1 MOCS Register54		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register55

MFX1_MOCS_55 - Media1 MOCS Register55

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CADCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_55 - Media1 MOCS Register55

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_55 - Media1 MOCS Register55

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register56

MFX1_MOCS_56 - Media1 MOCS Register56

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CAE0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_56 - Media1 MOCS Register56

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_56 - Media1 MOCS Register56		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register57

MFX1_MOCS_57 - Media1 MOCS Register57

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CAE4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_57 - Media1 MOCS Register57

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_57 - Media1 MOCS Register57

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register58

MFX1_MOCS_58 - Media1 MOCS Register58

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CAE8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_58 - Media1 MOCS Register58

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_58 - Media1 MOCS Register58		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register59

MFX1_MOCS_59 - Media1 MOCS Register59

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CAECh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_59 - Media1 MOCS Register59

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_59 - Media1 MOCS Register59

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register60

MFX1_MOCS_60 - Media1 MOCS Register60

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CAF0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_60 - Media1 MOCS Register60

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_60 - Media1 MOCS Register60		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register61

MFX1_MOCS_61 - Media1 MOCS Register61

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CAF4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_61 - Media1 MOCS Register61

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_61 - Media1 MOCS Register61		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register62

MFX1_MOCS_62 - Media1 MOCS Register62

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CAF8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_62 - Media1 MOCS Register62

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_62 - Media1 MOCS Register62		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register63

MFX1_MOCS_63 - Media1 MOCS Register63

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CAFCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

MFX1_MOCS_63 - Media1 MOCS Register63

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

MFX1_MOCS_63 - Media1 MOCS Register63

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media 1 PFET control register with lock

PFETCTL - Media 1 PFET control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0005000A
	0x0007000A
Size (in bits):	32
Address:	24088h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of MEDIA1 PGFETCTL register are R/W 1 = All bits of MEDIA1 PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (that is, writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:21	**Reserved** Access: RO Reserved
	20	**Power Well Status** Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (that is, writing a 0 will not clear the lock). These bits are not reset on FLR.
	19	**Powergood timer error** Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (that is, writing a 0 will not clear the lock). These bits are not reset on FLR.
	18:16	**Delay from enabling secondary PFETs to power good.** Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 320ns

PFETCTL - Media 1 PFET control register with lock

3'b100: 640ns
3'b101: 1280ns
3'b110: 2560ns
3'b111: 5120ns

Value	Name
101b	**[Default]**

15:13 Time period last primay pfet strobe to secondary pfet strobe

Access:	R/W Lock

Time period last primay pfet strobe to secondary pfet strobe
3'b000: 10ns (or 1 bclk)
3'b001: 20ns (or 2 bclk)
3'b010: 30ns (or 3 bclk)
3'b111: 80ns (or 8 bclk)

12:10 Time period b/w two adjacent strobes

Access:	R/W Lock

Time period b/w two adjacent strobes to the primary FETs
3'b000: 10ns (or 1 bclk)
3'b001: 20ns (or 2 bclk)
3'b010: 30ns (or 3 bclk)
3'b111: 80ns (or 8 bclk)

9:7 FET setup margin from enable to strobe

Access:	R/W Lock

Setup margin in design before sampling enable event at the first pre-charge sequencer/shift register flop
3'b000: 10ns (or 1 bclk)
3'b001: 20ns (or 2 bclk)
3'b010: 30ns (or 3 bclk)
3'b111: 80ns (or 8 bclk)

6:0 Number of flops to enable primary FETs

Access:	R/W Lock

Number of flops to enable primary FETs. For a setting of N there will be N+1 total strobes generated
7'b0000000: 10 Flops to be strobed
7'b0000001: 11 Flops to be strobed
7'b0000010: 12 Flops to be strobed
7'b0001111: 26 Flops to be strobed

Value	Name
0001010b	**[Default]**

MEMRR_BASE_LSB

MEMRR_BASE_LSB - MEMRR_BASE_LSB

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	108340h

The EMRR range is used to protect Xucode memory from unauthorized reads and writes. Any IO access to this range is aborted. This register controls the location of the EMRR range by indicating its starting address. It functions in tandem with the EMRR mask register.

DWord	Bit	Description
0	31:12	**RANGE_BASE** Default Value: 0000000h Access: RO This field corresponds to bits 38:12 of the base address memory range which is allocated to EMRR memory.
	11:0	**RESERVED** Default Value: 000h Access: RO Reserved

MEMRR_BASE_MSB

MEMRR_BASE_MSB - MEMRR_BASE_MSB

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	108344h

The EMRR range is used to protect Xucode memory from unauthorized reads and writes. Any IO access to this range is aborted. This register controls the location of the EMRR range by indicating its starting address. It functions in tandem with the EMRR mask register.

DWord	Bit	Description
0	31:7	**RESERVED** Default Value: 00000000h Access: RO Reserved
	6:0	**RANGE_BASE** Default Value: 000h Access: RO This field corresponds to bits 38:12 of the base address memory range which is allocated to EMRR memory.

MEMRR_MASK_LSB

MEMRR_MASK_LSB - MEMRR_MASK_LSB

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	108380h

This register controls the size of the EMRR range by indicating which address bits must match the EMRR base register value.

DWord	Bit	Description
0	31:12	**RANGE_BASE** Default Value: 0000000h Access: RO This field indicates which address bits must match EMRR base in order to qualify as an EMRR access.
	11	**RANGE_EN** Default Value: 0b Access: RO Indicates whether the EMRR range is enabled and valid.
	10	**LOCK** Default Value: 0b Access: RO Setting this bit locks all writeable settings in this register, including itself.
	9:0	**RESERVED** Default Value: 000h Access: R/W Reserved

MEMRR_MASK_MSB

MEMRR_MASK_MSB - MEMRR_MASK_MSB

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	108384h

This register controls the size of the EMRR range by indicating which address bits must match the EMRR base register value.

DWord	Bit	Description
0	31:7	**RESERVED** Default Value: 00000000h Access: RO Reserved
	6:0	**RANGE_MASK** Default Value: 000h Access: RO This field indicates which address bits must match EMRR base in order to qualify as an EMRR access.

Message Address

MA_0_2_0_PCI - Message Address

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	000B0h

This register contains the Message Address for MSIs sent by the device.

DWord	Bit	Description
0	31:2	**Message Address** Default Value: 00000000000000000000000000000000b Access: R/W Used by system software to assign an MSI address to the device. The device handles an MSI by writing the padded contents of the MD register to this address.
	1:0	**Force Dword Align** Default Value: 00b Access: RO Hardwired to 0 so that addresses assigned by system software are always aligned on a DWORD address boundary.

Message Control

MC_0_2_0_PCI - Message Control

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	16
Address:	000AEh

Message Signaled Interrupt control register. System software can modify bits in this register, but the device is prohibited from doing so. If the device writes the same message multiple times, only one of those messages is guaranteed to be serviced. If all of them must be serviced, the device must not generate the same message again until the driver services the earlier one.

DWord	Bit	Description
0	15:8	**RESERVED** Default Value: 000b Access: RO Reserved
	7	**64 Bit Capable** Default Value: 0b Access: RO Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message address register and is incapable of generating a 64-bit memory address.
	6:4	**Multiple Message Enable** Default Value: 000b Access: R/W System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested. Value: Number of requests 000: 1 001: 2 010: 4 011: 8 100: 16 101: 32 110: Reserved 111: Reserved
	3:1	**Multiple Message Capable** Default Value: 000b Access: RO System Software reads this field to determine the number of messages being requested by this device.

MC_0_2_0_PCI - Message Control

		Hardwired to 000b to indicate number of requests is 1.
	0	**MSI Enable** Default Value: 0b Access: R/W Controls the ability of this device to generate MSIs.

Message Data

MD_0_2_0_PCI - Message Data

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	16
Address:	000B4h

This register contains the Message Data for MSIs sent by the device.

DWord	Bit	Description
0	15:0	**MESSDATA** Default Value: 0000000000000000b Access: R/W Base message data pattern assigned by system software and used to handle an MSI from the device. When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16 bits are always set to 0. The lower 16 bits are supplied by this register.

Message Signaled Interrupts Capability ID

MSI_CAPID_0_2_0_PCI - Message Signaled Interrupts Capability ID

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x0000D005
Size (in bits):	16
Address:	000ACh

When a device supports MSI it can generate an interrupt request to the processor by writing a predefined data item (a message) to a predefined memory address.

DWord	Bit	Description
0	15:8	**Pointer to Next Capability** Default Value: 11010000b Access: RO This is a hardwired pointer to the next item in the capabilities list.
	7:0	**Capability ID** Default Value: 00000101b Access: RO This field is hardwired to the value 05h to identify the CAP_ID as being for MSI registers.

MGCMD

MGCMD - MGCMD

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	108300h

Mirror GT hardware uses for Vtd state.

DWord	Bit	Description
0	31	**TE** Default Value: 0b Access: R/W 0: Disable Vtd DMA remapping 1: Enable Vtd DMA remapping
	30	**SPARE1** Default Value: 0b Access: R/W Reserved. No hardware usage model.
	29	**SPARE2** Default Value: 0b Access: R/W Reserved. No hardware usage model.
	28	**SPARE3** Default Value: 0b Access: R/W Reserved. No hardware usage model.
	27	**SPARE4** Default Value: 0b Access: R/W Reserved. No hardware usage model.
	26	**SPARE5** Default Value: 0b

MGCMD - MGCMD

		Access: R/W Reserved. No hardware usage model.
	25	**Reserved**
	24	**SPARE6** Default Value: 0b Access: R/W Reserved. No HW usage model.
	23	**SPARE7** Default Value: 0b Access: R/W Reserved. No HW usage model.
	22:0	**RESERVED** Default Value: 00000000h Access: RO Reserved

Minimum Grant

MINGNT_0_2_0_PCI - Minimum Grant		
Register Space:	PCI: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	8	
Address:	0003Eh	
The Integrated Graphics Device has no requirement for the settings of Latency Timers.		
DWord	**Bit**	**Description**
0	7:0	**Minimum Grant Value** Default Value: 00000000b Access: RO Hardwired to 0s because the IGD does not burst as a PCI compliant master.

MIPI_AUTOPWG

MIPI_AUTOPWG	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B0C8h-6B0CBh
Name:	MIPIA_AUTOPWG
ShortName:	MIPIA_AUTOPWG
Power:	PG1
Reset:	soft
Address:	6B8C8h-6B8CBh
Name:	MIPIC_AUTOPWG
ShortName:	MIPIC_AUTOPWG
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:1	**RESERVED** Format: MBZ
	0	**MIPI_AUTO_PWG_ENABLE** Access: R/W SW driver writes to this bit to enable auto power gating for MIPI

MIPI_CLK_LANE_SWITCHING_TIME_CNT

MIPI_CLK_LANE_SWITCHING_TIME_CNT

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B088h-6B08Bh
Name:	MIPIA_CLK_LANE_SWITCHING_TIME_CNT
ShortName:	MIPIA_CLK_LANE_SWITCHING_TIME_CNT
Power:	PG1
Reset:	soft
Address:	6B888h-6B88Bh
Name:	MIPIC_CLK_LANE_SWITCHING_TIME_CNT
ShortName:	MIPIC_CLK_LANE_SWITCHING_TIME_CNT
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:16	**LS_HS_SSW_CNT** Access: R/W Low power to high speed switching time in terms byte clock (txbyteclkhs). This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc). Typical value - Number of byte clocks required to switch from low power mode to high speed mode after txrequesths_clk is asserted. Current Value is ah = 10 txbyteclkhs
	15:0	**HS_LS_PWR_SW_CNT** Access: R/W High speed to low power switching time in terms byte clock (txbyteclkhs). This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc). Typical value - Number of byte clocks request to switch from high speed mode to low power mode after txrequesths_clk is de-asserted. Current Value is 14h = 20 txbyteclkhs

MIPI_CLOCK_CTL

MIPI_CLOCK_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x6C006C00
Access:	R/W
Size (in bits):	32

Address:	46090h-46093h
Name:	MIPI Clock Control
ShortName:	MIPI_CLOCK_CTL
Power:	Always on
Reset:	soft

This register configures the additional MIPI clock dividers.
MIPI1 fields are used for transcoder MIPI A. MIPI2 fields are used for transcoder MIPI C.

Restriction
Restriction : The Tx escape clock must be as close as possible to, but not exceeding, 20 MHz.
Restriction : The Rx escape clock must be programmed to be as close as possible to, but not exceeding, 150 MHz.

DWord	Bit	Description
0	31:26	**MIPI1 Variable Divider** Default Value: 011011b **Description** Tx Escape Clock Divider: This field specifies the amount to divide the MIPI 8X clock to create the Tx escape clock. Program with the desired value -1.
	25	**Spare 25**
	24	**Spare 24**
	23	**Spare 23**
	22:21	**MIPI1 Controller Divider** **Description** Rx Escape Clock Divider Upper: This field, concatenated with Rx Escape Clock Divider Lower value, specifies the amount to divide the MIPI 8X clock to create the RX escape clock. Program the combined value of the upper and lower fields with the desired value -1.
	20:19	**MIPI1 8by3X Divider** **Description** This field specifies the amount to divide the MIPI 8X clock to create the MIPI 8/3X clock.

MIPI_CLOCK_CTL

Value	Name	Description
00b	Reserved	
01b	Divide by 2	
10b	Divide by 3	Use divide by 3 for both DPI and DBI modes
11b	Divide by 4	

18	**Spare 18**
17:16	**MIPI1 DPHY Divider** **Description** Rx Escape Clock Divider Lower: This field, concatenated with Rx Escape Clock Divider Upper value, specifies the amount to divide the MIPI 8X clock to create the RX escape clock. Program the combined value of the upper and lower fields with the desired value -1.
15:10	**MIPI2 Variable Divider** Default Value: 011011b Divide by 28 **Description** Tx Escape Clock Divider: This field specifies the amount to divide the MIPI 8X clock to create the Tx escape clock. Program with the desired value -1.
9	**Spare 9**
8	**Spare 8**
7	**Spare 7**
6:5	**MIPI2 Controller Divider** **Description** Rx Escape Clock Divider Upper: This field, concatenated with Rx Escape Clock Divider Lower value, specifies the amount to divide the MIPI 8X clock to create the RX escape clock. Program the combined value of the upper and lower fields with the desired value -1.
4:3	**MIPI2 8by3X Divider** **Description** This field specifies the amount to divide the MIPI 8X clock to create the MIPI 8/3X clock.
2	**Spare 2**

MIPI_CLOCK_CTL		
	1:0	**MIPI2 DPHY Divider** **Description** Rx Escape Clock Divider Lower: This field, concatenated with Rx Escape Clock Divider Upper value, specifies the amount to divide the MIPI 8X clock to create the RX escape clock. Program the combined value of the upper and lower fields with the desired value -1.

MIPI_CTRL

MIPI_CTRL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B104h-6B107h
Name:	MIPIA_CTRL
ShortName:	MIPIA_CTRL
Power:	PG1
Reset:	soft
Address:	6B904h-6B907h
Name:	MIPIC_CTRL
ShortName:	MIPIC_CTRL
Power:	PG1
Reset:	soft

Restriction
Restriction : Changing this register can only be done when the MIPI device_ready is turned OFF

DWord	Bit	Description
0	31	**Reserved** Format: MBZ
	30	**Reserved** Format: MBZ
	29	**Reserved** Format: MBZ
	28	**Reserved** Format: MBZ
	27:26	**Reserved** Format: MBZ
	25	**Reserved** Format: MBZ
	24:23	**Reserved** Format: MBZ

MIPI_CTRL

22:20	**Reserved**	
	Format:	MBZ
19:17	**Reserved**	
	Format:	MBZ
16	**Reserved**	
	Format:	MBZ
15:14	**Reserved**	
	Format:	MBZ
9:7	**Pipe Select**	
	Access:	R/W

These bits determine which Pipe this MIPI port will connect to.
It is not valid to enable and direct more than one pipe to one MIPI port.

Value	Name
000b	Pipe A
001b	Pipe B
010b	Pipe C
Others	Reserved

6:4	**RESERVED**	
	Format:	MBZ
3	**DSC Enable**	

This bit enables Display Stream Compression. It is double buffered to the rising edge of vblank.

Value	Name
0b	DSC Disable **[Default]**
1b	DSC Enable

2	**RGB FLIP**	
	Access:	R/W

Value	Name	Description
0b	Enable	DPI mode: RGB data from display pipe is flipped before MIPI IP and in MIPI IP. Result is RGB. DBI mode: RGB data from display pipe is flipped before MIPI IP. Result is BGR.
1b	Disable	DPI mode: RGB data from display pipe is flipped in MIPI IP. Result is BGR. DBI mode: RGB data from display pipe is not flipped. Result is RGB.

Programming Notes
The behavior of this setting is different between DPI and DBI.

MIPI_CTRL		
	1:0	**RESERVED** Format: MBZ

MIPI_DBI_BW_CTRL_REG

MIPI_DBI_BW_CTRL_REG	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B084h-6B087h
Name:	MIPIA_DBI_BW_CTRL_REG
ShortName:	MIPIA_DBI_BW_CTRL_REG
Power:	PG1
Reset:	soft
Address:	6B884h-6B887h
Name:	MIPIC_DBI_BW_CTRL_REG
ShortName:	MIPIC_DBI_BW_CTRL_REG
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:0	**BANDWIDTH_TIMER** Access: R/W DBI Bandwidth control Register. The bandwidth essential for transmitting 16 long packets containing 252 bytes meant for DCS write memory command is programmed in this register in terms of byte clocks. Based on the DSI transfer rate and the number of lanes configured the time taken to transmit 16 long packets in a DSI stream varies.Note: The value programmed in this timer must be greater than the actual time taken to carryout 16 long packets transmission in DSI stream plus the time taken to transmit two blanking packets

MIPI_DBI_FIFO_THRTL_REG

MIPI_DBI_FIFO_THRTL_REG

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B024h-6B027h
Name:	MIPIA_DBI_FIFO_THRTL_REG
ShortName:	MIPIA_DBI_FIFO_THRTL_REG
Power:	PG1
Reset:	soft
Address:	6B824h-6B827h
Name:	MIPIC_DBI_FIFO_THRTL_REG
ShortName:	MIPIC_DBI_FIFO_THRTL_REG
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:2	**RESERVED** Format: MBZ
	1:0	**DBI_FIFO_THRTL** Access: R/W DBI FIFO's watermark can be set using the following bits so as to enable dbi_stall de-assertion whenever the below FIFO condition is reached

Value	Name	Description
00b	half	(1/2) DBI fifo empty
01b	quarter	(1/4) DBI fifo empty
10b	empty	7 locations are empty
11b	Reserved	

MIPI_DEVICE_READY_REG

MIPI_DEVICE_READY_REG	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B000h-6B003h
Name:	MIPIA_DEVICE_READY_REG
ShortName:	MIPIA_DEVICE_READY_REG
Power:	PG1
Reset:	soft
Address:	6B800h-6B803h
Name:	MIPIC_DEVICE_READY_REG
ShortName:	MIPIC_DEVICE_READY_REG
Power:	PG1
Reset:	soft

MIPI Device Ready Register

DWord	Bit	Description
0	31:4	**RESERVED** Format: MBZ
	3	**BUS_POSSESSION** Access: R/W
	2:1	**ULPS_STATE** Access: R/W
	0	**DEVICE_READY_** Access: R/W Set by the processor to inform that device is ready

MIPI_DEVICE_RESET_TIMER

MIPI_DEVICE_RESET_TIMER	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B01Ch-6B01Fh
Name:	MIPIA_DEVICE_RESET_TIMER
ShortName:	MIPIA_DEVICE_RESET_TIMER
Power:	PG1
Reset:	soft
Address:	6B81Ch-6B81Fh
Name:	MIPIC_DEVICE_RESET_TIMER
ShortName:	MIPIC_DEVICE_RESET_TIMER
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:16	**RESERVED** Format: MBZ
	15:0	**DEVICE_RESET_TIMER** Access: R/W Timeout value to be checked for device to be reset after issuing reset entry command. If the timer expires the DSI Host enters normal operation

MIPI_DLBUFFER_CTRL

MIPI_DLBUFFER_CTRL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B144h-6B147h
Name:	MIPIA Dual Link Buffer Control
ShortName:	MIPIA_DLBUFFER_CTRL
Power:	PG1
Reset:	soft
Address:	6B944h-6B947h
Name:	MIPIC Dual Link Buffer Control
ShortName:	MIPIC_DLBUFFER_CTRL
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31	**ENABLE** Access: R/W This field enables the dual link buffer for DBI mode. 0 – Disable 1 – Enable
	30	**Frame vs Line Buffering** Access: R/W This field selects the buffering boundary. 0 – Begin buffering on a frame boundary 1 – Begin buffering on a line boundary Restriction : Only use the frame boundary setting.
	29:11	**RESERVED** Format: MBZ

MIPI_DLBUFFER_CTRL		
	10:0	**TARGET** Access: R/W This field indicates the number of pixels to hold in the slave link buffer before enabling the timing generator, so the Master and Slave DSI controllers are in sync. Valid only when operating in front back dual link mode. Value should only be programmed for the Slave DSI controller. If bit 31 is set then the target for the Slave DSI controller must be non-zero. Maximum value is 1440 decimal. **Programming Notes** Program target to 1/2 the frame width.

MIPI_DPHY_PARAM_REG

MIPI_DPHY_PARAM_REG

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32

Address:	6B080h-6B083h
Name:	MIPIA_DPHY_PARAM_REG
ShortName:	MIPIA_DPHY_PARAM_REG
Power:	PG1
Reset:	soft

Address:	6B880h-6B883h
Name:	MIPIC_DPHY_PARAM_REG
ShortName:	MIPIC_DPHY_PARAM_REG
Power:	PG1
Reset:	soft

Description

This register needs to be programmed in terms of HSDDR clock count.

DWord	Bit	Description
0	31:24	**EXIT_ZERO_COUNT** Access: R/W THS_0_TIM_UI_CNT and THS_EXIT_TIM_UI_CNT for dphy are programmed as exit zero count by the processor
	23:16	**TRAIL_COUNT** Access: R/W TCLK_POST_TIM_UI_CNT and TCLK_TRAIL_TIM_UI_CNT for dphy are programmed as trail count by the processor
	15:8	**CLK_ZERO_COUNT** Access: R/W TCLK_0_TIM_UI_CNT for dphy is programmed as clk zero count by the processor
	7:0	**PREPARE_COUNT** Access: R/W TCLK_PREP_TIM_UI_CNT and THS_PREP_TIM_UI_CNT for dphy are programmed as prepare count by the processor

MIPI_DPI_CTRL_REG

MIPI_DPI_CTRL_REG

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B048h-6B04Bh
Name:	MIPIA_DPI_CTRL_REG
ShortName:	MIPIA_DPI_CTRL_REG
Power:	PG1
Reset:	soft
Address:	6B848h-6B84Bh
Name:	MIPIC_DPI_CTRL_REG
ShortName:	MIPIC_DPI_CTRL_REG
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:8	**RESERVED** Format: MBZ
	7	**RSTTRG** Access: R/W
	6	**HS_LP** Access: R/W Set to '0' to indicate the special packets are sent through the DSI link using HS transmission and set to '1' to indicate that the special packets are sent through the DSI link using low power mode Value / Name / Description: 0 / High Speed / special packets are sent through the DSI link using HS transmission 1 / Low Power / special packets are sent through the DSI link using low power mode
	5	**BACK_LIGHT_OFF** Access: R/W Set to '1' to indicate a backlight OFF short packet has to be packetised for the DPI's virtual channel

MIPI_DPI_CTRL_REG

	4	**BACK_LIGHT_ON** Access: R/W Set to '1' to indicate a backlight ON short packet has to be packetised for the DPI's virtual channel
	3	**COLOR_MODE_OFF** Access: R/W Set to '1' to indicate a color mode OFF short packet has to be packetised for the DPI's virtual channel
	2	**COLOR_MODE_ON** Access: R/W Set to '1' to indicate a color mode ON short packet has to be packetised for the DPI's virtual channel
	1	**TURN_ON** Access: R/W Set to '1' to indicate a turn on short packet has to be packetised for the DPI's virtual channel
	0	**SHUT_DOWN** Access: R/W Set to '1' to indicate a shut down short packet has to be packetised for the DPI's virtual channel

MIPI_DPI_DATA_REGISTER

MIPI_DPI_DATA_REGISTER	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B04Ch-6B04Fh
Name:	MIPIA_DPI_DATA_REGISTER
ShortName:	MIPIA_DPI_DATA_REGISTER
Power:	PG1
Reset:	soft
Address:	6B84Ch-6B84Fh
Name:	MIPIC_DPI_DATA_REGISTER
ShortName:	MIPIC_DPI_DATA_REGISTER
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:6	**RESERVED** Format: MBZ
	5:0	**COMMAND_BYTE** Access: R/W Command Byte to represent the new or not defined command bytes usage for special features representation. [Like backlight ON and OFF]. This register should be programmed before the DPI control register is being programmed for backlight ON/OFF

MIPI_DPI_RESOLUTION_REG

MIPI_DPI_RESOLUTION_REG	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B020h-6B023h
Name:	MIPIA_DPI_RESOLUTION_REG
ShortName:	MIPIA_DPI_RESOLUTION_REG
Power:	PG1
Reset:	soft
Address:	6B820h-6B823h
Name:	MIPIC_DPI_RESOLUTION_REG
ShortName:	MIPIC_DPI_RESOLUTION_REG
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:16	**VERTICAL_ADDRESS** Access: R/W Shows the vertical address count in lines
	15:0	**HORIZONTAL_ADDRESS** Access: R/W Shows the horizontal address count in pixels If supported format in video mode is Compressed Image, Data Horizontal address counts in bytes

MIPI_DSI_FUNC_PRG_REG

MIPI_DSI_FUNC_PRG_REG

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000001
Access:	R/W
Size (in bits):	32
Address:	6B00Ch-6B00Fh
Name:	MIPIA_DSI_FUNC_PRG_REG
ShortName:	MIPIA_DSI_FUNC_PRG_REG
Power:	PG1
Reset:	soft
Address:	6B80Ch-6B80Fh
Name:	MIPIC_DSI_FUNC_PRG_REG
ShortName:	MIPIC_DSI_FUNC_PRG_REG
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:16	**RESERVED** Format: MBZ
	15:13	**SUPPORTED_DATA_WIDTH_IN_COMMAND_MODE** Access: R/W

Value	Name
000b	Command Mode not supported
001b	16 bit data
010b	Reserved
011b	Reserved
100b	Reserved
101b	option 2

DWord	Bit	Description
	12:11	**RESERVED_1** Format: MBZ
	10:7	**SUPPORTED_FORMAT_IN_VIDEO_MODE** Access: R/W

MIPI_DSI_FUNC_PRG_REG

Value	Name	Programming Notes
0000b	Video Mode not supported	
0001b	RGB565	
0010b	RGB666	Restriction : The RGB666 format has restrictions on the horizontal resolution. For isolated MIPI, the horizontal resolution must be evenly divisible by 4. For dual link MIPI, 1/2 the horizontal resolution plus the overlapping pixels must be evenly divisible by 4.
0011b	RGB 666 loosely packed format	
0100b	RGB888	

6:5 **CHANNEL_NUMBER_FOR_COMMAND_MODE**

Access:	R/W

Virtual channel number for command mode is programmed by the processor

4:3 **CHANNEL_NUMBER_FOR_VIDEO_MODE**

Access:	R/W

Virtual channel number for video mode is programmed by the processor

2:0 **DATA_LANES_PRG_R_EG**

Default Value:	001b
Access:	R/W

Number of data lanes to be supported is programmed by the processor

MIPI_EN_DLY_CNTR

MIPI_EN_DLY_CNTR

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B0F4h-6B0F7h
Name:	MIPIA_EN_DLY_CNTR
ShortName:	MIPIA_EN_DLY_CNTR
Power:	PG1
Reset:	soft
Address:	6B8F4h-6B8F7h
Name:	MIPIC_EN_DLY_CNTR
ShortName:	MIPIC_EN_DLY_CNTR
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:0	**TG_ENABLE_DELAY_COUNTER** Access: R/W This is the delay value which is counted down to delay the assertion of the ip_fg_enable on the DPI interface after the setting of the 'EN' signal in MIPI_PORT_CTRL register by s/w

MIPI_EOT_DISABLE_REGISTER

MIPI_EOT_DISABLE_REGISTER

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B05Ch-6B05Fh
Name:	MIPIA_EOT_DISABLE_REGISTER
ShortName:	MIPIA_EOT_DISABLE_REGISTER
Power:	PG1
Reset:	soft
Address:	6B85Ch-6B85Fh
Name:	MIPIC_EOT_DISABLE_REGISTER
ShortName:	MIPIC_EOT_DISABLE_REGISTER
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:10	**RESERVED** Format: MBZ
	9	**DEFEATURE_DPI_FIFO_CTR** Access: R/W Set by the processor to enable or disable the belowfeatures. 0 – Disable – Feature Disabled 1 – Enable – The "mipi_dpf_vblank_start" signal is asserted only when the complete frame is transferred in the DPHY line and also the DPI FIFO is flushed out at the end of each frame.
	8	**DPHY_DEFEATURE_EN** Access: R/W Set by the processor to enable or disable DPHY RTL fix for misaligned data lanes. 0 – Disable – disables the DPHY fix. 1 – Enable – enables the DPHY fix.
	7	**LP_RX_TIMEOUT_ERROR_RECOVERY_DISABLE**

MIPI_EOT_DISABLE_REGISTER

Access:	R/W

Set by the processor to enable or disable the LP_Rx_timeout error recovery if the processor clears LP_Rx_timeout error interrupt.

Value	Name	Description
0	Enable	LP_Rx_timeout error recovery action will be taken by the DSI Tx controller if the processor clears the LP_Rx_timeout error interrupt.
1	Disable	If the processor clears the LP_Rx_timeout error interrupt, LP_Rx_timeout error recovery action will not happen in DSI Tx contorller. LP Rx timeout error interrupt will act as an informative interrupt

6 **HS_TX_TIMEOUT_ERROR_RECOVERY_DISABLE**

Access:	R/W

Set by the processor to enable or disable the HS_Tx_timeout error recovery if the processor clears HS_Tx_timeout interrupt.

Value	Name	Description
0	Enable	HS_Tx_timeout error recovery action will be taken by the DSI Tx controller if the processor clears the HS_Tx_timeout error interrupt.
1	Disable	If the processor clears the HS_Tx_timeout error interrupt, HS_Tx_timeout error recovery action will not happen in DSI Tx contorller. HS Tx timeout error interrupt will act as an informative interrupt

5 **LOW_CONTENTION_RECOVERY_DISABLE**

Access:	R/W

Set by the processor to enable or disable the contention recovery procedure if the processor clears Low contention interrupt.

Value	Name	Description
0	Enable	Contention recovery will happen if the processor clears Low contention interrupt.
1	Disable	If the processor clears the low contention interrupt, contention recovery procedure will not be initiated by the DSI Tx contorller. Low contention interrupt will act as an informative interrupt

4 **HIGH_CONTENTION_RECOVERY_DISABLE**

Access:	R/W

Set by the processor to enable or disable the contention recovery procedure if the processor clears High contention interrupt.

Value	Name	Description
0	Enable	Contention recovery will happen if the processor clears High contention interrupt.
1	Disable	If the processor clears the high contention interrupt, contention recovery procedure will not be initiated by the DSI Tx contorller. Ignore the High Contention Interrupt in MIPI_INTR_STAT_REG

MIPI_EOT_DISABLE_REGISTER

3 TXDSI_TYPE_NOT_RECOGNISED_ERROR_RECOVERY_DISABLE

Access:	R/W

Set by the processor to enable or disable the error recovery action to be taken by the DSI Tx controller if TxDSI data type not recognised error interrupt is cleared by the processor.

Value	Name	Description
0	Enable	Error recovery action will be taken if TxDSI data type not recognised error interrupt is cleared by the processor.
1	Disable	If TxDSI data type not recognised error interrupt is cleared by the processor, error recovery action will not be taken by the DSI TX controller. Tx DSI data type not recognized error interrupt will act as an informative interrupt

2 TXECC_MULTIBIT_ERR_RECOVERY_DISABLE

Access:	R/W

Set by the processor to enable or disable the error recovery action to be taken by the DSI Tx controller if Tx ECC multibit error interrupt is cleared by the processor.

Value	Name	Description
0	Enable	Error recovery action will be taken if Tx ECC multibit error interrupt is cleared by the processor.
1	Disable	If Tx ECC multibit error interrupt is cleared by the processor, error recovery action will not be taken by the DSI TX controller. Tx multibit error interrupt will act as an informative interrupt

1 CLOCKSTOP

Access:	R/W

Set by the processor to enable or disable clock stopping feature during BLLP timing in a DPI transfer in dual channel mode or during DPI only mode and also when there is no traffic in the DBI interface in DBI only enabled mode. By default this register value is 0.

Value	Name	Description
0	Disable	clock stopping disabled
1	Enable	clock stopping enabled

0 EOT_DIS

Access:	R/W

Set by the processor to enable or disable EOT short packet transmission. By default this register value is 0. For backward comapatibility of earlier DSI systems, EOT short packet transmission can be disabled.

Value	Name	Description
0	Enable	EOT short packet transmission enabled
1	Disable	EOT short packet transmission disabled

MIPI_GEN_FIFO_STAT_REGISTER

MIPI_GEN_FIFO_STAT_REGISTER

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x1E060606
Access:	RO
Size (in bits):	32
Address:	6B074h-6B077h
Name:	MIPIA_GEN_FIFO_STAT_REGISTER
ShortName:	MIPIA_GEN_FIFO_STAT_REGISTER
Power:	PG1
Reset:	soft
Address:	6B874h-6B877h
Name:	MIPIC_GEN_FIFO_STAT_REGISTER
ShortName:	MIPIC_GEN_FIFO_STAT_REGISTER
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:29	**RESERVED** Format: MBZ
	28	**DPI_FIFO_EMPTY** Access: RO 0 Disable 1 Enable **[Default]**
	27	**DBI_FIFO_EMPTY** Access: RO 0 Disable 1 Enable **[Default]**
	26	**LP_CTRL_FIFO_EMPTY** Access: RO

MIPI_GEN_FIFO_STAT_REGISTER

		Value / **Name** 0 — Disable 1 — Enable **[Default]**
	25	**LP_CTRL_FIFO_HALF_EMPTY** Access: RO **Value** / **Name** 0 — Disable 1 — Enable **[Default]**
	24	**LP_CTRL_FIFO_FULL** Access: RO **Value** / **Name** 0 — Disable **[Default]** 1 — Enable
	23:19	**RESERVED_1** Format: MBZ
	18	**HS_CTRL_FIFO_EMPTY** Access: RO **Value** / **Name** 0 — Disable 1 — Enable **[Default]**
	17	**HS_CTRL_FIFO_HALF_EMPTY** Access: RO **Value** / **Name** 0 — Disable 1 — Enable **[Default]**
	16	**HS_CTRL_FIFO_FULL** Access: RO **Value** / **Name** 0 — Disable **[Default]** 1 — Enable
	15:11	**RESERVED_2**

MIPI_GEN_FIFO_STAT_REGISTER

		Format: MBZ
	10	**LP_DATA_FIFO_EMPTY** Access: RO **Value** / **Name** 0 – Disable 1 – Enable **[Default]**
	9	**LP_DATA_FIFO_HALF_EMPTY** Access: RO **Value** / **Name** 0 – Disable 1 – Enable **[Default]**
	8	**LP_DATA_FIFO_FULL** Access: RO **Value** / **Name** 0 – Disable **[Default]** 1 – Enable
	7:3	**RESERVED_3** Format: MBZ
	2	**HS_DATA_FIFO_EMPTY** Access: RO **Value** / **Name** 0 – Disable 1 – Enable **[Default]**
	1	**HS_DATA_FIFO_HALF_EMPTY** Access: RO **Value** / **Name** 0 – Disable 1 – Enable **[Default]**
	0	**HS_DATA_FIFO_FULL** Access: RO **Value** / **Name**

MIPI_GEN_FIFO_STAT_REGISTER			
		0	Disable **[Default]**
		1	Enable

MIPI_HIGH_LOW_SWITCH_COUNT

MIPI_HIGH_LOW_SWITCH_COUNT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B044h-6B047h
Name:	MIPIA_HIGH_LOW_SWITCH_COUNT
ShortName:	MIPIA_HIGH_LOW_SWITCH_COUNT
Power:	PG1
Reset:	soft
Address:	6B844h-6B847h
Name:	MIPIC_HIGH_LOW_SWITCH_COUNT
ShortName:	MIPIC_HIGH_LOW_SWITCH_COUNT
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:16	**RESERVED** Format: MBZ
	15:0	**HIGH_SPEED_TO_LOW_POWER_OR_LOW_POWER_TO_HIGH_SPEED_SWITCH_COUNT** Access: R/W High speed to low power or Low power to high speed switching time in terms of txbyteclkhs

MIPI_HORIZ_ACTIVE_AREA_COUNT

MIPI_HORIZ_ACTIVE_AREA_COUNT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B034h-6B037h
Name:	MIPIA_HORIZ_ACTIVE_AREA_COUNT
ShortName:	MIPIA_HORIZ_ACTIVE_AREA_COUNT
Power:	PG1
Reset:	soft
Address:	6B834h-6B837h
Name:	MIPIC_HORIZ_ACTIVE_AREA_COUNT
ShortName:	MIPIC_HORIZ_ACTIVE_AREA_COUNT
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:16	**RESERVED** Format: MBZ
	15:0	**HORIZONTAL_ACTIVE_AREA_COUNT** Access: R/W Shows the horizontal active area value in terms of txbyteclkhs

MIPI_HORIZ_BACK_PORCH_COUNT

MIPI_HORIZ_BACK_PORCH_COUNT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B02Ch-6B02Fh
Name:	MIPIA_HORIZ_BACK_PORCH_COUNT
ShortName:	MIPIA_HORIZ_BACK_PORCH_COUNT
Power:	PG1
Reset:	soft
Address:	6B82Ch-6B82Fh
Name:	MIPIC_HORIZ_BACK_PORCH_COUNT
ShortName:	MIPIC_HORIZ_BACK_PORCH_COUNT
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:16	**RESERVED** Format: MBZ
	15:0	**HORIZONTAL_BACK_PORCH_COUNT** Access: R/W Shows the horizontal back porch value in terms of txbyteclkhs

MIPI_HORIZ_FRONT_PORCH_COUNT

MIPI_HORIZ_FRONT_PORCH_COUNT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B030h-6B033h
Name:	MIPIA_HORIZ_FRONT_PORCH_COUNT
ShortName:	MIPIA_HORIZ_FRONT_PORCH_COUNT
Power:	PG1
Reset:	soft
Address:	6B830h-6B833h
Name:	MIPIC_HORIZ_FRONT_PORCH_COUNT
ShortName:	MIPIC_HORIZ_FRONT_PORCH_COUNT
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:16	**RESERVED** Format: MBZ
	15:0	**HORIZONTAL_FRONT_PORCH_COUNT** Access: R/W Shows the horizontal front porch value in terms of txbyteclkhs

MIPI_HORIZ_SYNC_PADDING_COUNT

MIPI_HORIZ_SYNC_PADDING_COUNT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B028h-6B02Bh
Name:	MIPIA_HORIZ_SYNC_PADDING_COUNT
ShortName:	MIPIA_HORIZ_SYNC_PADDING_COUNT
Power:	PG1
Reset:	soft
Address:	6B828h-6B82Bh
Name:	MIPIC_HORIZ_SYNC_PADDING_COUNT
ShortName:	MIPIC_HORIZ_SYNC_PADDING_COUNT
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:16	**RESERVED** Format: MBZ
	15:0	**HORIZONTAL_SYNC_PADDING_COUNT** Access: R/W Shows the horizontal sync padding value in terms of txbyteclkhs

MIPI_HS_GEN_CTRL_REGISTER

MIPI_HS_GEN_CTRL_REGISTER

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B070h-6B073h
Name:	MIPIA_HS_GEN_CTRL_REGISTER
ShortName:	MIPIA_HS_GEN_CTRL_REGISTER
Power:	PG1
Reset:	soft
Address:	6B870h-6B873h
Name:	MIPIC_HS_GEN_CTRL_REGISTER
ShortName:	MIPIC_HS_GEN_CTRL_REGISTER
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:24	**RESERVED** Format: MBZ
	23:8	**WORD_COUNT** Access: WO Specifies the word count for generic long packet Specifies the accompanied parameters for generic short packets.Note: Invalid parameters must be set to 00h
	7:6	**VIRTUAL_CHANNEL** Access: WO Used to specify the virtual channel for which the generic data transmission is intended
	5:0	**DATA_TYPE** Access: WO Used to specify the generic data types Value: 03h — Name: Generic short write no parameters Value: 13h — Name: Generic short write 1 parameter

MIPI_HS_GEN_CTRL_REGISTER			
		23h	Generic short write 2 parameters
		04h	Generic read no parameters
		14h	Generic read 1 parameter
		24h	Generic read 2 parameter
		29h	Generic long write
		05h	Manufacturer DCS short write no parameter
		15h	Manufacturer DCS short write 1 parameter
		06h	Manufacturer DCS read no parameter
		39h	Manufacturer DCS long write
		07h	Compression mode data type write , short write, 2 parameters
		0Ah	PPS long write

MIPI_HS_GEN_DATA_REGISTER

MIPI_HS_GEN_DATA_REGISTER	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B068h-6B06Bh
Name:	MIPIA_HS_GEN_DATA_REGISTER
ShortName:	MIPIA_HS_GEN_DATA_REGISTER
Power:	PG1
Reset:	soft
Address:	6B868h-6B86Bh
Name:	MIPIC_HS_GEN_DATA_REGISTER
ShortName:	MIPIC_HS_GEN_DATA_REGISTER
Power:	PG1
Reset:	soft

This register supports single byte, word, and Dword writes. It does not support 3 byte writes.

DWord	Bit	Description
0	31:0	**HS_GEN_DATA** Access: R/W Data port register used for generic data transfers in high speed mode

MIPI_HS_LS_DBI_ENABLE_REG

MIPI_HS_LS_DBI_ENABLE_REG

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32

Address:	6B078h-6B07Bh
Name:	MIPIA_HS_LS_DBI_ENABLE_REG
ShortName:	MIPIA_HS_LS_DBI_ENABLE_REG
Power:	PG1
Reset:	soft

Address:	6B878h-6B87Bh
Name:	MIPIC_HS_LS_DBI_ENABLE_REG
ShortName:	MIPIC_HS_LS_DBI_ENABLE_REG
Power:	PG1
Reset:	soft

Note : dbi_hs_lp_switch_reg has to be written only if DBI FIFO is empty

DWord	Bit	Description
0	31:1	**RESERVED** Format: MBZ
	0	**DBI_HS_LS_SWITCH_RE** Access: R/W

Value	Name	Description
1	enable	DBI packets have to be transmitted in Low power mode
0	disable	DBI packets have to be transmitted in High speed mode

MIPI_HS_READ_TRANSFER_COUNT

MIPI_HS_READ_TRANSFER_COUNT

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	6B07Ch-6B07Fh
Name:	MIPIA_HS_READ_TRANSFER_COUNT
ShortName:	MIPIA_HS_READ_TRANSFER_COUNT
Power:	PG1
Reset:	soft
Address:	6B87Ch-6B87Fh
Name:	MIPIC_HS_READ_TRANSFER_COUNT
ShortName:	MIPIC_HS_READ_TRANSFER_COUNT
Power:	PG1
Reset:	soft

Programming Notes

AHB should program this register before start the high speed DCS/MCS/Generic read transfer.

DWord	Bit	Description
0	31:17	**Spare 31 to 17** Access: R/W Reserved R/W for future use.
	16	**HS Read Defeature En** Access: R/W This field controls whether the HS read allow checking is enabled. 0 – Disable: Disable the new HS read allow checking so the DSI Tx allows the HS read transfer based on the internally calculated value. 1 – Enable: Enable the new HS read allow checking so the DSI Tx allows the HS read transfer based on the programmed HS read count value.
	15:0	**HS Read Count** Access: R/W This field gives the HS read transfer time in terms of txbyteclkhs clock. It is a time in-between the read command is transferred on the DSI PPI to stop state detection on the DSI Tx after the second BTA.

MIPI_HS_TX_TIMEOUT_REG

MIPI_HS_TX_TIMEOUT_REG	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B010h-6B013h
Name:	MIPIA_HS_TX_TIMEOUT_REG
ShortName:	MIPIA_HS_TX_TIMEOUT_REG
Power:	PG1
Reset:	soft
Address:	6B810h-6B813h
Name:	MIPIC_HS_TX_TIMEOUT_REG
ShortName:	MIPIC_HS_TX_TIMEOUT_REG
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:24	**RESERVED** Format: MBZ
	23:0	**HIGH_SPEED_TX_TIMEOUT_COUNTER** Access: R/W The maximum duration allowed for the DSI host to remain in high speed mode for a transmission. If the counter expires, HS mode is terminated with EOT and the lanes enter stop state

MIPI_INIT_COUNT_REGISTER

MIPI_INIT_COUNT_REGISTER	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B050h-6B053h
Name:	MIPIA_INIT_COUNT_REGISTER
ShortName:	MIPIA_INIT_COUNT_REGISTER
Power:	PG1
Reset:	soft
Address:	6B850h-6B853h
Name:	MIPIC_INIT_COUNT_REGISTER
ShortName:	MIPIC_INIT_COUNT_REGISTER
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:16	**RESERVED** Format: MBZ
	15:0	**MASTER_INIT_TIMER** Access: R/W Counter value in terms of low power clock to initialise the DSI Host IP [TINT] that drives a stop state on the mipi's D-PHY bus

MIPI_INTR_EN_REG_1

MIPI_INTR_EN_REG_1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B094h-6B097h
Name:	MIPIA_INTR_EN_REG_1
ShortName:	MIPIA_INTR_EN_REG_1
Power:	PG1
Reset:	soft
Address:	6B894h-6B897h
Name:	MIPIC_INTR_EN_REG_1
ShortName:	MIPIC_INTR_EN_REG_1
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:2	**RESERVED** Format: MBZ
	1	**DPI Line Timeout** Access: R/W Set to enable the interrupt for DPI line timeout.
	0	**MIPI_ENABLE_RX_CONNECTION_DETECTED** Access: R/W Set to enable the interrupt for contention detected error in the acknowledgement packet reports

MIPI_INTR_EN_REG

MIPI_INTR_EN_REG	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B008h-6B00Bh
Name:	MIPIA_INTR_EN_REG
ShortName:	MIPIA_INTR_EN_REG
Power:	PG1
Reset:	soft
Address:	6B808h-6B80Bh
Name:	MIPIC_INTR_EN_REG
ShortName:	MIPIC_INTR_EN_REG
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31	**TEARING_EFFECT** Access: R/W Set to enable the tearing effect interrupt
	30	**SPL_PKT_SENT_INTERRUPT** Access: R/W Set to enable the confirmation of transmission of the DPI event specific commands set in the dpi control and dpi data register
	29	**GEN_READ_DATA_AVAIL** Access: R/W Set to enable Generic Read available interrupt
	28	**LP_GENERIC_WR_FIFO_FULL** Access: R/W Set to enable the LP generic write fifo full interrupt
	27	**HS_GENERIC_WR_FIFO_FULL**

MIPI_INTR_EN_REG

		Access: R/W Set to enable the HS generic write fifo full interrupt
	26	**RX_PROT_VIOLATION** Access: R/W Set to enable protocol violation error
	25	**RX_INVALID_TX_LENGTH** Access: R/W Set to enable invalid transmission length error
	24	**ACK_WITH_NO_ERROR** Access: R/W Set to enable acknowledge trigger message reception with out any error
	23	**TURN_AROUND_ACK_TIMEOUT** Access: R/W Set to enable turn around acknowledgement sequence timeout
	22	**LP_RX_TIMEOUT** Access: R/W Set to enable low power reception count timeouts
	21	**HS_TX_TIMEOUT** Access: R/W Set to enable a high speed transmission timeout
	20	**DPI_FIFO_UNDERRUN** Access: R/W Set to enable if there is no data in the dpi fifo to make a in time delivery of the pixel data to the DSI receiver
	19	**LOW_CONTENTION** Access: R/W Set to enable a LP low fault interrupt
	18	**HIGH_CONTENTION** Access: R/W Set to enable a LP high fault interrupt

MIPI_INTR_EN_REG

	17	**TXDSI_VC_ID_INVALID** Access: R/W Set to enable the interrupt if the received packets virtual channel ID is invalid
	16	**TXDSI_DATA_TYPE_NOT_RECOGNISED** Access: R/W Set to enable the interrupt if the received packets data type is not recognised
	15	**TXCHECKSUM_ERROR** Access: R/W Set to enable the interrupt if the computed CRC differs from the received CRC value for the received packets
	14	**TXECC_MULTIBIT_ERROR** Access: R/W Set to enable the interrupt if there is no ECC correction for the packet or there are more than 2 bit errors in the packet received by Arasan DSI host
	13	**TXECC_SINGLE_BIT_ERROR** Access: R/W Set to enable the interrupt if ECC syndrome was computed and is corrected for one bit error during the reception of packets by the Arasan DSIhost
	12	**TXFALSE_CONTROL_ERROR** Access: R/W Set to enable the interrupt for the control error.,observed on the lanes by the Arasan_DSI_host
	11	**RXDSI_VC_ID_INVALID** Access: R/W Set to enable the interrupt for invalid virtual channel ID in the acknowledgment packet reports
	10	**RXDSI_DATA_TYPE_NOT_RECOGNISED** Access: R/W Set to enable the interrupt for the un recognised data type in the acknowledgment packet reports
	9	**RXCHECKSUM_ERROR** Access: R/W Set to enable the interrupt for the computed CRC differs from the received CRC value in the acknowledgment packet reports

MIPI_INTR_EN_REG

	8	**RXECC_MULTIBIT_ERROR** Access: R/W Set to enable the interrupt for no ECC correction for the packet or there are more than 2 bit errors reported in the acknowledgment packet
	7	**RXECC_SINGLE_BIT_ERROR** Access: R/W Set to enable the interrupt for ECC syndrome computation and one bit error correction for the acknowledgment packet
	6	**RXFALSE_CONTROL_ERROR** Access: R/W Set to enable the interrupt for control error in the acknowledgment packet reports
	5	**RXHS_RECEIVE_TIMEOUT_ERROR** Access: R/W Set to enable the interrupt for the high speed receive timeout Error in the acknowledgment packet reports
	4	**RX_LP_TX_SYNC_ERROR** Access: R/W Set to enable the interrupt for Low power transmission sync error in the acknowledgment packet reports
	3	**RXESCAPE_MODE_ENTRY_ERROR** Access: R/W Set to enable the interrupt for Escape Mode Entry command error in the acknowledgment packet reports
	2	**RXEOTSYNC_ERROR** Access: R/W Set to enable the interrupt for End of transmission synchronisation Error in the acknowledgement packet reports
	1	**RXSOTSYNC_ERROR** Access: R/W Set to enable the interrupt for start of transmission synchronisation error in the acknowledgement packet reports

MIPI_INTR_EN_REG		
	0	**RXSOT_ERROR** Access: R/W Set to enable the interrupt for start of transmission error in the acknowledgment packet reports

MIPI_INTR_STAT_REG_1

MIPI_INTR_STAT_REG_1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/WC
Size (in bits):	32
Address:	6B090h-6B093h
Name:	MIPIA_INTR_STAT_REG_1
ShortName:	MIPIA_INTR_STAT_REG_1
Power:	PG1
Reset:	soft
Address:	6B890h-6B893h
Name:	MIPIC_INTR_STAT_REG_1
ShortName:	MIPIC_INTR_STAT_REG_1
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:2	**RESERVED** Format: MBZ
	1	**DPI Line Timeout** Access: R/WC Set to 1'b1 by hardware when there is a DPI Line Timeout.
	0	**MIPI_RX_CONNECTION_DETECTED** Access: R/WC Set to 1'b1 by hardware if the contention detected in the display device and is reported in the Acknowledge packet by the display device.

MIPI_INTR_STAT_REG

MIPI_INTR_STAT_REG	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/WC
Size (in bits):	32
Address:	6B004h-6B007h
Name:	MIPIA_INTR_STAT_REG
ShortName:	MIPIA_INTR_STAT_REG
Power:	PG1
Reset:	soft
Address:	6B804h-6B807h
Name:	MIPIC_INTR_STAT_REG
ShortName:	MIPIC_INTR_STAT_REG
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31	**TEARING_EFFECT** Access: R/WC Set to indicate that tearing effect trigger message is received
	30	**SPL_PKT_SENT_INTERRUPT** Access: R/WC Set to confirm the transmission of the DPI event specific commands set in the dpi control and dpi data register
	29	**GEN_READ_DATA_AVAIL** Access: R/WC Set to indicate that the requested data for a Generic Read request is available in the buffer i.e., generic read response data is available in the read FIFO
	28	**LP_GENERIC_WR_FIFO_FULL** Access: R/WC Set to indicate that the LP generic write fifo is full

MIPI_INTR_STAT_REG

	27	**HS_GENERIC_WR_FIFO_FULL** Access: R/WC Set to indicate that the HS generic write fifo is full
	26	**RX_PROT_VIOLATION** Access: R/WC Set if DSI protocol violation error is reported in the acknowledge packet by the display device
	25	**RX_INVALID_TX_LENGTH** Access: R/WC Set if invalid transmission length error is reported in the acknowledge packet by the display device
	24	**ACK_WITH_NO_ERROR** Access: R/WC Set if acknowledge trigger message is received with out any error
	23	**TURN_AROUND_ACK_TIMEOUT** Access: R/WC Set if a turn around acknowledgement sequence is not received from the display device
	22	**LP_RX_TIMEOUT** Access: R/WC Set if a low power reception count expires this interrupt is generated
	21	**HS_TX_TIMEOUT** Access: R/WC Set if a high speed transmission prevails for more than the expected count value this interrupt is raised
	20	**DPI_FIFO_UNDERRUN** Access: R/WC Set to '1' if there is no data in the dpi fifo to make a in time delivery of the pixel data to the DSI receiver
	19	**LOW_CONTENTION** Access: R/WC Set to '1' if a LP low fault is registered by at the D-PHY contention detector

MIPI_INTR_STAT_REG

	18	**HIGH_CONTENTION** Access: R/WC Set to '1' if a LP high fault is registered by at the D-PHY contention detector
	17	**TXDSI_VC_ID_INVALID** Access: R/WC Set to '1' if the received virtual channel ID is invalid
	16	**TXDSI_DATA_TYPE_NOT_RECOGNISED** Access: R/WC Set to '1' if the received data type is not recognised
	15	**TXCHECKSUM_ERROR** Access: R/WC Set to '1' if the computed checksum differs from the received checksum value during the reception of packets by Arasan_DSI host.
	14	**TXECC_MULTIBIT_ERROR** Access: R/WC Set to '1' if there is no ECC correction for the packet or there are more than 2 bit errors in the packet received by Arasan_DSI_host
	13	**TXECC_SINGLE_BIT_ERROR** Access: R/WC Set to '1' if ECC syndrome was computed and is corrected for one bit error during the reception of packets by the Arasan_DSI_host
	12	**TXFALSE_CONTROL_ERROR** Access: R/WC Set to '1' if a control error is observed on the lanes by the Arasan_DSI_host
	11	**RXDSI_VC_ID_INVALID** Access: R/WC Set to '1' if the virtual channel ID is invalid by the display device is reported in the Acknowledge packet by the display device
	10	**RXDSI_DATA_TYPE_NOT_RECOGNISED** Access: R/WC Set to '1' if the data type is not recognised by the display device is reported in the Acknowledge packet by the display device

MIPI_INTR_STAT_REG

	9	**RXCHECKSUM_ERROR** Access: R/WC Set to '1' if the computed CRC differs from the received CRC value and is reported in the Acknowledge packet by the display device
	8	**RXECC_MULTIBIT_ERROR** Access: R/WC Set to '1' if there is no ECC correction for the packet or there are more than 2 bit errors in the packet is reported in the Acknowledge packet by the display device
	7	**RXECC_SINGLE_BIT_ERROR** Access: R/WC Set to '1' if ECC syndrome was computed and corrected for one bit error is reported in the Acknowledge packet by the display device
	6	**RXFALSE_CONTROL_ERROR** Access: R/WC Set to '1' if a control error is reported in the Acknowledge packet by the display device
	5	**RXHS_RECEIVE_TIMEOUT_ERROR** Access: R/WC Set to '1' if the high speed receive timer value expires and data transfer lasts on the data lane is reported in the Acknowledge packet by the display device
	4	**RX_LP_TX_SYNC_ERROR** Access: R/WC Set to '1' if Low power transmission sync error occurs in the display device and is reported in the Acknowledge packet by the display device
	3	**RXESCAPE_MODE_ENTRY_ERROR** Access: R/WC Set to '1' if Escape Mode Entry command is not understandable by the display device and is reported in the Acknowledge packet by the display device
	2	**RXEOTSYNCERROR** Access: R/WC Set to '1' if an end of transmission synchronisation error is reported in the Acknowledge packet by the display device

MIPI_INTR_STAT_REG		
	1	**RXSOTSYNCERROR** Access: R/WC Set to '1' if a start of transmission synchronisation error is reported in the Acknowledge packet by the display device
	0	**RXSOTERROR** Access: R/WC Set to '1' if a start of transmission error is reported in the Acknowledge packet by the display device

MIPI_LP_BYTECLK_REGISTER

MIPI_LP_BYTECLK_REGISTER	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B060h-6B063h
Name:	MIPIA_LP_BYTECLK_REGISTER
ShortName:	MIPIA_LP_BYTECLK_REGISTER
Power:	PG1
Reset:	soft
Address:	6B860h-6B863h
Name:	MIPIC_LP_BYTECLK_REGISTER
ShortName:	MIPIC_LP_BYTECLK_REGISTER
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:16	**RESERVED** Format: MBZ
	15:0	**LP_BYTECLK** Access: R/W Low power clock equivalence in terms of byte clock. The value programmed in this register is equal to the number of byte clocks occupied in one low power clock. This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc)

MIPI_LP_GEN_CTRL_REGISTER

MIPI_LP_GEN_CTRL_REGISTER

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B06Ch-6B06Fh
Name:	MIPIA_LP_GEN_CTRL_REGISTER
ShortName:	MIPIA_LP_GEN_CTRL_REGISTER
Power:	PG1
Reset:	soft
Address:	6B86Ch-6B86Fh
Name:	MIPIC_LP_GEN_CTRL_REGISTER
ShortName:	MIPIC_LP_GEN_CTRL_REGISTER
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:24	**RESERVED** Format: MBZ
	23:8	**WORD_COUNT** Access: WO Specifies the word count for generic long packet Specifies the accompanied parameters for generic short packets.Note: Invalid parameters must be set to 00h
	7:6	**VIRTUAL_CHANNEL** Access: WO Used to specify the virtual channel for which the generic data transmission is intended
	5:0	**DATA_TYPE** Access: WO Used to specify the generic data types Value / Name: 03h — Generic short write no parameters 13h — Generic short write 1 parameter

MIPI_LP_GEN_CTRL_REGISTER			
		23h	Generic short write 2 parameters
		04h	Generic read no parameters
		14h	Generic read 1 parameter
		24h	Generic read 2 parameter
		29h	Generic long write
		05h	Manufacturer DCS short write no parameter
		15h	Manufacturer DCS short write 1 parameter
		06h	Manufacturer DCS read no parameter
		39h	Manufacturer DCS long write
		07h	Compression mode data type write , short write, 2 parameters
		0Ah	PPS long write

MIPI_LP_GEN_DATA_REGISTER

MIPI_LP_GEN_DATA_REGISTER	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B064h-6B067h
Name:	MIPIA_LP_GEN_DATA_REGISTER
ShortName:	MIPIA_LP_GEN_DATA_REGISTER
Power:	PG1
Reset:	soft
Address:	6B864h-6B867h
Name:	MIPIC_LP_GEN_DATA_REGISTER
ShortName:	MIPIC_LP_GEN_DATA_REGISTER
Power:	PG1
Reset:	soft

This register supports single byte, word, and Dword writes. It does not support 3 byte writes.

DWord	Bit	Description
0	31:0	**LP_GEN_DATA** Access: R/W Data port register used for generic data transfers in low power mode

MIPI_LP_RX_TIMEOUT_REG

MIPI_LP_RX_TIMEOUT_REG	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B014h-6B017h
Name:	MIPIA_LP_RX_TIMEOUT_REG
ShortName:	MIPIA_LP_RX_TIMEOUT_REG
Power:	PG1
Reset:	soft
Address:	6B814h-6B817h
Name:	MIPIC_LP_RX_TIMEOUT_REG
ShortName:	MIPIC_LP_RX_TIMEOUT_REG
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:24	**RESERVED** Format: MBZ
	23:0	**LOW_POWER_RECEPTION_TIMEOUT_COUNTER** Access: R/W Timeout value to be checked for received short packets. If the timer expires the DSI Host enters stop state

MIPI_MAX_RETURN_PKT_SIZE_REGISTER

MIPI_MAX_RETURN_PKT_SIZE_REGISTER	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B054h-6B057h
Name:	MIPIA_MAX_RETURN_PKT_SIZE_REGISTER
ShortName:	MIPIA_MAX_RETURN_PKT_SIZE_REGISTER
Power:	PG1
Reset:	soft
Address:	6B854h-6B857h
Name:	MIPIC_MAX_RETURN_PKT_SIZE_REGISTER
ShortName:	MIPIC_MAX_RETURN_PKT_SIZE_REGISTER
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:10	**RESERVED** Format: MBZ
	9:0	**MAX_RETURN_PKT_SIZE** Access: R/W Set the count value in bytes to collect the return data packet for reverse direction data flow in data lane0 in response to a DBI read operation

MIPI_PORT_CTRL

MIPI_PORT_CTRL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x2010A060
Access:	R/W
Size (in bits):	32
Address:	6B0C0h-6B0C3h
Name:	MIPIA_PORT_CTRL
ShortName:	MIPIA_PORT_CTRL
Power:	PG1
Reset:	soft
Address:	6B8C0h-6B8C3h
Name:	MIPIC_PORT_CTRL
ShortName:	MIPIC_PORT_CTRL
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31	**EN** Access: R/W When this bit is disabled the MIPI DPI (video mode) is inactive and in it's low power state. When it is enabled it starts to generate timing for this MIPI port. Value / Name / Description: 0 / Disable / The port is disabled and all MIPI DPI interface are disable (timing generator is off) 1 / Enable / The port is enabled **Programming Notes** For MIPI dual-link in DPI mode, the port enable bits in both MIPI A control register and MIPI C control register shall be enabled.
	30:27	**ADJDLY_HSTX** Default Value: 0100b Access: R/W These four bits act as an encoded count of the number of buffer delays to insert on the ckdsi2x clock going to the six flops that are storing the HS TX data and clock signals. Default is 4 which is the equivalent of 1 buffer delay.

MIPI_PORT_CTRL

	25:24	**RESERVED** Format: MBZ
	23	**SELFLOPPED_HSTX** Access: R/W This bit muxes between the flopped (new) and unflopped (original) versions of the TX HS clock and data. **Value** / **Name** / **Description** 0 / Disable / Pass through original unflopped version 1 / Enable / Pass through the new flopped version of these signals
	22	**RESERVED** Format: MBZ
	21:18	**FLISDSI_ADJDLY_HSTX_MIPIA** Default Value: 0100b Access: R/W These bits act as an encoded count of the number of buffer delays to insert on the ckdsi2x clock going to the six flops that are storing the HS TX data and clock signals. Default is 4 which is the equivalent of 1 buffer delay.
	17	**AFE_LATCHOUT** Access: RO This bit reflects the value of the output latch of CLK A lane in DSI AFE b. The software driver can read this bit to see if the hold value (LP11 or LP00) to initialize from a sleep state (s0i1 or S0i3) correctly **Value** / **Name** / **Description** 1 / LP11 / Current value of output latch is 1 (D-PHY is in LP11 state) 0 / LP00 / Current value of output latch is 0 (D-PHY is in LP00 state)
	16	**LPOUTPUT_HOLD** Access: R/W **Value** / **Name** / **Description** 0 / Disable / Disable transparent latch inside DSI AFE. Output are driven by latch value. 1 / Enable / Enable transparent latch inside DSI AFE so data are driven by DSI DPHY
	15	**FLISDSI_ADJDLY_HSTX_MIPIC_HIGH_ORDER** Default Value: 1 Access: R/W The fourth bit of four bits act as an encoded count of the number of buffer delays to insert on the ckdsi2x clock going to the six flops that are storing the HS TX data and clock signals. Default is 1 which is the equivalent of 1 buffer delay.

MIPI_PORT_CTRL

14:11 MIPI4DPHY_AdjDly_HSTX_MIPI_C

Default Value:	0100b
Access:	R/W

These four bits act as an encoded count of the number of buffer delays to insert on the ckdsi2x clock going to the six flops that are storing the HS TX data and clock signals. Default is 4 which is the equivalent of 1 buffer delay.

10:8 Spare 10 to 8

Access:	R/W

Reserved R/W for future use.

7:5 FLISDSI_AdjDly_HSTX_MIPI_C_LOWER_ORDER

Default Value:	011b
Access:	R/W

The lower 3-bit of four bits act as an encoded count of the number of buffer delays to insert on the ckdsi2x clock going to the six flops that are storing the HS TX data and clock signals. Default is 3 which is the equivalent of 1 buffer delay.

4 TE Counter Delay

Access:	R/W

When enabled, DSI controller will start processing the subsequent frame only after the TE Delay Counter specified by bits 15:0 of the MIPI_TE_CTR register expires.

Value	Name
0	Disable
1	Enable

3:2 EFFECT

Access:	R/W

Value	Name	Description
00b	No tearing effect required	Memory write start as soon as write data is available
01b	TE trigger by MIPI DPHY and DSI protocol	
10b	TE trigger by GPIO pin	
11b	Reserved	

1 Reserved

Format:	MBZ

MIPI_RD_DATA_RETURN

MIPI_RD_DATA_RETURN	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	6B118h-6B137h
Name:	MIPIA_RD_DATA_RETURN
ShortName:	MIPIA_RD_DATA_RETURN_*
Power:	PG1
Reset:	soft
Address:	6B918h-6B937h
Name:	MIPIC_RD_DATA_RETURN
ShortName:	MIPIC_RD_DATA_RETURN_*
Power:	PG1
Reset:	soft

There are multiple instances of this register format per MIPI port.

DWord	Bit	Description
0	31:0	**RD_DATA_RETURN_PANEL** Access: RO This is the configuration data returned from the panel

MIPI_RD_DATA_VALID

MIPI_RD_DATA_VALID	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B138h-6B13Bh
Name:	MIPIA_RD_DATA_VALID
ShortName:	MIPIA_RD_DATA_VALID
Power:	PG1
Reset:	soft
Address:	6B938h-6B93Bh
Name:	MIPIC_RD_DATA_VALID
ShortName:	MIPIC_RD_DATA_VALID
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:8	**RESERVED** Format: MBZ
	7:0	**READ_DATA_VALID** Access: R/WC Each bit corresponds to presence of valid data in the registers above. When data is returned from the panel, H/W will write into these registers in sequence, and set the corresponding valid bit. SW must write a 1b to clear this bit.

MIPI_STATUS

MIPI_STATUS

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B0C4h-6B0C7h
Name:	MIPIA_STATUS
ShortName:	MIPIA_STATUS
Power:	PG1
Reset:	soft
Address:	6B8C4h-6B8C7h
Name:	MIPIC_STATUS
ShortName:	MIPIC_STATUS
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31	**Sideband TE** Access: R/WC This is a status bit which is set when a TE indication is received on the TE pin. Clear this bit by writing a 1b to it. Value / Name / Description: 0b / No TE / No TE indication 1b / TE / TE indication received.
	30	**TE message in LP mode** Access: R/WC This is a status bit which is set when TE signaling in DSI mode is received in LP mode. Clear this bit by writing a 0b to it. Value / Name / Description: 0b / No TE / No TE indication 1b / TE / TE indication received.
	29	**MIPI idle** Access: R/WC This is a status bit which is set when MIPI_AUTO_PWG_ENABLE (MIPI_AUTOPWG[0])is set and the DSI controller is done sending the last frame in Command Mode. Clear this bit by writing a 1b to

MIPI_STATUS

		it. Value / Name / Description 0b / MIPI Not Idle / DSI controller is not idle 1b / MIPI Idle / DSI Controller is idle.
	28:0	**RESERVED** Format: MBZ

MIPI_STOP_STATE_STALL

MIPI_STOP_STATE_STALL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B08Ch-6B08Fh
Name:	MIPIA_STOP_STATE_STALL
ShortName:	MIPIA_STOP_STATE_STALL
Power:	PG1
Reset:	soft
Address:	6B88Ch-6B88Fh
Name:	MIPIC_STOP_STATE_STALL
ShortName:	MIPIC_STOP_STATE_STALL
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:8	**RESERVED** Format: MBZ
	7:0	**MIPI_STOP_STATE_STALL_COUNTER** Access: R/W

MIPI_TE_CTR

MIPI_TE_CTR

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B108h-6B10Bh
Name:	MIPIA_TE_CTR
ShortName:	MIPIA_TE_CTR
Power:	PG1
Reset:	soft
Address:	6B908h-6B90Bh
Name:	MIPIC_TE_CTR
ShortName:	MIPIC_TE_CTR
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:16	**RESERVED** Format: MBZ
	15:0	**TE Delay Counter** Default Value: 0 No Delay programmed Access: R/W This is the number of MIPI host clocks of delay from the TE trigger to when the DSI controller will start processing the subsequent frame. This counter is only valid if bit 4 of the MIPI_PORT_CTRL register is set.

MIPI_TRANS_HACTIVE

MIPI_TRANS_HACTIVE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B0F8h-6B0FBh
Name:	MIPIA_TRANS_HACTIVE
ShortName:	MIPIA_TRANS_HACTIVE
Power:	PG1
Reset:	soft
Address:	6B8F8h-6B8FBh
Name:	MIPIC_TRANS_HACTIVE
ShortName:	MIPIC_TRANS_HACTIVE
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:13	**RESERVED** Format: MBZ
	12:0	**Horizontal Active** Access: R/W This field specifies Horizontal Active Display size.

MIPI_TRANS_VACTIVE

MIPI_TRANS_VACTIVE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B0FCh-6B0FFh
Name:	MIPIA_TRANS_VACTIVE
ShortName:	MIPIA_TRANS_VACTIVE
Power:	PG1
Reset:	soft
Address:	6B8FCh-6B8FFh
Name:	MIPIC_TRANS_VACTIVE
ShortName:	MIPIC_TRANS_VACTIVE
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:13	**RESERVED** Format: MBZ
	12:0	**Vertical Active** Access: R/W This field specifies Vertical Active Display size.

MIPI_TRANS_VTOTAL

MIPI_TRANS_VTOTAL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B100h-6B103h
Name:	MIPIA_TRANS_VTOTAL
ShortName:	MIPIA_TRANS_VTOTAL
Power:	PG1
Reset:	soft
Address:	6B900h-6B903h
Name:	MIPIC_TRANS_VTOTAL
ShortName:	MIPIC_TRANS_VTOTAL
Power:	PG1
Reset:	soft

MIPI A Enable Delay Counter

DWord	Bit	Description
0	31:13	**RESERVED** Format: MBZ
	12:0	**Vertical Total** Access: R/W This field specifies Vertical Total size. This field is programmed to the number of lines desired minus one.

MIPI_TURN_AROUND_TIMEOUT_REG

MIPI_TURN_AROUND_TIMEOUT_REG	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B018h-6B01Bh
Name:	MIPIA_TURN_AROUND_TIMEOUT_REG
ShortName:	MIPIA_TURN_AROUND_TIMEOUT_REG
Power:	PG1
Reset:	soft
Address:	6B818h-6B81Bh
Name:	MIPIC_TURN_AROUND_TIMEOUT_REG
ShortName:	MIPIC_TURN_AROUND_TIMEOUT_REG
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:6	**RESERVED** Format: MBZ
	5:0	**TURN_AROUND_TIMEOUT_REGISTER** Access: R/W Timeout value to be checked after the DSI host makes a turn around in the direction of transfers. If the timer expires the DSI Host enters stop state

MIPI_VERT_BACK_PORCH_COUNT

MIPI_VERT_BACK_PORCH_COUNT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B03Ch-6B03Fh
Name:	MIPIA_VERT_BACK_PORCH_COUNT
ShortName:	MIPIA_VERT_BACK_PORCH_COUNT
Power:	PG1
Reset:	soft
Address:	6B83Ch-6B83Fh
Name:	MIPIC_VERT_BACK_PORCH_COUNT
ShortName:	MIPIC_VERT_BACK_PORCH_COUNT
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:16	**RESERVED** Format: MBZ
	15:0	**VERTICAL_BACK_PORCH_COUNT** Access: R/W Shows the vertical back porch value in terms of lines

MIPI_VERT_FRONT_PORCH_COUNT

MIPI_VERT_FRONT_PORCH_COUNT

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B040h-6B043h
Name:	MIPIA_VERT_FRONT_PORCH_COUNT
ShortName:	MIPIA_VERT_FRONT_PORCH_COUNT
Power:	PG1
Reset:	soft
Address:	6B840h-6B843h
Name:	MIPIC_VERT_FRONT_PORCH_COUNT
ShortName:	MIPIC_VERT_FRONT_PORCH_COUNT
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:16	**RESERVED** Format: MBZ
	15:0	**VERTICAL_FRONT_PORCH_COUNT** Access: R/W Shows the vertical front porch value in terms of lines

MIPI_VERT_SYNC_PADDING_COUNT

MIPI_VERT_SYNC_PADDING_COUNT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B038h-6B03Bh
Name:	MIPIA_VERT_SYNC_PADDING_COUNT
ShortName:	MIPIA_VERT_SYNC_PADDING_COUNT
Power:	PG1
Reset:	soft
Address:	6B838h-6B83Bh
Name:	MIPIC_VERT_SYNC_PADDING_COUNT
ShortName:	MIPIC_VERT_SYNC_PADDING_COUNT
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:16	**RESERVED** Format: MBZ
	15:0	**VERTICAL_SYNC_PADDING_COUNT** Access: R/W Shows the vertical sync padding value in terms of lines

MIPI_VIDEO_MODE_FORMAT_REGISTER

MIPI_VIDEO_MODE_FORMAT_REGISTER

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B058h-6B05Bh
Name:	MIPIA_VIDEO_MODE_FORMAT_REGISTER
ShortName:	MIPIA_VIDEO_MODE_FORMAT_REGISTER
Power:	PG1
Reset:	soft
Address:	6B858h-6B85Bh
Name:	MIPIC_VIDEO_MODE_FORMAT_REGISTER
ShortName:	MIPIC_VIDEO_MODE_FORMAT_REGISTER
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:6	**RESERVED** Format: MBZ
	5	**RESERVED** Format: MBZ
	4	**De_feature** Access: R/W Set by the processor to support random DPI display resolution. Value 0 / Name disabled / Description: Random DPI display resolution support disabled. Value 1 / Name enabled / Description: Random DPI display resolution support enabled.
	3	**Video_BTA_Disable** Access: R/W Set by the processor to inform the DSI controller to disable the BTA sent at the last blanking line of VFP. By default, this bit is set to '0'. Value 0 / Name enable / Description: BTA sending at the last blanking line of VFP is enabled. Value 1 / Name disable / Description: BTA sending at the last blanking line of VFP is disabled.

MIPI_VIDEO_MODE_FORMAT_REGISTER

2 IP_TG_CONFIG

Access:	R/W

Set by the processor to inform that the DSI controller should discontinue the DPI transfer after the last line of the VFP after ip_tg_enable deassertion. By default, this bit is set to 0.

Value	Name	Description
0	disable	After ip_tg_enable deassertion, DSI Tx controller stops the DPI transfer immediately after the current packet is transmitted.
1	enable	After ip_tg_enable deassertion, DSI Tx controller discontinues the DPI transfer after the last line of the VFP

1:0 VIDEO_MODE_FMT

Access:	R/W

Sets the Video mode format (packet sequence) to be supported in DSI. In Non Burst Mode, in addition to programming this register the horizontal active area count register value should also be programmed equal to RGB word count value In Burst Mode, in addition to programming this register the horizontal active area count register value should also be programmed greater than the RGB word count value, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

Value	Name
00b	Reserved
01b	Non Burst Mode with Sync Pulse
10b	Non Burst Mode with Sync events
11b	Burst Mode

MIPI_WR_COMMAND

MIPI_WR_COMMAND	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B0ECh-6B0EFh
Name:	MIPIA_WR_COMMAND
ShortName:	MIPIA_WR_COMMAND
Power:	PG1
Reset:	soft
Address:	6B8ECh-6B8EFh
Name:	MIPIC_WR_COMMAND
ShortName:	MIPIC_WR_COMMAND
Power:	PG1
Reset:	soft

MIPI Write Data

DWord	Bit	Description
0	31:8	**RESERVED** Format: MBZ
	7:0	**MIPI_WR COMMAND** Access: R/W This register contains the command to be transferred to the panel in command mode.

MIPI_WR_DATA

MIPI_WR_DATA	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6B0CCh-6B0EBh
Name:	MIPIA_WR_DATA
ShortName:	MIPIA_WR_DATA_*
Power:	PG1
Reset:	soft
Address:	6B8CCh-6B8EBh
Name:	MIPIC_WR_DATA
ShortName:	MIPIC_WR_DATA_*
Power:	PG1
Reset:	soft

MIPI Write Data
There are multiple instances of this register format per MIPI Port.

DWord	Bit	Description
0	31:0	**WR_Data** Access: R/W These registers contain the parameters for the command to be transferred to the panel in command mode.

Mirror of Base Data of Stolen Memory

BDSM_0_2_0_PCI - Mirror of Base Data of Stolen Memory

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	0005Ch

Mirror of BSDM_0_0_0_PCI.
This register contains the base address of graphics data stolen DRAM memory.

DWord	Bit	Description
0	31:20	**Graphics Base of Stolen Memory** Default Value: 000000000000b Access: RO Variant This register contains bits 31 to 20 of the base address of stolen DRAM memory. BIOS determines the base of graphics stolen memory by subtracting the graphics stolen memory size (PCI Device 0 offset 52 bits 6:4) from TOLUD (PCI Device 0 offset BC bits 31:20).
	19:1	**RESERVED** Default Value: 000b Access: RO Reserved
	0	**Lock** Default Value: 0b Access: RO Variant This bit will lock all writeable settings in this register, including itself.

Mirror of Capabilities A

CAPID0_A_0_2_0_PCI - Mirror of Capabilities A

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	00044h

Mirror of CAPID0_A_0_0_0_PCI.

DWord	Bit	Description	
0	31	**Display HD Audio Disable**	
		Default Value:	0b
		Access:	RO Variant
	30	**PEG12 Disable**	
		Default Value:	0b
		Access:	RO Variant
	29	**PEG11 Disable**	
		Default Value:	0b
		Access:	RO Variant
	28	**PEG10 Disable**	
		Default Value:	0b
		Access:	RO Variant
	27	**PCI Express Link Width Upconfig Disable**	
		Default Value:	0b
		Access:	RO Variant
	26	**DMI Width**	
		Default Value:	0b
		Access:	RO Variant
	25	**ECC Disable**	
		Default Value:	0b
		Access:	RO Variant
	24	**Force DRAM ECC Enabled**	
		Default Value:	0b
		Access:	RO Variant
	23	**VTd Disable**	
		Default Value:	0b

CAPID0_A_0_2_0_PCI - Mirror of Capabilities A

	Access:	RO Variant
	0: Enable VTd 1: Disable VTd	
22	**DMI Gen 2 Disable**	
	Default Value:	0b
	Access:	RO Variant
21	**PEG Gen 2 Disable**	
	Default Value:	0b
	Access:	RO Variant
20:19	**DDR Size**	
	Default Value:	00b
	Access:	RO Variant
18	**Bclk overclocking disable**	
	Default Value:	0b
	Access:	RO Variant
17	**Disable 1N Mode**	
	Default Value:	0b
	Access:	RO Variant
16	**Full ULT Fuse Read Disable**	
	Default Value:	0b
	Access:	RO Variant
15	**Camarillo Device Disable**	
	Default Value:	0b
	Access:	RO Variant
14	**2 DIMMS per Channel Disable**	
	Default Value:	0b
	Access:	RO Variant
13	**X2APIC Enabled**	
	Default Value:	0b
	Access:	RO Variant
12	**Performance Dual Channel Disable**	
	Default Value:	0b
	Access:	RO Variant
11	**Internal Graphics Disable**	
	Default Value:	0b

CAPID0_A_0_2_0_PCI - Mirror of Capabilities A

		Access: RO Variant 0b: There is a graphics engine within this CPU. Internal Graphics Device (Device 2) is enabled and all of its memory and I/O spaces are accessable. Configuration cycles to Device 2 will be completed within the CPU. All non-SMM memory and IO accesses to VGA will be handled based on Memory and IO enables of Device 2 and IO registers within Device 2 and VGA Enable of the PCI to PCI bridge control (If PCI Express GFX attach is supported). A selected amount of Graphics Memory space is pre-allocated from the main memory based on Graphics Mode Select (GMS in the GGC Register). Graphics Memory is pre-allocated above TSEG Memory. 1b: There is no graphics engine within this CPU. Internal Graphics Device (Device 2) and all of its memory and I/O functions are disabled. Configuration cycle targeted to Device 2 will be passed on. All non-SMM memory and IO accesses to VGA will be handled based on VGA Enable of the PCI to PCI bridge control. Device 2 is disabled and hidden.
	10	**Reserved**
	9:8	**Capability Device ID** Default Value: 00b Access: RO Variant
	7:4	**Compatibility Rev ID** Default Value: 0000b Access: RO Variant
	3	**DDR Overclocking** Default Value: 0b Access: RO Variant
	2	**IA Overclocking Enabled by DSKU** Default Value: 0b Access: RO Variant
	1	**DDR Write Vref Enable** Default Value: 0b Access: RO Variant
	0	**DDR3L Enable** Default Value: 0b Access: RO Variant

Mirror of Capabilities B

CAPID0_B_0_2_0_PCI - Mirror of Capabilities B

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	00048h

Mirror of CAPID0_B_0_0_0_PCI.

DWord	Bit	Description	
0	31	**Reserved_31**	
		Default Value:	0b
		Access:	RO Variant
	30	**IA Overclocking DSKU Control Disable**	
		Default Value:	0b
		Access:	RO Variant
	29	**IA Overclocking Enable**	
		Default Value:	0b
		Access:	RO Variant
	28	**SMT Capability**	
		Default Value:	0b
		Access:	RO Variant
	27:25	**Cache Size Capability**	
		Default Value:	000b
		Access:	RO Variant
	24	**SVMDIS**	
		Default Value:	0b SVM mode enabled
		Access:	RO Variant
	23:21	**DDR3 Maximum Frequency Capability with 100 Memory**	
		Default Value:	000b
		Access:	RO Variant
	20	**Gen3 Disable Fuse for PCIe PEG Controllers**	
		Default Value:	0b
		Access:	RO Variant
	19	**Package Type**	
		Default Value:	0b

CAPID0_B_0_2_0_PCI - Mirror of Capabilities B

	Access:	RO Variant
18	**Additive Graphics Enabled**	
	Default Value:	0b
	Access:	RO Variant
	0 - Additive Graphics Disabled 1- Additive Graphics Enabled	
17	**Additive Graphics Capable**	
	Default Value:	0b
	Access:	RO Variant
	0 - Capable of Additive Graphics 1 - Not capable of Additive Graphics	
16	**Primary PEG Port x16 Disable**	
	Default Value:	0b
	Access:	RO Variant
15:12	**Reserved_15_12**	
	Default Value:	0000b
	Access:	RO Variant
11	**Reserved**	
10:8	**Reserved_10_8**	
	Default Value:	000b
	Access:	RO Variant
7	**Reserved**	
6:4	**DDR3 Maximum Frequency Capability**	
	Default Value:	000b
	Access:	RO Variant
3	**Reserved_3**	
	Default Value:	0b
	Access:	RO Variant
2	**DDR4 DSKU Enable**	
	Default Value:	0b
	Access:	RO
1	**Dual PEG Force x1 when VGA Enabled**	
	Default Value:	0b
	Access:	RO Variant

CAPID0_B_0_2_0_PCI - Mirror of Capabilities B			
	0	**Single PEG Force x1 when VGA Enabled**	
		Default Value:	0b
		Access:	RO Variant

Mirror of Device Enable

DEVEN0_0_2_0_PCI - Mirror of Device Enable

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x000000BF
Size (in bits):	32
Address:	00054h

Mirror of DEVEN_0_0_0_PCI.

DWord	Bit	Description
0	14	**Chap Enable** Default Value: 0b Access: RO Variant
	13	**Device 6 Enable** Default Value: 0b Access: RO
	12:11	**RESERVED** Default Value: 000b Access: RO
	10	**Device 5 Enable** Default Value: 0b Access: RO
	9:8	**RESERVED** Default Value: 000b Access: RO
	7	**Device 4 Enable** Default Value: 1b Access: RO Variant
	6	**RESERVED** Default Value: 000b Access: RO
	5	**Device 3 enable for Display HD Audio** Default Value: 1b Access: RO Variant
	4	**Internal Graphics Engine** Default Value: 1b

DEVEN0_0_2_0_PCI - Mirror of Device Enable

		Access: RO Variant 0: Bus 0 Device 2 is disabled and hidden 1: Bus 0 Device 2 is enabled and visible This bit will be set to 0b and remain 0b if Device 2 capability is disabled.
	3	**PEG10 Enable** Default Value: 1b Access: RO Variant
	2	**PEG11 Enable** Default Value: 1b Access: RO Variant
	1	**PEG12 Enable** Default Value: 1b Access: RO Variant
	0	**Host Bridge** Default Value: 1b Access: RO

Mirror of FUSE2 Control DW

FUSE2 - Mirror of FUSE2 Control DW

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	09120h

FUSE2 Control DW

DWord	Bit	Description
0	31:29	**GT SKU Fuse** Access: RO GT SKU Fuse Bits See project specific configuration table for possible values.
	28	**Spares** Access: RO
	27:25	**GT Slice Enable Fuse** Access: RO Slice Enables Bit25 - Slice0 Enable Bit26 - Slice1 Enable Bit27 - Slice2 Enable See project specific configuration table for possible values.
	24	**Spares1** Access: RO
	23:20	**GT Subslice Disable Fuse** Access: RO Subslice Disable Bits Bit 20 - Subslice0 Disable Bit 21 - Subslice1 Disable Bit 22 - Subslice2 Disable Bit 23 - Subslice3 Disable See project specific configuration table for possible values.
	19:18	**GT VDBox and VEBox Configuration Fuse** Access: RO VDBox and VEbox Configurations: 00b = Both VDBOXes and VEBOXes enabled

FUSE2 - Mirror of FUSE2 Control DW		
		01b = VDBOX1 and VEBOX1 enabled (GT1,2) 10b = VDBOX0 and VEBOX0 enabled (GT1,2) See project specific configuration table for possible values.
	17:16	**Spares3** Access: RO
	15:0	**Capability Fuse** Fixed Definitions within Capability Fuse: Bit 2: Pre-production/post-production fuse. 0b : Pre-Production. Pre or Post Production quality FW will run 1b : Post Production.only Production quality FW will run Other bits defined by SW PDT. Please refer to Project Specific SW PDT for definition/values for these bits.

MMCD Misc Control

MMCD_MISC_CTRL - MMCD Misc Control

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x8000003C
Size (in bits):	32
Address:	04DDCh

This register contains control bits for permute control line address, page faulting mode and cache control bits

DWord	Bit	Description
0	31	**Permute Compressed Line Address** Default Value: 1b Access: R/W Controls where the compressed line is written in memory 1'b0: Write to lower CL address, i.e bit[X]=0 1'b1: Write based on the hash selection as indicated by bit[27] (default)
	30	**Reserved**
	29	**Reserved**
	28	**Reserved**
	27	**Hash Select for Compressed Read/Write Address calculation** Default Value: 0b Access: R/W 1'b0: Legacy mode : Read/Write address computation will be done using a hash of Virtual address bits 6 to 11 bit[X] = bit[X] XOR bit[11] XOR bit[10] XOR bit[9] XOR bit[8] XOR bit[7] XOR bit[6] 1'b1: LLC/eLLC hot spotting avoidance mode : Read/Write address computation will be done using a hash of Virtual address bits 17 to 21 bit[X] = bit[X+1] XOR bit[17] XOR bit[18] XOR bit[19] XOR bit[20] XOR bit[21] Software needs to guarantee that the base address of the resource is aligned to 4MB or ensure that the virtual address is not changed between the passes for compressed surface handling
	26:14	**Reserved_1** Default Value: 0b Access: R/W
	13:11	**Page Faulting Mode** Default Value: 0b Access: R/W this field controls page faulting mode that will be used in the memory interface block for the

MMCD_MISC_CTRL - MMCD Misc Control

		given request coming from this surface 3'b000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:7	**Reserved_2** Default Value: 0b Access: R/W
	6	**Don't allocate on Miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM) 1'b0: Allocate on miss 1'b1: Do Not allocate on miss
	5:4	**Cache Replcament management** Default Value: 3h Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. If a particular allocation is done at youngest age 3 it tends to stay longer in cache as compared to older age allocation - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches 2'b11: Good chance of generating hits 2'b10: Poor chance of generating hits 2'b01: Don't change the LRU if it is a HIT 2'b00: Reserved
	3:2	**Target Cache** Default Value: 3h Access: R/W This field allows the choice of LLC vs eLLC for caching 2'b00: eLLC only 2'b01: LLC only 2'b10: LLC/eLLC allowed 2'b11: LLC/eLLC allowed
	1:0	**LLC/eDRAM Cacheability control** Default Value: 0b Access: R/W Memory type information used in LLC/eDRAM 2'b00: Use cacheability controls from page table/ UC with fence (if coherent cycle)

MMCD_MISC_CTRL - MMCD Misc Control		
		2'b01: Uncacheable(UC) - non-cacheable 2'b10: Writethrough (WT) 2'b11: Writeback (WB)

MMIO_INDEX

MMIO_INDEX - MMIO_INDEX

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	00000h

Contains address and target.
Punit cannot access IO space from message channel.
A 32 bit IO write to this port loads the offset of the MMIO register or offsetinto the GTT that needs to be accessed.
An IO Read returns the current value of this register. An 8/16 bit IO write to this register is completed but does not update this register.
This mechanism to access internal graphics MMIO registers must not be used to access VGA IO registers which are mapped through the MMIO space. VGA registers must be accessed directly through the dedicated VGA IO ports. This is used by SBIOS. It is not used by graphics driver.
This register is only accessible through the IOSF Primary bus. The base register is defined by IOBAR.

DWord	Bit	Description
0	31:2	**Register_offset** Default Value: 00000000h Access: R/W This field selects GTT entry or any one of the Dword registers within the MMIO register space of this device.
	1:0	**Target** Default Value: 00b Access: R/W 00 = MMIO Registers, 01 = GTT, 1X = Reserved

MMIO Mirror of GMCH Graphics Control Register

MGGC_ - MMIO Mirror of GMCH Graphics Control Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000500
Access:	RO
Size (in bits):	32
Address:	108040h

All the bits in this register are Intel TXT lockable.

DWord	Bit	Description
0	31:16	**RESERVED** Default Value: 000h Access: RO Reserved
	15:8	**GMS** Default Value: 05h Access: RO This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. It corresponds to DSM (Data Stolen Memory region) region. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled. BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0. BIOS Requirement: Given new sizes allow down to 8MB allocation, BIOS has to ensure there is sufficient space for WOPCM and basic GFX Stolen functions. 00h:0MB 01h:32MB 02h:64MB 03h:96MB 04h:128MB 05h:160MB 06h:192MB 07h:224MB 08h:256MB 09h:288MB 0Ah:320MB 0Bh:352MB 0Ch:384MB

MGGC_ - MMIO Mirror of GMCH Graphics Control Register

		0Dh:416MB 0Eh:448MB 0Fh:480MB 10h:512MB 11h - 1Fh: Reserved 20h:1024MB 21h - 2Fh: Reserved 30h:1536MB 31h - 3Fh: Reserved 40h: 2048MB 41h - EFh: Reserved F0h: 4MB F1h: 8MB F2h: 12MB F3h: 16MB F4h: 20MB F5h: 24MB F6h: 28MB F7h: 32MB F8h: 36MB F9h: 40MB FAh: 44MB FBh: 48MB FCh: 52MB FDh: 56MB FEh: 60MB FFh: Reserved Hardware functionality in case of programming this value to Reserved is not guaranteed.
	7:6	**GGMS** Default Value: 00b Access: RO This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware will derive the base of GSM from DSM only using the GSM size programmed in the register. Hardware functionality in case of programming this value to Reserved is not guaranteed. 0x0:No Preallocated Memory 0x1:2MB of Preallocated Memory 0x2:4MB of Preallocated Memory 0x3:8MB of Preallocated Memory

MGGC_ - MMIO Mirror of GMCH Graphics Control Register

	5:3	**RESERVED** Default Value: 000b Access: RO Enables the use of the iGFX enbines for Versatile Acceleration. 1 - iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 048000h. 0 - iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h.
	2	**VAMEN** Default Value: 0b Access: RO Reserved
	1	**IVD** Default Value: 0b Access: RO 0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub- Class Code field within Device 2 function 0 Class Code register is 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field (bits 7:3 of this register) pre-allocates no memory. This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override (CAPID0_A[IGD] = 1) or via a register (DEVEN[3] = 0). This register is locked by Intel TXT lock. 0:Enable 1:Disable
	0	**GGCLCK** Default Value: 0b Access: RO When set to 1b, this bit will lock all bits in this register.

MTOLUD

MTOLUD - MTOLUD

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00100000
Size (in bits):	32
Address:	108000h

This 32 bit register defines the Top of Low Usable DRAM. TSEG, GTT Graphics memory and Graphics Stolen Memory are within the DRAM space defined.
From the top, the Host optionally claims 1 to 64MBs of DRAM for internal graphics if enabled, 1or 2MB of DRAM for GTT Graphics Stolen Memory (if enabled) and 1, 2, or 8 MB of DRAM for TSEG if enabled.
Programming Example:
C1DRB3 is set to 4GB
TSEG is enabled and TSEG size is set to 1MB
Internal Graphics is enabled, and Graphics Mode Select is set to 32MB
GTT Graphics Stolen Memory Size set to 2MB
BIOS knows the OS requires 1G of PCI space.
BIOS also knows the range from 0_FEC0_0000h to 0_FFFF_FFFFh is not usable by the system. This 20MB range at the very top of addressable memory space is lost to APIC and LT.
According to the above equation, TOLUD is originally calculated to: 4GB = 1_0000_0000h
The system memory requirements are: 4GB (max addressable space) - 1GB (pci space) - 35MB (lost memory) = 3GB - 35MB (minimum granularity) = 0_ECB0_0000h
Since 0_ECB0_0000h (PCI and other system requirements) is less than 1_0000_0000h, TOLUD should be programmed to ECBh.
These bits are Intel TXT lockable.

DWord	Bit	Description
0	31:20	**TOLUD** Default Value: 001h Access: RO Variant This register contains bits 31 to 20 of an address one byte above the maximum DRAM memory below 4G that is usable by the operating system. Address bits 31 down to 20 programmed to 01h implies a minimum memory size of 1MB. Configuration software must set this value to the smaller of the following 2 choices: maximum amount memory in the system minus ME stolen memory plus one byte or the minimum address allocated for PCI memory. Address bits 19:0 are assumed to be 0_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register. The Top of Low Usable DRAM is the lowest address above both Graphics Stolen memory and Tseg. BIOS determines the base of Graphics Stolen Memory by subtracting the Graphics Stolen Memory Size from TOLUD and further decrements by Tseg size to determine base of Tseg. All

MTOLUD - MTOLUD

		the Bits in this register are locked in LT mode. This register must be 1MB aligned when reclaim is enabled.
	19:1	**RESERVED** Default Value: 000h Access: RO Variant Reserved
	0	**LOCK** Default Value: 0b Access: RO Variant This bit will lock all writeable settings in this register, including itself.

MTOUUD_LSB

MTOUUD_LSB - MTOUUD_LSB

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00100000
Size (in bits):	32
Address:	108080h

This 64 bit register defines the Top of Upper Usable DRAM.
Configuration software must set this value to TOM minus all ME stolen memory if reclaim is disabled. If reclaim is enabled, this value must be set to reclaim limit + 1byte, 1MB aligned, since reclaim limit is 1MB aligned.
Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than or equal to 4GB.
BIOS Restriction: Minimum value for TOUUD is 4GB.
These bits are Intel TXT lockable.

DWord	Bit	Description
0	31:20	**TOUUD** Default Value: 001h Access: RO This register contains bits 38 to 20 of an address one byte above the maximum DRAM memory above 4G that is usable by the operating system. Configuration software must set this value to TOM minus all ME stolen memory if reclaim is disabled. If reclaim is enabled, this value must be set to reclaim limit 1MB aligned since reclaim limit + 1byte is 1MB aligned. Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than 4GB. All the bits in this register are locked in Intel TXT mode.
	19:1	**RESERVED** Default Value: 000h Access: RO Reserved
	0	**LOCK** Default Value: 0b Access: RO This bit will lock all writeable settings in this register, including itself.

MTOUUD_MSB

MTOUUD_MSB - MTOUUD_MSB

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	108084h

This 64 bit register defines the Top of Upper Usable DRAM.
Configuration software must set this value to TOM minus all ME stolen memory if reclaim is disabled. If reclaim is enabled, this value must be set to reclaim limit + 1byte, 1MB aligned, since reclaim limit is 1MB aligned.
Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than or equal to 4GB.
BIOS Restriction: Minimum value for TOUUD is 4GB.
These bits are Intel TXT lockable.

DWord	Bit	Description
0	31:7	**RESERVED** Default Value: 0000000h Access: RO Reserved
	6:0	**TOUUD** Default Value: 00h Access: RO This register contains bits 38 to 20 of an address one byte above the maximum DRAM memory above 4G that is usable by the operating system. Configuration software must set this value to TOM minus all ME stolen memory if reclaim is disabled. If reclaim is enabled, this value must be set to reclaim limit 1MB aligned since reclaim limit + 1byte is 1MB aligned. Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than 4GB. All the bits in this register are locked in Intel TXT mode.

Multi Size Aperture Control

MSAC_0_2_0_PCI - Multi Size Aperture Control

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000001
Size (in bits):	8
Address:	00062h

This register determines the size of the graphics memory aperture (GMADR) in function 0 and in the trusted space, and affects certain bits of the GMADR register.
Bits [4:0] 00000b: 128MB, GMADR[26:4] is hardwired to all 0
Bits [4:0] 00001b: 256MB, GMADR[27:4] overriden to all 0
Bits [4:0] 00010b: illegal (hardware will treat this as 00011b)
Bits [4:0] 00011b: 512MB, GMADR[28:27] overriden to all 0
Bits [4:0] 00100-00110b: illegal (hardware will treat this as 00111b)
Bits [4:0] 00111b: 1024MB, GMADR[29:27] overriden to all 0
Bits [4:0] 01000-01110b: illegal (hardware will treat this as 01111b)
Bits [4:0] 01111b: 2048MB, GMADR[30:27] overriden to all 0
Bits [4:0] 10000-11110b: illegal (hardware will treat this as 11111b)
Bits [4:0] 11111b: 4096MB, GMADR[31:27] overriden to all 0

DWord	Bit	Description
0	7:5	**Reserved R/W** Default Value: 000b Access: R/W Scratch Bits
	4	**Untrusted Aperture Size Bit 4** Default Value: 0b Access: R/W Key
	3	**Untrusted Aperture Size Bit 3** Default Value: 0b Access: R/W Key
	2	**Untrusted Aperture Size Bit 2** Default Value: 0b Access: R/W Key
	1	**Untrusted Aperture Size Bit 1** Default Value: 0b Access: R/W Key

MSAC_0_2_0_PCI - Multi Size Aperture Control			
	0	**Untrusted Aperture Size Bit 0**	
		Default Value:	1b
		Access:	R/W Key

NDE_RSTWRN_OPT

NDE_RSTWRN_OPT

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	46408h-4640Bh
Name:	North Display Reset Warn Options
ShortName:	NDE_RSTWRN_OPT
Power:	PG0
Reset:	global

This register is used to control the display behavior on receiving a Reset Warning.

DWord	Bit	Description
0	31:7	**Reserved** Format: MBZ
	6	**Reserved** Format: MBZ
	5	**Reserved**
	4	**RST PCH Handshake En** This field enables the handshake with PCH display when processing the reset. This applies to all types of DE resets. By default it is disabled and the north display will not wait for south display to acknowledge the reset. Value / Name: 0b – Disable 1b – Enable **Programming Notes** This field must never be programmed to 1b.
	3:0	**Reserved**

Observation Architecture Control per Context

OACTXCONTROL - Observation Architecture Control per Context

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02360h

This register is implemented in render command streamer and render context save/restored.
This register should be initialized by SW appropriately on the very first submission of a context when OA is enabled.

DWord	Bit	Description
0	31	**Reserved** Format: PBC
	30:8	**Reserved** Format: PBC
	7:2	**Timer Period** Format: Select Specifies the period of the timer strobe as a function of the minimum TIME_STAMP resolution. The period is determined by selecting a specified bit from the TIME_STAMP register as follows: StrobePeriod = MinimumTimeStampPeriod * 2 **(TimerPeriod + 1)** The exponent is defined by this field. **Note:** The TIME_STAMP is not reset at start time so the phase of the strobe is not synchronized with the enable of the OA unit. This could result in approximately a full StrobePeriod elapsing prior to the first trigger. Usage for this mechanism should be time based periodic triggering, typically.
	1	**Timer Enable** Format: Enable **Description** This field enables the timer logic to output a periodic strobe, as defined by the Timer Period. When disabled the timer output is not asserted. Users should be aware that the timer-based report logic and the Boolean report trigger logic are logically OR'd together with no buffering of report triggers. This implies that only one performance counter report will be generated for clocks where both the timer-based report logic and the Boolean report trigger logic trigger a performance counter report. When "Specific Context Enable" bit is set to '1' in OACONTROL register, Timer based report

OACTXCONTROL - Observation Architecture Control per Context

trigger function gets enabled only for the selected context.
When "Specific Context Enable" bit is set to '0' in OACONTROL register, Timer based report trigger function gets enabled for all contexts.

Value	Name	Description
0h	Disable **[Default]**	Counter does not get written out on regular interval
1h	Enable	Counter gets written out on regular intervals, defined by the Timer Period

0 **Counter Stop-Resume Mechanism**

Format:	Select

Value	Name	Description
1h		resume counting for all counters

Outstanding Page Request Allocation

OPRA_0_2_0_PCI - Outstanding Page Request Allocation

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	0030Ch

DWord	Bit	Description
0	31:0	**Outstanding Page Request Allocation** Default Value: 00000000000000000000000000000000b Access: R/W This register contains the number of outstanding page request messages the associated Page Request Interface is allowed to issue.

Outstanding Page Request Capacity

OPRC_0_2_0_PCI - Outstanding Page Request Capacity

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00008000
Size (in bits):	32
Address:	00308h

DWord	Bit	Description
0	31:0	**Outstanding Page Request Capacity** Default Value: 00000000000000001000000000000000b Access: RO This register contains the number of outstanding page request messages the associated Page Request Interface physically supports. This is the upper limit on the number of pages that can be usefully allocated to the Page Request Interface. Hardwired to 32,768 requests.

Page Request Control

PR_CTRL_0_2_0_PCI - Page Request Control

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	16
Address:	00304h

DWord	Bit	Description
0	15:2	**RESERVED** Default Value: 000b Access: RO Reserved
	1	**Reset** Default Value: 0b Access: RO When the Enable field is clear, or is being cleared in the same register update that sets this field, writing a 1b to this field, clears the associated implementation dependent page request credit Counter and pending request state for the associated Page Request Interface. No action is initiated if this field is written to 0b or if this field is written with any value when the PRE field is set. Processor graphics does not use this field, and hardwires it as read-only (0).
	0	**Page-Request Enable** Default Value: 0b Access: R/W When Set, indicates that the page request interface on the endpoint is allowed to make page requests. If both this field and the Stopped field in Page Request Status register are Clear, then the Page request interface will not issue new page requests, but has outstanding page requests for which page responses is not yet received. When this field transitions from 0 to 1, all the status fields in the Page-Request Status register are cleared. Enabling a page request interface that has not successfully stopped has indeterminate results.

Page Request Extended Capability Header

PR_EXTCAP_0_2_0_PCI - Page Request Extended Capability Header

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00010013
Size (in bits):	32
Address:	00300h

Page Request Extended Capability reports support for page-faults on Device-2, compliant to PCI-Express ATS 1.1 Specification

DWord	Bit	Description
0	31:20	**Next Capability Offset** Default Value: 000000000000b Access: RO This is a hardwired pointer to the next item in the capabilities list. Value 000h indicates that this is the end of the PCI-Express Extended capability Linked List.
	19:16	**Version** Default Value: 0001b Access: RO Hardwired to capability version 1.
	15:0	**Capability ID** Default Value: 0000000000010011b Access: RO Hardwired to the Page Request Extended Capability ID

Page Request Status

PR_STATUS_0_2_0_PCI - Page Request Status

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00008000
Size (in bits):	16
Address:	00306h

DWord	Bit	Description
0	15	**PRG Response PASID Required** Default Value: 1b Access: RO If set, the Function expects a PASID TLP Prefix on PRG Response Messages when the corresponding page requests had a PASID TLP Prefix. If Clear, the function does not expect PASID TLP Prefixes on any PRG Response Message. Function behavior is undefined if this bit is Clear and the Function receives a PRG Response Message with a PASID TLP Prefix. Function behavior is undefined if this bit is Set and the Function receives a PRG Response Message with no PASID TLP Prefix when the corresponding Page Requests had a PASID TLP Prefix. This bit is RsvdZ if the Function does not support the PASID TLP Prefix.
	14:9	**RESERVED** Default Value: 000b Access: RO Reserved
	8	**Stopped** Access: RO When this field is Set, the associated page request interface has stopped issuing additional Page requests and that all previously issued Page requests have completed. When this field is clear the associate Page request interface either has not stopped or has stopped issuing new Page requests but has outstanding Page requests. Value: 0b — Name: **[Default]**
	7:2	**RESERVED** Default Value: 000b Access: RO Reserved

PR_STATUS_0_2_0_PCI - Page Request Status

	1	**Unexpected Page Request Group Index** Default Value: 0b Access: R/W One Clear When Set, indicates the function received a PRG response message containing a PRG index that has no matching request, a response failure. This field is Set by the Function and cleared when a 1b is written to the field.
	0	**Response Failure** Default Value: 0b Access: R/W One Clear When Set, indicates the function received a PRG response message indicating a response failure. The function expects no further response from the host (any received are ignored). This field is Set by the Function and cleared when a 1b is written to this field.

PAK_Stream-Out Report (Errors)

PAK_ERR - PAK_Stream-Out Report (Errors)

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	128E8h

DWord	Bit	Description
0	31:22	**Reserved** Format: MBZ
	21	**Incorrect IntraMBFlag in I-slice(AVCf)**
	20	**Out of Range Symbol Code(AVC/mpeg2)**
	19	**Incorrect MBType(AVC/mpeg2**
	18	**Motion Vectors are not inside the frame boundary(mpeg2)**
	17	**Scale code is zero(mpeg2)**
	16	**Incorrect DCTtype for given motionType(mpeg2)**
	15:8	**MB Y-position** Description: This field indicates Macro Block(MB) Y- position where an error occurred while encoding.
	7:0	**MB X-position** Description: This field indicates Macro Block(MB) X- position where an error occurred while encoding.

PASID Capability

PASID_CAP_0_2_0_PCI - PASID Capability

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00001402
Size (in bits):	16
Address:	00104h

PASID capability reports support for Process Address Space ID(PASID) on Device-2, compliant to PCI-Express PASID ECN.

DWord	Bit	Description
0	15:13	**RESERVED** Default Value: 000b Access: RO Reserved
	12:8	**Maximum PASID Width** Default Value: 10100b Access: RO Indicates the width of the PASID field supported by the Endpoint. Hardwired to 14h to indicate support for all PASID values (20 bits).
	7:3	**RESERVED** Default Value: 000b Access: RO Reserved
	2	**Privilege Mode Supported** Default Value: 0b Access: RO Hardwired to 0, the Endpoint supports operating in Non-privileged mode only, and will never request privileged mode in requests-with-PASID.
	1	**Execute Permission Supported** Access: RO Description: Hardwired to 1, the Endpoint supports requests-with-PASID that requests execute permission.

PASID_CAP_0_2_0_PCI - PASID Capability

		Value / **Name** 1b / **[Default]**
	0	**RESERVED** Default Value: 000b Access: RO Reserved

PASID Control

PASID_CTRL_0_2_0_PCI - PASID Control

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	8
Address:	00106h

Process Address Space ID (PASID) control for Device-2.

DWord	Bit	Description
0	15:3	**RESERVED** Default Value: 000b Access: RO Reserved
	2	**Privileged Mode Enable** Default Value: 0b Access: RO Hardwired to 0, the Endpoint is not permitted to request privileged mode in requests-with-PASID.
	1	**Execute Permission Enable** Default Value: 0b Access: R/W If Set, the Endpoint is permitted to request execute permission in requests-with-PASID. If Clear, the Endpoint is not permitted to do so. Behavior is undefined if this bit changes value when ATS Enable field in ATS Capability is Set. Processor graphics does not use this field. Software is expected to Set this field before configuring extended-context-entry for Device-2 with the Execute Request Enable field Set.
	0	**PASID Enable** Default Value: 0b Access: R/W If Set, the Endpoint is permitted to generate requests-with-PASID. If Clear, the Endpoint is not permitted to do so. Behavior is undefined if this bit changes value when ATS Enable field in ATS Capability is Set. If Priviliged Mode Supported field in PASID Capability register is Clear, then this field is treated as Reserved(0). Processor graphics does not use this field. Software is expected to Set this field before configuring extended-context-entry for Device-2 with Supervisor Request Enable field Set. For compatibility reasons, this field is implemented as RW.

PASID Extended Capability Header

PASID_EXTCAP_0_2_0_PCI - PASID Extended Capability Header

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x2001001B
Size (in bits):	32
Address:	00100h

PASID capability reports support for Process Address Space ID(PASID) on Device-2, compliant to PCI-Express PASID ECN.

DWord	Bit	Description
0	31:20	**Next Capability Offset** Default Value: 001000000000b Access: RO This is a hardwired pointer to the next item in the capabilities list.
	19:16	**Version** Default Value: 0001b Access: RO Hardwired to capability version 1.
	15:0	**Capability ID** Default Value: 0000000000011011b Access: RO Hardwired to the PASID Extended Capability ID

PAT Index High

PAT_INDEX_H - PAT Index High		
Register Space:	MMIO: 0/2/0	
Default Value:	0x03030303	
Size (in bits):	32	
Address:	040E4h	

DWord	Bit	Description
0	31:0	**PAT Index High** Default Value: 03030303h Access: R/W

PAT Index Low

PAT_INDEX_L - PAT Index Low		
Register Space:	MMIO: 0/2/0	
Default Value:	0x03030303	
Size (in bits):	32	
Address:	040E0h	
DWord	**Bit**	**Description**
0	31:0	**PAT Index Low** Default Value: 03030303h Access: R/W Bit[31:24]: PAT Index#3: Index#3 definition for page tables. (See bit[7:0] for definition.) Bit[23:16]: PAT Index#2: Index#2 definition for page tables. (See bit[7:0] for definition.) Bit[15:8]: PAT Index#1: Index#1 definition for page tables. (See bit[7:0] for definition.) Bit[7:0]: PAT Index#0: Index#0 definition for page tables. Bit[7]: Reserved. Bit[6]: Snoop Control. Note: S/W should NOT set this field in client platforms Bit[5:4]: (See below.) 00b: Age is 0. 01b: Age is 1. 10b: Age is 2. 11b: Age is 3. Bit[3:2]: (See below.) 00b: Override to eLLC Only. (This setting overrides the memory_object_control_state via surface state to be eLLC target only.) 01b: eLLC only. 10b: LLC only. 11b: eLLC/LLC. Bit[1:0]: (see below): 00b: Uncached with fence. 01b: Write Combining (traditional UC). 10b: Write Through. 11b: Write Back.

PCI Command

PCICMD_0_2_0_PCI - PCI Command

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	16
Address:	00004h

This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD Register in the IGD disables the IGD PCI compliant master accesses to main memory.

DWord	Bit	Description
0	15:11	**RESERVED** Default Value: 000b Access: RO Reserved
	10	**Interrupt Disable** Default Value: 0b Access: R/W This bit disables the device from asserting INTx#. 0: Enable the assertion of this device's INTx# signal. 1: Disable the assertion of this device's INTx# signal. DO_INTx messages will not be sent to DMI.
	9	**Fast Back-to-Back** Default Value: 0b Access: RO Not Implemented. Hardwired to 0.
	8	**SERR Enable** Default Value: 0b Access: RO Not Implemented. Hardwired to 0.
	7	**Wait Cycle Control** Default Value: 0b Access: RO Not Implemented. Hardwired to 0.

PCICMD_0_2_0_PCI - PCI Command

6 — Parity Error Enable

Default Value:	0b
Access:	RO

Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.

5 — Video Palette Snooping

Default Value:	0b
Access:	RO

This bit is hardwired to 0 to disable snooping.

4 — Memory Write and Invalidate Enable

Default Value:	0b
Access:	RO

Hardwired to 0. The IGD does not support memory write and invalidate commands.

3 — Special Cycle Enable

Default Value:	0b
Access:	RO

This bit is hardwired to 0. The IGD ignores Special cycles.

2 — Bus Master Enable

Default Value:	0b
Access:	R/W

0: Disable IGD bus mastering.
1: Enable the IGD to function as a PCI compliant master.

1 — Memory Access Enable

Default Value:	0b
Access:	R/W

This bit controls the IGD's response to memory space accesses.
0: Disable.
1: Enable.

PCICMD_0_2_0_PCI - PCI Command

	0	**I/O Access Enable** Default Value: 0b Access: R/W This bit controls the IGD's response to I/O space accesses. 0: Disable. 1: Enable. This field is RO 1'b0 if DEV2CTL[0] IOBARDIS at offset 0x58 is 1b.

PCI Express Capability

PCIECAP_0_2_0_PCI - PCI Express Capability

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000092
Size (in bits):	16
Address:	00072h

PCI Express Capability

DWord	Bit	Description
0	15:14	**RESERVED** Default Value: 000b Access: RO Reserved
	13:9	**Interrupt Message Number** Default Value: 00000b Access: RO This field indicates which MSI vector is used for the interrupt message generated in association with any of the status bits of this Capability structure. Since this device only supports one MSI vector, this field is hardwired to 0.
	8	**Slot Implemented** Default Value: 0b Access: RO This field is hardwired to 0 for an endpoint device.
	7:4	**Device Type** Default Value: 1001b Access: RO This field is hardwired to 9h to indicate a Root Complex Integrated Endpoint.
	3:0	**Capability Version** Default Value: 0010b Access: RO This field is hardwired to 2h to indicate Functions compliant to PCI Express 3.0 Base Specification.

PCI Express Capability Header

PCIECAPHDR_0_2_0_PCI - PCI Express Capability Header

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x0000AC10
Size (in bits):	16
Address:	00070h

PCI Express Capability Header

DWord	Bit	Description
0	15:8	**Next Capability Pointer** Default Value: 10101100b Access: RO This field is hardwired to point to the next PCI Capability structure, the MSI Capabilities at ACh.
	7:0	**Capability Identifier** Default Value: 00010000b Access: RO This field is hardwired to 10h to indicate that this is a PCI Express Capability structure.

PCI Express Capability Structure

DEVICESTS_0_2_0_PCI - PCI Express Capability Structure

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	16
Address:	0007Ah

PCI Express Capability Structure

DWord	Bit	Description
0	15:6	**RESERVED** Default Value: 0000000000b Access: RO Reserved
	5	**Transactions Pending** Default Value: 0b Access: RO When Set, this bit indicates that the Function has issued Non-Posted Requests that have not been completed. A Function reports this bit is cleared only when all outstanding Non-Posted Requests have completed or have been terminated by the Completion Timeout mechanism. This bit must also be cleared upon the completion of an FLR.
	4	**Aux Power Detected** Default Value: 0b Access: RO Functions that require Aux power report this bit as Set if Aux power is detected by the Function. Hardwired to 0b, the integrated graphics device does not require Aux power.
	3	**Unsupported Request Detected** Default Value: 0b Access: RO This bit indicates the Function received an Unsupported Request. Hardwired to 0b, the Root Complex Integrated Endpoint graphics device does not use the PCI Express error reporting mechanism.
	2	**Fatal Error Detected** Default Value: 0b Access: RO

DEVICESTS_0_2_0_PCI - PCI Express Capability Structure

		This bit indicates the status of Fatal errors detected. Hardwired to 0b, the Root Complex Integrated Endpoint graphics device does not use the PCI Express error reporting mechanism.
	1	**Non-Fatal Error Detected** Default Value: 0b Access: RO This bit indicates the status of Non-Fatal errors detected. Hardwired to 0b, the Root Complex Integrated Endpoint graphics device does not use the PCI Express error reporting mechanism.
	0	**Correctable Error Detected** Default Value: 0b Access: RO This bit indicates the status of Correctable errors detected. Hardwired to 0b, the Root Complex Integrated Endpoint graphics device does not use the PCI Express error reporting mechanism.

PCI Express Device Control

DEVICECTL_0_2_0_PCI - PCI Express Device Control

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	16
Address:	00078h

PCI Express Device Control

DWord	Bit	Description
0	15	**Initiate Function Level Reset** Default Value: 0b Access: R/W A write of 1b initiates Function Level Reset to the Function. During FLR, a read will return 1b since device 2 reads abort. If a local panel is powered on and configured to power down on reset, the FLR will typically take several hundred milliseconds to complete. The worst possible, although unrealistic, delay is 5 seconds.
	14:12	**Max Read Request Size** Default Value: 000b Access: RO Functions that do not generate Read Requests larger than 128 bytes and Functions that do not generate Read Requests on their own behalf are permitted to implement this field as Read Only (RO) with a value of 000b.
	11	**Enable No Snoop** Default Value: 0b Access: RO This bit is permitted to be hardwired to 0b if a Function would never Set the No Snoop attribute in transactions it initiates. The graphics device never generates a PCI Express TLP.
	10	**Aux Power PM Enable** Default Value: 0b Access: RO Functions that do not implement this capability hardwire this bit to 0b.

DEVICECTL_0_2_0_PCI - PCI Express Device Control

	9	**Phantom Functions Enable** Default Value: 0b Access: RO Functions that do not implement this capability hardwire this bit to 0b.
	8	**Extended Tag field Enable** Default Value: 0b Access: RO Functions that do not implement this capability hardwire this bit to 0b.
	7:5	**Max Payload Size** Default Value: 000b Access: RO Functions that support only the 128-byte max payload size are permitted to hardwire this field to 000b.
	4	**Enable Relaxed Ordering** Default Value: 0b Access: RO A Function is permitted to hardwire this bit to 0b if it never sets the Relaxed Ordering attribute in transactions it initiates as a Requester. The graphics device never generates a PCI Express TLP.
	3	**Unsupported Request Response Enable** Default Value: 0b Access: RO A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.
	2	**Fatal Error Enable** Default Value: 0b Access: RO A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.
	1	**Non-Fatal Error Enable** Default Value: 0b Access: RO A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.

DEVICECTL_0_2_0_PCI - PCI Express Device Control

	0	**Correctable Error Enable** Default Value: 0b Access: RO A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.

PCI Mirror of GMCH Graphics Control

MGGC0_0_2_0_PCI - PCI Mirror of GMCH Graphics Control

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000500
Size (in bits):	16
Address:	00050h

Mirror of GGC_0_0_0_PCI.

DWord	Bit	Description
0	15:8	**Graphics Mode Select** Default Value: 00000101b Access: RO Variant This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled. BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0. BIOS Requirement: Given new sizes allow down to 8MB allocation, BIOS has to ensure there is sufficient space for WOPCM and basic GFX Stolen functions. 00h:0MB 01h:32MB 02h:64MB 03h:96MB 04h:128MB 05h:160MB (default) 06h:192MB 07h:224MB 08h:256MB 09h:288MB 0Ah:320MB 0Bh:352MB 0Ch:384MB 0Dh:416MB 0Eh:448MB 0Fh:480MB 10h:512MB 11h - 1Fh: Reserved 20h:1024MB 21h - 2Fh: Reserved 30h:1536MB 31h - 3Fh: Reserved 40h: 2048MB

MGGC0_0_2_0_PCI - PCI Mirror of GMCH Graphics Control

41h - EFh: Reserved
F0h: 4MB
F1h: 8MB
F2h: 12MB
F3h: 16MB
F4h: 20MB
F5h: 24MB
F6h: 28MB
F7h: 32MB
F8h: 36MB
F9h: 40MB
FAh: 44MB
FBh: 48MB
FCh: 52MB
FDh: 56MB
FEh: 60MB
FFh: Reserved Hardware functionality in case of programming this value to Reserved is not guaranteed.

7:6 GTT Graphics Memory Size

Access:	RO Variant

This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware will derive the base of GSM from DSM only using the GSM size programmed in the register. Hardware functionality in case of programming this value to Reserved is not guaranteed.
0x0: No Preallocated Memory
0x1: 2MB of Preallocated Memory
0x2: 4MB of Preallocated Memory
0x3: 8MB of Preallocated Memory

Value	Name	Description
00b	**[Default]**	No Preallocated Memory
01b		2MB of Preallocated Memory
10b		4MB of Preallocated Memory
11b		8MB of Preallocated Memory

5:3 RESERVED

Default Value:	000b
Access:	RO

Reserved

2 Versatile Acceleration Mode Enable

MGGC0_0_2_0_PCI - PCI Mirror of GMCH Graphics Control

		Default Value: 0b Access: RO Variant Enables the use of the iGFX engines for Versatile Acceleration. 1 - iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 048000h. 0 - iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h.
	1	**IGD VGA Disable** Default Value: 0b Access: RO Variant 0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub- Class Code field within Device 2 function 0 Class Code register is 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field pre-allocates no memory. This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override (CAPID0_A[IGD] = 1) or via a register (DEVEN[3] = 0).
	0	**GGC Lock** Default Value: 0b Access: RO Variant **Description** When set to 1b, this bit will lock all bits in this register.

PCI Status

PCISTS2_0_2_0_PCI - PCI Status

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000010
Size (in bits):	16
Address:	00006h

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant master abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

DWord	Bit	Description
0	15	**Detected Parity Error** Default Value: 0b Access: RO Since the IGD does not detect parity, this bit is always hardwired to 0.
	14	**Signaled System Error** Default Value: 0b Access: RO The IGD never asserts SERR#, therefore this bit is hardwired to 0.
	13	**Received Master Abort Status** Default Value: 0b Access: RO The IGD never gets a Master Abort, therefore this bit is hardwired to 0.
	12	**Received Target Abort Status** Default Value: 0b Access: RO The IGD never gets a Target Abort, therefore this bit is hardwired to 0.
	11	**Signaled Target Abort Status** Default Value: 0b Access: RO Hardwired to 0. The IGD does not use target abort semantics.
	10:9	**DEVSEL Timing** Default Value: 00b Access: RO

PCISTS2_0_2_0_PCI - PCI Status

		Hardwired to 00.
	8	**Master Data Parity Error Detected** Default Value: 0b Access: RO Since Parity Error Response is hardwired to disabled, and the IGD does not do any parity detection, this bit is hardwired to 0.
	7	**Fast Back-to-Back** Default Value: 0b Access: RO Hardwired to 0 to be compliant to PCI Express Base Spec (rev 3.0).
	6	**User Defined Format** Default Value: 0b Access: RO Hardwired to 0.
	5	**66 MHz PCI Capable** Default Value: 0b Access: RO Hardwired to 0.
	4	**Capability List** Default Value: 1b Access: RO This bit is hardwired to 1 to indicate that the register at 34h provides an offset into the function's PCI Configuration Space containing a pointer to the location of the first item in the list.
	3	**Interrupt Status** Default Value: 0b Access: RO Variant This bit reflects the state of the interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the devices INTx# signal be asserted.
	2:0	**RESERVED** Default Value: 000b Access: RO Reserved

PCU Interrupt Definition

PCU Interrupt Definition

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	444E0h-444EFh
Name:	PCU Interrupts
ShortName:	PCU_INTERRUPT
Power:	PG0
Reset:	soft

This table indicates which events are mapped to each bit of the PCU Interrupt registers.
0x444E0 = ISR
0x444E4 = IMR
0x444E8 = IIR
0x444EC = IER

DWord	Bit	Description
0	31	**DDIA DC9 HPD** This field indicates DDIA hotplug activity was detected during DC9.
	30	**DDIB DC9 HPD** This field indicates DDIB hotplug activity was detected during DC9.
	29	**DDIC DC9 HPD** This field indicates DDIC hotplug activity was detected during DC9.
	28:26	**Unused_Int_28_26** These interrupts are currently unused.
	25	**PCU_Pcode2driver_Mailbox_Event**
	24	**PCU_Thermal_Event**
	23:0	**Unused_Int_23_0** These interrupts are currently unused.

PHY_CTL_DDI

PHY_CTL_DDI	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	64C00h-64C03h
Name:	PHY_CTL_DDI_A
ShortName:	PHY_CTL_DDI_A
Power:	PG0
Reset:	global
Address:	64C10h-64C13h
Name:	PHY_CTL_DDI_B
ShortName:	PHY_CTL_DDI_B
Power:	PG0
Reset:	global
Address:	64C20h-64C23h
Name:	PHY_CTL_DDI_C
ShortName:	PHY_CTL_DDI_C
Power:	PG0
Reset:	global

This register is on the ungated clock and the chip reset, not the FLR.
Writes to this register will not trigger PSR exit.

DWord	Bit	Description
0	31:30	**Reserved**
	29:28	**Reserved**
	27:26	**Reserved**
	25:24	**Reserved**
	23:22	**Reserved**
	21:20	**Reserved**
	19:18	**Reserved**
	17:16	**Reserved**
	15	**Spare 15**
	14	**Spare 14**

PHY_CTL_DDI

	13	**Spare 13**
	12	**Spare 12**
	11	**Spare 11**
	10	**Common Lane Powerdown Acknowledge** Access: RO
	9	**Lane Powerdown Acknowledge** Access: RO
	8	**Lane Status** Access: RO Value / Name: 0b – Disable 1b – Enable
	7	**Spare 7**
	6	**Spare 6**
	5	**Spare 5**
	4	**Reserved**
	3:0	**Reserved**

PHY_CTL_FAMILY

PHY_CTL_FAMILY

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	64C80h-64C83h
Name:	PHY_CTL_FAMILY_EDP
ShortName:	PHY_CTL_FAMILY_EDP
Power:	PG0
Reset:	global
Address:	64C90h-64C93h
Name:	PHY_CTL_FAMILY_DDI
ShortName:	PHY_CTL_FAMILY_DDI
Power:	PG0
Reset:	global

This register is on the ungated clock and the chip reset, not the FLR.
Writes to this register will not trigger PSR exit.

DWord	Bit	Description
0	31	**Common Reset** This field controls the reset_b (active low reset) which enables the PHY. Value: 0b = Disable; 1b = Enable
	30	**Powergood** Access: RO This field indicates that the PHY is powered up. Value: 0b = Not good; 1b = Good
	29	**Spare 29**
	28	**Spare 28**
	27	**Spare 27**
	26	**Spare 26**
	25	**Spare 25**

PHY_CTL_FAMILY		
	24	**Spare 24**
	23	**Spare 23**
	22	**Spare 22**
	21	**Spare 21**
	20	**Spare 20**
	19	**Spare 19**
	18	**Spare 18**
	17	**Spare 17**
	16	**Spare 16**
	15	**Spare 15**
	14	**Spare 14**
	13	**Spare 13**
	12	**Spare 12**
	11	**Spare 11**
	10	**Spare 10**
	9	**Spare 9**
	8	**Spare 8**
	7	**Spare 7**
	6	**Spare 6**
	5:4	**Reserved**
	3:0	**Reserved**

PIPE_SCANLINE

PIPE_SCANLINE

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32

This register enables the read back of the pipe vertical line counter.
The value increments at the leading edge of HSYNC.
The value resets to line zero at the first active line of the display.
In interlaced display timings, the scan line counter provides the current line in the field. One field can have a total number of lines that is one greater than the other field.

Restriction

Restriction : Not supported with MIPI DSI.

DWord	Bit	Description
0	31	**Current Field** This is an indication of the current display field.

Value	Name	Description
0b	Odd	First field (odd field)
1b	Even	Second field (even field)

DWord	Bit	Description
	30:13	**Reserved**
	12:0	**Line Counter for Display** This is an indication of the current display scan line.

Programming Notes

The line count value is from the display output timing generator, representing the scan line currently being output to a receiver.
Due to buffering within the display engine, the line being fetched (read) from the frame buffer is not directly linked to the line being output. It is possible for the fetched line to be hundreds of lines ahead of the timing generator output line.

PIPE_SCANLINECOMP

PIPE_SCANLINECOMP

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32

This register is used to initiate a display scan line compare. This MMIO driven scan line compare can not be used at the same time as the command streamer driven scan line compare on the same pipe. When this register is written with the Initiate Compare bit set to 1b, the Display Engine (DE) will start comparing the display pipe or plane (selectable) current scan line value (current scan line) with the start scan line value (current scan line >= start scan line) and the end scan line value (current scan line <= end scan line) to decide if the pipe scan line is inside or outside the scan line window of interest. DE will wait until the current scan line is either outside (Inclusive mode) or inside (Exclusive mode) the scan line window, then trigger a scan line event and stop any further comparing. The scan line event can cause display to send a scan line compare response to the command streamer, (used for releasing a MI_WAIT_FOR_EVENT on scan line window), if unmasked in the DERRMR mask register 0x44050. The scan line event can also cause display to generate a scan line compare interrupt, if the interrupt registers are configured for that. The value programmed should be the desired value - 1, so for scan line 0, the value programmed is vertical total, and for scan line 1, the value programmed is 0. The programmable range can include the vertical blank. In interlaced display timings, the current scan line is the current line of the current interlaced field. Either MMIO or a MI_LOAD_REGISTER_IMM command can be used to unmask the scan line render response 0x44050. That can be done anytime before programming this register. There is one instance of this register per pipe.

Restriction
Restriction : A new scan line compare must not be started until after the previous compare has finished. The end scan line value must be greater than or equal to the start scan line value. When using LRI care must be taken to follow all the programming rules for LRI targetting the display engine.
Restriction : Not supported with MIPI DSI.

DWord	Bit	Description
0	31	**Initiate Compare** This field initiates the scan line compare. When this register is written with this bit set to 1b, the display engine will do one complete comparison cycle, trigger a scan line event, then stop comparing. **Value** / **Name** 0b — Do nothing 1b — Initiate compare **Restriction** Restriction : Do not write this register again until after any previous scan line compare has completed.

PIPE_SCANLINECOMP

30	**Inclusive Exclusive Select** This field selects whether the scan line compare is done in inclusive mode, where display triggers the scan line event when outside the scan line window, or inclusive mode, where display triggers when inside the window. **Value** / **Name** / **Description** 0b / Exclusive / Exclusive mode: trigger scan line event when inside the scan line window 1b / Inclusive / Inclusive mode: trigger scan line event when outside the scan line window
29	**Counter Select** This field selects whether the scan line compare is done using the pipe timing generator scanline counter or a plane scanline counter. The pipe timing generator counts the scanlines being output from display. The plane counts the scan lines being fetched from the frame buffer. **Value** / **Name** / **Description** 0b / Timing generator / Use the scanline count from the pipe timing generator 1b / Plane 1 / Use the scanline count from plane 1 **Programming Notes** Due to buffering within the display engine, the line being fetched from the frame buffer is not directly linked to the line being output. It is possible for the fetched line to be hundreds of lines ahead of the timing generator output line. The plane scan line count more closely represents what data is currently being fetched by the plane.
28:16	**Start Scan Line** This field specifies the starting scan line number of the scan line window.
15	**Render Response Destination** This bit indicates what destination to send the scan line event render response to. **Value** / **Name** / **Description** 0b / CS / Send scan line event response to CS 1b / BCS / Send scan line event response to BCS
14:13	**Reserved**
12:0	**End Scan Line** This field specifies the ending scan line number of the scan line window.

PLANE_AUX_DIST

PLANE_AUX_DIST

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to PLANE_SURF or plane not enabled

This register is used to specify the distance from the main surface base address and the stride of the auxiliary surface.
Unlike the surface base address, this register value cannot be updated through flips.

DWord	Bit	Description
0	31:12	**Auxiliary Surface Distance** **Description** This offset specifies the distance (in multiple of 4K bytes) of the Auxiliary surface from the main surface. When using YUV planar formats this field represents the distance of UV surface. When using compressed surface this field represents the distance of control surface. In the graphics address space, the auxiliary surface should always be allocated after the main surface, and the programmed auxiliary surface distance must not be negative. **Restriction** It must be 4K page aligned.Allocate an extra 136 Page Table Entries (PTEs) beyond the end of the displayed surface. If 180 or 270 plane rotation capability is required, allocate an exra 136 PTEs before the begining of the surface. When address range limits are reached, wrap around to finish allocating the extra PTEs. Only the PTEs will be used, not the pages themselves. The end of the surface cannot be within 136 PTEs of the end of the graphics memory.
	11:10	**Reserved**
	9:0	**Auxiliary Surface Stride** **Description** This field specifies the stride of the auxiliary surface. Refer to PLANE_STRIDE register for stride programming details. When using YUV planar formats this field represents the stride of UV surface. When using compressed surface this field represents the stride of the control surface. Restriction : When using render compressed surfaces, the programmed auxiliary surface stride should not exceed 8 (8 * 128 = 1024 bytes).

PLANE_KEYMAX

PLANE_KEYMAX	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank, pipe not enabled, or plane not enabled

When plane source is YUV, this register specifies the maximum YUV key value to be used together with the minimum YUV key value and the channel enables to determine if the plane matches the key.
When plane source is RGB, this register is not used.

DWord	Bit	Description
0	31:24	**Plane Alpha Value** Specifies the plane alpha value when plane alpha is enabled in PLANE_KEYMSK register.
	23:16	**V Key Max Value** Specifies the maximum key value for the V channel.
	15:8	**Y Key Max Value** Specifies the maximum key value for the Y channel.
	7:0	**U Key Max Value** Specifies the maximum key value for the U channel.

PLANE_KEYMSK

PLANE_KEYMSK

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank, pipe not enabled, or plane not enabled

DWord	Bit	Description
0	31	**Plane Alpha Enable** Description: Enables the plane alpha. Color channels will be pre-multiplied by hardware with the plane alpha value from PLANE_KEYMAX register. Per-pixel alpha is defined in the PLANE_CTL register. Value 0b: Disable Value 1b: Enable
	30:27	**Reserved** Format: MBZ
	26	**V or R Key Channel Enable** Enables the V/Red channel for key comparison. A disabled channel will be ignored when determining a key match. Value 0b: Disable Value 1b: Enable
	25	**Y or G Key Channel Enable** Enables the Y/Green channel for key comparison. A disabled channel will be ignored when determining a key match. Value 0b: Disable Value 1b: Enable
	24	**U or B Key Channel Enable** Enables the U/Blue channel for key comparison. A disabled channel will be ignored when determining a key match. Value 0b: Disable Value 1b: Enable

PLANE_KEYMSK		
	23:16	**R Key Mask Value** Specifies the key mask for the Red channel. A zero bit in the mask indicates that the corresponding bit will be ignored when determining a key match.
	15:8	**G Key Mask Value** Specifies the key mask for the Green channel. A zero bit in the mask indicates that the corresponding bit will be ignored when determining a key match.
	7:0	**B Key Mask Value** Specifies the key mask for the Blue channel. A zero bit in the mask indicates that the corresponding bit will be ignored when determining a key match.

PLANE_KEYVAL

PLANE_KEYVAL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank, pipe not enabled, or plane not enabled

When plane source is YUV, this register specifies the minimum YUV key value to be used together with the maximum YUV key value and the channel enables to determine if the plane matches the key. When plane source is RGB, this register specifies the RGB key value to be used together with the channel masks to determine if the plane matches the key. RGB key matches can only occur for positive pixel values in the 0 to 1 range. Extended range pixel values will not match. MSB bits are used for comparison.

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:16	**V Min or R Key Value** Specifies the minimum key value for the V channel or the compare value for Red channel.
	15:8	**Y Min or G Key Value** Specifies the minimum key value for the Y channel or the compare value for Green channel.
	7:0	**U Min or B Key Value** Specifies the minimum key value for the U channel or the compare value for Blue channel.

PLANE_LEFT_SURF

PLANE_LEFT_SURF

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of left or right eye vertical blank (selectable), pipe not enabled. or plane not enabled; after armed
Double Buffer Armed By:	Write to PLANE_SURF or plane not enabled

Restriction
Restriction : This register must be programmed with a valid address prior to enabling stereo 3D on this pipe.

DWord	Bit	Description
0	31:12	**Left Surface Base Address** Format: GraphicsAddress[31:12] This address specifies the stereo 3D left eye surface base address bits 31:12. **Restriction** Restriction : This surface must have the same stride, tiling, and panning offset parameters as the right eye surface and meet all the same restrictions.
	11:0	**Reserved**

PLANE_OFFSET

PLANE_OFFSET

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank, pipe not enabled, or plane not enabled

This register specifies the panning for the plane surface. The start position is specified in this register as a (x, y) offset from the beginning of the surface. When performing 180 rotation, hardware will internally add the plane size to the offsets so the plane will start displaying from the bottom right corner of the image. When performing 90 rotation, the offset programmed should take the rotation in to consideration. X offset = (Surface height in tiles * tile height) - Y offset - Y Size, Y offset = X offset When performing 270 rotation, use the same programming as 90 rotation. For YUV planar format non-rotate cases, the UV surface offsets should be half of the Y surface offsets when the UV surface is tile row aligned. When the UV surface is not tile row aligned, the UV surface Y offset should also include the lines from the previous nearest tile row aligned address.

Restriction

Restriction : The plane size + offset must not exceed the maximum supported plane size.

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28:16	**Start Y Position** The Start Y Position or the Y Offset is the vertical offset in lines of the beginning of the active display plane relative to the display surface. **Restriction** Restriction : In 90/270 rotation modes, this offset must be even lines aligned for YUV 4:2:2, YUV 4:2:0 formats.
	15:13	**Reserved** Format: MBZ
	12:0	**Start X Position** The Start X Position or the X Offset is the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. **Restriction** Restriction : In 0/180 rotation modes, this offset must be even pixel aligned for YUV 4:2:2, YUV 4:2:0 formats.

PLANE_POS

PLANE_POS

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to PLANE_SURF or plane not enabled

This register specifies the screen position of the plane.
The origin of the plane position is always the upper left corner of the display pipe source image area.
When plane scaling is not enabled on this plane, this is the position of the plane when blended with other planes on this pipe.
When plane scaling is enabled on this plane, the scaler window position is the position of the plane when blended with other planes on this pipe.
When performing rotation, the plane image is rotated by hardware, but the position is not, so it must be adjusted if it is desired to maintain the same apparent position on a physically rotated display.

Restriction

Restriction : When plane scaling is not enabled on this plane, the plane must be completely contained within the pipe source area. Pipe source size >= plane position + plane size.
When plane scaling is enabled on this plane, the X and Y positions must be programmed to 0.

DWord	Bit	Description
0	31:28	**Reserved** Format: MBZ
	27:16	**Y Position** This specifies the vertical position of the plane upper left corner in lines.
	15:13	**Reserved** Format: MBZ
	12:0	**X Position** This specifies the horizontal position of the plane upper left corner in pixels.

PLANE_SIZE

PLANE_SIZE

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to PLANE_SURF or plane not enabled

This register specifies the plane source size, the size of the image fetched from the frame buffer.
When plane scaling is not enabled on this plane, this is the size of the plane when blended with other planes on this pipe.
When plane scaling is enabled on this plane, the scaler window size is the size of the plane when blended with other planes on this pipe.

Restriction

Restriction : When plane scaling is not enabled on this plane, the plane must be completely contained within the pipe source area. Pipe source size >= plane position + plane size.

DWord	Bit	Description
0	31:28	**Reserved** Format: MBZ
	27:16	**Height** This specifies the height of the plane in lines. The value in the register is the height minus one. **Restriction** Restriction : The height must be at least one line. The height is limited to maximum of 4096 lines. When plane scaling is enabled, the height must be atleast 8 lines.
	15:13	**Reserved** Format: MBZ
	12:0	**Width** This specifies the width of the plane in pixels. The value in the register is the width minus one. **Restriction** Restriction : The width must be even (programmed value odd) when YUV 4:2:2 or YUV 4:2:0 source pixel format is used. The width must be at least one pixel. The width should be less than or equal to the stride in pixels.

PLANE_SIZE

Tiling format	Bytes per pixel	Max Width supported in pixels (with no horizontal panning)
Linear, X Tiling	1,2,4,8	4096
Y Tiling	8	2048
	1,2,4	4096
Yf Tiling	8	Not supported
	1,2,4	4096

PLANE_STRIDE

PLANE_STRIDE

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to PLANE_SURF or plane not enabled

DWord	Bit	Description
0	31:10	**Reserved**
	9:0	**Stride** This field specifies the stride for the plane. The field is used to determine the line to line increment for the plane. For Linear memory, this field specifies the stride in chunks of 64 bytes (1 cache line). If the programmed value is 100, the actual stride = 100 * 64 = 6400 bytes. For X-Tiled & Y-Tiled memory, this field specifies the stride in number of tiles. For Tile X, if the programmed value is 10, the actual stride = 10 * 512 (X tile width) = 5120 bytes. For Tile Y legacy, if the programmed value is 10, the actual stride = 10 * 128 (Y tile width) = 1280 bytes. This register may be updated through MMIO writes or through command streamer initiated synchronous flips.

Tile Format	Width in bytes
Tile X	512
Tile Y (legacy)	128
Tile YF (8 bpp)	64
Tile YF (16 bpp, 32 bpp, 64 bpp)	128

Programming Notes
For YUV planar (NV12 or P0xx) source fomats, the Auxiliary surface (UV surface) stride should be programmed seperately in the PLANE_AUX_DIST register.

Restriction
Restriction : For YUV planar (NV12 or P0xx) plane pixel formats, the stride calculated in bytes should be equal for the Y and UV surfaces. In Tile Yf format, the stride value programmed for YUV planar - Y surface should be an even number of tiles in the non-rotate mode. The stride in bytes must not exceed the of the size of 8K pixels and 32K bytes

PLANE_STRIDE

Tile Format	Pixel Format	Maximum Stride	YUV Planar Maximum Auxiliary surface stride in tiles	Render Decompression Maximum Auxiliary surface stride in tiles
Linear Stride in cache-lines	64 bpp pixel format	512	NA	NA
	32 bpp pixel format	512	NA	NA
	16 bpp pixel format	256	NA	NA
	8 bpp pixel format	128	128	NA
X Tiling Stride in tiles	64 bpp pixel format	64	NA	NA
	32 bpp pixel format	64	NA	NA
	16 bpp pixel format	32	NA	NA
	8 bpp pixel format	16	16	NA
Y Tiling (Legacy) Stride in tiles	64 bpp pixel format	256	NA	NA
	32 bpp pixel format	256	NA	8
	16 bpp pixel format	128	NA	NA
	8 bpp pixel format	64	64	NA
YF Tiling Stride in	32 bpp pixel	256	NA	8

PLANE_STRIDE					
		tiles	format		
			16 bpp Pixel format	128	NA	NA
			8 bpp pixel format	128	64	NA

PLANE_SURF

PLANE_SURF

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of left or right eye vertical blank (selectable), pipe not enabled, or plane not enabled

Writes to this register arm primary registers for this pipe. A write to this register is considered a flip and can cause a flip done interrupt if the interrupt registers are configured for that. The values in this register may be updated through MMIO writes or through command streamer initiated flips. Synchronous updates (synchronous command streamer flips or synchronous MMIO writes) will update the plane surface values at the start of the next vertical blank. Asynchronous updates (asynchronous command streamer flips or asynchronous MMIO writes) will update the plane surface values at the next TLB request or at the start of the next vertical blank. Stereo 3D synchronous updates (stereo 3D command streamer flips or synchronous MMIO writes while stereo 3D is enabled) will update at the start of either the left or right eye vertical blank, selectable by the plane control register stereo surface vblank mask.

Asynchronous flip completion time depends greatly on how much data has been prefetched for power savings, and can take up to 1 full frame to complete. For faster flip completion, disable FBC and render compression and allocate a small amount of data buffer for the plane.

DWord	Bit	Description
0	31:12	**Surface Base Address** Format: GraphicsAddress[31:12] This address specifies the surface base address bits 31:12. In stereo 3D mode this is the right eye base address. In non-stereo 3D mode this is the only base address. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. **Restriction** The surface base address must be at least 256KB aligned in the Linear or X-tiling modes and must be at least 1MB aligned in the Y-tiling mode. Allocate an extra 136 Page Table Entries (PTEs) beyond the end of the displayed surface. If 180 or 270 plane rotation capability is required, allocate an exra 136 PTEs before the begining of the surface. When address range limits are reached, wrap around to finish allocating the extra PTEs. Only the PTEs will be used, not the pages themselves. For render compression, the padding must be added for both the main surface and the compression control surface. There must be padding between the main and the control surfaces. For planar YUV 420 formats, the padding must be added for both Y and UV surfaces.There must be padding between the Y and UV surfaces.
	11	**Reserved**
	10	**Reserved**

PLANE_SURF		
	9	**Reserved**
	8:7	**Reserved**
	6:4	**Reserved**
	3	**Ring Flip Source** This bit indicates if the source of the last ring flip was CS or BCS. This will determine where the flip done response is sent. **Value** / **Name** 0b / CS 1b / BCS
	2	**Reserved**
	1:0	**Reserved**

PLANE_SURFLIVE

PLANE_SURFLIVE		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
There is one instance of this register for each plane.		
DWord	**Bit**	**Description**
0	31:12	**Live Surface Base Address** Access: RO This gives the live value of the surface base address as being currently used for the plane.
	11	**Reserved** Format: MBZ
	10:9	**Reserved**
	8:6	**Reserved**
	5	**Reserved**
	4	**Reserved**
	3:0	**Reserved** Format: MBZ

PLANE_WM

PLANE_WM	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00004007
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank, plane not enabled, or pipe not enabled
Double Buffer Armed By:	Write to PLANE_SURF or plane not enabled
Address:	70140h-7015Fh
Name:	Cursor A Watermarks
ShortName:	CUR_WM_A_*
Power:	PG1
Reset:	soft
Address:	71140h-7115Fh
Name:	Cursor B Watermarks
ShortName:	CUR_WM_B_*
Power:	PG2
Reset:	soft
Address:	72140h-7215Fh
Name:	Cursor C Watermarks
ShortName:	CUR_WM_C_*
Power:	PG2
Reset:	soft
Address:	70240h-7025Fh
Name:	Plane 1 A Watermarks
ShortName:	PLANE_WM_1_A_*
Power:	PG1
Reset:	soft
Address:	70340h-7035Fh
Name:	Plane 2 A Watermarks
ShortName:	PLANE_WM_2_A_*
Power:	PG1
Reset:	soft

PLANE_WM	
Address:	70440h-7045Fh
Name:	Plane 3 A Watermarks
ShortName:	PLANE_WM_3_A_*
Power:	PG1
Reset:	soft
Address:	70540h-7055Fh
Name:	Plane 4 A Watermarks
ShortName:	PLANE_WM_4_A_*
Power:	PG1
Reset:	soft
Address:	71240h-7125Fh
Name:	Plane 1 B Watermarks
ShortName:	PLANE_WM_1_B_*
Power:	PG2
Reset:	soft
Address:	71340h-7135Fh
Name:	Plane 2 B Watermarks
ShortName:	PLANE_WM_2_B_*
Power:	PG2
Reset:	soft
Address:	71440h-7145Fh
Name:	Plane 3 B Watermarks
ShortName:	PLANE_WM_3_B_*
Power:	PG2
Reset:	soft
Address:	71540h-7155Fh
Name:	Plane 4 B Watermarks
ShortName:	PLANE_WM_4_B_*
Power:	PG2
Reset:	soft
Address:	72240h-7225Fh
Name:	Plane 1 C Watermarks
ShortName:	PLANE_WM_1_C_*
Power:	PG2
Reset:	soft

PLANE_WM

Address:	72340h-7235Fh
Name:	Plane 2 C Watermarks
ShortName:	PLANE_WM_2_C_*
Power:	PG2
Reset:	soft

Address:	72440h-7245Fh
Name:	Plane 3 C Watermarks
ShortName:	PLANE_WM_3_C_*
Power:	PG2
Reset:	soft

Programming Notes

There are eight regular watermarks and a transition watermark per plane/cursor. For YUV planar source formats, only the Y surface watermark value should be programmed. Watermark programming instructions are documented separately.

Restriction

Restriction : For minimum watermark requirements refer to Display Watermark Programming section.

DWord	Bit	Description
0	31	**Enable** This field enables this watermark. All the watermarks at this level for all enabled planes must be enabled before the level will be used. Value: 1b — Name: Enable Value: 0b — Name: Disable
	30	**Reserved**
	29:19	**Reserved** Format: MBZ
	18:14	**Lines** Default Value: 01h **Description** This field contains the watermark value in lines. Hardware ignores the lines for the the transition watermark. Hardware ignores the lines for the level 0 watermark.
	13:10	**Reserved**

PLANE_WM		
	9:0	**Blocks** Default Value: 007h This field contains the watermark value in blocks of 8 cachelines.

PORT_CL1CM_DW0

PORT_CL1CM_DW0	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000707
Access:	R/W
Size (in bits):	32
Address:	162000h-162003h
Name:	PORT_CL1CM_DW0_A
ShortName:	PORT_CL1CM_DW0_A
Power:	PG0
Reset:	global
Address:	6C000h-6C003h
Name:	PORT_CL1CM_DW0_BC
ShortName:	PORT_CL1CM_DW0_BC
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:20	**Preserve Default 31 20** Default Value: 000000000000b The values in this field must not be changed.
	19	**ialldl_powerdown** Access: RO status bit to indicate all data lanes are powered down
	18	**ianydl_powerdown** Access: RO status bit to indicate any data lane is powered down
	17	**iphypwrgack** Access: RO PHY power ack status
	16	**iphypwrgood** Access: RO PHY power good status

PORT_CL1CM_DW0		
	15:0	**Preserve Default 15 0** Default Value: 0000011100000111b The values in this field must not be changed. **Programming Notes** Bit 7 is reserved and defaults to 0, but the DDI PHY Initialization sequence specifies a read to it as part of determining when this register is accessible.

PORT_CL1CM_DW9

PORT_CL1CM_DW9	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x80800080
Access:	R/W
Size (in bits):	32
Address:	162024h-162027h
Name:	PORT_CL1CM_DW9_A
ShortName:	PORT_CL1CM_DW9_A
Power:	PG0
Reset:	global
Address:	6C024h-6C027h
Name:	PORT_CL1CM_DW9_BC
ShortName:	PORT_CL1CM_DW9_BC
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:16	**Preserve Default 31 16** Default Value: 1000000010000000b The values in this field must not be changed.
	15:8	**iref0rcoffset**
	7:0	**Preserve Default 7 0** Default Value: 10000000b The values in this field must not be changed.

PORT_CL1CM_DW10

PORT_CL1CM_DW10	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x80800080
Access:	R/W
Size (in bits):	32
Address:	162028h-16202Bh
Name:	PORT_CL1CM_DW10_A
ShortName:	PORT_CL1CM_DW10_A
Power:	PG0
Reset:	global
Address:	6C028h-6C02Bh
Name:	PORT_CL1CM_DW10_BC
ShortName:	PORT_CL1CM_DW10_BC
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:16	**Preserve Default 31 16** Default Value: 1000000010000000b The values in this field must not be changed.
	15:8	**iref1rcoffset**
	7:0	**Preserve Default 7 0** Default Value: 10000000b The values in this field must not be changed.

PORT_CL1CM_DW28

PORT_CL1CM_DW28	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x330B0040
Access:	R/W
Size (in bits):	32
Address:	162070h-162073h
Name:	PORT_CL1CM_DW28_A
ShortName:	PORT_CL1CM_DW28_A
Power:	PG0
Reset:	global
Address:	6C070h-6C073h
Name:	PORT_CL1CM_DW28_BC
ShortName:	PORT_CL1CM_DW28_BC
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:24	**Preserve Default 31 24** Default Value: 00110011b The values in this field must not be changed.
	23	**ocl1powerdownen** Dynamic Power Down Enable for Channel 0
	22	**oldo_dynpwrdownen**
	21:7	**Preserve Default 21 7** Default Value: 001011000000000b The values in this field must not be changed.
	6:2	**susclkdisable_delay** Default Value: 10000b 16 Cycle Delay This register will control the number of cycles to delay the susclk enable de-assertion, in addition to the de-assertion of the CLKREQ signal sent to the SOC. The criclk enable must be continuously de-asserted for the duration of this delay in order for the de-asserted state to be captured by the clock gating controller. 5'b00000 – 0 Cycle Delay 5'b00001 – 1 Cycle Delay 5'b00010 – 2 Cycle Delay .....

PORT_CL1CM_DW28		
		5'b11110 – 30 Cycle Delay 5'b11111 – 31 Cycle Delay
	1:0	**sus_clk_config**

PORT_CL1CM_DW30

PORT_CL1CM_DW30	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x3E000010
Access:	RO
Size (in bits):	32
Address:	162078h-16207Bh
Name:	PORT_CL1CM_DW30_A
ShortName:	PORT_CL1CM_DW30_A
Power:	PG0
Reset:	global
Address:	6C078h-6C07Bh
Name:	PORT_CL1CM_DW30_BC
ShortName:	PORT_CL1CM_DW30_BC
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:7	**Preserve Default 31 7** Default Value: 00111110000000000000000b The values in this field must not be changed.
	6	**ocl2_ldofuse_pwrenb**
	5:0	**Preserve Default 5 0** Default Value: 010000b The values in this field must not be changed.

PORT_CL2CM_DW6

PORT_CL2CM_DW6	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6C358h-6C35Bh
Name:	PORT_CL2CM_DW6_BC
ShortName:	PORT_CL2CM_DW6_BC
Power:	PG0
Reset:	global

PHY CL2 Common Dword 6
Instances per PHY dual/single
DDIB/C: PHY dual, base 0x6C000
CL2 common config base 0x340

DWord	Bit	Description
0	31:29	**Reserved** Format: PBC The values in this field must not be changed. Use read/modify/write to update this register.
	28	**oldo_dynpwrdownen** Dynamic Power Down Enable for Channel 1
	27:0	**Reserved** Format: PBC The values in this field must not be changed. Use read/modify/write to update this register.

PORT_PCS_DW10

PORT_PCS_DW10	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	162428h-16242Bh
Name:	PORT_PCS_DW10_LN01_A
ShortName:	PORT_PCS_DW10_LN01_A
Power:	PG0
Reset:	global
Address:	162628h-16262Bh
Name:	PORT_PCS_DW10_LN23_A
ShortName:	PORT_PCS_DW10_LN23_A
Power:	PG0
Reset:	global
Address:	162C28h-162C2Bh
Name:	PORT_PCS_DW10_GRP_A
ShortName:	PORT_PCS_DW10_GRP_A
Power:	PG0
Reset:	global
Address:	6C428h-6C42Bh
Name:	PORT_PCS_DW10_LN01_B
ShortName:	PORT_PCS_DW10_LN01_B
Power:	PG0
Reset:	global
Address:	6C628h-6C62Bh
Name:	PORT_PCS_DW10_LN23_B
ShortName:	PORT_PCS_DW10_LN23_B
Power:	PG0
Reset:	global
Address:	6CC28h-6CC2Bh
Name:	PORT_PCS_DW10_GRP_B
ShortName:	PORT_PCS_DW10_GRP_B
Power:	PG0

PORT_PCS_DW10

Reset:	global
Address:	6C828h-6C82Bh
Name:	PORT_PCS_DW10_LN01_C
ShortName:	PORT_PCS_DW10_LN01_C
Power:	PG0
Reset:	global
Address:	6CA28h-6CA2Bh
Name:	PORT_PCS_DW10_LN23_C
ShortName:	PORT_PCS_DW10_LN23_C
Power:	PG0
Reset:	global
Address:	6CE28h-6CE2Bh
Name:	PORT_PCS_DW10_GRP_C
ShortName:	PORT_PCS_DW10_GRP_C
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31	**reg_tx2swingcalcinit**
	30	**reg_tx1swingcalcinit**
	29:26	**Reserved** Format: MBZ
	25	**reg_tx1deemp**
	24	**reg_tx2deemp**
	23:0	**Reserved** Format: MBZ

PORT_PCS_DW12

PORT_PCS_DW12	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	162430h-162433h
Name:	PORT_PCS_DW12_LN01_A
ShortName:	PORT_PCS_DW12_LN01_A
Power:	PG0
Reset:	global
Address:	162630h-162633h
Name:	PORT_PCS_DW12_LN23_A
ShortName:	PORT_PCS_DW12_LN23_A
Power:	PG0
Reset:	global
Address:	162C30h-162C33h
Name:	PORT_PCS_DW12_GRP_A
ShortName:	PORT_PCS_DW12_GRP_A
Power:	PG0
Reset:	global
Address:	6C430h-6C433h
Name:	PORT_PCS_DW12_LN01_B
ShortName:	PORT_PCS_DW12_LN01_B
Power:	PG0
Reset:	global
Address:	6C630h-6C633h
Name:	PORT_PCS_DW12_LN23_B
ShortName:	PORT_PCS_DW12_LN23_B
Power:	PG0
Reset:	global
Address:	6CC30h-6CC33h
Name:	PORT_PCS_DW12_GRP_B
ShortName:	PORT_PCS_DW12_GRP_B
Power:	PG0

PORT_PCS_DW12

Reset:	global
Address:	6C830h-6C833h
Name:	PORT_PCS_DW12_LN01_C
ShortName:	PORT_PCS_DW12_LN01_C
Power:	PG0
Reset:	global
Address:	6CA30h-6CA33h
Name:	PORT_PCS_DW12_LN23_C
ShortName:	PORT_PCS_DW12_LN23_C
Power:	PG0
Reset:	global
Address:	6CE30h-6CE33h
Name:	PORT_PCS_DW12_GRP_C
ShortName:	PORT_PCS_DW12_GRP_C
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:23	**Reserved** Format: MBZ
	22:20	**reg_tx2_stagger_mult** These bits set the lane staggering multiplier for the transmitter based on the linkclk period. 000b: 0x 001b: 1x 010b: 2x 011b: 4x 100b: 8x 101b: 16x 110b: 32x 111b: 64x
	19	**reg_lanestagger_by_group**
	18:16	**reg_tx1_stagger_mult** These bits set the lane staggering multiplier for the transmitter based on the linkclk period. 000b: 0x 001b: 1x

PORT_PCS_DW12

		010b: 2x 011b: 4x 100b: 8x 101b: 16x 110b: 32x 111b: 64x
	15:7	**Reserved** Format: MBZ
	6	**reg_lanestagger_strap_ovrd**
	5	**Reserved** Format: MBZ
	4:0	**reg_lanestagger_strap**

Value	Name	Description
02h	2	Symbol rate 25 to 33 MHz
04h	4	Symbol rate 34 to 67 MHz
07h	7	Symbol rate 68 to 135 MHz
0Dh	13	Symbol rate 136 to 270 MHz
18h	24	Symbol rate 271 to 540 MHz

PORT_PLL_0

PORT_PLL_0	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000001B
Access:	R/W
Size (in bits):	32
Address:	162100h-162103h
Name:	PORT_PLL_0_A
ShortName:	PORT_PLL_0_A
Power:	PG0
Reset:	global
Address:	6C100h-6C103h
Name:	PORT_PLL_0_B
ShortName:	PORT_PLL_0_B
Power:	PG0
Reset:	global
Address:	6C380h-6C383h
Name:	PORT_PLL_0_C
ShortName:	PORT_PLL_0_C
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:8	**Reserved**
	7:0	**i_fbdivratio** Default Value: 00011011b m2 divider. Second stage of feedback divider

PORT_PLL_1

PORT_PLL_1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000100
Access:	R/W
Size (in bits):	32
Address:	162104h-162107h
Name:	PORT_PLL_1_A
ShortName:	PORT_PLL_1_A
Power:	PG0
Reset:	global
Address:	6C104h-6C107h
Name:	PORT_PLL_1_B
ShortName:	PORT_PLL_1_B
Power:	PG0
Reset:	global
Address:	6C384h-6C387h
Name:	PORT_PLL_1_C
ShortName:	PORT_PLL_1_C
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:18	**Reserved** Format: MBZ
	17	**i_divretimeren**
	16	**i_fbdivdutycycsel**
	15:12	**Reserved** Format: MBZ
	11:8	**i_ndivratio** Default Value: 0001b
	7:3	**Reserved** Format: MBZ
	2:0	**i_fbpredivratio**

PORT_PLL_2

PORT_PLL_2	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	162108h-16210Bh
Name:	PORT_PLL_2_A
ShortName:	PORT_PLL_2_A
Power:	PG0
Reset:	global
Address:	6C108h-6C10Bh
Name:	PORT_PLL_2_B
ShortName:	PORT_PLL_2_B
Power:	PG0
Reset:	global
Address:	6C388h-6C38Bh
Name:	PORT_PLL_2_C
ShortName:	PORT_PLL_2_C
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:22	**Reserved** Format: MBZ
	21:0	**i_fracdiv** Fractional divider

PORT_PLL_3

PORT_PLL_3			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000002		
Access:	R/W		
Size (in bits):	32		
Address:	16210Ch-16210Fh		
Name:	PORT_PLL_3_A		
ShortName:	PORT_PLL_3_A		
Power:	PG0		
Reset:	global		
Address:	6C10Ch-6C10Fh		
Name:	PORT_PLL_3_B		
ShortName:	PORT_PLL_3_B		
Power:	PG0		
Reset:	global		
Address:	6C38Ch-6C38Fh		
Name:	PORT_PLL_3_C		
ShortName:	PORT_PLL_3_C		
Power:	PG0		
Reset:	global		

DWord	Bit	Description
0	31:17	**Reserved** Format: MBZ
	16	**i_fracnen_h** Fractional Modulator Enable
	15:9	**Reserved** Format: MBZ
	8	**i_fracmodorder**
	7:4	**Reserved** Format: MBZ
	3:0	**i_feedfwrdgain** Default Value: 0010b

PORT_PLL_4

PORT_PLL_4			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Address:	162110h-162113h		
Name:	PORT_PLL_4_A		
ShortName:	PORT_PLL_4_A		
Power:	PG0		
Reset:	global		
Address:	6C110h-6C113h		
Name:	PORT_PLL_4_B		
ShortName:	PORT_PLL_4_B		
Power:	PG0		
Reset:	global		
Address:	6C390h-6C393h		
Name:	PORT_PLL_4_C		
ShortName:	PORT_PLL_4_C		
Power:	PG0		
Reset:	global		
DWord	**Bit**	**Description**	
0	31:0	**Reserved**	
		Format:	MBZ

PORT_PLL_6

PORT_PLL_6	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00010803
Access:	R/W
Size (in bits):	32
Address:	162118h-16211Bh
Name:	PORT_PLL_6_A
ShortName:	PORT_PLL_6_A
Power:	PG0
Reset:	global
Address:	6C118h-6C11Bh
Name:	PORT_PLL_6_B
ShortName:	PORT_PLL_6_B
Power:	PG0
Reset:	global
Address:	6C398h-6C39Bh
Name:	PORT_PLL_6_C
ShortName:	PORT_PLL_6_C
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:19	**Reserved** Format: MBZ
	18:16	**i_gainctrl** Default Value: 001b Gain for loop filter
	15:13	**Reserved** Format: MBZ
	12:8	**i_int_coeff** Default Value: 01000b integral coefficient = 2^(-int_coeff), targeting up to 2^-16
	7:4	**Reserved** Format: MBZ

PORT_PLL_6		
	3:0	**i_prop_coeff** Default Value: 0011b proportional coefficient = 2^(-prop_coeff)

PORT_PLL_8

PORT_PLL_8	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0007000D
Access:	R/W
Size (in bits):	32
Address:	162120h-162123h
Name:	PORT_PLL_8_A
ShortName:	PORT_PLL_8_A
Power:	PG0
Reset:	global
Address:	6C120h-6C123h
Name:	PORT_PLL_8_B
ShortName:	PORT_PLL_8_B
Power:	PG0
Reset:	global
Address:	6C3A0h-6C3A3h
Name:	PORT_PLL_8_C
ShortName:	PORT_PLL_8_C
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:19	**Reserved** Format: MBZ
	18	**i_tdccalsetupdeten_h** Default Value: 1b **Programming Notes** Display software must not change this field.
	17:16	**i_tdcsel** Default Value: 11b **Programming Notes** Display software must not change this field.
	15:10	**Reserved**

PORT_PLL_8			
		Format:	MBZ
	9:0	**i_tdctargetcnt**	
		Default Value:	0000001101b
		TDC Target Count	

PORT_PLL_9

PORT_PLL_9	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00040305
Access:	R/W
Size (in bits):	32
Address:	162124h-162127h
Name:	PORT_PLL_9_A
ShortName:	PORT_PLL_9_A
Power:	PG0
Reset:	global
Address:	6C124h-6C127h
Name:	PORT_PLL_9_B
ShortName:	PORT_PLL_9_B
Power:	PG0
Reset:	global
Address:	6C3A4h-6C3A7h
Name:	PORT_PLL_9_C
ShortName:	PORT_PLL_9_C
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:19	**Reserved** Format: MBZ
	18:16	**i_pllwait_cntr** Default Value: 100b Display software must not change this field.
	15:11	**Reserved** Format: MBZ
	10	**i_useidvdata_h** Display software must not change this field.
	9	**i_dcoditheren_h** Default Value: 1b Display software must not change this field.

PORT_PLL_9		
	8	**i_afccntsel** Default Value: 1b Display software must not change this field.
	7:4	**Reserved** Format: MBZ
	3:1	**i_lockthresh** Default Value: 010b Lock threshold
	0	**i_lockthreshsel** Default Value: 1b Display software must not change this field.

PORT_PLL_10

PORT_PLL_10	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x70000000
Access:	R/W
Size (in bits):	32
Address:	162128h-16212Bh
Name:	PORT_PLL_10_A
ShortName:	PORT_PLL_10_A
Power:	PG0
Reset:	global
Address:	6C128h-6C12Bh
Name:	PORT_PLL_10_B
ShortName:	PORT_PLL_10_B
Power:	PG0
Reset:	global
Address:	6C3A8h-6C3ABh
Name:	PORT_PLL_10_C
ShortName:	PORT_PLL_10_C
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:28	**i_pllpwrmode** Default Value: 0111b Display software must not change this field.
	27	**i_dcoampovrden_h** DCO amplitude override enable
	26	**i_dcocoarse_ovrd_h** Display software must not change this field.
	25:24	**i_dcofinesel** Display software must not change this field.
	23:16	**i_dcocoarse** Display software must not change this field.

PORT_PLL_10		
	15:14	**Reserved** Format: MBZ
	13:10	**i_dcoamp** DCO amplitude override value
	9:0	**i_dcofine** Display software must not change this field.

PORT_PLL_11

PORT_PLL_11			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Address:	16212Ch-16212Fh		
Name:	PORT_PLL_11_A		
ShortName:	PORT_PLL_11_A		
Power:	PG0		
Reset:	global		
Address:	6C12Ch-6C12Fh		
Name:	PORT_PLL_11_B		
ShortName:	PORT_PLL_11_B		
Power:	PG0		
Reset:	global		
Address:	6C3ACh-6C3AFh		
Name:	PORT_PLL_11_C		
ShortName:	PORT_PLL_11_C		
Power:	PG0		
Reset:	global		
DWord	**Bit**	**Description**	
0	31:0	**Reserved**	
		Format:	MBZ

PORT_PLL_12

PORT_PLL_12			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Address:	162130h-162133h		
Name:	PORT_PLL_12_A		
ShortName:	PORT_PLL_12_A		
Power:	PG0		
Reset:	global		
Address:	6C130h-6C133h		
Name:	PORT_PLL_12_B		
ShortName:	PORT_PLL_12_B		
Power:	PG0		
Reset:	global		
Address:	6C3B0h-6C3B3h		
Name:	PORT_PLL_12_C		
ShortName:	PORT_PLL_12_C		
Power:	PG0		
Reset:	global		
DWord	**Bit**	**Description**	
0	31:0	**Reserved**	
		Format:	MBZ

PORT_PLL_EBB_0

PORT_PLL_EBB_0	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	162034h-162037h
Name:	PORT_PLL_EBB_0_A
ShortName:	PORT_PLL_EBB_0_A
Power:	PG0
Reset:	global
Address:	6C034h-6C037h
Name:	PORT_PLL_EBB_0_B
ShortName:	PORT_PLL_EBB_0_B
Power:	PG0
Reset:	global
Address:	6C340h-6C343h
Name:	PORT_PLL_EBB_0_C
ShortName:	PORT_PLL_EBB_0_C
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:13	**o_dtp1divsel** P1-Divider to divide VCO clock from PLL before P2 divider
	12:8	**o_dtp2divsel** P2-Divider to divide VCO clock from PLL after P1 divider
	7:2	**Reserved** Format: MBZ
	1	**i_pllfreqlock** Access: RO Value: 0b — Name: Not lock

PORT_PLL_EBB_0			
		1b	Lock
	0	**i_plllock** Access: RO Value / Name 0b — Not lock 1b — Lock	

PORT_PLL_EBB_4

PORT_PLL_EBB_4	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	162038h-16203Bh
Name:	PORT_PLL_EBB_4_A
ShortName:	PORT_PLL_EBB_4_A
Power:	PG0
Reset:	global
Address:	6C038h-6C03Bh
Name:	PORT_PLL_EBB_4_B
ShortName:	PORT_PLL_EBB_4_B
Power:	PG0
Reset:	global
Address:	6C344h-6C347h
Name:	PORT_PLL_EBB_4_C
ShortName:	PORT_PLL_EBB_4_C
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:15	**Reserved** Format: PBC
	14	**o_dtafcrecal** Access: R/WC AFC Recalibration This bit is required to be set if the N-div, M1div, M2div, or PLL reference clocks are updated. This bit clears when the PLL transitions from the disabled to enabled state. 0b disable 1b enable
	13	**o_dtdclkpen_h** Enable 10 bit clock to display controller. 0b disable

PORT_PLL_EBB_4			
		1b	enable
	12:0	**Reserved**	
		Format:	PBC

PORT_PLL_ENABLE

PORT_PLL_ENABLE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	46074h-46077h
Name:	Port PLL Enable A
ShortName:	PORT_PLL_ENABLE_A
Power:	Always on
Reset:	soft
Address:	46078h-4607Bh
Name:	Port PLL Enable B
ShortName:	PORT_PLL_ENABLE_B
Power:	Always on
Reset:	soft
Address:	4607Ch-4607Fh
Name:	Port PLL Enable C
ShortName:	PORT_PLL_ENABLE_C
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31	**PLL Enable** This field enables or disables the port PLL. Value / Name: 0b – Disable 1b – Enable
	30	**PLL Lock** Access: RO This fields indicates the status of the port PLL Lock. Value / Name: 0b – Not locked or not enabled 1b – Locked

PORT_PLL_ENABLE

	29:28	**Reserved** Format: MBZ
	27	**Reference Select** Select between PLL references. 1b: Non-SSC 0b: SSC
	26:25	**Reserved** Format: MBZ
	24:0	**Reserved**

PORT_PLL_PCS_0

PORT_PLL_PCS_0	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	162400h-162403h
Name:	PORT_PLL_PCS_0_TX01_A
ShortName:	PORT_PLL_PCS_0_TX01_A
Power:	PG0
Reset:	global
Address:	162600h-162603h
Name:	PORT_PLL_PCS_0_TX23_A
ShortName:	PORT_PLL_PCS_0_TX23_A
Power:	PG0
Reset:	global
Address:	6C400h-6C403h
Name:	PORT_PLL_PCS_0_TX01_B
ShortName:	PORT_PLL_PCS_0_TX01_B
Power:	PG0
Reset:	global
Address:	6C600h-6C603h
Name:	PORT_PLL_PCS_0_TX23_B
ShortName:	PORT_PLL_PCS_0_TX23_B
Power:	PG0
Reset:	global
Address:	6C800h-6C803h
Name:	PORT_PLL_PCS_0_TX01_C
ShortName:	PORT_PLL_PCS_0_TX01_C
Power:	PG0
Reset:	global
Address:	6CA00h-6CA03h
Name:	PORT_PLL_PCS_0_TX23_C
ShortName:	PORT_PLL_PCS_0_TX23_C
Power:	PG0

PORT_PLL_PCS_0

Reset: global

DWord	Bit	Description
0	31:17	**Reserved** Format: PBC
	16	**reg_tx2_soft_reset_n** Active low reset to independently reset Tx lane2 in Display Port. reg_softreset_enable is the override enable for this reset to take effect Value: 0b — Name: Lane 2 Reset Value: 1b — Name: Lane 2 Active
	15:8	**Reserved** Format: PBC
	7	**reg_tx1_soft_reset_n** Active low reset to independently reset Tx lane1 in Display Port. reg_softreset_enable is the override enable for this reset to take effect Value: 0b — Name: Lane 1 Reset Value: 1b — Name: Lane 1 Active
	6:0	**Reserved** Format: PBC

PORT_REF_DW3

PORT_REF_DW3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	16218Ch-16218Fh
Name:	PORT_REF_DW3_A
ShortName:	PORT_REF_DW3_A
Power:	PG0
Reset:	global
Address:	6C18Ch-6C18Fh
Name:	PORT_REF_DW3_BC
ShortName:	PORT_REF_DW3_BC
Power:	PG0
Reset:	global

PHY Ref Dword 3
Instances per PHY dual/single
DDIA: PHY single, base 0x162000
DDIB/C: PHY dual, base 0x6C000
CL1 Ref base 0x180

DWord	Bit	Description
0	31:23	**Reserved** Format: PBC The values in this field must not be changed. Use read/modify/write to update this register.
	22	**grc_done** Access: RO
	21:0	**Reserved** Format: PBC The values in this field must not be changed. Use read/modify/write to update this register.

PORT_REF_DW6

PORT_REF_DW6	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00808080
Access:	R/W
Size (in bits):	32
Address:	162198h-16219Bh
Name:	PORT_REF_DW6_A
ShortName:	PORT_REF_DW6_A
Power:	PG0
Reset:	global
Address:	6C198h-6C19Bh
Name:	PORT_REF_DW6_BC
ShortName:	PORT_REF_DW6_BC
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:24	**grccode** Access: RO
	23:16	**ogrccode_fast** Default Value: 0x80
	15:8	**ogrccode_slow** Default Value: 0x80
	7:0	**ogrccode_nom** Default Value: 0x80

PORT_REF_DW8

PORT_REF_DW8	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x30000000
Access:	R/W
Size (in bits):	32
Address:	1621A0h-1621A3h
Name:	PORT_REF_DW8_A
ShortName:	PORT_REF_DW8_A
Power:	PG0
Reset:	global
Address:	6C1A0h-6C1A3h
Name:	PORT_REF_DW8_BC
ShortName:	PORT_REF_DW8_BC
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31	**fcomprefsel** GRC Flash Comparator Ref Select Value: 0 — Name: 400 ohm Value: 1 — Name: 100 ohm
	30:16	**Preserve Default 30 16** Default Value: 011000000000000b The values in this field must not be changed.
	15	**grcdis**
	14:2	**Preserve Default 14 2** Default Value: 0000000000000b The values in this field must not be changed.
	1	**grc_rdy_ovrd**
	0	**cfg_usegrcaslrc**

PORT_TX_DW2

PORT_TX_DW2	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00809800
Access:	R/W
Size (in bits):	32
Address:	162508h-16250Bh
Name:	PORT_TX_DW2_LN0_A
ShortName:	PORT_TX_DW2_LN0_A
Power:	PG0
Reset:	global
Address:	162588h-16258Bh
Name:	PORT_TX_DW2_LN1_A
ShortName:	PORT_TX_DW2_LN1_A
Power:	PG0
Reset:	global
Address:	162708h-16270Bh
Name:	PORT_TX_DW2_LN2_A
ShortName:	PORT_TX_DW2_LN2_A
Power:	PG0
Reset:	global
Address:	162788h-16278Bh
Name:	PORT_TX_DW2_LN3_A
ShortName:	PORT_TX_DW2_LN3_A
Power:	PG0
Reset:	global
Address:	162D08h-162D0Bh
Name:	PORT_TX_DW2_GRP_A
ShortName:	PORT_TX_DW2_GRP_A
Power:	PG0
Reset:	global
Address:	6C508h-6C50Bh
Name:	PORT_TX_DW2_LN0_B
ShortName:	PORT_TX_DW2_LN0_B

PORT_TX_DW2	
Power:	PG0
Reset:	global
Address:	6C588h-6C58Bh
Name:	PORT_TX_DW2_LN1_B
ShortName:	PORT_TX_DW2_LN1_B
Power:	PG0
Reset:	global
Address:	6C708h-6C70Bh
Name:	PORT_TX_DW2_LN2_B
ShortName:	PORT_TX_DW2_LN2_B
Power:	PG0
Reset:	global
Address:	6C788h-6C78Bh
Name:	PORT_TX_DW2_LN3_B
ShortName:	PORT_TX_DW2_LN3_B
Power:	PG0
Reset:	global
Address:	6CD08h-6CD0Bh
Name:	PORT_TX_DW2_GRP_B
ShortName:	PORT_TX_DW2_GRP_B
Power:	PG0
Reset:	global
Address:	6C908h-6C90Bh
Name:	PORT_TX_DW2_LN0_C
ShortName:	PORT_TX_DW2_LN0_C
Power:	PG0
Reset:	global
Address:	6C988h-6C98Bh
Name:	PORT_TX_DW2_LN1_C
ShortName:	PORT_TX_DW2_LN1_C
Power:	PG0
Reset:	global
Address:	6CB08h-6CB0Bh
Name:	PORT_TX_DW2_LN2_C
ShortName:	PORT_TX_DW2_LN2_C

PORT_TX_DW2

Power:	PG0
Reset:	global

Address:	6CB88h-6CB8Bh
Name:	PORT_TX_DW2_LN3_C
ShortName:	PORT_TX_DW2_LN3_C
Power:	PG0
Reset:	global

Address:	6CF08h-6CF0Bh
Name:	PORT_TX_DW2_GRP_C
ShortName:	PORT_TX_DW2_GRP_C
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:16	**omargin000** Default Value: 10000000b
	15:8	**ouniqtranscale** Default Value: 10011000b
	7:0	**Reserved** Format: MBZ

PORT_TX_DW3

PORT_TX_DW3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	16250Ch-16250Fh
Name:	PORT_TX_DW3_LN0_A
ShortName:	PORT_TX_DW3_LN0_A
Power:	PG0
Reset:	global
Address:	16258Ch-16258Fh
Name:	PORT_TX_DW3_LN1_A
ShortName:	PORT_TX_DW3_LN1_A
Power:	PG0
Reset:	global
Address:	16270Ch-16270Fh
Name:	PORT_TX_DW3_LN2_A
ShortName:	PORT_TX_DW3_LN2_A
Power:	PG0
Reset:	global
Address:	16278Ch-16278Fh
Name:	PORT_TX_DW3_LN3_A
ShortName:	PORT_TX_DW3_LN3_A
Power:	PG0
Reset:	global
Address:	162D0Ch-162D0Fh
Name:	PORT_TX_DW3_GRP_A
ShortName:	PORT_TX_DW3_GRP_A
Power:	PG0
Reset:	global
Address:	6C50Ch-6C50Fh
Name:	PORT_TX_DW3_LN0_B
ShortName:	PORT_TX_DW3_LN0_B

PORT_TX_DW3	
Power:	PG0
Reset:	global
Address:	6C58Ch-6C58Fh
Name:	PORT_TX_DW3_LN1_B
ShortName:	PORT_TX_DW3_LN1_B
Power:	PG0
Reset:	global
Address:	6C70Ch-6C70Fh
Name:	PORT_TX_DW3_LN2_B
ShortName:	PORT_TX_DW3_LN2_B
Power:	PG0
Reset:	global
Address:	6C78Ch-6C78Fh
Name:	PORT_TX_DW3_LN3_B
ShortName:	PORT_TX_DW3_LN3_B
Power:	PG0
Reset:	global
Address:	6CD0Ch-6CD0Fh
Name:	PORT_TX_DW3_GRP_B
ShortName:	PORT_TX_DW3_GRP_B
Power:	PG0
Reset:	global
Address:	6C90Ch-6C90Fh
Name:	PORT_TX_DW3_LN0_C
ShortName:	PORT_TX_DW3_LN0_C
Power:	PG0
Reset:	global
Address:	6C98Ch-6C98Fh
Name:	PORT_TX_DW3_LN1_C
ShortName:	PORT_TX_DW3_LN1_C
Power:	PG0
Reset:	global
Address:	6CB0Ch-6CB0Fh
Name:	PORT_TX_DW3_LN2_C
ShortName:	PORT_TX_DW3_LN2_C

PORT_TX_DW3

Power:	PG0
Reset:	global

Address:	6CB8Ch-6CB8Fh
Name:	PORT_TX_DW3_LN3_C
ShortName:	PORT_TX_DW3_LN3_C
Power:	PG0
Reset:	global

Address:	6CF0Ch-6CF0Fh
Name:	PORT_TX_DW3_GRP_C
ShortName:	PORT_TX_DW3_GRP_C
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:28	**Reserved** Format: MBZ
	27	**ouniqetrangenmethod**
	26	**oscaledcompmethod**
	25:0	**Reserved** Format: MBZ

PORT_TX_DW4

PORT_TX_DW4	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	162510h-162513h
Name:	PORT_TX_DW4_LN0_A
ShortName:	PORT_TX_DW4_LN0_A
Power:	PG0
Reset:	global
Address:	162590h-162593h
Name:	PORT_TX_DW4_LN1_A
ShortName:	PORT_TX_DW4_LN1_A
Power:	PG0
Reset:	global
Address:	162710h-162713h
Name:	PORT_TX_DW4_LN2_A
ShortName:	PORT_TX_DW4_LN2_A
Power:	PG0
Reset:	global
Address:	162790h-162793h
Name:	PORT_TX_DW4_LN3_A
ShortName:	PORT_TX_DW4_LN3_A
Power:	PG0
Reset:	global
Address:	162D10h-162D13h
Name:	PORT_TX_DW4_GRP_A
ShortName:	PORT_TX_DW4_GRP_A
Power:	PG0
Reset:	global
Address:	6C510h-6C513h
Name:	PORT_TX_DW4_LN0_B
ShortName:	PORT_TX_DW4_LN0_B

PORT_TX_DW4	
Power:	PG0
Reset:	global
Address:	6C590h-6C593h
Name:	PORT_TX_DW4_LN1_B
ShortName:	PORT_TX_DW4_LN1_B
Power:	PG0
Reset:	global
Address:	6C710h-6C713h
Name:	PORT_TX_DW4_LN2_B
ShortName:	PORT_TX_DW4_LN2_B
Power:	PG0
Reset:	global
Address:	6C790h-6C793h
Name:	PORT_TX_DW4_LN3_B
ShortName:	PORT_TX_DW4_LN3_B
Power:	PG0
Reset:	global
Address:	6CD10h-6CD13h
Name:	PORT_TX_DW4_GRP_B
ShortName:	PORT_TX_DW4_GRP_B
Power:	PG0
Reset:	global
Address:	6C910h-6C913h
Name:	PORT_TX_DW4_LN0_C
ShortName:	PORT_TX_DW4_LN0_C
Power:	PG0
Reset:	global
Address:	6C990h-6C993h
Name:	PORT_TX_DW4_LN1_C
ShortName:	PORT_TX_DW4_LN1_C
Power:	PG0
Reset:	global
Address:	6CB10h-6CB13h
Name:	PORT_TX_DW4_LN2_C
ShortName:	PORT_TX_DW4_LN2_C

PORT_TX_DW4

Power:	PG0
Reset:	global
Address:	6CB90h-6CB93h
Name:	PORT_TX_DW4_LN3_C
ShortName:	PORT_TX_DW4_LN3_C
Power:	PG0
Reset:	global
Address:	6CF10h-6CF13h
Name:	PORT_TX_DW4_GRP_C
ShortName:	PORT_TX_DW4_GRP_C
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:24	**ow2tapdeemph9p5**
	23:0	**Reserved** Format: MBZ

PORT_TX_DW5

PORT_TX_DW5	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00780000
Access:	R/W
Size (in bits):	32
Address:	162514h-162517h
Name:	PORT_TX_DW5_LN0_A
ShortName:	PORT_TX_DW5_LN0_A
Power:	PG0
Reset:	global
Address:	162594h-162597h
Name:	PORT_TX_DW5_LN1_A
ShortName:	PORT_TX_DW5_LN1_A
Power:	PG0
Reset:	global
Address:	162714h-162717h
Name:	PORT_TX_DW5_LN2_A
ShortName:	PORT_TX_DW5_LN2_A
Power:	PG0
Reset:	global
Address:	162794h-162797h
Name:	PORT_TX_DW5_LN3_A
ShortName:	PORT_TX_DW5_LN3_A
Power:	PG0
Reset:	global
Address:	162D14h-162D17h
Name:	PORT_TX_DW5_GRP_A
ShortName:	PORT_TX_DW5_GRP_A
Power:	PG0
Reset:	global
Address:	6C514h-6C517h
Name:	PORT_TX_DW5_LN0_B
ShortName:	PORT_TX_DW5_LN0_B
Power:	PG0

PORT_TX_DW5	
Reset:	global
Address:	6C594h-6C597h
Name:	PORT_TX_DW5_LN1_B
ShortName:	PORT_TX_DW5_LN1_B
Power:	PG0
Reset:	global
Address:	6C714h-6C717h
Name:	PORT_TX_DW5_LN2_B
ShortName:	PORT_TX_DW5_LN2_B
Power:	PG0
Reset:	global
Address:	6C794h-6C797h
Name:	PORT_TX_DW5_LN3_B
ShortName:	PORT_TX_DW5_LN3_B
Power:	PG0
Reset:	global
Address:	6CD14h-6CD17h
Name:	PORT_TX_DW5_GRP_B
ShortName:	PORT_TX_DW5_GRP_B
Power:	PG0
Reset:	global
Address:	6C914h-6C917h
Name:	PORT_TX_DW5_LN0_C
ShortName:	PORT_TX_DW5_LN0_C
Power:	PG0
Reset:	global
Address:	6C994h-6C997h
Name:	PORT_TX_DW5_LN1_C
ShortName:	PORT_TX_DW5_LN1_C
Power:	PG0
Reset:	global
Address:	6CB14h-6CB17h
Name:	PORT_TX_DW5_LN2_C
ShortName:	PORT_TX_DW5_LN2_C
Power:	PG0

PORT_TX_DW5

Reset:	global
Address:	6CB94h-6CB97h
Name:	PORT_TX_DW5_LN3_C
ShortName:	PORT_TX_DW5_LN3_C
Power:	PG0
Reset:	global
Address:	6CF14h-6CF17h
Name:	PORT_TX_DW5_GRP_C
ShortName:	PORT_TX_DW5_GRP_C
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31	**ocalcinit**
	30	**ocalccont**
	29:23	**Reserved** Format: MBZ
	22	**ovrd_setdata_h** Default Value: 1b
	21	**ovrd_resetdata_h** Default Value: 1b
	20	**ovrd_setdata_l** Default Value: 1b
	19	**ovrd_resetdata_l** Default Value: 1b
	18	**ovrd_dcc1010en**
	17	**ovrd_dfxbypassen**
	16	**ovrd_dccmode**
	15:12	**Reserved** Format: MBZ
	11	**otxclkspare**
	10	**DCC compout polarity** Invert the DCC compout polarity
	9	**DCC Delay Range 1** Adjust DCC delay range to 1st setting
	8	**DCC Delay Range 2** Adjust DCC delay range to 2nd setting

PORT_TX_DW5		
	7:0	**Reserved** Format: MBZ

PORT_TX_DW14

PORT_TX_DW14	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	162538h-16253Bh
Name:	PORT_TX_DW14_LN0_A
ShortName:	PORT_TX_DW14_LN0_A
Power:	PG0
Reset:	global
Address:	1625B8h-1625BBh
Name:	PORT_TX_DW14_LN1_A
ShortName:	PORT_TX_DW14_LN1_A
Power:	PG0
Reset:	global
Address:	162738h-16273Bh
Name:	PORT_TX_DW14_LN2_A
ShortName:	PORT_TX_DW14_LN2_A
Power:	PG0
Reset:	global
Address:	1627B8h-1627BBh
Name:	PORT_TX_DW14_LN3_A
ShortName:	PORT_TX_DW14_LN3_A
Power:	PG0
Reset:	global
Address:	162D38h-162D3Bh
Name:	PORT_TX_DW14_GRP_A
ShortName:	PORT_TX_DW14_GRP_A
Power:	PG0
Reset:	global
Address:	6C538h-6C53Bh
Name:	PORT_TX_DW14_LN0_B
ShortName:	PORT_TX_DW14_LN0_B
Power:	PG0

PORT_TX_DW14	
Reset:	global
Address:	6C5B8h-6C5BBh
Name:	PORT_TX_DW14_LN1_B
ShortName:	PORT_TX_DW14_LN1_B
Power:	PG0
Reset:	global
Address:	6C738h-6C73Bh
Name:	PORT_TX_DW14_LN2_B
ShortName:	PORT_TX_DW14_LN2_B
Power:	PG0
Reset:	global
Address:	6C7B8h-6C7BBh
Name:	PORT_TX_DW14_LN3_B
ShortName:	PORT_TX_DW14_LN3_B
Power:	PG0
Reset:	global
Address:	6CD38h-6CD3Bh
Name:	PORT_TX_DW14_GRP_B
ShortName:	PORT_TX_DW14_GRP_B
Power:	PG0
Reset:	global
Address:	6C938h-6C93Bh
Name:	PORT_TX_DW14_LN0_C
ShortName:	PORT_TX_DW14_LN0_C
Power:	PG0
Reset:	global
Address:	6C9B8h-6C9BBh
Name:	PORT_TX_DW14_LN1_C
ShortName:	PORT_TX_DW14_LN1_C
Power:	PG0
Reset:	global
Address:	6CB38h-6CB3Bh
Name:	PORT_TX_DW14_LN2_C
ShortName:	PORT_TX_DW14_LN2_C
Power:	PG0

PORT_TX_DW14

Reset:	global
Address:	6CBB8h-6CBBBh
Name:	PORT_TX_DW14_LN3_C
ShortName:	PORT_TX_DW14_LN3_C
Power:	PG0
Reset:	global
Address:	6CF38h-6CF3Bh
Name:	PORT_TX_DW14_GRP_C
ShortName:	PORT_TX_DW14_GRP_C
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31	**Reserved** Format: PBC The values in this field must not be changed. Use read/modify/write to update this register.
	30	**latency_optim**
	29:0	**Reserved** Format: PBC The values in this field must not be changed. Use read/modify/write to update this register.

Power Clock State Register

PWR_CLK_STATE - Power Clock State Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000066
	0x00000466
Access:	R/W
Size (in bits):	32
Address:	020C8h
Name:	Render Power Clock State Register
ShortName:	R_PWR_CLK_STATE
Address:	220C8h
Name:	BCS Power Clock State Register
ShortName:	BCS_PWR_CLK_STATE
Address:	120C8h
Name:	VCS Power Clock State Register
ShortName:	VCS_PWR_CLK_STATE
Address:	1A0C8h
Name:	VECS Power Clock State Register
ShortName:	VECS_PWR_CLK_STATE

This register contains the mode selection for configuring render engine to attain desired performance and power requirements for a given context. This register is render context save/restored. This register must be initialized correctly when the context is submitted for the first time. This register is context save/restored as part of Exec-List context image in both Exec-List and Ring-Buffer mode of scheduling. This register contents are valid only when "Enable" bit [31] of the register is set.

Programming Notes

This register is only functional for RenderCS. This register must not be exercised in VideoCS, BlitterCS and VideoEnhancementCS.

This register must not be programmed directly through CPU MMIO cycle.
Exec-List Scheduling Mode: Every context can have its own required render engine configuration by programming this register appropriately in the logical render context image in memory (LRCA) before submitting the context to the execlist submit port. This register must not be programmed using MI_LOAD_REGISTER_IMM command in ring buffer or in batch buffer, however programming "NON-SLM Indication" field through MI_LOAD_REGISTER_IMM is an exception defined below. If a need arises to change the render configuration for a context being executed in HW, Scheduler must preempt the context and update the desired render configuration in the logical render context image in memory and resubmit the context. Only "NON-SLM Indictaion" field in R_PWR_CLK_STATE register is allowed to be modified through MI_LOAD_REGISTER_IMM command in ring_buffer or privileged_batch_buffer. SW must modify only "NON-SLM Indication" field and must ensure to program other fields with the same value as in LRCA. SW must ensure to

PWR_CLK_STATE - Power Clock State Register

program PIPECONTROl flush command with CS Stall and HDC Flush prior to programming MI_LOAD_REGISTER_IMM command to modify "NON-SLM Indication" in R_PWR_CLK_STATE register.
Example: //R_PWR_CLK_STATE register value in LRCA configured with two slices and NON-SLM indication reset: 0x80005_0000 //SW desires to set NON-SLM Indication filed in ring buffer MI_LOAD_REGISTER_IMM 0x20C8, 0x8005_0100

Ring Buffer Scheduling: This register must be programmed using MI_LOAD_REGISTER_IMM command in the ring buffer. When this register is being programmed to re-configure the number of slices, SW must context save the state before programming this register and restore the state after programming the register via dummy MI_SET_CONTEXT command, this will ensure the existing state is programmed to all the new slices that are powered up, in case of slice shutdown (slice power down) this is not required.
Example:
MI_SET_CONTEXT -> CXTA
MI_BATCH_BUFFER_START
MI_BATCH_BUFFER_START
MI_SET_CONTEXT -> CXTB //Dummy Context to save existing render state to be restored latter.
MI_LOAD_REGISTER_IMM : R_PWR_CLK_STATE (1 Slice to 3 Slices) // Slice configuration done.
MI_STORE_DATA_IMM (Update R_PWR_CLK_STATE value in CTXA context image to modified value)
MI_SET_CONTEXT -> CXTA // Context restore of valid state to all the slices powered up with R_PWR_CLK_STATE restored with modifed value.

Power Clock State Enable must be always set with Render Power Clock state properly configured upon exercising Slice Shutdown or when “Render Power Gate Enabled” via POWERGATE_ENABLE register.

DWord	Bit	Description
0	31	**Power Clock State Enable** Format: U1 Value / Name / Description: 0h – Power Clock State Disabled – No specific power state set, bits[30:0] are ignored. 1h – Power Clock State Enabled – Power Clock is set and bit[30:0] are valid and have the desired state.
	30:0	**Power Clock State** Format: Power Clock State Format

Power Management Capabilities

PMCAP_0_2_0_PCI - Power Management Capabilities

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000022
Size (in bits):	16
Address:	000D2h

This register provides information on the capabilities of the function related to powermanagement.

DWord	Bit	Description
0	15:11	**PME Support** Default Value: 00000b Access: RO This field indicates the power states in which the IGD may assert PME#. Hardwired to 0 to indicate that the IGD does not assert the PME# signal.
	10	**D2 Support** Default Value: 0b Access: RO Hardwired to 0 to indicate the D2 power management state is not supported.
	9	**D1 Support** Default Value: 0b Access: RO Hardwired to 0 to indicate that the D1 power management state is not supported.
	8:6	**RESERVED** Default Value: 000b Access: RO Reserved
	5	**Device Specific Initialization** Default Value: 1b Access: RO Hardwired to 1 to indicate that special initialization of the IGD is required before generic class device driver is to use it.
	4	**RESERVED** Default Value: 000b

PMCAP_0_2_0_PCI - Power Management Capabilities

		Access: RO Reserved
	3	**PME Clock** Default Value: 0b Access: RO Hardwired to 0 to indicate IGD does not support PME# generation.
	2:0	**Version** Default Value: 010b Access: RO Hardwired to 010b to indicate that there are 4 bytes of power management registers implemented and that this device complies with revision 1.1 of the PCI Power Management Interface Specification.

Power Management Capabilities ID

PMCAPID_0_2_0_PCI - Power Management Capabilities ID

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000001
Size (in bits):	16
Address:	000D0h

This register contains the PCI Power Management Capability ID and the next capability pointer.

DWord	Bit	Description
0	15:8	**Next Capability Pointer** Default Value: 00000000b Access: RO This is a hardwired pointer to the next item in the capabilities list.
	7:0	**Capability Identifier** Default Value: 00000001b Access: RO Hardwired to 01h for power management.

Power Management Control and Status

PMCS_0_2_0_PCI - Power Management Control and Status

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	16
Address:	000D4h

DWord	Bit	Description
0	15	**PME Status** Default Value: 0b Access: RO This bit is hardwired to 0 to indicate that IGD does not support PME# generation from D3 (cold).
	14:13	**Data Scale** Default Value: 00b Access: RO This field is hardwired to 00 to indicate IGD does not support data register.
	12:9	**Data Select** Default Value: 0000b Access: RO This field is hardwired to 0h to indicate IGD does not support data register.
	8	**PME Enable** Default Value: 0b Access: RO This bit is hardwired to 0 to indicate that PME# assertion from D3 (cold) is disabled.
	7:2	**RESERVED** Default Value: 000b Access: RO Reserved
	1:0	**Power State** Default Value: 00b Access: RO Variant

PMCS_0_2_0_PCI - Power Management Control and Status		
		This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. Behavior of the graphics controller in supported states is detailed in the power management section of the Bspec. Bits[1:0] Power state 00: D0 Default 01: D1 Not Supported 10: D2 Not Supported 11: D3

PP_CONTROL

PP_CONTROL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000002
Access:	R/W
Size (in bits):	32
Address:	C7204h-C7207h
Name:	Panel Power 1 Control
ShortName:	PP_CONTROL_1
Power:	PG0
Reset:	soft
Address:	C7304h-C7307h
Name:	Panel Power 2 Control
ShortName:	PP_CONTROL_2
Power:	PG0
Reset:	soft

DWord	Bit	Description
0	31:9	**Reserved** Format: MBZ
	8:4	**Power Cycle Delay** This field provides the delay for the eDP T12 time; the shortest time from panel power disable to power enable. If panel power power state target is set to on during this delay, the power on sequence will not commence until the delay is complete. The value should be programmed to (desired delay / 100 milliseconds) + 1. Writing a value of 0 selects no delay or is used to abort the delay if it is active. Value: 00000b — Name: No delay Value: 00101b — Name: 400 mS Restriction: Restriction : A correct value must be programmed before enabling panel power.
	3	**VDD Override** This field forces VDD on. This is intended for panels that require VDD to be asserted before accessing AUX channel. Value | Name

PP_CONTROL

0b	Not Force
1b	Force

Restriction
Restriction : When software clears this bit from '1' to '0' (stop forcing VDD on) it must ensure that T4 power cycle delay is met before setting this bit to '1' again.

2 **Backlight Enable**

This field enables the backlight when hardware is in the correct panel power sequence state.

Value	Name
0b	Disable
1b	Enable

1 **Power Down on Reset**

This field selects whether the panel will run the power down sequence when a reset is detected.

Value	Name
0b	Do not run power down on reset
1b	Run power down on reset **[Default]**

Programming Notes
Running power down on reset is recommended for panel protection.

0 **Power State Target**

This field sets the panel power state target.
It can be written at any time and takes effect at the completion of any current power cycle.

Value	Name	Description
0b	Off	If panel power is currently on, the power off sequence starts immediately. If a power on sequence is currently in progress, the power off sequence starts after the power on state is reached, which may include a power cycle delay.
1b	On	If panel power is currently off, the power on sequence starts immediately. If a power off sequence is currently in progress, the power on sequence starts after the power off state is reached and the power cycle delay is met.

PP_OFF_DELAYS

PP_OFF_DELAYS		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	C720Ch-C720Fh	
Name:	Panel Power 1 Off Delays	
ShortName:	PP_OFF_DELAYS_1	
Power:	PG0	
Reset:	soft	
Address:	C730Ch-C730Fh	
Name:	Panel Power 2 Off Delays	
ShortName:	PP_OFF_DELAYS_2	
Power:	PG0	
Reset:	soft	

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28:16	**Power Down Delay** This fields provides the delay during power down. Software programs this field with the time delay for the eDP T10 time value; the time from source ending valid video data to source disabling panel power. Software controls the source valid video data output. The time unit is 100us.
	15:13	**Reserved** Format: MBZ
	12:0	**Backlight Off to Power Down** This field provides the backlight off to power down delay. Software programs this field with the time delay for the eDP T9 time value; the time from backlight disable to source ending valid video data. Software controls the backlight disable and source valid video data output. The time unit is 100us.

PP_ON_DELAYS

PP_ON_DELAYS	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	C7208h-C720Bh
Name:	Panel Power 1 On Delays
ShortName:	PP_ON_DELAYS_1
Power:	PG0
Reset:	soft
Address:	C7308h-C730Bh
Name:	Panel Power 2 On Delays
ShortName:	PP_ON_DELAYS_2
Power:	PG0
Reset:	soft

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28:16	**Power Up Delay** This field provides the delay during panel power up. Software programs this field with the delay for eDP T3; the time from enabling panel power to when the sink HPD and AUX channel should be ready. Software controls when AUX channel transactions start. The time unit is 100us.
	15:13	**Reserved** Format: MBZ
	12:0	**Power On to Backlight On** This field provides the power on to backlight enable delay. Software controls the source valid video data output and can enable backlight after this delay has been met. Hardware will not allow the backlight to enable until after the power up delay (eDP T3) and this delay have passed. The time unit is 100us.

PP_STATUS

PP_STATUS	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	C7200h-C7203h
Name:	Panel Power 1 Status
ShortName:	PP_STATUS_1
Power:	PG0
Reset:	soft
Address:	C7300h-C7303h
Name:	Panel Power 2 Status
ShortName:	PP_STATUS_2
Power:	PG0
Reset:	soft

DWord	Bit	Description
0	31	**Panel Power On Status** Value / Name / Description: 0b / Off / Panel power down has completed. A power cycle delay may be currently active. 1b / On / Panel power up has completed or power down sequence in progress. **Programming Notes** Software is responsible for enabling the embedded panel display only at the correct point as defined in the mode set sequence.
	30	**Reserved** Format: MBZ
	29:28	**Power Sequence Progress** Value / Name / Description: 00b / None / Panel is not in a power sequence 01b / Power Up / Panel is in a power up sequence (may include power cycle delay) 10b / Power Down / Panel is in a power down sequence 11b / Reserved / Reserved
	27	**Power Cycle Delay Active** Power cycle delays occur after a panel power down sequence or after a hardware reset.

PP_STATUS

		Value / **Name** 0b — Not Active **[Default]** 1b — Active
	26:4	**Reserved** Format: MBZ
	3:0	**Reserved**

PPPR

PPPR - PPPR

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	124824h

GT uses this register to post pending page requests to software, such as x86 page faults.
A write to this register triggers an MSI per the registers PRESTS, PRECTL, PREDATA, PREADR, and PREUADR.

DWord	Bit	Description
0	31:1	**RESERVED** Default Value: 0000000h Access: RO Reserved
	0	**POST PENDING PAGE REQUEST** Default Value: 0h Access: WO Post Pending Page Request

PPRO

PPRO - PPRO

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	124820h

GT uses this register to post Page Request Queue overflow faults

DWord	Bit	Description
0	31:1	**RESERVED** Default Value: 0000000h Access: RO Reserved
	0	**POST PAGE REQUEST OVERFLOW FAULT** Default Value: 0h Access: WO Post Page Request overflow fault

PRMRR_BASE_LSB

PRMRR_BASE_LSB - PRMRR_BASE_LSB			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	04CD8h		
The PMRR range is used to protect Xucode memory from unauthorized reads and writes. This register controls the location of the PRMRR range by indicating its starting address. It functions in tandem with the PRMRR mask register. This register is a LOCAL CR register and not an MMIO register			
DWord	**Bit**	**Description**	
0	31:12	**RANGE_BASE**	
		Default Value:	00000h
		Access:	R/W Lock
		This field corresponds to bits 38:12 of the base address memory range which is allocated to EMRR memory.	
	11:0	**RESERVED**	
		Default Value:	000h
		Access:	RO
		Reserved	

PRMRR_BASE_MSB

PRMRR_BASE_MSB - PRMRR_BASE_MSB			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	8		
Address:	04CDCh		
The PMRR range is used to protect Xucode memory from unauthorized reads and writes. This register controls the location of the PRMRR range by indicating its starting address. It functions in tandem with the PRMRR mask register. This register is a LOCAL CR register and not an MMIO register			
DWord	**Bit**	**Description**	
0	6:0	**RANGE_BASE** Default Value: 00h Access: R/W Lock This field corresponds to bits 38:12 of the base address memory range which is allocated to EMRR memory.	

PRMRR_MASK_LSB

PRMRR_MASK_LSB - PRMRR_MASK_LSB

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04CE0h

This register controls the size of the PRMRR range by indicating which address bits must match the PRMRR base register value.
This register is a LOCAL CR register and not an MMIO register

DWord	Bit	Description
0	31:12	**RANGE_MASK** Default Value: 00000h Access: R/W Lock This field indicates which address bits must match PRMRR base in order to qualify as an PRMRR access.
	11	**RANGE_EN** Default Value: 0b Access: R/W Lock Indicates whether the EMRR range is enabled and valid.
	10	**LOCK** Default Value: 0b Access: R/W Lock Setting this bit locks all writeable settings in this register, including itself.
	9	**IWB_EN** Default Value: 0b Access: R/W Lock Implicit Writeback enable. Used by the System agent with memory tracing.
	8	**TRACE_EN** Default Value: 0b Access: R/W Lock Trace enable. Used by the System agent to enable memory tracing.

PRMRR_MASK_LSB - PRMRR_MASK_LSB

	7:0	**RESERVED** Default Value: 00h Access: RO Reserved

PRMRR_MASK_MSB

PRMRR_MASK_MSB - PRMRR_MASK_MSB		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	8	
Address:	04CE4h	
This register controls the size of the PRMRR range by indicating which address bits must match the PRMRR base register value. This register is a LOCAL CR register and not an MMIO register		
DWord	**Bit**	**Description**
0	6:0	**RANGE_MASK** Default Value: 00h Access: R/W Lock This field indicates which address bits must match PRMRR base in order to qualify as an PRMRR access.

PS_WIN_SZ

PS_WIN_SZ

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank

This register specifies the size in pixels of the scaled output window. A programmed value of (100, 100) will result in scaled output window of size 100x100 pixels.
Writes to this register arm PS registers on this pipe. After arming, any write to other PS registers will disarm all PS registers. Subsequent write to this register will arm them again.

Restriction

Restriction : When scaling a pipe, the scaled output must fit inside the pipe active area, so Pipe active size >= PS window position + PS window size.
When scaling a plane, the scaled output must fit inside the pipe source area, so Pipe source size >= PS window position + PS window size.

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28:16	**XSIZE** This field specifies the horizontal size in pixels of the scaled output window.
	15:13	**Reserved** Format: MBZ
	12:0	**YSIZE** This field specifies the vertical size in scan lines of the scaled output window. Restriction : Bit 0 must be zero for interlaced modes.

PS Depth Count

PS_DEPTH_COUNT - PS Depth Count	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02350h

This register stores the value of the count of samples that have passed the depth test. This register is part of the context save and restore. Note that the value of this register can be obtained in a pipeline-synchronous fashion without a pipeline flush by using the 3DCONTROL command. See 3D Overview in the 3D volume.
More details about the precise event counted by this register are located **here**.

Restriction
Restriction: Due to known HW issue this register doesn't reflect correct value and hence not dependable.

DWord	Bit	Description
0..1	63:32	**Depth Count UDW** This register reflects the total number of samples that have passed the depth test (i.e., will be visible). All samples are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Samples that pass the depth test but fail the stencil test will not be counted.
	31:0	**Depth Count LDW** This register reflects the total number of samples that have passed the depth test (i.e., will be visible). All samples are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Samples that pass the depth test but fail the stencil test will not be counted.

PWR_WELL_CTL

PWR_WELL_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32

Address:	45400h-45403h
Name:	Power Well Control 1
ShortName:	PWR_WELL_CTL1
Power:	PG0
Reset:	global

Address:	45404h-45407h
Name:	Power Well Control 2
ShortName:	PWR_WELL_CTL2
Power:	PG0
Reset:	global

Description

This register is used for display power control. There are multiple instances of this register format to allow software components to have parallel control of the display power.
PWR_WELL_CTL1 is generally used for BIOS to control power.
PWR_WELL_CTL2 is generally used for driver to control power.
The power enable requests from all sources are logically ORd together to enable the power, so the power will only disable after all sources have requested the power to disable.
When a power well is disabled (powered down), access to any registers in the power well will complete, but write data will be dropped and read data will be all zeroes.
The display connections diagram indicates which functional blocks are contained in each power well. The display MMIO register specification has a field for each register to indicate which power well it is in.

This register is on the ungated clock and the chip reset, not the FLR reset.

Restriction

Restriction : The power request field must not be changed for a resource while a power enable/disable for that resource is currently in progress, as indicated by power well state for that resource.

Restriction : Power wells must be enabled and disabled following the display initialization and mode set sequences.

DWord	Bit	Description
0	31	**Power Well 2 Request** Access: R/W

PWR_WELL_CTL

This field requests power well #2 to enable or disable.

Value	Name
0b	Disable
1b	Enable

Restriction
Restriction : Power well #2 must not be enabled until after FUSE_STATUS Fuse PG1 Distribution Status is Done. Power well #2 must not be enabled when Power well #1 is disabled.

30 Power Well 2 State

Access:	RO

This field indicates the status of power well #2.

Value	Name
0b	Disabled
1b	Enabled

29 Power Well 1 Request

Access:	R/W

This field requests power well #1 to enable or disable.

Value	Name
0b	Disable
1b	Enable

Restriction
Restriction : Power well #1 must not be enabled until after FUSE_STATUS Fuse PG0 Distribution Status is Done. Power well #1 must not be disabled when Power well #2 is enabled.

28 Power Well 1 State

Access:	RO

This field indicates the status of power well #1.

Value	Name
0b	Disabled
1b	Enabled

27:26 Reserved

Format:	MBZ

25:24 Reserved

Format:	MBZ

23:16 Reserved

PWR_WELL_CTL			
		Format:	MBZ
	15:14	**Reserved**	
		Format:	MBZ
	13:12	**Reserved**	
		Format:	MBZ
	11:10	**Reserved**	
		Format:	MBZ
	9:0	**Reserved**	
		Format:	MBZ

RC6 Context Base

RC6CTXBASE - RC6 Context Base		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00D48h	
RC6 Location		
DWord	**Bit**	**Description**
0	31:12	**RC6 Memory Base Low** Access: R/W Lock This field is used to set the base of memory where the RC6 power context will be saved This value MUST be above the base and below the top of stolen memory This register is locked (becomes read-only) when RC6MEMLOCK is 1
	11:4	**RC6 Memory Base High** Access: R/W Lock This field corresponds to bits [39:32] of RC6MEMBASE Use above 4GB is not currently supported, and these bits must be set to 0 This register is locked (becomes read-only) when RC6MEMLOCK is 1
	3	**Reserved** Access: RO
	2	**Write Register Content to GT** Access: R/W Lock RPMunit will forward C6 context steering bit/DRAM context base value to MSQCunit on boot vector message as part of GT C6 exit flow. Writing to this bit will re-initiate a c6 steering bit/dram base write to MSQCunit(in GT) even after boot vector message. This bit is self-cleared on sampling. This register is locked (becomes read-only) when RC6MEMLOCK is 1
	1	**RC6 DRAM Only** Access: R/W Lock 1'b0 : Allow C6 context to go to either DRAM or C6SRAM, as specified by RC6LOCATION(default) 1'b1 : C6 context always goes to DRAM; RC6LOCATION is ignored This register is locked (becomes read-only) when RC6MEMLOCK is 1

RC6CTXBASE - RC6 Context Base		
	0	**RC6Context Base Register Lock** Access: R/W Lock 1'b0 : All fields of this register are writable (default) 1'b1 : This register is Read Only BIOS must set this bit to prevent further changes

RC6 LOCATION

RC6LOCATION - RC6 LOCATION

Register Space:	MMIO: 0/2/0
Default Value:	0x00000001
Size (in bits):	32
Address:	00D40h

RC6 Location

DWord	Bit	Description
0	31	**RC6Context Location Lock** Access: R/W Lock 1'b0 : All fields of this register are writable (default) 1'b1 : This register is Read Only BIOS must set this bit to prevent further changes
	30:1	**Reserved** Access: RO
	0	**RC6Context Location** Access: R/W Lock 1'b0 : Send context data to C6SRAM (default) 1'b1 : Send context data to DRAM location specified in RC6MEMBASE Value: 1b — Name: **[Default]**

RCC LRA 0

RCC_LRA_0 - RCC LRA 0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0200FE00
Size (in bits):	32
Address:	04A40h

DWord	Bit	Description
0	31:27	**Reserved** Default Value: 00000b Access: RO
	26:18	**RCC LRA1 Min** Access: R/W Minimum value of programmable LRA1. Value: 010000000b — Name: **[Default]**
	17:9	**RCC LRA0 Max** Access: R/W Maximum value of programmable LRA0. Value: 001111111b — Name: **[Default]**
	8:0	**RCC LRA0 Min** Default Value: 000000000b Access: R/W Minimum value of programmable LRA0.

RCC LRA 1

RCC_LRA_1 - RCC LRA 1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x3FDE13BD
Size (in bits):	32
Address:	04A44h

DWord	Bit	Description
0	31	**Reserved** Default Value: 0b Access: RO
	30:22	**RCC LRA2 Max** Access: R/W Maximum value of programmable LRA2. Value: 011111111b — Name: **[Default]**
	21:13	**RCC LRA2 Min** Access: R/W Minimum value of programmable LRA2. Value: 011110000b — Name: **[Default]**
	12:11	**GATR LRA** Default Value: 10b Access: R/W Which LRA should GATR use.
	10:2	**RCC LRA1 Max** Access: R/W Maximum value of programmable LRA1. If RCCLRA2Min == RCCLRA2Max , GATR LRA is disabled, GATR cycles are mapped to RCCLRA0 If RCCLRA2Min == RCCLRA2Max , GATR LRA is disabled, RCCLRA1Max will default to RCCLRA2Max to reuse GATR entries Value: 011101111b — Name: **[Default]**

RCC_LRA_1 - RCC LRA 1

	1	**MSC LRA** Default Value: 0b Access: R/W Which LRA should MSC use.
	0	**RCC LRA** Default Value: 1b Access: R/W Which LRA should RCC use.

Revision Identification

RID2_0_2_0_PCI - Revision Identification

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	8
Address:	00008h

This register contains the revision number for Device #2 Functions 0.

DWord	Bit	Description
0	7:4	**Revision Identification Number MSB** Default Value: 0000b Access: RO Variant Firmware Only Four MSB of RID
	3:0	**Revision Identification Number** Default Value: 0000b Access: RO Variant Firmware Only Four LSB of RID

RTADDR_LSB

RTADDR_LSB - RTADDR_LSB

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	124830h

Register providing the base address of root-entry table.

DWord	Bit	Description
0	31:12	**RTA** Default Value: 0000000h Access: R/W This register points to base of page aligned, 4KB-sized root-entry table in system memory. Hardware ignores and not implements bits 63:HAW, where HAW is the host address width. Software specifies the base address of the root-entry table through this register, and programs it in hardware through the SRTP field in the Global Command register. Reads of this register returns value that was last programmed to it.
	11	**RTT** Default Value: 0h Access: R/W This field specifies the type of root-table referenced by the Root Table Address (RTA) field; 0: Root Table 1: Extended Root Table
	10:0	**RESERVED** Default Value: 000h Access: R/W Reserved

RTADDR_MSB

RTADDR_MSB - RTADDR_MSB		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	124834h	
Register providing the base address of root-entry table.		
DWord	**Bit**	**Description**
0	31:7	**RESERVED** Default Value: 000000h Access: R/W Reserved
	6:0	**RTA** Default Value: 00h Access: R/W This register points to base of page aligned, 4KB-sized root-entry table in system memory. Hardware ignores and not implements bits 63:HAW, where HAW is the host address width. Software specifies the base address of the root-entry table through this register, and programs it in hardware through the SRTP field in the Global Command register. Reads of this register returns value that was last programmed to it.

SCRATCH1

SCRATCH1 - SCRATCH1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000001
Size (in bits):	32
Address:	0B11Ch

DWord	Bit	Description
0	31:13	**SCRATCH** Access: R/W
	12	**SLM Save ECC hang Fix Disable** Access: R/W 0 - Hang indication sent to ltiseqslunit when uncorrectable error detected in any of the SLM lanes 1 - Hang indication sent to ltiseqslunit when uncorrectable error detected only in SLM lane0 lbcf_slmsave_ecc_hang_fix_disable
	11	**Snoop SLM Save Restore Fix Disable** Access: R/W 0 (default): Snoop fix during SLM Save Restore is enabled 1 : Snoop fix in LTCD during SLM Save Restore is disabled lbcf_ltcd_snpfix_dis
	31:10	**SCRATCH** Access: R/W
	10	**LTCD LAST TX IROW FIX** Access: R/W 0 (default): last transaction hitting irow before self-init/ebb-init bug fix enabled 1 : last transaction hitting irow before self-init/ebb-init bug fix disabled lbcf_lasttx_hitirow_fix_dis
	9	**LSQC RORW Performance Fix Disable** Access: R/W 0 (default) : Order cam match should not be qualified with destination for read serialization fix. 1 : Order cam match will be qualified with destination for read serialization fix. lbcf_csr_lsqc_rorwperf_dis

SCRATCH1 - SCRATCH1

	8	**Eviction Performance Fix Enable** Access: R/W Disable Eviction Performance fix 0 (default) - Enable Eviction Performance Fix in LSQC 1 - Disable Eviction Performance Fix in LSQC Value of this bit should be same as LBCF register bit 0xb118[22]. Value of this bit should be same as LNCF register bit 0xb008[0]. lbcf_csr_evict_perf_fix_en
	31:7	**SCRATCH** Access: R/W
	7	**Prefetch Page Fault Hang Fix Enable** Access: R/W 0 (default) - State/URB prefetch request does not hang for page fault,but no cache fill is done 1 - State/URB prefetch request hangs for page fault. lbcf_csr_cfg_pf_pgflt_fix_en
	6	**Coherent SQCAM Disable** Access: R/W 0 (default) - Enable sqcam look up for coh cycles 1 - Disable sqcam look up for coh cycles lbcf_csr_coh_sqcam_en
	5	**SLM/Non-SLM Fair Arbitration Fix Disable** Access: R/W 0 (default) - SLM/non-SLM Fair arbitration fix is enabled 1 - SLM/non-SLM Fair arbitration fix is disabled lbcf_csr_fairarb_perf_fix_dis
	4	**LSQC Non Coherent Flush on PM Flush Disable** Access: R/W 0 :(default) When PM flush is sent to L3, LSQC will generate Query to flush coherent and Non coherent Lines (DC/L3 ways) from L3. 1: When PM flush is sent to L3, LSQC will generate Query to flush only the Coherent Lines (DC/L3 ways) from L3. lbcf_csr_lsqc_flush_nc_on_pm_flush_dis

SCRATCH1 - SCRATCH1

	3	**roinv stall deassert** Default Value: 0 Access: R/W 0-When any of the text,const,state,text flag ro invalidation is in progress the stall is not deasserted 1-When any of the text,const,state,text flag ro invalidation is in progress the stall is deasserted lbcf_ltcd_roinv_stall_deassert
	2	**LBS SLA Retry Timer Decrement** Default Value: 0b Access: R/W 1: LBS SLA Retry Timer Decrement is enabled 0: LBS SLA Retry Timer Decrement is disabled This bit needs to be programmed to 1 to avoid SNOOP response livelock lbcf_lbs_sla_retry_timer_dec_en
	1	**LSQC COH SNOOP COAMA STREAM FIX EN** Default Value: 0b Access: R/W 1: Coherent Snoop Coama Stream related fix is enabled. 0: Fix is disabled lbcf_lsqc_coh_snp_coama_stream_fix_en
	0	**Reserved**

SCRATCH 2 for LNCFunit

SCRATCH_LNCF2 - SCRATCH 2 for LNCFunit

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	0B0A0h

DWord	Bit	Description
0	31	**Disable LNI SLM-ATOMIC on P1** Access: R/W Disable SLMATM on LNI Port1 0 (default) - slm atomic can go on port1 1 - Set the behavior to old rtl without the fix lncf_csr_lni_slmatomic_p1_cb
	30	**LNI Read on Port0 with memrdrtn CB** Access: R/W LNI Read on Port0 with memrdrtn CB 0 - (default) Read will be scheduled on Port-0 along with Memory Read Return 1 - Read will not be scheduled on Port0 along with Memory Read Return lncf_csr_lni_rdonp0_memrd_cb
	29	**LNI Write on P1 with memrdrtn CB** Access: R/W LNI Write on P1 with memrdrtn CB 0 - (default) Writes from p0 local bank will be routed to output port1 when mem rd rtn is present 1 - Writes from p0 local bank will not be routed to port1 in presence of mem rd rtn lncf_csr_lni_wronp1_memrd_cb
	28	**LNI HDCx WR toggle Signal Fix CB** Access: R/W LNI HDCx WR toggle Signal Fix CB 0 - (default) Hdcxwr_tgl will not toggle if HDC Writes are granted on both P0 and P1 1 - (default) Hdcxwr_tgl toggle if HDC Writes are granted on both P0 and P1 lncf_csr_lni_hdcxwr_tgl_cb
	27	**Reserved**
	26	**Reserved**
	25	**Reserved**

SCRATCH_LNCF2 - SCRATCH 2 for LNCFunit		
	24	**Reserved**
	23	**Reserved**
	22:0	**SCRATCH 2 field for LNCFunit** Access: R/W

SCRATCH2 Register

SCRATCH2 - SCRATCH2 Register		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B140h	
DWord	**Bit**	**Description**
0	31:0	**SCRATCH2** Access: R/W

SCRATCH for LNCFunit

SCRATCH_LNCF1 - SCRATCH for LNCFunit

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000001
Size (in bits):	32
Address:	0B008h

DWord	Bit	Description
0	31:8	**SCRATCH register for LNCFunit** Access: R/W
	7	**Reserved3** Access: R/W Reserved
	6	**Reserved3** Access: R/W Reserved
	5	**Disable LNI Port1 Read Priority** Access: R/W 0: (Default) Allow LNI to arbitrate read with highest priority over write on port1. 1: Allow LNI to arbitrate write with highest priority over read on port1. lncf_csr_lni_p1_read_priority_dis
	4	**LNI Partial Write Fix Disable** Access: R/W 0: (Default) Enable fix to disable write on port1 for a partial write. 1: Disable port1 write disable fix for a partial write. lncf_csr_lni_parwrfix_dis
	3	**LNE Arbitration Performance Fix** Access: R/W 0: (Default) Enable the performance fix for the case where LNE was inserting bubbles in SS read returns . HSD 2121468 1: Disable the performance fix for HSD 2121468 . lncf_csr_lne_perf_fix_dis

SCRATCH_LNCF1 - SCRATCH for LNCFunit

	2	**Memory fill delay** Access: R/W lncf_csr_lni_gt2_memfill_dis. 0:mem fills gt2 latency will be 1 . 1:mem fill gt2 latency will be same as gt3.
	1	**flush start delay** Access: R/W lncf_csr_lni_disable_flush_start_delay. 0:Flush processing in LNIunit starts one clock after receiving the flush command default. 1:Flush processing in LNIunit starts in the same clock in which flush command is received.
	0	**Non-IA coherent atomics enable** Default Value: 1b Access: R/W 0: atomics in GTI (). 1: atomics in L3 (non-IA atomic) (Default). Output signal from LNCF unit lncf_csr_lni_glblatmcs_l3. Value for this bit should be same as lbcf_csr_lsqc_glblatmcs_l3 b118[22]. Value of this bit should be same as LBCF register bit 0xb11c[8]. Adding Xbuf 8 MCP.

Slice 0 PFET control register with lock

PFETCTL - Slice 0 PFET control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0007005A
Size (in bits):	32
Address:	24188h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of this register are R/W 1 = All bits of this register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:21	**Reserved** Access: RO Reserved
	20	**Power Well Status** Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	19	**Powergood timer error** Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	18:16	**Delay from enabling secondary PFETs to power good.** Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 320ns

PFETCTL - Slice 0 PFET control register with lock

3'b100: 640ns
3'b101: 1280ns
3'b110: 2560ns
3'b111: 5120ns

Value	Name
111b	**[Default]**

15:13 **Time period last primay pfet strobe to secondary pfet strobe**

Access:	R/W Lock

Time period last primay pfet strobe to secondary pfet strobe
3'b000: 10ns (or 1 bclk)
3'b001: 20ns (or 2 bclk)
3'b010: 30ns (or 3 bclk)
3'b111: 80ns (or 8 bclk)

12:10 **Time period b/w two adjacent strobes**

Access:	R/W Lock

Time period b/w two adjacent strobes to the primary FETs
3'b000: 10ns (or 1 bclk)
3'b001: 20ns (or 2 bclk)
3'b010: 30ns (or 3 bclk)
3'b111: 80ns (or 8 bclk)

9:7 **FET setup margin from enable to strobe**

Access:	R/W Lock

Setup margin in design before sampling enable event at the first pre-charge sequencer/shift register flop
3'b000: 10ns (or 1 bclk)
3'b001: 20ns (or 2 bclk)
3'b010: 30ns (or 3 bclk)
3'b111: 80ns (or 8 bclk)

6:0 **Number of flops to enable primary FETs**

Default Value:	1011010b
Access:	R/W Lock

Number of flops to enable primary FETs. For a setting of N there will be N+1 total strobes generated
7'b0000000: 10 Flops to be strobed
7'b0000001: 11 Flops to be strobed
7'b0000010: 12 Flops to be strobed
7'b0001111: 26 Flops to be strobed

Slice 0 SubSlice 0 PFET control register with lock

PFETCTL - Slice 0 SubSlice 0 PFET control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0007000A
Size (in bits):	32
Address:	24408h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of PFETCTL register are R/W 1 = All bits of PFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:21	**Reserved** Access: RO Reserved
	20	**Power Well Status** Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	19	**Powergood timer error** Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	18:16	**Delay from enabling secondary PFETs to power good.** Default Value: 111b Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns

PFETCTL - Slice 0 SubSlice 0 PFET control register with lock

		3'b010: 160ns 3'b011: 320ns 3'b100: 640ns 3'b101: 1280ns 3'b110: 2560ns 3'b111: 5120ns
	15:13	**Time period last primay pfet strobe to secondary pfet strobe** Access: R/W Lock Time period last primay pfet strobe to secondary pfet strobe 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	12:10	**Time period b/w two adjacent strobes** Access: R/W Lock Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	9:7	**FET setup margin from enable to strobe** Access: R/W Lock Setup margin in design before sampling enable event at the first pre-charge sequencer/shift register flop 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	6:0	**Number of flops to enable primary FETs** Access: R/W Lock Number of flops to enable primary FETs. For a setting of N there will be N+1 total strobes generated 7'b0000000: 10 Flops to be strobed 7'b0000001: 11 Flops to be strobed 7'b0000010: 12 Flops to be strobed 7'b0001111: 26 Flops to be strobed

Value	Name
0001010b	**[Default]**

Slice 0 SubSlice 1 PFET control register with lock

PFETCTL - Slice 0 SubSlice 1 PFET control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0007000A
Size (in bits):	32
Address:	24488h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of Slice 0 PFETCTL register are R/W 1 = All bits of Slice 0 PFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:21	**Reserved** Access: RO Reserved
	20	**Power Well Status** Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	19	**Powergood timer error** Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	18:16	**Delay from enabling secondary PFETs to power good.** Default Value: 111b Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns

PFETCTL - Slice 0 SubSlice 1 PFET control register with lock

		3'b010: 160ns 3'b011: 320ns 3'b100: 640ns 3'b101: 1280ns 3'b110: 2560ns 3'b111: 5120ns
	15:13	**Time period last primay pfet strobe to secondary pfet strobe** Access: R/W Lock Time period last primay pfet strobe to secondary pfet strobe 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	12:10	**Time period b/w two adjacent strobes** Access: R/W Lock Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	9:7	**FET setup margin from enable to strobe** Access: R/W Lock Setup margin in design before sampling enable event at the first pre-charge sequencer/shift register flop 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	6:0	**Number of flops to enable primary FETs** Access: R/W Lock Number of flops to enable primary FETs. For a setting of N there will be N+1 total strobes generated 7'b0000000: 10 Flops to be strobed 7'b0000001: 11 Flops to be strobed 7'b0000010: 12 Flops to be strobed 7'b0001111: 26 Flops to be strobed

Value	Name
0001010b	**[Default]**

Slice 0 SubSlice 2 PFET control register with lock

PFETCTL - Slice 0 SubSlice 2 PFET control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0007000A
Size (in bits):	32
Address:	24508h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of Slice 0 PFETCTL register are R/W 1 = All bits of Slice 0 PFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:21	**Reserved** Access: RO Reserved
	20	**Power Well Status** Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	19	**Powergood timer error** Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	18:16	**Delay from enabling secondary PFETs to power good.** Default Value: 111b Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns

PFETCTL - Slice 0 SubSlice 2 PFET control register with lock

		3'b010: 160ns 3'b011: 320ns 3'b100: 640ns 3'b101: 1280ns 3'b110: 2560ns 3'b111: 5120ns
	15:13	**Time period last primay pfet strobe to secondary pfet strobe** Access: R/W Lock Time period last primay pfet strobe to secondary pfet strobe 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	12:10	**Time period b/w two adjacent strobes** Access: R/W Lock Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	9:7	**FET setup margin from enable to strobe** Access: R/W Lock Setup margin in design before sampling enable event at the first pre-charge sequencer/shift register flop 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	6:0	**Number of flops to enable primary FETs** Access: R/W Lock Number of flops to enable primary FETs. For a setting of N there will be N+1 total strobes generated 7'b0000000: 10 Flops to be strobed 7'b0000001: 11 Flops to be strobed 7'b0000010: 12 Flops to be strobed 7'b0001111: 26 Flops to be strobed

Value	Name
0001010b	**[Default]**

Software SCI

SWSCI_0_2_0_PCI - Software SCI

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	16
Address:	000E8h

This register serves 2 purposes:
1) Support selection of SMI or SCI event source (SMISCISEL - bit15)
2) SCI Event trigger (GSSCIE - bit 0). To generate a SW SCI event, software should program bit 15 (SMISCISEL) to 1. This is typically programmed once (assuming SMIs are never triggered). On a "0" to "1" subsequent transition in bit 0 of this register (caused by a software write operation), a SCI message will be sent to cause the TCOSCI_STS bit in GPE0 register to be set to 1. The corresponding SCI event handler in BIOS is to be defined as a _Lxx method, indicating level trigger to the operating system. Once written as 1, software must write a "0" to this bit to clear it, and all other write transitions (1-0, 0-0, 1-1) will not cause a SCI message to be sent. To generate a SW SMI event, software should program bit 15 to 0 and trigger SMI via writes to SWSMI register (See SWSMI register for programming details).

DWord	Bit	Description
0	15	**SMI or SCI event select** Default Value: 0b Access: R/W 0 = SMI (default) 1 = SCI If selected event source is SMI, SMI trigger and associated scratch bits accesses are performed via SWSMI register. If SCI event source is selected, the rest of the bits in this register provide SCI trigger capability and associated SW scratch pad area.
	14:1	**Software scratch bits** Default Value: 00000000000000b Access: R/W Read/write bits not used by hardware.
	0	**Software SCI Event** Default Value: 0b Access: R/W If SCI event is selected (SMISCISEL = 1), on a 0 to 1 transition of GSSCIE bit, a SCI message will be sent to cause the TCOSCI_STS bit in GPE0 register to be set to 1. Software must write a 0 to clear this bit.

Software SMI

SWSMI_0_2_0_PCI - Software SMI

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	16
Address:	000E0h

DWord	Bit	Description
0	15:8	**Software Scratch Bits** Default Value: 00000000b Access: R/W
	7:1	**Software Flag** Default Value: 0000000b Access: R/W Used to indicate caller and SMI function desired, as well as return result.
	0	**GMCH Software SMI Event** Default Value: 0b Access: R/W When Set this bit will trigger an SMI. Software must write a "0" to clear this bit. SMI will be triggered only if SWSCI[SMISCISEL] is set to select SMI.

Subsystem Identification

SID2_0_2_0_PCI - Subsystem Identification

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	16
Address:	0002Eh

This register is used to uniquely identify the subsystem where the PCI device resides.

DWord	Bit	Description
0	15:0	**Subsystem Identification** Default Value: 0000000000000000b Access: R/W Once This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.

Subsystem Vendor Identification

SVID2_0_2_0_PCI - Subsystem Vendor Identification

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	16
Address:	0002Ch

This register is used to uniquely identify the subsystem where the PCI device resides.

DWord	Bit	Description
0	15:0	**Subsystem Vendor ID** Default Value: 0000000000000000b Access: R/W Once This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.

Super Queue Internal Cnt Register I

SQCNT1 - Super Queue Internal Cnt Register I

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	09024h

SQ Internal Counter Register

DWord	Bit	Description
0	31:24	**RSVD** Access: RO
	23:20	**SQRWCQD** Access: R/W Read-Write Request Queue Command Get Delay: This indicates the number of clocks that are inserted between each GFX cycle being accepted on the GFX Read or GFX Write ports. By default, this is disabled, which means that the RWRQ is able to accept one cycle per clock. By any other value, the RWRQ inserts the number of idle clocks listed in this register before accepting another cycle from GFX, essentially throttling the bandwidth. During each idle clock, RWRQ is guaranteed not to assert its command get to either read or write port. 0000b = Disabled (no additional clocks added). 0001b = One idle clock inserted between command gets. 0010b = Two idle clocks inserted between command gets. ... 1111b = Fifteen idle clocks inserted between command gets.
	19:16	**SQCQD** Access: R/W Read-Only Request Queue Command Get Delay: This indicates the number of clocks that are inserted between each GFX cycle being accepted on the GFX Read-Only port. By default, this is disabled, which means that the RORQ will be able to accept one cycle per clock. By any other value, the RORQ inserts the number of idle clocks listed in this register before accepting another cycle from GFX, essentially throttling the bandwidth. During each idle clock, RORQ is guaranteed not to assert its command get. 0000b = Disabled (no additional clocks added). 0001b = One idle clock inserted between command gets. 0010b = Two idle clocks inserted between command gets. ... 1111b = Fifteen idle clocks inserted between command gets.

SQCNT1 - Super Queue Internal Cnt Register I

	15:9	**SQDPTH** Access: R/W Super Queue Depth: 7Fh = SQ Depth of 127. 7Eh = SQ Depth of 126. ... 40h = SQ Depth of 64. 3Fh = SQ Depth of 63. 3Eh = SQ Depth of 62. ... 07h = SQ Depth of 7. 06h = SQ Depth of 6. 05h = SQ Depth of 5. 04h = SQ Depth of 4. 03h = SQ Depth of 3. 02h = SQ Depth of 2. 01h = Reserved. 00h = Disabled (SQ Depth of MAX) (default). For the sizes that are larger than the physical SQ size, the depth limitation is treated as disabled. if SQDPTH > 88 for BXT B-step, SQ Depth should be treated as MAX that h/w is capable of. NOTE - FOR BXT-A STEP, REGISTER DESCRIPTION IS SIMILAR TO SKL DESCRIPTION. THIS FIELD IS ONLY ACCURATE FOR BXT-B STEP AND BEYOND.
	8	**RSVD** Access: RO
	7	**Reserved**
	6:0	**SQIDICNT** Access: R/W Outstanding SQ IDI Cycle Counter: This indicates the maximum number of outstanding cycles that are presented to IDI/uncore at any given time by Super Queue. By default, this is MAX, but can be throttled back to support fewer IDI cycles. 0 = Disabled (MAX). 1-127 = Max number of outstanding IDI cycles. For the sizes that are larger than the physical SQ size, the depth limitation is treated as disabled. (i.e. if SQIDICNT is greater than 88 for BXT B-step, SQ IDI limitation should be treated as MAX that h/w is capable of). NOTE - FOR BXT-A STEP, REGISTER DESCRIPTION IS SIMILAR TO SKL DESCRIPTION. THIS FIELD IS ONLY ACCURATE FOR BXT-B STEP AND BEYOND.

TILECTL

TILECTL - TILECTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	101000h

Tile control and TLB control.

DWord	Bit	Description
0	31:3	**Reserved** Default Value: 00000000h Access: RO Reserved
	2	**Reserved** Default Value: 0b Access: RO Reserved.
	1	**TLBPF** Default Value: 0b Access: R/W Store multiple PTE enable. This bit must be set to 1 for BXT A0 0: Only one Page Table Entry is stored in the Translation Lookaside Buffer cache. 1: Multiple Page Table Entries (8) are stored in the Translation Lookaside Buffer cache.
	0	**SWZCTL** Default Value: 0b Access: R/W In order to spread DRAM accesses between multiple channels in the most efficient way, address bits can be used as a channel select. The Driver needs to obtain the need for memory address swizzling via DRAM configuration registers and set the following bits. x0b - No Address Swizzling x1b - Address bit [6] needs to be swizzled for tiled surfaces

Top Of Low Usable DRAM

TOLUD_0_0_0_PCI - Top Of Low Usable DRAM

Register Space:	PCI: 0/0/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	000BCh

This 32 bit register defines the low usable DRAM.

DWord	Bit	Description
0	31:20	**TOLUD** Default Value: 000000000000b Access: R/W Lock This register contains bits 31 to 20 of an address one byte above the maximum DRAM memory above 4G that is usable by the operating system. The top of low usable DRAM is the lowest address above both graphics stolen memory and Tseg.
	19:1	**RESERVED** Default Value: 000b Access: RO Reserved
	0	**Lock** Default Value: 0b Access: R/W Key Lock This bit will lock all writeable settings in this register, including itself.

Top Of Upper Usable DRAM

TOUUD_0_0_0_PCI - Top Of Upper Usable DRAM

Register Space:	PCI: 0/0/0
Source:	BSpec
Default Value:	0x00000000, 0x00000000
Size (in bits):	64
Address:	000A8h

This 64 bit register defines the top of upper usable DRAM.

DWord	Bit	Description
0	63:39	**RESERVED** Default Value: 000b Access: RO Reserved
	38:20	**TOUUD** Default Value: 00000000000000000000b Access: R/W Lock This register contains bits 38 to 20 of an address one byte above the maximum DRAM memory above 4G that is usable by the operating system.
	19:1	**RESERVED** Default Value: 000b Access: RO Reserved
	0	**Lock** Default Value: 0b Access: R/W Key Lock This bit will lock all writeable settings in this register, including itself.

TSEG Base Memory

TSEGMB_0_0_0_PCI - TSEG Base Memory

Register Space:	PCI: 0/0/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	000B8h

This 32 bit register defines the TSEG Base.

DWord	Bit	Description
0	31:20	**TSEG Memory Base** Default Value: 000000000000b Access: R/W Lock This register contains the base address of TSEG DRAM memory. BIOS determines the base of TSEG memory which must be at or below Graphics Base of GTT Stolen Memory (PCI Device 0 Offset B4 bits 31:20). Bios must program the value of TSEGMB to be the same as BGSM when TSEG is disabled.
	19:1	**RESERVED** Default Value: 000b Access: RO Reserved
	0	**Lock** Default Value: 0b Access: R/W Key Lock This bit will lock all writeable settings in this register, including itself.

Unit Level Clock Gating Control 2

UCGCTL2 - Unit Level Clock Gating Control 2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	09404h

Unit Level Clock Gating Control Registers.

DWord	Bit	Description
0	31	**VFunit Clock Gating Disable** Access: R/W VFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	30	**VDSunit Clock Gating Disable** Access: R/W VDSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	29	**VDIunit Clock Gating Disable** Access: R/W VDIunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	28	**VCSunit Clock Gating Disable** Access: R/W VCSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	27	**DTOunit Clock Gating Disable** Access: R/W DTOunit Clock Gating Disable Control:

UCGCTL2 - Unit Level Clock Gating Control 2

		'0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	26	**VCPunit Clock Gating Disable** Access: R/W VCPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	25	**VCDunit Clock Gating Disable** Access: R/W VCDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	24	**URBMunit Clock Gating Disable** Access: R/W URBMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	23	**TSGunit Clock Gating Disable** Access: R/W TSGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	22	**TDLunit Clock Gating Disable** Access: R/W TDLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	21	**TDSunit Clock Gating Disable** Access: R/W TDSunit Clock Gating Disable Control:

UCGCTL2 - Unit Level Clock Gating Control 2

		'0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always) Programming note: To work around a clock gating issue for A0-D0, the clock gating disable must be set to a 1 unless the offset h229c bit 11, Replay Mode, is set to 0, mid-cmdbuffer preemption Clock gating on tdsunit cannot be disabled or set to 1
	20	**SVSMunit Clock Gating Disable** Access: R/W SVSMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	19	**SVGunit Clock Gating Disable** Access: R/W SVGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	18	**SOunit Clock Gating Disable** Access: R/W SOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	17	**SIunit Clock Gating Disable** Access: R/W SIunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	16	**SFunit Clock Gating Disable** Access: R/W SFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	15	**SECunit Clock Gating Disable**

UCGCTL2 - Unit Level Clock Gating Control 2

		Access: R/W SECunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	14	**SCunit Clock Gating Disable** Access: R/W SCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	13	**RCZunit Clock Gating Disable** Access: R/W RCZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	12	**RCPBunit Clock Gating Disable** Access: R/W RCPBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	11	**RCCunit Clock Gating Disable** Access: R/W RCCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	10	**QCunit Clock Gating Disable** Access: R/W QCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL2 - Unit Level Clock Gating Control 2

	9	**PSDunit Clock Gating Disable** Access: R/W PSDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	8	**PLunit Clock Gating Disable** Access: R/W PLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	7	**MTunit Clock Gating Disable** Access: R/W MTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	6	**MPCunit Clock Gating Disable** Access: R/W MPCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	5	**TDGunitClock Gating Disable** Access: R/W TDGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	4	**MSCunit Clock Gating Disable** Access: R/W MSCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL2 - Unit Level Clock Gating Control 2

	3	**TEunit Clock Gating Disable** Access: R/W TEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	2	**TETGunit Clock Gating Disable** Access: R/W TETGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	1	**MAunit Clock Gating Disable** Access: R/W MAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	0	**IZunit Clock Gating Disable** Access: R/W IZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

Unit Level Clock Gating Control 6

UCGCTL6 - Unit Level Clock Gating Control 6

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	09430h

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31	**SPARE 3 clock gate disable** Access: R/W SPARE 3 unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	30:28	**HDCunit clock gate disable** Access: R/W HDC units Clock Gating Disable Control: HDCREQ bit 28, HDCRET bit 29, HDCTLB bit 30. '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always) **Programming Notes** 3x6: Bit 28 (HDCREQ) must be set to disable clock gating.
	27	**MUCunit clock gate disable** Access: R/W MUC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	26	**GACVunit cuclk gate disable** Access: R/W GACV units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL6 - Unit Level Clock Gating Control 6

25	**GACBunit clock gate disable** Access: R/W GACB units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
24	**GAPSunit clock gate disable** Access: R/W GAPS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
23	**GAMTunit clock gate disable** Access: R/W GAMT units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
22	**Reserved**
21	**OASCREP** Access: R/W OASCREP units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
20	**OAADDRunit clock gate disable bit** Access: R/W OAADDR units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
19	**GACVunit clock gate disable** Access: R/W GACV units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality)

UCGCTL6 - Unit Level Clock Gating Control 6

		'1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	18	**BDMunit clock gate disable** Access: R/W BDM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	17	**GATSunit clock gate disable** Access: R/W GATS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	16	**OATREPunit clock gate disable** Access: R/W OATREP units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	15	**STunit clock gate disable** Access: R/W ST units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	14	**SDEunit clock gate disable** Access: R/W SDE units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	13	**VIN(VID6) unit clock gate disable** Access: R/W VIN(VID6) units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL6 - Unit Level Clock Gating Control 6

	12	**VIN(VID5) unit clock gate disable** Access: R/W VIN(VID5) units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	11	**WVOPunit clock gate disable** Access: R/W WVOP units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	10	**WUSB unit clock gate disable** Access: R/W WUSB units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	9	**WSECunit clock gate disable** Access: R/W WSEC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	8	**WRSunit clcok gate disable** Access: R/W WRS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	7	**WQRCunit clock gate disable** Access: R/W WQRC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL6 - Unit Level Clock Gating Control 6

	6	**WMPC unit level clock gate disable** Access: R/W WMPC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	5	**WINunit Clock gate disable** Access: R/W WIN units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	4	**WIME unit clock gate disable** Access: R/W WIME units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	3	**WHME unit clock gate disable** Access: R/W WHME units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	2	**WAVMunit Clock Gate Disable** Access: R/W WAVM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	1	**VSHMunit clock gate disable** Access: R/W VSHM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL6 - Unit Level Clock Gating Control 6		
	0	**VSLunit Clock gating disable** Access: R/W VSL units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

VEBOX MOCS Register0

VEBOX_MOCS_0 - VEBOX MOCS Register0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030
Size (in bits):	32
Address:	0CB00h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_0 - VEBOX MOCS Register0

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_0 - VEBOX MOCS Register0		
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register1

VEBOX_MOCS_1 - VEBOX MOCS Register1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034
Size (in bits):	32
Address:	0CB04h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_1 - VEBOX MOCS Register1

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_1 - VEBOX MOCS Register1

	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register2

VEBOX_MOCS_2 - VEBOX MOCS Register2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038
Size (in bits):	32
Address:	0CB08h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_2 - VEBOX MOCS Register2

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_2 - VEBOX MOCS Register2

	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register3

VEBOX_MOCS_3 - VEBOX MOCS Register3

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031
Size (in bits):	32
Address:	0CB0Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_3 - VEBOX MOCS Register3

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_3 - VEBOX MOCS Register3		
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register4

VEBOX_MOCS_4 - VEBOX MOCS Register4

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CB10h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_4 - VEBOX MOCS Register4

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_4 - VEBOX MOCS Register4

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register5

VEBOX_MOCS_5 - VEBOX MOCS Register5

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CB14h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_5 - VEBOX MOCS Register5

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_5 - VEBOX MOCS Register5

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register6

VEBOX_MOCS_6 - VEBOX MOCS Register6

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CB18h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_6 - VEBOX MOCS Register6

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_6 - VEBOX MOCS Register6

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register7

VEBOX_MOCS_7 - VEBOX MOCS Register7

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CB1Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_7 - VEBOX MOCS Register7

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_7 - VEBOX MOCS Register7

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register8

VEBOX_MOCS_8 - VEBOX MOCS Register8

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CB20h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_8 - VEBOX MOCS Register8

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_8 - VEBOX MOCS Register8

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register9

VEBOX_MOCS_9 - VEBOX MOCS Register9

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CB24h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_9 - VEBOX MOCS Register9

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_9 - VEBOX MOCS Register9

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register10

VEBOX_MOCS_10 - VEBOX MOCS Register10

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CB28h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_10 - VEBOX MOCS Register10

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_10 - VEBOX MOCS Register10

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register11

VEBOX_MOCS_11 - VEBOX MOCS Register11

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CB2Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_11 - VEBOX MOCS Register11

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_11 - VEBOX MOCS Register11

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register12

VEBOX_MOCS_12 - VEBOX MOCS Register12

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CB30h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_12 - VEBOX MOCS Register12

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_12 - VEBOX MOCS Register12

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register13

VEBOX_MOCS_13 - VEBOX MOCS Register13

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CB34h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_13 - VEBOX MOCS Register13

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_13 - VEBOX MOCS Register13

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register14

VEBOX_MOCS_14 - VEBOX MOCS Register14

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CB38h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_14 - VEBOX MOCS Register14

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_14 - VEBOX MOCS Register14

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register15

VEBOX_MOCS_15 - VEBOX MOCS Register15

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CB3Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_15 - VEBOX MOCS Register15

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_15 - VEBOX MOCS Register15

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register16

VEBOX_MOCS_16 - VEBOX MOCS Register16

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030
Size (in bits):	32
Address:	0CB40h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_16 - VEBOX MOCS Register16

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_16 - VEBOX MOCS Register16

	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register17

VEBOX_MOCS_17 - VEBOX MOCS Register17

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034
Size (in bits):	32
Address:	0CB44h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_17 - VEBOX MOCS Register17

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_17 - VEBOX MOCS Register17

	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register18

VEBOX_MOCS_18 - VEBOX MOCS Register18

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038
Size (in bits):	32
Address:	0CB48h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_18 - VEBOX MOCS Register18

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_18 - VEBOX MOCS Register18

	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register19

VEBOX_MOCS_19 - VEBOX MOCS Register19

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031
Size (in bits):	32
Address:	0CB4Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_19 - VEBOX MOCS Register19

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_19 - VEBOX MOCS Register19

	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register20

VEBOX_MOCS_20 - VEBOX MOCS Register20

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CB50h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_20 - VEBOX MOCS Register20

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_20 - VEBOX MOCS Register20

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register21

VEBOX_MOCS_21 - VEBOX MOCS Register21

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CB54h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_21 - VEBOX MOCS Register21

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_21 - VEBOX MOCS Register21		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register22

VEBOX_MOCS_22 - VEBOX MOCS Register22

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CB58h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_22 - VEBOX MOCS Register22

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_22 - VEBOX MOCS Register22

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register23

VEBOX_MOCS_23 - VEBOX MOCS Register23

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CB5Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_23 - VEBOX MOCS Register23

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_23 - VEBOX MOCS Register23

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register24

VEBOX_MOCS_24 - VEBOX MOCS Register24

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CB60h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_24 - VEBOX MOCS Register24

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_24 - VEBOX MOCS Register24

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register25

VEBOX_MOCS_25 - VEBOX MOCS Register25

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CB64h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_25 - VEBOX MOCS Register25

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_25 - VEBOX MOCS Register25

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register26

VEBOX_MOCS_26 - VEBOX MOCS Register26

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CB68h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_26 - VEBOX MOCS Register26

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_26 - VEBOX MOCS Register26

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register27

VEBOX_MOCS_27 - VEBOX MOCS Register27

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CB6Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_27 - VEBOX MOCS Register27

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_27 - VEBOX MOCS Register27

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register28

VEBOX_MOCS_28 - VEBOX MOCS Register28

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CB70h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_28 - VEBOX MOCS Register28

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_28 - VEBOX MOCS Register28

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register29

VEBOX_MOCS_29 - VEBOX MOCS Register29

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CB74h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_29 - VEBOX MOCS Register29

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX MOCS Register30

VEBOX_MOCS_30 - VEBOX MOCS Register30

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CB78h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_30 - VEBOX MOCS Register30

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_30 - VEBOX MOCS Register30

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register31

VEBOX_MOCS_31 - VEBOX MOCS Register31

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CB7Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_31 - VEBOX MOCS Register31

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_31 - VEBOX MOCS Register31

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register32

VEBOX_MOCS_32 - VEBOX MOCS Register32

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030
Size (in bits):	32
Address:	0CB80h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_32 - VEBOX MOCS Register32

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_32 - VEBOX MOCS Register32

	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register33

VEBOX_MOCS_33 - VEBOX MOCS Register33

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034
Size (in bits):	32
Address:	0CB84h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_33 - VEBOX MOCS Register33

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_33 - VEBOX MOCS Register33

	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register34

VEBOX_MOCS_34 - VEBOX MOCS Register34

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038
Size (in bits):	32
Address:	0CB88h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_34 - VEBOX MOCS Register34

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_34 - VEBOX MOCS Register34

	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register35

VEBOX_MOCS_35 - VEBOX MOCS Register35

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031
Size (in bits):	32
Address:	0CB8Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_35 - VEBOX MOCS Register35

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_35 - VEBOX MOCS Register35

	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register36

VEBOX_MOCS_36 - VEBOX MOCS Register36

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CB90h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_36 - VEBOX MOCS Register36

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_36 - VEBOX MOCS Register36		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register37

VEBOX_MOCS_37 - VEBOX MOCS Register37

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CB94h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_37 - VEBOX MOCS Register37

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_37 - VEBOX MOCS Register37

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register38

VEBOX_MOCS_38 - VEBOX MOCS Register38

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CB98h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_38 - VEBOX MOCS Register38

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_38 - VEBOX MOCS Register38

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register39

VEBOX_MOCS_39 - VEBOX MOCS Register39

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CB9Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_39 - VEBOX MOCS Register39

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_39 - VEBOX MOCS Register39

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register40

VEBOX_MOCS_40 - VEBOX MOCS Register40

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CBA0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_40 - VEBOX MOCS Register40

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_40 - VEBOX MOCS Register40		
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register41

VEBOX_MOCS_41 - VEBOX MOCS Register41

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CBA4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_41 - VEBOX MOCS Register41

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_41 - VEBOX MOCS Register41

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register42

VEBOX_MOCS_42 - VEBOX MOCS Register42

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CBA8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_42 - VEBOX MOCS Register42

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_42 - VEBOX MOCS Register42

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register43

VEBOX_MOCS_43 - VEBOX MOCS Register43

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CBACh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_43 - VEBOX MOCS Register43

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_43 - VEBOX MOCS Register43

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register44

VEBOX_MOCS_44 - VEBOX MOCS Register44

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CBB0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_44 - VEBOX MOCS Register44

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_44 - VEBOX MOCS Register44

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register45

VEBOX_MOCS_45 - VEBOX MOCS Register45

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CBB4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_45 - VEBOX MOCS Register45

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_45 - VEBOX MOCS Register45

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register46

VEBOX_MOCS_46 - VEBOX MOCS Register46

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CBB8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_46 - VEBOX MOCS Register46

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_46 - VEBOX MOCS Register46

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register47

VEBOX_MOCS_47 - VEBOX MOCS Register47

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CBBCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_47 - VEBOX MOCS Register47

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_47 - VEBOX MOCS Register47

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register48

VEBOX_MOCS_48 - VEBOX MOCS Register48

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030
Size (in bits):	32
Address:	0CBC0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_48 - VEBOX MOCS Register48

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_48 - VEBOX MOCS Register48		
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register49

VEBOX_MOCS_49 - VEBOX MOCS Register49

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034
Size (in bits):	32
Address:	0CBC4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_49 - VEBOX MOCS Register49

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_49 - VEBOX MOCS Register49

	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register50

VEBOX_MOCS_50 - VEBOX MOCS Register50

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038
Size (in bits):	32
Address:	0CBC8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_50 - VEBOX MOCS Register50

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_50 - VEBOX MOCS Register50

	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register51

VEBOX_MOCS_51 - VEBOX MOCS Register51

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031
Size (in bits):	32
Address:	0CBCCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_51 - VEBOX MOCS Register51

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_51 - VEBOX MOCS Register51		
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register52

VEBOX_MOCS_52 - VEBOX MOCS Register52

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CBD0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_52 - VEBOX MOCS Register52

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_52 - VEBOX MOCS Register52		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register53

VEBOX_MOCS_53 - VEBOX MOCS Register53

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CBD4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_53 - VEBOX MOCS Register53

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_53 - VEBOX MOCS Register53

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register54

VEBOX_MOCS_54 - VEBOX MOCS Register54

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CBD8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_54 - VEBOX MOCS Register54

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_54 - VEBOX MOCS Register54

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register55

VEBOX_MOCS_55 - VEBOX MOCS Register55

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CBDCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_55 - VEBOX MOCS Register55

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_55 - VEBOX MOCS Register55

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register56

VEBOX_MOCS_56 - VEBOX MOCS Register56

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CBE0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_56 - VEBOX MOCS Register56

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_56 - VEBOX MOCS Register56

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register57

VEBOX_MOCS_57 - VEBOX MOCS Register57

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CBE4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_57 - VEBOX MOCS Register57

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_57 - VEBOX MOCS Register57

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register58

VEBOX_MOCS_58 - VEBOX MOCS Register58

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032
Size (in bits):	32
Address:	0CBE8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_58 - VEBOX MOCS Register58

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_58 - VEBOX MOCS Register58		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register59

VEBOX_MOCS_59 - VEBOX MOCS Register59

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036
Size (in bits):	32
Address:	0CBECh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_59 - VEBOX MOCS Register59

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_59 - VEBOX MOCS Register59

	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register60

VEBOX_MOCS_60 - VEBOX MOCS Register60

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A
Size (in bits):	32
Address:	0CBF0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_60 - VEBOX MOCS Register60

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_60 - VEBOX MOCS Register60		
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register61

VEBOX_MOCS_61 - VEBOX MOCS Register61

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033
Size (in bits):	32
Address:	0CBF4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_61 - VEBOX MOCS Register61

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_61 - VEBOX MOCS Register61

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register62

VEBOX_MOCS_62 - VEBOX MOCS Register62

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037
Size (in bits):	32
Address:	0CBF8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_62 - VEBOX MOCS Register62

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_62 - VEBOX MOCS Register62

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register63

VEBOX_MOCS_63 - VEBOX MOCS Register63

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B
Size (in bits):	32
Address:	0CBFCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Snoop Control Field** Default Value: 0b Access: R/W Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care

VEBOX_MOCS_63 - VEBOX MOCS Register63

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

VEBOX_MOCS_63 - VEBOX MOCS Register63

	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Vendor Identification

VID2_0_2_0_PCI - Vendor Identification		
Register Space:	PCI: 0/2/0	
Source:	BSpec	
Default Value:	0x00008086	
Size (in bits):	16	
Address:	00000h	
This register combined with the Device Identification register uniquely identifies any PCI device.		
DWord	**Bit**	**Description**
0	15:0	**Vendor Identification Number** Default Value: 1000000010000110b Access: RO PCI standard identification for Intel.

VGA_CONTROL

VGA_CONTROL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x80000000
Access:	R/W
Size (in bits):	32
Address:	41000h-41003h
Name:	VGA Control
ShortName:	VGA_CONTROL
Power:	PG0
Reset:	global

Restriction
Restriction : VGA requires panel fitting to be enabled. VGA is always connected to pipe A. VGA can not be enabled while the display power well is powered down. VGA display should only be enabled if all display planes other than VGA are disabled.

DWord	Bit	Description
0	31	**VGA Display Disable** This bit will disable the VGA compatible display mode. It has no effect on VGA register or A0000-BFFFF memory aperture accesses which are controlled by the PCI configuration and VGA I/O register settings. **Value** / **Name** 0b – Enable 1b – Disable **[Default]** **Restriction** Restriction : The VGA SR01 screen off bit must be programmed when enabling and disabling VGA. See the VGA Registers document. Restriction : GT driver mailbox must be programmed when enabling and disabling VGA. See the "VGA" section.
	30:27	**Reserved** Format: PBC
	26	**VGA Border Enable** This bit determines if the VGA border areas are included in the active display area. The border will be scaled along with the pixel data. **Value** / **Name**

VGA_CONTROL

	0b	Disable
	1b	Enable

25 Reserved

Format:	PBC

24 Pipe CSC Enable

Description
This bit enables pipe color space conversion for the VGA pixel data.

Value	Name
0b	Disable
1b	Enable

23:21 Reserved

Format:	PBC

20 Legacy 8Bit Palette En

This bit affects reads and writes to the palette through VGA I/O addresses.
In the 6-bit mode, the 8-bits of data are shifted up two bits on the write (upper two bits are lost) and shifted two bits down on the read.
This provides backward compatibility for original VGA programs as well as VESA VBE support for 8-bit palette.
It does not affect palette accesses through the palette register MMIO path.

Value	Name
0b	6 bit DAC
1b	8 bit DAC

19 Reserved

18 Reserved

17:16 Reserved

Format:	PBC

15:12 Reserved

11:8 Reserved

7:6 Blink Duty Cycle

Controls the VGA text mode blink duty cycle relative to the VGA cursor blink duty cycle.

Value	Name	Description
00b	100%	100% Duty Cycle, Full Cursor Rate
01b	25%	25% Duty Cycle, 1/2 Cursor Rate
10b	50%	50% Duty Cycle, 1/2 Cursor Rate
11b	75%	75% Duty Cycle, 1/2 Cursor Rate

VGA_CONTROL		
	5:0	**VSYNC Blink Rate** Controls the VGA blink rate in terms of the number of VSYNCs per on/off cycle. **Programming Notes** Program with (VSYNCs/cycle)/2-1

Video BIOS ROM Base Address

ROMADR_0_2_0_PCI - Video BIOS ROM Base Address

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	00030h

The IGD does not use a separate BIOS ROM, therefore this register is hardwired to 0s.

DWord	Bit	Description
0	31:18	**ROM Base Address** Default Value: 00000000000000b Access: RO Hardwired to 0's.
	17:11	**Address Mask** Default Value: 0000000b Access: RO Hardwired to 0s to indicate 256 KB address range.
	10:1	**Reserved** Default Value: 0000000b Access: RO Reserved
	0	**ROM BIOS Enable** Default Value: 0b Access: RO Hardwired to 0 to indicate ROM not accessible.

VTd Status

VTD_STATUS_0_2_0_PCI - VTd Status

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	8
Address:	00063h

This register contains indicator bits for Graphics VTd mode.

DWord	Bit	Description
0	7:1	**RESERVED** Default Value: 000b Access: RO Reserved
	0	**GFX VTd Active** Default Value: 0b Access: RO Variant Firmware Only Reflects GFX VTd Mode is active. 1 - if active, 0 if inactive.

Wait For Event and Display Flip Flags Register 1

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32

This register is the saved value of what wait for events are still valid. This register is part of context save and restore for RC6 feature.

Programming Notes	Source
Programming Restriction: This register should NEVER be programmed by SW, this is for HW internal use only.	
VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be exercised for reads or writes.	VideoCS, VideoCS2, VideoEnhancementCS

DWord	Bit	Description
0	31:25	**Reserved** Format: MBZ
	24	**Display Plane 11 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 11 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	23	**Display Plane 11 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 11 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	22	**Display Plane 10 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 10 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

		Pending Condition in the Device Programming Interface chapter of MI Functions.
	21	**Display Plane 10 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 10 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	20	**Display Plane 9 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 9 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	19	**Display Plane 9 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 9 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	18	**Display Plane 8 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 8 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	17	**Display Plane 8 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 8 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	16	**Display Plane 7 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 7 Flip Pending condition. If a flip

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

		request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	15	**Display Plane 7 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 7 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	14	**Display Pipe C Scan Line Event Pending** Format: Enable This field indicates scan line event operation is pending from Display Pipe C. This field gets set when MI_SCANLINE_INCL/EXCL command is parsed for Display Plane-C and gets reset on scan line event completion for Display Plane-C.
	13	**Display Pipe B Scan Line Event Pending** Format: Enable This field indicates scan line event operation is pending from Display Pipe B. This field gets set when MI_SCANLINE_INCL/EXCL command is parsed for Display Plane-B and gets reset on scan line event completion for Display Plane 3.
	12	**Display Pipe A Scan Line Event Pending** Format: Enable This field indicates scan line event operation is pending from Display Pipe A. This field gets set when MI_SCANLINE_INCL/EXCL command is parsed for Display Plane-A and gets reset on scan line event completion for Display Plane 1.
	11	**Reserved** Format: MBZ
	10	**Display Plane 3 Asyncronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	9	**Display Plane 3 Syncronous Flip Display Pending** Format: Enable

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

		This field enables a wait for the duration of a Display Plane 3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	8	**Display Plane 6 Syncronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 6 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	7	**Reserved** Source: BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS Format: MBZ
	7	**Display Plane 3 Asyncronous Performance Flip Pending Wait Enable** Source: RenderCS Format: Enable This field enables a wait for the duration of a Display Plane 3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	6	**Display Plane 3 Asyncronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 3 "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	5	**Display Plane 3 Syncronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	4	**Display Plane 6 Syncronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 6 Flip Pending condition. If a flip

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

		request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	3	**Reserved** Format: MBZ
	2	**Display Pipe C Scan Line Wait Enable** Format: Enable This field enables a wait while a Display Pipe C Scan Line condition exists. This condition is defined as the the start of the scan line specified in the Pipe C Display Scan Line Count Range Compare Register. See Scan Line Event in the Device Programming Interface chapter of MI Functions.
	1	**Display Pipe C Vertical Blank Wait Enable** Format: Enable This field enables a wait until the next Display Pipe C Vertical Blank event occurs. This event is defined as the start of the next Display Pipe C vertical blank period. Note that this can cause a wait for up to an entire refresh period. See Vertical Blank Event (See Programming Interface).
	0	**Reserved** Format: MBZ

Watchdog Counter Control

PR_CTR_CTL - Watchdog Counter Control

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000001
Access:	R/W
Size (in bits):	32

Restriction

Restriction: SW must enable and disable watch dog counter inline to a command sequence of any given workload within the same command buffer dispatch. Watch Dog counter once enabled doesn't stop unless it is explicitly disabled. SW must explicitly reset the watch dog counter by disabling it before enabling the watch dog counter for a new command sequence. Preemption could happen in a command sequence prior to watch dog counter getting disabled resulting in watch dog counter enabled following preemption. In Ring Buffer Mode of scheduling, SW must explicitly take care of disabling the watch dog counter as part of the preemption sequence. SW must explicitly reset the watch dog counter by disabling it before enabling the watch dog counter for a new command sequence. In Execution List Mode of scheduling, SW must do one of the following programing sequences to ensure watch dog timer is properly managed on context preemption. SW must not preempt workload that has watch dog timer enabled, that can be done by placing MI_ARB_ON_OFF command around the workload. OR SW must disable watch dog timer through direct MMIO access before submitting any execution list to the Execution List Submit port.

DWord	Bit	Description
0	31	**Count Select** Format: U1 **Value / Name / Description** 0h **[Default]** Use eight times the time stamp base unit to increment the watch dog count. The granularity of the time stamp base unit is defined in the "Time Stamp Bases" subsection in Power Management chapter. 1h Use the fixed function clock (csclk) to increment the watchdog count
	30:0	**Counter Logic Op** Default Value: 1h This field specifies the action to be taken by the clock counter to generate interrupts. Writing a Zero value to this register starts the counting. Writing a Value of 0000_0001 to this counter stops the counter.

WM_MISC

WM_MISC

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	45260h-45263h
Name:	Watermark Miscellaneous
ShortName:	WM_MISC
Power:	PG0
Reset:	soft

DWord	Bit	Description
0	31	**Reserved** Format: PBC
	30:28	**Reserved**
	27	**MIPI DBI Method** This field controls the behavior for the TTNF calculation for MIPI DBI. Value / Name / Description: 0b / Calculated / TTNF calculated in active area and all 1s outside of active. TTVBI all 1s. 1b / Simple / TTNF all 0s in active area and all 1s outside of active. TTVBI all 1s.
	26	**Reserved** Format: MBZ
	25:24	**MIPI DBI On Pipe C** This field selects whether MIPI DBI is on this pipe. This changes the TTNF and TTVBI calculations. Value / Name: 00b / MIPI DBI not on this pipe 10b / MIPIA DBI or dual link DBI on this pipe 11b / MIPIC DBI on this pipe
	23:22	**MIPI DBI On Pipe B** This field selects whether MIPI DBI is on this pipe. This changes the TTNF and TTVBI calculations. Value / Name: 00b / MIPI DBI not on this pipe 10b / MIPIA DBI or dual link DBI on this pipe 11b / MIPIC DBI on this pipe

WM_MISC

	21:20	**MIPI DBI On Pipe A** This field selects whether MIPI DBI is on this pipe. This changes the TTNF and TTVBI calculations. **Value** / **Name** 00b — MIPI DBI not on this pipe 10b — MIPIA DBI or dual link DBI on this pipe 11b — MIPIC DBI on this pipe
	19:0	**Reserved**

ZTLB LRA 0

ZTLB_LRA_0 - ZTLB LRA 0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x01007E00
Size (in bits):	32
Address:	04A30h

DWord	Bit	Description
0	31	**Reserved**
	30:29	**Reserved** Default Value: 00b Access: RO
	28:27	**STC LRA** Default Value: 00b Access: R/W Which LRA should STC use.
	26:18	**ZTLB LRA1 Min** Default Value: 001000000b Access: R/W Minimum value of programmable LRA1.
	17:9	**ZTLB LRA0 Max** Default Value: 000111111b Access: R/W Maximum value of programmable LRA0.
	8:0	**ZTLB LRA0 Min** Default Value: 000000000b Access: R/W Minimum value of programmable LRA0.

ZTLB LRA 1

ZTLB_LRA_1 - ZTLB LRA 1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x33BD80BF
Size (in bits):	32
Address:	04A34h

DWord	Bit	Description
0	31	**Reserved** Default Value: 0b Access: RO
	30:29	**HIZ LRA** Default Value: 01b Access: R/W Which LRA should HIZ use.
	28:27	**RCZ LRA** Default Value: 10b Access: R/W Which LRA should RCZ use.
	26:18	**ZTLB LRA2 Max** Access: R/W Maximum value of programmable LRA2. Value: 011101111b — Name: **[Default]**
	17:9	**ZTLB LRA2 Min** Default Value: 011000000b Access: R/W Minimum value of programmable LRA2.
	8:0	**ZTLB LRA1 Max** Default Value: 010111111b Access: R/W Maximum value of programmable LRA1.

ZTLB LRA 2

ZTLB_LRA_2 - ZTLB LRA 2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x000DFEF0
Size (in bits):	32
Address:	04A38h

DWord	Bit	Description
0	31:20	**Reserved** Default Value: 000000000000b Access: RO
	19:18	**GATR LRA** Default Value: 11b Access: R/W Which LRA should GATR use.
	17:9	**ZTLB LRA3 Max** Access: R/W Maximum value of programmable LRA3. Value: 011111111b — Name: **[Default]**
	8:0	**ZTLB LRA3 Min** Access: R/W Minimum value of programmable LRA3. Value: 011110000b — Name: **[Default]**