Intel® UHD Graphics Open Source

Programmer's Reference Manual

For the 2018 – 2019 Intel Core™ Processors and Pentium® Gold Processor Series based on the "Amber Lake" Platform

Volume 1: Configurations

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Configurations Overview

The Intel "Gen" Graphics Architecture was first introduced to the market in 2004. Since that time, the architecture and implementation have evolved to add many new features, increase performance, and improve power efficiency.

Each product generation has its own configurations chapter with the following subsections:

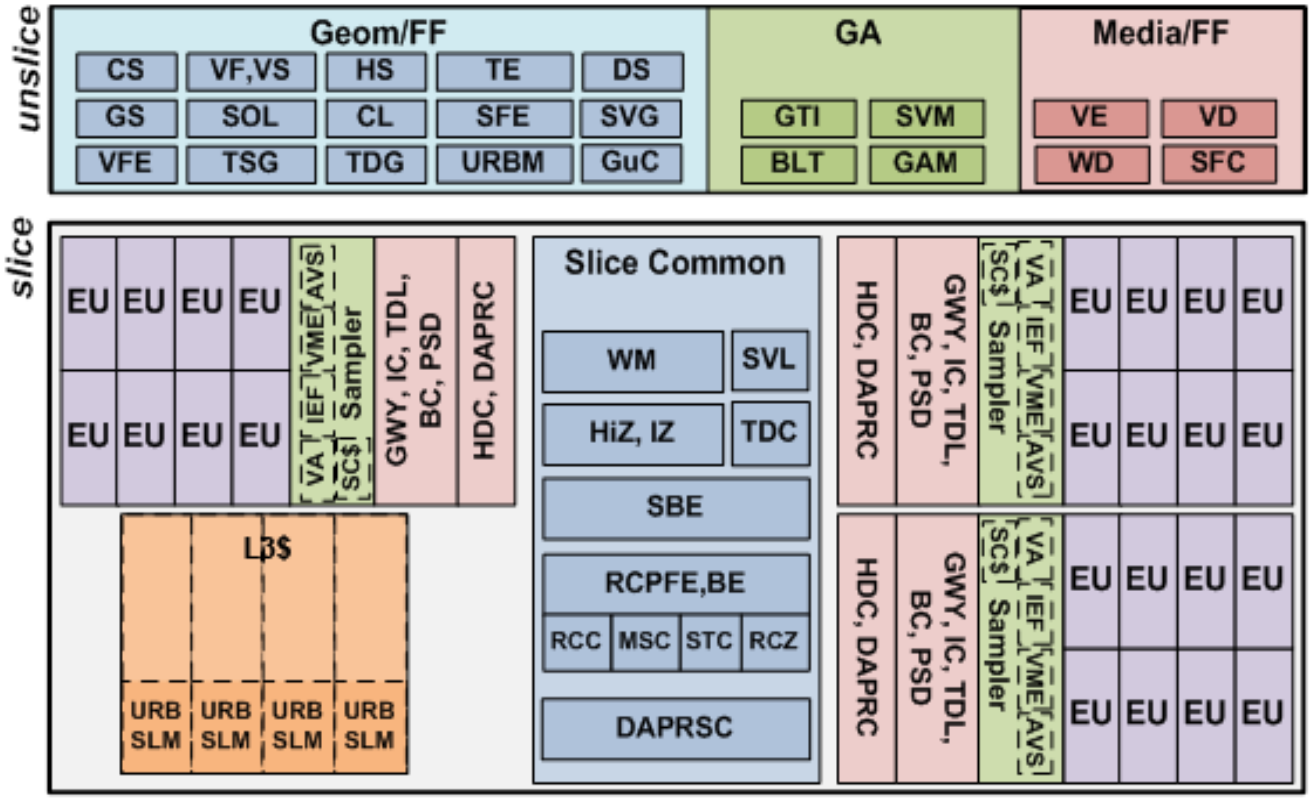
- Top Level Block Diagrams - Shows basic feature blocks of the project's graphics architecture, for GT configurations.
- Device Attributes - Lists details of the graphics configuration options for each project.
- Steppings and Device IDs - Lists all the current unique GT Die / Packages for a specific project.

Top Level Block Diagrams AML

The diagrams below show basic feature blocks of the Gen9 Amber Lake (AML) graphics architecture.

GT2 Configuration

The GT2 configuration contains one Unslice and one Slice with separate power domains for each, although they share a single clock domain.



This diagram is based on the following functional partitions:

(a) Geometry Fixed Functions (Geom/FF)

(b) Media Fixed Functions (Media/FF)

(c) Global Assets and GT Interface (GA)

(d) One or more Subslices (three shown)

(e) A Slice Common block

(f) An L3 Cache (L3$) block

Note that the combination of (a), (b), and (c) is typically referred to as the "unslice", while a combination of (d), (e), and (f) is referred to as a compute "slice".

The functionality in each of these groupings is further broken down as follows:

- Unslice – Fixed function pipelines for 3D, GPGPU, and Media operations, and interface to the outside world.
    - The 3D Geometry / Fixed Function (Geom/FF) block consisting of:
        - 3D fixed function pipeline (CS, VFVS, HS, TE, DS, GS, SOL, SL, SFE, SVG)
        - Video Front-End unit (VFE)
        - Thread Spawner unit (TSG) and the global Thread Dispatcher unit (TDG)
        - Unified Return Buffer Manager (URBM)
    - Media fixed function assets:
        - Video Decode (VD) Box
        - Video Encode (VE) Box
        - Wireless Display (WD) BOX
        - Scaler & Format Converter (SFC)
    - The Global Assets (GA) block as the primary interface and memory stream gateway to the outside world, consisting of:
        - GT Interface (GTI)
        - State Variable Manager (SVM)
        - Blitter (BLT)
        - Graphics Arbiter (GAM)
- Subslice (three shown) – A compute unit with supporting fixed- or shared-function assets sufficient for the EU capability.
    - A bank of Execution Units (EUs) – eight per subslice shown
    - Sampler, supporting both media and 3D functions
    - Gateway (GWY)
    - Instruction cache (IC)
    - Local Thread Dispatcher (TDL)
    - Barycentric Calculator (BC)
    - Pixel Shader Dispatcher (PSD)
    - Data Cluster (HDC)
    - Dataport Render Cache (DAPRC) - two per subslice
- Slice Common – Scalable fixed function assets which support the compute horsepower provided two or more subslices.
    - 3D Fixed Function:
        - Windower/Mask unit (WM)
        - Hi-Z (HZ) and Intermediate Z (IZ)
        - Setup Backend (SBE)
        - RCPFE, BE
        - 3D stream caches (RCC, MSC, STC, RCZ)

    - Media Fixed Functions:
        - DAPRSC
        - SVL
        - TDC
- L3 Cache – backing L3 cache for certain memory streams emanating from subslices.
    - L3 Data cache with support for data, URB, and shared local memory (SLM)

Device Attributes AML

The following table lists detailed GT device attributes for Amber Lake (AML) SKUs.

NOTE: This information is preliminary, and subject to change.

Product Configuration Attribute Table	
Product Family	**AML**
Architectural Name *	**1x3x8**
SKU Name	**POR**
Global Attributes	
Slice count	1
Subslice Count	3
EU/Subslice	8
EU count (total)	23 / 24 [b]
Thread Count	7
Thread Count (Total)	161 / 168
FLOPs/Clk - Half Precision, MAD (peak)	736 / 768
FLOPs/Clk - Single Precision, MAD (peak)	368 / 384
FLOPs/Clk - Double Precision, MAD (peak)	92 / 96
Unslice clocking (coupled/decoupled from Cr slice)	coupled
GTI / Ring Interfaces	1
GTI bandwidth (bytes/unslice-clk)	64: R
	64: W
eDRAM Support	N/A
Graphics Virtual Address Range	48 bit
Graphics Physical Address Range	39 bit
Caches & Dedicated Memories	
L3 Cache, total size (bytes)	768K
L3 Cache, bank count	4
L3 Cache, bandwidth (bytes/clk)	4x 64: R 4x 64: W
L3 Cache, D$ Size (Kbytes)	512K
URB Size (kbytes)	384K
SLM Size (kbytes)	0, 192K
LLC/L4 size (bytes) [1]	~2MB/CPU core
Instruction Cache (IC, bytes)	3x 48K
Color Cache (RCC, bytes)	24K
MSC Cache (MSC, bytes)	16K

Product Configuration Attribute Table	
HiZ Cache (HZC, bytes)	12K
Z Cache (RCZ, bytes)	32K
Stencil Cache (STC, bytes)	8K
Instruction Issue Rates	
FMAD, SP (ops/EU/clk)	8
FMUL, SP (ops/EU/clk)	8
FADD, SP (ops/EU/clk)	8
MIN,MAX, SP (ops/EU/clk)	8
CMP, SP (ops/EU/clk)	8
INV, SP (ops/EU/clk)	2
SQRT, SP (ops/EU/clk)	2
RSQRT, SP (ops/EU/clk)	2
LOG, SP (ops/EU/clk)	2
EXP, SP (ops/EU/clk)	2
POW, SP (ops/EU/clk)	1
IDIV, SP (ops/EU/clk)	1-6
TRIG, SP (ops/EU/clk)	2
FDIV, SP (ops/EU/clk)	1
Load/Store	
Data Ports (HDC)	3
L3 Load/Store (dwords/clk)	3x 64
SLM Load/Store (dwords/clk)	3x 64
Atomic Inc, 32b - sequential addresses (dwords/clk)	3x 64
Atomic Inc, 32b - same address (dwords/clk)	3x 4
Atomic CmpWr, 32b - sequential addresses (dwords/clk)	3x 32
Atomic CmpWr, 32b - same address (dwords/clk)	3x 4
3D Attributes	
Geometry pipes	1
Samplers (3D)	3
Texel Rate, point, 32b (tex/clk)	12
Texel Rate, point, 64b (tex/clk)	12
Texel Rate, point, 128b (tex/clk)	12
Texel Rate, bilinear, 32b (tex/clk)	12
Texel Rate, bilinear, 64b (tex/clk)	12
Texel Rate, bilinear, 128b (tex/clk)	3
Texel Rate, trilinear, 32b (tex/clk)	12

Product Configuration Attribute Table	
Texel Rate, trilinear, 64b (tex/clk)	6
Texel Rate, trilinear, 128b (tex/clk)	1.5
Texel Rate, aniso 2x, MIP Linear,, 32b (tex/clk)	3
Texel Rate, aniso 4x, MIP Linear,, 32b (tex/clk)	1.5
Texel Rate, aniso 8x, MIP Linear,, 32b (tex/clk)	0.75
Texel Rate, aniso 16x, MIP Linear,, 32b (tex/clk)	0.375
HiZ Rate, (ppc)	64
IZ Rate, (ppc)	16
Stencil Rate (ppc)	64
(500 MHz, DDR-2400 or eDRAM; Range depends on dynamic compression ratio)	
Pixel Rate, fill, 32bpp (pix/clk, RCC hit)	8
Pixel Rate, fill, 32bpp (pix/clk, LLC hit @ 1.0x unslice clk) [2]	
Pixel Rate, fill, 32bpp (pix/clk, LLC hit, @ 1.5x unslice clk) [2]	N/A
Pixel Rate, fill, 32bpp (pix/clk, memory, @ 1.0x unslice clk) [2]	
Pixel Rate, fill, 32bpp (pix/clk, memory, @ 1.5x unslice clk) [2]	N/A
(500 MHz, DDR-2400 or eDRAM; Range depends on dynamic compression ratio)	
Pixel Rate, blend, 32bpp (p/clk, RCC hit)	8
Pixel Rate, blend, 32bpp (p/clk, LLC hit, @ 1.0x unslice clk) [2]	
Pixel Rate, blend, 32bpp (p/clk, LLC hit, @ 1.5x unslice clk) [2]	N/A
Pixel Rate, blend, 32bpp (pix/clk, memory, @ 1.0x unslice clk) [2]	
Pixel Rate, blend, 32bpp (pix/clk, memory, @ 1.5x unslice clk) [2]	N/A
Media Attributes	
Samplers (media)	3
VDBox Instances	1
VEBox Instances	1
SFC Instances	1
WGBox Instances	N/A
Display Attributes	
Display Pipes	3
Display Planes per Pipe	3
DDI ports	2
eDP ports	1

Product Configuration Attribute Table
Footnotes: * Architectural Name = Slice Count x Subslice Count x EUs per Subslice [a] SKU naming & details has not yet been decided. [b] One EU reserved for die recovery purposes.

Stepping and Device IDs AML

The following table lists variations of GT Die / Packages for Gen9 Amber Lake (AML).

This information is preliminary, and subject to change at any time.

Segment	SKU	TDP	EUs	CPU Brand	Brand #	GFX Name	CPU Stepping	GT/Display Version	DID2 Grouping	DID2 8th Gen	Rev ID	POR
Mobile	Y22	5	24	Core i7	615	Intel® UHD Graphics	KBL Y0	KBL G0/C0	1	0x591C	0x0	Y
Mobile	Y22	5	24	Core i5	615	Intel® UHD Graphics	KBL Y0	KBL G0/C0	1	0x591C	0x0	Y
Mobile	Y22	5	24	Core m3	615	Intel® UHD Graphics	KBL Y0	KBL G0/C0	1	0x591C	0x0	Y
Mobile	Y22	6	23	Celeron	615	Intel® UHD Graphics	KBL Y0	KBL G0/C0	1	0x591C	0x0	Y
Mobile	Y22	6	24	Pentium	615	Intel® UHD Graphics	KBL Y0	KBL G0/C0	1	0x591C	0x0	Y
Mobile	Y22	7	24	Core i3	617	Intel® UHD Graphics	KBL Y0	KBL G0/C0	2	0x87C0	0x0	Y
Mobile	Y22	7	24	Core i5	617	Intel® UHD Graphics	KBL Y0	KBL G0/C0	2	0x87C0	0x0	Y
Mobile	Y22	7	24	Core i7	617	Intel® UHD Graphics	KBL Y0	KBL G0/C0	2	0x87C0	0x0	Y
Mobile	Y42	7	24	Core i3	TBD	Intel® UHD Graphics	WHL W0	KBL G0 / KBL C0	3	0x87CA	0x0	Y
Mobile	Y42	7	24	Core i5	TBD	Intel® UHD Graphics	WHL W0	KBL G0 / KBL C0	3	0x87CA	0x0	Y

Segment	SKU	TDP	EUs	CPU Brand	Brand #	GFX Name	CPU Stepping	GT/Display Version	DID2 Grouping	DID2 8th Gen	Rev ID	POR
Mobile	Y42	7	24	Core i7	TBD	Intel® UHD Graphics	WHL W0	KBL G0 / KBL C0	3	0x87CA	0x0	Y
Mobile	Y42	7	24	Core i3	TBD	Intel® UHD Graphics	WHL V0	CFL C0 / KBL C0	3	0x87CA	0x2	Y
Mobile	Y42	7	24	Core i5	TBD	Intel® UHD Graphics	WHL V0	CFL C0 / KBL C0	3	0x87CA	0x2	Y
Mobile	Y42	7	24	Core i7	TBD	Intel® UHD Graphics	WHL V0	CFL C0 / KBL C0	3	0x87CA	0x2	Y

Note: **AML GT baseline = KBL R (KBL G0 GT/C0 Display) and pair with SPT. Should follow the same KBL R family device enumeration, and any WA from KBL R should continue to be carried over.

Note: **AML 42 GT baseline = WHL 42, will need to follow the CFL/WHL family device enumeration, and any WA from CFL/WHL continued to be carried forward.

Note: AML 42 is based off WHL42 pair with SPT PCH. Need to follow the same for the Macro for product family as WHL/CFL.