# Intel<sup>®</sup> OpenSource HD Graphics PRM

**Volume 3 Part 2: Display Registers – CPU Registers** 

For the all new 2010 Intel Core Processor Family Programmer's Reference Manual (PRM)

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# **Revision History**

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# 1. CPU Display Registers [DevILK]

## 1.1 Introduction and Register Summary

This chapter contains the register descriptions for the display portion of a family of integrated graphics devices. These registers do vary by devices within the family of devices so special attention needs to be paid to which devices use which registers and register fields.

Different devices within the family may add, modify, or delete registers or register fields relative to another device in the same family based on the supported functions of that device. Additional information on the use and programming of these registers can be found in the display chapter.

The following table contains the sections break down where the register information is contained within this chapter:

Address Range	Description
40000h-4FFFFh	Shared Functions
50000h-5FFFFh	Messages
60000h-6FFFFh	Pipe and Port Controls
70000h-7FFFh	Plane Controls



# 1.1.1 Terminol ogy

Description	Software Use	Should be implemented as
Read/Write	This bit can be read or written.	
Reserved:	Don't assume a value for these bits. Writes have no effect.	Writes are ignored. Reads return zero.
Reserved: write as zero, must be zero, or MBZ	Software must always write a zero to these bits. This allows new features to be added using these bits that will be disabled when using old software and as the default case.	Writes are ignored. Reads return zero. Maybe be connected as Read/Write in future projects.
Reserved: software must preserve contents	Software must write the original value back to this bit. This allows new features to be added using these bits.	Read only Read/Write.
Read Only	This bit is read only. The read value is determined by hardware. Writes to this bit have no effect.	According to each specific bit. The bit value is determined by hardware and not affected by register writes to the actual bit.
Read/Clear	This bit can be read. Writes to it with a one cause the bit to clear.	Hardware events cause the bit to be set and the bit will be cleared on a write operation where the corresponding bit has a one for a value.
Double Buffered	Write when desired. Read gives the unbuffered value (written value) unless specified otherwise. Written values will update to take effect after a certain point.  Some have a specific arming sequence where a write to another register is required before the update can take place. This is used to ensure atomic updates of several registers.	Two stages of registers used. First stage is written into and used for readback (unless specified otherwise). First stage value is transferred into second stage at the update point. Second stage value is used to control hardware. Arm/disarm flag needed for specific arming sequences.

# 1.1.2 Register Protection for Panel Protection

TBD



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## 1.1.3 Display Mode Set Sequence

#### **Enable sequence**

[DevIBX and DevCPT]: PCH clock reference source and PCH SSC modulator warmup = 1uS

[DevIBX and DevCPT]: PCH FDI receiver PLL warmup = 25us

[DevIBX and DevCPT]: PCH DPLL warmup = 50uS [ILK]: CPU PLL warmup = 20uS

[ILK]: CPU FDI transmitter PLL warmup = 10us

[ILK]: DMI latency = 20uS

FDI training pattern 1 time = 0.5uS

FDI training pattern 2 time = 1.5uS

FDI idle pattern time = 31uS

#### **Enable sequence**



#### Enable panel power as needed to retrieve panel configuration

- 1. Enable PCH clock reference source and PCH SSC modulator, wait for warmup (Can be done anytime before enabling port)
- 2. If enabling port on PCH: (Must be done before enabling CPU pipe or FDI)
  - a. Enable PCH FDI Receiver PLL, wait for warmup plus DMI latency
  - b. Switch from Rawclk to PCDclk in FDI Receiver (FDI A OR FDI B)
  - c. [ILK] CPU FDI PLL is always on and does not need to be enabled
- 3. Enable CPU panel fitter if needed for hires, required for VGA (Can be done anytime before enabling CPU pipe)
- 4. Configure CPU pipe timings, M/N/TU, and other pipe settings (Can be done anytime before enabling CPU pipe)
- 5. Enable CPU pipe
- 6. Configure and enable CPU planes (VGA or hires)
- 7. If enabling port on PCH:
  - a. Train FDI
    - i. Set pre-emphasis and voltage (iterate if training steps fail)
    - ii. Enable CPU FDI Transmitter and PCH FDI Receiver with Training Pattern 1 enabled.
    - iii. Wait for FDI training pattern 1 time
    - iv. Read PCH FDI Receiver ISR
    - v. Enable training pattern 2 on CPU FDI Transmitter and PCH FDI Receiver
    - vi. Wait for FDI training pattern 2 time
    - vii. Read PCH FDI Receiver ISR
    - viii. Enable normal pixel output on CPU FDI Transmitter and PCH FDI Receiver
    - ix. Wait for FDI idle pattern time for link to become active
  - b. Configure and enable PCH DPLL, wait for PCH DPLL warmup (Can be done anytime before enabling PCH transcoder)
  - c. Configure PCH transcoder timings, M/N/TU, and other transcoder settings (should match CPU settings).
  - d. Enable PCH transcoder
- 8. Enable ports
- 9. Enable panel power through panel power sequencing
- 10. Wait for panel power sequencing to reach enabled steady state
- 11. Disable panel power override
- 12. Enable panel backlight



#### Disable sequence

- 1. Disable Panel backlight
- 2. Disable panel power through panel power sequencing
- 3. Disable CPU planes (VGA or hires)
- 4. [ILK] Disable CPU panel fitter
- 5. Disable CPU pipe
- 6. Wait for CPU pipe off status (CPU pipe config register pipe state)
- 7. [DevILK], [DevIBX and DevCPT] If disablingDisplayPort on PCH, write the DisplayPort control register bit 31 to 0b.
- 8. [ILK] Disable CPU panel fitter (Can be done anytime after CPU pipe is off)
- 9. If disabling CPU embedded DisplayPort A
  - a. Disable port
  - b. Disable CPU DisplayPort PLL in the DisplayPort A register
  - c. Disable PCH 120MHz clock source output to CPU
- 10. Else disabling port on PCH:
  - a. Disable CPU FDI Transmitter and PCH FDI Receiver
  - b. Disable port
  - c. Disable PCH transcoder
  - d. Wait for PCH transcoder off status (PCH transcoder config register transcoder state)
  - e. DevCPT] Disable Transcoder DisplayPort Control if DisplayPort was used
  - f. [DevCPT] Disable Transcoder DPLL Enable bit in DPLL\_SEL
  - g. Disable PCH DPLL (Can be done anytime after PCH ports and transcoder are off)
  - h. If no other PCH transcoder is enabled
    - i. Switch from PCDclk to Rawclk in PCH FDI Receiver
    - ii. Disable PCH FDI Receiver PLL
- 11. If SSC is no longer needed, disable PCH SSC modulator
- 12. If clock reference no longer needed, disable PCH clock reference source



# 2. North Shared Functions (40000h–4FFFh)

# 2.1 VGA Control Registers

## 2.1.1 VGACNTRL—VGA Display Plane Control Register

	VGACNTRL—VGA Display Plane Control Register				
Register Ty	Register Type: MMIO				
Address O	Address Offset: 41000h				
Project:	All				
Default Val		900h			
Access:	R/W				
Size (in bits	s): 32				
Bit De			scription		
31 VGA_Display_Disable		ay_Disable			
Project: All		All			
Default Value: 0b		e: 0b	VGA Display Enabled		
BFFFF memory aperture access settings. VGA display should or		ory aperture acce A display should	ompatible display mode. It has no effect on VGA register or esses which are controlled by the PCI configuration and VGA only be enabled if all display planes other than VGA are disay planes need to stay disabled, only the VGA popup (curso	A register abled. After	
	Value Na	me	Description	Project	
	0b	Enable	VGA Display Enabled	All	
	1b	Disable	VGA Display Disabled	All	
30	Reserved	Project: /	II Format: PBC		

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### VGACNTRL—VGA Display Plane Control Register

29 VGA\_Pipe\_Select

Project: All Default Value: 0b

For dual pipe devices, this bit determines which pipe is to receive the VGA display data. This must be changed only when the VGA display is in the disabled state via the VGA display disable bit or during the write to enable VGA display.

Value N	a me	Description	Project
0b	PipeA	Selects Assigns the VGA display to Pipe A	All
1b	PipeB	Selects Assigns the VGA display to Pipe B	All

28:27 **Reserved** Project: All Format: PBC

26 VGA\_Border\_Enable

Project: All Default Value: 0b

This bit determines if the VGA border areas are included in the active display area and do or do not appear on the port output.

The border if enabled will be scaled along with the pixel data. Setting this bit allows the popup to be positioned overlapping the border area of the image.

Value N	a me	Description	Project
0b	Disable	VGA Border areas are not included in the image size calculations for active area.	All
1b	Enable	VGA Border areas are enabled and passed to the display pipe for display and used in the image size calculations.	All

25 Reserved Project: All Format: PBC

24 Pipe\_Color\_Space\_Conversion\_Enable

Project: All Default Value: 0b

This bit enables pipe color space conversion for the VGA pixel data. CSC mode in the pipe CSC registers must be set to match the format of the VGA pixel data.

Value Na me		Description	Project
0b	Bypass	VGA pixel data bypasses the pipe color space conversion logic	All
1b	Pass	VGA pixel data passes through the pipe color space conversion logic	All



#### VGACNTRL—VGA Display Plane Control Register

#### 23 VGA\_Palette\_Read\_Select

Project: All Default Value: 0b

This bit only applies to dual display pipe devices and determines which palette VGA palette read accesses will occur from.

VGA palette reads are reads from I/O address 0x3c9.

Value N	a me	Description	Project
0b	Palette A	VGA palette reads will access Palette A	All
1b	Palette B	VGA palette reads will access Palette B	All

#### 22 VGA\_Palette\_A\_Write\_Disable

Project: All Default Value: 0b

This determines which palette the VGA palette writes will have as a destination. One or both palettes can be the destination. If both are disabled, writes will not affect the palette contents.

VGA palette writes are writes to I/O address 0x3C9h.

Value Na me		Description	Project
0b Update Palette A		VGA palette writes will update Palette A	All
1b	Not Update Palette A	VGA palette writes will not update Palette A	All

#### 21 VGA\_Palette\_B\_Write\_Disable

Project: All Default Value: 0b

This determines which palette the VGA palette writes will have as a destination. One or both palettes can be the destination. If both are disabled, writes will not affect the palette contents.

VGA palette writes are writes to I/O address 0x3C9h.

	Value N	a me	Description	Project
Ī	0b	Update Palette B	VGA palette writes will update Palette B	All
	1b	Not Update Palette B	VGA palette writes will not update Palette B	All

#### 20 Legacy\_VGA\_8-Bit\_Palette\_Enable

Project: All Default Value: 0b

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This bit only affects reads and writes to the palette through VGA I/O addresses. In the 6-bit mode, the 8-bits of data are shifted up two bits on the write (upper two bits are lost) and shifted two bits down on the read. It provides backward compatibility for original VGA programs (in it's default state) as well as VESA VBE support for 8-bit palette. It does not affect palette accesses through the palette register MMIO path.

Value Na	me	Description	Project
0b	6 bit DAC	6-bit DAC	All
1b	8 bit DAC	8-bit DAC	All



19	Reserved				
18	Reserved				
17:16	Reserved	Project:	All	F	format: PBC
15:12	Reserved				
11:8	Reserved				
7:6	Blink_Duty	_Cycle			
7:6	Blink_Duty_ Project:	_Cycle	All		
7:6			All 00b		
7:6	Project: Default Valu	ie:	00b	k duty cycle <u>relative to the VGA cursor blink</u>	duty cycle.
7:6	Project: Default Valu	ie:	00b	k duty cycle <u>relative to the VGA cursor blink</u> Description	duty cycle.  Project
7:6	Project: Default Valu Controls the	ie: VGA text mo	00b		1
7:6	Project: Default Valu Controls the	e: VGA text mo	00b	Description	Project
7:6	Project: Default Value Controls the  Value Na  00b	vGA text mome	00b	Description  100% Duty Cycle, Full Cursor Rate	Project All
7:6	Project: Default Value Controls the  Value Na  00b  01b	re: VGA text mo me 100% 25%	00b	Description  100% Duty Cycle, Full Cursor Rate  25% Duty Cycle, ½ Cursor Rate	Project All All



## 2.2 Sine ROM Registers

## 2.2.1 SINE\_ROM—Sine ROM

## SINE\_ROM—Sine ROM

Register Type: MMIO
Address Offset: 42200h
Project: All

**Default Value:** 00000000h Access: R/W Special

Size (in bits): 32

This register can be used to calculate a sine (or cosine). The intent is to enable calculation of filter coefficients.

The angle is written to bits [16:6] as a 11 bit fixed point 0.11 value (example for setting different degrees below). Then the sine is read from bits [16:6] as a 11 bit fixed point, 1.10 value.

the sine is re	ad from ous [16:6] as a	11 bit fixed point	, 1.10 value			
Bit De			so	cription		
31:17	Reserved Project	t: All		Fo	ormat:	
16:6	Sine					
	Project:	All				
	Default Value:	0b				
	Write the angle, read	the sine				
	Programming Notes	<b>3</b>				
	Examples of values to	o write:				
	00000000000b = 0 o	r 360 degrees				
	01000000000b = 90	degrees				
	10000000000b = 180	) dearees				
	11000000000b = 270	-				
		-				+
5:0	Reserved Project	t: All		Fo	ormat:	╛



**Project** 

ΑII

ΑII

## 2.3 Power Measurement Registers

Value Na

0b

1b

me

Plane A

Plane B

These registers are read by the PMU to get information for use in device power estimation.

## 2.3.1 DE\_POWER1 - Display Engine Power Register 1

DE\_POWER1 - Display Engine Power Register 1 43208hMMIO **Register Type:** Project:Address All42400h Offset: Default Value:Project: 00000000hDevSNB Access:Default R/W00000000h Value: Size (in bits):Access: 32Read Only The contents of this register can not be changed, except bit 31, while compression is enabled Size (in bits): Bit De scription 31:8 Reserved Project: ΑII Format: MBZ Enable\_Frame\_Buffer\_Compression Project: ΑII Default Value: 0b This bit is used to globally enable DPFC function at the next Vertical Blank start. Value Na me Description **Project** 0b Disable Disable frame buffer compression ΑII 1b ΑII Enable Enable frame buffer compression Plane\_SelectTransmit\_Lanes\_Enabled 307:4 Project: ΑII Range 0..12 The total number of eDP & FDI lanes enabled. Default Value: 0b

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Description

Plane A

Plane B



		DE_POWER1	- Displ	lay Engine Power Register 1				
293:2	CPU_Fer	nce_EnableEnabled	Panel_Fit	ters				
	Project:	_	ILKAII					
	Range 02							
	Each ena	bled panel fitter cons	umes an a	dditional xx mW of power.				
	Default Value: 0b							
	Value N	a me	Descrip	otion		Project		
	0b	No CPU Disp Buf		Buffer is not in a CPU fence. No modifi wed from CPU to the Display Buffer	cations	All		
	1b	CPU Disp Buf	Display	Buffer exists in a CPU fence		All		
291:0	Enabled_	DPLLs						
	Project:	All						
	Range	02						
	Each DPI	L enabled consumes	s xx mW of	power.				
	Reserved	d						
	Reserved	d Project: A	II	Forma	t: MBZ			
28								
27	CS_SYN	C_FLIP_NUKE_Disa	ble					
	Project:	All						
	Default V	alue: 0b						
	Setting th	is bit will disable the	command s	streamer SYNC Flips from resetting the	DPFC.			
	Value N	a me		Description	Project			
	0b	Enable		Enable the CS SYNC Flip Nuke	All			
	1b	Disable		Disable the CS SYNC Flip Nuke	All			
26	MMIO_S	YNC_FLIP_Nuke_Di	sable					
	Project:	All						
	Default V	alue: 0b						
	Setting th	nis bit will disable the	MMIO Syn	c Flip from resetting the DPFC.				
	Value N	a me		Description	Project			
	0b	Enable		Enable the MMIO Sync Flip Nuke	All			
	1b	Disable		Disable the MMIO Sync Flip Nuke	All			
25	Persister	nt_Mode						
	Project:	All						
	Default V	alue: 0b						
	Value N	a me	Descripti	on		Project		
	0b	Non Persistent	Non Persi	istent Mode		All		



24:16	Reserved						
15	Reserved						
14:8	Reserved	Projec	ct: All		Format:	MBZ	
7:6	Compress	sion_Limit					
	Project:		All				
	Default Value: 0b						
	This regist		inimum lin	nit on compression. It is also u	sed to determine the	size of the	
		ression		Pixel I	ormat		
	Ra	atio		16 bpp	32 k	ppp	
	1		Not Sup	ported	Supported (CFB=F	В)	
	1/2		Supporte	ed (CFB=FB)	Supported (CFB=1)	/2 FB)	
	1/4		Supporte	ed (CFB=1/2FB)	Supported (CFB=1)	/4 FB)	
	CFB = Coi	mpressed F	rame Buff	er Size			<u>.</u>
	CFB = Cor	•		er Size cription			Projec
		•	<b>Desc</b>	cription ompression, compressed buffe	er is the same size as	the	<b>Projec</b>
	Value Na	1:1	1:1 c unco	cription ompression, compressed buffe mpressed buffer			All
	Value Na	a me	1:1 c unco 2:1 c	cription ompression, compressed buffe			+ -
	Value Na	1:1	1:1 c unco 2:1 c unco	cription ompression, compressed buffer ompressed buffer ompression, compressed buffer	er is one half the size	of the	All
	Value Na	1:1 2:1	1:1 c unco 2:1 c unco	cription ompression, compressed buffer mpressed buffer ompression, compressed buffer mpressed buffer. ompression, compressed buffer mpressed buffer.	er is one half the size	of the	All
5:4	Value Na 00b 01b 10b 11b	1:1 2:1 4:1	1:1 c unco 2:1 c unco 4:1 c unco	cription ompression, compressed buffer mpressed buffer ompression, compressed buffer mpressed buffer. ompression, compressed buffer mpressed buffer.	er is one half the size	of the	All All All
5:4	Value Na 00b 01b 10b 11b	me 1:1 2:1 4:1 Reserved	1:1 c unco 2:1 c unco 4:1 c unco	cription ompression, compressed buffer mpressed buffer ompression, compressed buffer mpressed buffer. ompression, compressed buffer mpressed buffer.	er is one half the size	of the	All All All
5:4	Value Na 00b 01b 10b 11b Write_Bac Project: Default Va	a me 1:1 2:1 4:1 Reserved ck_Waterm	Desc 1:1 c unco 2:1 c unco 4:1 c unco Rese ark	ompression, compressed buffer mpressed buffer ompressed buffer. ompressed buffer. ompression, compressed buffer mpressed buffer. erved	er is one half the size or is one quarter the s	of the	All All All
5:4	Value Na 00b 01b 10b 11b Write_Bac Project: Default Va Compress	a me 1:1 2:1 4:1 Reserved ck_Waterm	1:1 c unco 2:1 c unco 4:1 c unco Rese ark All 0b	cription ompression, compressed buffer mpressed buffer ompression, compressed buffer mpressed buffer. ompression, compressed buffer mpressed buffer.	er is one half the size or is one quarter the size of	of the ize of the	All All All All
5:4	Value Na 00b 01b 10b 11b Write_Bac Project: Default Va Compress writing the	a me 1:1 2:1 4:1 Reserved ck_Waterm due: ed data write data out to	1:1 c unco 2:1 c unco 4:1 c unco Rese ark All 0b	ompression, compressed buffer mpressed buffer ompression, compressed buffer mpressed buffer. ompression, compressed buffer mpressed buffer. erved	er is one half the size of the	of the ize of the	All All All All
5:4	Value Na 00b 01b 10b 11b Write_Bac Project: Default Va Compress writing the effect.	a me 1:1 2:1 4:1 Reserved ck_Waterm due: ed data write data out to	1:1 c unco 2:1 c unco 4:1 c unco Rese ark All 0b te back en memory.	cription  ompression, compressed buffer ompressed buffer ompressed buffer. ompressed buffer. ompression, compressed buffer mpressed buffer. erved  gine waits for this amount of de Compression SR mode must I	er is one half the size of the	of the ize of the be ready be d for this to	All All All
5:4	Value Na  00b  01b  10b  11b  Write_Bac  Project: Default Va  Compress writing the effect.  Value Na	a me 1:1 2:1 4:1 Reserved ck_Waterm alue: sed data write data out to	1:1 c unco 2:1 c unco 4:1 c unco Rese ark All 0b te back en memory.	ompression, compressed buffer mpressed buffer ompression, compressed buffer mpressed buffer. ompression, compressed buffer mpressed buffer. erved  gine waits for this amount of day Compression SR mode must be compressed buffer.	er is one half the size of the	of the ize of the be ready be d for this to	All All All All



	DE_P	OWER1 – Display Engine Power Register 1
3:0	CPU_Fence_Numb	per
	Project:	DevILK
	Default Value:	0b
	This field specifies the uncompressed fram	ne CPU visible FENCE number corresponding to the placement of the e buffer
3:0	Reserved	

# 2.3.2 DE\_POWER2 – Display Engine Power Register 2

		DE DOMEDO Divido Essivo Domenio de	•	
		DE_POWER2 – Display Engine Power Register	2	
Register Ty	/pe:	MMIO		
Address Of	ffset:	42404h		
Project:		DevSNB		
Default Val	ue:	0000000h		
Access:		Read Only		
Size (in bit	s):	32		
Bit De		scription		
31:0	DE_t	pandwidth_counter	Project:	All
		counter increments on every cache line put arriving at the DE. The bandw g the difference between two reads at a known interval. The counter is onl		

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# 2.4 DPFC Control Registers (43200h-433FFh)

## 2.4.1 DPFC\_CB\_BASE - DPFC Compressed Buffer Base Address

		PFC_	CB_BASE	– DPF	C Compresse	ed Buffer Bas	se Addre	ess
Register Ty	/pe:	MMIO						
Address O	ffset:	43200h						
Project:		All						
Default Val	ue:	000000	00h					
Access:		R/W						
Size (in bit	s):	32						
The conten	ts of t	his regis	ster can not	be chang	ed while compres	ssion is enabled.		
Bit De					scripti	on		
31:28	Rese	rved	Project:	All			Format:	MBZ
27:12	Com	pressed	_Frame_Buf	fer_Offset	_Address		Project:	All
	This	register	specifies offse	et of the Co	ompressed Frame	Buffer from the ba	se of stoler	n memory.
	The	buffer m	ust be 4K byte	e aligned.				
11:0	Rese	rved	Project:	All			Format:	MBZ

## 2.4.2 DPFC\_CONTROL — DPFC Control

	DPFC_CONTROL— DPFC Control
Register Type:	MMIO
Address Offset:	43208h
Project:	All
Default Value:	0000000h
Access:	R/W
Size (in bits):	32



		DPFC_	СО	NTROL— DPFC Control		
Bit De				scription		
31	Project: Default Val This bit is [ILK, Work  P  E  P  O  R  R	used to globally enablearound to allow CxSF rerequisite: Frame but nable primary plane of rogram Pipe Main Wa	le DF R after on the aterm on the	PFC function at the next Vertical Blank start.  er Frame Buffer Compression is disabled: compression and display pipe enabled e selected pipe if it is not already enabled nark for the selected pipe (WM0_PIPE_A or V e selected pipe ession ark	VM0_Pipe	e_B) to all
	• R	estore primary plane				
	Value Na	me		Description		Project
	0b	Disable		Disable frame buffer compression		All
	1b	Enable		Enable frame buffer compression		All
30	Plane_Sell Project: Default Val	All				
	Value Na	me	De	scription	Project	;
	0b	Plane A	Pla	ne A	All	
	1b	Plane B	Pla	ine B	All	
29	CPU_Fend Project: Default Val	All				
	Value Na	me	De	scription		Project
	0b	No CPU Disp Buf		splay Buffer is not in a CPU fence. No modificallowed from CPU to the Display Buffer	cations	All
	1b	CPU Disp Buf	Dis	splay Buffer exists in a CPU fence		All
28	Reserved	Project: All		Format	:: MB	<u></u>



		DPF	C_CONT	ROL— DPFC Control		
27	CS_SYN	C_FLIP_NUKE_Dis	able			
	Project:	All				
	Default V	alue: 0b				
	Setting th	is bit will disable the	command	streamer SYNC Flips from resetting the	DPFC.	
	Value N	la me		Description	Project	
	0b	Enable		Enable the CS SYNC Flip Nuke	All	
	1b	Disable		Disable the CS SYNC Flip Nuke	All	
26	Project: Default V			c Flin from resetting the DPFC		
26	Project: Default V	All alue: Ob		c Flip from resetting the DPFC.  Description	Project	
26	Project: Default V	All alue: Ob			Project	
26	Project: Default Volume N	All alue: Ob nis bit will disable the		Description		
26	Project: Default Volume Nob	All alue: 0b nis bit will disable the Enable Disable		Description Enable the MMIO Sync Flip Nuke	All	
	Project: Default V Setting th  Value N Ob 1b	All alue: 0b nis bit will disable the Enable Disable		Description Enable the MMIO Sync Flip Nuke	All	
	Project: Default V Setting tr  Value N 0b 1b  Persister	All alue: 0b nis bit will disable the Enable Disable nt_Mode		Description Enable the MMIO Sync Flip Nuke	All	
	Project: Default Volume Nob 1b  Persister Project:	All alue: 0b nis bit will disable the la me Enable Disable nt_Mode All alue: 0b		Description  Enable the MMIO Sync Flip Nuke  Disable the MMIO Sync Flip Nuke	All	Project
	Project: Default Volue Nob 1b  Persister Project: Default Volue Nob 1b	All alue: 0b nis bit will disable the Enable Disable nt_Mode All alue: 0b	Descripti	Description  Enable the MMIO Sync Flip Nuke  Disable the MMIO Sync Flip Nuke	All	<b>Project</b> All



## **DPFC\_CONTROL— DPFC Control**

#### 24:16 Compression\_Control

Project: All Security: Test Default Value: 0b

Setting the bits in this register disables certain compression capabilities.

Value Na	me	Description	Project
1XXXXXXXXb	Disable	Run length without 1 nibble ([ILK] this setting is not allowed)	All
0XXXXXXXXb	Enable	Run length with 1 nibble	All
X1XXXXXXXb	Disable	Run length without 2 nibble ILK] this setting is not allowed)	All
X0XXXXXXXb	Enable	Run length with 2 nibble	All
XX1XXXXXXb	Disable	Mono Palette Disabled	All
XX0XXXXXXb	Enable	Mono Palette Enabled	All
XXX1XXXXXb	Disable	Historical Palette Disabled	All
XXX0XXXXXb	Enable	Historical Palette Enabled	All
XXXX1XXXXb	Disable	Delta 6 Disabled	All
XXXX0XXXXb	Enable	Delta 6 Enabled	All
XXXXX1XXXb	Disable	Delta 5 Disabled	All
XXXXX0XXXb	Enable	Delta 5 Enabled	All
XXXXXX1XXb	Disable	Delta 4 Disabled	All
XXXXXX0XXb	Enable	Delta 4 Enabled	All
XXXXXXX1Xb	Disable	Delta 3 Disabled	All
XXXXXXX0Xb	Enable	Delta 3 Enabled	All
XXXXXXXX1b	Disable	Delta 2 Disabled	All
XXXXXXXX0b	Enable	Delta 2 Enabled	All

#### 15 **SLB\_Initialization\_Flush\_Disable\_Control**

Project: All Security: Test Default Value: 0b

14:8

Setting this bit will disable the SLB flush mechanism for the first frame DPFC is on.

Valu	ue N	a me		Description	Project
0b		Enable		Enable the SLB initialization flush	All
1b		Disable		Disable SLB initialization flush	All
Rese	rved	l Project:	All	Format	: MBZ



## **DPFC\_CONTROL— DPFC Control**

#### 7:6 Compression\_Limit

Project: All Default Value: 0b

This register sets a minimum limit on compression. It is also used to determine the size of the compressed buffer.

Compression	Pixel F	Format
Ratio	16 bpp	32 bpp
1	Not Supported	Supported (CFB=FB)
1/2	Supported (CFB=FB)	Supported (CFB=1/2 FB)
1/4	Supported (CFB=1/2FB)	Supported (CFB=1/4 FB)

FB = Frame Buffer Size

CFB = Compressed Frame Buffer Size

Value N	a me	Description	Project
00b	1:1	1:1 compression, compressed buffer is the same size as the uncompressed buffer	All
01b	2:1	2:1 compression, compressed buffer is one half the size of the uncompressed buffer.	All
10b	4:1	4:1 compression, compressed buffer is one quarter the size of the uncompressed buffer.	All
11b	Reserved	Reserved	All

#### 5:4 Write\_Back\_Watermark

Project: All Default Value: 0b

Compressed data write back engine waits for this amount of data (per segment) to be ready before writing the data out to memory. Compression SR mode must be a 1, or SR disabled for this to take effect.

Value Na	me	Description	Project
00b	4 cache lines	4 cache lines	All
01b	8 cache lines	8 cache lines	All
1Xb	Reserved	Reserved	All

#### 3:0 CPU\_Fence\_Number

Project: All Default Value: 0b

This field specifies the CPU visible FENCE number corresponding to the placement of the uncompressed frame buffer.[



# 2.4.3 DPFC\_RECOMP\_CTL — DPFC ReComp Control

		DPFC_REC	OMP_CTL — DPI	C ReComp	Со	ntrol	
Register Ty Address O Project: Default Val Access: Size (in bits	ffset: 4320 All ue: 0000 R/W	_					
Bit De			SCr	iption	A 11		1407
31:28	Reserved			Project:	All	Format:	MBZ
27	Project: Default Val		Description				Project
	Ob	Disable	Disable				All
	1b	Enable	Enable				All
26:16	If this many	Stall_Invalidation of or more invalidation then start the rec	tions occur in one frame,	Project: stop compressi	All on un	itil the num	ber falls below
15:6	Reserved	Project:	All			Format:	MBZ
5:0	After invali		ount watermark, wait this ma ion on the following fram	•	All e rest	arting the c	compressor.

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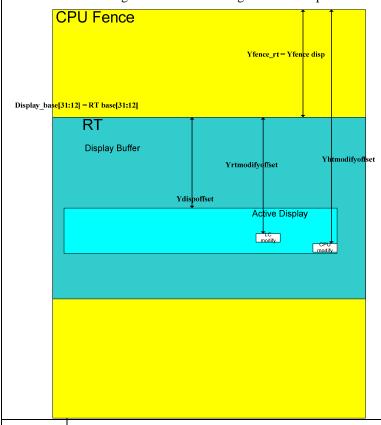
# 2.4.4 DPFC\_CPU\_Fence\_Offset — Y Offset CPU Fence Base to Display Buffer Base

## DPFC\_CPU\_Fence\_Offset — Y Offset CPU Fence Base to Display Buffer Base

Register Type: MMIO
Address Offset: 43218h
Project: All

Default Value: 00000000h Access: R/W Size (in bits): 32

The contents of this register can not be changed while compression is enabled.



Bit De				scription
31:22	Reserved	Project:	All	Format: MBZ
21:0	Yfence_disp			Project: All
	Y offset from t	the CPU fenc	e to the Di	splay Buffer base.
	[DevSNB] The			programmed to match the Display Buffer base, so this offset must



# 2.5 Interrupt Control Registers

# 2.5.1 Display Engine Interrupt Registers Bit Definition

	Display Engine Interrupt Re	gisters Bit Definition
Project:	All	
Size (in bits	•	the displacement for some which
	gine (DE) interrupt bits come from events within	the display engine, except for some which  STIIR and PMIIR are ORed together to generate
the CPU in		311111 and Fivility are Ofted together to generate
	r Engine Interrupt Control Registers all share the	e same bit definitions from this table.
Bit De	sc	ription
31	Master_Interrupt_Control	Project: All Format:
	This bit exists only in the DEIER Display Engine Inte	errupt Enable Register.
	This is the master control for the Display to CPU into propagate to the system.	errupt. This bit must be set to 1 for any interrupts
30	Reserved Project: All	Format:
29	Sprite_Plane_B_flip_done	Project: All Format:
	This is an active high pulse when a sprite plane B fli	p is done.
28	Sprite_Plane_A_flip_done	Project: All Format:
	This is an active high pulse when a sprite plane A fli	p is done.
27	Primary_Plane_B_flip_done	Project: All Format:
	This is an active high pulse when a primary plane B	flip is done.
26	Primary_Plane_A_flip_done	Project: All Format:
	This is an active high pulse when a primary plane A	flip is done.
25	PCU_event [DevILK]:	Project: DevILK Format:
	This is an active high pulse when a thermal or render and status should be checked in RGVINTRSTS (MC event comes display directly on a wire.	er geyserville event has occured. Interrupt source CHBAR+1184h) and TIS1 (MCHBAR+101Eh). This
25	Reserved Project: DevSNB	Format:
24	GTT_fault	Project: All Format:
	This is an active high level while either of the GTT F	ault Status register bits are set.
23	Poison	Project: All Format:
	This is an active high pulse on receiving the poison	message.
22	Performance_counter	Project: All Format:
	This is an active high pulse when the performance of the Performance Counter Source register.	counter reaches the threshold value programmed in



	Display Engine Interrupt Registers Bit Definition
21	PCH_Display_interrupt_event Project: All Format:
	This is an active high level while there is an interrupt being generated by the PCH Display. It will stay asserted until the interrupts in the PCH Display are all cleared. Only the rising edge of the PCH Display interrupt will cause the IIR to be set here, so all PCH Display Interrupts, including back to back interrupts, must be cleared before a new PCH Display Interrupt can cause the IIR to be set here.
20	AUX_Channel_A Project: All Format:
	This is an active high pulse on the AUX A done event.
18	GSE Project: DevSNB Format:
	This is an active high pulse on the GSE system level event.
17	DPST_histogram_event Project: All Format:
	This is an active high pulse on the DPST histogram event.
16	DPST_phase_in_event Project: All Format:
	This is an active high pulse on the DPST phase in event.
15	Pipe_B_vblank Project: All Format:
	This is an active high level for the duration of the Pipe B vertical blank.
14	Pipe_B_even_field Project: All Format:
	This is an active high level for the duration of the Pipe B interlaced even field.
13	Pipe_B_odd_field Project: All Format:
	This is an active high level for the duration of the Pipe B interlaced odd field.
12	Pipe_B_line_compare Project: All Format:
	This is an active high level for the duration of the selected Pipe B scan lines.
11	Pipe_B_vsync Project: All Format:
	This is an active high level for the duration of the Pipe B vertical sync.
10	Pipe_B_CRC_done Project: All Format:
	This is an active high pulse on the Pipe B CRC done.
9	Pipe_B_CRC_error Project: All Format:
	This is an active high pulse on the Pipe B CRC error.
8	Pipe_B_FIFO_underrun Project: All Format:
	This is an active high level for the duration of the Pipe B FIFO underrun.
7	Pipe_A_vblank Project: All Format:
	This is an active high level for the duration of the Pipe A vertical blank.
6	Pipe_A_even_field Project: All Format:
	This is an active high level for the duration of the Pipe A interlaced even field.
5	Pipe_A_odd_field Project: All Format:
	This is an active high level for the duration of the Pipe A interlaced odd field.
4	Pipe_A_line_compare Project: All Format:
	This is an active high level for the duration of the selected Pipe A scan lines.
3	Pipe_A_vsync Project: All Format:
	This is an active high level for the duration of the Pipe A vertical sync.
2	Pipe_A_CRC_done Project: All Format:
	This is an active high pulse on the Pipe A CRC done.



	Display Engine Interrupt Regi	sters Bit	Def	finition
1	Pipe_A_CRC_error	Project:	All	Format:
	This is an active high pulse on the Pipe A CRC error.			
0	Pipe_A_FIFO_underrun	Project:	All	Format:
	This is an active high level for the duration of the Pipe	A FIFO unde	errun.	

## 2.5.2 DEISR — Display Engine Interrupt Status Register

#### **DEISR** — Display Engine Interrupt Status Register

Register Type: MMIO
Address Offset: 44000h
Project: All
Default Value: 0000000

**Default Value:** 000000000h **Access:** Read Only

Size (in bits): 32

The ISR register contains the non-persistent value of all interrupt status bits. The IMR register selects which of these interrupt conditions are reported in the persistent IIR (i.e., set bits must be cleared by software). Bits in the IER are used to selectively enable IIR bits to cause CPU interrupts.

י שווו וווי פוום	LIX ale us	sed to selectively enable	int bits to cause or o interrupts.		
Bit De			scription		
31:0	Display_	Engine_Interrupt_Status_	Bits		
	Project:	All			
	Format:	Display Engine Interrupt R	egisters Bit Definition	See Description	Above
	This field	contains the non-persisten	t values of all interrupt status bits.		
	Value N	a me	Description		Project
	0b	Condition Doesn't exist	Interrupt Condition currently does not	exist	All
	1b	Condition Exists	Interrupt Condition currently exists		All

#### **Programming Notes**

Some inputs to this register are short pulses; therefore software should not expect to use this register to sample these conditions.

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## 2.5.3 DEIMR — Display Engine Interrupt Mask Register

## **DEIMR** — Display Engine Interrupt Mask Register

Register Type: MMIO
Address Offset: 44004h
Project: All

**Default Value:** FFFFFFFh

Access: R/W Size (in bits): 32

The IMR register is used by software to control which Interrupt Status Register bits are "masked" or "unmasked". "Unmasked" bits will be reported in the IIR, possibly triggering a CPU interrupt, and will persist in the IIR until cleared by software. "Masked" bits will not be reported in the IIR and therefore cannot generate CPU interrupts.

Bit De			scription	
31:0	Display_l	Engine_Interrupt_	_Mask_Bits	
	Project:	Al	II	
				0 5 : :: 41
	Format:	Display Engine Int	errupt Registers Bit Definition	See Description Above
			errupt Registers Bit Definition k which selects which interrupt bits from the I	•
		contains a bit masl		•
	This field	contains a bit masl	k which selects which interrupt bits from the I	SR are reported in the IIR.  Project



## 2.5.4 DEIIR — Display Engine Interrupt Identity Register

### **DEIIR** — Display Engine Interrupt Identity Register

Register Type: MMIO
Address Offset: 44008h
Project: All
Default Value: 0000000

Default Value: 00000000h Access: R/W Clear Size (in bits): 32

The IIR register contains the interrupt bits that are "unmasked" by the IMR and thus can generate CPU interrupts (if enabled via the IER). When a CPU interrupt is generated, this should be the first register to be interrogated to determine the source of the interrupt. **Writing a '1' into the appropriate bit position within this register clears interrupts**.

Bit De			scription			
31:0	Display_Engine_Interrupt_Identity_Bits					
	Project:	All				
	Format: Display Engine Interrupt Registers Bit Definition See Description					
			in this register will generate a CPU interrupt. Bits set	in this		
	the appro	priate bit(s)	the interrupt condition is "cleared" via software by writing and pending interrupt if two or more of the same interrupt.	ting a '1' to		
	the appro	priate bit(s)  bit, the IIR can store a seco	,	ting a '1' to		
	the appro	priate bit(s) " bit, the IIR can store a seco	ond pending interrupt if two or more of the same inter	ting a '1' to		



## 2.5.5 DEIER — Display Engine Interrupt Enable Register

## **DEIER** — Display Engine Interrupt Enable Register

Register Type: MMIO
Address Offset: 4400Ch
Project: All
Default Value: 00000000h
Access: R/W

Size (in bits): 32

The IER register contains an interrupt enable bit for each interrupt bit in the IIR register. A disabled interrupt will still appear in the Interrupt Identity Register to allow polling of interrupt sources.

wiii stiii app	pear in the in	iterrupt identit	y Register to allow polling of interrupt so	ources.		
Bit De			scription			
31:0	Display_Engine_Interrupt_Enable_Bits					
	Project:	All				
	Format:	Display En	gine Interrupt Registers Bit Definition	See Description Above		
	•	entity Register b propagate to the	ecomes set. The DEIER master interrupt or ne system.	ontrol bit must be set to 1 for any		
	Value Na	me	Description	Project		
	0b	Disable	Disable	All		
	1b	Enable	Enable	All		



## 2.5.6 GT Interrupt Registers Bit Definition

## **GT Interrupt Registers Bit Definition**

Project: All Size (in bits): 32

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GT interrupt bits come to display either directly on wires [DevILK] or through interrupt message 0x50200 [DevSNB]. . The DEIIR and GTIIR and PMIIR are ORed together to generate the CPU interrupt.

The GT Interrupt Control Registers all share the same bit definition from this table.

Bit De		scription			
31:10	Reserved Project: DevI	_K Format:			
9	Bit_Stream_Pipeline_Counter_E	exceeded_Notify_Interrupt			
	Project: DevILK				
	The counter threshold for the executempt hang recovery.	cution of the Bit Stream Pipeline is exceeded. Driver needs to			
7	Page_Fault				
	Project: DevILK				
	This bit is set whenever there is a pending PPGTT (page or directory) fault.				
6	Media_Decode_Pipeline_Counter_Exceeded_Notify_Interrupt				
	Project: DevILK				
	The counter threshold for the executang recovery.	cution of the media pipeline is exceeded. Driver needs to attempt			
5	Video_Decode_Command_Parser_User_Interrupt				
	Project: DevILK				
	Command Parser. Note that instru	JSER_INTERRUPT instruction is executed on the Media Decode action execution is not halted and proceeds normally. A mechanism truction is required to associate a particular meaning to a user			
4	PIPE_CONTROL_Notify_Interrupt				
	Project: DevILK				
		specified in 3D pipeline document may optionally generate an ed with a fence is completed ahead of the MSI. This ordering is not anism is used.			



	GT Interrupt Registers Bit Defini	ition				
3	Render_Command_Parser_Master_Error					
	Project: DevILK					
	When this status bit is set, it indicates that the hardware has detect upon an error condition and cleared by a CPU write of a one to the Error ID register followed by a write of a one to this bit in the IIR. If the error comes from the "Error Status Register" which along with which error conditions will cause the error status bit to be set and the error conditions will cause the error status bit to be set and the error conditions will cause the error status bit to be set and the error conditions will cause the error status bit to be set and the error conditions will cause the error status bit to be set and the error conditions will cause the error status bit to be set and the error can be expressed as the error can	e appropriate bit contained in the Further information on the source of the "Error Mask Register" determine				
	Page Table Error: Indicates a page table error.					
	<b>Instruction Parser Error</b> : The Renderer Instruction Parser encour instruction.	nters an error while parsing an				
2	Sync_Status					
	Project: DevILK					
	This bit is toggled when the Instruction Parser completes a flush win INSTPM register. The toggle event will happen after all the graphic Status DWord write resulting from this toggle will cause the CPU's coherent as well (flush and invalidate the render cache).	s engines are flushed. The HW				
0	Render_Command_Parser_User_Interrupt					
	Project: DevILK					
	This status bit is set when an MI_USER_INTERRUPT instruction is Parser. Note that instruction execution is not halted and proceeds MI_STORE_DATA instruction is required to associate a particular in	normally. A mechanism such as an				
31:0	Reserved					
31	Reserved Project: DevSNB	Format:				
29	Blitter_page_directory_faults					
	Project: DevSNB					
	This is a write of logic1 via interrupt message from GT via 0x50200 l	bit29				
28:27	Reserved Project: DevSNB	Format:				
26	Blitter_MI_FLUSH_DW_notify					
	Project: DevSNB					
	This is a write of logic1 via interrupt message from GT via 0x50200 l	bit26				
25	Blitter_Command_Streamer_error_interrupt					
	Project: DevSNB					
	This is a write of logic1 via interrupt message from GT via 0x50200 l	bit25				
24	Billter_MMIO_sync_flush_status					
	Project: DevSNB					
	This is a write of logic1 via interrupt message from GT via 0x50200 l	bit24				
23	Reserved Project: DevSNB	Format:				
22	Blitter_Command_Streamer_MI_USER_INTERRUPT					
	Project: DevSNB					
	This is a write of logic1 via interrupt message from GT via 0x50200 l					
21	Reserved Project: DevSNB	Format:				



	GT Interrupt Registers Bit Definition	l				
19	Video_page_directory_faults					
	Project: DevSNB					
	This is a write of logic1 via interrupt message from GT via 0x50200 bit19					
18	Video_Command_Streamer_Watchdog_counter_exceeded					
	Project: DevSNB					
	This is a write of logic1 via interrupt message from GT via 0x50200 bit18					
17	Reserved Project: DevSNB	Format:	MBZ			
16	Video_MI_FLUSH_DW_notify					
	Project: DevSNB					
	This is a write of logic1 via interrupt message from GT via 0x50200 bit16					
15	Video_Command_Streamer_error_interrupt					
	Project: DevSNB					
	This is a write of logic1 via interrupt message from GT via 0x50200 bit15					
14	Video_MMIO_sync_flush_status					
	Project: DevSNB					
	This is a write of logic1 via interrupt message from GT via 0x50200 bit14					
13	Reserved Project: DevSNB	Format:				
12	Video_Command_Streamer_MI_USER_INTERRUPT					
	Project: DevSNB					
	This is a write of logic1 via interrupt message from GT via 0x50200 bit12					
1:9	Reserved Project: DevSNB	Format:				
7	Render_page_directory_faults					
	Project: DevSNB					
	This is a write of logic1 via interrupt message from GT via 0x50200 bit7					
6	Render_Command_Streamer_Watchdog_counter_exceeded					
	Project: DevSNB					
	This is a write of logic1 via interrupt message from GT via 0x50200 bit6	_				
5	Reserved Project: DevSNB	Format:				
4	Render_PIPE_CONTROL_notify					
	Project: DevSNB					
	This is a write of logic1 via interrupt message from GT via 0x50200 bit4					
3	Render_Command_Streamer_error_interrupt					
	Project: DevSNB					
	This is a write of logic1 via interrupt message from GT via 0x50200 bit3.					
2	Render_MMIO_sync_flush_status					
	Project: DevSNB					
	This is a write of logic1 via interrupt message from GT via 0x50200 bit2					
0	Render_Command_Streamer_MI_USER_INTERRUPT					
U	Project: DevSNB					



#### 2.5.7 GTISR — GT Interrupt Status Register

#### GTISR — GT Interrupt Status Register

Register Type: MMIO
Address Offset: 44010h
Project: All
Default Value: 00000000h
Access: Read Only
Size (in bits): 32

The ISR register contains the non-persistent value of all interrupt status bits. The IMR register selects which of these interrupt conditions are reported in the persistent IIR (i.e., set bits must be cleared by software). Bits in the IER are used to selectively enable IIR bits to cause CPU interrupts.

scription  Is_Bits  All  GT Interrupt Registers Bit Definition See Description  In the non-persistent values of all interrupt status bits.  Description	
All  GT Interrupt Registers Bit Definition  See Description  ne non-persistent values of all interrupt status bits.	
GT Interrupt Registers Bit Definition See Description se non-persistent values of all interrupt status bits.	
ne non-persistent values of all interrupt status bits.	
<u> </u>	
Description	
	Project
Doesn't Exist Interrupt Condition currently does not exist	All
n Exists Interrupt Condition currently exists	All
Condition	, ,

#### 2.5.8 GTIMR — GT Interrupt Mask Register

to sample these conditions.

# Register Type: MMIO Address Offset: 44014h Project: All Default Value: FFFFFFFF

Default Value: FFFF Access: R/W Size (in bits): 32

The IMR register is used by software to control which Interrupt Status Register bits are "masked" or "unmasked". "Unmasked" bits will be reported in the IIR, possibly triggering a CPU interrupt, and will persist in the IIR until cleared by software. "Masked" bits will not be reported in the IIR and therefore cannot generate CPU interrupts.

For command streamer interrupts DO NOT use this register to mask interrupt events. Instead use the individual command streamer MASK bits.



		GTIMR	— GT Interrupt Mask Regist	er				
Bit De		scription						
31:0	GT_Interrupt_Mask_Bits							
	Project:	All						
	Format: GT Interrupt Registers Bit Definition See Description Above							
	This field	contains a bit mask	which selects which interrupt bits from the	ne ISR are reported in the IIR.				
	Value N	a me	Description	Project				
	0b	Not Masked	IIR All					
	1b	Masked	Masked – will not be reported in the	IIR All				

#### 2.5.9 GTIIR — GT Interrupt Identity Register

#### **GTIIR** — **GT Interrupt Identity Register**

Register Type: MMIO
Address Offset: 44018h
Project: All
Default Value: 00000000h
Access: R/W Clear
Size (in bits): 32

1b

Condition Detected

The IIR register contains the interrupt bits that are "unmasked" by the IMR and thus can generate CPU interrupts (if enabled via the IER). When a CPU interrupt is generated, this should be the first register to be interrogated to determine the source of the interrupt. Writing a '1' into the appropriate bit position within this register clears interrupts.

tilis regist	ci cicais	r clears interrupts.						
Bit De		scription						
31:0	GT_Inter	GT_Interrupt_Identity_Bits						
	Project:	All						
	Format:	GT Interrupt	Registers Bit Definition	See Description Ab	ove			
	IMR. If e register w	This field holds the persistent values of the interrupt bits from the ISR which are "unmasked" by the IMR. If enabled by the IER, bits set in this register will generate a CPU interrupt. Bits set in this register will remain set (persist) until the interrupt condition is "cleared" via software by writing a '1' to the appropriate bit(s).						
	Value N	Value Na me Description Pr						
	0b	Condition Not Detected	Interrupt Condition Not Detected		All			

ΑII

Interrupt Condition Detected (may or may not have

actually generated a CPU interrupt)



## 2.5.10 GTIER — GT Interrupt Enable Register

#### **GTIER** — **GT Interrupt Enable Register**

Register Type: MMIO
Address Offset: 4401Ch
Project: All

Default Value: 00000000h Access: R/W Size (in bits): 32

The IER register contains an interrupt enable bit for each interrupt bit in the IIR register. A disabled interrupt will still appear in the Interrupt Identity Register to allow polling of interrupt sources.

Bit De	scription								
31:0	GT_Interru	GT_Interrupt_Enable_Bits							
	Project:	All							
	Format:	GT In	terrupt Registers Bit Definition	on See Description	n Above				
	Interrupt Ide	The bits in this register enable a CPU interrupt to be generated whenever the corresponding bit in the nterrupt Identity Register becomes set. The DEIER master interrupt control bit must be set to 1 for any nterrupts to propagate to the system.							
	Value Na	Value Na me Description Project							
	0b	Disable	Disable		All				
	1b	Enable	Enable		All				



# 2.5.11 Power Management Interrupt Registers Bit Definition [DevSNB]

	Power Management Interrupt Registers Bit I	Definition [D	evSNB]
Project:	DevSNB		
Size(in bits	): 32		
	agement interrupt bits come to display through interrupt me	essage 0x50210	). The DEIIR and
	PMIIR are ORed together to generate the CPU interrupt.	a bit dafinitian f	romo thio toble
	Management Interrupt Control Registers all share the same	e bit definition in	om this table.
Bit De	scription		
31:26	Reserved Project: All	Format:	
25	PCU_pcode2driver_mailbox_event	Project: A	ll Format:
	This is a write of logic1 via interrupt message from PCU via 0x50	)210 bit25	
24	PCU_Thermal_Event	Project: A	ll Format:
	This is a write of logic1 via interrupt message from PCU via 0x50	)210 bit24	
23:7	Reserved Project: All	Format	::
6	Render_Frequency_Downward_Timeout_During_RC6_interest	rupt Project:	All Format:
	This is a write of logic1 via interrupt message from GT via 0x502	10 bit6	
5	RP_UP_threshold_interrupt	Project: A	II Format:
	This is a write of logic1 via interrupt message from GT via 0x502	10 bit5	
4	RP_DOWN_threshold_interrupt	Project: A	ll Format:
	This is a write of logic1 via interrupt message from GT via 0x502	10 bit4	
3	Reserved Project: All	Format	::
2	Render_geyserville_UP_evaluation_interval_interrupt	Project: A	ll Format:
	This is a write of logic1 via interrupt message from GT via 0x502	10 bit2	
1	Render_geyserville_Down_evaluation_interval_interrupt	Project: A	ll Format:
	BitFieldDesc	-	
0	Reserved Project: All	Format	: MBZ



#### 2.5.12 PMISR — PM Interrupt Status Register

#### **PMISR** — **PM Interrupt Status Register**

Register Type: MMIO
Address Offset: 44020h
Project: DevSNB
Default Value: 00000000h
Access: Read Only
Size (in bits): 32

The ISR register contains the non-persistent value of all interrupt status bits. The IMR register selects which of these interrupt conditions are reported in the persistent IIR (i.e., set bits must be cleared by software). Bits in the IER are used to selectively enable IIR bits to cause CPU interrupts.

Bit De	scription							
31:0	Power_Man	nagement_Interrupt	t_Status_Bits					
	Project: All							
ļ	Format: Po	Format: Power Management Interrupt Registers Bit Definition See Description Above						
	This field contains the non-persistent values of all interrupt status bits.							
	This field co	ntains the non-persi	istent values of all interrupt status bits					
	This field cor	ntains the non-persi	istent values of all interrupt status bits  Description		Project			
	l				Project All			

Some inputs to this register are short pulses, therefore software should not expect to use this register

# 2.5.13 PMIMR — Power Management Interrupt Mask Register

to sample these conditions.

# PMIMR — Power Management Interrupt Mask Register Register Type: MMIO Address Offset: 44024h Project: DevSNB Default Value: FFFFFFFh Access: R/W Size (in bits): 32

The IMR register is used by software to control which Interrupt Status Register bits are "masked" or "unmasked". "Unmasked" bits will be reported in the IIR, possibly triggering a CPU interrupt, and will persist in the IIR until cleared by software. "Masked" bits will not be reported in the IIR and therefore cannot generate CPU interrupts.

For power management interrupts DO NOT use this register to mask interrupt events. Instead use the individual power management MASK bits in the corresponding PMunit register space.



Bit De	scription						
31:0	Power_Management_Interrupt_Mask_Bits						
	Project: All						
	Format: Po	Format: Power Management Interrupt Registers Bit Definition See Description Above					
	This field contains a bit mask which selects which interrupt bits from the ISR are reported in the IIR.						
	This field co	ntains a bit mask	which selects which interrupt bits from t	he ISR are reported in the IIR			
	This field co	ntains a bit mask <b>me</b>	which selects which interrupt bits from t	he ISR are reported in the IIR  Project			
			·	Project			

## 2.5.14 PMIIR — Power Management Interrupt Identity Register

	PMIIR — Power Management Interrupt Identity Register
Register Type:	MMIO
Address Offset:	44028h
Project:	DevSNB
Default Value:	0000000h
Access:	R/W Clear
Size (in bits):	32
The IIR register of	contains the interrupt bits that are "unmasked" by the IMR and thus can generate CPU

The IIR register contains the interrupt bits that are "unmasked" by the IMR and thus can generate CPU interrupts (if enabled via the IER). When a CPU interrupt is generated, this should be the first register to be interrogated to determine the source of the interrupt. Writing a '1' into the appropriate bit position within this register clears interrupts.

interrogated this registe			of the interrupt. Writing a '1' into the appro	priate bit position within				
Bit De			scription					
31:0	Power_M	Power_Management_Interrupt_Identity_Bits						
	Project:	Project: All						
	Format: Power Management Interrupt Registers Bit Definition See Description Above							
	This field holds the persistent values of the interrupt bits from the ISR which are "unmasked" by the IMR. If enabled by the IER, bits set in this register will generate a CPU interrupt. Bits set in this register will remain set (persist) until the interrupt condition is "cleared" via software by writing a '1' to the appropriate bit(s).							
	conditions	For each bit, the IIR can store a second pending interrupt if two or more of the same interrupt conditions occur before the first condition is cleared. Upon clearing the interrupt, the IIR bit will momentarily go low, then return high to indicate there is another interrupt pending.						
	Value Na me Description Project							
	0b	IC No Detect	Interrupt Condition Not Detected	All				
	1b	IC Detect	Interrupt Condition Detected (may or may not ha actually generated a CPU interrupt)	ave All				



ΑII

#### 2.5.15 PMIER — Power Management Interrupt Enable Register

PMIER — Power Management Interrupt Enable Register

Register Type: MMIO
Address Offset: 4402Ch
Project: DevSNB
Default Value: 00000000h
Access: R/W
Size (in bits): 32

1b

The IER register contains an interrupt enable bit for each interrupt bit in the IIR register. A disabled interrupt will still appear in the Interrupt Identity Register to allow polling of interrupt sources.

Bit		Description						
31:0	Power Man	agement Interru	ıpt Enable Bits					
	Project: All							
	Format: Po	Format: Power Management Interrupt Registers Bit Definition See Description Above						
	Interrupt Ide	The bits in this register enable a CPU interrupt to be generated whenever the corresponding Interrupt Identity Register becomes set. The DEIER master interrupt control bit must be set any interrupts to propagate to the system.						
	Value Na	me	Description	Project				
	Oh	Disable	Disable	All				

Enable

## 2.5.16 Port Hot Plug Control Register

Enable

	Digital Port Hot Plug Control Register					
Register Ty	pe: MMIO					
<b>Address Off</b>	set: 44030h					
Project:	All					
Default Valu	Default Value: 00000000h					
Access:	R/W					
Size (in bits	): 32					
Bit De			sc	ription		
31:5	Reserved F	Project: /	All	Format:		



#### **Digital Port Hot Plug Control Register**

4 Digital\_Port\_A\_Hot\_Plug\_Detect\_Input\_Enable

Project: All Default Value: 0b

Controls the state of the HPD buffer for the digital port. The buffer state is independent of whether the port is enabled or not.

Value N	a me	Description	Project
0b	Disable	Buffer disabled	All
1b	Enable	Buffer enabled. Hot plugs bit reflect the electrical state of the HPD pin	All

3:2 Digital\_Port\_A\_Hot\_Plug\_Short\_Pulse\_Duration

Project: All Default Value: 0b

These bits define the duration of the pulse defined as a short pulse.

Value Na	me	Description	Project
00b	2ms	2 ms	All
01b	4.5ms	4.5 ms	All
10b	6ms	6 ms	All
11b	100ms	100 ms	All

1:0 Digital\_Port\_A\_Hot\_Plug\_Interrupt\_Detect\_Status

Project: All

Access: R/W Clear

Default Value: 0b

This reflects hot plug detect status on the digital port. This bit is used for either monitor hotplug/unplug or for notification of a sink event. When either a long or short pulse is detected, one of these bits will set. These bits are ORed together to go to the main ISR hotplug register bit. These are sticky bits, cleared by writing 1s to them.

Value Na	me	Description	Project
00b	Not Detected	Digital port hot plug event not detected	All
1Xb	Long Pulse	Digital port long pulse hot plug event detected	All
X1b	Short Pulse	Digital port short pulse hot plug event detected	All



# 2.5.17 GTT Fault Status Register

		GTT F	ault	Status Register		
Register Ty Address O' Project: Default Val Access: Size (in bit	ffset: 44040 All ue: 00000 R/W 0	0h 0000h				
Bit De	scription					
31:8	Reserved	Project: All		Format	::	
7	Project: Default Value This is a stite main IS	cky bit, cleared by writing		All the GTT Fault Status bits are ORenes to display either directly on a wire		
	Value Na	me	Desc	ription	Project	
	0b	Not Detected	Even	t not detected	All	
	1b	Detected	Even	t detected	All	
6	Project: Default Value This is a stite main IS	cky bit, cleared by writing R GTT Fault bit. This eve	ent com	All the GTT Fault Status bits are ORenes to display either directly on a wire for directly on a wire ILK] or through me	or through message	
	Value Na	me	Desc	ription	Project	
	0b	Not Detected	Even	t not detected	All	
	1b	Detected	Even	t detected	All	
5	Project: Default Valu This reflects	GTT fault status for this		This is a sticky bit, cleared by writing the main ISR GTT Fault bit.	1 to it. All the GTT	
	Value Na	me		Description	Project	
	0b	Not Detected		Event not detected	All	
	1b	Detected		Event detected	All	



#### **GTT Fault Status Register**

#### 4 Cursor\_A\_GTT\_Fault\_Status

Project: All Default Value: 0b

This reflects GTT fault status for this plane. This is a sticky bit, cleared by writing 1 to it. All the GTT Fault Status bits are ORed together to go to the main ISR GTT Fault bit.

Value Na	me	Description	Project
0b	Not Detected	Event not detected	All
1b	Detected	Event detected	All

#### 3 Sprite\_B\_GTT\_Fault\_Status

Project: All Default Value: 0b

This reflects GTT fault status for this plane. This is a sticky bit, cleared by writing 1 to it. All the GTT Fault Status bits are ORed together to go to the main ISR GTT Fault bit.

Value Na	me	Description	Project
0b	Not Detected	Event not detected	All
1b	Detected	Event detected	All

#### 2 Sprite\_A\_GTT\_Fault\_Status

Project: All Default Value: 0b

This reflects GTT fault status for this plane. This is a sticky bit, cleared by writing 1 to it. All the GTT Fault Status bits are ORed together to go to the main ISR GTT Fault bit.

Value Na	me	Description	Project
0b	Not Detected	Event not detected	All
1b	Detected	Event detected	All

#### 1 Primary\_B\_GTT\_Fault\_Status

46

Project: All Default Value: 0b

This reflects GTT fault status for this plane. This is a sticky bit, cleared by writing 1 to it. All the GTT Fault Status bits are ORed together to go to the main ISR GTT Fault bit.

Value Na	me	Description	Project
0b	Not Detected	Event not detected	All
1b	Detected	Event detected	All



GTT Fault Status Register						
0	Primary_A_	GTT_Fault_Sta	atus			
	Project:	Α	.II			
	Default Valu	Default Value: 0b				
	This reflects GTT fault status for this plane. This is a sticky bit, cleared by writing 1 to it. All the GTT Fault Status bits are ORed together to go to the main ISR GTT Fault bit.					
						1 to it. All the GTT
						1 to it. All the GTT  Project
	Fault Status	bits are ORed t		o the main ISR GTT Fault b		<u> </u>

# 2.6 Display Engine Render Response

# 2.6.1 Display Engine Render Response Message Bit Definition

Display Engine Render Response Message Bit Definition						
Project:	DevSNB					
Size(in bits	): 32					
	gine (DE) render response message bits come from events v gine Render Response Message Registers all share the sam					
Bit De	scription					
31:14	Reserved Project: All			Format:	MBZ	
13	Pipe_B_Start_of_Horizontal_Blank_Event	Project:	All	Format:		
	This even will be reported on the start of the Pipe B Horizontal Bla	ank.				
12	Reserved Project: All			Format:	MBZ	
11	Pipe_B_Start_of_Vertical_Blank_Event	Project:	All	Format:		
	This even will be reported on the start of the Pipe B Vertical Blank	ζ.				
10	Pipe_B_Sprite_Plane_Flip_Done_Event	Project:	All	Format:		
	This even will be reported on the completion of a flip for the Pipe I	B Sprite Plan	ne.			
9	Pipe_B_Primary_Plane_Flip_Done_Event	Project:	All	Format:		
	This even will be reported on the completion of a flip for the Pipe I	B Primary Pla	ane.			
8	Pipe_B_Scanline_Event	Project:	All	Format:		
	This even will be reported on the start of the scan line specified in Range Compare Register.	the Pipe B [	Display	Scan Line	Count	
7:6	Reserved Project: All			Format:	MBZ	
5	Pipe_A_Start_of_Horizontal_Blank_Event	Project:	All	Format:		
	This even will be reported on the start of the Pipe A Horizontal Bla	ank.				



	Display Engine Render Response N	lessage Bit Det	initio	on	
4	Reserved Project: All			Format:	MBZ
3	Pipe_A_Start_of_Vertical_Blank_Event	Project:	All	Format:	
	This even will be reported on the start of the Pipe A Verti	ical Blank.			
2	Pipe_A_Sprite_Plane_Flip_Done_Event	Project:	All	Format:	
	This even will be reported on the completion of a flip for	the Pipe A Sprite Plan	ie.		
1	Pipe_A_Primary_Plane_Flip_Done_Event	Project:	All	Format:	
	This even will be reported on the completion of a flip for	the Pipe A Primary Pla	ane.		
0	Pipe_A_Scanline_Event	Project:	All	Format:	
	This even will be reported on the start of the scan line sp Range Compare Register.	pecified in the Pipe A [	Display	Scan Line	Count

# 2.6.2 DERRMR — Display Engine Render Response Mask Register

#### **DERRMR** — Display Engine Render Response Mask Register

Register Type: MMIO
Address Offset: 44050h
Project: DevSNB
Default Value: FFFFFFFh

Access: R/W Size (in bits): 32

48

This register is used by software to control which render response message bits are "masked" or "unmasked". "Unmasked" bits will cause a render response message to be sent and will be reported in that message. "Masked" bits will not be reported and will not cause a render response message to be sent.

message.	"Masked"	Masked" bits will not be reported and will not cause a render response message to be sent.				
Bit De		scription				
31:0	Project: Format: This field	All Display Engine Rende	oonse_Message_Mask_Bits  Pr Response Message Bit Definition See  nich selects which events cause and are reported i	Description Above n the render		
	Value N	a me	Description	Project		
	0b	Not Masked	Not Masked – will be cause and be reported in the message	All		
	1b	Masked	Masked – will not cause or be reported in the	All		

Doc Ref #: IHD\_OS\_V3Pt2\_3\_10

message



# 2.7 Display Arbitration Control

# 2.7.1 DISP\_ARB\_CTL—Display Arbiter Control

		DISP_	ARB_C	TL—Display Arbiter Control	
Register Ty	pe: MMIO				
Address Of	-				
Project: All					
Default Val	ue: C22406	22h			
Access:	R/W				
Size (in bits	•				
Trusted Type: 1					
Bit De				scription	
31	FBC_Memory	_Wake			
	Project:		All		
	Security:		Test		
	Default Value:		1b		
	Setting this bit allows FBC compressed write requests to wake memory from SR (default: on)				
30	KVMr_Memory_Wake				
	Project:		All		
	Security:		Test		
	Default Value:		1b		
	Setting this bit	allows KVI	∕Ir display v	write back requests to wake memory from SR. (default: on)	
29	Opportunistic	_Fetch_M	ode_Enabl	e	
	Project:		All		
	Security:		Test		
	Default Value:		0b		
		em from Se	lfRefresh.	ata fetches (even when above watermark) when other clients For any opportunistic fetch to happen, display should not be in the	
28	Reserved	Project:	All	Format:	
27:26	HP_Queue_W	/atermark			
	Project:		All		
	Default Value:		00b		



#### **DISP\_ARB\_CTL—Display Arbiter Control**

25:24 LP\_Write\_Request\_Limit

Project: All

Default Value: 10b 4

The value in this register indicates the maximum number of back to back LP write requests that will be accepted from a single client before re-arbitrating.

Value Na	me	Description	Project
00b	1	1	All
01b	2	2	All
10b	4	4 (default)	All
11b	8	8	All

23:20 TLB\_Request\_Limit

Project: All

Default Value: 0010b 2

Range: 1..15

The value in this register indicates the maximum number of TLB requests that can be made in an arbitration loop. Range 1 - 15, (default 2). Zero is not a valid programming.

19:16 TLB\_Request\_In-Flight\_Limit

Project: All

Default Value: 0100b 4

Range: 1..15

The value in this register indicates the maximum number of TLB (or VTd) requests that can be in flight at any given time. Range 1 – 15, (default 4). Zero is not a valid programming.

15 FBC\_Watermark\_Disable

Project: All
Security: Test
Default Value: 0b

Setting this bit disables the FBC watermarks.

[ILK, This bit must be set to 1 for all steppings.

14:13 Address\_Swizzling\_for\_Tiled-Surfaces

Project: All Default Value: 00b

DRAM configuration registers show if memory address swizzling is needed.

Value Na	me	Description	Project
00b	No Display	No display request address swizzling	All
01b	Enable	Enable display request address bit[6] swizzling for tiled surfaces	All
1Xb	Reserved	Reserved	All



12	Reserved Proje	ect: All		Format:			
1:8	HP_Page_Break_Li	mit					
	Project:	All					
	Default Value:	0110b	6				
	Range:	115					
		The value in this register represents the maximum number of page breaks allowed in a HP request chain. Range 1 – 15, (default 6). Zero is not a valid programming.					
7	Reserved Proj	ect: All		Format:			
6:0	HP_Data_Request_	Limit					
	Project:	All					
	Default Value:	01000010b	34				
	Range:	1127					

# 2.7.2 DISP\_ARB\_CTL2—Display Arbiter Control 2 [DevSNB]

		DISP_ARB	_CTL2—Dis	play Arbiter Control 2 [DevSNB]
Register Ty	уре:	MMIO		
Address O	ffset:	45004h		
Project:		DevSNB		
Default Val	lue:	00000000h		
Access:		R/W		
Size (in bit	s):	32		
Bit De				scription
31:9	Rese	rved Project	t: All	Format:
8	Fetch	_Timing		
	Proje	ct:	All	
	Defau	ılt Value:	0b	
	regist	er is used to spec	rify when an oppo	en Opportunistic Fetches are enabled. The value in this rtunistic fetch can happen. For any opportunistic fetch to cess of waking the system.
	Valu	ıe Na me	Description	Project
	0b	FE inSR	Fetch on falli	ng edge of inSR All
	1b	Not inSR	Fetch when r	ot inSR All



#### DISP\_ARB\_CTL2—Display Arbiter Control 2 [DevSNB]

7 Opportunistic\_Fetch\_Behavior

Project: All Default Value: 0h

The value in this register is valid only when Opportunistic Fetches are enabled. The value in this register represents the fetch behavior when an opportunistic fetch is triggered. For any opportunistic fetch to happen, display should not be in the process of waking the system.

Ī	Value Na	me	Description	Project
	0h	One Burst	One Burst Only	All
	1h	Fill FIFO	Fill FIFO to Top	All

6 Reserved Project: All Format: MBZ

5:4 Inflight\_HP\_Read\_Request\_Limit

Project: All Default Value: 00b

The value in this register represents the maximum number of HP read request transactions that can inflight at any given time.

Value Na	me	Description	Project
00b	128 HP	128 HP inflight transactions limit	All
01b	64 HP	64 HP inflight transactions limit	All
10b	32 HP	32 HP inflight transactions limit	All
11b	16 HP	16 HP inflight transactions limit	All

3:2 Reserved Project: All Format:

1:0 RTID\_FIFO\_Watermark

52

Project: All Default Value: 0b

The value in this register represents the watermark value for the RTID FIFO. HP transactions will start only when the FIFO level is above or equal the watermark

Value N	a me	Description	Project
00b	8 RTIDs	8 RTIDs available in FIFO	All
01b	16 RTIDs	16 RTIDs available in FIFO	All
10b	32 RTIDs	32 RTIDs available in FIFO	All
11b	RESERVED	Reserved	All



#### 2.8 Display Watermark Registers

The watermark registers are used to control the display to memory request timing. The watermarks must be programmed according to the rules provided in the "Programming Watermarks" document. The default values of the watermarks should allow the display to operate in any mode supported by the memory configuration. However, the default watermarks are not optimized for power or memory bandwidth efficiency. Watermarks must enable from the bottom up, meaning if WM2 is disabled, WM3 must also be disabled, and if WM1 is disabled, both WM2 and WM3 must also be disabled. Watermark latency values must increase from the bottom up, meaning WM1 (if enabled) must have higher latency than WM0, and so on. [ILK] The low power 1 display watermark register latency value must be programmed to match the Memory Latency Timer Register (MLTR, MCHBAR BDF 0:0:0, Offset 0x1222) Self Refresh Latency Time microsecond value, and the low power 2 display watermark register latency value must be programmed to match the Memory Latency Timer Register MPLL Shutdown Latency Time microsecond value.

#### 2.8.1 WM0\_PIPE\_A—Pipe A Main Watermarks

		WM0_	PIPE_A	—Pipe A Main Watermarks	
Register Ty	/pe: MMIO				
Address Of	ffset: 45100h	า			
Project:	All				
Default Val	ue: 007838	318h			
Access:	R/W				
Size (in bits	s): 32				
Bit De				scription	
31:23	Reserved	Project:	All	Format:	
22:16	Pipe_A_Prin	nary_Waterm	ark	Project:	All
	Number in 64 memory	4Bs of data in	FIFO belo	w which the Pipe A Primary stream will generate requests to	
15:14	Reserved	Project:	All	Format:	
13:8	Pipe_A_Spri	ite_Waterma	·k	Project:	All
	Number in 64 memory	4Bs of data in	FIFO belo	w which the Pipe A Sprite stream will generate requests to	
7:5	Reserved	Project:	All	Format:	
4:0	Pipe_A_Cur	sor_Waterma	ırk	Project:	All
	Number in 64 memory	4Bs of data in	FIFO belo	w which the Pipe A Cursor stream will generate requests to	



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# 2.8.2 WM0\_PIPE\_B—Pipe B Main Watermarks

		WM0_	PIPE_B-	–Pipe B Main Watermarks	
Register Ty	ype: MMIO				
Address O	ffset: 45104h	า			
Project:	All				
<b>Default Val</b>	ue: 007838	318h			
Access:	R/W				
Size (in bit	s): 32				
Trusted Ty	pe: 1				
Bit De				scription	
31:23	Reserved	Project:	All	Format:	
22:16	Pipe_B_Prir	nary_Waterm	nark	Project:	All
	Number in 64 memory	4Bs of data in	FIFO belov	which the Pipe B Primary stream will generate requests to	
15:14	Reserved	Project:	All	Format:	
13:8	Pipe_B_Spr	ite_Waterma	rk	Project:	All
	Number in 64 memory	4Bs of data in	FIFO belov	which the Pipe B Sprite stream will generate requests to	
7:5	Reserved	Project:	All	Format:	
4:0	Pipe_B_Cur	sor_Waterma	ark	Project:	All
	Number in 64 memory	4Bs of data in	FIFO belov	which the Pipe B Cursor stream will generate requests to	



#### 2.8.3 WM1—Low Power 1 Display Watermarks

WM1—Low Power 1	l Display Watermark	(S
-----------------	---------------------	----

Register Type: MMIO
Address Offset: 45108h
Project: All
Default Value: 00000000h
Access: R/W
Size (in bits): 32

These watermark values will be used only when one pipe is enabled and no sprites are enabled (or the conditions for using the Low Power 1 Sprite Watermark are met) and the display is in LP1 state.

				, , ,		
Bit De				scription		
31	Enabled				Project:	All
	Enables LP1	watermarks				
30:24	Latency				Project:	All
	The latency a	associated wit	h the LI	P1 watermarks in half usecs.		
23:20	FBC_LP1_W	/atermark			Project:	All
	Number of ed	quivalent lines	of the	primary display for this WM		
19:17	Reserved	Project:	All	Format:		
16:8	LP1_Primary	y_Watermark	(		Project:	All
	Number in 64	Bs of data in	FIFO b	elow which the Primary stream will generate reques	ts to memo	ory.
7:6	Reserved	Project:	All	Format:		
5:0	LP1_Cursor	_Watermark			Project:	All
	Number in 64	1Bs of data in	FIFO b	elow which the Cursor stream will generate request	s to memor	у.

#### 2.8.4 WM2—Low Power 2 Display Watermarks

#### WM2—Low Power 2 Display Watermarks

Register Type: MMIO
Address Offset: 4510Ch
Project: All
Default Value: 00000000h
Access: R/W
Size (in bits): 32

These watermark values will be used only when one pipe is enabled and no sprites are enabled and the display is in LP2 state.



	WM2—Low Power 2 Display Waterman	rks	
Bit De	scription		
31	Enabled	Project:	All
	Enables LP2 watermarks		
30:24	Latency	Project:	All
	The latency associated with the LP2 watermarks in half usecs.		
23:20	FBC_LP2_Watermark	Project:	All
	Number of equivalent lines of the primary display for this WM		
19:17	Reserved Project: All	Format:	
16:8	LP2_Primary_Watermark	Project:	All
	Number in 64Bs of data in FIFO below which the Primary stream will ger	nerate requests to memo	ory.
7:6	Reserved Project: All	Format:	
5:0	LP2_Cursor_Watermark	Project:	All
	Number in 64Bs of data in FIFO below which the Cursor stream will gen	erate requests to memor	y.

# 2.8.5 WM3—Low Power 3 Display Watermarks

	WM3—Low Power 3 Display Waterma	
Register Ty	••	
	ffset: 45110h	
Project:	All	
Default Val		
Access:	R/W	
Size (in bit	s): 32	
	ermark values will be used only when one pipe is enabled and no	sprites are enabled and the
display is ir	LP3 state.	
Bit De	scription	
31	Enabled	Project: All
	Enables LP3 watermarks	
30:24	Latency	Project: All
	The latency associated with the LP3 watermarks in half usecs.	
23:20	FBC_LP3_Watermark	Project: All
	Number of equivalent lines of the primary display for this WM	
19:17	Reserved Project: All	Format:
16:8	LP3_Primary_Watermark	Project: All

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	WM3—Low Power 3 Display Watermarks						
5:0	LP3_Cursor_Watermark	Project:	All				
	Number in 64Bs of data in FIFO below which the Cursor stream will generate reque	ests to memor	y.				

# 2.8.6 WM1S—Low Power 1 Sprite Watermark

	WM1S—Low Power 1 Sprite Watermark
Register Ty	pe: MMIO
Address O	
Project:	All
<b>Default Val</b>	ue: 00000000h
Access:	R/W
Size (in bit	): 32
	nark will be used only when one pipe is enabled and a sprite is enabled and sprite scaling is not if the display is in LP1 state.
Bit De	scription
31	Enabled Project: All
	Enables LP1 Sprite watermark. This bit allows memory self refresh to be entered when sprite is enabled.
30:8	Reserved Project: All Format:
7:0	LP1_Sprite_Watermark
	Project: All
	Default Value: 0b
	Number in 64Bs of data in FIFO below which the Sprite stream will generate requests to memory.



# 2.9 Refresh Rate Hardware Control Register

# 2.10 Display Clock Control Registers (46000h-461FFH)

## 2.10.1 FDIPLL0 — Flexible Display Interface PLL BIOS 0 [DevILK]

	FDIPLL0 - Flexible Display Interface PLL BIOS 0						
			kible Display II	iterrace Fi			
Register Ty	-	MMIO					
Address O	nset:	46000h					
Project:		DevILK					
Security: Default Val		Test 082B3019	h				
Access:	ue.	R/W	П				
Size (in bits	e)·	R/W 32					
•	Buffer Update Point: Write of 1 to FDI PLL Frequency Change Request						
Boubio Bui	CLKCNTL [13] can force an immediate update to FDI PLL but PLL may unlock.					may unlock.	
Flexible Dis	Flexible Display Interface PLL BIOS 0						
Bit De	Bit De scription						
31	Reference_clock_select(REFCLKSEL)						
	Project:	All					
	Default Valu	e: 0b					
	Ref Clock S	elect. In CTM (HVM	) register output is in	verted.			
	Value Na	me	Description				Project
	0b	PXP PLL	From PXP PLL (ab	utdrefclkpxpin	)		All
	1b	IO pads	From IO pads : ipl_	trefclkinn / ipl_	_trefc	lkinp	All
30:28	Reserved	Project: All				Format:	
27:24	Spare_inpu	ts_to_PLL(SPARE)	)	Project:	All	Default Value:	1000b
	Spare inputs	s to PLL					
	io_dlk_dlpll_	_odpllsparein[4:1]					
	io_dlk_dlpll_	odpllsparein[6:5] go	to "DT"				
23:16	Common_C	Clock_Count(COMC	CLKCNT)	Project:	All	Default Value:	00101011b
	Number of c	locks in one commo	n clock period				
	You really c	an't change this valu	ue as the common clo	ock is set by P	WRC	OK.	
	Changing th	is register mid count	would be bad.				
15	Reserved	Project: All				Format:	



#### FDIPLL0 - Flexible Display Interface PLL BIOS 0

14:12 CD\_frequency\_divider(CDFREQDIV)

Project: All

Default Value: 011b div 6

CD freq divider. Div 2 connected VSS.

Value Na	me	Description	Project
000b	div 3	div 3	All
001b	div 4	div 4	All
010b	div 5	div 5	All
011b	div 6	div 6	All
100b	div 7	div 7	All
101b	div 8	div 8	All
110b	div 9	div 9	All
111b	div 10	div 10	All

11:10 **Reserved** Project: All Format:

9:8 Ref\_clock\_divider(REFCLKDIV)

Project: All Default Value: 00b

Ref clock divider.

Value Na	me	Description	Project
00b	div 1	div 1	All
01b	div 2	div 2	All
10b	div 3	div 3	All
11b	div 4	div 4	All

7:0 Feedback\_Clock\_Divider(FBCLKDIV) Project: All Default Value: 00011001b

FB clock divider.

ref clk (100mhz) \* fb = vco

"FB clock divider" + 2 = fb

19 h = 25 + 2 = 27

27 \*100 = 2700 ps VCO



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# 2.10.2 FDIPLL1 — Flexible Display Interface PLL BIOS 1 [DevILK]

		FDIPLL1 -	Flexible Displ	ay Interface PLL BIOS 1	
Register Ty	ype: MMIO				
Address O	ffset: 46004	h			
Project:	DevIL	K			
Security:	Test				
<b>Default Val</b>	ue: 00000	000h			
Access:	R/W				
Size (in bit					
Flexible Dis	splay Interfac	ce PLL BIOS	1		
Bit De				scription	
31:13	Reserved	Project:	All		Format:
12:8	Monitor_Po	rt_Mux_Select	(MONPORTMUXS	EL)	Project: All
	Monitor Port Mux Select				
7:3	Reserved	Project:	All	Format	:
2	Monitor_Mux_Select_1(MONMUXSEL1)				
	Project: All				
	Default Value: 0b				
	monitor mux				
	monitor muz	C Select 1			
	Value Na	me	Description		Project
	0b	abutment	abutment		All
	1b	local	local		All
1	Monitor Mu	ıx_Select_0(M	ONMUXSEL0)		
	Project:	`	, M		
	Default Valu	-	 b		
	monitor mux				
		C Select 0	1		,
	Value Na	me	Description		Project
	0b	abutment	abutment		All
	1b	local	local		All
0	_	ort_Bias_Enabl Bias Enable	e(MONBIASEN)		Project: All



# 2.10.3 FDIPLL2 — Flexible Display Interface PLL BIOS 2 [DevILK]

	FDIPLL2 - Flexible Display Interface PLL BIOS 2		
Register Ty	/pe: MMIO		
Address O			
Project:	DevILK		
Security:	Test		
Default Val			
Access: Size (in bit	R/W s): 32		
-	ffer Update Point: Write of 1 to FDI PLL Frequency Change Request		
	CLKCNTL [13] can force an immediate update to FDI PLL but P	LL may unlo	ck.
Flexible Dis	splay Interface PLL BIOS 2	·	
Bit De	scription		
31:27	Reserved Project: All	Format:	
26:24	sbpllcbtune(SBPLLCBTUNE)	Project:	All
	sbpllcbtune		
23	chp2enb(CHP2ENB)	Project:	All
	chp2enb		
22	chp1enb(CHP1ENB)	Project:	All
	chp1enb		
21:20	pherrdetsel(PHERRDETSEL)	Project:	All
	pherrdetsel		
19	fastlockenb(FASTLOCKENB)	Project:	All
	fastlockenb		
18	frcopenloop(FRCOPENLOOP)	Project:	All
	frcopenloop		
17:15	chop2thresh(CHOP2THRESH)	Project:	All
	chop2thresh		
14	vclksel(VCLKSEL) Project: All		
	vclksel		
13	sleepcnt(SLEEPCNT)	Project:	All
	sleepcnt		
12:11	startuprate(STARTUPRATE)	Project:	All
	startuprate		
10:9	lockcount(LOCKCOUNT)	Project:	All
	lockcount		
8:6	startupvref(STARTUPVREF)	Project:	All
	startupvref		



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	FDIPLL2 - Flexible Display Interface PLL BIOS 2					
5:3	lockthresh(LOCKTHRESH)	Project:	All			
	lockthresh					
2:0	chop1thresh(CHOP1THRESH)	Project:	All			
	chop1thresh					

# 2.10.4 DPPLL0 —display port PLL BIOS 0 [DevILK]

		DPPLL0 - dis	splay po	rt PLL BIO	S 0			
Register Ty	ype:	MMIO						
Address O	ffset:	4600Ch						
Project:		DevILK						
Security:		Test						
<b>Default Val</b>	ue:	0007012Bh						
Access:		R/W						
Size (in bit	•	32						
Double But	ffer Update Point:	Write of 1 to Displa						
P 1	( DI L DIOO 0	CLKCNTL [14] car	n force an in	nmediate updat	te to I	OP PLL but F	LL n	nay unlock.
display por	t PLL BIOS 0							
Bit De			sc	ription				
31:28	Reserved Pro	ject: All				Format:		
27	FDI_Link_Calibrati	on(FDILINKCAL)	Project:	All <b>Default</b>		Value:	0b	
	A-step reset to 1 ar	nd no function. B-ste	p and beyor	nd, reset to 0 a	nd fui	nction listed l	oelow	<i>I</i> .
	TX curcal far-end RX DC term enable; assert to 1 when far-end RX termination has vss-termination turned on during per-lane calibration for PEG & FDI, 0 in system and 1 on tester; for ILK DMI this is							
	hard-coded internal	to the AFE to a 1; fo	r Pineview [	DMI, 0 in syster	m and	d 1 on tester.		
26:24	Spare_inputs_to_F	PLL(SPARE)		Project:	All	Default Val	ue:	000b
	FDI link is calbrated	with DMI specific co	nditions. Bit	: 27				
23:16	Common_Clock_C	ount(COMCLKCNT	)	Project:	All	Default Val	ue:	00000111b
	Common Clock Cou	unt						
	Number of clocks in	n one common clock	period.					
	You really can't cha	ange this value as the	e common c	lock is set by P	WRC	K.		
	Changing this regist	ter mid count would h	ne bad.					



DPPLL0 - display port PLL BIOS 0	<b>DPPLL0</b>	- display	port PLL	BIOS 0
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Div\_2\_of\_VCO(VCODIV2) 15

> Project: ΑII

Default Value: 0b div 6

Div 2 of VCO.

Value Na	me	Description	Project
0b	div 1	Div 1 ( 2700 mode )	All
1b	div 2	Div 2 ( 1620 mode )	All

14:10 Reserved Project: Format: ΑII

9:8 Ref\_clock\_divider(REFCLKDIV)

> Project: ΑII 01b

Default Value:

Ref clock divider.

Value Na	me	Description	Project
00b	div 1	div 1	All
01b	div 2	div 2	All
10b	div 3	div 3	All
11b	div 4	div 4	All

7:0 Feedback\_Clock\_Divider(FBCLKDIV) Project: All Default Value: 00101011b

FB clock divider.

ref clk (100mhz) \* fb = vco

"FB clock divider" + 2 = fb

2B h = 43 + 2 = 45

45 \* 2 / 120 = 2700 ps VCO

34 h = 52 + 2 = 54

54 \* 2 / 120 = 3240 ps VCO



# 2.10.5 DPPLL1 —display port PLL BIOS 1 [DevILK]

		DPPLL	1 - display port PLL BIOS 1				
Project: Security: Default Val Access: Size (in bit	ffset: 46010 DevIL Test lue: 00000 R/W	h K 000h					
Bit De			scription				
31:29	Reserved	Project: All		Format:			
28:24	Monitor_Po	rt_Mux_Select(MO : Mux Select	NPORTMUXSEL)	Project: All			
23:19	Reserved	Project: All	Form	at:			
18	Monitor_Mux_Select_1(MONMUXSEL1)  Project: All  Default Value: 0b  monitor mux select 1						
	Value Na	me	Description	Project			
	0b	abutment	abutment	All			
	1b	local	local	All			
17	17 Monitor_Mux_Select_0(MONMUXSEL0) Project: All Default Value: 0b monitor mux select 0						
	Value Na	me	Description	Project			
	0b	abutment	abutment	All			
	1b	local	local	All			
16	Monitor_Port_Bias_Enable(MONBIASEN)  Monitor Port Bias Enable  Project: Al						
15:2	Reserved	Project: All		Format:			
1	Disable_2D_DP_PLL_off/on_control(DISDPPLLOFF)  Disable 2D DP PLL off/on control  When set to 1, masks hdl_cp_dppll_en from turning off/on DP PLL						



	DPPLL1 - display port PLL BIOS 1							
0	Use_Hard_Coded_Solutions(HRDCODSOL) Project: All							
	Double Buffer Update Point: Write of 1 to DisplayPort PLL Frequency Change Request							
	Use hard coded solutions based on							
	hdl_dpa_162mhz_sel, 0 (270) 1 (162)							
	Or use CP registers.							
	FB register, Div 2 of VCO will be hard coded if this bit set to 0.							
	In CTM (HVM) register output is inverted.							

# 2.10.6 DPPLL2 —display port PLL BIOS 2 [DevILK]

		DPPLL2 - display port PLL BIOS 2			
Register Ty	ype: MMIO				
Address O	ffset:	46014h			
Project:		DevILK			
Security:		Test			
<b>Default Val</b>	ue:	0000000h			
Access:		R/W			
Size (in bits	•	32			
Double But	ffer Update Point:	Write of 1 to DisplayPort PLL Frequency Change Requ			
		CLKCNTL [14] can force an immediate update to DP F	PLL but PLL may unlock		
display por	t PLL BIOS 2				
Bit De		scription			
31:27	Reserved Pro	ect: All	Format:		
26:24	sbpllcbtune(SBPL	LCBTUNE)	Project: All		
	sbpllcbtune				
23	chp2enb(CHP2EN	В)	Project: All		
	chp2enb				
22	chp1enb(CHP1EN	В)	Project: All		
	chp1enb				
21:20	pherrdetsel(PHER	RDETSEL)	Project: All		
	pherrdetsel				
19	fastlockenb(FAST	LOCKENB)	Project: All		
	fastlockenb				
18	frcopenloop(FRCC	PENLOOP)	Project: All		
	frcopenloop				



	DPPLL2 - display port PLL BIO	<b>S 2</b>
17:15	chop2thresh(CHOP2THRESH)	Project: All
	chop2thresh	
14	vclksel(VCLKSEL) Project: All Access: RW	
	vclksel	
13	sleepcnt(SLEEPCNT)	Project: All
	sleepcnt	
12:11	startuprate(STARTUPRATE)	Project: All
	startuprate	
10:9	lockcount(LOCKCOUNT)	Project: All
	lockcount	
8:6	startupvref(STARTUPVREF)	Project: All
	startupvref	
5:3	lockthresh(LOCKTHRESH)	Project: All
	lockthresh	
2:0	chop1thresh(CHOP1THRESH)	Project: All
	chop1thresh	

# 2.10.7 3DCGDIS0 — 3D Clock Gate Disable 0 [DevILK]

		3	BD CI	ock Gating Disable Format			
Project:	DevIL	DevILK					
Bit De		scription					
0	Clock_Gati	ng_Disable					
	Project:		All				
	Default Valu	ie:	0b				
	Value Na	me		Description	Project		
	0b	Enable		Clock Gating Enabled	All		
	1b	Disable		Clock Gating Disabled	All		

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#### 3DCGDIS0 - 3D Clock Gate Disable 0

Register Type: MMIO
Address Offset: 46020h
Project: DevILK
Security: Test
Default Value: 00000000h
Access: R/W
Size (in bits): 32

3D Clock G	Sate Disable 0.	This register is not reset to default values on graphics reset.
		1.41

30 svgunit_Clock_Gating_Disable Project: All Format: 3 29 svrrunit_Clock_Gating_Disable Project: All Format: 3 28 svrwunit_Clock_Gating_Disable Project: All Format: 3 27 svtsunit_Clock_Gating_Disable Project: All Format: 3 28 dapunit_Clock_Gating_Disable Project: All Format: 3 29 svrwunit_Clock_Gating_Disable Project: All Format: 3 30 svgunit_Clock_Gating_Disable Project: All Format: 3 30 svgu	3D Clock Gating Disable Format
30 svgunit_Clock_Gating_Disable Project: All Format: 3 29 svrrunit_Clock_Gating_Disable Project: All Format: 3 28 svrwunit_Clock_Gating_Disable Project: All Format: 3 27 svtsunit_Clock_Gating_Disable Project: All Format: 3 28 dapunit_Clock_Gating_Disable Project: All Format: 3 29 svrwunit_Clock_Gating_Disable Project: All Format: 3 30 svgunit_Clock_Gating_Disable Project: All Format: 3 30 svgu	3D Clock Gating Disable Format
29 svrrunit_Clock_Gating_Disable Project: All Format: 3 28 svrwunit_Clock_Gating_Disable Project: All Format: 3 27 svtsunit_Clock_Gating_Disable Project: All Format: 3 26 dapunit_Clock_Gating_Disable Project: All Format: 3 27 svtsunit_Clock_Gating_Disable Project: All Format: 3 28 svrwunit_Clock_Gating_Disable Project: All Format: 3	3D Clock Gating Disable Format
28 svrwunit_Clock_Gating_Disable Project: All Format: 3 27 svtsunit_Clock_Gating_Disable Project: All Format: 3 28 project: All Format: 3 29 project: All Format: 3 20 project: All Format: 3 20 project: All Format: 3	3D Clock Gating Disable Format
27 svtsunit_Clock_Gating_Disable Project: All Format: 3 26 dapunit_Clock_Gating_Disable Project: All Format: 3 25 rccmunit_Clock_Gating_Disable Project: All Format: 3	3D Clock Gating Disable Format
26 dapunit_Clock_Gating_Disable Project: All Format: 3 25 rccmunit_Clock_Gating_Disable Project: All Format: 3	3D Clock Gating Disable Format 3D Clock Gating Disable Format 3D Clock Gating Disable Format
25 rccmunit_Clock_Gating_Disable Project: All Format:	3D Clock Gating Disable Format 3D Clock Gating Disable Format
	3D Clock Gating Disable Format
24 rephyunit Clock Gating Disable Project: All Format:	
Topomani_orodic_outing_bloable	
23 rczmunit_Clock_Gating_Disable Project: All Format: 3	3D Clock Gating Disable Format
22 eumunit_Clock_Gating_Disable Project: All Format: 3	3D Clock Gating Disable Format
21 emmunit_Clock_Gating_Disable Project: All Format: 3	3D Clock Gating Disable Format
20 icunit_Clock_Gating_Disable Project: All Format: 3	3D Clock Gating Disable Format
19 iscmunit_Clock_Gating_Disable Project: All Format: 3	3D Clock Gating Disable Format
18 mariunit_Clock_Gating_Disable Project: All Format:	U32
[DevILK] This bit must be 1.	
17 masfunit_Clock_Gating_Disable Project: All Format: 3	3D Clock Gating Disable Format
16 mawbunit_Clock_Gating_Disable Project: All Format:	3D Clock Gating Disable Format
15 tdmunit_Clock_Gating_Disable Project: All Format: 3	3D Clock Gating Disable Format
14 mtmunit_Clock_Gating_Disable Project: All Format: 3	3D Clock Gating Disable Format
13 dgunit_Clock_Gating_Disable Project: All Format: 3	3D Clock Gating Disable Format
12 dmunit_Clock_Gating_Disable Project: All Format: 3	3D Clock Gating Disable Format
11 flunit_Clock_Gating_Disable Project: All Format: 3	3D Clock Gating Disable Format
10 <b>ftunit_Clock_Gating_Disable</b> Project: All Format: 3	3D Clock Gating Disable Format
9 plunit_Clock_Gating_Disable Project: All Format: 3	3D Clock Gating Disable Format
8 qcunit_Clock_Gating_Disable Project: All Format: 3	3D Clock Gating Disable Format
7 scunit_Clock_Gating_Disable Project: All Format: 3	3D Clock Gating Disable Format
6 siunit_Clock_Gating_Disable Project: All Format: 3	3D Clock Gating Disable Format



	3DCGDIS0 - 3E	Clock (	ate	Disable	e <b>0</b>
5	sounit_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format
4	avsunit_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format
3	iefunit_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format
2	vdiunit_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format
1	svsmunit_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format
	Bit 1 of register 0x46020 needs to be 1 fo	r DevILK B,	C and	d any other	later steppings.
0	vscunit_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format

# 2.10.8 3DCGDIS1 — 3D Clock Gate Disable 1 [DevILK]

	3DCGDIS1 - 3D	Clock (	Sate Disak	ole 1
Register Ty	ype: MMIO			
Address O	ffset: 46024h			
Project:	DevILK			
Security:	Test			
Default Val				
Access:	R/W			
Size (in bit	•			
	Sate Disable 1. This register is not rese			graphics reset.
Bits [22:21]	] also activate cp_cg3ddisavc bit 22 and	cp_cg3a	disved bit 21	
Bit De		scr	iption	
31:27	Reserved Project: All			Format:
26	eumunit_Clock_Gating_Disable	Project:	All Format	: 3D Clock Gating Disable Format
25	eumunit_Clock_Gating_Disable	Project:	All Format	: 3D Clock Gating Disable Format
24	eumunit_Clock_Gating_Disable	Project:	All Format	: 3D Clock Gating Disable Format
23	vadunit_Clock_Gating_Disable	Project:	All Format	: 3D Clock Gating Disable Format
22	vcmmunit_Clock_Gating_Disable	Project:	All Format	: 3D Clock Gating Disable Format
21	vcpmunit_acmunit_aimunit_ammunit_ Clock_Gating_Disable	Project:	All Format	: 3D Clock Gating Disable Format
20	vcrunit_vcdmunit_Clock_Gating_Disable	Project:	All Format	: 3D Clock Gating Disable Format
19	tsunit_Clock_Gating_Disable	Project:	All Format	: 3D Clock Gating Disable Format
18	gwunit_Clock_Gating_Disable	Project:	All Format	: 3D Clock Gating Disable Format
17	vfemunit_Clock_Gating_Disable	Project:	All Format	: 3D Clock Gating Disable Format
16	bcsmmunit_Clock_Gating_Disable	Project:	All Format	: 3D Clock Gating Disable Format



3DCGDIS1 - 3D	Clock C	ate	Disable	e 1
bfhmunit_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format
bfunit_bdunit_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format
clmunit_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format
gsmunit_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format
vfmunit_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format
Errata: Clock gating must always be disabled.				
vs0munit_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format
csrmunit_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format
fhmunit_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format
urbunit_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format
sfmunit_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format
hizunit_hzmemunit_Clock_Gating_Dis able	Project:	All	Format:	3D Clock Gating Disable Format
stcunit_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format
wmunit_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format
izunit_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format
psdunit_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format
svdrunit_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format
	bfhmunit_Clock_Gating_Disable bfunit_bdunit_Clock_Gating_Disable clmunit_Clock_Gating_Disable gsmunit_Clock_Gating_Disable vfmunit_Clock_Gating_Disable Errata: Clock gating must always be disabled. vs0munit_Clock_Gating_Disable csrmunit_Clock_Gating_Disable fhmunit_Clock_Gating_Disable urbunit_Clock_Gating_Disable sfmunit_Clock_Gating_Disable sfmunit_Lock_Gating_Disable hizunit_hzmemunit_Clock_Gating_Disable stcunit_Clock_Gating_Disable wmunit_Clock_Gating_Disable izunit_Clock_Gating_Disable izunit_Clock_Gating_Disable psdunit_Clock_Gating_Disable	bfhmunit_Clock_Gating_DisableProject:bfunit_bdunit_Clock_Gating_DisableProject:clmunit_Clock_Gating_DisableProject:gsmunit_Clock_Gating_DisableProject:vfmunit_Clock_Gating_DisableProject:Errata: Clock gating must always be disabled.Project:vs0munit_Clock_Gating_DisableProject:csrmunit_Clock_Gating_DisableProject:thmunit_Clock_Gating_DisableProject:urbunit_Clock_Gating_DisableProject:sfmunit_Clock_Gating_DisableProject:hizunit_hzmemunit_Clock_Gating_DisableProject:stcunit_Clock_Gating_DisableProject:wmunit_Clock_Gating_DisableProject:izunit_Clock_Gating_DisableProject:psdunit_Clock_Gating_DisableProject:psdunit_Clock_Gating_DisableProject:	bfhmunit_Clock_Gating_DisableProject:Allbfunit_bdunit_Clock_Gating_DisableProject:Allclmunit_Clock_Gating_DisableProject:Allgsmunit_Clock_Gating_DisableProject:Allvfmunit_Clock_Gating_DisableProject:AllErrata: Clock gating must always be disabled.Project:Allvs0munit_Clock_Gating_DisableProject:Allfhmunit_Clock_Gating_DisableProject:Allurbunit_Clock_Gating_DisableProject:Allsfmunit_Clock_Gating_DisableProject:Allhizunit_hzmemunit_Clock_Gating_DisableProject:Allstcunit_Clock_Gating_DisableProject:Allwmunit_Clock_Gating_DisableProject:Allizunit_Clock_Gating_DisableProject:Allpsdunit_Clock_Gating_DisableProject:Allpsdunit_Clock_Gating_DisableProject:All	bfunit_bdunit_Clock_Gating_DisableProject:All Format:clmunit_Clock_Gating_DisableProject:All Format:gsmunit_Clock_Gating_DisableProject:All Format:vfmunit_Clock_Gating_DisableProject:All Format:Errata: Clock gating must always be disabled.Project:All Format:vs0munit_Clock_Gating_DisableProject:All Format:csrmunit_Clock_Gating_DisableProject:All Format:fhmunit_Clock_Gating_DisableProject:All Format:urbunit_Clock_Gating_DisableProject:All Format:sfmunit_Clock_Gating_DisableProject:All Format:hizunit_hzmemunit_Clock_Gating_DisableProject:All Format:stcunit_Clock_Gating_DisableProject:All Format:wmunit_Clock_Gating_DisableProject:All Format:izunit_Clock_Gating_DisableProject:All Format:psdunit_Clock_Gating_DisableProject:All Format:

# 2.10.9 3DRAMCGDIS0 — 3D RAM Clock Gate Disable 0 [DevILK]

3DRAMCGDIS0 - 3D RAM Clock Gate Disable 0							
Register Ty	/pe:	MMIO					
<b>Address Of</b>	ffset:	46028h					
Project:	DevILK						
Security:		Test					
<b>Default Valu</b>	ue:	0000000h					
Access:		R/W					
Size (in bits	s):	32					
3D RAM CI	ock G	ate Disable 0.	This register is not reset to defa	ult values on graphics reset.			
Bit De			scriptio	on			
31	Bonu	ıs_bit_2	Project: All	I			
30	Bonu	ıs_bit_1	Project: All	1			



3DRAMCGDIS0 - 3D RAM Clock Gate Disable 0							
29	row2_msunit_RAM_Clock_Gating_Dis able	Project:	All	Format:	3D Clock Gating Disable Format		
28	row1_msunit_RAM_Clock_Gating_Dis able	Project:	All	Format:	3D Clock Gating Disable Format		
27	row2_gaunit _RAM_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format		
26	row1_gaunit _RAM_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format		
25	msunit_RAM_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format		
24	gvunit_RAM_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format		
23	acmunit_RAM_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format		
22	ammunit_RAM_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format		
21	bdunit_RAM_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format		
20	bfunit_RAM_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format		
19	vfmunit_RAM_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format		
18	csrmunit_RAM_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format		
17	fhmunit_RAM_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format		
16	urbunit_RAM_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format		
15	sfmunit_RAM_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format		
14	hizunit_hzmemunit_RAM_Clock_Gatin g_Disable	Project:	All	Format:	3D Clock Gating Disable Format		
13	stcunit_RAM_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format		
12	wmunit_RAM_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format		
11	izunit_RAM_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format		
10	psdunit_RAM_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format		
9	rccmunit_RAM_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format		
8	rcpbmunit_RAM_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format		
7	rczmunit_RAM_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format		
6	eumunit_RAM_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format		
5	icunit_RAM_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format		
4	iscmunit_RAM_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format		
3	mtmunit_RAM_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format		
2	dmunit_RAM_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format		
1	scunit_RAM_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format		
0	svsmunit_RAM_Clock_Gating_Disable	Project:	All	Format:	3D Clock Gating Disable Format		



# 2.10.10 FDIPLLFREQCTL — FDI PLL Frequency Control [DevILK]

	FDIPLLFREQCTL - FDI PLL Frequency Control	I					
Register Ty	rpe: MMIO						
Address Of	Address Offset: 46030h						
Project:							
Security:							
<b>Default Val</b>							
Access:	Access: R/W						
Size (in bits							
FDI PLL Fr	equency Control						
Bit De	scription						
31:25	Reserved Project: All	Format:					
24	FDI_PLL_Frequency_Change_Request(DLPLLFREQCHNG)	Project:	All				
	Frequency Change Request and Status.						
	Write of 1 to this bit starts frequency change.						
	Hardware clears to 0 when complete.						
	R/W* - Flop w/sync clear						
23:20	Reserved Project: All	Format:					
19:8	FDI_PLL_Lock_Limit_(DLPLLLOCKLMT)	Project:	All				
	# of bclks to wait for FDI PLL Lock during frequency change						
	Default value is equivalent to 10us						
7:0	FDI_PLL_Disable_Count_Limit_(DLPLLDISCNTLMT)	Project:	All				
	# of bclks to keep FDI PLL enable de-asserted during frequency change						
	Default value is equivalent to 1.02us						



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# 2.10.11DPPLLFREQCTL — display port PLL Frequency Control [DevILK]

	DPPLLFREQCTL - display port PLL Frequency Co	ntrol					
D							
Register Ty	•						
Address Of							
Project:							
Security:	Test						
Default Val							
Access:	R/W						
Size (in bits							
DisplayPort	PLL Frequency Control						
Bit De	scription						
31:25	Reserved Project: All	Format:					
24	DisplayPort_PLL_Frequency_Change_Request(DPPLLFREQCHNG)	Project: All					
	Frequency Change Request and Status.						
	Write of 1 to this bit starts frequency change.						
	Hardware clears to 0 when complete.						
	R/W* - Flop w/sync clear						
23:20	Reserved Project: All	Format:					
19:8	DisplayPort_PLL_Lock_Limit(DPPLLLOCKLMT)	Project: All					
	# of bclks to wait for DP PLL Lock during frequency change						
	default value is equivalent to 10us						
7:0	DisplayPort_PLL_Disable_Count_Limit_(DPPLLDISCNTLMT)	Project: All					
	# of bclks to keep DP PLL enable de-asserted during frequency change						
	default value is equivalent to 1.02us						



# 2.10.12FDIDPMAXPHASE — FDI/DP Max Phase [DevILK]

	EDIDDMA VDIJA CE EDI/DD Mey Dhees		
	FDIDPMAXPHASE - FDI/DP Max Phase		
Register Ty			
Address O			
Project:	DevILK		
Security:	Test		
Default Val	30. <u>2</u> 0.0		
Access:	R/W s): 32		
Size (in bits FDI/DP Ma			
Bit De	scription		
31:26	Reserved Project: All	Format:	
25:16	DP_Virtual_comclk_limit(DPCOMCLKLMT):	Project:	All
	DP Virtual comclk limit, number of dpclks equivalent to comclk period		
	Default comclk = 900ns		
	Default dpclk = 3704ps		
15:10	Reserved Project: All	Format:	
9:0	CD_Virtual_comclk_limit(CDCOMCLKLMT)	Project:	All
	CD Virtual comclk limit, number of cdclks equivalent to comclk period		
	Default comclk = 900ns		
ı	Default cdclk = 2222ps		

# 2.10.13FDIDPBONUS — FDI/DP Bonus Register [DevILK]

		FDIDPBONUS - FDI/DP Bonus Register
Register Type:	MMIO	
Address Offset:	4603Ch	
Project:	DevILK	
Security:	Test	
<b>Default Value:</b>	00000000h	
Access:	R/W	
Size (in bits):	32	
FDI/DP Bonus R	egister	



	FDIDPBONUS - FDI/DP Bonus Register				
Bit De		scription			
31:16	Bonus_Field_1(BONUS1)	Project:	All		
15:0	Bonus_Field_0(BONUS0)		Project:	All	

# 2.10.14CLKCNT — Clock Counter Register [DevILK]

		CL	CNT - Clock (	Counter Register		
Register Ty	pe: MMIO					
<b>Address Of</b>	fset: 46040h	1				
Project:	DevILK					
Security:	Test					
Default Valu	ue: 000000	000h				
Access:	R/W					
Size (in bits	s): 32					
Clock Coun	ter Register					
Bit De				scription		
31:1	Reserved	Project:	All		Format:	
0	Start_Clock_	_Counter_Mo	de(STARTCLKCNT	):	Project:	All
	Start clock co	ounter mode				

# 2.10.15CTCLKCNTRL — CT Clock Control [DevILK]

		CTCLKCNTRL - CT Clock Control
Register Type:	MMIO	
Address Offset:	46044h	
Project:	DevILK	
Security:	Test	
<b>Default Value:</b>	00000000h	
Access:	R/W	
Size (in bits):	32	
CT Clock Contro		

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			LKCNTRL - CT Clock Control		
Bit De		scription			
31:17	Reserved	Project:	All	Format:	
16	Block_2D(E	BLOCK2D)		Project:	All
	Blocks 2D fr	om gating DA or	DB clock, used in CTM mode		
15:13	Reserved	Project:	All	Format:	
12	DB_clock_d	off(DBCLKOFF)		Project:	All
11:9	Reserved	Project:	All	Format:	
8	DA_clock_off(DACLKOFF)  Turn off da clock				All
7:5	Reserved	Project:	All	Format:	
4		urce_select(DBS rce DB clock	SRCSEL)	Project:	All
	Value Na	me	Description	Project	
	0b	FDI	FDI	All	
	1b	DisplayPort	DisplayPort	All	
3:1	Reserved	Project:	All	Format:	
0		urce_select(DAS	SRCSEL)	Project:	All
	Value Na	me	Description	Project	
	0b	FDI	FDI	All	
	1b	DisplayPort	DisplayPort	All	



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# 2.11 Backlight Control and Modulation Histogram Registers

# 2.11.1 BLC\_PWM\_CTL2—Backlight PWM Control Register 2

	- RI	C PWM CTI:	2—Backlight PWM Control Register	2
Register Ty Address Or Project: Default Val Access: Size (in bits Bit De	ype: MMIO ffset: 48250 All ue: 00000 R/W	h 000h le	scription	
	This bit enal	oles the PWM count	er logic	
	Value Na	me	Description	Project
	0b	Disable	PWM disabled (drives 0 always)	All
	1b	Enable	PWM enabled	All
30	Reserved	Project: All	Format:	
29	PWM_Pipe_	_assignment		
	Project: Default Valu This bit assignust be disa	gns PWM to a pipe.	The PWM counter will run off of this pipe's PLL. ange the value of this field.	The PWM function
	Value Na	me	Description	Project
	0b	Pipe A	Pipe A	All
	1b	Pipe B	Pipe B	All
28:27	Reserved	Project: All	Format:	
26	Project: Access: Default Valu This bit will t	be set by hardware	Clear when a Phase-In interrupt has occurred. Software interrupt generation.	will clear this bit by



	BLC_	PWM_CTL	2—Backlight PWM Control Registe	r 2	
25	Phase_In_Enat	ole		Project: All	
			phase in based on the programming of the Phase hase in is completed.	In registers below.	
24	Phase_In_Interrupt_Enable Project: A				
	Setting this bit e	Setting this bit enables an interrupt to be generated when the PWM phase in is completed.			
23:16	Phase_In_time	_base			
	Project:	All			
	Default Value:	0b			
	This field determines the number of VBLANK events that pass before one increment occurs.				
	Value Na	me	Description	Project	
	0b		Invalid	All	
	01h-FFh		VBlank Count	All	
15:8	Phase_In_Cou	nt		Project: All	
	This field determines the number of increment events in this phase in. Writes to this register should only occur when hardware-phase-ins are disabled. Reads to this register can occur any time, wher the value in this field indicates the number of increment events remaining to fully apply a phase-in request as hardware automatically decrements this value. A value of 0 is invalid.				
7:0	Phase_In_Incre	ement		Project: All	
	This field indica	tes the amount	to adjust the PWM duty cycle register on each inc	rement event.	
	This is a two's complement number.				

# 2.11.2 BLC\_PWM\_CTL—Backlight PWM Control Register

	Е	3LC_PWI	/I_CTL—Back	light PWM Control Registe	r	
Register Ty	ype: MMIO	)				
Address O	ffset: 48254	<b>∔</b> h				
Project:	All					
<b>Default Val</b>	lue: 00000	)000h				
Access:	R/W					
Size (in bit	<b>s):</b> 32					
Bit De		scription				
31:16	Reserved	Project:	All	Fo	ormat:	
15:0	Backlight_l	Duty_Cycle		P	roject:	All
	This field determines the number of time base events for the active portion of the PWM backlight control. This should never be larger than the frequency field. A value of zero will turn the backlight of A value equal to the backlight modulation frequency field will be full on. This field gets updated where is desired to change the intensity of the backlight, it will take affect at the end of the current PWM cycle. This value represents the active time of the PWM stream in PCH display raw clock periods multiplied by 128.		acklight off. ted when it PWM			



# 2.11.3 BLM\_HIST\_CTL—Image Enhancement Histogram Control Register

#### **BLM\_HIST\_CTL—Image Enhancement Histogram Control Register**

Register Type: MMIO
Address Offset: 48260h
Project: All
Default Value: 00000000h
Access: R/W

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Size (in bits): 32

Bit De scription

31 Image\_Enhancement\_Histogram\_Enabled

Project: All Default Value: 0b

This bit enables the Image Enhancement histogram logic to collect data.

Value N	a me	Description	Project
0b	Disable	Image histogram is disabled	All
1b	Enable	The image histogram is enabled. When this bit is changed from a zero to a one, histogram calculations will begin after the next VBLANK of the assigned pipe.	All

30 Image\_Enhancement\_Modification\_Table\_Enabled

Project: A
Default Value 0

This bit enables the Image Enhancement modification table.

Value N	a me	Description	Project
0b	Disable	Disabled	All
1b	Enable	Enabled. When this bit is changed from a zero to a one, modifications begin after the next VBLANK of the assigned pipe.	All



29	Image Enh	ancement_Pipe_a	essianment		
23	Project:	All	assignment		
	Default Valu				
			to a pipe. IE events will be synchron disabled in order to change the value		
	Value Na	me	Description	Project	
	0b	Pipe A	Pipe A	All	
	1b	Pipe B	Pipe B	All	
28:25	Reserved	Reserved Project: All Forma			
24	Histogram	Mode Select			
	Project:	All			
	Default Valu	e: 0b			
	Value Na	me	Description	Project	
	0b	YUV	YUV Luma Mode	All	
	1b	HSV	HSV Intensity Mode	All	
23:16	Sync_to_Pl	nase_In_Count		Project: Al	
	This field inc	dicates the phase i Phase in is enable	n count number on which the Image E d.	nhancement table will be loaded if	
15	Reserved	Project: All	F	ormat:	
14:13	Enhanceme	ent_mode			
	Project:	All			
	Default Valu	e: 00b			
	Value Na	me	Description	Project	
	00b	Direct	Direct look up mode	All	
	01b	Additive	Additive mode	All	
	10b	Multiplicative	Multiplicative mode	All	
	1 1 .00				

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Setting this bit enables the double buffered registers to be loaded on the phase in count value specified instead of the next vblank.



11	Bin_Reg	Bin_Register_Function_Select						
	Project:		All					
	Default V	alue:	0b					
	This field	indicates w	hat data is being written to or read from the bin data register.					
	Value N	la me	Description	Project				
	0b	втс	Bin Threshold Count. A read from the bin data register returns that bin's threshold value from the most recent vblank load event (guardband threshold trip). Valid range for the Bin Index is 0 to 31.	All				
	1b	BIE	Bin Image Enhancement Value. Valid range for the Bin Index is 0 to 32	All				
10:7	Reserve	<b>d</b> Projec	t: All Format:					
		ister Index	- Du-	ject: All				

# 2.11.4 Image Enhancement Bin Data Register

	Image Enh	ancement	t Bin Data Register(F0	Threshold Count	Usage)	
Register Type: MMIO						
Address O	ffset:	48264	4h			
Project:		All				
Exists If:		BLM_I	_HIST_CTL:Bin Register Function	n Select = 0		
Default Val	ue:	00000	0000h			
Access:		Read (	Only			
Size (in bit	s):	32				
ind the Bin	Register Inde	ex.	the correct register by progra this Function is Read Only	mming the Bin Registe	er Function	Select
Bit De			scription			
31	Busy_Bit				Project:	All
	If set, the eng	ine is busy, th	he rest of the register is undefine	d. If clear, the register c	ontains valid	d data.
30:22	Reserved	Project:	All	Format:		•
21:0	Bin_Count				Project:	All
	The total number	per of pixels in	n this bin, value is updated at the	start of each vblank.		



#### Image Enhancement Bin Data Register(F1 Image Enhancement Usage)

Register Type: MMIO
Address Offset: 48264h
Project: All

Exists If: BLM\_HIST\_CTL:Bin Register Function Select = 1

 Default Value:
 00000000h

 Access:
 R/W

 Size (in bits):
 32

Double Buffer Update Point: Next vblank if in normal mode, or on phase in Sync event frame if it is enabled

Writes to this address are steered to the correct register by programming the Bin Register Function Select and the Bin Register Index.

Function 1 usage (Image Enhancement) this Function is Read/Write

Bit De				scription
31:10	Reserved	Project:	All	Format:
9:0	Image_Bin_	Correction_F	actor	Project: All
	normal mode	e, or on the ph	nase in Sy	rites to this register are double buffered on the next vblank if in vnc event frame if it is enabled. The value written here is the 10bit est point of the bin.



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# 2.11.5 Histogram Threshold Guardband Register

		His	togram	Threshold Guardband Register				
Register Ty	ype:		MMIO					
Address O	ffset:		48268h					
Project:			All					
<b>Default Val</b>	Default Value: 00000000h							
Access:	Access: R/W							
•	Size (in bits): 32							
Double Bu	ffer Update	Point:	Start of ve	rtical blank				
Bit De				scription				
31	Histogram	_Interrup	t_enable					
	Project:		All					
	Default Val	ue:	0b					
	Value Na	me	Descripti	on		Project		
	0b	Disable	Disabled			All		
	1b	Enable	This generates a histogram interrupt once a Histogram event occurs. Software must always program 1.					
30	Histogram	_Event_s	tatus					
	Project:		All					
	Access:		R/W C	Clear				
	Default Val	ue:	0b					
	When a His	stogram e	vent has oc software ne	curred, this will get set by the hardware. For any r eds to clear this bit by writing a '1'. The default sta	more Histog te for this b	ram it is '0'		
	Value Na	me		Description	Project			
	0b	Not Occ	curred	Histogram event has not occurred	All			
	1b	Occure	d	Histogram event has occurred	All			
29:22	Guardban	d_Interru	ot_Delay		Proj	ect: All		
	An interrup	t is always	generated	after this many consecutive frames of the guardbabuffered on start of vblank. A value of 0 is invalid	and thresho			
21:0	Threshold	_Guardba	ınd		Proj	ect: All		
	This value is used to determine the guardband for the threshold interrupt generation. This single value is used for all the segments. This value is double buffered on start of vblank							



### 2.12 Motion Blur Mitigation (MBM) Control

These registers are use to control the MBM logic. (Sometimes called LOT, panel overdrive, or LRTC).

Before enabling MBM, software should have identically programmed both pipes source size and gamma tables. Additionally, before executing a flip on the selected pipe (which generates the MBM frame) software should have loaded the address of the reference frame into the second plane(s), this can be done by MMIO or by a flip command. The second pipe does not need to have it's panel fitter, link, or link PLL enabled (or anything else down the pipe from MBM).

### 2.12.1 MBM\_CTRL—MBM Control

			MBI	M_CTRL—MBM Control			
Register Ty Address O Project: Default Val Access: Size (in bits	ffset: 48800 All lue: 00000 R/W	) Dh					
Bit De				scription			
31	MBM_Enab	ole					
	Project:		All				
	Default Valu	re:	0b				
	This bit enables MBM logic.						
	Value Na	me		Description	Project		
	0b	Disable		MBM is Disabled	All		
	1b	Enable		MBM is Enabled	All		
30	Reserved	Proje	ct: All	Format:			
29	MBM Pipe	Select					
	Project:		All				
	Default Valu	ıe:	0b				
	This bit ass	igns MBM	modification	on to the selected pipe.			
	Value Na	me	Descripti	on	Project		
	0b I	Pipe A	PipeA (Pip previous b	peA will fetch the current buffer and PipeB will fetch the buffer)	All		
	1b I	Pipe B	PipeB (Pip previous b	peB will fetch the current buffer and PipeA will fetch the buffer)	All		



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			MBM_	CTRL—MBM Co	ontrol				
28:27	MBM_Surfa	MBM_Surface_select							
	Project:		All						
	Default Valu	ie:	0b						
	Value Na	me	Description	on		Project			
	00b	None	None			All			
	01b	Sprite	Sprite Only	У		All			
	10b	Primary	Primary Or	nly		All			
	11b	Both	Both sprite	and primary		All			
26:24	Reserved	Project:	All			Format:			
23:16	MBM_Delta	_Threshol	d						
	Project:		All						
	Default Valu	ie:	d0000000b						
				nt and previous compor Otherwise, the current va					
15:0	Reserved	Project	: All		Format	•			



#### 2.12.2 MBM\_TBL—MBM Overdrive Table

#### MBM\_TBL—MBM Overdrive Table

Register Type: MMIO
Address Offset: 48810h
Project: All
Default Value: 00000000h
Access: R/W
Size (in bits): 63x32

These will be the overdrive values to be used as the lookup table entries for MBM. Correction table factors are stored x-major, groups of input values go together, ascending from row entry zero. The first row is internally hard coded to 0, so the first address actually corresponds to the second row of the table. The last row is internally hard coded to 256, so only 7 rows total are programmable.

#### Overdrive table address offsets:

	0	31	63	95	127	159	191	223	255
0	0	0	0	0	0	0	0	0	0
31	48810h	48814h	48818h	4881Ch	48820h	48824h	48828h	4882Ch	48830h
63	48834h	48838h	4883Ch	48840h	48844h	48848h	4884Ch	48850h	48854h
95	48858h	4885Ch	48860h	48864h	48868h	4886Ch	48870h	48874h	48878h
127	4887Ch	48880h	48884h	48888h	4888Ch	48890h	48894h	48898h	4889Ch
159	488A0h	488A4h	488A8h	488ACh	488B0h	488B4h	488B8h	488BCh	488C0h
191	488C4h	488C8h	488CCh	488D0h	488D4h	488D8h	488DCh	488E0h	488E4h
223	488E8h	488ECh	488F0h	488F4h	488F8h	488FCh	48900h	48904h	48908h
255	256	256	256	256	256	256	256	256	256

Previous Pixel Value Range
Current Pixel Value Range
Address Offset
Hard Coded Value

DWord B	t	Description		
062	31:24	Reserved Project: All	Format:	
	23:16	Red_MBM_overdrive_value	Project: All	
	15:8	Green_MBM_overdrive_value	Project: All	
	7:0	Blue_MBM_overdrive_value	Project: All	



#### 2.13 Color Conversion & Control Registers

These registers contain the coefficients of the pipe color space converter. There are 12 values in 6 registers for each pipe. This color space conversion is used to convert the RGB frame buffer data into YUV data for use on the HDMI, DisplayPort or analog TV output. Or alternately a YUV frame buffer could be converted to RGB.

The high color channel is the most significant bits of the color. The low color channel is the least significant bits of the color. The medium color channel is the bits between high and low. For example: In RGB modes Red is in the High channel, Green in Medium, and Blue in Low. In YUV modes, U is in the High channel, Y in Medium, and V in Low.

The color space conversion registers are double buffered and are updated on the start of vertical blank following a write to the CSC Mode register for the respective pipe.

			CSC	Coefficient Description	
Project: Default Val Size (in bits		0h			
oefficients	s for the C			n-exponent-mantissa format. Two CS ata packing in each dword.	C coefficients are stored
Bit De				scription	
15	Sign Project:		All		
	Value N	a me		Description	Project
	0b Positive			Positive	All
	1b	Negative		Negative	All
14:12	Exponent Project: Represen	_	All		
	Value N	a me	Desc	cription	Project
	110b	4	4 or ı	mantissa is bb.bbbbbbb	All
	111b	2	2 or 1	mantissa is b.bbbbbbbb	All
	000b	1	1 or ı	mantissa is 0.bbbbbbbbbb	All
	001b	0.5	0.5 o	r mantissa is 0.0bbbbbbbbb	All
	010b	0.25	0.25	or mantissa is 0.00bbbbbbbbbb	All
	011b	0.125	0.12	5 or mantissa is 0.000bbbbbbbbbb	All
	others	Reserved	Rese	arved	All



			CSC Coefficient Description			
11:3	Mantissa				Project:	All
2:0	Reserved	Project:	All	Format:		

#### The matrix equations are as follows:

```
Y = (RY * R) + (GY * G) + (BY * B)

U = (RU * R) + (GU * G) + (BU * B)

V = (RV * R) + (GV * G) + (BV * B)
```

The standard programming for RGB to YUV is in the following table.

	Bt	1.601	Bt.709		
	Value	Program	Value	Program	
RU	0.2990	0x1990	0.21260	0x2D98	
GU	0.5870	0x0968	0.71520	0x0B70	
BU	0.1140	0x3E98	0.07220	0x3940	
RV	-0.1687	0xAAC8	-0.11460	0xBEA8	
GV	-0.3313	0x9A98	-0.38540	0x9C58	
BV	0.5000	0x0800	0.50000	0x0800	
RY	0.5000	0x0800	0.50000	0x0800	
GY	-0.4187	0x9D68	-0.45420	0x9E88	
BY	-0.0813	0xBA68	-0.04580	0xB5E0	

The standard programming for YUV to sRGB without scaling is in the following table.

The input is VYU on high, medium, and low channels respectively.

The output is RGB on high, medium, and low channels respectively.

Program the pre-CSC offsets to -128, -16, and -128 for high, medium, and low channels respectively.



The coefficients can be scaled if desired.

	Bt.601	Reverse	Bt.709	Reverse
	Value	Program	Value	Program
GY	1.000	0x7800	1.000	0x7800
BY	0.000	0x0000	0.000	0x0000
RY	1.371	0x7AF8	1.574	0x7C98
GU	1.000	0x7800	1.000	0x7800
BU	-0.336	0x9AC0	-0.187	0xABF8
RU	-0.698	0x8B28	-0.468	0x9EF8
GV	1.000	0x7800	1.000	0x7800
BV	1.732	0x7DD8	1.855	0x7ED8
RV	0.000	0x0000	0.000	0x0000

# 2.13.1 Pipe A Color Control

# 2.13.1.1 CSC\_A\_Coefficients 1

			CSC_A_C	oefficients 1		
Register Ty	/pe:	MMIO				
Address O	ffset:	49010h				
Project:		All				
<b>Default Val</b>	ue:	00000000	)h			
Access:		R/W				
Size (in bits	s):	32				
Double But	fer Update Point:	Start of ve	Start of vertical blank after armed			
Double But	ffer Armed By:	Write to C	SC_A_Mode			
Bit De				scription		
31:16	RY Pro	ject: All	Format:	CSC COEFFICIENT DESCRIPTION		
	CSC coefficient.	See format de	escription abo	ove.		
15:0	<b>GY</b> Pro	ject: All	Format:	CSC COEFFICIENT DESCRIPTION		
	CSC coefficient.	See format de	escription abo	ove.		

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## 2.13.1.2 CSC\_A\_Coefficients 2

		C	SC_A_C	oefficients 2	
Register Type:	I	MMIO			
Address Offset:	4	49014h			
Project:	,	ΔII			
<b>Default Value:</b>	(	00000000h			
Access:	: R/W				
Size (in bits):	bits): 32				
Double Buffer Upd	ate Point:	pint: Start of vertical blank after armed			
<b>Double Buffer Arm</b>	Oouble Buffer Armed By: Write to CSC_A_Mode				
Bit De				scription	
31:16 <b>BY</b>	Project:	All	Format:	CSC COEFFICIENT DESCRIPTION	
CSC c	SC coefficient. See format description above.				
15:0 Reserv	<b>ved</b> Projec	t: All		Format:	

#### 2.13.1.3 CSC\_A\_Coefficients 3

	CSC_A_Coeffic	cients 3			
Register Typ	vpe: MMIO				
Address Off	<b>ifset:</b> 49018h				
Project:	All				
<b>Default Valu</b>	ue: 00000000h				
Access:	R/W				
Size (in bits)	s): 32	32			
<b>Double Buff</b>	fer Update Point: Start of vertical blank after arn	ned			
<b>Double Buffe</b>	fer Armed By: Write to CSC_A_Mode				
Bit De	sc	ription			
31:16	RU Project: All Format: CSC	COEFFICIENT DESCRIPTION			
	CSC coefficient. See format description above.				
15:0	GU Project: All Format: CSC	COEFFICIENT DESCRIPTION			
	CSC coefficient. See format description above.				



#### 2.13.1.4 CSC\_A\_Coefficients 4

		CSC_A_C	coefficients 4		
Register Ty	pe:	MMIO			
<b>Address Of</b>	fset:	4901Ch			
Project:		All			
Default Valu	ue:	00000000h			
Access:		R/W			
Size (in bits	s):	32			
<b>Double Buf</b>	fer Update Point:	ate Point: Start of vertical blank after armed			
Double Buf	fer Armed By:	Write to CSC_A_Mode	)		
Bit De			scription		
31:16	<b>BU</b> Project	t: All Format:	CSC COEFFICIENT DESCRIPTION		
	CSC coefficient. Se	e format description abo	ove.		
15:0	Reserved Proj	ect: All	Format:		

## 2.13.1.5 CSC\_A\_Coefficients 5

			CSC_A_C	oefficients 5	
Register Ty	/pe:	MMIO			
Address O	ffset:	49020h			
Project:		All			
<b>Default Val</b>	ue:	0000000	0h		
Access:		R/W			
Size (in bit	s):	32			
Double But	ffer Update Point:	Start of vertical blank after armed			
Double But	ffer Armed By:	Write to 0	CSC_A_Mode		
Bit De				scription	
31:16	<b>RV</b> Projec	ct: All	Format:	CSC COEFFICIENT DESCRIPTION	
	CSC coefficient. Se	ee format d	lescription abo	ove.	
15:0	<b>GV</b> Project	ct: All	Format:	CSC COEFFICIENT DESCRIPTION	
	CSC coefficient. See format description above.				



# 2.13.1.6 CSC\_A\_Coefficients 6

		CSC_	A_C	pefficients 6	
Register Type:	MI	MIO			
Address Offset:	49	024h			
Project:	All				
Default Value:	00	000000h			
Access:	R/W				
Size (in bits):	bits): 32				
<b>Double Buffer Update F</b>	Point: St	Start of vertical blank after armed			
<b>Double Buffer Armed B</b>	puble Buffer Armed By: Write to CSC_A_Mode				
Bit De				scription	
31:16 <b>BV</b>	Project:	All For	mat:	CSC COEFFICIENT DESCRIPTION	
CSC coeffic	SC coefficient. See format description above.				
15:0 Reserved	Project:	All		Format:	

#### 2.13.1.7 CSC\_A\_M ode

	CSC_A_Mode	
Register Type:	MMIO	
Address Offset:	49028h	
Project:	All	
Default Value:	0000000h	
Access:	R/W	
Size (in bits):	32	
<b>Double Buffer Update Point:</b>	Start of vertical blank	
Writes to this register arm C	SC_A registers	
Bit De	scription	
31:3 Reserved Pro	ect: All	Format:



#### **CSC A Mode**

2 CSC\_Black\_Screen\_Offset

Project: All Default Value: 0b

Adds an offset to the data output from CSC

In sRGB ouput mode: RGB is defined as R`+ 1/16, G`+ 1/16, B`+ 1/16

In rcYUV output mode: YUV is defined as Y'+ 1/16, U and V are output in excess 2048 format

Value N	a me	Description	Project
0b	No Offset	CSC output has no offset added (will be RGB or YUV, depending on bit 0)	All
1b	Offset	CSC output has offset added (will be sRGB or rcYUV depending on bit 0)	All

#### 1 CSC\_Position

Project: All Default Value: 0b

Selects the CSC position in the pipe.

Value N	a me	Description	
0b	CSC After	CSC is after gamma and DPST image enhancement	All
1b	CSC Before	CSC is before gamma and DPST image enhancement	All

#### 0 CSC\_Mode

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Project: All Default Value: 0b Selects the CSC direction.

Value N	a me	Description	Project
0b	RGB to YUV	RGB to YUV conversion	All
1b	YUV to RGB	YUV to RGB conversion	All



## 2.13.1.8 Pre-CSC\_A High Color Channel Offset

	-	Pre-CSC_A High	Color Channel	Offset	
Register Type:		MMIO			
Address Offset:		49030h			
Project:		All			
Default Value:		00000000h			
Access:		R/W			
Size (in bits):		32			
<b>Double Buffer Update</b>	Point:	Start of vertical blank a	after armed		
Double Buffer Armed	Ву:	Write to CSC_A_Mode	<b>;</b>		
Bit De			scription		
31:13 Reserved	Pro	ject: All		Format:	
12:0 <b>Pre-CSC_</b>	High_Co	lor_Channel_Offset		Project:	All
This 13-bit	2's comp	element value is used to	give an offset to the	color channel as it enters CSC	ogic.

# 2.13.1.9 Pre-CSC\_A Medium Color Channel Offset

Register Ty	/pe:	MMIO				
Address O	•	49034h				
Project:		All				
Default Val	ue:	00000000h				
Access:		R/W				
Size (in bit	s):	32				
Double Bu	ffer Update Point:	Start of vertical blank after armed				
Double Bu	ffer Armed By:	Write to CSC_A_Mode				
Bit De		scrip	tion			
31:13	Reserved Pro	oject: All	Format:			
12:0	Pre-CSC_Medium	Pre-CSC_Medium_Color_Channel_Offset Project: Al				
	This 13-bit 2's com	plement value is used to give an offs	set to the color channel as it enters CSC logic.			



#### 2.13.1.10 Pre-CSC\_A Low Color Channel Offset

	Pre-CSC_A Low Color Ch	nannel Offset			
Register Type:	MMIO				
Address Offset:	49038h				
Project:	All				
Default Value:	00000000h				
Access:	R/W	R/W			
Size (in bits):	32	32			
<b>Double Buffer Update Poin</b>	t: Start of vertical blank after armed				
<b>Double Buffer Armed By:</b>	Write to CSC_A_Mode				
Bit De	script	ion			
31:13 Reserved	Project: All	Format:			
12:0 Pre-CSC_Low_	_Color_Channel_Offset	Project: All			
This 13-bit 2's o	complement value is used to give an offs	et to the color channel as it enters CSC logic.			

# 2.13.2 Pipe B Color Control

#### 2.13.2.1 CSC\_B\_Coefficients 1

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		CSC_B_C	Coefficients 1	
Register Type:	MMIO			
Address Offset:	49110h	1		
Project:	All			
Default Value:	000000	000h		
Access:	R/W			
Size (in bits):	32			
<b>Double Buffer Update Poi</b>	nt: Start of	vertical blank a	after armed	
<b>Double Buffer Armed By:</b>	Write to	CSC_B_Mode	9	
Bit De			scription	
31:16 <b>RY</b>	Project: All	Format:	CSC COEFFICIENT DESCRIPTION	
CSC coefficier	nt. See forma	description abo	ove.	
15:0 <b>GY</b>	Project: All	Format:	CSC COEFFICIENT DESCRIPTION	
CSC coefficier	nt. See forma	description abo	ove.	



## 2.13.2.2 CSC\_B\_Coefficients 2

	CSC_B_Coefficients 2		
Register Type:	MMIO		
Address Offset:	49114h		
Project:	All		
Default Value:	0000000h		
Access:	R/W		
Size (in bits):	32		
<b>Double Buffer Update Point:</b>	Start of vertical blank after armed		
Double Buffer Armed By:	Write to CSC_B_Mode		
Bit De	scription		
31:16 <b>BY</b> Pro	ject: All Format: CSC COEFFICIENT DESCRIPTION		
CSC coefficient.	See format description above.		
15:0 <b>Reserved</b> P	roject: All Format:		

# 2.13.2.3 CSC\_B\_Coefficients 3

			CSC_B_C	oefficients 3	
Register Type:		MMIO			
Address Offset:		49118h			
Project:		All			
Default Value:		00000000	)h		
Access:		R/W			
Size (in bits):		32			
<b>Double Buffer U</b>	pdate Point:	Start of ve	ertical blank a	ifter armed	
<b>Double Buffer A</b>	rmed By:	Write to C	SC_B_Mode		
Bit De				scription	
31:16 <b>RU</b>	Project	All	Format:	CSC COEFFICIENT DESCRIPTION	
CSC coefficient. See format description above.					
15:0 <b>GU</b>	Project	All	Format:	CSC COEFFICIENT DESCRIPTION	
CSC	coefficient. See	format de	escription abo	ove.	



## 2.13.2.4 CSC\_B\_Coefficients 4

		CSC_B_Coefficients 4
Register Type:		MMIO
Address Offset:		4911Ch
Project:		All
<b>Default Value:</b>		0000000h
Access:		R/W
Size (in bits):		32
<b>Double Buffer Update</b>	Point:	Start of vertical blank after armed
<b>Double Buffer Armed B</b>	By:	Write to CSC_B_Mode
Bit De		scription
31:16 <b>BU</b>	Project:	t: All Format: CSC COEFFICIENT DESCRIPTION
CSC coeffic	cient. See	ee format description above.
15:0 Reserved	Project:	et: All Format:

## 2.13.2.5 CSC\_B\_Coefficients 5

			CSC_B_C	oefficients 5	
Register Ty	pe:	MMIO			
Address Of	fset:	49120h			
Project:		All			
Default Valu	ie:	00000000	)h		
Access:		R/W			
Size (in bits):		32			
<b>Double Buff</b>	fer Update Point:	Start of ve	ertical blank a	fter armed	
Double Buff	fer Armed By:	Write to C	SC_B_Mode		
Bit De				scription	
31:16	<b>RV</b> Proje	ct: All	Format:	CSC COEFFICIENT DESCRIPTION	
	CSC coefficient. See format description above.				
15:0	<b>GV</b> Proje	ct: All	Format:	CSC COEFFICIENT DESCRIPTION	
	CSC coefficient. S	ee format d	escription abo	ove.	

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# 2.13.2.6 CSC\_B\_Coefficients 6

CSC_B_Coefficients 6			
Register Type:	MMIO		
Address Offset:	49124h	1	
Project:	All		
Default Value:	0000000	000h	
Access:	R/W		
Size (in bits):	32		
<b>Double Buffer Update Poi</b>	nt: Start of v	vertical blank after armed	
<b>Double Buffer Armed By:</b>	Write to	o CSC_B_Mode	
Bit De		scription	
31:16 <b>BV</b>	Project: All	Format: CSC COEFFICIENT DESCRIPTION	
CSC coefficier	nt. See format o	description above.	
15:0 Reserved	Project: All	Format:	

## 2.13.2.7 CSC\_B\_M ode

	CSC_B_N	lode
Register Type:	MMIO	
Address Offset:	49128h	
Project:	All	
Default Value:	00000000h	
Access:	R/W	
Size (in bits):	32	
Double Buffer Update Point:	Start of vertical blank	
Writes to this register arm C	SC_B registers	
Bit De	•	scription
31:3 Reserved Pro	ject: All	Format:



#### CSC\_B\_Mode

2 CSC\_Black\_Screen\_Offset

Project: All Default Value: 0b

Adds an offset to the data output from CSC

In sRGB ouput mode: RGB is defined as R`+ 1/16, G`+ 1/16, B`+ 1/16

In rcYUV output mode: YUV is defined as Y'+ 1/16, U and V are output in excess 2048 format

Value N	a me	Description	Project
0b	No Offset	CSC output has no offset added (will be RGB or YUV, depending on bit 0)	All
1b	Offset	CSC output has offset added (will be sRGB or rcYUV depending on bit 0)	All

1 CSC\_Position

Project: All Default Value: 0b

Selects the CSC position in the pipe.

Value N	a me	Description	Project
0b	CSC After	CSC is after gamma and DPST image enhancement	All
1b	CSC Before	CSC is before gamma and DPST image enhancement	All

0 CSC\_Mode

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Project: All Default Value: 0b

Selects the CSC direction. Input and output formats and position within the pipe

	Value N	a me	Description	Project
Ī	0b	RGB to YUV	RGB to YUV conversion	All
	1b	YUV to RGB	YUV to RGB conversion	All



## 2.13.2.8 Pre-CSC\_B High Color Channel Offset

		Pre-CSC_B High Color (	Channel Offset	
Register Ty	rpe:	MMIO		
Address Of	fset:	49130h		
Project:		All		
<b>Default Valu</b>	ue:	00000000h		
Access:		R/W		
Size (in bits): Double Buffer Update Point:		32		
		Start of vertical blank after arme	ed	
Double Buf	fer Armed By:	Write to CSC_B_Mode		
Bit De		scr	ption	
31:13 <b>Reserved</b> Proj		ject: All	Format:	
12:0	Pre-CSC_B_High_	Color_Channel_Offset	Projec	t: All
	This 13-bit 2's comp	plement value is used to give an o	ffset to the color channel as it enters CS	C logic.

## 2.13.2.9 Pre-CSC\_B Medium Color Channel Offset

Pre-CSC_B Medium Color Channel Offset						
Register Type:	MMIO					
Address Offset:	49134h					
Project:						
Default Value:	ue: 00000000h					
Access:	R/W					
Size (in bits):	s): 32					
<b>Double Buffer Update Point:</b>	ffer Update Point: Start of vertical blank after armed					
Double Buffer Armed By:	Iffer Armed By: Write to CSC_B_Mode					
Bit De	scription					
31:13 Reserved F	Reserved Project: All Format:					
12:0 Pre-CSC_B_Med	Pre-CSC_B_Medium_Color_Channel_Offset Project: All					
This 13-bit 2's co	mplement value is used to give an offset to	o the color channel as it enters CSC logic.				



#### 2.13.2.10 Pre-CSC\_B Low Color Channel Offset

	Pre-CSC_B Low Color Channel Offset				
Register Type:	MMIO				
Address Offset: 49138h					
Project:	ct: All				
Default Value:	ue: 00000000h				
Access:	R/W				
Size (in bits):	s): 32				
<b>Double Buffer Update Poin</b>	Iffer Update Point: Start of vertical blank after armed				
<b>Double Buffer Armed By:</b>	•				
Bit De	scription				
31:13 Reserved	Project: All Form	nat:			
12:0 Pre-CSC_B_Lc	Pre-CSC_B_Low_Color_Channel_Offset Project: All				
This 13-bit 2's o	complement value is used to give an offset to the color channel a	as it enters CSC logic.			

#### 2.14 Display Palette Registers (4A000h-4CFFFh)

The display palette provides a means to correct the gamma of an image stored in a frame buffer to match the gamma of the monitor or presentation device. Additionally, the display palette provide a method for converting indexed data values to color values for VGA and 8-bpp indexed display modes. The display palette is located after the plane blender. Using the individual plane gamma enables, the blended pixels can go through or bypass the palette on a pixel by pixel basis.

The display palette can be accessed through multiple methods and operate in one of three different modes.

8 bit legacy palette mode (for indexed VGA and 8 bpp formats and for legacy gamma): 256 entries of 24 bits each (8 bits per color).

For indexed formats, an 8 bit per pixel value is used to lookup a 24 bit per pixel value from the palette which then is padded to 36 bits. This permits a compact data format to choose from 256 colors out of a larger palette of colors. The legacy palette is accessible through both MMIO and VGA palette register I/O addresses. Through VGA palette register I/O addresses, the palette can look as though there are only 6 bits per color component (this mapping is handled inside the VGA engine).

For legacy gamma, the 36 bits per pixel gamma input is chopped to 24 bits and used to lookup a 24 bit pixel value from the palette which then is padded to 36 bits. This permits a color to be re-mapped to a different brightness for gamma correction. This provides the lowest quality gamma and should only be used for legacy requirements.



10 bit precision palette mode (for 10 bit gamma):

1024 entries of 30 bits each (10 bits per color).

For 10 bit gamma, the 36 bits per pixel gamma input is chopped to 30 bits and used to lookup a 30 bit pixel value from the palette which then is padded to 36 bits. This permits a color to be re-mapped to a different brightness for gamma correction. This provides the highest quality gamma for non-indexed pixel data formats of 30 bits per pixel or less.

#### 12 bit interpolated gamma mode:

512 entries of 16 bits each (format described in 12 bit interpolated gamma programming notes).

For 12 bit interpolated gamma, the 36 bits per pixel gamma input is used to lookup reference points (16 bits per color in 12.4 format) along a gamma curve and interpolate a 36 bit pixel result. This permits a color to be re-mapped to a different brightness for gamma correction. This provides the highest quality gamma for pixel data formats greater than 30 bits per pixel.

Pixel chopping refers to removing the LSBs of each color component to reduce bits per pixel. Pixel padding refers to adding LSBs to each color component to increase bits per pixel.

Accesses to the palette entries require that the core display clock is running at the time of the update. All write accesses to the palette must be in dwords. Byte or word writes to the palettes are not allowed.

#### 2.14.1 LGC\_PALETTE\_ A—Pipe A Legacy Display Palette

		LGC_PAL	_GC_PALETTE_A—Pipe A Legacy Display Palette				
Register Ty Address Of	•	O 00h					
Project:	All	JUN .					
Default Val		JUUUUUh					
Access: Size (in bits		V (DWORD acc x32	ess only, r	o byte acce	ess)		
DWord Bi	t					Description	
0255	31:24	Reserved	Project:	All			Format:
	23:16	Red_Palette	_Entry	Project:	All	Format:	
	15:8	Green_Palet	te_Entry	Project:	All	Format:	
	7:0	Blue_Palette	_Entry	Project:	All	Format:	<u> </u>



# 2.14.2 LGC\_PALETTE\_ B—Pipe B Legacy Display Palette

		LGC_PAL	_GC_PALETTE_B—Pipe B Legacy Display Palette				
Register Ty	rpe: MN	IO					
<b>Address Of</b>	fset: 4A8	300h					
Project:	All						
<b>Default Val</b>	ue: UU	UUUUUUh					
Access:	R/V	(DWORD access only, no byte acce		ess)			
Size (in bits	s): 256	x32					
DWord Bi	t					Description	
0255	31:24	Reserved	Project:	All			Format:
	23:16	Red_Palette	_Entry	Project:	All	Format:	
	15:8	Green_Palet	tte_Entry	Project:	All	Format:	·
	7:0	Blue_Palette	e_Entry	Project:	All	Format:	

# 2.14.3 PREC\_PALETTE\_A—Pipe A Precision Display Palette

	10 bit Precision Palette Mode Format				
Project:	All				
Format for 10 bit precision palette mode.					
Bit De	Bit De scription				
31:30	Reserved Project: All	Format:			
29:20	Red_Palette_Entry	Project: All			
19:10	Green_Palette_Entry	Project: All			
9:0	Blue_Palette_Entry	Project: All			

	12-bit Interpolated Precision Palette Mod	e (odd Dword) Format
Project:	All	
Format for	12 bit interpolated gamma mode, odd dwords.	
Bit De	scription	
31:30	Reserved Project: All	Format:
29:20	Red_ Base[11:2]	Project: All
19:10	Green_ Base[11:2]	Project: All



	12-bit Interpolated Precision Palette Mode (odd Dword) Forma	at	
9:0	Blue_Base[11:2] Pro	ject:	All

	12-bit Int	terpolated	d Precision Pa	lette Mode (even D	word) Format	
Project:	All					
Format for	12 bit interpo	lated gamm	a mode, odd dwor	ds		
Bit De				scription		
31:30	Reserved	Project:	All		Format:	MBZ
29:28	Red_Base[1	:0]			Project:	All
27:24	Red_Fractio	n			Project:	All
23:20	Reserved	Project:	All		Format:	
19:18	Green_Base	[1:0]			Project:	All
17:14	Green_Fract	ion			Project:	All
13:10	Reserved	Project:	All		Format:	
9:8	Blue_Base[1	1:0]			Project:	All
7:4	Blue_Fraction	on			Project:	All
3:0	Reserved	Project:	All		Format:	

	PRE	C_PALETTE_A	A—Pipe A	Prec	ision Disp	lay Palette(10 bit)
Register Typ	oe: MM	IO				
<b>Address Off</b>	set: 4B0	0h				
Project:	All					
<b>Exists If:</b>	PIP	EACONF:Pipe_A_P	alette/Gamma	_Unit_ı	mode = 01b	
<b>Default Valu</b>	e: UUI	JUUUUUh				
Access:	R/W	/ (DWORD access o	only, no byte ac	ccess)		
Size (in bits)	): 102	4x32				
DWord Bit					Description	
01023	31:0	10bit_mode	Project:	All	Format:	10 bit Precision Palette Mode Format
		See format descrip	otion above			



PREC\_PALETTE\_A—Pipe A Precision Display Palette(12 bit)

Register Type: MMIO
Address Offset: 4B000h
Project: All

Exists If: PIPEACONF:Pipe\_A\_Palette/Gamma\_Unit\_mode = 10b

**Default Value:** UUUUUUUUh

Access: R/W (DWORD access only, no byte access)

**Size (in bits):** 1024x32

DWord Bit

0,2,4,..102
2
31:0
12bit\_even Project: All Format: 12-bit Interpolated Precision Palette Mode (even Dword)
Format
See format description above

1,3,5,..102
3
31:0
12bit\_odd Project: All Format: 12-bit Interpolated Precision Palette Mode (odd Dword)
Format
See format description above

#### 2.14.4 PREC\_PALETTE\_B—Pipe B Precision Display Palette

PREC\_PALETTE\_B—Pipe B Precision Display Palette(10 bit)

Register Type: MMIO
Address Offset: 4C000h
Project: All

Exists If: PIPEBCONF:Pipe\_B\_Palette/Gamma\_Unit\_mode = 01b

**Default Value:** UUUUUUUUh

Access: R/W (DWORD access only, no byte access)

**Size (in bits):** 1024x32

DWord Bit

0..1023 31:0 10bit\_mode Project: All Format: 10 bit Precision Palette Mode Format

See format description above



PREC_PALETTE_B—Pipe B Precision Display Palette(12 bit	PREC PALETTE	B—Pipe	<b>B Precision Dis</b>	play F	Palette(12	bit)
--	--------------	--------	------------------------	--------	------------	------

Register Type: MMIO
Address Offset: 4C000h
Project: All

Exists If: PIPEBCONF:Pipe\_B\_Palette/Gamma\_Unit\_mode = 10b

**Default Value:** UUUUUUUUh

Access: R/W (DWORD access only, no byte access)

**Size (in bits):** 1024x32

DWord B	t	Description
01023	63:32	12bit_odd Project: All Format: 12-bit Interpolated Precision Palette Mode (odd Dword) Format
		See format description above
	31:0	12bit_even Project: All Format: 12-bit Interpolated Precision Palette Mode (even Dword) Format
		See format description above

#### 12-bit Interpolated Gamma Programming Notes:

The 12-bit gamma correction curve is represented by specifying a set of reference points spaced equally along the desired curve. Red, Green, and Blue each have 513 reference points. The first 512 reference points are stored in the precision palette RAM, and the final value is stored in the GCMAX register. The first 512 reference points are 16 bits represented in a 12.4 format with 12 integer and 4 fractional bits. The final reference points are 17 bits represented in a 13.4 format with 13 integer and 4 fractional bits.

During operation the appropriate reference point pairs (adjacent) are selected for each color, and the output is interpolated between these two reference point values.

To program the gamma correction reference points, calculate the desired gamma curve for inputs from 0 to 4096. Every 8th point on the curve (0, 8, 16 ... 4088, 4096) becomes a reference point. Convert the gamma value to the 13.4 format. The first 512 reference points are saved to the precision palette RAM, where the even DWords contain the lower 6 bits of the reference point value, and the odd DWords contain the upper 10 bits of the reference point value. The final 513th reference point is saved in the GCMAX registers in 13.4 format.

Example equation for gamma curve of 2.2:

For (X = 0..4096) { gamma =  $[(X / 4096) ^ 2.2] * 4096$  }

The curve must be flat or increasing, never decreasing.



# 2.14.5 PIPEAGCMAX—Pipe A Gamma Correction Max

	Pipe Max Gamma Correction Format					
Project: Default Val	Project: All Default Value: 00010000h					
Bit De	Bit De scription					
31:17	Reserved Project: All Format:					
16:0	Max_Color_Gamma_Correction_Point Project: All 513 <sup>th</sup> reference point for the color channel of the 12-bit pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 4096.0.					

PIPEAGCMAX—Pipe A Gamma Correction Max								
Register Type: MM		IO						
		000h						
Project: All								
Default Value: 000		10000h						
Access:	R/W	V						
Size (in bits): 3x32								
DWord Bi	t				Description			
0	0 31:0		Project:	All	Format:	Pipe Max Gamma Correction Format		
1	1 31:0		Project:	ct: All Format: Pipe Max Gamma Correc Format		Pipe Max Gamma Correction Format		
2	2 31:0 <b>Blue</b>		Project:	All	Format:	Pipe Max Gamma Correction Format		



# 2.14.6 PIPEBGCMAX —Pipe B Gamma Correction Max

PIPEBGCMAX—Pipe B Gamma Correction Max								
Register Type: MM		IIO						
Address Offset: 4D0		010h						
Project: All								
Default Value: 000		10000h						
Access:	R/V	V						
Size (in bits	s): 3x3	2						
DWord Bi	t				Description			
0	0 31:0		Project:	All	Format:	Pipe Max Gamma Correction Format		
1	1 31:0		Project:	All	Format:	Pipe Max Gamma Correction Format		
2 31:0 <b>E</b>		Blue	Project:	All	Format:	Pipe Max Gamma Correction Format		

# 2.15 Software Flag Registers (4F000h–4F10Fh)

# 2.15.1 Software Flag Registers

Software Flag Registers								
Register Type: M		IO						
<b>Address Offse</b>	t: 4F0	00h						
Project:	All							
<b>Default Value:</b>	000	00000h						
Access:	R/W	1						
Size (in bits):	36x3	32						
					e space and have no dire he software architecture.	ct effect on h	ardware	
DWord Bit					Description			
035	31:0	Reserved	Project:	All		Format:	PBC	



# 2.15.2 GT Scratchpad

**GT Scratchpad** 

Register Type: MMIO
Address Offset: 4F100h
Project: All
Default Value: 00000000h
Access: R/W

8x32

Size (in bits):

These registers are used as scratch pad data storage space and have no direct effect on hardware

operation. The use of these registers is defined by the software architecture.

DWord Bit Description

0..7 31:0 Reserved Project: All Format: PBC



# 3. North Pipe and Port Controls (60000h–6FFFh)

# 3.1.1 Pipe A Timing

# 3.1.1.1 HTOTAL\_A—Pipe A Horizontal Total Register

		HTOTAL	Δ—Pine Δ	Horizontal Total F	Pagistar Pagistar		
D t. t T	14140	IIIOIAL	_A—ripe A	i i o i i o i a i i o i a i i	register		
Register Ty	•						
Address O		1					
Project:	All	2001-					
Default Val		Juun					
Access:	R/W						
Size (in bit	s): 32						
Bit De				scription			
31:29	Reserved	Project:	All		Format:	MBZ	
28:16	Pipe_A_Hori	izontal_Total	_Display_Clock	s		Project:	All
		d, front/back		o to 8192 pixels encomp re period. This field is pro			locks
		ould always b	e equal or great	e of two when driving the er to the sum of the horiz			
15:12	Reserved	Project:	All		Format:	MBZ	
11:0	Pipe_A_Hori	izontal_Activ	e_Display_Pixe	ls		Project:	All
		tive display pi		Display resolutions up to pixel number 0. The va			
				o multiples of two pixels vorizontal active display si			VDS



# 3.1.1.2 HBLANK\_A—Pipe A Horizontal Blank Register

		HBLANK	_A—Pip	e A Horizontal Blank Register
Register Ty Address Of Project: Default Val Access: Size (in bits	60004h All ue: 000000 R/W			
Bit De				scription
31:29	Reserved	Project:	All	Format:
28:16	number relat End pixel pos considered p that there is The number channel mod	eld specifies to the horisition, where cosition 1, etc. no left hand both of clocks with le.  added in the report of the cost	Deposition zontal activate first activate Horizonta order area in blank negister would activate the position of the position o	Project: All of Horizontal Blank End expressed in terms of the absolute pixel ve display start. The value programmed should be the HBLANK live pixel is considered position 0; the second active pixel is all blank ending at the same point as the horizontal total indicates. HBLANK size has a minimum value of 32 clocks. HBLANK size has a minimum value of 32 clocks.  Therefore the desired programmed to the same value as the second active pixel is all blank ending at the same value as the second active pixel is all blank ending at the same value as the second active pixel is all blank ending at the same value as the second active pixel is all blank ending at the same value as the second active pixel pixel is all blank ending at the same value as the second active pixel
15:13	Reserved	Project:	All	Format:
12:0	number relat Start pixel po considered p The number LVDS port in active region The value los	eld specifies to the horized to the horized to the horized to sition, where the sosition 1, etc. of clocks for latitude the channel of the ch	he Horizon zontal active the first according to both left an mode. Ho gister woul	Project: All tal Blank Start position expressed in terms of the absolute pixel we display start. The value programmed should be the HBLANK tive pixel is considered position 0; the second active pixel is dright borders need to be a multiple of two when driving the rizontal blank should only start after the end of the horizontal d be equal to RightBorder+Active-1.

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# 3.1.1.3 HSYNC\_A—Pipe A Horizontal Sync Register

		HSYNC	_A—Pi	pe A Horizontal Sync Register				
Register Ty	pe: MMIO							
Address O	ffset: 60008h	)						
Project:	All							
Default Val		000h						
Size (in bit	s): 32							
Bit				Description				
31:29	Reserved	Project:	All	Format: MBZ				
28:16	Pipe_A_Horizontal_Sync_End							
	Project:		All					
	Default Value	):	0b					
This 13-bit field specifies the horizontal Sync End position expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HSYN End pixel position, where the first active pixel is considered position 0; the second active pixel is considered position 1, etc.								
	two channel r	mode. This v	/alue shοι	eriod needs to be a multiple of two when driving the LVDS port in ald be greater than the horizontal sync start position and would be +FrontPorch+Sync-1.				
15:13	Reserved	Project:	All	Format: MBZ				
12:0	Pipe_A_Hori	zontal_Syn	c_Start					
	Project:		All					
	Default Value	):	0b					
	number relati Start pixel po considered p	ive to the hore sition, where osition 1, etc HBLANK wil	rizontal ac the first a . Note tha	antal Sync Start position expressed in terms of the absolute pixel tive display start. The value programmed should be the HSYNC active pixel is considered position 0; the second active pixel is at when HSYNC Start is programmed equal to HBLANK Start, both ted on the same pixel clock. It should never be programmed to less				
	LVDS port in	two channel	mode. TI	nning of the line needs to be a multiple of two when driving the his register should not be less than the horizontal active end. This active+RightBorder+FrontPorch-1.				



# 3.1.1.4 VTOTAL\_A—Pipe A Vertical Total Register

		VTOTA	L_A—Pip	e A Vertical Total Register		
Address O Project: Default Val Access: Size (in bit	All ue: 000000 R/W	h				
Bit De	3). 32			scription		
31:29	Reserved	Project:	All	Format:		
28:16	This 13 bit fie Lines, top/bo required mini active, vertical leading edge lines in both	ttom border a us one. Vertical border, and of the horizon	ertical Total und retrace per cal total needs the vertical b ntal sync. For laced modes,	p to 8192 lines encompassing the Vertical Action. The value programmed should be the near to be large enough to be greater than the sulank regions. The vertical counter is increme interlaced display modes, this indicates the thardware automatically divides this number	umber of line om of the ver nted on the otal number	tical of
15:12	Reserved	Project:	All	Format:		
11:0	This 12-bit fie with the desir vertical active of lines in bo	red number of e area must b	ertical active of lines minus of e seven lines. terlaced mode	display resolutions up to 4096 lines. It should one. When using the internal panel fitting log For interlaced display modes, this indicates es, hardware automatically divides this number	ic, the minim the total nur	num nber

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# 

		VBLAN	<u> </u>	ipe A Vertical Blank Register	
Address O Project: Default Val Access: Size (in bit	All 000000 R/W				
Bit				Description	
31:29	Reserved	Project:	All	Format:	
28:16	number relati line position, etc. The end vertical total. interlaced dis in each field. lines.	eld specifies to ve to the ver where the fir of vertical bl This registe play modes, It does not o	the Vertical tical active st active lin lank should r should be hardware acount the tv	Project:  I Blank End position expressed in terms of the absolute Line display start. The value programmed should be the VBLANK in the is considered line 0, the second active line is considered line display be after the start of vertical blank and before or equal to the eloaded with the Vactive+BottomBorder+VBlank-1. For automatically divides this number by 2 to get the vertical blank that wo half lines that get added when operating in modes with half the er must always be programmed to the same value as the Vertical blank.	e 1, end
15:13	Reserved	Project:	All	Format:	
12:0	relative to the position, whe Minimum verl active. This r hardware aut count the two	eld specifies to e vertical activate the first actical blank size register is loa omatically die half lines the	the Vertical ve display setive line is ze is required with the vides this rat get adde	Project:  Il Blank Start expressed in terms of the absolute line number start. The value programmed should be the VBLANK Start line considered line 0, the second active line is considered line 1, even to be at least three lines. Blank should start after the end of the Vactive+BottomBorder-1. For interlaced display modes, number by 2 to get the vertical blank start in each field. It does not be done or the vertical blank start in each field. It does not set when operating in modes with half lines.	etc. f not



# 3.1.1.6 VSYNC\_A—Pipe A Vertical Sync Register

		VSYNC	C_A—Pi	pe A Vertical Sync Register	
	MMIO	)			
Address O	ffset: 60014	ŀh			
Project:	All				
<b>Default Val</b>	ue: 00000	)000h			
Access:	R/W				
Size (in bit	s): 32				
Bit De				scription	
31:29	Reserved	Project:	All	Format:	
28:16	Pipe_A_Ve	rtical_Sync_E	nd	Project:	All
	number rela line position etc. This re- display mod	tive to the verti , where the firs gister should b les, hardware a	ical active on tactive line e loaded wi automaticall	Sync End position expressed in terms of the absolute Line display start. The value programmed should be the VSYNC is considered line 0, the second active line is considered line that Vactive+BottomBorder+FrontPorch+Sync-1. For interface line divides this number by 2 to get the vertical sync end in each that get added when operating in modes with half lines.	line 1, laced ach
15:13	Reserved	Project:	All	Format:	
12:0	Pipe_A_Ve	rtical_Sync_S	tart	Project:	All
	number rela line position etc. This re- modes, hard	tive to the verti , where the firs gister would be dware automati	ical active on tactive line e loaded wit ically divide	Sync Start position expressed in terms of the absolute line display start. The value programmed should be the VSYNC e is considered line 0, the second active line is considered in Vactive+BottomBorder+FrontPorch-1. For interlaced dises this number by 2 to get the vertical sync start in each fiel get added when operating in modes with half lines.	line 1, splay

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# 3.1.1.7 PIPEASRC—Pipe A Source Image Size

		PIPE	ASRC—Pipe A Source Image	Size					
		MMIC	O						
Address O	ffset:	6001	Ch						
Project:		All	All						
<b>Default Val</b>	ue:	0000	0000h						
Access:		R/W							
Size (in bit	s):	32							
Double Bu	ffer Update Point:	Start	of vertical blank						
Bit De			scription						
31:28	Reserved P	roject:	All	Format:	MBZ				
27:16	Pipe_A_Horizon	tal_Sourc	ce_Image_Size		Project:	All			
	image created by image size minus	the displa one.	dorizontal source image size up to 4096. ay planes sent to the blender. The value	programmed sho	uld be the so				
			at is a multiple of two (even numbers) wh						
	channel mode. T Except in the case programmed to a	his implie e of panel value ide	es that for this mode, the value programm I fitting internal or in an external device, the thical to the horizontal active. This is the immed while the pipe is enabled.	ned will always be his register field w	an odd num vould be	nber.			
15:12	channel mode. T Except in the case programmed to a that is allowed to	his implie e of panel value ide	es that for this mode, the value programm I fitting internal or in an external device, the ntical to the horizontal active. This is the	ned will always be his register field w	an odd num vould be	nber.			
15:12 11:0	channel mode. T Except in the case programmed to a that is allowed to	his implie e of panel value ide be progra roject:	es that for this mode, the value programm I fitting internal or in an external device, the ntical to the horizontal active. This is the immed while the pipe is enabled.	ned will always be his register field w only register of th	e an odd num vould be he timing reg	nber.			
	channel mode. T  Except in the case programmed to a that is allowed to   Reserved P  Pipe_A_Vertical_ This 12-bit field s	This implies of panel value ide be progra troject:  Source_pecifies the down the dow	es that for this mode, the value programm I fitting internal or in an external device, the ntical to the horizontal active. This is the number of the pipe is enabled.  All  Image_Size  ne vertical source image size up to 4096 lisplay planes sent to the blender. The value of the pipe is the vertical source image size up to 4096 lisplay planes sent to the blender.	ned will always be his register field we only register of the Format:	e an odd nun vould be he timing reg MBZ Project: nines the siz	nber. gisters All e of			
	channel mode. T  Except in the case programmed to a that is allowed to   Reserved P  Pipe_A_Vertical_ This 12-bit field s the image created source image size  Except in the case	This implies of panel value ide be prograde roject:  Source_pecifies the dependence of panel end	es that for this mode, the value programm I fitting internal or in an external device, the ntical to the horizontal active. This is the number of the pipe is enabled.  All  Image_Size  ne vertical source image size up to 4096 lisplay planes sent to the blender. The value of the pipe is the vertical source image size up to 4096 lisplay planes sent to the blender.	hed will always be his register field we only register of the Format:  lines. This determalue programmed	e an odd num would be he timing reg MBZ Project: nines the siz I should be t	nber. gisters All e of			



# 3.1.1.8 VSYNCSHIFT\_A— Vertical Sync Shift Register

		VSYNCS	HIFT A—	/ertical Sync Shift Register	
	MMI		_		
Address O	ffset: 6002	28h			
Project:	All				
Default Va	lue: 0000	0000h			
Access:	R/W				
Size (in bit	s): 32				
Trusted Ty	<b>/pe:</b> 1				
Bit				Description	
31:13	Reserved	Project:	All	Format:	
12:0	Pipe_A_S	econd_Field_V	ertical_Sync_	Shift Project: All	
				nment for the start of the interlaced second field expressed in ve to the horizontal active display start.	
	This value	will only be use	ed if the PIPEA	CONF is programmed to an interlaced mode.	
				ical sync should start one pixel after the point halfway the value of this register should be programmed to:	
	(horizontal	sync start - floo	or[horizontal to	al / 2]).	
		ctual horizontal ed into the regis		horizontal total values and not the minus one values	
		al sync shift only position is align		the interlaced second field. In all other cases the vertical tal sync start.	

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#### 3.1.2 Pipe A M/N Values

Calculation of TU is as follows:
For modes that divide into the link frequency evenly,
Active/TU = payload/capacity
Please note that this is the same ratio as data m/n:
Payload/capacity = dot clk \* bytes per pixel / ls\_clk \* # of lanes

#### 3.1.2.1 PipeADataN1— Pipe A Data N value 1

#### PipeADataM1— Pipe A Data M value 1

Register Type: MMIO
Address Offset: 60030h
Project: All
Default Value: 00000000h
Access: R/W
Size (in bits): 32

This is the primary pipe data M value used for embedded DisplayPort and FDI. It is used in conjunction with the data N value 1. When switching between two refresh rates, both the M1/N1 data and link values and the M2/N2 link values must be programmed. Data M value 1 is used for the higher power M value setting.

Bit				Description		
31	Reserved	Project:	All	Format:	MBZ	
24	Reserved	Project:	All	Format:	MBZ	
23:0	Pipe_A_Data	a_M_value			Project:	All
	This field is t	he m value fo	r internal use o	f the DDA. Calculation of this value is as	follows:	
	Data m/n = o	dot clock * by	tes per pixel /	ls_clk * # of lanes		



#### 3.1.2.2 PipeADataM2— Pipe A Data M value 2

#### PipeADataM2— Pipe A Data M value 2

Register Type: MMIO
Address Offset: 60038h
Project: All
Default Value: 00000000h
Access: R/W

32

Size (in bits):

This is the second pipe data M value used for embedded FDI. It is used in conjunction with the data N value 2. When switching between two refresh rates, both the M1/N1 data and link values and the M2/N2 link values must be programmed. This value updates at the beginning of vblank. Data M value 2 is used for the lower power M value setting.

Bit De				scription		
31	Reserved	Project:	All	Format:	MBZ	
24	Reserved	Project:	All	Format:	MBZ	
23:0	Pipe_A_Data This field is t		or internal use of the	e DDA. Calculation of this value is as t	Project: follows:	All
	Data m/n = o	dot clock * b	ytes per pixel / ls_	clk * # of lanes		

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#### 3.1.2.3 PipeADataN2— Pipe A Data N value 2

#### PipeADataN2— Pipe A Data N value 2

Register Type: MMIO
Address Offset: 6003Ch
Project: All
Default Value: 00000000h
Access: R/W
Size (in bits): 32

This is the second pipe data N value used for FDI. It is used in conjunction with the data N value 2. When switching between two refresh rates, both the M1/N1 data and link values and the M2/N2 link values must be programmed. This value updates at the beginning of vblank. Data N value 2 is used for the lower power N value setting.

Bit De				scription		
31:24	Reserved	Project:	All	Format:	MBZ	
23:0	Pipe_A_Dat				Project:	All
	This field is	the n value for	internal us	se of the DDA. Calculation of this value is as fol	llows:	
	Data m/n =	dot clock * b	ytes per pi	xel / ls_clk * # of lanes		

#### 3.1.2.4 PipeADPLinkM1— Pipe A Link M value 1

#### PipeADPLinkM1— Pipe A Link M value 1

Register Type: MMIO
Address Offset: 60040h
Project: All
Default Value: 00000000h

Access: R/W Size (in bits): 32

This is the primary link data M value used for embedded FDI. It is used in conjunction with the link N value 1. When switching between two refresh rates, both the M1/N1 data and link values and the M2/N2 link values must be programmed. This value updates at the beginning of vblank. Link M value 1 is used for the higher power M value setting.

Bit De				scription	
31:24	Reserved	Project:	All	Format:	MBZ



PipeADPLinkM1— Pipe A Link M value 1												
23:0	Pipe_A_Link_M_value	Project:	ΑII									
	This field is the m value for external transmission in the Main Stream Attributes. value is as follows:	Calculation of this										
	Link m/n = pixel clk / ls clk											

#### 3.1.2.5 PipeADPLinkN1— Pipe A Link N value 1

#### PipeADPLinkN1— Pipe A Link N value 1

Register Type: MMIO
Address Offset: 60044h
Project: All
Default Value: 00000000h
Access: R/W
Size (in bits): 32

This is the primary link data N value used for embedded FDI. It is used in conjunction with the link N value 1. When switching between two refresh rates, both the M1/N1 data and link values and the M2/N2 link values must be programmed. This value updates at the beginning of vblank. Link N value 1 is used for the higher power N value setting.

Bit De	scription										
31:24	Reserved Project: All Format: MBZ										
23:0	Pipe_A_Link_N_value Project: All This field is the n value for external transmission in the Main Stream Attributes and VB-ID. Calculation of this value is as follows (to be filled in):										
	Link m/n = pixel clk / ls_clk										

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#### 3.1.2.6 PipeADPLinkM2— Pipe A Link M value 2

#### PipeADPLinkM2— Pipe A Link M value 2

Register Type: MMIO
Address Offset: 60048h
Project: All
Default Value: 00000000h
Access: R/W
Size (in bits): 32

This is the secondary link data M value used for embedded FDI. It is used in conjunction with the link N value 2. When switching between two refresh rates, both the M1/N1 data and link values and the M2/N2 link values must be programmed. This value updates at the beginning of vblank. Link M value 2 is used for the lower power M value setting.

	Bit De	scription										
İ	31:24	Reserved Project: All Format: MBZ										
	23:0	Pipe_A_Link_M_value       Project:       All         This field is the m value for external transmission in the Main Stream Attributes. Calculation of this value is as follows:										
		Link m/n = pixel clk / ls_clk										

#### 3.1.2.7 PipeADPLinkN2— Pipe A Link N value 2

#### PipeADPLinkN2— Pipe A Link N value 2

Register Type: MMIO
Address Offset: 6004Ch
Project: All
Default Value: 00000000h

Access: R/W
Size (in bits): 32

This is the secondary link data N value used for embedded FDI. It is used in conjunction with the link N value 1. When switching between two refresh rates, both the M1/N1 data and link values and the M2/N2 link values must be programmed. This value updates at the beginning of vblank. Link N value 2 is used for the lower power N value setting.

Bit De				scription		
31:24	Reserved	Project:	All	Format:	MBZ	



PipeADPLinkN2— Pipe A Link N value 2											
23:0	Pipe_A_Link_N_value Project: A										
	This field is the n value for external transmission in the Main Stream Attributes and VB-ID. Calculation of this value is as follows (to be filled in):										
	Link m/n = pixel clk / ls_clk										

# 3.1.3 Pipe B M/N Values

# 3.1.3.1 PipeBDataM1— Pipe B Data M value 1

			Pipe	BDataM <sup>1</sup>	— Pipe B Data	a M value 1	
Register Ty	ype:	MMIO					
<b>Address Offset:</b>		61030h					
Project:		All					
Default Value:		0000000	)0h				
Access:		R/W					
Size (in bits	s):	32					
See pipe A	descr	iption					
Bit De					scription	1	
31	Rese	rved	Project:	All		Format:	MBZ
30:25	TU_S	ize				Project:	All
	See p	ipe A de	scription				
24	Rese	rved	Project:	All		Format:	MBZ
23:0	Pipe_	B_Data_	_M_value			Project:	All
	See p	ipe A de	scription				

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# 3.1.3.2 PipeBDataN1— Pipe B Data N value 1

			Pipe	BDataN1	— Pip	e B Data N	l value 1		
Register Ty	pe: N	MMIO							
Address Of	fset: 6	61034h							
Project:	A	All .							
Default Valu	ue: (	00000	00h						
Access:	F	R/W							
Size (in bits	s): 3	32							
See pipe A	descrip	otion							
Bit De						scription			
31:24	Reserv	ved	Project:	All			Forma	at:	MBZ
23:0	Pipe_E	3_Data	_N_value				Project	:	All
	See pi	pe A de	escription						

# 3.1.3.3 PipeBDataM2— Pipe B Data M value 2

		Pipe	BDataM2-	– Pipe B Data I	VI value 2	
Register Ty	ype: MM	0				
Address O	ffset: 610	38h				
Project:	All					
<b>Default Val</b>	ue: 000	00000h				
Access:	R/W	•				
Size (in bits	s): 32					
See pipe A	description					
Bit De				scription		
31	Reserved	Project:	All		Format:	MBZ
30:25	TU_Size				Project:	All
	See pipe	A description				
24	Reserved	Project:	All		Format:	MBZ
23:0	Pipe_B_0	ata_M_value			Project:	All
	See pipe	A description				



# 3.1.3.4 PipeBDataN2— Pipe B Data N value 2

			Pipe	BDataN	2— Pip	e B Data	N value 2		
Register Ty	pe: N	MMIO							
Address Of	fset: 6	6103Ch							
Project:	A	ΔII							
Default Valu	ue: (	000000	00h						
Access:	F	R/W							
Size (in bits	s): 3	32							
See pipe A	descrip	otion							
Bit De						scription			
31:24	Reser	ved	Project:	All			Forma	t:	MBZ
23:0	Pipe_E	B_Data	_N_value	·	·		Project:		All
	See pi	pe A de	escription						

# 3.1.3.5 PipeBDPLinkM1— Pipe B Link M value 1

			PipeB	DPLin	kM1— P	ipe B Lir	nk M valu	ie 1	
Register Ty	/pe:	MMIO							
<b>Address Of</b>	ffset:	61040h							
Project:		All							
<b>Default Valu</b>	ue:	000000	00h						
Access:		R/W							
Size (in bits	s):	32							
See pipe A	descrip	tion							
Bit De						scription	n		
31:24	Reser	rved	Project:	All				Format:	MBZ
23:0	Pipe_	B_Link	_M_value			·		Project:	All
	See p	ipe A de	escription						

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# 3.1.3.6 PipeBDPLinkN1— Pipe B Link N value 1

PipeBDPLinkN1— Pipe B Link N value 1										
Register Ty	pe: N	MMIO								
<b>Address Of</b>	fset: 6	61044h								
Project:		AII								
Default Valu	ue: (	000000	00h							
Access:	F	R/W								
Size (in bits	s): 3	32								
See pipe A	descrip	otion.								
Bit De						scription				
31:24	Reserv	ved	Project:	All				Format:	MBZ	
23:0	Pipe_E	B_Link	_N_value			•		Project:	All	
	See pi	pe A de	scription							

# 3.1.3.7 PipeBDPLinkM2— Pipe B Link M value 2

			PipeB	DPLin	kM2— Pi	pe B Link	M value	2	
Register Ty	ype:	MMIO							
Address Of	ffset:	61048h							
Project:		All							
<b>Default Val</b>	ue:	000000	00h						
Access:		R/W							
Size (in bits	s):	32							
See pipe A	descri	ption							
Bit De						scription			
31:24	Reser	ved	Project:	All				Format:	MBZ
23:0	Pipe_	B_Link	_M_value					Project:	All
	See p	ipe A de	escription						



# 3.1.3.8 PipeBDPLinkN2— Pipe B Link N value 2

			PipeB	DPLink	N2— P	ipe B Li	nk N va	lue 2	
Register Ty	/pe:	MMIO							
Address Offset: 6104Ch									
Project:	Project: All								
<b>Default Valu</b>	ue:	000000	00h						
Access:		R/W							
Size (in bits	s):	32							
See pipe A	descri	ption							
Bit De						scriptio	n		
31:24	Rese	rved	Project:	All				Format:	MBZ
23:0	Pipe_	B_Link	_N_value					Project:	All
	See p	ipe A de	escription						

# 3.1.4 Panel Fitter Control Registers

# 3.1.4.1 PF\_PWR\_GATE\_CT RL—Panel Fitter Power Gate Control

	PFA_PWR_GATE_CTRL—Panel Fitter A Power Gate Control								
Register Ty	/pe:	MMIO							
Address O	ffset:	68060h							
Project:		DevSNB							
<b>Default Val</b>	ue:	00006453h							
Access:		R/W							
Size (in bits	s):	32							
<b>Double But</b>	ffer Update Point:	Start of vertical blank after armed							
<b>Double But</b>	ffer Armed By:	Write to PFA_WIN_SZ							
Bit De		scription	1						
31:16	Reserved Pro	eject: All	Format: MBZ						

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5:13	LATE_S	LATE_SIGNAL_SEQUENCE_START Project: All						
	Start of the late signal to the first RAM bank in number of cdclks after the start of power gating sequence. Applicable for both power gating on and off conditions.							
	Value N	la me	Description	Project				
	000b	Start time 0	Start time 0	All				
	001b	Start time 256	Start time 256	All				
	010b	Start time 512	Start time 512	All				
	011b	Start time 768	Start time 768	All				
	100b	Start time 1024	Start time 1024	All				
	101b	Start time 1280	Start time 1280	All				
	110b	Start time 1536	Start time 1536	All				
	111b	Start time 1792	Start time 1792	All				
12	Reserve	d Project: All	Format:	MBZ				
11:9	MID_SIG	NAL_SEQUENCE_STA	ART Project:	All				
	Start of the mid signal to the first RAM bank in number of cdclks after the start of power gatin sequence. Applicable for both power gating on and off conditions.							
				er gaung				
		e. Applicable for both po						
	sequence	e. Applicable for both po	ower gating on and off conditions.					
	value N	e. Applicable for both po	Description	Project				
	Value N	e. Applicable for both po	Description Start time 0	Project All				
	Value N 000b 001b	e. Applicable for both policy  Na me  Start time 0  Start time 256	Description Start time 0 Start time 256	Project All All				
	Value N 000b 001b 010b	e. Applicable for both policy  Na me  Start time 0  Start time 256  Start time 512	Description Start time 0 Start time 256 Start time 512	Project All All All				
	Value N 000b 001b 010b 011b	e. Applicable for both policy  Na me  Start time 0  Start time 256  Start time 512  Start time 768	Description Start time 0 Start time 256 Start time 512 Start time 768	Project All All All All				
	Value N 000b 001b 010b 011b 100b	e. Applicable for both policy  Na me  Start time 0  Start time 256  Start time 512  Start time 768  Start time 1024	Description Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024	Project All All All All All				
	Value N 000b 001b 010b 011b 100b 101b	e. Applicable for both policy  Na me  Start time 0  Start time 256  Start time 512  Start time 768  Start time 1024  Start time 1280	Description Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024 Start time 1280	Project All All All All All All				
8	Sequence  Value N  000b  001b  010b  011b  100b  101b  110b	Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024 Start time 1280 Start time 1536 Start time 1792	Description Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024 Start time 1280 Start time 1536	Project All All All All All All All All All				
8 7:6	Sequence   Value N	Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024 Start time 1280 Start time 1536 Start time 1792	Description Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024 Start time 1280 Start time 1536 Start time 1792	Project All All All All All All All All All Al				
	sequence  Value N  000b  001b  010b  100b  101b  110b  111b  Reserve  LATE_Si  Delay be	e. Applicable for both policy  Na me Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024 Start time 1280 Start time 1536 Start time 1792  d Project: All	Description Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024 Start time 1280 Start time 1536 Start time 1792  Format: Project: into successive RAM banks in number of cdclks. A	Project All All All All All All All All All Al				
	sequence  Value N  000b  001b  010b  100b  101b  110b  111b  Reserve  LATE_Si  Delay be	Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024 Start time 1280 Start time 1536 Start time 1792 d Project: All	Description Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024 Start time 1280 Start time 1536 Start time 1792  Format: Project: into successive RAM banks in number of cdclks. A	Project All All All All All All All All All Al				
	value N 000b 001b 010b 011b 100b 111b 110b 111b Reserve LATE_S Delay be power ga	Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024 Start time 1280 Start time 1536 Start time 1792 d Project: All	Description Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024 Start time 1280 Start time 1536 Start time 1792 Format: Project: into successive RAM banks in number of cdclks. Ass.	Project All All All All All All All All All Al				
	sequence  Value N  000b  001b  010b  100b  101b  110b  111b  Reserve  LATE_Si  Delay be power gar  Value N	Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024 Start time 1280 Start time 1792 d Project: All IGNAL_DELAY tween late signals going ating on and off condition	Description Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024 Start time 1280 Start time 1536 Start time 1792  Format: Project: into successive RAM banks in number of cdclks. As.  Description	Project All All All All All All All All All Al				
	sequence  Value N  000b  001b  010b  101b  100b  111b  Reserve  LATE_S  Delay be power ga  Value N  00b	Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024 Start time 1280 Start time 1536 Start time 1792 d Project: All IGNAL_DELAY tween late signals going ating on and off condition Name Start time 0	Description Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024 Start time 1280 Start time 1536 Start time 1792  Format:  Project: into successive RAM banks in number of cdclks. As.  Description Start time 0	Project All All All All All All All All All Al				



	PF	A_PWR_GATE_C	FRL—Panel Fitter A Power Gate Control					
4:3	MID_SIG	GNAL_DELAY	Project: All					
		Delay between mid signals going into successive RAM banks in number of cdclks. Applicable power gating on and off conditions.						
	Value	Na me	Description	Project				
	00b	Start time 0	Start time 0	All				
	01b	Start time 256	Start time 256	All				
	10b	Start time 512	Start time 512	All				
	11b	Start time 768	Start time 768	All				
2	Reserve	ed Project: All	Format: MB.	Z				
1:0	EARLY	EARLY_SIGNAL_DELAY Project: All						
		etween early signals goin wer gating on and off con-	g into successive RAM banks in number of cdclks. Applications.	able for				
	Value	Na me	Description	Project				
	00b	Start time 0	Start time 0	All				
	01b	Start time 256	Start time 256	All				
	10b	Start time 512	Start time 512	All				
	11b	Start time 768	Start time 768	All				

PFB_PWR_GATE_0	CTRL—Panel Fit	tter B Power (	Gate Control
 14140			

Register Type: MMIO
Address Offset: 68860h
Project: DevSNB
Default Value: 00006453h
Access: R/W
Size (in bits): 32

**Double Buffer Update Point:** Start of vertical blank after armed

**Double Buffer Armed By:** Write to PFA\_WIN\_SZ

 Bit De
 scription

 31:16
 Reserved
 Project: All
 Format: MBZ



15:13	PFB	CNAL SECUENCE STA		All				
15.13	Start of th	LATE_SIGNAL_SEQUENCE_START  Start of the late signal to the first RAM bank in number of cdclks after the start of power gatin sequence. Applicable for both power gating on and off conditions.						
	Value N	T	Description	Project				
	000b	Start time 0	Start time 0	All				
	001b	Start time 256	Start time 256	All				
	010b	Start time 512	Start time 512	All				
	011b	Start time 768	Start time 768	All				
	100b	Start time 1024	Start time 1024	All				
	101b	Start time 1280	Start time 1280	All				
	110b	Start time 1536	Start time 1536	All				
	111b	Start time 1792	Start time 1792	All				
12	Reserve	<b>d</b> Project: All	Format:	MBZ				
11:9	MID SIG	NAL_SEQUENCE_STAR	T Project:	All				
	Start of the mid signal to the first RAM bank in number of cdclks after the start of power gating sequence. Applicable for both power gating on and off conditions.							
				ower gating				
		e. Applicable for both pow		Project				
	sequence	e. Applicable for both pow	er gating on and off conditions.					
	value N	e. Applicable for both pow	Description	Project				
	Value N	e. Applicable for both pow  Na me  Start time 0	Description Start time 0	Project All				
	Value N 000b 001b	e. Applicable for both pow  la me  Start time 0  Start time 256	Description Start time 0 Start time 256	Project All All				
	Value N 000b 001b 010b	e. Applicable for both pow  Na me  Start time 0  Start time 256  Start time 512	Description Start time 0 Start time 256 Start time 512	Project All All All				
	Value N 000b 001b 010b 011b	e. Applicable for both power.  Name  Start time 0  Start time 256  Start time 512  Start time 768	Description Start time 0 Start time 256 Start time 512 Start time 768	Project All All All All				
	value N 000b 001b 010b 011b 100b	e. Applicable for both pow  Na me  Start time 0  Start time 256  Start time 512  Start time 768  Start time 1024	Description Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024	Project All All All All All All				
	Value N 000b 001b 010b 011b 100b	e. Applicable for both power.  Na me  Start time 0  Start time 256  Start time 512  Start time 768  Start time 1024  Start time 1280	Description Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024 Start time 1280	Project All All All All All All All All				
8	Value N 000b 001b 010b 011b 100b 101b	Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024 Start time 1280 Start time 1536 Start time 1792	Description Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024 Start time 1280 Start time 1536	Project All All All All All All All All All				
8 7:6	Sequence   Value N   000b   001b   010b   100b   110b   111b   Reserved	Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024 Start time 1280 Start time 1536 Start time 1792	Description Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024 Start time 1280 Start time 1536 Start time 1792	Project All All All All All All All All All Al				
_	sequence  Value N  000b  001b  010b  100b  101b  110b  111b  Reserved  LATE_SI  Delay bet	Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024 Start time 1280 Start time 1536 Start time 1792 d Project: All	Description Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024 Start time 1280 Start time 1536 Start time 1792 Format: Project: ato successive RAM banks in number of cdclks.	Project All All All All All All All All All Al				
_	sequence  Value N  000b  001b  010b  100b  101b  110b  111b  Reserved  LATE_SI  Delay bet	Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024 Start time 1280 Start time 1792 d Project: All IGNAL_DELAY tween late signals going in ting on and off conditions.	Description Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024 Start time 1280 Start time 1536 Start time 1792 Format: Project: ato successive RAM banks in number of cdclks.	Project All All All All All All All All All Al				
_	value N 000b 001b 010b 011b 100b 110b 111b Reserved LATE_SI Delay bet power gar	Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024 Start time 1280 Start time 1792 d Project: All IGNAL_DELAY tween late signals going in ting on and off conditions.	Description Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024 Start time 1280 Start time 1536 Start time 1792 Format: Project: atto successive RAM banks in number of cdclks.	Project All All All All All All All All All Al				
_	value N 000b 001b 010b 011b 100b 111b 111b Reserved LATE_SI Delay bet power ga	Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024 Start time 1280 Start time 1792 d Project: All IGNAL_DELAY tween late signals going in ting on and off conditions.	Description Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024 Start time 1280 Start time 1536 Start time 1792  Format:  Project:  nto successive RAM banks in number of cdclks.	Project All All All All All All All All All Al				
_	sequence  Value N  000b  001b  010b  101b  100b  111b  Reserved  LATE_SI  Delay bet power gar  Value N  00b	Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024 Start time 1280 Start time 1536 Start time 1792 d Project: All IGNAL_DELAY tween late signals going inting on and off conditions. Na me Start time 0	Description Start time 0 Start time 256 Start time 512 Start time 768 Start time 1024 Start time 1280 Start time 1536 Start time 1792  Format: Project: ato successive RAM banks in number of cdclks.  Description Start time 0	Project All All All All All All All All All Al				



4:3	MID_SIG	SNAL_DELAY	Project: All		
		etween mid signals going i ating on and off conditions	nto successive RAM banks in number of cdclks. Applicab	le for both	
	Value	Na me	Description	Project	
	00b	Start time 0	Start time 0	All	
	01b	Start time 256	Start time 256	All	
	10b	Start time 512	Start time 512	All	
	11b	Start time 768	Start time 768	All	
2	Reserve	ed Project: All	Format: MBZ		
1:0	_	SIGNAL_DELAY	Project: All into successive RAM banks in number of cdclks. Applica	ble for	
		ver gating on and off cond		210 101	
	2011 901				
	Value	Na me	Description	Project	
		Na me Start time 0	Description Start time 0	Project All	
	Value		•	Project All All	
	Value 00b	Start time 0	Start time 0	All	

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# 3.1.4.2 PF\_WIN\_POS—Panel Fitter Window Position

	F	PFA_WIN	PO	S—Panel Fitter A Window Position
Register Ty	ype:	MMI	0	
Address O	ffset:	6807	<b>7</b> 0h	
Project:		All		
<b>Default Val</b>	ue:	0000	00000	h
Access:		R/W		
Size (in bit	s):	32		
Double But	ffer Update Po	oint: Star	of ve	rtical blank after armed
Double Bu	ffer Armed By	v: Write	e to P	FA_WIN_SZ
Bit De				scription
31:29	Reserved	Project:	All	Format:
28:16	XPOS	Project:	All	
	The X coordi of horizontal		s) of th	ne upper left most pixel of the display window. Measured from the end
15:12	Reserved	Project:	All	Format:
11:0	YPOS	Project:	All	
		,		e upper left most pixel of the display window. Measured from the end Region (or end of the vertical interval, whatever).



# PFB\_WIN\_POS—Panel Fitter B Window Position

MMIO **Register Type: Address Offset:** 68870h Project: ΑII

00000000h **Default Value:** Access: R/W Size (in bits): 32

Double Buffer Update Point:
Double Buffer Armed By: Start of vertical blank after armed

Double Bu	ffer Armed By	. Writ	e to PFB_	WIN_SZ
Bit De				scription
31:29	Reserved	Project:	All	Format:
28:16	XPOS	Project:	All	
	The X coording of horizontal I	\ I	s) of the u	pper left most pixel of the display window. Measured from the end
15:12	Reserved	Project:	All	Format:
11:0	YPOS	Project:	All	
				per left most pixel of the display window. Measured from the end on (or end of the vertical interval, whatever).



#### 3.1.4.3 PF\_WIN\_SZ—Pane I Fitter Window Size

Coordinates are determined with a value of (0,0) being the upper left corner of the display device (rotation does not affect this). Writes to the window size arm PF registers for the pipe.

		PFA_W	IN_S	Z—Panel Fitter A Window Size	
Register Ty	ype:	MMI	0		
Address O	ffset:	6807	'4h		
Project:	All				
<b>Default Val</b>	ue:	0000	0000h		
Access:		R/W			
Size (in bits	s):	32			
Double But	ffer Update Po	oint: Star	of vert	tical blank	
Bit De				scription	
31:29	Reserved	Project:	All	Format:	
28:16	XSIZE	Project:	All		
	The horizont	al size in pixe	s of the	e desired video window.	
15:12	Reserved	Project:	All	Format:	
11:0	YSIZE	Project:	All		
	The vertical s	size in pixels o	of the d	lesired video window. LSB must be zero for interlaced modes	

	PF	B_WIN	_SZ—Panel Fitter B Window Size
Register Ty	/pe:	MMIO	
Address O	ffset:	68874h	
Project:		All	
<b>Default Val</b>	ue:	000000	00h
Access:		R/W	
Size (in bit	s):	32	
Double But	ffer Update Point:	Start of	vertical blank
Bit De			scription
31:29	Reserved Pro	oject: Al	II Format:
28:16	XSIZE Pro	oject: Al	II
	The horizontal size	in pixels o	f the desired video window.
15:12	Reserved Pro	oject: Al	II Format:
11:0	YSIZE Pro	oject: Al	II .
	The vertical size in	pixels of th	ne desired video window. LSB must be zero for interlaced modes



# 3.1.4.4 PF\_CTRL\_1—Panel Fitter Control 1

		PF	A_CTRL	_1—Panel Fitter A Control 1			
Register Ty	ype:	N	1MIO				
Address Offset:			8080h				
Project:			.II				
<b>Default Val</b>	lue:	0	0000000h				
Access:			2/W				
Size (in bit	•		2				
	ffer Update			cal blank after armed			
Bit De	Buffer Armed By: Write to PFA_WIN_SZ  De scription						
31	Enable_Pi	ne Scaler		conjune.			
01	Project:	po_ooa.o.	All				
	Default Val	IIO.	0b				
	Value Na	ı		Description	Project		
	0b	Disable		Data bypasses the scaler	All		
	1b	Enable		The scaler is enabled	All		
30	Reserved						
29	Reserved						
28	Reserved						
27	VADAPT		Project:	All			
	Puts the ac	laptive vertic	al filter into	adaptive mode, intended for use in interlace output mo	des only.		
	Value Na	me	Description	on	Project		
	0b	Disable	Adaptive f	filtering disabled	All		
	1b	Enable	Adaptive f	filtering enabled	All		
26:25	VADAPT_I		Project:	All adaptive mode, intended for use in interlace output mo	doe only		
	-		ai iiilei iiilo				
	Value Na			Description	Project		
	l <del></del>	Least Adapt		Least Adaptive (Recommended)	All		
	01b	Moderately	Adaptive	Moderately Adaptive	All		
	10b	Reserved		Reserved	All		
	11b	Most Adapti	ve	Most Adaptive	All		

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24:23	FILTER_SELECT Project: All									
	Filter co	efficient selecti	on							
	Value	Value Na me Description								
	00b	Programme	d	Programmed Coefficients (Recommended)	All					
	01b	Hardcoded	Med	Hardcoded Coefficients for Medium 3x3 Filtering	All					
	10b	Edge Enhai	nce	Hardcoded Coefficients for Edge Enhancing 3x3 Filtering	All					
	11b	Edge Softer	n	Hardcoded Coefficients for Edge Softening 3x3 Filtering	All					
22	CHR_PI Chroma			ject: All n be used to further reduce chroma bandwidth in TV modes.						
	Value	Na me	Desc	cription	Project					
	0b	Disable	Pre-f	ilter disabled	All					
	1b	Enable	Pre-f	e-filter enabled						
		•	•		•					
21	Reserve	ed								
21	Reserve									



		PF	B_CTR	L_1	I—Panel Fitter B Control 1					
Register Ty	уре:	N	ИМІО							
Address O	ffset:	6	8880h							
Project:	All									
Default Val	ue: 00000000h									
Access:	R/W									
Size (in bit										
	e Buffer Update Point: Start of vertical blank after armed e Buffer Armed By: Write to PFB_WIN_SZ									
Bit De	Tier Armed I	<u>эу. v</u>	viile lo Fr	D_V	scription					
	F	01								
31	Enable_Pi	pe_Scaler	Δ.II							
	Project:		All							
	Default Val	ue:	0b							
	Value Na	me		<b>Description</b> Property of the						
	0b	Disable	Data bypasses the scaler A							
	1b	Enable	The scaler is enabled All							
30	Reserved	Reserved								
29	Reserved									
28	Reserved									
27	VADAPT		Projec	t:	All					
	Puts the ac	daptive vertion	cal filter in	to ac	daptive mode, intended for use in interlace output mo	des only.				
	Value Na	me	Descrip	otion		Project				
	0b	Disable	Adaptive	e filte	ering disabled	All				
	1b	Enable	Adaptive	e filte	ering enabled	All				
26:25	VADAPT_I	MODE	Projec	:t:	All					
	Puts the ac	daptive vertion	cal filter in	to ac	daptive mode, intended for use in interlace output mo	des only.				
	Value Na	me			Description	Project				
	00b	Least Adapt	tive		Least Adaptive (Recommended)	All				
	01b	Moderately	Adaptive		Moderately Adaptive	All				
	10b	Reserved			Reserved	All				
	11b	Most Adapti	ive		Most Adaptive	All				



	FILTER_SELECT Project: All									
	Filter coe	Filter coefficient selection								
	Value N	Na me		Description	Project					
	00b	Programme	d	Programmed Coefficients (Recommended)	All					
	01b	Hardcoded	Med	Hardcoded Coefficients for Medium 3x3 Filtering	All					
	10b	Edge Enhar	nce	Hardcoded Coefficients for Edge Enhancing 3x3 Filtering	All					
	11b	Edge Softer	1	Hardcoded Coefficients for Edge Softening 3x3 Filtering	All					
22	CHR_PR			ject: All  n be used to further reduce chroma bandwidth in TV modes.						
				cription	Project					
	0b	Disable	Pre-f	ilter disabled	All					
	1b	Enable	Pre-f	ilter enabled	All					
	10		•		•					
21	Reserve	d								

# 3.1.5 Panel Fitter Coefficient Registers

Coefficients for the panel fitter filters are stored in sign-exponent-mantissa format. The number of mantissa bit varies based on the filter. There are three exponent bits but not all values are allowed, ranges are specified per filter. Two filter coefficients are stored in each dword, the tables below show the data packing in each of the words. Unused bits are considered reserved and should be written zero. The default value of all coefficient registers is 00000000h. Coefficients greater than 1.0 are only allowed in the center tap of the filter, center coeffs can not use the "100" exponent.

For RGB modes the Luma and Chroma filter coeffs are programmed with the same values.

Panel Fitter Coefficient Definition											
Project:	All										
Bit De		scription									
15	Sign_bit Project:	А	I								
	Value Na	me	Description	Project							
	0b	Positive	Positive	All							
	1b	Negative	Negative	All							



14	Reserved	Project:	All	Form	nat: MBZ
13:12	Exponent_l	oits			
	Project:		All		
	The meaning	g of the expor	ent bit	s varies for center tap or non-center tap coeffic	ients.
	Value Na	me		Description	Project
	00b	2 or 0.125		Center taps: 2 or mantissa is b.bbbbbb	All
				Non-center taps: 0.125 or mantissa is 0.000bbbbbbbb	
	01b	1		1 or mantissa is 0.bbbbbbbb	All
	10b	0.5		0.5 or mantissa is 0.0bbbbbbb	All
	11b	0.25		0.25 or mantissa is 0.00bbbbbbb	All
	others	Reserved		Reserved	All
11:3	Mantissa		Projec	xt: All	
				d on the filter, but the MSB of the mantissa is a $1.9$ bits of mantissa.	always bit 11.
	Non-center	tap coefficient	s use o	only the upper 7 bits of mantissa and the lower	2 bits are ignored.
2:0	Reserved	Project:	All	Form	nat: MBZ



#### 3.1.6 Panel Fitter Horizontal Coefficients

Coefficients are packed in the horizontal coefficient registers as follows (with the letter representing the tap and the number representing the coefficient set):

Address	bits [31:16]	bits[15:0]
68x00	B0	A0
68x04	D0	C0
68x08	F0	E0
68x0C	A1	G0
68x10	C1	B1

etc....

# 3.1.6.1 PF\_HFILT L\_COEF—Panel Fitter Horizontal Luma/Red Coefficients

PFA_HFILTL_COEF—Panel Fitter A Horizontal Luma/Red Coefficients									
Register Ty	pe: Mi	MIO							
<b>Address Of</b>	<b>fset:</b> 68	100h							
Project:	All								
Default Valu	fault Value: 00000000h								
Access:	R/	W							
Size (in bits	60	x32							
Center coef	17 phases of 7 taps require 60 dwords Center coefficient is 1.2.9 Other coefficients are 1.2.7								
DWord Bi	t				Description				
059	31:16	Coefficient2	Project:	All	Format:	Panel Fitter Coefficient Definition			
	15:0	Coefficient1	Project:	All	Format:	Panel Fitter Coefficient Definition			



#### PFB\_HFILTL\_COEF—Panel Fitter B Horizontal Luma/Red Coefficients

Register Type: MMIO
Address Offset: 68900h
Project: All
Default Value: 0000000

 Default Value:
 00000000h

 Access:
 R/W

 Size (in bits):
 60x32

17 phases of 7 taps require 60 dwords

Center coefficient is 1.2.9 Other coefficients are 1.2.7

DWord B	t		Description					
059	31:16	Coefficient2	Project:	All	Format:	Panel Fitter Coefficient Definition		
	15:0	Coefficient1	Project:	All	Format:	Panel Fitter Coefficient Definition		

# 3.1.6.2 PF\_HFILT C\_COEF—Panel Fitter Horizontal Chroma/Green and Blue Coefficients

## PFA\_HFILTC\_COEF—Panel Fitter A Horizontal Chroma/Green and Blue Coefficients

Register Type: MMIO
Address Offset: 68200h
Project: All

 Default Value:
 00000000h

 Access:
 R/W

 Size (in bits):
 60x32

17 phases of 7 taps require 60 dwords

Center coefficient is 1.2.9
Other coefficients are 1.2.7

DWord B	t	Description				
059	31:16	Coefficient2	Project:	All	Format:	Panel Fitter Coefficient Definition
	15:0	Coefficient1	Project:	All	Format:	Panel Fitter Coefficient Definition



#### PFB\_HFILTC\_COEF—Panel Fitter B Horizontal Chroma/Green and Blue Coefficients

Register Type: MMIO
Address Offset: 68A00h
Project: All
Default Value: 00000000h

Access: R/W Size (in bits): 60x32

17 phases of 7 taps require 60 dwords

Center coefficient is 1.2.9
Other coefficients are 1.2.7

DWord B	it	Description					
059	31:16	Coefficient2	Project:	All	Format:	Panel Fitter Coefficient Definition	
	15:0	Coefficient1	Project:	All	Format:	Panel Fitter Coefficient Definition	

#### 3.1.7 Panel Fitter Vertical Coefficients

Coefficients are packed in the vertical coefficient registers as follows (with the letter representing the tap and the number representing the coefficient set). When the vertical filter is in 3 line mode the three taps used are A, C & E, B & C must be programmed to zero in three line mode.

Address	bits [31:16]	bits[15:0]
68x00	B0	A0
68x04	D0	C0
68x08	A1	E0
68x0C	C1	B1
68x10	E1	D1

etc....



#### 3.1.7.1 PF\_VFILT L\_COEF—Panel Fitter Vertical Luma/Red Coefficients

PFA\_VFILTL\_COEF—Panel Fitter A Vertical Luma/Red Coefficients

Register Type: MMIO
Address Offset: 68300h
Project: All

 Default Value:
 00000000h

 Access:
 R/W

 Size (in bits):
 43x32

17 phases of 5 taps require 43 dwords

Center coefficient is 1.2.9 Other coefficients are 1.2.7

DWord B	t	Description				
042	31:16	Coefficient2	Project:	All	Format:	Panel Fitter Coefficient Definition
	15:0	Coefficient1	Project:	All	Format:	Panel Fitter Coefficient Definition

#### PFB\_VFILTC\_COEF—Panel Fitter B Vertical Chroma/Green and Blue Coefficients

Register Type: MMIO
Address Offset: 68C00h
Project: All
Default Value: 00000000h

Access: R/W Size (in bits): 43x32

17 phases of 5 taps require 43 dwords

Center coefficient is 1.2.9 Other coefficients are 1.2.7

DWord B	t	Description					
042	31:16	Coefficient2	Project:	All	Format:	Panel Fitter Coefficient Definition	
	15:0	Coefficient1	Project:	All	Format:	Panel Fitter Coefficient Definition	



# 3.1.7.2 PF\_VFILT C\_COEF—Panel Fitter Vertical Chroma/Green and Blue Coefficients

#### PFA\_VFILTC\_COEF—Panel Fitter A Vertical Chroma/Green and Blue Coefficients

Register Type: MMIO
Address Offset: 68400h
Project: All
Default Value: 00000000h
Access: R/W
Size (in bits): 43x32

17 phases of 5 taps require 43 dwords

Center coefficient is 1.2.9
Other coefficients are 1.2.7

DWord B	t	Description					
042	31:16	Coefficient2	Project:	All	Format:	Panel Fitter Coefficient Definition	
	15:0	Coefficient1	Project:	All	Format:	Panel Fitter Coefficient Definition	

## PFB\_VFILTC\_COEF—Panel Fitter B Vertical Chroma/Green and Blue Coefficients

Register Type: MMIO
Address Offset: 68C00h
Project: All
Default Value: 00000000h
Access: R/W
Size (in bits): 43x32

17 phases of 5 taps require 43 dwords

Center coefficient is 1.2.9
Other coefficients are 1.2.7

DWord B	t	Description						
042	31:16	Coefficient2	Project:	All	Format:	Panel Fitter Coefficient Definition		
	15:0	Coefficient1	Project:	All	Format:	Panel Fitter Coefficient Definition		

# 3.1.8 FDI AFE Control (6C000h-6DFFFh)

Documented separately



# 4. Plane Controls (70000h-7FFFFh)

### 4.1.1 Display Pipeline A

#### 4.1.1.1 PIPEA DSL—Pipe A Display Scan Line

#### PIPEA\_DSL—Pipe A Display Scan Line

Register Type: MMIO
Address Offset: 70000h
Project: All
Default Value: 00000000h
Access: Read Only
Size (in bits): 32

This register enables the read back of the display pipe vertical "line counter". The value increments at the leading edge of HSYNC and can be safely read any time. The value resets to line zero at the first active line of the display. In interlaced display timings, the scan line counter provides the current line in the field. One field will have a total number of lines that is one greater than the other field. Content locked display will adjust the total number of lines displayed.

Bit De	scription								
31	Current_F	ield							
	Project:		All						
	Default Va								
	Provides read back of the current field being displayed on display pipe A.								
	Value Na	n me	Description		Project				
	0b	Odd	First field (od	d field)	All				
	1b	Even	Second field	(even field)	All				
30:13	Reserved	Proje	ect: All	Format:					
12:0	Line_Cou	Projec	t: All						
	Provides read back of the display pipe A vertical line counter. This is an indication of the current display scan line to be used by software to synchronize with the display.								



#### 4.1.1.2 PIPEA SLC—Pipe A Display Scan Line Count Range Compare

PI	PIPEA_SLC—Pipe A Display Scan Line Count Range Compare						
Register Type:	MMIO						
Address Offset:	70004h						
Project:	Project: All						
<b>Default Value:</b>	00000000h						
Access:	access:						
Size (in hits):	32						

**[DevSNB]** The scan line number register is compared with the display line value from the pipe timing generator. The result of this comparison is used to generate interrupts and render responses. The value programmed should be desired value – 1, so for line 0, the value programmed is VTOTAL, and for line 1, the value programmed is 0. Content locked display will adjust the total number of lines displayed.

**[ILK]** The Top and Bottom Line Count Compare registers are compared with the display line values from pipe A timing generator. The Top compare register operator is a less than or equal, while the Bottom compare register operator is a greater than or equal. The results of these 2 comparisons are used to generate interrupts. For range check, the value programmed should be the (desired value – 1), so for line 0, the value programmed is VTOTAL, and for line 1, the value programmed is 0. Content locked display will adjust the total number of lines displayed.

Bit De				scription			
31	Inclusive/Exclusive						
	Project: ILK						
	Default Value: 0b						
	Value Na	me	Description			Project	
	0b	Exclusive	Exclusive: outside	e of the range		All	
	1b	Inclusive	Inclusive: within t	he range		All	
30:29	Reserved		Project:	ILK	Forma	t: MBZ	
28:16	Start_Sca	n_Line_Number	Project:	ILK	Forma	t:	
	Range:		0Vertica	l Total			
	This field s	specifies the start	ing scan line numb	er of the Scan Line Window.			
	Scan line (	0 is the first line o	of the display frame	•			
15:13	Reserved		Project:	ILK	Forma	t: MBZ	
12:0	End_Scan	_Line_Number	Project:	ILK	Forma	t:	
	Range:		0Vertical Tota	I			
	This field s	specifies the endi	ng scan line numbe	er of the Scan Line Window.			
	Scan line (	0 is the first line o	of the display frame				
31:13	Reserved		Project:	DevSNB	Forma	t: MBZ	
12:0	Scan_Line	e_Number					
	Project:	D	evSNB				
	Range	0	Vertical Total				
	This field s	pecifies the scan	line number on wh	ich to generate scan line inte	rrupt and render r	esponse.	



		PIPEACONF	—Pipe A Configuration Register	
Register Ty	/pe:	MMIO		
Address Of	-	70008h		
Project:		All		
Default Val	ue:	00000000	h	
Access:		R/W		
Size (in bits	s):	32		
Double But	ffer Update P	oint: Start of ve	ertical blank OR pipe disabled	
Bit De			scription	
31	Pipe_A_Ena	able		
	Project:	All		
	Default Valu	e: 0b		
Setting this bit to the value of one, turns on pipe A. This must be done before any planes are on this pipe. Changing it to a zero should only be done when all planes that are assigned to have been disabled. Turning the pipe enable bit off disables the timing generator in this pipe Synchronization pulses to the display are not maintained if the timing generator is disabled. timing registers must contain valid values before this bit is enabled.				
	Value Na	me	Description	Project
	0b	Disable	Disable	All
	1b	Enable	Enable	All
30	Pipe_State			
	Project:	All		
	Default Valu	e: 0b		
	This bit indic	ates the actual stat	e of the pipe. Since there can be some delay between dising off, this bit indicates the true current state of the pipe.	sabling the
	Value Na	me	Description	Project
	0b	Disable	Disable State	All
	1b	Enable	Enable State	All
29	Reserved	Project: All	Format:	
28:27	Reserved		. 5	
26	Reserved			
26	Reserved	Project: De	vILK Format:	



25:24 Pipe\_A\_Palette/Gamma\_Unit\_Mode

Project: All Default Value: 0b

These bits select which mode the pipe gamma correction logic works in. See the Display Palette Registers for information on the different palette/gamma modes. Other gamma units such as in the sprite are unaffected by this bit.

Value Na	me me	Description	Project
00b	8 bit	8-bit Legacy Palette Mode	All
01b	10 bt	10-bit Precision Palette Mode	All
10b	12 bit	12-bit Interpolated Gamma Mode	All
11b	Reserved	Reserved	All

23:21 Interlaced\_Mode

Project: All Default Value: 0b

These bits are used for software control of interlaced behavior. They are updated immediately if the pipe is off, or in the vertical blank after programming if pipe is enabled.

Note: VGA display modes do not work while in interlaced fetch modes

Value N	a me	Description	Project
000b	PF-PD	Progressive Fetch / Progressive display	All
001b	PF-ID	Progressive Fetch / Interlaced display (TV) Requires panel fitting to be enabled	All
010b	Reserved	Reserved	All
011b	IF-ID	Interlaced Fetch / Interlaced display (programmable sync, normal interlaced)	All
100b	IF-ID-DBL	Interlaced embedded panel with interlaced fetch (pixel doubling power savings mode, no PF enabled)	All
101b	PF-ID-DBL	Interlaced embedded panel with progressive fetch (pixel doubling power savings mode with PF enabled) Requires panel fitting to be enabled	All
others	Reserved	Reserved	All



20 **Display\_Power\_Mode\_Switch** 

Project: All Default Value: 0b

This bit is used for software to set the power saving progressive mode. The pipe enters or exits the power savings mode on the vblank after this bit is written. Please note that bits 17:16 of this register must be set to 00 in order for this bit to take effect.

Value Na me		Description	Project
0b	Progressive	Pipe is in progressive mode	All
1b	Power save	Pipe is in power savings progressive mode	All

19 Reserved: Must be zero

18 Reserved: Must be zero

17:16 Refresh\_Rate\_CxSR\_Mode\_Association

Project: All Default Value: 0b

These bits select how refresh rates are tied to big FIFO mode on pipe A. When they are set to anything other than 00, bits 23:21 of this register must be programmed to 000. Switching between 01 and 10 settings directly is not allowed. Software must program this field to 00 before switching. Software is responsible for enabling this mode only for integrated display panels that support corresponding mode.

Value N	a me	Description	Project
00b	None	No dynamic refresh rate change enabled. Software control through bits 23:21 only	All
01b	PTP	Progressive-to-progressive refresh rate change enabled and tied to big FIFO mode. For the CPU and PCH, link and data M and N 1 values are used for high power settings. For the PCH, pixel clock FPA0 values are used for high power settings	All
10b	PTI	Progressive-to-interlaced refresh rate change enabled and tied to big FIFO mode. Pixel clock value does not change in this case. However, data and link M values in the CPU and PCH (as appropriate) are divided by 2 (shifted right by 1 bit) when in big FIFO mode. If scaling is enabled, the planes will fetch progressive data which will be interlaced by the panel fitter. If scaling is disabled, the planes will fetch interlaced data, reducing the amount of data fetched	All
11b		Reserved	All



#### 15:14 **Display\_Rotation\_Info**

Project: All Default Value: 0b

These are informative bits set by software to indicate this pipe is being rotated. Software should set these for both hardware and software rotation cases. Hardware rotation is <u>not</u> enabled through these bits.

Value N	a me	Description	Project
00b	None	No rotation on this pipe	All
01b	90	90° rotation on this pipe	All
10b	180	180° rotation on this pipe	All
11b	270	270° rotation on this pipe	All

#### 13 Color\_Range\_Select

Project: All Default Value: 0b

This bit is used to select the color range of outputs.

Value N	a me	Description	Project
0b	Full	Apply full 0-2 <sup>n</sup> - 1 color range to the output	All
1b	CE	Apply CE color range to the output	All

#### 12:11 Pipe\_output\_color\_space\_select

Project: All Default Value: 0b

Informs the ports of the pipe output color space. Plane data formats and CSC need to be programmed to match what is selected here.

Value N	a me	Description	Project
00b	RGB	RGB	All
01b	YUV 601	YUV 601	All
10b	YUV 709	YUV 709	All
11b	Reserved	Reserved	All

#### 10:9 Reserved

10	0:9	Reserved	Project:	DevILK	Format:	
	8	Reserved	Project:	All	Format:	MBZ



7:5 Bits\_Per\_Color

Project: All Default Value: 0b

This field selects the number of bits per color sent to a receiver device connected to this pipe. Color format takes place on the Vblank after being written. Color format change can be done independent of a pixel clock change.

Software should enable dithering in the pipe/port if selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer.

Value Na me		Description	Project
000b	8 bits	8 bits per color	All
001b	10 bits	10 bits per color	All
010b	6 bits	6 bits per color	All
011b	12 bits	12 bits per color	All
1XXb	Reserved	Reserved	All

#### 4 Dithering\_enable

Project: All Default Value: 0b
This bit enables dithering

Value N	a me	Description				
0b	Disable	Dithering disabled	All			
1b	Enable	Dithering enabled	All			

#### 3:2 Dithering\_type

Project: All
Default Value: 0b
These bits select dithering type.

Value Na me		Description	Project
00b	Spatial	Spatial only	All
01b	ST1	Spatio-Temporal 1	All
10b	Reserved	Reserved	All
11b	Reserved	Reserved	All

#### 1 Reserved

0 Reserved Project: All Format: MBZ

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# **4.1.2 Display Pipeline A Counters and Timestamps**

## 4.1.2.1 PIPEA\_FRMCOUNT—P ipe A Frame Counter

PIPEA_FRMCOUNT—Pipe A Frame Counter							
Register Ty	ype:	MMIO					
Address O	ffset:	70040h					
Project:		All					
<b>Default Val</b>	ue:	00000000h					
Access:		Read Only					
Size (in bits	s):	32					
Bit De					scription		
31:0	Pipe.	_Frame_Counter	Project:	All	Format:		
	Provides read back of the display pipe frame counter. This counter increments on every start of vertical blank and rolls over back to 0 after 2^32 frames.						

## 4.1.2.2 PIPEA\_FLI PCOUNT—Pipe A Flip Counter

	PIPEA_FLIPCOUNT—Pipe A Flip Counter							
Register Type:		MMIO						
Address Of	ffset:	70044h						
<b>Project:</b>		All						
Default Value:		00000000h						
Access:		Read Only						
Size (in bits	s):	32						
Bit De					scription			
31:0	Pipe_	_Flip_Counter	Project:	All	Format:			
	of the	primary plane on	this pipe. Th	is includes	nter. This counter increments on each flip of the surface s command streamer asynchronous and synchronous surface address. It rolls over back to 0 after 2^32 flips.			



# 4.1.2.3 PIPEA\_ FRMTIMESTAMP—Pipe A Frame Time Stamp

		PIPEA_FRMTIMESTAMP—	Pipe A Fram	e Time St	amp	
Register Ty	ype:	MMIO				
Address O	ffset:	70048h				
Project:		All				
Default Val	ue:	00000000h				
Access:		Read Only				
Size (in bit	s):	32				
Bit De			scription			
31:0	Pipe	_Frame_Time_Stamp		Project:	All	Format:
		ides read back of the display pipe frame ti of vertical blank. The TIMESTAMP regist				

# 4.1.2.4 PIPEA\_ FLIPTIMESTAMP—Pipe A Flip Time Stamp

	PIPEA_FLIPTIMESTAMP—Pipe A Flip Time Stamp						
Register Ty	ype: MMIO						
Address O	ffset: 7004Ch						
Project:	All						
<b>Default Val</b>	ue: 00000000h						
Access:	Read Only						
Size (in bits	s): 32						
Bit De		scription					
31:0	Pipe_Flip_Time_Stamp	Project: All Format:					
	of the surface of the primary plane on this pi	me stamp. The time stamp value is sampled on each flip ipe. This includes command streamer asynchronous and ne primary plane surface address. The TIMESTAMP ralue.					

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# 4.1.3 Display Timestamp

This register provides an elapsed real-time value that can be used as a timestamp for GPU events over short periods of time.

The register counts at a constant frequency by adjusting the increment amount according to the actual core display clock frequency. SW therefore does not need to know the reference clock frequency.

## 4.1.3.1 TIMESTAMP\_HI—T ime Stamp High Value

	TIMESTAMP_HI—Time Stamp High Value							
Register Ty Address O Project: Default Val Access:	### 10070h  All  ue: 00000000h  R/W Clear							
Size (in bit	s): 32							
Bit De	scription							
31:0	TIMESTAMP_High Project: All Format:  This field increments every microsecond. The value in this field is latched in the Pipe Flip TIMESTAMP registers when flips occur, and in the Pipe Frame TIMESTAMP registers at start of vertical blank. The register value will reset if any value is written to it. The register is not reset by a graphics software reset.							



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# 4.1.4 Display Pipeline B

# 4.1.4.1 PIPEB\_DSL—Pipe B Display Scan Line

		PIPE	B_DSL—Pipe B D	Display Scan L	_ine				
Register Ty	/pe: MMIO								
Address O	ffset: 71000	h							
Project:	All								
Default Val	ue: 00000	000h							
Access:	Read	Only							
Size (in bit	s): 32								
See Pipe A	description								
Bit De	De scription								
31	Current_Field								
	Project:		All						
	Default Valu	e:	0b						
	Provides read back of the current field being displayed on display pipe B.								
	Value Na	me	Description					Project	
	0b	First	First field (odd fi	eld)				All	
	1b	Second	Second field (ev	en field)				All	
30:13	Reserved			Project:	All	Format:	MB	Z	
00.10									
12:0	Line_Count	ter_for_Displa	ıy	Project:	ΑII	Format:			



# 4.1.4.2 PIPEB\_SLC—Pipe B Display Scan Line Count Range Compare

	PIPEB	SLC—P	ipe B C	Display Scan Line Count Range Compare	
Register Ty Address Of Project:	ffset: 7100 All	)4h	-		
Default Val	ue: 0000 R/W	00000h			
Size (in bits					
See Pipe A	-	n			
Bit De	•			scription	
31	Inclusive/	Exclusive			
	Project:		All		
	Default Va	lue:	0b		
	Value Na	n me	Descrip	tion	Project
	0b	Exclusive	Exclusiv	e: outside of the range	All
	1b	Inclusive	Inclusive	: within the range	All
30:29	Reserved	Project	: All	Format:	_
28:16	Start_Sca	n_Line_Num	ber		
	Project:		All		
	Default Va	lue:	0b		
	Format:		U13	Scan lines, where scan line 0 is the first line of the display	frame.
	Range		0Disp	lay Buffer height in lines-1	
	See pipe A	A description			
15:13	Reserved	Project	: All	Format:	
12:0	End_Scan	_Line_Numl	ber		
	Project:		All		
	Default Va	lue:	0b		
	Format:		U13	Scan lines, where scan line 0 is the first line of the display	frame.
	Range		0Disp	lay Buffer height in lines-1	
	See pipe A	A description			



		PIPEBCONF	—Pipe B Configuration Register					
Register Ty	vpe:	MMIO						
Address Of		71008h	71008h					
Project:		All	All					
<b>Default Val</b>	ue:	000000001	0000000h					
Access:		R/W						
Size (in bits	s):	32						
Double But	ffer Update P	oint: Start of ve	rtical blank OR pipe disabled					
Bit De								
31	Pipe_B_Ena	able						
	Project:	All						
	Default Valu	e: 0b						
	Setting this bit to the value of one, turns on pipe B. This must be done before any planes are enabled on this pipe. Changing it to a zero should only be done when all planes that are assigned to this pipe have been disabled. Turning the pipe enable bit off disables the timing generator in this pipe. Synchronization pulses to the display are not maintained if the timing generator is disabled. Pipe timing registers must contain valid values before this bit is enabled.							
	Value Na	me	Description	Project				
	0b	Disable	Disable	All				
	1b	Enable	Enable	All				
30	Pipe_State							
50	Project:	All						
	1							
	Default Value: 0b  This bit indicates the actual state of the pipe. Since there can be some delay between disabling the pipe and the pipe actually shutting off, this bit indicates the true current state of the pipe.							
	Value Na	me	Description	Project				
	0b	Disable	Disable	All				
	1b	Enable	Enable	All				
29	Reserved	Project: All	Form	nat:				
28:27	Reserved	.,						
26	Reserved							
		Project: DevIL	,	Format:				

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25:24 Pipe\_B\_Palette/Gamma\_Unit\_Mode

Project: All Default Value: 0b

These bits select which mode the pipe gamma correction logic works in. See the Display Palette Registers for information on the different palette/gamma modes. Other gamma units such as in the sprite are unaffected by this bit.

Value Na	me me	Description	Project
00b	8 bit	8-bit Legacy Palette Mode	All
01b	10 bit	10-bit Precision Palette Mode	All
10b	12 bit	12-bit Interpolated Gamma Mode	All
11b	Reserved	Reserved	All

23:21 Interlaced\_Mode

Project: All Default Value: 0b

These bits are used for software control of interlaced behavior. They are updated immediately if the pipe is off, or in the vertical blank after programming if pipe is enabled.

Note: VGA display modes do not work while in interlaced fetch modes

Value Na me		Description	Project
000b	PF-PD	Progressive Fetch / Progressive display	All
001b	PF-ID	Progressive Fetch / Interlaced display (TV) Requires panel fitting to be enabled	All
010b	Reserved	Reserved	All
011b	IF-ID	Interlaced Fetch / Interlaced display (programmable sync, normal interlaced)	All
100b	IF-ID-DBL	Interlaced embedded panel with interlaced fetch (pixel doubling power savings mode, no PF enabled)	All
101b	PF-ID-DBL	Interlaced embedded panel with progressive fetch (pixel doubling power savings mode with PF enabled) Requires panel fitting to be enabled in progressive mode	All
11Xb	Reserved	Reserved	All



20 **Display\_Power\_Mode\_Switch** 

Project: All Default Value: 0b

This bit is used for software to set the power saving progressive mode. The pipe enters or exits the power savings mode on the vblank after this bit is written. Please note that bits 17:16 of this register must be set to 00 in order for this bit to take effect.

Value Na me		Description			
0b Progressive		Pipe is in progressive mode	All		
1b Power Save		Pipe is in power savings progressive mode	All		

19 Reserved: Must be zero

18 Reserved: Must be zero

17:16 Refresh\_Rate\_CxSR\_Mode\_Association

Project: All Default Value: 0b

These bits select how refresh rates are tied to big FIFO mode on pipe B. When they are set to anything other than 00, bits 23:21 of this register must be programmed to 000. Switching between 01 and 10 settings directly is not allowed. Software must program this field to 00 before switching. Software is responsible for enabling this mode only for integrated display panels that support corresponding mode.

Value N	a me	Description	Project
00b	None	No dynamic refresh rate change enabled. Software control through bits 23:21 only	All
01b	PTP	Progressive-to-progressive refresh rate change enabled and tied to big FIFO mode. For the CPU and PCH, link and data M and N 1 values are used for high power settings. For the PCH, pixel clock FPA0 values are used for high power settings	All
10b	PTI	Progressive-to-interlaced refresh rate change enabled and tied to big FIFO mode. Pixel clock value does not change in this case. However, data and link M values in the CPU and PCH (as appropriate) are divided by 2 (shifted right by 1 bit) when in big FIFO mode. If scaling is enabled, the planes will fetch progressive data which will be interlaced by the panel fitter. If scaling is disabled, the planes will fetch interlaced data, reducing the amount of data fetched	All
11b	Reserv ed	Reserved	All

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15:14 **Display\_Rotation\_Info** 

Project: All Default Value: 0b

These are informative bits set by software to indicate this pipe is being rotated. Software should set these for both hardware and software rotation cases. Hardware rotation is <u>not</u> enabled through these bits.

Value N	a me	Description	Project
00b	None	No rotation on this pipe	All
01b	90	90° rotation on this pipe	All
10b	180	180° rotation on this pipe	All
11b	270	270° rotation on this pipe	All

13 Color\_Range\_Select

Project: All Default Value: 0b

This bit is used to select the color range of outputs.

Value Na me		Description			
0b	Full	Apply full 0-2 <sup>n</sup> - 1 color range to the output	All		
1b	CE	Apply CE color range to the output	All		

12:11 Pipe\_output\_color\_space\_select

Project: All Default Value: 0b

Informs the ports of the pipe output color space. Plane data formats and CSC need to be programmed to match what is selected here.

Value N	a me	Description	Project
00b	RGB	RGB	All
01b	YUV 601	YUV 601	All
10b	YUV 709	YUV 709	All
11b	Reserved	Reserved	All

10:9 Reserved

10:9	Reserved	Project:	DevILK	Format:
8	Reserved	Project:	All	Format: MBZ



7:5 Bits\_Per\_Color

Project: All Default Value: 0b

This field selects the number of bits per color sent to a receiver device connected to this pipe. Color format takes place on the Vblank after being written. Color format change can be done independent of a pixel clock change.

Software should enable dithering in the pipe/port if selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer.

Value N	a me	Description	Project
000b	8 bits	8 bits per color	All
001b	10 bits	10 bits per color	All
010b	6 bits	6 bits per color	All
011b	12 bits	12 bits per color	All
1XXb	Reserved	Reserved	All

4 Dithering\_enable

Project: All
Default Value: 0b
This bit enables dithering

Value Na me		Description			
0b	Disable	Dithering disabled	All		
1b	Enable	Dithering enabled	All		

3:2 Reserved

1 Reserved

0 Reserved Project: All Format: MBZ

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# **4.1.5** Display Pipeline B Counters and Timestamps

## 4.1.5.1 PIPEB\_FRMCOUNT—P ipe B Frame Counter

PIPEB_FRMCOUNT—Pipe B Frame Counter								
Register Typ	e: MMIO							
Address Offs	set: 71040h							
Project:	All							
<b>Default Value</b>	e: 00000000h							
Access:	Read Only							
Size (in bits)	32							
Bit De				scription				
31:0 <b>F</b>	Pipe_Frame_Counter	Project:	All	Format:				
	See Pipe A description							

# 4.1.5.2 PIPEB\_FLI PCOUNT—Pipe B Flip Counter

	PIPEB_FLIPCOUNT—Pipe B Flip Counter								
Register Ty	-	MMIO							
Address Of	fset:	71044h							
Project:		All							
<b>Default Valu</b>	ue:	00000000h							
Access:		Read Only							
Size (in bits	s):	32							
Bit De					scription				
31:0 <b>Pipe</b>		Flip_Counter	Project:	All	Format:				
	See F	Pipe A description	n						



## 4.1.5.3 PIPEB FRMTIMESTAMP—Pipe B Frame Time Stamp

		PIPEB_FRMTIMESTA	AMP—Pi	pe B Fram	ne Time Star	np	
Register Typ	oe:	MMIO					
Address Off	set:	71048h					
Project:		All					
<b>Default Valu</b>	e:	0000000h					
Access:		Read Only					
Size (in bits)	):	32					
Bit De				scription			
31:0	Pipe_	Frame_Time_Stamp			Project:	All	Format:
,	See F	Pipe A description					

# 4.1.5.4 PIPEB FLIPTIMESTAMP—Pipe B Flip Time Stamp

		PIPEB_FLIPTIM	IESTAMP-	-Pipe B Flip	Time Stam	р	
Register Ty	ype:	MMIO					
Address Of	ffset:	7104Ch					
Project:		All					
<b>Default Val</b>	ue:	00000000h					
Access:		Read Only					
Size (in bits	s):	32					
Bit De				scription			
31:0	Pipe	_Flip_Time_Stamp			Project:	All	Format:
	See	Pipe A description					

# 4.1.6 Cursor A Plane Control Registers

The CURACNTR active register will be updated on the vertical blank or when pipe is disabled, after the CURABASE or CURAPOPUPBASE trigger register is written, or when cursor A is not yet enabled – thus providing an atomic update of the cursor A control and base address registers.



# 4.1.6.1 CURACNT R—Cursor A Control Register

		Cl	JRACNT	R—Cursor A Control Register					
Register Ty	vne:		MMIO	3					
Address O			70080h						
Project:			All						
Default Val									
Access:			R/W						
Size (in bits	s):		32						
Double But	ffer Update	Point:	Start of ve	rtical blank or pipe disabled or cursor disabled, af	ter armed				
<b>Double But</b>	ffer Armed I	Ву:	Write to Cl	URABASE or CURAVGAPOPUPBASE					
For Hi-res	modes Curs	sor A is co	onnected t	to pipe A only. For VGA popup it follows the	VGA pipe	select.			
Bit De				scription					
31:28	Reserved	Proje	ct: All	Format	t:				
27	Popup_Cu	rsor_Ena	bled						
	Project:		All						
	Default Val	ue:	0b						
				en using Cursor A as a popup cursor. When in poss as a <u>physical</u> address instead of a graphics ad		nardware			
	Value Na	me		Description	Project				
	0b	Hi-Res		Cursor A is hi-res	All				
	1b	VGA		Cursor A is popup	All				
26	Cursor_Ga	amma_En	abled						
	Project:		All						
	Default Val	ue:	0b						
				using the cursor in a non-VGA mode. In VGA pone gamma (palette) unit.	p-up operati	on, the			
	Value Na	me	Descripti	on		Project			
	0b	Bypass	Cursor pix	kel data bypasses gamma correction or palette		All			
	1b	Gamma	Cursor pix	xel data is gamma to be corrected in the pipe		All			
25	Reserved	Proje	ct: All	Format	t:				



		С	URACNTR—Cursor A Control Register					
24	Pipe_Co	lor_Space	_Conversion_Enable					
	Project:		All					
	Default Value: 0b							
			e color space conversion for the cursor pixel data. CSC mode in the pipe of the cursor pixel data.	CSC				
	Value N	la me	Description	Project				
	0b	Bypass	Cursor pixel data bypasses the pipe color space conversion logic	All				
	1b	Pass	Cursor pixel data passes through the pipe color space conversion logic	All				
23:16	Reserve	<b>d</b> Pro	ject: All Format:					
15	180°_Rotation  Project: All  Default Value: 0b  This mode causes the cursor to be rotated 180°. Only 32 bits per pixel cursors can be rotated. This field must be zero when the cursor format is 2 bits per pixel.							
	Value N	la me	Description	Project				
	0b	None	No rotation	All				
	1b 180 180° Rotation of 32 bit per pixel cursors		180° Rotation of 32 bit per pixel cursors	All				
14	Trickle_Feed_Enable Project: DevSNB Default Value: 0b							
	Value Na me Description Proje							
	0b Enable Trickle Feed Enabled - Data requests are sent whenever there is space in the Display Data Buffer							
	1b	Disable	Trickle Feed Disabled - Data requests are sent in bursts	All				
14	Reserve	d Pro	ject: DevILK Format:					
13:6	Reserve	<b>d</b> Pro	ject: All Format:					



5	Cursor M	ode Sele	ect					
	Bit 5	Bits 2:0	Mode					
	0	000	Cursor is disabled. This is the default after reset. When the cursor register value changes from enabled to disabled, the cursor will stop fetching data at the following VBLANK event.  The cursor enable can be overridden by the pipe cursor disable bit. The value of these bits do not change when disabled by the pipe cursor disable bit.					
	0	001	Reserved					
	0	010	128 x 128 32bpp AND/INVERT (not available for VGA use) See description off 64 x 64 32bpp AND/INVERT format for byte usage					
	0	011	256 x 256 32bpp AND/INVERT (not available for VGA use) See description off 64 x 64 32bpp AND/INVERT format for byte usage					
	0	100	64 x 64 2bpp Indexed 3-color and transparency mode					
	0	101	64 x 64 2bpp Indexed AND/XOR 2-plane mode					
	0	110	64 x 64 2bpp Indexed 4-color mode					
	0	111	64 x 64 32bpp AND/INVERT (not available for VGA use) For each pixel:					
			Least significant three bytes provides cursor RGB 888 color information Most Significant Byte:					
			All Ones: Opaque, show the cursor color					
			All Zeros: Transparent (color must also equal zero)					
	1	000	Other: Invert the underlying display pixel data (ignore the color)  Reserved					
	1	000	Reserved					
	1	010	128 x 128 32bpp ARGB (8:8:8:8 MSB-A:R:G:B) (not available for VGA use)					
	1	011	256 x 256 32bpp ARGB (8:8:8:8 MSB-A:R:G:B) (not available for VGA use)					
	1	100	64 x 64 32bpp AND/XOR (not available for VGA use) For each pixel: Least significant three bytes provides cursor RGB 888 color information					
			Most Significant Byte: All Ones: Opaque, show the cursor color					
			All Zeros: Transparent (color must also equal zero) Other: XOR the cursor color with the underlying display pixel data					
	1	101	128 x 128 32bpp AND/XOR (not available for VGA use) See description off 64 x 64 32bpp AND/XOR format for byte usage					
	1	110	256 x 256 32bpp AND/XOR (not available for VGA use) See description off 64 x 64 32bpp AND/XOR format for byte usage					
	1	111	64 x 64 32bpp ARGB (8:8:8:8 MSB-A:R:G:B) (not available for VGA use)					
4:3	Reserved	<b>j</b> P	Project: All Format:					
2:0	Cursor_I	Mode_S	elect[2:0]					
	Project:		All					
	Default V	alue:	0b					
	1							



## 4.1.6.2 CURABASE—Cursor A Base Address Register

Register Type: MMIO
Address Offset: 70084h
Project: All

 Default Value:
 00000000h

 Access:
 R/W

 Size (in bits):
 32

Double Buffer Update Point: Start of vertical blank or pipe disabled

#### Writes to this register arm CURA registers

This register is only used when cursor A is in the hi-res mode. In VGA popup mode CURAVGAPOPUPBASE is used instead and this register <u>must not be written.</u> This register specifies the graphics memory address at which the cursor image data is located.

Bit De	scription										
31:12	Cursor_Base	Cursor_Base_Address[31:12]									
	Project:		All								
	Address:		GraphicsA	.ddress[31:12]							
			es bits 31:12 of the <u>graphics</u> address of the base of the cursor for hi-res mode. The sused for VGA popup cursor is in the CURAVGAPOPUPBASE register.								
	be tiled. Whe	The cursor surface address must be 4K byte aligned. The cursor must be in linear memory, it cannot be tiled. When performing 180° rotation, this address does not change, hardware will internally offset to start from the last pixel of the last line of the cursor.									
11:0	Reserved	Project:	All	Format:							



# 4.1.6.3 CURAPOS—Cursor A Position Register

	CURAPOS—Curso	or A Position Register						
Register Ty	rpe: MMIO							
Address O	•							
Project:	: All							
Default Val	alue: 00000000h							
Access:	R/W							
Size (in bits	s): 32							
	fer Update Point: Start of vertical blank							
	er specifies the screen position of the curs of the active image for the display pipe th	sor. The origin of the cursor position is always the at the cursor is assigned.	upper					
Bit De		scription						
31	Cursor_Y-Position_Sign_Bit	Project:	All					
	For normal high resolution display modes, the	bit value that specifies the horizontal position of cursor. ne cursor must have at least a single pixel positioned ov or, the entire cursor must be positioned over the active ar						
30:28	Reserved Project: All	Format: MBZ						
27:16	Cursor_Y-Position_Magnitude_Bits	Project:	All					
	cursor. The sign bit of this value is provided entire cursor must be positioned over the ac	a signed 12-bit value that specifies the vertical position by bit 31of this register. For use as a VGA Popup, the ctive area of the VGA image. Enabling the border in VG register) includes the border in what is considered the						
	When performing 180° rotation, this field spet to the end of the active video area in the unit	ecifies the vertical position of the lower right corner relat ortated orientation	ive					
15	Cursor_X-Position_Sign_Bit	Project:	All					
	For normal high resolution display modes, the active screen. For use as a VGA Popup	bit value that specifies the horizontal position of cursor. The cursor must have at least a single pixel positioned over the entire cursor must be positioned over the active are GA (VGA Border Enable bit in the VGA Config register) as "active area".	ea					
14:12	Reserved Project: All	Format: MBZ						
11:0	Cursor_X-Position_Magnitude_Bits	Project:	All					
	These 12 bits provide the signed 13-bit valuabit is provided by bit 15 of this register.	e that specifies the horizontal position of cursor. The si	gn					
	When performing 180° rotation, this field sperelative to the end of the active video area in	ecifies the horizontal position of the lower right corner at the unrotated orientation.						



# 4.1.6.4 CURAVGAPOPUPBASE—Curs or A VGA Popup Base Address Register

## **CURAVGAPOPUPBASE—Cursor A VGA Popup Base Address Register**

Register Type: MMIO
Address Offset: 7008Ch
Project: All

 Default Value:
 00000000h

 Access:
 R/W

 Size (in bits):
 32

Double Buffer Update Point: Start of vertical blank or pipe disabled

#### Writes to this register arm CURA registers

This register is only used when cursor A is in the VGA popup mode. In hi-res mode CURABASE is used instead and this register <u>must not be written.</u> This register specifies the physical memory address at which the cursor image data is located.

Bit De	scription								
31:12	Cursor_VG/	Cursor_VGA_Popup_Base_Address[31:12]							
	Project:	All							
	Address:	PhysicalAddress[	31:12]						
	This field specifies bits 31:12 of the								

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# 4.1.6.5 CURAPAL ET—Cursor A Palette registers

	Cursor Palette Format									
Project:	All									
Bit De	scription									
31:24	Reserved Pro	ject: All			Format:	MBZ				
23:16	Red_or_Y_Value	Project:	All	Format:						
		and excess 128 i	notation	n for the UV values	nge unsigned numbers The data can be pre- gamma corrector.					
15:8	Green_or_U_Value	Project:	All	Format:	·					
7:0	Blue_or_V_Value	Project:	All	Format:						

CURAPALET—Cursor A Palette registers						
Register Type:	MMIO					
Address Offset:	70090h					
Project:	All					
Default Value:	0000000h					
Access:	R/W					
Size (in bits):	4x32					
Double Buffer Update Point:	Start of vertical blank or pipe disabled					

The cursor palette provides color information when using one of the indexed modes. The two-bit index selects one of the four colors or two of the colors when in the AND/XOR cursor mode. The cursor palette provides color information when using one of the indexed modes. The two-bit index selects one of the four colors or two of the colors when in the AND/XOR cursor mode.

The table below describes the palette usage for different cursor modes and indexes.

	lor 4co	lor
palette 0	palette 0	palette 0
palette 1	palette 1	palette 1
transparent	transparent	palette 2
invert destination	palette 3	palette 3
	(palette 3 all 1s)	
	palette 1 transparent	palette 1 palette 1 transparent transparent invert destination palette 3 (palette 3 all

Palette 3 must be programmed with all 1s for invert destination.

DWord B	rd Bit				Description	
0	31:0	CURAPALET0	Project:	All	Format:	Cursor Palette Format



CURAPALET—Cursor A Palette registers							
1	31:0	CURAPALET1	Project:	All	Format:	Cursor Palette Format	
2	31:0	CURAPALET2	Project:	All	Format:	Cursor Palette Format	
3	31:0	CURAPALET3	Project:	All	Format:	Cursor Palette Format	

## 4.1.6.6 CURASURFLIVE—Cursor A Live Surface Base Address

		CURASURFLIVE—Cursor A Live Su	rface Base Address
Register Ty	/pe:	MMIO	
Address Of	ffset:	700ACh	
Project:		All	
<b>Default Val</b>	ue:	0000000h	
Access:		Read Only	
Size (in bits	s):	32	
Bit De		scription	1
31:0	Curs	or_A_Live_Surface_Base_Address	Project: All Format:
	This	gives the live value of the surface base address as be	eing currently used for the plane.



# **4.1.7 Cursor B Plane Control Registers**

The CURBCNTR active register will be updated on the vertical blank or when pipe is disabled, after the CURBBASE trigger register is written, or when cursor B is not yet enabled – thus providing an atomic update of the cursor B control and base address registers.

## 4.1.7.1 CURBCNT R—Cursor B Control Register

		CU	RBCNTR—Cursor B Control Register					
Register Ty	me.		MMIO					
Address Of	•		700C0h					
Project:			All					
Default Value:			00000000h					
Access:			R/W					
Size (in bits):			32					
Double But	•	Point:	Start of vertical blank or pipe disabled or cursor disabled, after ar	med				
Double But	fer Armed		Write to CURBBASE					
Cursor B is	connected	to pipe B on	ly.					
Bit De			scription					
31:27	Reserved Project: All Format: MBZ							
26	Cursor_G	Samma_Ena	ble					
	Project: All							
	•	Default Value: 0b						
	Value N	a me	Description	Pr	oject			
	0b	Bypass	Cursor pixel data bypasses gamma correction	All				
	1b	Corrected	Cursor pixel data is gamma to be corrected	All				
25	Reserved	l Projec	ct: All Format:					
24	Pipe Col	or Space C	Conversion_Enable					
	Project:		All					
	Default Value: 0b							
	This bit enables pipe color space conversion for the cursor pixel data. CSC mode in the pipe CS registers must be set to match the format of the cursor pixel data							
	Value N	a me	Description		Project			
	0b	Bypass	Cursor pixel data bypasses the pipe color space conversion logi	С	All			
	1b	pass	Cursor pixel data passes through the pipe color space conversion	n logic.	All			
23:16	Reserved	l Projec	et: All Format:					



CURBCNTR—Cursor	<b>B</b> Control	Register

15 **180°\_Rotation** 

Project: All Default Value: 0b

This mode causes the cursor to be rotated 180°. Only 32 bits per pixel cursors can be rotated. This field must be zero when the cursor format is 2 bits per pixel.

Value Na	me	Description	Project
0b	None	No rotation	All
1b	180	180° Rotation of 32 bit per pixel cursors	All

14 Trickle\_Feed\_Enable

Project: DevSNB Default Value: 0b

Value Na	me	Description	Project
0b	Enable	Trickle Feed Enabled - Data requests are sent whenever there is space in the Display Data Buffer.	All
1b	Disable	Trickle Feed Disabled - Data requests are sent in bursts.	All

14	Reserved	Project:	DevILK		Format:	
13:6	Reserved	Project:	All		Format:	MBZ
5	Cursor_Mode	_Select	Project:	All	Format:	
	<b>Cursor Mode</b>	Select				
	Defined in CUI	RACNTR-	-Cursor A C	ontrol	Register Bit 5.	
4:3	Reserved	Project:	All		Format:	
2:0	Cursor_Mode	_Select	Project:	All	Format:	
	These three bir Control Registe		with bit 5 se	elect th	e mode for cursor as shown in CURACNTR	Cursor A



# 4.1.7.2 CURBBASE—Cursor B Base Address Register

	CUR	BBASE—Curs	sor B Base Address Register			
Register Ty	/pe:	MMIO				
Address O	ffset:	700C4h				
Project: All						
<b>Default Val</b>	ue:	00000000h				
Access:		R/W				
Size (in bits	s):	32				
<b>Double But</b>	ffer Update Point:	Start of vertical bl	lank or pipe disabled			
	his register arm C er specifies the gra	•	dress at which the cursor image data is locate	ed.		
Bit De			scription			
31:12	Cursor_Base_Add	Cursor_Base_Address[31:12]				
	Project:	All				
	Address:	GraphicsAdo	lress[31:12]			
		ies the graphics add gisters on the next d	dress of the cursor. It also acts as a trigger event t lisplay event.	to force the		
		orming 180° rotation	C byte aligned. The cursor must be in linear memory, this address does not change, hardware will intered to the cursor.			
11:0	Reserved Pro	ject: All	Format: M	/IBZ		



# 4.1.7.3 CURBPOS—Cursor B Position Register

		CURBP	OS—Curso	or B Posit	ion Regist	er		
Register Ty	/pe:	MMIO						
Address O	ffset:	700C8h	1					
Project:		All						
<b>Default Val</b>	ue:	000000	00h					
Access:		R/W						
Size (in bits	s):	32						
	fer Update Point:		vertical blank of					
	er specifies the scr					or position	is always the	e upper
left corner of	of the active image	for the di	isplay pipe tha	at the curso	r is assigned.			
Bit De				scriptio	n			
31	Cursor_Y-Position	n_Sign_Bi	it				Project:	All
	This bit provides the For normal high resthe active screen.							
30:28	Reserved Pro	oject: A	ΔII			Format:	MBZ	
27:16	Cursor_Y-Position	n_Magnitu	ıde_Bits				Project:	All
	This register provide cursor. The sign b					ecifies the v	ertical position	n of
	When performing 1 to the end of the ac					the lower rig	ght corner rela	ative
15	Cursor_X-Position	n_Sign_Bi	it				Project:	All
	This bit provides the For normal high resthe active screen.							
14:12	Reserved Pro	oject: A	ΔII			Format:	MBZ	
11:0	Cursor_X-Position	n_Magnitu	ıde_Bits				Project:	All
	These 12 bits provided by b			e that specifie	es the horizonta	al position of	cursor. The	sign
	When performing 1 to the end of the ac					the lower rio	ght corner rela	ative

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#### 4.1.7.4 CURBPAL ET—Cursor B Palette registers

Register Type: MMIO
Address Offset: 700D0h
Project: All
Default Value: 00000000h
Access: R/W
Size (in bits): 4x32

Double Buffer Update Point: Start of vertical blank or pipe disabled

The cursor palette provides color information when using one of the indexed modes. The two-bit index selects one of the four colors or two of the colors when in the AND/XOR cursor mode. The cursor palette provides color information when using one of the indexed modes. The two-bit index selects one of the four colors or two of the colors when in the AND/XOR cursor mode. See Cursor A palette usage table.

DWord B	it				Description	
0	31:0	CURBPALET0	Project:	All	Format:	Cursor Palette Format
1	31:0	CURBPALET1	Project:	All	Format:	Cursor Palette Format
2	31:0	CURBPALET2	Project:	All	Format:	Cursor Palette Format
3	31:0	CURBPALET3	Project:	All	Format:	Cursor Palette Format

#### 4.1.7.5 CURBSURFLIVE—Curs or B Live Surface Base Address Register

CURBSURFLIVE—Cursor B Live Surface Base	e Address Register
---	--------------------

Register Type: MMIO
Address Offset: 700ECh
Project: All
Default Value: 00000000h
Access: Read Only
Size (in bits): 32

Bit De scription

31:0 Cursor\_Live\_Surface\_Base\_Address Project: All Format:
This gives the live value of the surface base address as being currently used for the plane.



# 4.1.8 Primary A Plane Control

The DSPACNTR and DSPASTRIDE active registers will be updated on the vertical blank or when pipe is disabled, after the DSPASURF trigger register is written, or when the primary A is not yet enabled – thus providing an atomic update of the primary A control, stride, and base address registers.

## 4.1.8.1 DSPACNT R—Primary A Control Register

		DS	PACNTR—Primary A Control Register							
Register Ty	pe:		MMIO							
Address Of	fset:		70180h							
Project:			All							
Default Valu	ıe:		0000000h							
Access:			R/W							
Size (in bits	s):		32							
Double Buf			Start of vertical blank or pipe disabled or primary disabled, after armed							
Double Buf			Write to DSPASURF							
Primary A P	ane is con	nected to pi	pe A only.							
Bit De			scription							
31	Primary_	_Plane_Ena	able Project: All Format:	Enable						
	memory	fetches cea	t, the primary plane will generate pixels for display. When set to zero, primary plane ease and plane output is transparent. The display pipe must be enabled to enable an override for the enable of the plane in the Pipe Configuration register. When in							
			FO mode, write to this register to enable the plane will be internally buffered and FIFO mode is exiting.							
30	Gamma_Enable									
	Project:		All							
	Default Value: 0b									
	This bit should only be changed after the plane has been disabled. It controls the bypassing display pipe gamma unit for the plane pixel data. For 8-bit indexed display data, this bit should be a one.									
	Value N	la me	Description	Project						
	0b	Bypass	Plane pixel data bypasses the display pipe gamma correction logic	All						
	1b	Correct	Plane pixel data is gamma corrected in the display pipe gamma correction logic.	All						

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#### **DSPACNTR—Primary A Control Register**

29:26 **Source\_Pixel\_Format** 

Project: All Default Value: 0b

These bits should only be changed after the plane has been disabled. Pixel format of 8-bit indexed uses the pipe palette. Before entering the blender, each source format is converted to 12 bits per pixel.

Value Na me		Description	Project
0010b	8bpp	8-bpp Indexed	All
0101b	16-bit BGRX (5:6:5 MSB-R:G:B) pixel format (compatible).		All
0110b	32-bit BGRX (8:8:8:8 MSB-X:R:G:B)	pixel format. Ignore alpha	All
1000b	32-bit RGBX (2:10:10:10 MSB-X:B:G:R)	pixel format. Ignore alpha	All
1010b	32-bit BGRX (2:10:10:10 MSB-X:R:G:B)	pixel format. Ignore alpha	All
1100b	64-bit RGBX Floating Point(16:16:16:16 MSB-X:B:G:R)	pixel format. Ignore alpha	All
1110b	32-bit RGBX (8:8:8:8 MSB-X:B:G:R)	pixel format. Ignore alpha	All
	Use of 64bpp format will limit the maximum dot clock to 80% of cdclk		
others	Reserved	Reserved	All

Plane\_Extended\_Range\_Source\_Select

Project: DevSNB Default Value: 0b

This bit is used to indicate when the plane source pixel format should be processed as having extended range. This is only valid with certain source pixel formats. If the pipe is extended range and plane extended range source is not selected, the plane will fit the source pixel data into the 0 to 1 region of the extended range.

Value Na me		Description	
0b	Normal	Normal range source selected	All
1b	Extended	Extended range source selected.	All

25 Reserved Project: DevILK Format:



#### **DSPACNTR—Primary A Control Register**

24 Pipe\_Color\_Space\_Conversion\_Enable

Project: All Default Value: 0b

This bit enables pipe color space conversion for the plane pixel data. CSC mode in the pipe CSC registers must be set to match the format of the plane pixel data.

Value N	a me	Description	Project
0b	Bypass	Plane pixel data bypasses the pipe color space conversion logic	All
1b	Pass	Plane pixel data passes through the pipe color space conversion logic.	All

23:16 Reserved Project: All Format:

15 **180°\_Display\_Rotation** 

Project: All Default Value: 0b

This mode causes the plane to be rotated 180°. In addition to setting this bit, software must also set the surface address offset to the lower right corner of the unrotated image.

Value Na me		Description	Project
0b	None	No rotation	All
1b	180	180° rotation	All

14 Trickle\_Feed\_Enable

Project: All Default Value: 0b

[ILK]: This bit must always be programmed to '1'.

Value Na me		a me Description	
0b	Enable	Trickle Feed Enabled - Plane data requests are sent whenever there is space in the Display Data Buffer.	All
1b	Disable	Trickle Feed Disabled - Plane data requests are sent in bursts	All

13 Data\_Buffer\_Partitioning\_Control

Project: All Security: Test Default Value: 0b

Note: When in CxSR Max FIFO mode, this bit will be ignored.

Value N	a me	Description	Project
0b	Use Sprite	Primary A Data Buffer will use Sprite A buffer space when Sprite A is disabled	All
1b	Not use Sprite	Primary A Data Buffer will not use Sprite A buffer space when Sprite A is disabled	All

12:11 Reserved Project: All Format:



#### **DSPACNTR—Primary A Control Register**

10 Tiled\_Surface

Project: All Default Value: 0b

This bit indicates that the plane surface data is in tiled memory. Only X tiling is supported for display surfaces.

When this bit is set, it affects the hardware interpretation of the DSPATILEOFF, DSPALINOFF, and DSPASURF registers.

Value Na me		Description	Project
0b	Linear	Plane uses linear memory	All
1b	X-tiled	Plane uses X-tiled memory	All

#### 9 Asynchronous\_Surface\_Address\_Update\_Enable

Project: All Default Value: 0b

This bit will enable asynchronous updates of the surface address when written by MMIO. The surface address will change with the next TLB request or when start of vertical blank is reached. Updates during vertical blank may not complete until after the first few active lines are displayed.

#### Restrictions:

- No command streamer initiated surface address updates to this plane are allowed when this bit is enabled.
- Wait for flip done indication in pipe status register before writing the surface address register again with this bit set.

Value N	a me	Description	Project
0b	Sync	Surface Address MMIO writes will update synchronous to start of vertical blank	All
1b	Async	Surface Address MMIO writes will update asynchronously	All

8:0 Reserved Project: All Format: MBZ



#### **Primary Plane Source Pixel Format Mapping of Bits to Colors:**

Note: For 64-bit Floating Point format, each of the 16 bit color components is 1:5:10 MSB-

sign:exponent:fraction

PRIMARY RGB	Ignored	Red	Green	Blue
16-bit BGRX 5:6:5	N/A	15:11	10:5	4:0
32-bit BGRX 8:8:8	31:24	23:16	15:8	7:0
32-bit RGBX 10:10:10	31:30	9:0	19:10	29:20
32-bit BGRX 10:10:10	31:30	29:20	19:10	9:0
64-bit RGBX Float 16:16:16	63:48	15:0	31:16	47:32
32-bit RGBX 8:8:8	31:24	7:0	15:8	23:16

# 4.1.8.2 DSPALINOFF—Primar y A Linear Offset Register

DSPALINOFF—Primary A Linear Offset Register				
Register Ty	ype:	MMIO		
Address O	ffset:	70184h		
Project:		All		
<b>Default Val</b>	ue:	0000000h		
Access:		R/W		
Size (in bit	s):	32		
Double Bu	ffer Update Point:	Start of vertical blank or pipe disabled		
Bit De	scription			
31:0	Primary_Linear_Of	ffset Project: All Format:		
	This register provides the linear panning byte offset into the primary plane. This value is added to the surface address to get the address of the first pixel to be displayed. This offset must be at least pixel aligned. When performing 180° rotation, the unpanned offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address. When the surface is tiled, the contents of this register are ignored.			

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## 4.1.8.3 DSPAST RIDE—Primary A Stride Register

	DS	SPASTRIDE	—Prin	nary A Stride Register
Register Ty	/pe:	MMIO		
Address O	ffset:	70188h		
Project:		All		
<b>Default Val</b>	ue:	00000000h		
Access:		R/W		
Size (in bits	s):	32		
Double But	ffer Update Point:	Start of vertica	al blank o	r pipe disabled or primary disabled, after armed
Double But	ffer Armed By:	Write to DSPA	ASURF	
Bit De				scription
31:16	Reserved Proj	ect: All		Format:
15:6	Primary_Stride	Project:	All	Format:
	aligned. When using line to line incremen	g tiled memory, t for the display ad stream or wri	this must . This reg	s. When using linear memory, this must be 64 byte be 512 byte aligned. This value is used to determine the gister is updated through either a command packet passed a register. The stride is limited to a maximum of 32K bytes
5:0	Reserved Proj	ect: All		Format:

## 4.1.8.4 DSPASURF—Primary A Surface Base Address Register

DSPASU	RF—Primary A Surface Base Address Registe	r
Register Type:	MMIO	
Address Offset:	7019Ch	
Project:	All	
Default Value:	0000000h	
Access:	R/W	
Size (in bits):	32	
<b>Double Buffer Update Point:</b>	Start of vertical blank or pipe disabled	



	DSP	ASURF—	Primary A	Surface Base	e Address Re	egiste	er
Bit De				scription			
31:12	Primary_Su	rface_Base_	Address				
	Project:	All					
	Address:	Gr	aphicsAddress	[31:12]			
	(x, y) offsets	in the DSPA	TILEOFF regist	address. When the surface. When the surface. ALINOFF register.	ace is in linear me		
	tiled memory software or b	, this address y command p	must be 256K packets in the c	performing asynch aligned. This regi command stream. physical pages thr	ster can be writter It represents an of	n directly	y through
11:3	Reserved	Project:	All		Fo	rmat:	
2	Reserved	Project:	ILK		Fo	rmat:	MBZ
0	Reserved	Project:	All		Eo	rmat:	MBZ

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#### 4.1.8.5 DSPATILEOFF—Primar y A Tiled Offset Register

## **DSPATILEOFF—Primary A Tiled Offset Register**

Register Type: MMIO
Address Offset: 701A4h
Project: All
Default Value: 00000000h

Default Value: 00000 Access: R/W Size (in bits): 32

**Double Buffer Update Point:** Start of vertical blank or pipe disabled

This register specifies the panning for the display surface. The surface base address is specified in the DSPASURF register, and this register is used to describe an offset from that base address. When the surface is in linear memory, the offset is specified in the DSPALINOFF register and the contents of this register are ignored. When the surface is tiled, the start position is specified in this register as an (x, y) offset from the beginning of the surface.

Bit De	scriptio	on
31:28	Reserved Project: All	Format: MBZ
27:16	Primary_Start_Y-Position	Project: All Format:
	These 12 bits specify the vertical position in lines of the beathe display surface. When performing 180° rotation, this fright corner relative to the start of the active display plane	field specifies the vertical position of the lower
15:12	Reserved Project: All	Format: MBZ
11:0	Primary_Start_X-Position	Project: All Format:
	These 12 bits specify the horizontal offset in pixels of the to the display surface. When performing 180° rotation, th lower right corner relative to the start of the active display	is field specifies the horizontal position of the



## 4.1.8.6 DSPASURFLIVE—Pr imary A Live Surface Base Address

	1	DSPASURFLIVE—Primary A Live Surface Base Address
Register Ty	ype: N	MMIO
Address O	ffset: 7	'01ACh
Project:	A	All
<b>Default Val</b>	lue: 0	0000000h
Access:	F	Read Only
Size (in bit	<b>s</b> ): 3	32
<b>Trusted Ty</b>	pe: 1	
Bit De		scription
31:0	Primar	ry_Live_Surface_Base_Address
	Project	:: All
	Addres	ss: GraphicsAddress[31:0]
	This giv	ves the live value of the surface base address as being currently used for the plane.

## 4.1.9 Primary B Plane Control

The DSPBCNTR and DSPBSTRIDE active registers will be updated on the vertical blank or when pipe is disabled, after the DSPBSURF trigger register is written, or when the primary B is not yet enabled – thus providing an atomic update of the primary B control, stride, and base address registers.

## 4.1.9.1 DSPBCNT R—Primary B Control Register

D	SPBCNTR—Primary B Control Register
Register Type:	MMIO
Address Offset:	71180h
Project:	All
Default Value:	0000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe disabled or primary disabled, after armed
Double Buffer Armed By:	Write to DSPBSURF
Primary B Plane is connected	to pipe B only



		DS	SPBCNTR—Primary B Control Register	
Bit De			scription	
31	Primary_	Plane_Ena	able Project: All Format:	Enable
	memory for the plane. Self Refre	etches ceas . There is a esh Big FIF	the primary plane will generate pixels for display. When set to zero, prim se and plane output is transparent. The display pipe must be enabled to in override for the enable of the plane in the Pipe Configuration register. O mode, write to this register to enable the plane will be internally buffere FO mode is exiting.	enable Vhen in
30	Gamma_	Enable		
	Project:		All	
	Default V	'alue:	0b	
			be changed after the plane has been disabled. It controls the bypassing unit for the plane pixel data. For 8-bit indexed display data, this bit should	
	Value N	a me	Description	Project
	0b	Bypass	Plane pixel data bypasses the display pipe gamma correction logic	All
	1b	Correct	Plane pixel data is gamma corrected in the display pipe gamma correction logic.	All
29:26	Source_F	Pixel_Form	nat	
23.20	Project: Default Va	alue: s should or	All  Ob  nly be changed after the plane has been disabled. Pixel format of 8-bit in e. Before entering the blender, each source format is converted to 12 bits.	
∠J.∠U	Project: Default Va These bit uses the	alue: s should or pipe palette	All  0b  nly be changed after the plane has been disabled. Pixel format of 8-bit in	
∠J.∠U	Project: Default Va These bit uses the pixel.	alue: s should or pipe palette	All 0b nly be changed after the plane has been disabled. Pixel format of 8-bit in e. Before entering the blender, each source format is converted to 12 bits	s per
∠J.∠U	Project: Default Value N	alue: s should or pipe palette a me 8bpp	All 0b nly be changed after the plane has been disabled. Pixel format of 8-bit in e. Before entering the blender, each source format is converted to 12 bits  Description	Projec
<u>-</u> 3.20	Project: Default Value Note:  Output  Default	alue: s should or pipe palette  a me  8bpp  16-bit BG	All 0b nly be changed after the plane has been disabled. Pixel format of 8-bit in e. Before entering the blender, each source format is converted to 12 bits    Description	Project All
∠J.∠U	Project: Default Values the pixel.  Value Note: 0010b 0101b	alue: s should or pipe palette  me  8bpp  16-bit BG	All Ob nly be changed after the plane has been disabled. Pixel format of 8-bit in e. Before entering the blender, each source format is converted to 12 bits  Description 8-bpp Indexed  BRX (5:6:5 MSB-R:G:B) pixel format (XGA compatible).	Project All All All
∠J.∠U	Project: Default Values the pixel.  Value Non10b 0110b	alue: s should or pipe palette  a me 8bpp 16-bit BG 32-bit BG	All Ob only be changed after the plane has been disabled. Pixel format of 8-bit in the Before entering the blender, each source format is converted to 12 bits  Description 8-bpp Indexed FRX (5:6:5 MSB-R:G:B) pixel format (XGA compatible). FRX (8:8:8:8 MSB-X:R:G:B) pixel format. Ignore alpha	Project All All a All a All
ZJ.ZU	Project: Default Values the pixel.  Value Non10b 0101b 0110b 1000b	alue: s should or pipe palette  a me 8bpp 16-bit BG 32-bit BG 32-bit BG	All Ob nly be changed after the plane has been disabled. Pixel format of 8-bit in e. Before entering the blender, each source format is converted to 12 bits    Description	Project All All a All a All a All
ZJ.ZU	Project: Default Value Note of the pixel.  Value Note of the pixel of	alue: s should or pipe palette  a me 8bpp 16-bit BG 32-bit BG 32-bit BG 32-bit RG	All Ob only be changed after the plane has been disabled. Pixel format of 8-bit in the Before entering the blender, each source format is converted to 12 bits  Description 8-bpp Indexed pixel format (XGA compatible).  GRX (8:8:8:8 MSB-X:R:G:B)  GRX (2:10:10:10 MSB-X:B:G:R)  GRX (2:10:10:10 MSB-X:R:G:B)  GRX (2:10:10:10 MSB-X:R:G:B)  GRX (2:10:10:10 MSB-X:R:G:B)  GRX (2:10:10:10 MSB-X:R:G:B)  Description 8-bpp Indexed pixel format (XGA compatible).  Fixel format Ignore alph pixel format. Ignore alph	Project All All a All a All a All
۷.۷۰	Project: Default Value Note of the pixel.  Value Note of the pixel of	alue: s should or pipe palette  a me  8bpp  16-bit BG  32-bit BG  32-bit RG  32-bit RG  44-bit RG  Use of 64  80% of co	All Ob only be changed after the plane has been disabled. Pixel format of 8-bit in the Before entering the blender, each source format is converted to 12 bits  Description 8-bpp Indexed pixel format (XGA compatible).  GRX (8:8:8:8 MSB-X:R:G:B)  GRX (2:10:10:10 MSB-X:B:G:R)  GRX (2:10:10:10 MSB-X:R:G:B)  GRX (2:10:10:10 MSB-X:R:G:B)  GRX (2:10:10:10 MSB-X:R:G:B)  GRX (2:10:10:10 MSB-X:R:G:B)  Description 8-bpp Indexed pixel format (XGA compatible).  Fixel format Ignore alph pixel format. Ignore alph	Project All All a All a All a All a All



## **DSPBCNTR—Primary B Control Register**

Plane\_Extended\_Range\_Source\_Select

Project: DevSNB Default Value: 0b

This bit is used to indicate when the plane source pixel format should be processed as having extended range. This is only valid with certain source pixel formats. If the pipe is extended range and plane extended range source is not selected, the plane will fit the source pixel data into the 0 to 1 region of the extended range.

Value N	a me	Description	Project
0b	Normal	Normal range source selected	All
1b	Extended	Extended range source selected.	All

25 **Reserved** Project: DevILK Format:

#### 24 Pipe\_Color\_Space\_Conversion\_Enable

Project: All Default Value: 0b

This bit enables pipe color space conversion for the plane pixel data. CSC mode in the pipe CSC registers must be set to match the format of the plane pixel data.

Value N	a me	Description	Project
0b	Bypass	Plane pixel data bypasses the pipe color space conversion logic	All
1b	Pass	Plane pixel data passes through the pipe color space conversion logic.	All

23:16 Reserved Project: All Format:

#### 15 **180°\_Display\_Rotation**

Project: All Default Value: 0b

This mode causes the plane to be rotated 180°. In addition to setting this bit, software must also set the surface address offset to the lower right corner of the unrotated image.

Value N	a me	Description	Project
0b	None	No rotation	All
1b	180	180° rotation	All

#### 14 Trickle\_Feed\_Enable

Project: All Default Value: 0b

[DevILK] This bit must always be programmed to '1'.

Value N	a me	Description	Project
0b	Enable	Trickle Feed Enabled - Plane data requests are sent whenever there is space in the Display Data Buffer.	All
1b	Disable	Trickle Feed Disabled - Plane data requests are sent in bursts	All



		DS	SPBCNTR—Primary B Control Register		
13	Data_But	ffer_Partiti	ioning_Control		
	Project:		All		
	Security:		Test		
	Default Va	alue:	0b		
	Note: Whe	en in CxSR	Max FIFO mode, this bit will be ignored.		
	Value N	a me	Description	Project	
	0b	Use Sprite	Primary B Data Buffer will use Sprite B buffer space when Sprite B is disabled.	All	
	1b	Not Use Sprite	Primary B Data Buffer will not use Sprite B buffer space when Sprite B is disabled	All	
12:11	Reserved	l Proje	ect: All Format:		
10	Tiled_Sui	rface			
	Project:		All		
	Default Va	alue:	0b		
	This bit indicates that the plane surface data is in tiled memory. Only X tiling is supported for display surfaces.				
	surfaces.				
	When this	s bit is set, RF register	it affects the hardware interpretation of the DSPBTILEOFF, DSPBLINOF's.	F, and	
	When this	RF register		F, and	
	When this DSPBSU	RF register	S.	1	
	When this DSPBSU	RF register	Description	Project	
9	When this DSPBSU  Value N  0b  1b	RF register  a me  Linear  X-tiled	Plane uses X-tiled memory  Plane uses X-tiled memory	Project All	
9	When this DSPBSU  Value N  0b  1b	RF register  a me  Linear  X-tiled	Description Plane uses linear memory	Project All	
9	When this DSPBSU  Value N  0b  1b  Asynchro	RF register  a me  Linear  X-tiled  onous_Sur	Description Plane uses linear memory Plane uses X-tiled memory  face_Address_Update_Enable	Project All	
9	When this DSPBSU  Value N  0b  1b  Asynchro  Project: Default Va  This bit w address v	a me Linear X-tiled  onous_Sur  alue: ill enable a vill change	Description Plane uses linear memory Plane uses X-tiled memory  face_Address_Update_Enable All	Project All All	
9	When this DSPBSU  Value N  0b  1b  Asynchro  Project: Default Va  This bit w address v	RF register  a me Linear X-tiled  conous_Sur  alue: ill enable a vill change rtical blank	Description Plane uses linear memory Plane uses X-tiled memory  face_Address_Update_Enable All 0b  synchronous updates of the surface address when written by MMIO. The with the next TLB request or when start of vertical blank is reached. Updates.	Project All All	
9	When this DSPBSUI  Value N  0b  1b  Asynchro  Project: Default Va  This bit w address v during ver  Restriction	RF register  a me Linear X-tiled  onous_Sur  alue: ill enable a vill change rtical blank ons:	Description Plane uses linear memory Plane uses X-tiled memory  face_Address_Update_Enable All 0b  synchronous updates of the surface address when written by MMIO. The with the next TLB request or when start of vertical blank is reached. Updates.	Project All All e surface dates	
9	When this DSPBSU  Value N  0b  1b  Asynchro  Project: Default Va  This bit w address v during ver leader of the control of the	RF register  a me Linear X-tiled  conous_Sur  alue: iill enable a will change riical blank cons: command enabled.	Plane uses linear memory  Plane uses X-tiled memory  face_Address_Update_Enable  All  0b  synchronous updates of the surface address when written by MMIO. Th with the next TLB request or when start of vertical blank is reached. Upo may not complete until after the first few active lines are displayed.  If streamer initiated surface address updates to this plane are allowed when the indication in pipe status register before writing the surface address in	Project All All e surface dates	
9	When this DSPBSU  Value N  0b  1b  Asynchro  Project: Default Va  This bit w address v during ver leader of the control of the	RF register  a me Linear X-tiled  chous_Sur  alue: iill enable a vill change rtical blank chos: command enabled. ait for flip d pain with thi	Plane uses linear memory  Plane uses X-tiled memory  face_Address_Update_Enable  All  0b  synchronous updates of the surface address when written by MMIO. Th with the next TLB request or when start of vertical blank is reached. Upo may not complete until after the first few active lines are displayed.  If streamer initiated surface address updates to this plane are allowed when the indication in pipe status register before writing the surface address in	Project All All e surface dates	
9	When this DSPBSUI  Value N  0b  1b  Asynchro  Project: Default Va  This bit w address v during ver restriction is  - No ag	RF register  a me Linear X-tiled  chous_Sur  alue: iill enable a vill change rtical blank chos: command enabled. ait for flip d pain with thi	Plane uses linear memory  Plane uses X-tiled memory  face_Address_Update_Enable  All  0b  synchronous updates of the surface address when written by MMIO. The with the next TLB request or when start of vertical blank is reached. Upon may not complete until after the first few active lines are displayed.  If streamer initiated surface address updates to this plane are allowed when the indication in pipe status register before writing the surface address resis bit set.	Project All All e surface dates en this bit	

See DSPACNTR - Primary Plane Source Pixel Format Mapping of Bits to Colors



## 4.1.9.2 DSPBLINOFF—Primar y B Linear Offset Register

	DSPE	BLINOFF—Primary B Linear Offset Register		
Register Ty	ype:	MMIO		
Address Offset:		71184h		
Project:		All		
Default Val	ue:	0000000h		
Access:		R/W		
Size (in bit	s):	32		
Double Bu	ffer Update Point:	Start of vertical blank or pipe disabled		
Bit De		scription		
31:0	Primary_Linear_O	ffset	Project:	All
	surface address to galigned. When perfipixel of the last line	es the linear panning byte offset into the primary plane. This value get the address of the first pixel to be displayed. This offset must be orming 180° rotation, the unpanned offset must be the difference be of the display data in its unrotated orientation and the display surfact tiled, the contents of this register are ignored.	oe at least poetween the	pixel e last

## 4.1.9.3 DSPBST RIDE—Primary B Stride Register

	D	SPBSTRIDE—	-Primary B Stride Register		
Register Ty	ype:	MMIO			
Address O	ffset:	71188h			
Project:		All			
<b>Default Val</b>	lue:	00000000h			
Access:		R/W			
Size (in bits	s):	32			
Double But	ffer Update Point:	Start of vertical blank or pipe disabled or primary disabled, after armed			
Double But	ffer Armed By:	Write to DSPBS	SURF		
Bit De			scription		
31:16	Reserved Pro	ect: All	Format:	MBZ	
15:6	Primary_Stride		Project	: All	
	aligned. When usin line to line incremer	g tiled memory, this t for the display. The nd stream or writes	n bytes. When using linear memory, this means to be 512 byte aligned. This value is us his register is updated through either a come to this register. The stride is limited to a material stricts.	sed to determine the mand packet passed	
5:0	Reserved Pro	ect: All	Format:	MBZ	



## 4.1.9.4 DSPBSURF—Primary B Surface Base Address Register

	DSPBS	SURF—	Primar	y B Surface	Base Add	ress Registe	r
Register T	vpe:	MM	0				
Address O	711	9Ch					
Project:	All						
Default Va	000	00000h					
Access:		R/W	,				
Size (in bit	s):	32					
Double Bu	ffer Update Poin	t: Star	t of vertica	al blank or pipe dis	sabled		
Writes to t	his register arr	n DSPB	registers	}			
Bit De				scri	ption		
31:12	Primary_Surface	e_Base_	Address				
	Project:	All					
	Address:	Gr	aphicsAdd	dress[31:12]			
	(x, y) offsets in	the DSPB	TILEOFF r	pase address. Whe register. When the DSPBLINOFF reg	e surface is in		is specified using anning is
	tiled memory, th software or by c	is address ommand p	must be 2 backets in	Vhen performing a 256K aligned. Th the command streed to physical pag	is register can eam. It repres	be written directly ents an offset from	y through
11:3	Reserved	Project:	All			Format:	
2	Reserved	Project:	ILK			Format:	MBZ
0	Reserved	Project:	All			Format:	MBZ



## 4.1.9.5 DSPBTILEOFF—Primar y B Tiled Offset Register

Address Offset: 711A4h
Default: 00000000h
Normal Access: Read/Write

Double Buffer Update Point: Start of vertical blank or pipe disabled

Size: 32 bits

This register specifies the panning for the display surface. The surface base address is specified in the DSPBSURF register, and this register is used to describe an offset from that base address. When the surface is in linear memory, the offset is specified in the DSPBLINOFF register and the contents of this register are ignored. When the surface is tiled, the start position is specified in this register as an (x, y) offset from the beginning of the surface.

Bit De	scriptions
31:28	Reserved: Write as zero
27:16	<b>Primary Start Y-Position:</b> These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180° rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.
15:12	Reserved: Write as zero
11:0	<b>Primary Start X-Position:</b> These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180° rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the unrotated orientation.

## 4.1.9.6 DSPBSURFLIVE—Pr imary B Live Surface Base Address

	DSPBSU	RFLIVE—Primary B Live Surface Base Address
Register Ty	oe: MMIO	
<b>Address Off</b>	set: 711ACh	
Project:	All	
Default Valu	e: 00000000h	
Access:	Read Only	
Size (in bits	): 32	
Bit De		scription
31:0	Primary_Live_Sur	face_Base_Address
	Project:	All
	Address:	GraphicsAddress[31:0]
	This gives the live	value of the surface base address as being currently used for the plane.

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## 4.1.10 Video Sprite A Control

Two video sprites are provided for the display of video content. These sprite planes provide windowing and keying functions as well as gamma and color space conversion from YUV to RGB. Each sprite plane is attached to only one of the pipes, Video Sprite A to pipe A and Video Sprite B to pipe B. Apart from the pipe assignments, the functionality is identical.

The DVSACNTR, DVSASTRIDE, DVSAPOS, DVSASIZE, and DVSASCALE active registers will be updated on the vertical blank or when pipe is disabled, after the DVSASURF trigger register is written, or when the sprite A is not yet enabled – thus providing an atomic update of the video sprite A control, stride, position, size, scale, and base address registers.

## 4.1.10.1 DVSACNT R—Video Sprite A Control Register

		DVS	ACNTR—Video Sprite A Control Register		
Register T	уре:		MMIO		
Address Offset:			72180h		
Project:			All		
Default Val	lue:		0000000h		
Access:			R/W		
Size (in bit	,		32		
	ffer Update		Start of vertical blank or pipe disabled or sprite disabled, after armed		
	ffer Armed		Write to DVSASURF		
√ideo Sprit	te A Plane	is connec	ted to pipe A only.		
Bit De			scription		
31	Sprite_Er	nable	Project: All Format: Enable		
	When this bit is set, the sprite plane will generate pixels for display. When set to zero, sprite plane memory fetches cease and plane output is transparent. The display pipe must be enabled to enable the plane. When in Self Refresh Big FIFO mode, write to this register to enable the plane will be internally buffered and delayed while Big FIFO mode is exiting.				
	internally i	buffered ar	nd delayed while Big FIFO mode is exiting.	be	
30	Gamma_l		nd delayed while Big FIFO mode is exiting.	be	
30	_		nd delayed while Big FIFO mode is exiting.  All	De	
30	Gamma_l	Enable		De	
30	Gamma_I Project: Default Va There are correction display pla	Enable  alue:  two gamm in the dispane. Gamr	All	ne gamma ta from this	
30	Gamma_I Project: Default Va There are correction display pla	Enable  alue: two gamm in the disp ane. Gamr lues into th	All  Ob  a adjustments possible in the video sprite data path. This bit controls the lay pipe not the gamma control in this plane. It affects only the pixel data according the control of the control of the control of the video sprite is disabled by loa	ne gamma ta from this	
30	Gamma_I Project: Default Va There are correction display pla default va	Enable  alue: two gamm in the disp ane. Gamr lues into th	All  Ob  a adjustments possible in the video sprite data path. This bit controls the lay pipe not the gamma control in this plane. It affects only the pixel date and correction logic that is contained in the video sprite is disabled by loatose registers.	ne gamma ta from this ding the	



29	Reserve	ed Proje	ect: All	Format	: MBZ			
28	YUV_B	/pass_Exce	ss-512_Format_	Conversion				
	Project:		All					
	Default Value: 0b							
	Value	Na me	Description		Project			
	0b	Disable	Disable excess	s-512 conversion	All			
	1b	Enable	Enable excess	s-512 conversion	All			
27	Range_	Correction_	Disable					
	Project:		All					
	Default '	Value:	0b					
	be used	if full range	YUV source mate	this bit will generate range compressed RGB erial is used. This bit has no effect on RGB s	ource format			
	Value		Description		Project All			
	0b	Enable	Range correcti	Range correction enabled				
	1b	1b Disable No range correction						
26:25	Source	Source_Pixel_Format						
	Project:		DevSNB					
	Default '	Value:	0b					
	This field selects the pixel format for the sprite. Before entering the blender, each source format is converted to 12 bits per pixel.							
						At 10		
		ed to 12 bits		Description				
	converte	ed to 12 bits	per pixel.	Description  YUV 4:2:2 packed pixel format (byte order programmed separately)				
	Value	Na me YUV 4:2:2	per pixel.	YUV 4:2:2 packed pixel format (byte order		Projec		
	Value 00b	Na me YUV 4:2:2	pit 2:10:10:10	YUV 4:2:2 packed pixel format (byte order programmed separately)  RGB 32-bit 2:10:10:10 pixel format (color of	order	Projec		
	Value 00b 01b	Na me YUV 4:2::  RGB 32-t	pit 2:10:10:10	YUV 4:2:2 packed pixel format (byte order programmed separately)  RGB 32-bit 2:10:10:10 pixel format (color or programmed separately). Ignore alpha.  RGB 32-bit 8:8:8:8 pixel format (color order	order er I format	Project All		



## **DVSACNTR—Video Sprite A Control Register**

26:25 **Source\_Pixel\_Format** 

Project: ILK Default Value: 0b

This field selects the pixel format for the sprite. Before entering the blender, each source format is converted to 12 bits per pixel.

Value N	a me	Description	Project
00b	YUV 4:2:2	YUV 4:2:2 packed pixel format (byte order programmed separately)	All
01b	Reserved	Reserved	All
10b	32-bit BGRX	32-bit BGRX (8:8:8:8 MSB-X:R:G:B) pixel format. Ignore alpha.	All
11b	Reserved	Reserved	All

24 Pipe\_Color\_Space\_Conversion\_Enable

Project: All Default Value: 0b

This bit enables pipe color space conversion for the plane pixel data. This is separate from the color conversion logic within the sprite plane. CSC mode in the pipe CSC registers must be set to match the format of the plane pixel data after the color conversion logic within the sprite plane.

Value N	a me	Description	Project
0b	Disable	Plane pixel data bypasses the pipe color space conversion logic	All
1b	Enable	Plane pixel data passes through the pipe color space conversion logic	All

23 Reserved Project: All Format: MBZ

22 Sprite\_Source\_Key\_Enable

Project: All Default Value: 0b

This bit enables source color keying. Sprite pixel values that match (within range) the key will become transparent. Source key can not be enabled if destination key is enabled.

Value Na me		Description	Project
0b	Disable	Sprite source key is disabled	All
1b	Enable	Sprite source key is enabled	All



## **DVSACNTR—Video Sprite A Control Register**

21 Plane\_Extended\_Range\_Source\_Select

Project: DevSNB Default Value: 0b

This bit is used to indicate when the plane source pixel format should be processed as having extended range. This is only valid with certain source pixel formats. If the pipe is extended range and plane extended range source is not selected, the plane will fit the source pixel data into the 0 to 1 region of the extended range.

Value Na me		Description	Project
0b	Normal	Normal range source selected	All
1b	Extended	Extended range source selected	All

21 Reserved Project: ILK Format:

20 RGB\_Color\_Order

Project: DevSNB Default Value: 0b

This field is used to select the color order when using RGB data formats. For other formats, this field is ignored.

Value Na me		Description	Project
0b	BGRX	BGRX (MSB-X:R:G:B)	All
1b	RGBX	RGBX (MSB-X:B:G:R)	All

20 Reserved Project: ILK Format:

19 Color\_Conversion\_Disabled

Project: All Default Value: 0b

This bit enables or disables the color conversion logic internal to the sprite. Color conversion is intended to be used with the formats that support YUV format. This bit is ignored when using RGB source formats.

Value N	a me	Description	Project
0b	Enable	Pixel data is sent through the sprite color conversion logic (only applies to YUV formats)	All
1b	Disable	Pixel data is not sent through the sprite YUV->RGB color conversion logic.	All



## **DVSACNTR—Video Sprite A Control Register**

18 YUV\_Format

Project: All Default Value: 0b

This bit specifies the source YUV format for the YUV to RGB color conversion operation. This field is ignored when source data is RGB.

Value N	a me	Description	Project
0b	BT.601	ITU-R Recommendation BT.601	All
1b	BT.709	ITU-R Recommendation BT.709	All

#### 17:16 YUV\_Byte\_Order

Project: All Default Value: 0b

This field is used to select the byte order when using YUV 4:2:2 data formats. For other formats, this field is ignored.

Value N	a me	Description	Project
00b	YUYV	YUYV (8:8:8:8 MSB-V:Y <sub>2</sub> :U:Y <sub>1</sub> )	All
01b	UYVY	UYVY (8:8:8:8 MSB-Y <sub>2:</sub> V:Y <sub>1:</sub> U)	All
10b	YVYU	YVYU (8:8:8:8 MSB-U:Y <sub>2</sub> :V:Y <sub>1</sub> )	All
11b	VYUY	VYUY (8:8:8:8 MSB-Y <sub>2:</sub> U:Y <sub>1:</sub> V)	All

#### 15 **180°\_Display\_Rotation**

Project: All Default Value: 0b

This mode causes the plane to be rotated 180°. In addition to setting this bit, software must also set the surface address offset to the lower right corner of the unrotated image and calculate the x, y offset as relative to the lower right corner.

Value Na me		Description	Project
0b	None	No rotation	All
1b	180	180° rotation	All



14	Trickle-F	Trickle-Feed_Enable							
	Project: DevSNB								
	Default Value: 0b								
	Value N	a me	Description	Description					
	0b	Enable	Trickle Feed Enabled - Data requests a space in the Display Data Buffer	are sent whenever there is	All				
	1b	Disable	Trickle Feed Disabled - Data requests	are sent in bursts.	All				
14	Reserved	<b>d</b> Proje	ect: ILK	Format:					
13:11	Reserved	<b>d</b> Proje	ect: All	Format:					
10	Tiled_Su	rface							
	Project:		All						
	Default Va	alue:	0b						
	This bit indicates that the surface data is in tiled memory. The tile pitch is specified in bytes in the DVSASTRIDE register. Only X tiling is supported for display surfaces.								
					es in the				
	DVSAST	RIDE regis s bit is set,		surfaces.					
	DVSAST When this	RIDE regis	ter. Only X tiling is supported for display	surfaces.	URFADDR				
	DVSAST When this registers.	RIDE regis	ter. Only X tiling is supported for display it affects the hardware interpretation of th	surfaces. he DVSASTART and DVSAS	URFADDR				
	DVSAST When this registers.  Value N	RIDE regis s bit is set,	ter. Only X tiling is supported for display it affects the hardware interpretation of the Description	surfaces. ne DVSASTART and DVSAS  Project	URFADDR				
9:3	DVSAST When this registers.  Value N 0b	RIDE regis s bit is set, me Linear Tiled	ter. Only X tiling is supported for display it affects the hardware interpretation of the Description  Linear memory  Tiled memory	surfaces.  ne DVSASTART and DVSAS  Project  All	URFADDR				
9:3	DVSAST When this registers.  Value N 0b 1b  Reserved	RIDE regis s bit is set, me Linear Tiled	ter. Only X tiling is supported for display it affects the hardware interpretation of the Description Linear memory Tiled memory ect: All	surfaces.  ne DVSASTART and DVSAS  Project  All  All	URFADDR				
	DVSAST When this registers.  Value N 0b 1b  Reserved	RIDE regis s bit is set, a me Linear Tiled Proj	ter. Only X tiling is supported for display it affects the hardware interpretation of the Description Linear memory Tiled memory ect: All	surfaces.  ne DVSASTART and DVSAS  Project  All  All	URFADDR				
	DVSAST When this registers.  Value N 0b 1b  Reserved Sprite_De	RIDE regis s bit is set, a me Linear Tiled Proje estination	ter. Only X tiling is supported for display it affects the hardware interpretation of the Description  Linear memory  Tiled memory  ect: All  Key	surfaces.  ne DVSASTART and DVSAS  Project  All  All	URFADDR				
	DVSAST When this registers.  Value N 0b 1b  Reserved Sprite_De Project: Default Vi This bit e key value	RIDE regis s bit is set, a me Linear Tiled Proje estination alue: enables the en in DVSAK	ter. Only X tiling is supported for display it affects the hardware interpretation of the Description Linear memory Tiled memory  ect: All  Key All	surfaces.  ne DVSASTART and DVSAS  Project All All  Format: ME  the primary plane on this pipe the primary plane pixel is parted.	urrador  ct  3Z  matches the assed				
	DVSAST When this registers.  Value N 0b 1b  Reserved Sprite_De Project: Default Vi This bit e key value	RIDE regis s bit is set, a me Linear Tiled Projuestination alue: anables the e in DVSAK he blender	ter. Only X tiling is supported for display it affects the hardware interpretation of the Description Linear memory Tiled memory  ect: All  Key All Ob destination key function. If the pixel for the EYVAL the sprite pixel is used, otherwise	surfaces.  ne DVSASTART and DVSAS  Project All All  Format: ME  the primary plane on this pipe the primary plane pixel is parted.	URFADDR  ct  3Z  e matches the assed oled.				
	DVSAST When this registers.  Value N 0b 1b  Reserved Sprite_De Project: Default Value through the	RIDE regis s bit is set, a me Linear Tiled Projuestination alue: anables the e in DVSAK he blender	ter. Only X tiling is supported for display it affects the hardware interpretation of the Description  Linear memory  Tiled memory  ect: All  Key  All  0b  destination key function. If the pixel for the EYVAL the sprite pixel is used, otherwise unmodified. Destination Key can not be	Project All Format: ME	urrador  ct  3Z  matches the assed oled.				



**Sprite Source Pixel Format Mapping of Bits to Colors:**Note: For RGB formats, see the primary source pixel format mapping

SPRITE YUV	Y1	U	Y2	v
YUV 4:2:2 YUYV	7:0	15:8	23:16	31:24
YUV 4:2:2 UYVY	15:8	7:0	31:24	23:16
YUV 4:2:2 YVYU	7:0	31:24	23:16	15:8
YUV 4:2:2 VYUY	15:8	23:16	31:24	7:0



## 4.1.10.2 DVSALINOFF—Video Sprite A Linear Offset Register

	DVSALI	NOFF—Vid	eo Sp	rite A Linear Offset Register
Register T	ype:	MMIO		
Address O	ffset:	72184h		
Project:		All		
Default Val	lue:	00000000h		
Access:		R/W		
Size (in bit	s):	32		
Double Bu	ffer Update Point:	Start of vertical	al blank o	or pipe disabled
Bit De				scription
31:0	Sprite_Linear_Offs	et Project:	All	Format:
	surface address to g aligned for RGB forr unpanned offset mu	get the address of mats and even p st be the different and the display	of the first ixel alignates ance betw	e offset into the sprite plane. This value is added to the st pixel to be displayed. This offset must be at least pixel ned for YUV formats. When performing 180° rotation, the ween the last pixel of the last line of the display data in its e address. When the surface is tiled, the contents of this

## 4.1.10.3 DVSASTRIDE—Video Sprite A Stride Register

	DVS	ASTRIDE—	·Vide	o Sprite A Stride Register		
Register Ty	/pe:	MMIO				
Address Of	ffset:	72188h				
Project:		All				
Default Val	ue:	00000000h				
Access:		R/W				
Size (in bits): 32						
Double But	fer Update Point:	Start of vertica	ıl blank	or pipe disabled or sprite disabled, after armed		
Double Buffer Armed By: Write to DVS						
Bit De				scription		
31:15	Reserved Pro	ject: All		Format:		
14:6	Sprite_Stride	Project:	All	Format:		
This is the stride for the sprite in bytes. When using linear memory, this must be 64 byte aligned. When using tiled memory, this must be 512 byte aligned. This register is updated through either a command packet passed through the command stream or writes to this register. The stride is limited to a maximum of 16K bytes when sprite scaling is not enabled, 4K bytes when sprite scaling is enabled, for both linear and tiled memory.						
5:0	Reserved Pro	ject: All		Format:		



## 4.1.10.4 DVSAPOS—Video Sprite A Position Register

		DVSAP	OS—Vi	deo S	prite A Positi	on Regis	ter		
Register Ty	ype:	MM	IIO						
Address O	721	7218Ch							
Project:		All	All						
<b>Default Val</b>	ue:	000	00000h						
Access:		R/V	V						
Size (in bits	s):	32							
Double Bu	ffer Update Po	int: Sta	rt of vertic	al blank	or pipe disabled or	sprite disabl	led, after a	rmed	
Double But	ffer Armed By	Wri	te to DVS	ASURF					
	er specifies the ay active area					care that th	e sprite d	oes not extend out	
Bit De					scription				
31:28	Reserved	Project:	All				Format:	MBZ	
27:16	Sprite_Y-Pos	sition	Project:	All	Format:				
	beginning of the position of the	the active vice lower right prite rectang	deo area. corner re	When policy to the state of the	lines of the sprite erforming 180° rota he end of the active completely contains	ation, this fiel e video area	d specifies in the unre	s the vertical otated orientation.	
15:12	Reserved	Project:	All				Format:	MBZ	
11:0	Sprite_X-Pos	sition	Project:	All	Format:				
	beginning of to position of the	the active vice original loventation. The	deo area. ver right c e defined	When pe orner rela sprite rea	in pixels of the spirorming 180° rota ative to the original ctangle must alway	ition, this field I end of the a	d specifies ctive video	the horizontal area in the	



## 4.1.10.5 DVSASIZE—Video Sprite A Size Register

	D	VSASIZE	—Vid	eo Sprite A Siz	ze Register				
Register Ty	/pe:	MMIO							
Address O		72190h	72190h						
Project:		All							
<b>Default Val</b>	ue:	00000000	h						
Access:		R/W							
Size (in bit	s):	32							
Double Bu	ffer Update Point:	Start of ve	rtical bla	nk or pipe disabled	or sprite disabled, after a	rmed			
Double Bu	ffer Armed By:	Write to D	VSASUF	RF					
	er specifies the size active area. ie. Xp				are that the sprite does	not extend out of			
Bit De				scription					
31:28	Reserved Pro	ject: All			Format:	MBZ			
27:16	Sprite_Height	Project:	All	Format:					
	This register field is used to specify the height of the sprite in lines. The value in the register is the height minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.								
15:12	Reserved Pro	ject: All			Format:	MBZ			
11:0	Sprite_Width	Project:	All	Format:					
	This register field is used to specify the width of the sprite in pixels. This does not have to be the same as the stride but should be less than or equal to the stride in pixels. The value in the register is the width minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.								
		The sprite width (actual width, not the width minus one value) is limited to even values when YUV source pixel format is used, or Pixel Multiply is set to Line/Pixel doubling or Pixel doubling.							

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## 4.1.10.6 DVSAKEYVAL—Video Sprite A Color Key Value Register

## **DVSAKEYVAL—Video Sprite A Color Key Value Register**

Register Type: MMIO
Address Offset: 72194h
Project: All
Default Value: 00000000h

Access: R/W Size (in bits): 32

**Double Buffer Update Point:** Start of vertical blank or pipe disabled

This register specifies the key color to be used with the mask bits to determine if the sprite source data matches the key. This register will only have an effect when the sprite color key is enabled. In source key mode this value is the minimum value for the range compare. In destination key mode this value is the compare value.

Bit De	scription	
31:24	Reserved Project: All	Format: MBZ
23:16	V_Source_Key_Min_Value/R_Source/Dest_Key_Value	Project: All Format:
	Specifies the color key (minimum) value for the sprite V channel sor destination key compare value.	source key or the Red channel source
15:8	Y_Source_Key_Min_Value/G_Source/Dest_Key_Value	Project: All Format:
	Specifies the color key (minimum) value for the sprite Y channel source or destination key compare value.	source key or the Green channel
7:0	U_Source_Key_Min_Value/B_Source/Dest_Key_Value	Project: All Format:
	Specifies the color key (minimum) value for the sprite U channel source or destination key compare value.	source key or the Blue channel



## 4.1.10.7 DVSAKEYMSK—Vid eo Sprite A Color Key Mask Register

## **DVSAKEYMSK—Video Sprite A Color Key Mask Register**

Register Type: MMIO
Address Offset: 72198h
Project: All
Default Value: 00000000h
Access: R/W
Size (in bits): 32

Double Buffer Update Point: Start of vertical blank or pipe disabled

For source key this register specifies which channels to perform range checking on.

For destination key this register specifies the key mask to be used with the color value bits to determine if the display source data matches the key when enabled. A zero bit in the mask indicates that the corresponding bit match failure should be ignored when determining if the pixel matches.

Note that source key and destination key are mutually exclusive modes of operation, they can not be used simultaneously. For the function that is not enabled, the associated bits in this register should be programmed to zeroes.

Bit De	scription			
31:27	Reserved Project: All	Form	at:	MBZ
26	V/R_Channel_Source_Key_Enable	Project:	All	Format:
	Specifies the source color key enable for the V/Red channel			
25	Y/G_Channel_Source_Key_Enable	Project:	All	Format:
	Specifies the source color key enable for the Y/Green channel			
24	U/B_Channel_Source_Key_Enable	Project:	All	Format:
	Specifies the source color key enable for the U/Blue channel			
23:16	R_mask_Dest_Key_Value	Project:	All	Format:
	Specifies the destination color key mask for the sprite R channel			
15:8	G_mask_Dest_Key_Value	Project:	All	Format:
	Specifies the destination color key mask for the sprite G channel			
7:0	B_mask_Dest_Key_Value	Project:	All	Format:
	Specifies the destination color key mask for the sprite B channel			

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## 4.1.10.8 DVSASURF—Video Sprite A Surface Address Register

	DVSASI	JRF—\	ideo Sprite A Surface Address Register			
Register Ty	ype:	MMIO				
Address O	ffset:	7219C	1			
Project:		All				
Default Val	ue:	00000	00h			
Access:		R/W				
Size (in bit	s):	32				
Double But	ffer Update Point:	Start of vertical blank or pipe disabled				
Writes to tl	his register arm DV	SA regis	ers			
Bit De			scription			
31:12	Sprite_Surface_Base_Address					
	Project:	All				
	Address:	Grap	nicsdress[31:12]			
	This address specifies the surface base address. When the surface is tiled, panning is specified usir (x, y) offsets in the DVSATILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DVSALINOFF register.					
	This address must be 4K aligned. It represents an offset from the graphics memory aperture base is mapped to physical pages through the global GTT. The value in this register is updated through command streamer with synchronous flips.					
11:0	Reserved Pro	oject:	All Format:			



## 4.1.10.9 DVSAKEYMAXVAL —Video Sprite A Color Key Max Value Register

Register Type: MMIO
Address Offset: 721A0h
Project: All

 Default Value:
 00000000h

 Access:
 R/W

 Size (in bits):
 32

**Double Buffer Update Point:** Start of vertical blank or pipe disabled

This register specifies the key color to be used with the mask bits to determine if the sprite source data matches the key. This register will only have an effect when the sprite source color key is enabled

Bit De	scription								
31:24	Reserved Project: All	Format: MBZ							
23:16	V_Key_Max_Value	Project: All Format:							
	Specifies the color key value for the sprite V channel								
15:8	Y_Key_Max_Value	Project: All Format:							
	Specifies the color key value for the sprite Y channel								
7:0	U_Key_Max_Value	Project: All Format:							
	Specifies the color key value for the sprite U channel								

## 4.1.10.10 DVSATILEOFF—Video Sprite A Tiled Offset Register

## **DVSATILEOFF**—Video Sprite A Tiled Offset Register

Register Type: MMIO
Address Offset: 721A4h
Project: All
Default Value: 00000000h
Access: R/W
Size (in bits): 32

**Double Buffer Update Point:** Start of vertical blank or pipe disabled

This register specifies the panning for the sprite surface in tiled memory. The surface base address is specified in the DVSASURFADDR register, and this register is used to describe an offset from that base address. When the surface is in linear memory, the offset is specified in the DVSALINOFF register and the contents of this register are ignored. When the surface is tiled, the start position is specified in this register as an (x, y) offset from the beginning of the surface.

	Bit De				scription		
Ī	31:28	Reserved	Project:	All	Format:	MBZ	



	DVSATILEOFF—Video Sprite A Tiled Offset Register										
27:16	Sprite_Start_Y-Position	Project: All Format:									
	These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180° rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.										
15:12	Reserved Project: All	Format: MBZ									
11:0	Sprite_Start_X-Position	Project: All Format:									
	These 12 bits specify the horizontal offset in pixels of the to the display surface. The offset must be even pixel align rotation, this field specifies the horizontal position of the lo active display plane in the unrotated orientation.	ned for YUV formats. When performing 180°									

# 4.1.10.11 DVSASURFLIVE—Vi deo Sprite A Live Surface Base Address Register

D	VSASURF	LIVE—Video Sprite A Live Surface Base Address Register					
Register T	ype: MMIO						
Address O	ffset: 721AC	h					
Project:	All						
<b>Default Val</b>	lue: 000000	000h					
Access:	Read C	Only					
Size (in bit	s): 32						
Bit De		scription					
31:0	Sprite_Surfa	ce_Base_Address					
	Project:	All					
	Address:	GraphicsAddress[31:0]					
	This gives the live value of the surface base address as being currently used for the plane.						



## 4.1.10.12 DVSASCALE—Video Sprite A Scaler Control

#### **DVSASCALE**—Video Sprite A Scaler Control

Register Type: MMIO
Address Offset: 72204h
Project: All
Default Value: 00000000h

 Default Value:
 00000000

 Access:
 R/W

 Size (in bits):
 32

Double Buffer Update Point: Start of vertical blank or pipe disabled or sprite disabled, after armed

Double Buffer Armed By: Write to DVSASURF

This register controls the sprite scaling. The DVSASIZE register gives the destination (output to pipe) size of the sprite. This register gives the source (input to sprite) size of the sprite. When scaling is enabled, the source size will be scaled up or down to the destination size.

Upscaling of any amount is allowed. Downscaling up to 16X (source/destination) is allowed. Downscaling greater than 2X will involve decimation. Downscaling increases memory bandwidth requirements. Scaling can not be used with the sprite 64bpp source pixel format. Source and destination sizes must be 3x3 (3x6 when interlacing) or greater when scaling is enabled.

Horizontal downscaling limits the maximum dot clock allowed as percent of cdclk. Rules to calculate the allowed dot clock:

Start with maximum dot clock 90% of cdclk. (There is a separate requirement that planes using 64bpp formats can not be enabled with dot clock >80% of cdclk when sprite is enabled on the same pipe) Subtract 10% more per horizontal decimation step (decimation steps at 2x, 4x, 8x, and 16x downscale). Subtract 10% more if sprite is using the RGB data format.

Subtract 10% more if sprite scaling is enabled on the other pipe.

Then divide that by horizontal downscale amount within each decimation step.

The result is the maximum allowed dot clock as percent of cdclk frequency.

#### Example:

Scale factor	<b>Decimation</b> amount	YUV single pipe dot clock %	YUV dual pipe dot clock %	RGB single pipe dot clock %	RGB dual pipe dot clock %	Comment
1	1	90	80	80	70	No scaling
1.5	1	60	53	53	46	
1.99	1	45	40	40	35	Max downscale before decimation starts
2	2	80	70	70	60	
3	2	53	46	46	40	
3.99	2	40	35	35	30	
4	4	70	60	60	50	
6	4	46	40	40	33	
7.99	4	35	30	30	25	
8	8	60	50	50	40	
12	8	40	33	33	26	
15.99	8	30	25	25	20	Worst case dot clock
16	16	50	40	40	30	Max downscaling allowed

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		DVS	ASCALE—Video Sprite A Scaler Control							
Bit De		scription								
31	Scaling_Enable Project: All Format: Enable  Enables the scaling function. Source width can be no more than 4k bytes. For best picture quality, disable when scaling is not required.									
30:29	Filter_Co	ntrol								
	Project: All									
	Default Va	alue:	0b							
	Filter sele	ection								
	Value N	a me	Description	Project						
	00b	Medium	Medium Filtering	All						
	01b	Enhancing	g Edge Enhancing Filtering	All						
	10b	Softening	Edge Softening Filtering	All						
	11b	Reserved	Reserved	All						
	Project: Default Va	d_Field_Off alue:	All Ob							
	Project: Default Value Select the surface da	alue: e vertical off ata.	All 0b set of the filtered data. Software is responsible for updating this to matc	1						
	Project: Default Value N	alue: e vertical off ata. a me	All 0b set of the filtered data. Software is responsible for updating this to matc  Description	Project						
	Project: Default Value N Ob	alue: e vertical offata.  a me	All 0b set of the filtered data. Software is responsible for updating this to matc  Description Vertical initial phase of 0	Project All						
07	Project: Default Value Nob	alue: e vertical offeata.  a me 0 0.5	All 0b set of the filtered data. Software is responsible for updating this to mato  Description  Vertical initial phase of 0  Vertical initial phase of 0.5	Project						
27	Project: Default Value Nob 1b Even/Ode	alue: e vertical offata.  a me	All 0b set of the filtered data. Software is responsible for updating this to mato  Description  Vertical initial phase of 0  Vertical initial phase of 0.5  able	Project All						
27	Project: Default Value Nob 1b Even/Ode Project:	alue: e vertical off ata.  a me 0 0.5 d_Field_En	All 0b set of the filtered data. Software is responsible for updating this to mate  Description Vertical initial phase of 0 Vertical initial phase of 0.5  able All	Project All						
27	Project: Default Value N Ob 1b Even/Odd Project: Default Va	alue: e vertical offeata.  a me 0 0.5 d_Field_En	All 0b set of the filtered data. Software is responsible for updating this to mato  Description  Vertical initial phase of 0  Vertical initial phase of 0.5  able	Project All						
27	Project: Default Value N Ob 1b Even/Odd Project: Default Va	alue: e vertical offeata.  a me 0 0.5 d_Field_En alue:	All 0b set of the filtered data. Software is responsible for updating this to mato  Description  Vertical initial phase of 0  Vertical initial phase of 0.5  able All 0b	Project All						
27	Project: Default Value Nob 1b Even/Ode Project: Default Value Nob 1c	alue: e vertical offeata.  a me 0 0.5 d_Field_En alue:	All 0b set of the filtered data. Software is responsible for updating this to mato  Description  Vertical initial phase of 0  Vertical initial phase of 0.5  able All 0b the vertical offset of the filtered data.	Project All All						
27	Project: Default Value Nob 1b Even/Ode Project: Default Value Nob And Project: Default Value Nob Even/Ode Project: Default Value Nob Even/Ode	alue: e vertical off ata.  a me 0 0.5 d_Field_En alue: djustment of	All 0b set of the filtered data. Software is responsible for updating this to mate  Description Vertical initial phase of 0 Vertical initial phase of 0.5  able All 0b the vertical offset of the filtered data.  Description	Project All All Project						
27	Project: Default Value N Ob Teven/Ode Project: Default Value N Ob Under N Ob Ob Ob	alue: e vertical offeata.  a me 0 0.5 d_Field_En alue: djustment of a me Disable Enable	All 0b set of the filtered data. Software is responsible for updating this to mato  Description  Vertical initial phase of 0  Vertical initial phase of 0.5  able All 0b if the vertical offset of the filtered data.  Description  Off (Vertical initial phase is 1/2 the scale factor)	Project All Project All						
	Project: Default Value Nob 1b Even/Ode Project: Default Value Nob 1b Source_Nob The horizing 3. The 4k bytes,	alue: e vertical officata.  a me 0 0.5 d_Field_En alue: djustment of a me Disable Enable Vidth ontal size of value progrecounting free	All 0b set of the filtered data. Software is responsible for updating this to mato  Description  Vertical initial phase of 0  Vertical initial phase of 0.5  able All 0b it the vertical offset of the filtered data.  Description  Off (Vertical initial phase is 1/2 the scale factor)  On (Vertical initial phase is selected by the Even/Off Field Offset bit)	Project All All Project All All aminimum more than						



DVSASCALE—Video Sprite A Scaler Control									
10:0	Source_Height Project: All Format:								
	The vertical size of the source image to be scaled in lines. If the source is a field, this is the number of lines in the field. Max number of lines is 2048; minimum is 3 (6 when interlacing). The value programmed is one less than the number of lines.								
	The height must be end of the three			is enabled and the pipe has set planes to interlaced fetch. odd.					

## 4.1.10.13 DVSAGAMC—Video Sprite A Gamma Correction Registers

				DV	SGAM	C Ref	erenc	e Point		
Project:		All								
Bit De							scripti	on		
31:30	Rese	Reserved Project: All Format:								Format:
29:20	Red	Gamm	a Referenc	e Point				Project:	All	Format:
19:10	Green Gamma Reference Point							Project:	All	Format:
9:0	Blue	Gamm	na Referen	ce Point	t			Project:	All	Format:
				DVSG	AMC	Max R	efere	nce Poin	f	
Project:		All								
Bit De							scripti	on		
31:11	Rese	rved	Project:	All		Format:				
10:0	Fina	Gamn	na Max Re	ference	Point			Project:	All	Format:
		DVSA	AGAMC-	-Vide	o Spri	ite A G	amm	a Correct	tion	Registers
Register T	ype:	MMIO								
Address O	ffset:	72300	)h							
Project:		All								
Default Val	lue:	: 00000000h; 04010040h; 08020080h; 0C0300C0h; 10040100h; 14050140h; 18060180h; 1C0701C0h; 20080200h; 24090240h; 280A0280h; 2C0B02C0h; 300C0300h; 340D0340h; 380E0380h; 3C0F03C0h; 00000400h; 00000400h; 00000400h;								
Access:		R/W								
Size (in bit	s):	19x32								



These registers are used to determine the characteristics of the gamma correction for the sprite pixel data *pre-blending*. Additional gamma correction can be done in the display pipe gamma if desired.

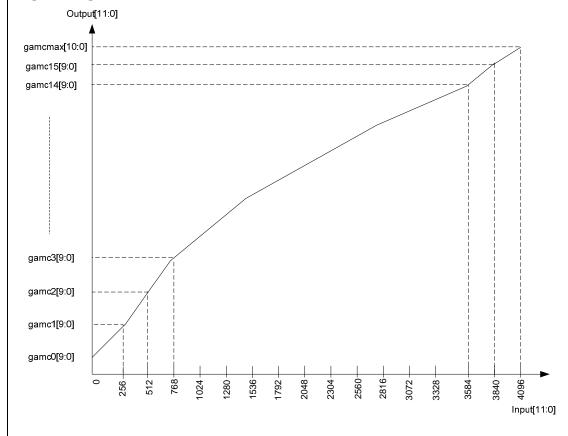
The gamma correction curve is represented by specifying a set of reference points spaced equally along the desired curve. Red, Green, and Blue each have 17 reference points. The first 16 reference points are 10 bit values with Red, Green, and Blue sharing a single register for each point. The final max reference point is an 11 bit value with separate registers for Red, Green, and Blue. The curve must be flat or increasing, never decreasing.

During operation the appropriate reference point pairs (adjacent) are selected for each color, and the output is interpolated between these two reference point values.

The gamma correction registers are not double-buffered. They should only be updated when the sprite is off, otherwise, screen artifacts may show.

To pass sprite pixel data through gamma correction unchanged, program the gamma reference points to the default linear ramp values. When the output from sprite is set in YUV format by programming CSC bypass, or the sprite source pixel format is RGB, the sprite gamma correction will be bypassed.

#### Programming of the Piecewise-linear Estimation of Gamma Correction Curve



DWord Bi	t	Description					
0	31:0	GAMC0	Project:	All	Format:	DVSGAMC Reference Point	
1	31:0	GAMC1	Project:	All	Format:	DVSGAMC Reference Point	



2	31:0	GAMC2	Project:	All	Format:	DVSGAMC Reference Point
3	31:0	GAMC3	Project:	All	Format:	DVSGAMC Reference Point
4	31:0	GAMC4	Project:	All	Format:	DVSGAMC Reference Point
5	31:0	GAMC5	Project:	All	Format:	DVSGAMC Reference Point
6	31:0	GAMC6	Project:	All	Format:	DVSGAMC Reference Point
7	31:0	GAMC7	Project:	All	Format:	DVSGAMC Reference Point
8	31:0	GAMC8	Project:	All	Format:	DVSGAMC Reference Point
9	31:0	GAMC9	Project:	All	Format:	DVSGAMC Reference Point
10	31:0	GAMC10	Project:	All	Format:	DVSGAMC Reference Point
11	31:0	GAMC11	Project:	All	Format:	DVSGAMC Reference Point
12	31:0	GAMC12	Project:	All	Format:	DVSGAMC Reference Point
13	31:0	GAMC13	Project:	All	Format:	DVSGAMC Reference Point
14	31:0	GAMC14	Project:	All	Format:	DVSGAMC Reference Point
15	31:0	GAMC15	Project:	All	Format:	DVSGAMC Reference Point
16	31:0	GAMCmaxR	Project:	All	Format:	DVSGAMC Max Reference Point
17	31:0	GAMCmaxG	Project:	All	Format:	DVSGAMC Max Reference Point
18	31:0	GAMCmaxB	Project:	All	Format:	DVSGAMC Max Reference Point

## 4.1.11 Video Sprite B Control

The DVSBCNTR, DVSBSTRIDE, DVSBPOS, DVSBSIZE, and DVSBSCALE active registers will be updated on the vertical blank or when pipe is disabled, after the DVSBSURF trigger register is written, or when the sprite B is not yet enabled – thus providing an atomic update of the video sprite B control, stride, position, size, scale, and base address registers.



## 4.1.11.1 DVSBCNT R—Video Sprite B Control Register

		DVS	BCNTR—Video Sprite B Control Register			
Register Type:			MMIO			
Address Offset:			73180h			
Project:			All			
<b>Default Val</b>	lue:		0000000h			
Access:			R/W			
Size (in bits	s):		32			
Double But			Start of vertical blank or pipe disabled or sprite disabled, after armed			
Double But			Write to DVSBSURF			
Video Sprit	e B Plane	is connec	eted to pipe B only.			
Bit De			scription			
31	Sprite_E	nable	Project: All Format: Enable			
	memory f the plane	fetches ceas e. When in S	the sprite plane will generate pixels for display. When set to zero, sprite se and plane output is transparent. The display pipe must be enabled to Self Refresh Big FIFO mode, write to this register to enable the plane will delayed while Big FIFO mode is exiting.	o enable		
30	Gamma_	_Enable				
	Project:		All			
	Default V	'alue:	0b			
	There are two gamma adjustments possible in the video sprite data path. This bit controls the gamma correction in the display pipe not the gamma control in this plane. It affects only the pixel data from this display plane. Gamma correction logic that is contained in the video sprite is disabled by loading the default values into those registers.					
	correction this displ	n in the display plane. G	olay pipe not the gamma control in this plane. It affects only the pixel da Samma correction logic that is contained in the video sprite is disabled b	ata from		
	correction this displ	n in the display plane. Gult values in	olay pipe not the gamma control in this plane. It affects only the pixel da Samma correction logic that is contained in the video sprite is disabled b	ata from		
	correction this display the defau	n in the display plane. Gult values in	play pipe not the gamma control in this plane. It affects only the pixel da Gamma correction logic that is contained in the video sprite is disabled but to those registers.	ata from by loading		
	correctio this displ the defau	n in the display plane. Gult values in	play pipe not the gamma control in this plane. It affects only the pixel da Gamma correction logic that is contained in the video sprite is disabled be to those registers.  Description	eta from by loading  Project		
29	correction this displication the defaution value N	n in the display plane. Gult values into the line of t	clay pipe not the gamma control in this plane. It affects only the pixel da Gamma correction logic that is contained in the video sprite is disabled be to those registers.  Description  Plane pixel data bypasses the display pipe gamma correction logic  Plane pixel data is gamma corrected in the pipe gamma correction logic	Project All All		
29	value N 0b 1b Reserved	n in the display plane. Gult values into the line of t	play pipe not the gamma control in this plane. It affects only the pixel da Gamma correction logic that is contained in the video sprite is disabled be to those registers.  Description  Plane pixel data bypasses the display pipe gamma correction logic  Plane pixel data is gamma corrected in the pipe gamma correction logic  ect: All Format: MBZ	Project All All		
	correction this display the defaution of	n in the display plane. Gult values into the line of t	play pipe not the gamma control in this plane. It affects only the pixel da Gamma correction logic that is contained in the video sprite is disabled be to those registers.  Description  Plane pixel data bypasses the display pipe gamma correction logic  Plane pixel data is gamma corrected in the pipe gamma correction logic  ect: All Format: MBZ  ss-512_Format_Conversion	Project All All		
	value N 0b 1b Reserved	n in the display plane. Gult values into la	play pipe not the gamma control in this plane. It affects only the pixel da Gamma correction logic that is contained in the video sprite is disabled be to those registers.  Description  Plane pixel data bypasses the display pipe gamma correction logic  Plane pixel data is gamma corrected in the pipe gamma correction logic  ect: All Format: MBZ	Project All All		
	value N Ob 1b Reserved YUV_By  Project:	n in the display plane. Gult values into la	play pipe not the gamma control in this plane. It affects only the pixel da Gamma correction logic that is contained in the video sprite is disabled by to those registers.  Description  Plane pixel data bypasses the display pipe gamma correction logic  Plane pixel data is gamma corrected in the pipe gamma correction logic  ect: All Format: MBZ  ss-512_Format_Conversion  All	Project All All		
	value N Ob 1b Reserved YUV_By  Project: Default V	n in the display plane. Gult values into la	play pipe not the gamma control in this plane. It affects only the pixel da Gamma correction logic that is contained in the video sprite is disabled by to those registers.  Description  Plane pixel data bypasses the display pipe gamma correction logic  Plane pixel data is gamma corrected in the pipe gamma correction logic  ect: All Format: MBZ  ss-512_Format_Conversion  All  Ob	Project All All		



#### **DVSBCNTR—Video Sprite B Control Register**

27 Range\_Correction\_Disable

Project: All Default Value: 0b

Setting this bit disables the YUV range correction logic. Normally the range compressed YUV is expanded to full range RGB, setting this bit will generate range compressed RGB. This bit should also be used if full range YUV source material is used. This bit has no effect on RGB source formats.

Value N	a me	Description	Project
0b	Enable	Range correction enabled	All
1b	Disable	No range correction	All

26:25 Source\_Pixel\_Format

Project: DevSNB

Default Value: 0b

This field selects the pixel format for the sprite. Before entering the blender, each source format is converted to 12 bits per pixel.

Value Na me		Description	
00b	YUV 4:2:2	YUV 4:2:2 packed pixel format (byte order programmed separately)	All
01b	RGB 32-bit 2:10:10:10	RGB 32-bit 2:10:10:10 pixel format (color order programmed separately). Ignore alpha.	All
10b	RGB 32-bit 8:8:8	RGB 32-bit 8:8:8:8 pixel format (color order programmed separately). Ignore alpha.	All
11b	RGB 64-bit 16:16:16:16 Use of 64bpp format will limit the maximum dot clock to 80% of cdclk.	RGB 64-bit 16:16:16:16 floating point pixel format (color order programmed separately). Ignore alpha.	All

#### 26:25 **Source\_Pixel\_Format**

Project: DevILK
Default Value: 0b

This field selects the pixel format for the sprite. Before entering the blender, each source format is converted to 12 bits per pixel.

Value N	a me	Description	Project
00b	YUV 4:2:2	YUV 4:2:2 packed pixel format (byte order programmed separately)	All
01b	Reserved	Reserved	All
10b	32-bit BGRX	32-bit BGRX (8:8:8 MSB-X:R:G:B) pixel format. Ignore alpha.	All
11b	Reserved	Reserved	All



## **DVSBCNTR—Video Sprite B Control Register**

24 Pipe\_Color\_Space\_Conversion\_Enable

Project: All Default Value: 0b

This bit enables pipe color space conversion for the plane pixel data. This is separate from the color conversion logic within the sprite plane. CSC mode in the pipe CSC registers must be set to match the format of the plane pixel data after the color conversion logic within the sprite plane.

Value N	a me	Description	Project
0b	Disable	Plane pixel data bypasses the pipe color space conversion logic	All
1b	Enable	Plane pixel data passes through the pipe color space conversion logic	All

23 **Reserved** Project: All Format: MBZ

22 Sprite\_Source\_Key\_Enable

Project: All Default Value: 0b

This bit enables source color keying. Sprite pixel values that match (within range) the key will become transparent. Source key can not be enabled if destination key is enabled.

Value N	a me	Description	Project
0b	Disable	Sprite source key is disabled	All
1b	Enable	Sprite source key is enabled	All

22 Sprite\_Source\_Key\_Enable

Project: All Default Value: 0b

This bit enables source color keying. Sprite pixel values that match (within range) the key will become transparent. Source key can not be enabled if destination key is enabled.

Value N	a me	Description	Project
0b		Sprite source key is disabled	All
1b		Sprite source key is enabled	All



DVSBCNTR—Video	Sprite B	Control	Register
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Plane\_Extended\_Range\_Source\_Select

Project: DevSNB Default Value: 0b

This bit is used to indicate when the plane source pixel format should be processed as having extended range. This is only valid with certain source pixel formats. If the pipe is extended range and plane extended range source is not selected, the plane will fit the source pixel data into the 0 to 1 region of the extended range.

	Value N	a me	Description	Project
ſ	0b	Normal	Normal range source selected	All
ſ	1b	Extended	Extended range source selected	All

21 Reserved Project: DevILK Format:

20 RGB\_Color\_Order

Project: DevSNB Default Value: 0b

This field is used to select the color order when using RGB data formats. For other formats, this field is ignored.

Value N	a me	Description	Project
0b	BGRX	BGRX (MSB-X:R:G:B)	All
1b	RGBX	RGBX (MSB-X:B:G:R)	All

20 Reserved Project: DevILK Format:

Color\_Conversion\_Disabled

Project: All Default Value: 0b

This bit enables or disables the color conversion logic internal to the sprite. Color conversion is intended to be used with the formats that support YUV format. This bit is ignored when using RGB source formats.

Value N	a me	Description	Project
0b	Enable	Pixel data is sent through the sprite color conversion logic (only applies to YUV formats)	All
1b	Disable	Pixel data is not sent through the sprite YUV->RGB color conversion logic.	All



## **DVSBCNTR—Video Sprite B Control Register**

18 YUV\_Format

Project: All Default Value: 0b

This bit specifies the source YUV format for the YUV to RGB color conversion operation. This field is ignored when source data is RGB.

Value N	a me	Description	Project
0b	BT.601	ITU-R Recommendation BT.601	All
1b	BT.709	ITU-R Recommendation BT.709	All

#### 17:16 YUV\_Byte\_Order

Project: All Default Value: 0b

This field is used to select the byte order when using YUV 4:2:2 data formats. For other formats, this field is ignored.

Value Na me		Description	Project
00b	YUYV	YUYV (8:8:8:8 MSB-V:Y <sub>2:</sub> U:Y <sub>1</sub> ) All	
01b	UYVY	UYVY (8:8:8:8 MSB-Y <sub>2</sub> :V:Y <sub>1</sub> :U) All	
10b	YVYU	YVYU (8:8:8:8 MSB-U:Y <sub>2</sub> :V:Y <sub>1</sub> ) All	
11b	VYUY	VYUY (8:8:8:8 MSB-Y <sub>2</sub> :U:Y <sub>1</sub> :V) All	

#### 15 **180°\_Display\_Rotation**

Project: All Default Value: 0b

This mode causes the plane to be rotated 180°. In addition to setting this bit, software must also set the surface address offset to the lower right corner of the unrotated image and calculate the x, y offset as relative to the lower right corner.

Value Na me		Description	Project
0b	None	No rotation All	
1b	180	180° rotation All	

## 14 Trickle-Feed\_Enable

Project: DevSNB Default Value: 0b

Valu	e Na me	Description	Project
0b	Ob Enable Trickle Feed Enabled - Data requests are sent whenever there is space in the Display Data Buffer All		All
1b	Disable	Trickle Feed Disabled - Data requests are sent in bursts.	All

14 **Reserved** Project: DevILK Format:



		DVS	BCNTR—Vid	eo Sprite B Control Register		
13:11	Reserved Project: All			Format:		
10	Tiled_Surface					
	Project:		All			
	Default V	alue:	0b			
	This bit indicates that the surface data is in tiled memory. The tile pitch is specified in bytes in the DVSBSTRIDE register. Only X tiling is supported for display surfaces.					
	When this bit is set, it affects the hardware interpretation of the DVSBSTART and DVSBSURFADDR registers.					
	Value N	a me	Description	Project		
	0b	Linear	Linear memory	All		
	1b	Tiled	Tiled memory	All		
9:3	Reserved Project: All Format: MBZ					
2	Sprite_Destination_Key					
	Project: All					
	Default Value: 0b					
	This bit enables the destination key function. If the pixel for the primary plane on this pipe matches the key value in DVSBKEYVAL the sprite pixel is used, otherwise the primary plane pixel is passed through the blender unmodified. Destination Key can not be enabled if source key is enabled.					
	Value N	a me	Description	Project		
	0b	Disable	Destination Key	is disabled All		
	1b	Enable	Destination Key	is enabled All		
1:0	Reserved Project: All Format: MBZ					

See DVSACNTR - Sprite Source Pixel Format Mapping of Bits to Colors

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### 4.1.11.2 DVSBLINOFF—Video Sprite B Linear Offset Register

	DVSBLI	NOFF—Video Sprite B Linear Offset Register					
Register Ty	ype:	MMIO					
Address O	ffset:	73184h					
Project:		All					
Default Val	lue:	0000000h					
Access:		R/W					
Size (in bit	s):	32					
Double Bu	ffer Update Point:	Start of vertical blank or pipe disabled					
Bit De		scription					
31:0	Sprite_Linear_Offs	Sprite_Linear_Offset Project: All Format:					
	This register provides the linear panning byte offset into the sprite plane. This value is added to the surface address to get the address of the first pixel to be displayed. This offset must be at least pixel aligned for RGB formats and even pixel aligned for YUV formats. When performing 180° rotation, the unpanned offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address. When the surface is tiled, the contents of this register are ignored.						



## 4.1.11.3 DVSBSTRIDE—Video Sprite B Stride Register

DVSBSTRIDE—Video Sprite B Stride Register							
Register Type:	Type: MMIO						
<b>Address Offset:</b>		73188h					
Project:		All					
<b>Default Value:</b>		00000000h					
Access:		R/W					
Size (in bits):		32					
<b>Double Buffer Up</b>	date Point:	Start of verti	cal blank	or pipe disabled or sprite disabled, after armed			
<b>Double Buffer Arm</b>	ned By:	Write to DVS	BSURF				
Bit De				scription			
31:15 Reser	ved Pro	ect: All		Format:			
14:6 Sprite	_Stride	Project:	All	Format:			
When comm to a m	This is the stride for the sprite in bytes. When using linear memory, this must be 64 byte aligned. When using tiled memory, this must be 512 byte aligned. This register is updated through either a command packet passed through the command stream or writes to this register. The stride is limited to a maximum of 16K bytes when sprite scaling is enabled, for both linear and tiled memory.						
5:0 Reser	<b>ved</b> Pro	ect: All		Format:			

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### 4.1.11.4 DVSBPOS—Video Sprite B Position Register

-									
	DVSBPOS—Video Sprite B Position Register								
Register T	ype:	MM	10						
Address O	ffset:	731	8Ch						
Project:		All							
<b>Default Val</b>	lue:	000	00000h						
Access:		R/W	'						
Size (in bit	s):	32							
Double Bu	ffer Update Point	t: Star	t of vertica	al blank o	r pipe disabled c	or sprite disal	bled, after a	rmed	
Double Bu	ffer Armed By:	Writ	e to DVSE	BSURF					
	er specifies the pay active area.					care that t	he sprite d	oes not extend out	
Bit De					scription				
31:28	Reserved	Project:	All				Format:	MBZ	
27:16	Sprite_Y-Positi	on	Project:	All	Format:				
	These 12 bits specify the vertical position in lines of the sprite (upper left corner) relative to the beginning of the active video area. When performing 180° rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.								
15:12	Reserved	Project:	All				Format:	MBZ	
11:0	Sprite_X-Positi	on	Project:	All	Format:				
	These 12 bits specify the horizontal position in pixels of the sprite (upper left corner) relative the beginning of the active video area. When performing 180° rotation, this field specifies the horizontal position of the original lower right corner relative to the original end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.								



### 4.1.11.5 DVSBSIZE—Video Sprite B Size Register

		DVSB	SIZE-	–Vic	leo Sprite B Siz	e Register	
Register T	ype:	MMI	0				
Address O	ffset:	7319	90h				
Project:		All					
Default Val	lue:	0000	0000h				
Access:		R/W					
Size (in bit	s):	32					
Double Bu	ffer Update Poi	nt: Start	of vert	ical bl	ank or pipe disabled o	or sprite disabled, after a	ırmed
Double Bu	ffer Armed By:	Write	e to DV	SBSU	RF		
	er specifies the active area. i					re that the sprite does	not extend out of
Bit De					scription		
31:28	Reserved	Project:	All			Format:	MBZ
27:16	Sprite_Height	t Pro	ject:	All	Format:		
	height minus of	This register field is used to specify the height of the sprite in lines. The value in the register is the height minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.					
15:12	Reserved	Project:	All			Format:	MBZ
11:0	Sprite_Width	Pro	ject:	All	Format:		
	same as the s	This register field is used to specify the width of the sprite in pixels. This does not have to be the same as the stride but should be less than or equal to the stride in pixels. The value in the register is the width minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.					
		The sprite width (actual width, not the width minus one value) is limited to even values when YUV source pixel format is used, or Pixel Multiply is set to Line/Pixel doubling or Pixel doubling.					

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### 4.1.11.6 DVSBKEYVAL—Video Sprite B Color Key Value Register

### **DVSBKEYVAL—Video Sprite B Color Key Value Register**

Register Type: MMIO
Address Offset: 73194h
Project: All

 Default Value:
 00000000h

 Access:
 R/W

 Size (in bits):
 32

**Double Buffer Update Point:** Start of vertical blank or pipe disabled

This register specifies the key color to be used with the mask bits to determine if the sprite source data matches the key. This register will only have an effect when the sprite color key is enabled. In source key mode this value is the minimum value for the range compare. In destination key mode this value is the compare value.

Bit De	scription								
31:24	Reserved Project: All	Format: MBZ							
23:16	V_Source_Key_Min_Value/R_Source/Dest_Key_Value	Project: All Format:							
	Specifies the color key (minimum) value for the sprite V channel sor destination key compare value.	source key or the Red channel source							
15:8	Y_Source_Key_Min_Value/G_Source/Dest_Key_Value	Project: All Format:							
	Specifies the color key (minimum) value for the sprite Y channel source or destination key compare value.	source key or the Green channel							
7:0	U_Source_Key_Min_Value/B_Source/Dest_Key_Value	Project: All Format:							
	Specifies the color key (minimum) value for the sprite U channel source or destination key compare value.	source key or the Blue channel							



### 4.1.11.7 DVSBKEYMSK—Vid eo Sprite B Color Key Mask Register

#### **DVSBKEYMSK—Video Sprite B Color Key Mask Register**

Register Type: MMIO
Address Offset: 73198h
Project: All
Default Value: 00000000h
Access: R/W
Size (in bits): 32

Double Buffer Update Point: Start of vertical blank or pipe disabled

For source key this register specifies which channels to perform range checking on.

For destination key this register specifies the key mask to be used with the color value bits to determine if the display source data matches the key when enabled. A zero bit in the mask indicates that the corresponding bit match failure should be ignored when determining if the pixel matches.

Note that source key and destination key are mutually exclusive modes of operation, they can not be used simultaneously. For the function that is not enabled, the associated bits in this register should be programmed to zeroes.

Bit De	scription			
31:27	Reserved Project: All	Forma	at:	MBZ
26	V/R_Channel_Source_Key_Enable	Project:	All	Format:
	Specifies the source color key enable for the V/Red channel			
25	Y/G_Channel_Source_Key_Enable	Project:	All	Format:
	Specifies the source color key enable for the Y/Green channel			
24	U/B_Channel_Source_Key_Enable	Project:	All	Format:
	Specifies the source color key enable for the U/Blue channel			
23:16	R_mask_Dest_Key_Value	Project:	All	Format:
	Specifies the destination color key mask for the sprite R channel			
15:8	G_mask_Dest_Key_Value	Project:	All	Format:
	Specifies the destination color key mask for the sprite G channel			
7:0	B_mask_Dest_Key_Value	Project:	All	Format:
	Specifies the destination color key mask for the sprite B channel			

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## 4.1.11.8 DVSBSURF—Video Sprite B Surface Address Register

	DVSBSU	JRF—Video Sp	rite B Surface Address Register					
Register Ty	ype:	MMIO	MMIO					
Address O	ffset:	7319Ch						
Project:		All						
<b>Default Val</b>	ue:	00000000h						
Access:		R/W						
Size (in bit	s):	32						
Double But	ffer Update Point:	Start of vertical bla	ank or pipe disabled					
Writes to tl	his register arm DV	SB registers						
Bit De			scription					
31:12	Sprite_Surface_B	ase_Address						
	Project:	All						
	Address:	GraphicsAddres	s[31:12]					
	This address specifies the surface base address. When the surface is tiled, panning is specified using (x, y) offsets in the DVSBTILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DVSBLINOFF register.							
This address must be 4K aligned. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. The value in this register is updated through the command streamer with synchronous flips.								
11:0	Reserved Pro	oject: All	Format:					



#### 4.1.11.9 DVSBKEYMAXVAL —Video Sprite B Color Key Max Value Register

#### **DVSBKEYMAXVAL—Video Sprite B Color Key Max Value Register**

Register Type: MMIO
Address Offset: 731A0h
Project: All

 Default Value:
 00000000h

 Access:
 R/W

 Size (in bits):
 32

**Double Buffer Update Point:** Start of vertical blank or pipe disabled

This register specifies the key color to be used with the mask bits to determine if the sprite source data matches the key. This register will only have an effect when the sprite source color key is enabled.

Bit De	scription							
31:24	Reserved Project: All	Format: MBZ						
23:16	V_Key_Max_Value	Project: All Format:						
	Specifies the color key value for the sprite V channel							
15:8	Y_Key_Max_Value	Project: All Format:						
	Specifies the color key value for the sprite Y channel							
7:0	U_Key_Max_Value	Project: All Format:						
	Specifies the color key value for the sprite U channel							

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### 4.1.11.10 DVSBTILEOFF—Video Sprite B Tiled Offset Register

### **DVSBTILEOFF**—Video Sprite B Tiled Offset Register

Register Type: MMIO
Address Offset: 731A4h
Project: All
Default Value: 00000000h

Access: R/W
Size (in bits): 32
Trusted Type: 1

**Double Buffer Update Point:** Start of vertical blank or pipe disabled

This register specifies the panning for the sprite surface in tiled memory. The surface base address is specified in the DVSBSURFADDR register, and this register is used to describe an offset from that base address. When the surface is in linear memory, the offset is specified in the DVSBLINOFF register and the contents of this register are ignored. When the surface is tiled, the start position is specified in this register as an (x, y) offset from the beginning of the surface.

Bit De	scription					
31:28	Reserved Project: All	Format: MBZ				
27:16	Sprite_Start_Y-Position	Project: All Format:				
	These 12 bits specify the vertical position in lines of the the display surface. When performing 180° rotation, th right corner relative to the start of the active display pla	is field specifies the vertical position of the lower				
15:12	Reserved Project: All	Format: MBZ				
11:0	Sprite_Start_X-Position	Project: All Format:				
	These 12 bits specify the horizontal offset in pixels of the to the display surface. The offset must be even pixel a rotation, this field specifies the horizontal position of the active display plane in the unrotated orientation.	ligned for YUV formats. When performing 180°				



# 4.1.11.11 DVSBSURFLIVE—Vi deo Sprite B Live Surface Base Address Register

D	VSBSU	JRFLIVE—Video Sprite B Live Surface Base Address Register				
Register Ty	ype: M	MIO				
Address O	ffset: 73	1ACh				
Project:	Al					
<b>Default Val</b>	lue: 00	000000h				
Access:	Re	ead Only				
Size (in bit	<b>s)</b> : 32					
Bit De		scription				
31:0	Sprite_Surface_Base_Address					
	Project:	All				
	Address	: GraphicsAddress[31:0]				
	This gives the live value of the surface base address as being currently used for the plane.					

### 4.1.11.12 DVSBSCALE—Video Sprite B Scaler Control

DVSBSCALE—Video Sprite B Scaler Control						
Register Type:	MMIO					
Address Offset:	73204h					
Project:	All					
Default Value:	0000000h					
Access:	R/W					
Size (in bits):	32					
<b>Double Buffer Update Point:</b>	Start of vertical blank or pipe disabled or sprite disabled, after armed					
Double Buffer Armed By:	Write to DVSBSURF					

This register controls the sprite scaling. The DVSBSIZE register gives the destination (output to pipe) size of the sprite. This register gives the source (input to sprite) size of the sprite. When scaling is enabled, the source size will be scaled up or down to the destination size.

Upscaling of any amount is allowed. Downscaling up to 16X (source/destination) is allowed. Downscaling greater than 2X will involve decimation. Downscaling increases memory bandwidth requirements. Scaling can not be used with the sprite 64bpp source pixel format. Source and destination sizes must be 3x3 (3x6 when interlacing) or greater when scaling is enabled.

Horizontal downscaling limits the maximum dot clock allowed as percent of cdclk. See DVSASCALE for the rules to calculate the allowed dot clock.

Bit	Description							
31	Scaling_Enable	Project:	All	Format:	Enable			
		is not required.	. When ir		than 4k bytes. For best picture quality, Big FIFO mode, scaling enable will be			



30:29	Filter_Control								
	Project:		All	All					
	Default Value:		0b						
	Filter sele								
	Value Na me		Description	Project					
	00b Medium		Medium Filtering	All					
01b		Enhancin	g Edge Enhancing Filtering	All					
	10b Softening		Edge Softening Filtering						
	11b	Reserved	Reserved	All					
28	Even/Odd_Field_Offset								
	Project:								
	Default V	Default Value: 0b							
	Select the vertical offset of the filtered data. Software is responsible for updating this to match the surface data.								
	Value N	la me	Description						
	0b	0	Vertical initial phase of 0	All					
	1b	0.5	Vertical initial phase of 0.5	All					
27	Even/Odd_Field_Enable								
	Project:								
	Default V	Default Value: 0b							
	Enable adjustment of the vertical offset of the filtered data.								
	Enable a	-,	r the vertical offset of the filtered data.						
	Value N	1	Description	Project					
		1		<b>Project</b>					
	Value N	la me	Description						
26:16	Value N	la me Disable Enable	Description Off (Vertical initial phase is 1/2 the scale factor)	All					
26:16	Value N 0b 1b Source_ The horiz is 3. The 4k bytes,	Na me Disable Enable Width contal size of a value programming from	Description  Off (Vertical initial phase is 1/2 the scale factor)  On (Vertical initial phase is selected by the Even/Off Field Offset bit)	All All minimum more than					
	Value N 0b 1b Source_ The horiz is 3. The 4k bytes,	Disable Enable Width contal size of evalue programming from the evaluation of the ev	Description  Off (Vertical initial phase is 1/2 the scale factor)  On (Vertical initial phase is selected by the Even/Off Field Offset bit)  Project: All Format:  If the source image to be scaled in pixels. Max number of pixels is 2048; rammed is one less than the number of pixels. Source width can be no room a 64 byte alignment. The sprite width (actual width, not the width minuten values when YUV source pixel format is used.	All All minimum more than					
26:16 15:11 10:0	Value N  Ob  1b  Source_ The horizis 3. The 4k bytes, value) is	Disable Enable Width contal size of value progression to evalue to evalue de Projection de Projectio	Description  Off (Vertical initial phase is 1/2 the scale factor)  On (Vertical initial phase is selected by the Even/Off Field Offset bit)  Project: All Format:  If the source image to be scaled in pixels. Max number of pixels is 2048; rammed is one less than the number of pixels. Source width can be nor of a 64 byte alignment. The sprite width (actual width, not the width minuten values when YUV source pixel format is used.	All minimum more than					



#### 4.1.11.13 DVSBGAMC—Video Sprite B Gamma Correction Registers

**DVSBGAMC—Video Sprite B Gamma Correction Registers** 

**Register Type:** MMIO Address Offset: 73300h **Project:** 

00000000h; 04010040h; 08020080h; 0C0300C0h; 10040100h; 14050140h; 18060180h; 1C0701C0h; 20080200h; 24090240h; 280A0280h; 2C0B02C0h; 300C0300h; 340D0340h; 380E0380h; 3C0F03C0h; 00000400h; 00000400h; 00000400h; **Default Value:** 

R/W Access: Size (in bits): 19x32

See Video	Sprite A d	escription						
DWord Bit		Description						
0	31:0	GAMC0	Project:	All	Format:	DVSGAMC Reference Point		
1	31:0	GAMC1	Project:	All	Format:	DVSGAMC Reference Point		
2	31:0	GAMC2	Project:	All	Format:	DVSGAMC Reference Point		
3	31:0	GAMC3	Project:	All	Format:	DVSGAMC Reference Point		
4	31:0	GAMC4	Project:	All	Format:	DVSGAMC Reference Point		
5	31:0	GAMC5	Project:	All	Format:	DVSGAMC Reference Point		
6	31:0	GAMC6	Project:	All	Format:	DVSGAMC Reference Point		
7	31:0	GAMC7	Project:	All	Format:	DVSGAMC Reference Point		
8	31:0	GAMC8	Project:	All	Format:	DVSGAMC Reference Point		
9	31:0	GAMC9	Project:	All	Format:	DVSGAMC Reference Point		
10	31:0	GAMC10	Project:	All	Format:	DVSGAMC Reference Point		
11	31:0	GAMC11	Project:	All	Format:	DVSGAMC Reference Point		
12	31:0	GAMC12	Project:	All	Format:	DVSGAMC Reference Point		
13	31:0	GAMC13	Project:	All	Format:	DVSGAMC Reference Point		
14	31:0	GAMC14	Project:	All	Format:	DVSGAMC Reference Point		
15	31:0	GAMC15	Project:	All	Format:	DVSGAMC Reference Point		
16	31:0	GAMCmaxR	Project:	All	Format:	DVSGAMC Max Reference Point		
17	31:0	GAMCmaxG	Project:	All	Format:	DVSGAMC Max Reference Point		
18	31:0	GAMCmaxB	Project:	All	Format:	DVSGAMC Max Reference Point		