Intel Open Source Graphics Programmer's Reference Manual (PRM) for the 2013 Intel® Core™ Processor Family, including Intel HD Graphics, Intel Iris™ Graphics and Intel Iris Pro Graphics

Volume 2c: Command Reference: Registers (Haswell)

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Command Reference: Registers

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Execute Condition Code Register

EXCC - Execute Condition Code Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W,RO
Size (in bits):	32
Trusted Type:	1
Address:	02028h

This register contains user defined and hardware generated conditions that are used by MI_WAIT_FOR_EVENT commands. An MI_WAIT_FOR_EVENT instruction excludes the executing ring from arbitration if the selected event evaluates to a 1, while instruction is discarded if the condition evaluates to a 0. Once excluded a ring is enabled into arbitration when the selected condition evaluates to a 0.
This register also contains control for the invalidation of indirect state pointers on context restore.

DWord	Bit	Description
0	31:16	**Mask Bits** Format: Mask[15:0] These bits serves as a write enable for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.
	15:12	**Reserved** Project: HSW Format: MBZ
	11	**Pending Indirect State Dirty Bit** Project: HSW Access: RO This field keeps track of whether or not an indirect state pointer command has been parsed in the current context. Clears either on a context save or explicitly through a flush command. This bit is Read Only.
	10:7	**Pending Indirect State Counter** Project: HSW This field keeps track of the maximum number of indirect state pointers pending in the system. When the register is saved/restored, it saves either a value of 1 or 0. This field is Read-Only.

EXCC - Execute Condition Code Register		
	6:5	**Reserved** Format: MBZ
	4:0	**User Defined Condition Codes** The software may signal a Stream Semaphore by setting the Mask bit and Signal Bit together to match the bit field specified in a WAIT_FOR_EVENT (Semaphore).

Ring Buffer Tail

RING_BUFFER_TAIL - Ring Buffer Tail	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02030h
Name:	RCS Ring Buffer Tail
ShortName:	RCS_RING_BUFFER_TAIL
Address:	12030h
Name:	VCS Ring Buffer Tail
ShortName:	VCS_RING_BUFFER_TAIL
Address:	1A030h
Name:	VECS Ring Buffer Tail
ShortName:	VECS_RING_BUFFER_TAIL
Valid Projects:	[DevHSW+]
Address:	22030h
Name:	BCS Ring Buffer Tail
ShortName:	BCS_RING_BUFFER_TAIL

These registers are used to define and operate the "ring buffer" mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a linear memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information.

Refer to the Programming Interface chapter for a detailed description of the parameters specified in this ring buffer register set, restrictions on the placement of ring buffer memory, arbitration rules, and in how the ring buffer can be used to pass instructions.

Ring Buffer Tail Offsets must be properly programmed before ring is enabled. A Ring Buffer can be enabled when empty.

DWord	Bit	Description	
0	31:21	**Reserved**	
		Format:	MBZ
	20:3	**Tail Offset**	
		Format:	GraphicsAddress[20:3]

RING_BUFFER_TAIL - Ring Buffer Tail		
		This field is written by software to specify where the valid instructions placed in the ring buffer end. The value written points to the QWord past the last valid QWord of instructions. In other words, it can be defined as the next QWord that software will write instructions into. Software must write subsequent instructions to QWords following the Tail Offset, possibly wrapping around to the top of the buffer (i.e., software can't skip around within the buffer). Note that all DWords prior to the location indicated by the **Tail Offset** must contain valid instruction data - which may require instruction padding by software. See **Head Offset** for more information.
	2:0	**Reserved** Format: MBZ

Ring Buffer Head

RING_BUFFER_HEAD - Ring Buffer Head	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02034h
Name:	RCS Ring Buffer Head
ShortName:	RCS_RING_BUFFER_HEAD
Address:	12034h
Name:	VCS Ring Buffer Head
ShortName:	VCS_RING_BUFFER_HEAD
Address:	1A034h
Name:	VECS Ring Buffer Head
ShortName:	VECS_RING_BUFFER_HEAD
Valid Projects:	[DevHSW+]
Address:	22034h
Name:	BCS Ring Buffer Head
ShortName:	BCS_RING_BUFFER_HEAD

This register is used to define and operate the ring buffer mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a physical memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. Refer to the Programming Interface chapter for a detailed description of the parameters specified in this ring buffer register set, restrictions on the placement of ring buffer memory, arbitration rules, and in how the ring buffer can be used to pass instructions.

Ring Buffer Head Offsets must be properly programmed before ring is enabled. A Ring Buffer can be enabled when empty.

DWord	Bit	Description
0	31:21	**Wrap Count** Format: U11 count of ring buffer wraps This field is incremented by 1 whenever the **Head Offset** wraps from the end of the buffer back to the start (i.e., whenever it wraps back to 0). Appending this field to the **Head Offset** field effectively creates a virtual 4GB Head "Pointer" which can be used as a tag associated with instructions placed in a ring buffer. The Wrap Count itself will wrap to 0 upon overflow.

RING_BUFFER_HEAD - Ring Buffer Head

	20:2	**Head Offset** Format: GraphicsAddress[20:2] DWord Offset This field indicates the offset of the *next* instruction DWord to be parsed. Software will initialize this field to select the first DWord to be parsed once the RB is enabled. (Writing the Head Offset while the RB is enabled is UNDEFINED). Subsequently, the device will increment this offset as it executes instructions - until it reaches the QWord specified by the **Tail Offset**. At this point the ring buffer is considered "empty". **Programming Notes** A RB can be enabled empty or containing some number of valid instructions.
	1	**Reserved** Format: MBZ
	0	**Reserved** Project: HSW Source: BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS Exists If: //BCS, VCS, VCS2, VECS Format: MBZ
	0	**Wait for Condition Indicator** Project: HSW Source: RenderCS Exists If: //RCS This is a read only value used to indicate whether or not the command streamer is currently waiting for a conditional code to be cleared from 0x2028

Ring Buffer Start

RING_BUFFER_START - Ring Buffer Start	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02038h
Name:	RCS Ring Buffer Start
ShortName:	RCS_RING_BUFFER_START
Address:	12038h
Name:	VCS Ring Buffer Start
ShortName:	VCS_RING_BUFFER_START
Address:	1A038h
Name:	VECS Ring Buffer Start
ShortName:	VECS_RING_BUFFER_START
Valid Projects:	[DevHSW+]
Address:	22038h
Name:	BCS Ring Buffer Start
ShortName:	BCS_RING_BUFFER_START

These registers are used to define and operate the "ring buffer" mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a physical memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. Refer to the Programming Interface chapter for a detailed description of the parameters specified in this ring buffer register set, restrictions on the placement of ring buffer memory, arbitration rules, and in how the ring buffer can be used to pass instructions.

DWord	Bit	Description
0	31:12	**Starting Address** Format: GraphicsAddress[31:12]RingBuffer This field specifies Bits 31:12 of the 4KB-aligned starting Graphics Address of the ring buffer. Address bits 31 down to 29 must be zero. All ring buffer pages must map to Main Memory (uncached) pages. Ring Buffer addresses are always translated through the global GTT.
	11:0	**Reserved** Format: MBZ

Ring Buffer Control

RING_BUFFER_CTL - Ring Buffer Control	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0203Ch
Name:	RCS Ring Buffer Control
ShortName:	RCS_RING_BUFFER_CTL
Address:	1203Ch
Name:	VCS Ring Buffer Control
ShortName:	VCS_RING_BUFFER_CTL
Address:	1A03Ch
Name:	VECS Ring Buffer Control
ShortName:	VECS_RING_BUFFER_CTL
Valid Projects:	[DevHSW+]
Address:	2203Ch
Name:	BCS Ring Buffer Control
ShortName:	BCS_RING_BUFFER_CTL

Description	Project
These registers are used to define and operate the ring buffer mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a physical memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. Refer to the Programming Interface chapter for a detailed description of the parameters specified in this ring buffer register set, restrictions on the placement of ring buffer memory, arbitration rules, and in how the ring buffer can be used to pass instructions.	
Ring Buffer Head and Tail Offsets must be properly programmed before it is enabled. A Ring Buffer can be enabled when empty.	
Graphics Engine doesn't go IDLE when head offset is not equal to tail offset when ring buffer is disabled. PSMI controller waits for HW to go Idle as part of the PSMI flow. When PSMI flow happens in middle of ring buffer initialization where in Head offset is not equal to Tail offset and Ring Buffer disabled, PMSI flow will hang waiting for Graphics Engine to go IDLE. (During ring buffer initialization SW programs Head and Tail offsets prior to enabling Ring Buffer). In order to avoid this dead lock PSMI controller must detect this case and program head and tail offset to be equal to allow Graphics	HSW

RING_BUFFER_CTL - Ring Buffer Control

Engine to go IDLE, before exiting PSMI flow original head and tail offsets should be restored.	

DWord	Bit	Description
0	31:21	**Reserved** Format: MBZ
	20:12	**Buffer Length** Format: U9-1 in 4 KB pages - 1 This field is written by SW to specify the length of the ring buffer in 4 KB Pages.Range = [0 = 1 page = 4 KB, 1FFh = 512 pages = 2 MB] Value / Name / Description: 0 / / 1 page = 4 KB 1FFh / / 512 pages = 2 MB
	11	**RBWait** Description / Project: Indicates that this ring has executed a WAIT_FOR_EVENT instruction and is currently waiting. Software can write a "1" to clear this bit, write of "0" has no effect. When the RB is waiting for an event and this bit is cleared, the wait will be terminated and the RB will be returned to arbitration. / RenderCS: RBWait is not set on executing WAIIT_FOR_EVENT instruction waiting on Async Flip Pending. / HSW
	10	**Semaphore Wait** Description / Project: Indicates that this ring has executed a MI_SEMAPHORE_MBOX instruction with register compare and is currently waiting. / HSW
	9	**Reserved** Format: MBZ
	8	**Reserved** Project: HSW Format: MBZ
	7:3	**Reserved** Format: MBZ
	2:1	**Automatic Report Head Pointer** Project: HSW Source: RenderCS Exists If: //RCS This field is written by software to control the automatic "reporting" (write) of this ring buffer's "Head Pointer" register (register DWord 1) to the corresponding location within the Hardware Status Page. Automatic reporting can either be disabled or enabled at 4KB, 64KB or 128KB

RING_BUFFER_CTL - Ring Buffer Control

boundaries within the ring buffer.

Value	Name	Description
0h	MI_AUTOREPORT_OFF	Automatic reporting disabled
1h	MI_AUTOREPORT_64KBMI_AUTOREPORT_4KB	Report every 16 pages (64KB) when the Per-Process Virtual Address Space bit is set, the ring buffer reports every 4KB.
2h	Reserved	
3h	MI_AUTOREPORT_128KB	Report every 32 pages (128KB)

Programming Notes
When the Per-Process Virtual Address Space bit is set and automatic head reporting is desired, this field must be set to option 1 since the ring buffer will be only 16KB in size. The head pointer will be reported to the head pointer location in the Per-Process Hardware Status Page when it passes each 4KB page boundary. When the above-mentioned bit is reset, reporting will behave just as on the prior devices (as documented above), and option 1 will report on 64KB boundary.

2:1 **Automatic Report Head Pointer**

Source:	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS
Exists If:	//BCS, VCS, VCS2, VECS

Description	Project
This field is written by software to control the automatic "reporting" (write) of this ring buffer's "Head Pointer" register (register DWord 1) to the corresponding location within the Hardware Status Page. Automatic reporting can either be disabled or enabled at 4KB, 64KB or 128KB boundaries within the ring buffer.	
When the **Per-Process Virtual Address Space** bit is set and automatic head reporting is desired, this field must be set to option 2 since the ring buffer will be only 16KB in size. The head pointer will be reported to the head pointer location in the Per-Process Hardware Status Page when it passes each 4KB page boundary. When the above-mentioned bit is set, reporting will behave just as on the prior devices (as documented above), and option 2 is not legal.	HSW

Value	Name	Description
0	MI_AUTOREPORT_OFF	Automatic reporting disabled
1	MI_AUTOREPORT_64KB	Report every 16 pages (64KB)
2	MI_AUTOREPORT_4KB	Report every page (4KB) This mode must not be enabled in Ring Buffer mode of scheduling to minimize the auto reports.
3	MI_AUTOREPORT_128KB	Report every 32 pages (128KB)

0 **Ring Buffer Enable**

RING_BUFFER_CTL - Ring Buffer Control

Format:	Enable

This field is used to enable or disable this ring buffer. It can be enabled or disabled regardless of whether there are valid instructions pending. If disabled and the ring head equals ring tail, all state currently loaded in hardware is considered invalid.

Programming Notes	Project
Ring Buffer Mode of Scheduling: SW must follow the below programming notes during SW initialization phase or while enabling render engine's ring buffer for the first time, this would be coming out of boot, standby, hibernate or reset. This flow must be also followed during ring replay when ring buffer is disabled and enabled during debug. • SW must set the Force Wakeup bit to prevent GT from entering C6. • SW must dispatch workload (dummy context) to initialize render engine with default state such that any context switches that occur subsequently (Power Save) will save and restore coherent device state. Indirect pointers used in 3D states must point to valid graphics surface existing in memory. PP_DCLV followed by PP_DIR_BASE register should be programmed as part of initialization workload if PPGTT is enabled in GFX_MODE register. • SW must ensure all the register (MMIO) initialization/programming through CPU happens in this block or latter, this ensures the MMIO state is save/restored on subsequent context switches (Power Sequences). • Once the render engine is programmed with valid state and the configuration, Force Wakeup bit should be reset to enable C6 entry.	HSW

Render/Video Semaphore Sync Register

RVSYNC - Render/Video Semaphore Sync Register	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	02040h
This register is written by VCS, read by CS.	

DWord	Bit	Description
0	31:0	**Semaphore Data** Semaphore data for synchronization between render engine and blitter engine.

Render/Blitter Semaphore Sync Register

RBSYNC - Render/Blitter Semaphore Sync Register		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	02044h	
This register is written by BCS, read by CS.		
DWord	**Bit**	**Description**
0	31:0	**Semaphore Data** Semaphore data for synchronization between render engine and blitter engine.

Render/Video Enhancement Semaphore Sync Register

RVESYNC - Render/Video Enhancement Semaphore Sync Register		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	02048h	
This register is written by VECS, read by CS.		
DWord	**Bit**	**Description**
0	31:0	**Semaphore Data** Semaphore data for synchronization between render engine and video enhancement engine.

NOP Identification Register

NOPID - NOP Identification Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Size (in bits):	32
Trusted Type:	1
Address:	02094h

Description	Project
Access: RW	HSW
The NOPID register contains the Noop Identification value specified by the last MI_NOOP instruction that enabled this register to be updated.	

DWord	Bit	Description
0	31:22	**Reserved** Format: MBZ
	21:0	**Reserved**

Hardware Status Mask Register

HWSTAM - Hardware Status Mask Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0xFFFFFFFF
Access:	R/W,RO
Size (in bits):	32
Trusted Type:	1
Address:	02098h

The HWSTAM register has the same format as the Interrupt Control Registers. The bits in this register are mask bits that prevent the corresponding bits in the Interrupt Status Register from generating a Hardware Status Write (PCI write cycle). Any unmasked interrupt bit (HWSTAM bit set to 0) will allow the Interrupt Status Register to be written to the ISR location (within the memory page specified by the Hardware Status Page Address Register) when that Interrupt Status Register bit changes state.

Programming Notes

- To write the interrupt to the HWSP, the corresponding IMR bit must also be clear (enabled).
- At most 1 bit can be unmasked at any given time.

DWord	Bit	Description
0	31:0	**Hardware Status Mask Register** Default Value: FFFFFFFFh Format: Array of Masks Refer to the Interrupt Control Register section for bit definitions. Reserved bits are RO.

Render Mode Register for Software Interface

MI_MODE - Render Mode Register for Software Interface

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0209Ch

The MI_MODE register contains information that controls software interface aspects of the Memory Interface function.

DWord	Bit	Description
0	31:16	**Masks** Format: Mask[15:0] A 1 in a bit in this field allows the modification of the corresponding bit in Bits 15:0
	15	**Suspend Flush** Format: U1 **Value / Name / Description** 0h / No Delay **[Default]** / HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well 1h / Delay Flush / Suspend flush is active **Programming Notes** This should only be written to from the ring using MI_SUSPEND_FLUSH. It is considered undefined if written by software through MMIO
	14	**Async Flip Performance mode** Project: HSW Format: U1 **Value / Name / Description** 0h / Performance mode enabled **[Default]** / The stall of the flip event is in the windower 1h / Performance mode disabled / The stall of the flip event is in the command stream

MI_MODE - Render Mode Register for Software Interface

Programming Notes	Project
This bit must be set to '1' on all projects disabling Async Flip Performance mode.	HSW
When Async Flip Performance mode is enabled stall is in the Windower allowing the commands following the MI_WAIT_FOR_EVENT to be parsed by command streamer, this breaks the usage model of controlling the display message generation in display engine using MI_LOAD_REGISTER_IMMEDIATE commands from ring buffer.	

13 **Flush Performance mode**

Project:	HSW
Format:	U1

Value	Name	Description
0h	run fast restore **[Default]**	No NonPipelined SV flush.
1h	run slow legacy restore	With NonPipelined SV flush.

12 **Reserved**

Project:	DevHSW+
Format:	MBZ

11 **Invalidate UHPTR enable**

Format:	Enable

If bit set H/W clears the valid bit of UHPTR (2134h, bit 0) when current active head pointer is equal to UHPTR.

10 **Reserved**

Project:	HSW
Format:	MBZ

9 **Rings Idle**

Format:	U1

Read Only Status bit

Value	Name	Description
0h	Not Idle **[Default]**	Parser not Idle or Ring Arbiter not Idle.
1h	Idle	Parser Idle and Ring Arbiter Idle.

Programming Notes
Writes to this bit are not allowed.

8 **Stop Rings**

Format:	U1

Value	Name	Description

0h	**[Default]**	Normal Operation.
1h		Parser is turned off and Ring arbitration is turned off.

Programming Notes
Software must set this bit to force the Rings and Command Parser to Idle. Software must read a 1 in the Ring Idle bit after setting this bit to ensure that the hardware is idle.
Software must clear this bit for Rings to resume normal operation.

7

Reserved

Project:	HSW
Format:	MBZ

6

Vertex Shader Timer Dispatch Enable

Project:	HSW
Format:	Enable

Value	Name	Description
0h	Disable **[Default]**	Disable the timer for dispatch of single vertices from the vertex shader. Vertex shader will try to collect 2 vertices before a dispatch
1h	Enable	Enable the timer for dispatch of single vertices. Dispatch a single vertex shader thread after the timer expires.

5

Reserved

Format:	MBZ

4

Reserved

Project:	HSW
Format:	MBZ

3:1

Reserved

Project:	HSW
Format:	MBZ

0

Mask IIR disable

Format:	Disable

Mask IIR disable. Nominally the Interrupt controller masks interrupts in the IIR register if an interrupt acknowledge from the 3gio interface is pending. Setting this bit to a 1 allows interrupts to be visible to the interrupt controller while an interrupt acknowledge is pending.

Thread Mode Register

FF_MODE - Thread Mode Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000 [NOVALIDPROJECTS] 0x00A01010 [NOVALIDPROJECTS] 0x28A00000 [NOVALIDPROJECTS] 0x28A01010 [HSW]
Access:	R/W
Size (in bits):	32

Address: 020A0h

This register is used to program the FF shader Mode.

DWord	Bit	Description
0	31	**Reserved** Project: HSW Format: MBZ
	30	**Reserved** Project: HSW Format: MBZ
	29:26	**DS Hit Max Value** Format: U4 Description / Project: If the number of hits reaches the DS Hit Max Value and there is a pending miss to be dispatched, the DS will dispatch the pending miss vertex as a single dispatch. / Programming the value beyond the range will have undefined behavior. / HSW Value / Name / Project: 10 / **[Default]** / HSW [1,11] / / HSW
	25:20	**VS Hit Max Value** Format: U6 Description / Project:

	If the number of hits reaches the VS Hit Max Value and there is a pending miss to be dispatched, the VS will dispatch the pending miss vertex as a single dispatch.	
	Programming the value beyond the range will have undefined behavior.	HSW

Value	Name	Project
10	**[Default]**	
[1,26]		HSW

19 **DS Reference Count Full Force Miss Enable**

Project:	HSW
Format:	Enable

Value	Name	Description
0b	**[Default]**	On a hit to the DS cache and the associated handle's reference count is full then stall until a derefernce.
1b		On a hit to the DS cache and the associated handle's reference count is full then force the cycle as a miss and allocate a new handle.

Programming Notes	Project
This must be enabled to improve performance of domain point thru put in DS	HSW

18:16 **Reserved**

Project:	DevHSW+
Format:	MBZ

15 **VS Reference Count Full Force Miss Enable**

Project:	HSW
Format:	U1

Value	Name	Description
[0,1]		
0b	**[Default]**	On a hit to the VS cache and the associated handle's reference count is full then stall until a derefernce.
1b		On a hit to the VS cache and the associated handle's reference count is full then force the cycle as a miss and allocate a new handle.

Programming Notes	Project
The VS Reference Count Full Force Miss Enable must remain at the default value of 0.	HSW

14:13 **Reserved**

Project:	DevHSW+
Format:	MBZ

FF_MODE - Thread Mode Register

	12	**Reserved** Default Value: 1h Project: DevHSW+ Format: Must Be One
	11:7	**Reserved** Format: MBZ
	6:5	**Reserved** Project: DevHSW+ Format: MBZ
	4	**Reserved** Default Value: 1h Project: DevHSW+ Format: Must Be One
	3:0	**Reserved** Format: MBZ

Interrupt Mask Register

IMR - Interrupt Mask Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0xFFFFFFFF
Access:	R/W,RO
Size (in bits):	32
Address:	020A8h

The IMR register is used by software to control which Interrupt Status Register bits are masked or unmasked. Unmasked bits will be reported in the IIR, possibly triggering a CPU interrupt, and will persist in the IIR until cleared by software. Masked bits will not be reported in the IIR and therefore cannot generate CPU interrupts.

DWord	Bit	Description
0	31:0	**Interrupt Mask Bits** Format: InterruptMask[32] Refer to the Interrupt Control Register section for bit definitions. This field contains a bit mask which selects which interrupt bits (from the ISR) are reported in the IIR. Reserved bits in the Interrupt Control Register are RO.

Value	Name	Description
FFFF FFFFh	**[Default]**	
0h	Not Masked	Will be reported in the IIR
1h	Masked	Will not be reported in the IIR

Error Identity Register

EIR - Error Identity Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W,RO
Size (in bits):	32
Address:	020B0h

The EIR register contains the persistent values of Hardware-Detected Error Condition bits. Any bit set in this register will cause the Master Error bit in the ISR to be set. The EIR register is also used by software to clear detected errors (by writing a 1 to the appropriate bit(s)), except for the unrecoverable bits described.)

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Error Identity Bits** Format: Array of Error condition bits See the table titled Hardware-Detected Error Bits. This register contains the persistent values of ESR error status bits that are unmasked via the EMR register. (See Table Table 3-3. Hardware-Detected Error Bits). The logical OR of all (defined) bits in this register is reported in the Master Error bit of the Interrupt Status Register. In order to clear an error condition, software must first clear the error by writing a 1 to the appropriate bit(s) in this field. If required, software should then proceed to clear the Master Error bit of the IIR. Reserved bits are RO. **Value** / **Name** 1h — Error occurred **Programming Notes** Writing a 1 to a set bit will cause that error condition to be cleared. However, neither the Page Table Error bit (Bit 4) nor the Instruction Error bit (Bit 0) can be cleared except by reset (i.e., it is a fatal error).

Error Mask Register

EMR - Error Mask Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x000000FF
Access:	R/W,RO
Size (in bits):	32
Address:	020B4h

The EMR register is used by software to control which Error Status Register bits are masked or unmasked. Unmasked bits will be reported in the EIR, thus setting the Master Error ISR bit and possibly triggering a CPU interrupt, and will persist in the EIR until cleared by software. Masked bits will not be reported in the EIR and therefore cannot generate Master Error conditions or CPU interrupts. Reserved bits are RO.

DWord	Bit	Description
0	31:8	**Reserved** Format: Must Be One **Programming Notes** These bits are not implemented in HW and must be set to '1'
	7:0	**Error Mask Bits** Format: Array of error condition mask bits See the table titled Hardware-Detected Error Bits. This register contains a bit mask that selects which error condition bits (from the ESR) are reported in the EIR.

Value	Name	Description
FFh	**[Default]**	
0h	Not Masked	Will be reported in the EIR
1h	Masked	Will not be reported in the EIR

Error Status Register

ESR - Error Status Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	020B8h

The ESR register contains the current values of all Hardware-Detected Error condition bits (these are all by definition persistent). The EMR register selects which of these error conditions are reported in the persistent EIR (i.e., set bits must be cleared by software) and thereby causing a Master Error interrupt condition to be reported in the ISR.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Error Status Bits** Format: Array of error condition bits See the table titled Hardware-Detected Error Bits. This register contains the non-persistent values of all hardware-detected error condition bits. Value: 1h — Name: Error Condition Detected

Instruction Parser Mode Register

INSTPM - Instruction Parser Mode Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000 [NOVALIDPROJECTS] 0x00006000 [NOVALIDPROJECTS] 0x00006080 [HSW]
Access:	R/W,RO
Size (in bits):	32
Trusted Type:	1

Address: 020C0h

The INSTPM register is used to control the operation of the Instruction Parser. Certain classes of instructions can be disabled (ignored) - often useful for detecting performance bottlenecks. Also, Synchronizing Flush operations can be initiated - useful for ensuring the completion (vs. only parsing) of rendering instructions.

Programming Notes

- If an instruction type is disabled, the parser will read those instructions but not process them.
- Error checking will be performed even if the instruction is ignored.
- All Reserved bits are implemented.
- This Register is saved and restored as part of Context.

DWord	Bit	Description
0	31:16	**Mask Bits** Format: Mask[15:0] Masks: These bits serve as write enables for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.
	15	**Reserved** Project: HSW Access: RO Format: MBZ

INSTPM - Instruction Parser Mode Register

14:13 Predicate Enable

Project:	HSW

This field sets the Predicate Enable status in render command streamer when parsed.

Value	Name	Description	Project
0h	Predicate Always	Following Commands will be NOOPED by RCS/RS unconditionally.	HSW
1h	Predicate Reset	Following Commands will be NOOPED by RCS/RS only if the MI_PREDICATE_STATUS_2 is clear.	HSW
2h	Predicate Set	Following Commands will be NOOPED by RCS/RS only if the MI_PREDICATE_STATUS_2 is set.	HSW
3h	Predicate Disable **[Default]**	Predication is Disabled and RCS/RS will process commands as usual.	HSW

Programming Notes
SW must use MI_SET_PREDICATE instead of MMIO access.

12 Reserved

Project:	HSW

11 CLFLUSH Toggle

Project:	HSW
Access:	RO
Format:	U1

This bit changes polarity each time the MI_CLFLUSH command completes. This bit is Read Only.

10 Reserved

Project:	HSW
Format:	MBZ

9 TLB Invalidate

Project:	HSW
Format:	U1

If set, this bit allows the command stream engine to invalidate the 3D render TLBs. This bit is valid only with the Sync flush enable. Note: GFX soft resets do not invalidate TLBs, it is up to GFX driver to explicitly invalidate TLBs post reset.

8 Memory Sync Enable

Project:	HSW
Format:	U1

If set, this bit allows the command stream engine to write out the data from the local caches to memory. This bit is valid only with the Sync flush enable

INSTPM - Instruction Parser Mode Register

	7	**Force Sync Command Ordering** Default Value: 1b Project: HSW Format: Enable By default, driver/OS synchronization commands (MI_STORE_DATA_IMM, for instance) can execute out of order with respect to 3D state and 3D primitive commands. When set, this bit forces ordering of these commands. See section 3.2.2 for a list of these commands.
	6	**CONSTANT_BUFFER Address Offset Disable** Project: HSW Format: Disable When this bit is clear, the 3DSTATE_CONSTANT_* Buffers' Starting Address is used as a DynamicStateOffset. That is, it serves as an offset from the Dynamic State Base Address. Accesses will be subject to Dynamic State bounds checking. When this bit is set, the 3DSTATE_CONSTANT_* Buffers' Starting Address is used as a true GraphicsAddress (not an offset). No bounds checking will be performed during access.
	5	**Sync Flush Enable** Project: HSW Format: U1 This field is used to request a Sync Flush operation. The device will automatically clear this bit before completing the operation. See Sync Flush (Programming Environment). **Programming Notes** • The command parser must be stopped prior to issuing this command by setting the Stop Rings bit in register MI_MODE. Only after observing Rings Idle set in MI_MODE can a Sync Flush be issued by setting this bit. Once this bit becomes clear again, indicating flush complete, the command parser is re-enabled by clearing Stop Rings.
	4	**Reserved** Project: HSW
	3	**Media Instruction Disable** Project: HSW Format: U1 This bit instructs the Renderer instruction parser to parse and error-check Media instructions, but not execute them. Format = Disable
	2	**3D Rendering Instruction Disable** Project: HSW Format: U1 This bit instructs the Renderer instruction parser to parse and error-check 3D Rendering

		instructions, but not execute them. This bit must always be set by software if 3D State Instruction Disable is set. Setting this bit without setting 3D State Instruction Disable is allowed. Format = Disable
	1	**3D State Instruction Disable** Project: HSW Format: Disable
	0	**Texture Palette Load Instruction Disable** Project: HSW Format: U1 This bit instructs the Renderer instruction parser to parse and error-check Texture Palette Load instructions, but not execute them. Format = Disable

Control Register for Power Management

WAIT_FOR_RC6_EXIT - Control Register for Power Management

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	020CCh

DWord	Bit	Description
0 This register gets power context save/restored. Bit[0] contents of this register doesn't get save/restored.	31:16	**Mask Bits** Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:14	**Reserved** Format: MBZ
	13:9	**Reserved** Project: HSW Format: MBZ
	8	**Render Inhibit** Format: Disable **Value / Name / Description** 0h / Disabled **[Default]** / When not Set CS doesn't take any special action. 1h / Enabled / When Set CS will not save/restore render context as part of power context save/restore. Render context includes RS context as well if enabled. **Programming Notes** If this bit is set S/W should set Resource Streamer Context Enable (Bit[7] of this register)as well.
	7	**Resource Streamer Context Enable**

WAIT_FOR_RC6_EXIT - Control Register for Power Management

		Format: Enable

Value	Name	Description
1h	Disable	The current context does not include the resource streamer context
0h	Enable **[Default]**	The current context does include the resource streamer context.

6:4	**Reserved** Project: HSW
3:2	**Selective Read Addressing** Project: HSW This field controls the outbound read request originating from Render Command Streamer. Programming this field selects the read return value from the unit in given slice and half slice.

Value	Name
00b	Upper Left Half-slice only **[Default]**
01b	Upper Right Half-slice only
10b	Lower Left Half-slice only
11b	Lower Right Half-slice only

1	**Reserved** Format: MBZ
0	**WAIT FOR RC6 EXIT** Format: Disable

Value	Name	Description
0h	Disabled **[Default]**	When not Set CS doesn't take any action.
1h	Enabled	When Set CS will stop on the next appropriate command boundary and will initiate IDLE sequence with PM.

Programming Notes
WAIT_FOR_RC6_EXIT functionality is only supported in ring buffer mode of scheduling and not supported in execlist mode of scheduling.

RCS Batch Buffer State Register

RCS_BB_STATE - RCS Batch Buffer State Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000 [HSW]
Access:	RO
Size (in bits):	32
Address:	02110h

This register contains the attributes of the current batch buffer initiated from the Ring Buffer.

This register should not be written by software. These fields should only get written by a context restore. Software should always set these fields via the MI_BATCH_BUFFER_START command when initiating a batch buffer.
This register is saved and restored with context.

DWord	Bit	Description
0	31:9	**Reserved** Format: MBZ
	8	**Reserved** Project: DevHSW:GT3:A Format: MBZ
	8	**Non-Privileged** Project: DevHSW, EXCLUDE(DevHSW:GT3:A) Format: U1 If set, this batch buffer is non-privileged and cannot execute privileged commands. If clear, this batch buffer is privileged and will execute privileged commands. Note: This field reflects the effective privilege level and may not be the same as the Non-Privileged Indicator written using MI_BATCH_BUFFER_START. **Value** / **Name** / **Description** 0h / Privileged **[Default]** / Batch Buffer is Privileged. 1h / Non-Privileged / Batch Buffer is Non-Privileged.
	7	**Resource Streamer Enable** Project: DevHSW+ Format: U1 When this bit is set, the Resource Streamer will execute the batch buffer. When this bit is clear the Resource Streamer will not execute the batch buffer.

RCS_BB_STATE - RCS Batch Buffer State Register

	6	**Reserved**
	5	**Address Space Indicator** Project: HSW Value / Name / Description 0h / GGTT **[Default]** / This batch buffer is located in GGTT memory 1h / PPGTT / This batch buffer is located in PPGTT memory.
	4	**Reserved** Project: DevHSW+, EXCLUDE(DevHSW:GT3:A), EXCLUDE(DevHSW:GT3:B) Format: MBZ
	4	**Reserved** Project: Pre-DevHSW, DevHSW:GT3:A, DevHSW:GT3:B
	3:0	**Reserved** Format: MBZ

Second Level Batch Buffer Head Pointer Register

SBB_ADDR - Second Level Batch Buffer Head Pointer Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	CommandStreamer
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	02114h
Name:	RCS Second Level Batch Buffer Head Pointer Register
ShortName:	RCS_SBB_ADDR
Valid Projects:	[HSW+]

This register contains the current DWord Graphics Memory Address of the last-initiated batch buffer.

Programming Notes

This register should NEVER be programmed by driver, this is for HW internal use only. This register should not be written by software. These fields should only get written by a context restore. Software should always set these fields via the MI_BATCH_BUFFER_START command when initiating a batch buffer.
This register is saved and restored with context.

DWord	Bit	Description
0	31:2	**Second Level Batch Buffer Head Pointer** Format: GraphicsAddress[31:2] This field specifies the DWord-aligned Graphics Memory Address where the last initiated Second Level Batch Buffer is currently fetching commands. This field is meaningful only when Valid field is set to "1".
	1	**Reserved** Format: MBZ
	0	**Valid** Format: U1

Value	Name	Description	Project
0h	Invalid **[Default]**	Second Level Batch buffer Invalid	DevHSW+
1h	Valid	Second Batch buffer Valid	DevHSW+

Second Level Batch Buffer State Register

SBB_STATE - Second Level Batch Buffer State Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000 [HSW]
Access:	R/W
Size (in bits):	32
Address:	02118h

This register contains the attributes of the second level batch buffer initiated from the batch Buffer.

This register should not be written by software. These fields should only get written by a context restore. Software should always set these fields via the MI_BATCH_BUFFER_START command when initiating a batch buffer.
This register is saved and restored with context.

DWord	Bit	Description
0	31:9	**Reserved** Format: MBZ
	8	**Reserved** Project: DevHSW:GT3:A Format: MBZ
	8	**Non-Privileged** Format: DevHSW,EXCLUDE(DevHSW:GT3:A) If set, this second level batch buffer is non-privileged and cannot execute privileged commands. If clear, this second level batch buffer is privileged and will execute privileged commands. Note: This field reflects the effective privilege level and may not be the same as the Non-Privileged written using MI_BATCH_BUFFER_START. **Value** / **Name** / **Description** 0h / Privileged **[Default]** / Second level Batch Buffer is Privileged. 1h / Non-Privileged / Second level Batch Buffer is Non-Privileged.
	7	**Resource Streamer Enable** Format: U1 When this bit is set, the Resource Streamer will execute the batch buffer. When this bit is clear the Resource Streamer will not execute the batch buffer.
	6	**Reserved** Project: HSW

SBB_STATE - Second Level Batch Buffer State Register

	5	**Address Space Indicator** Project: HSW Format: MI_BufferSecurityType If set, this second level batch buffer is non-secure and cannot execute privileged commands nor access privileged (GGTT) memory. It will be accessed via the PPGTT. If clear, this batch buffer is secure and will be accessed via the GGTT.DevHSW+ When Per-Process GTT Enable is set, it is assumed that all code is in a secure environment, independent of address space. Under this condition, this bit only specifies the address space (GGTT or PPGTT). All commands are executed "as-is"

Value	Name	Description	Project
0h	MIBUFFER_SECURE **[Default]**	Located in GGTT memory	DevHSW+
1h	MIBUFFER_NONSECURE	Located in PPGTT memory	DevHSW+

	4	**Reserved** Project: DevHSW+, EXCLUDE(DevHSW:GT3:A), EXCLUDE(DevHSW:GT3:B) Format: MBZ
	4	**Reserved** Project: DevHSW:GT3:A, DevHSW:GT3:B
	3:0	**Reserved** Format: MBZ

Mode Register for GAFS

GAFS_MODE - Mode Register for GAFS

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	0212Ch

DWord	Bit	Description
0	31:16	**Mask Bits** Format: Mask[15:0] Masks: These bits serve as write enables for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.
	15:11	**Reserved** Format: MBZ
	10	**Reserved** Project: HSW
	9	**Reserved**
	8:2	**Reserved** Format: MBZ
	1:0	**Reserved** Project: DevHSW+ Format: MBZ

Pending Head Pointer Register

UHPTR - Pending Head Pointer Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02134h
Name:	RCS Pending Head Pointer Register
ShortName:	RCS_UHPTR
Address:	12134h
Name:	VCS Pending Head Pointer Register
ShortName:	VCS_UHPTR
Address:	1A134h
Name:	VECS Pending Head Pointer Register
ShortName:	VECS_UHPTR
Valid Projects:	[DevHSW+]
Address:	22134h
Name:	BCS Pending Head Pointer Register
ShortName:	BCS_UHPTR

Programming Notes

Once SW uses UHPTR to preempt the existing workload, should explicitly program MI_SET_CONTEXT to save the preempted context status before submitting the new workload. In case SW doesn't want to save the state of the preempted context, it should at the minimum program RS_PREEMPT_STATUS to 0x0 so that the register status doesn't interfere with the new workloads.

DWord	Bit	Description
0	31:3	**Head Pointer Address** Format: GraphicsAddress[31:3] **Description** / **Project** This register represents the GFX address offset where execution should continue in the ring buffer following execution of an MI_ARB_CHECK command. / HSW
	2:1	**Reserved** Format: MBZ

UHPTR - Pending Head Pointer Register

	0	**Head Pointer Valid** **Description** / **Project** This bit is set by the software to request a pre-emption. / It is reset by hardware when an MI_ARB_CHECK command is parsed by the command streamer. The hardware uses the head pointer programmed in this register at the time the reset is generated. / HSW **Value** / **Name** / **Description** 0 / InValid / No valid updated head pointer register, resume execution at the current location in the ring buffer 1 / Valid / Indicates that there is an updated head pointer programmed in this register

Second Level Batch Buffer Head Pointer Preemption Register

SBB_PREEMPT_ADDR - Second Level Batch Buffer Head Pointer Preemption Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1

Address:	0213Ch
Name:	RCS Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	RCS_SBB_PREEMPT_ADDR

Description	Project
This register gets updated with the DWord-aligned graphics memory address of the PREEMPTABLE command in the second level batch buffer on which preemption has occurred. This register value should be looked at only when the preemption has occurred in the second level batch buffer. This is indicated by "Ring/Batch Indicator" in "RING_BUFFER_HEAD_PREEMPT_REG". This register value retains its previous value and doesn't change when the preemption occurs on a preemptable command in ring buffer or in batch buffer. Preemption is triggered by valid UHPTR in ring buffer mode of scheduling and by a pending execlist in Exec-List mode of scheduling. This is a global register and context save/restored as part of power context image.	
Preemptable Commands / **Project** / **Source** MI_ARB_CHECK / HSW / RenderCS	HSW

Programming Notes
Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:2	**Second Level Batch Buffer Head Pointer** Format: GraphicsAddress[31:2] This field specifies the DWord-aligned Graphics Memory Address of the PREEMPTABLE command in a batch buffer where the Preemption has occurred.
	1:0	**Reserved** Format: MBZ

Batch Buffer Head Pointer Register

BB_ADDR - Batch Buffer Head Pointer Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	02140h
Name:	RCS Batch Buffer Head Pointer Register
ShortName:	RCS_BB_ADDR
Address:	12140h
Name:	VCS Batch Buffer Head Pointer Register
ShortName:	VCS_BB_ADDR
Valid Projects:	HSW
Address:	1A140h
Name:	VECS Batch Buffer Head Pointer Register
ShortName:	VECS_BB_ADDR
Address:	22140h
Name:	BCS Batch Buffer Head Pointer Register
ShortName:	BCS_BB_ADDR

This register contains the current DWord Graphics Memory Address of the last-initiated batch buffer.

Programming Notes

Programming Restriction: This register should NEVER be programmed by driver. This is for HW internal use only.

DWord	Bit	Description
0	31:2	**Batch Buffer Head Pointer** Project: DevHSW+ Format: GraphicsAddress[31:2] This field specifies the DWord-aligned Graphics Memory Address where the last initiated Batch Buffer is currently fetching commands. If no batch buffer is currently active, the Valid bit will be 0 and this field will be meaningless.
	1	**Reserved**

BB_ADDR - Batch Buffer Head Pointer Register

		Format: MBZ
	0	**Valid** Format: U1 **Value** / **Name** / **Description** 0h / Invalid **[Default]** / Batch buffer Invalid 1h / Valid / Batch buffer Valid

Batch Buffer Head Pointer Preemption Register

BB_PREEMPT_ADDR - Batch Buffer Head Pointer Preemption Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02148h
Name:	RCS Batch Buffer Head Pointer Preemption Register
ShortName:	RCS_BB_PREEMPT_ADDR

Description	Project
This register gets updated with the DWord-aligned graphics memory address of the PREEMPTABLE command in the batch buffer on which preemption has occurred. This register gets updated with the DWord-aligned graphics memory address of the command following the MI_BATCH_START corresponding to the second level batch buffer, when the preemption has occurred in the second level batch buffer. This register value should be looked at only when the preemption has occurred in the batch buffer. This is indicated by "Ring/Batch Indicator" in "RING_BUFFER_HEAD_PREEMPT_REG". This register value retains its previous value and doesn't change when the preemption occurs on a preemptable command in ring buffer. Preemption is triggered by valid UHPTR in ring buffer mode of scheduling and by a pending execlist in Exec-List mode of scheduling. Note that this register is only for debug mode in ExecList mode of scheduling. This is a global register and context save/restored as part of power context image.	
Preemptable Commands / **Project** / **Source**: MI_ARB_CHECK / HSW / RenderCS	HSW

Programming Notes
Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:2	**Batch Buffer Head Pointer** Format: GraphicsAddress[31:2] This field specifies the DWord-aligned Graphics Memory Address of the PREEMPTABLE command in a batch buffer where the Preemption has occurred.

BB_PREEMPT_ADDR - Batch Buffer Head Pointer Preemption Register

	1:0	**Reserved** Format: MBZ

RING_BUFFER_HEAD_PREEMPT_REG

RING_BUFFER_HEAD_PREEMPT_REG - RING_BUFFER_HEAD_PREEMPT_REG

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0214Ch
Name:	RCS RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RCS_RING_BUFFER_HEAD_PREEMPT_REG

Description	Project
This register contains the Head pointer offset in the ring when the last PREEMPTABLE command was executed and caused the head pointer to move due to the UHPTR register being valid. If the PREEMPTABLE command is executed as part of the batch buffer then the value of the register will be the offset in the ring of the command past the batch buffer start that contained the preemptable command. This is a global register and context save/restored as part of power context image.	
Preemptable Commands / **Project** / **Source** MI_ARB_CHECK / HSW / RenderCS	HSW

Programming Notes
Programming Restriction: **This register should NEVER be programmed by driver. This is for HW internal use only.**

DWord	Bit	Description
0	31:21	**Reserved** Format: MBZ
	20:2	**Preempted Head Offset** Format: U19 This field contains the Head pointer offset in the ring when the last MI_ARB_CHECK command was executed and caused the head pointer to move due to the UHPTR register being valid.
	1:0	**Ring/Batch Indicator** Format: Enabled

RING_BUFFER_HEAD_PREEMPT_REG - RING_BUFFER_HEAD_PREEMPT_REG

Value	Name	Description	Project
0h	Ring	Preemptable command was executed in ring and caused head pointer to be updated.	
1h	Batch	Preemptable command was executed in batch and caused head pointer to be updated.	
2h	2nd level batch	Preemptable command was executed in second level batch and caused head pointer to be updated.	DevHSW+

Batch Buffer Start Head Pointer Register

BB_START_ADDR - Batch Buffer Start Head Pointer Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02150h

This register contains the address specified in the last MI_START_BATCH_BUFFER command.

Programming Notes

Programming Restriction:
This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:2	**Batch Buffer Start Head Pointer** Format: GraphicsAddress[31:2] This field specifies the DWord-aligned Graphics Memory Address where the last initiated Batch Buffer starting address.
	1	**Preempted Batch Buffer RS Control Stop Flag** Format: Flag This field specifies RS Control Stop Flag when a batch buffer is preempted. This is for HW internal use and should not be written by SW. This bit gets reset when RS_PREEMPTED field of RS_PREEMPT_STATUS is written Zero. This bit is set by: • Ctx restore of this bit • MI_RS_CONTROL_STOP (except for the ctx restore command) This bit is cleared by: • MI_RS_CONTROL_START • Any Batch start except resubmitted RS batch • A batch end that doesn't include preemption • Ctx save Writing 0 to bit[0] of the RS STATUS register

BB_START_ADDR - Batch Buffer Start Head Pointer Register		
	0	**Reserved** Format: MBZ

Batch Address Difference Register

BB_ADDR_DIFF - Batch Address Difference Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32

Address:	02154h
Name:	RCS Batch Address Difference Register
ShortName:	RCS_BB_ADDR_DIFF
Valid Projects:	[DevHSW+]

This register contains the difference between the start of the last batch and where the last initiated Batch Buffer is currently fetching commands.

Programming Notes

Programming Restriction:

This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:2	**Batch Buffer Address Difference** Format: GraphicsAddress[31:2] This field specifies the DWord-aligned difference between the starting address of the batch buffer and where the last initiated Batch Buffer is currently fetching commands.
	1:0	**Reserved** Format: MBZ

Batch Offset Register

BB_OFFSET - Batch Offset Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000001
Access:	R/W
Size (in bits):	32
Address:	02158h
Name:	RCS Batch Offset Register
ShortName:	RCS_BB_OFFSET

Description	Project
This register contains the offset value to be added to the Batch Buffer Start Address in the MI_BATCH_BUFFER_START command when the Enable Offset bit in MI_BATCH_BUFFER_START command is set.	
Preemptable Commands / **Source**: MI_ARB_CHECK / RenderCS	HSW

Programming Notes	Project
This register is loaded with the **Batch Buffer Address Difference** whenever a batch buffer is ended due to preemption on MI_ARB_CHECK command and when the enable load is set.	HSW

DWord	Bit	Description
0	31:2	**Batch Buffer Offset** Format: GraphicsAddress[31:2] This field specifies the DWord-aligned offset between the starting address of the batch buffer and where the last initiated Batch Buffer is currently fetching commands.
	1	**Reserved** Format: MBZ
	0	**Enable Load** Default Value: 1 Format: Enable **Description** / **Project**: If this bit is set then the Batch Buffer Offset is loaded with the Batch Buffer Address Difference whenever a batch buffer is ended due to a MI_ARB_CHECK command. / HSW

Resource Streamer Preemption Status

RS_PREEMPT_STATUS - Resource Streamer Preemption Status

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0215Ch

Preemption from First Level Batch Buffer:
This register contains the offset in to the Batch Buffer on which Resource streamer got preempted. Note that it is offset from the Batch Start Address and not the graphics address corresponding to the preempted instruction on Batch Buffer. This register's contents will be looked at by Command Streamer on the next RS Start Trigger to provide the appropriate batch start address. Following preemption, context save happens on which this register is context saved, after context save the register gets auto reset by Command Streamer. This register gets context save/restored by Render Command Streamer as part of its render context.

Preemption from Second Level Batch Buffer:
This register contains the graphics address of the instruction in Second Level Batch Buffer on which Resource streamer got preempted. This register's contents will be looked at by Command Streamer on the next RS Start Trigger to provide the appropriate batch start address. Following preemption, context save happens on which this register is context saved, after context save the register gets auto reset by Command Streamer. This register gets context save/restored by Render Command Streamer as part of its render context.

Programming Notes

- This register is accessed by Render Command Streamer as part of render context save/restore; this register should be exercised by S/W only for resetting the register contents if required.
- Following preemption if there is no context save, SW should program this register with 0x0 so that it does not interfere with proceeding workloads.

DWord	Bit	Description
0	31:2	**Batch Buffer Offset** Format: Offset[31:2] This field specifies the DWord-aligned offset from the batch start address on which Resource Streamer got preempted.
	1	**RS_PREEMPT_STATUS** Format: MBZ This field when not set indicates RS got preempted on a natural sync point else it got preempted on a draw call.

RS_PREEMPT_STATUS - Resource Streamer Preemption Status		
	0	**RS_PREEMPTED** Default Value: 0 Format: Enable If this bit is set indicates Resource Streamer got preempted. Other fields of this register are valid only when this bit is set.

Batch Buffer Start Head Pointer Register for Upper DWord

BB_START_ADDR_UDW - Batch Buffer Start Head Pointer Register for Upper DWord

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02170h

This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space specified in the last MI_START_BATCH_BUFFER command.

Programming Notes

Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Batch Buffer Start Head Pointer Upper DWORD** Format: GraphicsAddress[47:32] This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space for the last initiated Batch Buffer starting address.

Watchdog Counter Control

PR_CTR_CTL - Watchdog Counter Control

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000001 [HSW]
Access:	R/W
Size (in bits):	32
Address:	02178h
Name:	RCS Watchdog Counter Control
ShortName:	PR_CTR_CTL

DWord	Bit	Description
0	31	**Count Select** Project: HSW Format: U1 Value / Name / Description: 0h **[Default]** Use the timestamp to increment the watchdog count (every 640ns) 1h Use the fixed function clock (csclk) to increment the watchdog count
	30:0	**Counter Logic Op** Default Value: 1h This field specifies the action to be taken by the clock counter to generate interrupts. Writing a Zero value to this register starts the counting. Writing a Value of 0000_0001 to this counter stops the counter.

Render Watchdog Counter Threshold

PR_CTR_THRSH - Render Watchdog Counter Threshold

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00150000
Access:	R/W
Size (in bits):	32
Address:	0217Ch

DWord	Bit	Description
0	31:0	**Counter logic Threshold** Default Value: 00150000h Format: U32 This field specifies the threshold that the hardware checks against for the value of the render clock counter before generating an interrupt. The counter in hardware generates an interrupt when the threshold is reached, rolls over and starts counting again. The interrupt generated is the "Media Hang Notify" interrupt since this watchdog timer is intended primarily to remedy VLD hangs on the main pipeline.

Watchdog Counter Threshold

PR_CTR_THRSH - Watchdog Counter Threshold

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00145855
Access:	R/W
Size (in bits):	32
Address:	0217Ch
Name:	RCS Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH

DWord	Bit	Description
0	31:0	**Counter Logic Threshold** Default Value: 00145855h Format: U32 This field specifies the threshold that the hardware checks against for the value of the render clock counter before generating an interrupt. The counter in hardware generates an interrupt when the threshold is reached, rolls over and starts counting again. The interrupt generated is the "Media Hang Notify" interrupt since this watchdog timer is intended primarily to remedy VLD hangs on the main pipeline.

Current Context Register

CCID - Current Context Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02180h

This register contains the current logical rendering context address associated with the ring buffer in ring buffer mode of scheduling. This register contents are not valid in Exec-List mode of scheduling.

Programming Notes

The CCID register must not be written directly (via MMIO) unless the Command Streamer is completely idle (i.e., the Ring Buffer is empty and the pipeline is idle). Note that, under normal conditions, the CCID register should only be updated from the command stream using the MI_SET_CONTEXT command.

DWord	Bit	Description
0	31:12	**Logical Render Context Address (LRCA)** Default Value: 0h Format: GraphicsAddress[31:12] This field contains the 4 KB-aligned Graphics Memory Address of the current Logical Rendering Context. Bit 11 MBZ.
	11:10	**Reserved** Format: MBZ
	9	**HD DVD Context** Value 0h: Regular Context Value 1h: HD DVD Context — Special considerations for TDP allow for higher voltage and frequency.
	8	**Reserved** Format: Must Be One
	7:4	**Reserved** Format: MBZ
	3	**Extended State Save Enable** Format: Enable

CCID - Current Context Register

		If set, the extended state identified in the Logical Context Data section of the Memory Data Formats chapter, is saved as part of switching away from this logical context.
	2	**Extended State Restore Enable** Format: Enable If set, the extended state identified in the Logical Context Data section of the Memory Data Formats chapter, was loaded (or restored) as part of switching to this logical context.
	1	**Reserved** Format: MBZ
	0	**Valid** Format: U1

Value	Name	Description
0h	Invalid **[Default]**	The other fields of this register are invalid. A switch away from the context will not invoke a context save operation.
1h	Valid	The other fields of this register are valid, and a switch from the context will invoke the normal context save/restore operations.

Render Watchdog Counter

PR_CTR - Render Watchdog Counter	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	02190h

DWord	Bit	Description
0	31:0	**Counter Value** Format: U32 This register reflects the render watchdog counter value itself. It cannot be written to.

Context Sizes

CXT_SIZE - Context Sizes

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0xF54D430D
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	021A8h

The actual size of a logical rendering context is the amount of data stored/restored during a context switch and is measured in 64B cache lines.

This register will be power context save/restored. Note that this register will default to the correct value, so software should not have to modify it.

DWord	Bit	Description
0	31:26	**Power Context Size** Default Value: 3Dh This field indicates the Power context data that needs to be save/restored.
	25:23	**Ring Context Size** Default Value: 2h This field indicates the Ring context data that needs to be save/restored.
	22:15	**Render Context Size** Default Value: 9Ah This field indicates the size of the render context data that needs to be save/restored when extended mode is not enabled for a context; this also excludes VF context size.
	14:7	**SOL Context Offset** Default Value: 86h This field indicates the offset of the SOL context in to the render context. Power context size should be added to derive the offset in case of power context.
	6	**Reserved** This field indicates the amount of data that need not be save/restored from render context in GT1 mode. Note: This is the amount of data not save/restored from TDL and SC in GT1 mode.

CXT_SIZE - Context Sizes		
		Default Value=0h
	5:0	**VF State Context Size** Default Value: Dh This field indicates the amount of VF unit data context save/restored in cachelines.

Resource Streamer Context Offset

RS_CXT_OFFSET - Resource Streamer Context Offset

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x000029C0
Access:	Read/32 bit Write Only
Size (in bits):	32
Address:	021B4h

DWord	Bit	Description
0	31:6	**RS Offset** Format: U26 This field indicates the offset (64bytes granular) in to the logical rendering context to which Resource Streamer context is save/restored when enabled. This field register must not be written directly (via MMIO) unless the Command Streamer is completely idle (i.e., the Ring Buffer is empty and the pipeline is idle) and RC6 is disabled. On way to program this register is via Load Register Immediate command in the ring buffer as part of initialization sequence. Value / Name / Description A7h / **[Default]** / DefaultValueDesc
	5:0	**Reserved** Format: MBZ

URB Context Offset

URB_CXT_OFFSET - URB Context Offset		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	RenderCS	
Default Value:	0x00008580	
Access:	Read/32 bit Write Only	
Size (in bits):	32	
Address:	021B8h	
DWord	**Bit**	**Description**
0	31:6	**URB Offset** Default Value: 216h This field indicates the offset (64bytes granular) in to the logical rendering context to which URB contents are save/restored when enabled. This field register must not be written directly (via MMIO) unless the Command Streamer is completely idle (i.e., the Ring Buffer is empty and the pipeline is idle) and RC6 is disabled. One way to program this register is via Load Register Immediate command in the ring buffer as part of initialization sequence.
	5:0	**Reserved** Format: MBZ

Predicate Rendering Data Result 2

MI_PREDICATE_RESULT_2 - Predicate Rendering Data Result 2

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02214h

DWord	Bit	Description
0	31:1	**Reserved** Format: MBZ
	0	**MI_PREDICATE_RESULT_2** This bit must be loaded with by SW based on GT mode of operation. This register must be loaded appropriately before using MI_SET_PREDICATE command. Value / Name / Description 1h / / Indicates GT3 mode and lower slice is enabled. 0h / **[Default]** / Indicates GT2 mode and lower slice is disabled.

PPGTT Directory Cacheline Valid Register

PP_DCLV - PPGTT Directory Cacheline Valid Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Size (in bits):	64

Address: 02220h

Description	Project
Access: R/W	HSW
This register controls update of the on-chip PPGTT Directory Cache during a context restore. Bits that are set will trigger the load of the corresponding 16 directory entry group. This register is restored with context (prior to restoring the on-chip directory cache itself). This register is also restored when switching to a context whose LRCA matches the current CCID if the **Force PD Restore** bit is set in the context descriptor. The context image of this register must be updated and maintained by SW; SW should not normally need to read this register. This register can also effectively be used to limit the size of a process's virtual address space. Any access by a process that requires a PD entry in a set that is not enabled in this register will cause a fatal error, and no fetch of the PD entry will be attempted.	

Programming Notes	Project
Page Directory Base Register is a Global Context Register (power context) and not maintained per context in ring buffer mode of submission. One should explicitly load PP_DCLV followed by PP_DIR_BASE register through Load Register Immediate commands in Ring Buffer before submitting a context. One should program these registers after ensuring the pipe is completely flushed with TLB's invalidated.	HSW

DWord	Bit	Description
0	63:32	**Reserved** Project: All Format: MBZ
	31:0	**PPGTT Directory Cache Restore [1..32] 16 entries** Project: All Format: BitMask[Enable] If set, the [1st..32nd] 16 entries of the directory cache are considered valid and will be brought in on context restore. If clear, these entries are considered invalid and fetch of these entries will not be attempted.

Matched Context ID Reset Register

MTCH_CID_RST - Matched Context ID Reset Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0222Ch
Valid Projects:	HSW

This register is used to generate a Context ID specific reset (Render Only). To initiate a reset, the register is written with the pending bit set. Hardware compares the current context ID with the register and on match generates a Render Only reset. After reset is complete, HW clears the pending bit and can be programmed to generate an interrupt. The match bit is set. If the current context ID does not match this register, the pending bit is reset and an interrupt is generated. The match bit is reset.The match indicates the result of the last comparison, and its valid only when pending bit is zero.Please see MCIDRST interrupt bit assignment in the Interrupt Control Registers.

DWord	Bit	Description
0	31:12	**Match Context ID** Format: U20 Contains the context ID to be compared with the currently running context ID.
	11:2	**Reserved** Format: MBZ
	1	**Match** Format: U1 This bit indicates the result of the match operation; 1 means the Current Context ID matches the Match Context ID field.
	0	**Pending** Format: U1 This bit indicates that a matched context ID reset is pending. The bit should be set when the register is written (in order to have a pending MTCH_CID_RST request), and will be reset by hardware to indicate that the operation is completed (Either with a match or mismatch)

Count Active Channels Dispatched

TS_GPGPU_THREADS_DISPATCHED - Count Active Channels Dispatched

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02290h

This register is used to count the number of active channels that TS sends for dispatch. For each dispatch the active bits in the execution mask are summed and added to this register. This register is reset when a write occurs to 2290h

DWord	Bit	Description
0	63:0	**GPGPU_THREADS_DISPATCHED** Format: U64 This count is increased by the number of active bits in the execution mask each time the TS sends a GPGPU dispatch.

Graphics Mode Register

GFX_MODE - Graphics Mode Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000 [NOVALIDPROJECTS]
	0x00000800 [HSW]
Size (in bits):	32
Trusted Type:	1

Address:	0229Ch
Valid Projects:	HSW

Description	Project
This register contains a control bit for the new execlist and 2-level PPGTT functions.	
DefaultValue = 00002800h	HSW

DWord	Bit	Description
0	31:16	**Mask Bits** Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:14	**Reserved** Project: HSW Format: MBZ
	13	**Flush TLB invalidation Mode** Project: HSW Format: U1 This field controls the invalidation if the TLB cache inside the hardware. When enabled this bit limits the invalidation of the TLB only to batch buffer boundaries, to pipe_control commands which have the TLB invalidation bit set and sync flushes. If disabled, the TLB caches are flushed for every full flush of the pipeline.
	12	**Reserved** Project: All Format: MBZ
	11	**Replay Mode** Project: HSW

Format:	U1 Context Switch Granularity

This field controls the granularity of the replay mechanism when coming back into a previously preempted context.

Value	Name	Description
1h	mid-cmdbuffer preemption **[Default]**	Drawcall Level. Pipeline is flushed before switching to the next context. Commands parsed are committed to completing before a context switch.

Programming Notes
A fixed function pipe flush is required before modifying this field. Unless pre-emption at a mid-triangle is required the bit must be set.

10 **Reserved**

Project:	All
Format:	MBZ

9 **Per-Process GTT Enable**

Project:	HSW
Format:	Enabled

Per-Process GTT Enable

Value	Name	Description
0h	PPGTT Disable **[Default]**	When clear, the Global GTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.
1h	PPGTT Enable	When set, the PPGTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space. The PD Offset and PD Cacheline Valid registers must be set in all pipes (blitter, MFX, render) before any workload is submitted to hardware. This mode enables support for big pages (32k).

8 **Reserved**

Project:	HSW

7 **Reserved**

Project:	HSW
Format:	MBZ

6:1 **Reserved**

Project:	HSW
Format:	MBZ

0 **Reserved**

Project:	Pre-DevHSW, DevHSW:GT3:A
Format:	MBZ

GFX_MODE - Graphics Mode Register		
	0	**Privilege Check Disable** Project: DevHSW, EXCLUDE(DevHSW:GT3:A) Format: Enable This field when set, disables Privilege Violation checks on non-privileged batch buffers. When set Privileged commands are allowed to be executed from non-privileged batch buffers.

CS Power Management FSM

CSPWRFSM - CS Power Management FSM

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	022ACh

This register contains the state code of the Power Management FSM, FBC Forward FSM, CSSTDT FSM, CSARB FSM, CSBUPDATE FSM. Decoding the contents of this register will indicate what the state of the corresponding state machine.

DWord	Bit	Description
0	31:30	**Reserved** Format: MBZ
	29:28	**CSFBCSLICE0** Format: U2 FBC message forward FSM state

Value	Name
0h	CSFBCIDLE_0
1h	CSFBCMODIFY_0
2h	CSFBCCLEAN_0
3h	CSFBCDONE_0

	27:24	**Reserved** Format: MBZ
	23:21	**CS ARB** Format: U3 Overall state of the command streamer. Describes what state CS is in

Value	Name	Project
0h	ARBIDLE_s	
1h	P0RNG_s CS	
2h	P0BATCH_s	
3h	ARBCHK	
4h	ARBCHK1	
5h	CTXOP_s	

CSPWRFSM - CS Power Management FSM

6h	WABATCH_s	HSW+
7h	PSLBATCH	HSW+

20 Reserved

Format:	MBZ

19:17 CSSWITCH

Format:	U3

Arbiters CSSWITCH FSM state decoding.

Value	Name
0h	SWIDLE_s
1h	SWITCH_s
2h	ASREQ_s
3h	DMACHK_s
4h	ARBWAIT_s
5h	FIFORECFG_s
6h-7h	Reserved

16:13 CSCSBUPDATE

Format:	U4

CS Power Management CSBLOCK FSM state

Value	Name
0h	CSBIDLE
1h	CSQ
2h	WRPTR
3h	SEMA1
4h	SEMA2
5h	TS1
6h	TS2
7h	TS3
8h	TS4
9h	DUMMYREQ
Ah	DUMMYWT
Bh	INTWT
Ch-Fh	Reserved

12:11 R2MWRREQ

Format:	U2

CSSTDT memory request FSM state

Value	Name

CSPWRFSM - CS Power Management FSM

0h	WRIDLE
1h	WRREQ_HW1
2h	WRREQ_HW2
3h	WRRD

10 **Reserved**

Format:	MBZ

9:7 **LOADARB**

Format:	U3

CSSTDT arbiter FSM state

Value	Name
0h	LDIDLE
1h	LDAUTO
2h	LDPRSR
3h	LDCTX
4h	LDFLSH
5h	LDREG
6h	LDSHR1

Programming Notes

LOADARB FSM states needs 4 bits for encoding, however only 3bits have been mapped on MMIO. 8h -> LDLRM is the state which is missed out, due to less bits mapped, LDLRM/LDIDLE cant be resolved with certain.

6:4 **CSBLOCK**

Format:	U3

CS Power Management CSBLOCK FSM state

Value	Name
0h	CSBLOCK
1h	CSCTXARB
2h	CSUNBLOCKRESTORE
3h	CSUNBLOCK
4h	CSPREP4BLOCK
5h-7h	Reserved

3:0 **CSIDLE**

Format:	U4

CS Power Management CSBLOCK FSM state

Value	Name

CSPWRFSM - CS Power Management FSM			
		0h	CSBUSY
		1h	CNTWT
		2h	FLSHREQ
		3h	FLSHWT
		4h	CTXSAVE
		5h	CSREQBLOCK
		6h	PMTURNOFF
		7h	PMIDLEWT
		8h	IDLE
		9h	PMTURNON
		Ah	PMBUSYWT
		Bh	DOPFFCGREQ
		Ch	DOPFFCGWAIT
		Dh	DOPFFCG
		Eh	DOPFFCUGREQ
		Fh	DOPFFCUGWAIT

PS Invocation Count for Slice0

PS_INVOCATION_COUNT_SLICE0 - PS Invocation Count for Slice0	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	022C8h

This register stores the value of the count of pixels that get shaded in Slice0. This register is part of the context save and restore. This register should not be programmed by SW.Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).

DWord	Bit	Description
0..1	63:0	**PS Invocation Count** Reflects a count of the total number of pixels (DevHSW: including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice0. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Depth Count for Slice0

PS_DEPTH_COUNT_SLICE0 - PS Depth Count for Slice0	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	022D8h

This register stores the value of the count of pixels that have passed the depth test in Slice0. This register is part of the context save and restore. This register should not be programmed by SW.Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).

DWord	Bit	Description
0..1	63:0	**Depth Count** This register reflects the total number of pixels that have passed the depth test in Slice0(i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Invocation Count for Slice1

PS_INVOCATION_COUNT_SLICE1 - PS Invocation Count for Slice1	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	022F0h

This register stores the value of the count of pixels that get shaded in Slice0. This register is part of the context save and restore. This register should not be programmed by SW.Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).

DWord	Bit	Description
0..1	63:0	**PS Invocation Count** Reflects a count of the total number of pixels (DevHSW: including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice1. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Depth Count for Slice1

PS_DEPTH_COUNT_SLICE1 - PS Depth Count for Slice1	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	022F8h

This register stores the value of the count of pixels that have passed the depth test in Slice1. This register is part of the context save and restore. This register should not be programmed by SW.Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).

DWord	Bit	Description
0..1	63:0	**Depth Count** This register reflects the total number of pixels that have passed the depth test in Slice1(i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

HS Invocation Counter

HS_INVOCATION_COUNT - HS Invocation Counter		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	02300h	
This register stores the number of patch objects processed by the HS unit. E.g., A PATCHLIST_2 topology with 6 vertices would cause this counter to increment by 3 (there are 3 2-vertex patch objects in that topology).This register is part of the context save and restore.		
DWord	**Bit**	**Description**
0	63:0	**HS Invocation Count** Number of patch objects processed by the HS stage. Updated only when HS Enable and HS Statistics Enable are set in 3DSTATE_HS

DS Invocation Counter

DS_INVOCATION_COUNT - DS Invocation Counter	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02308h

This register stores the number of domain points shaded by the DS threads. Domain points which hit in the DS cache will not cause this register to increment. Note that the spawning of a DS thread which shades two domain points will cause this counter to increment by two.This register is part of the context save and restore.

DWord	Bit	Description
0	63:0	**DS Invocation Count** Number of domain points shaded by the DS threads. Updated only when DS Function Enable and Statistics Enable are set in 3DSTATE_DS

IA Vertices Count

IA_VERTICES_COUNT - IA Vertices Count	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02310h

This register stores the count of vertices processed by VF. This register is part of the context save and restore.

DWord	Bit	Description
0	63:0	**IA Vertices Count Report** Total number of vertices fetched by the VF stage. This count is updated for every input vertex as long as Statistics Enable is set in VF_STATE (see the Vertex Fetch Chapter in the 3D Volume.)

Primitives Generated By VF

IA_PRIMITIVES_COUNT - Primitives Generated By VF		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	02318h	
This register stores the count of primitives generated by VF. This register is part of the context save and restore.		
DWord	**Bit**	**Description**
0	63:0	**IA Primitives Count Report** Total number of primitives output by the Vertex Fetch (IA) stage. This count is updated for every primitive output by the VF stage, as long as Statistics Enable is set in VF_STATE (see the Vertex Fetch Chapter in the 3D Volume.)

VS Invocation Counter

VS_INVOCATION_COUNT - VS Invocation Counter		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	02320h	
This register stores the value of the vertex count shaded by VS. This register is part of the context save and restore.		
DWord	**Bit**	**Description**
0	63:0	**VS Invocation Count Report** Number of vertices that are dispatched as threads by the VS stage. Updated only when **Statistics Enable** is set in VS_STATE (see the Vertex Shader Chapter in the 3D Volume.)

GS Invocation Counter

GS_INVOCATION_COUNT - GS Invocation Counter		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	02328h	
This register stores the number of objects that are part of geometry shader threads. This register is part of the context save and restore.		
DWord	**Bit**	**Description**
0	63:0	**GS Invocation Count** Number of objects that are dispatched as a geometry shader threads invoked by the GS stage. Updated only when **Statistics Enable** is set in GS_STATE (see the Geometry Shader Chapter in the 3D Volume.)

GS Primitives Counter

GS_PRIMITIVES_COUNT - GS Primitives Counter		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	02330h	
This register reflects the total number of primitives that have been output by the Geometry Shader stage. This register is part of the context save and restore.		
DWord	**Bit**	**Description**
0	63:0	**GS Primitives Count** Total number of primitives output by the geometry stage. Updated only when Statistics Enable is set in GS_STATE (see the Geometry Shader Chapter in the 3D Volume.)

Clipper Invocation Counter

CL_INVOCATION_COUNT - Clipper Invocation Counter		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	02338h	
This register stores the count of objects entering the Clipper stage. This register is part of the context save and restore.		
DWord	**Bit**	**Description**
0	63:0	**CL Invocation Count Report** Number of objects entering the clipper stage. Updated only when Statistics Enable is set in CLIP_STATE (see the Clipper Chapter in the 3D Volume.)

Clipper Primitives Counter

CL_PRIMITIVES_COUNT - Clipper Primitives Counter	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02340h

This register reflects the total number of primitives that have been output by the clipper. This register is part of the context save and restore.

DWord	Bit	Description
0	63:0	**Clipped Primitives Output Count** Total number of primitives output by the clipper stage. This count is updated for every primitive output by the clipper stage, as long as Statistics Enable is set in SF_STATE (see the Clipper and SF Chapters in the 3D Volume.)

PS Invocation Count

PS_INVOCATION_COUNT - PS Invocation Count

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02348h

Note	Description	Project
[DevHSW:GT3:A]	This counter may have incorrect value when EDSC = 1. This register stores the value of the count of pixels that get shaded. This register is part of the context save and restore.	DevHSW:GT3:A

DWord	Bit	Description
0..1	63:0	**PS Invocation Count** Reflects a count of the total number of pixels (DevHSW: including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Depth Count

PS_DEPTH_COUNT - PS Depth Count	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02350h

This register stores the value of the count of samples that have passed the depth test. This register is part of the context save and restore. Note that the value of this register can be obtained in a pipeline-synchronous fashion without a pipeline flush by using the 3DCONTROL command. See 3D Overview in the 3D volume.

DWord	Bit	Description
0..1	63:0	**Depth Count** This register reflects the total number of samples that have passed the depth test (i.e., will be visible). All samples are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Samples that pass the depth test but fail the stencil test will not be counted.

Reported Timestamp Count

TIMESTAMP - Reported Timestamp Count

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	RO. This register is not set by the context restore.
Size (in bits):	64
Address:	02358h

Description	Project
This register provides an elapsed real-time value that can be used as a timestamp for GPU events over short periods of time. Note that the value of this register can be obtained in a 3D pipeline-synchronous fashion without a pipeline flush by using the PIPE_CONTROL command. See 3D Geometry Pipeline in the "3D and Media" volume.This register (effectively) counts at a constant frequency by adjusting the increment amount according to the actual reference clock frequency. SW therefore does not need to know the reference clock frequency.This register is not reset by a graphics reset. It will maintain its value unless a full chipset reset is performed.	
Note: On Core platforms, the TIMESTAMP register is initialized with the value of the PCU ART and hence tracks bits 38:3 of the 100 MHz ART fairly closely. However, due to variability in the actual time it takes to download the ART value to GT, the value of the TIMESTAMP register will be lower than the value of the PCU ART by an amount dependent on the relative IA/CLR/GT frequencies at the time the timestamp was downloaded to GT (expected to range between 100 and 600 ns). When comparing the value sampled from this register by GT HW to values read from the PCU timer by other system agents, timing differences between GT HW reading the TIMESTAMP register and the involved non-GT agent(s) reading the PCU ART must also be comprehended.	HSW

DWord	Bit	Description
0	63:36	**Reserved** Format: MBZ
	35:0	**Timestamp Value** Format: U36 Description: This register toggles every 80 ns. The upper 28 bits are zero. (Project: HSW)

Observation Architecture Control

OACONTROL - Observation Architecture Control

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02360h
Valid Projects:	HSW

This register controls global OA functionality, report format, interrupt steering and context filtering.

DWord	Bit	Description
0	31:12	**Select Context ID** Project: HSW Specifies the context ID of the one context that affects the performance counters. All other contexts are ignored.
	11:6	**Timer Period** Project: HSW Format: Select Specifies the period of the timer strobe as a function of the minimum TIME_STAMP resolution. The period is determined by selecting a specified bit from the TIME_STAMP register as follows: StrobePeriod = MinimumTimeStampPeriod * $2^{(\text{TimerPeriod} + 1)}$ The exponent is defined by this field. Note: The TIME_STAMP is not reset at start time so the phase of the strobe is not synchronized with the enable of the OA unit. This could result in approximately a full StrobePeriod elapsing prior to the first trigger. Usage for this mechanism should be time based periodic triggering, typically.
	5	**Timer Enable** Project: HSW Format: Enable Description: This field enables the timer logic to output a periodic strobe, as defined by the Timer Period. When disabled the timer output is not asserted. Project: HSW Users should be aware that while programming Timer based and Threshold Counter

based triggers simultaneously for internal reporting, they should be programmed such a way that they are not consecutively triggered. If programmed simultaneously, RTL pulse detection logic will have problem when these triggers occur in consecutive clock cycles.

Value	Name	Description
0h	Disable **[Default]**	Counter does not get written out on regular interval
1h	Enable	Counter gets written out on regular intervals, defined by the Timer Period

4:2 **Reserved**

Project:	HSW
Format:	MBZ

1 **Specific Context Enable**

Format:	Enable

Enables counters to work on a context specific workload. The context is given by bits 31:12. OA unit level clock gating must be ENABLED when using specific ContextID feature.

Value	Name	Description	Project
0h	Disable **[Default]**	All contexts are considered	
1h	Enable	Only the contexts with the Select Context ID are considered	HSW

0 **Performance Counter Enable**

Project:	All
Format:	Enable

Global performance counter enable. If clear, no counting will occur. MI_REPORT_PERF_COUNT is undefined when clear.

Programming Notes	Project
When this bit is set, in order to have coherent counts, RC6 power state and render trunk clock gating must be disabled. This can be achieved by programming MMIO registers as 0xA094=0x0 and 0xA090[31]=1.	HSW

Observation Architecture Status Register 1

OASTATUS1 - Observation Architecture Status Register 1

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02364h
Valid Projects:	HSW

This register is used to program the OA unit.

DWord	Bit	Description
0	31:6	**Tail Pointer** Project: HSW Virtual address of the internal trigger based buffer and it is updated for every 64B cacheline write to memory when reporting via internal trigger. This pointer will not be updated for MI_REPORT_PERF_COUNT command based writes. **Programming Notes** When OA is enabled, this address must be programmed by SW to the base address of the internal trigger base mechanism. SW must ensure that Tail pointer and the Head Pointer (in OASTATUS2) do not have different values while programming.
	5:3	**Inter Trigger Report Buffer Size** Project: HSW This field indicates the size of buffer for internal trigger mechanism. This field is programmed in terms of multiple of 128KB.

Value	Name	Description	Project
0h	All context considered **[Default]**		
0b		128KB	HSW
1b		256KB	HSW
2		512KB	HSW
3		1MB	HSW
4		2MB	HSW
5		4MB	HSW
6		8MB	HSW
7		16MB	HSW

OASTATUS1 - Observation Architecture Status Register 1

	2	**Counter OverFlow Error** Format: Select This bit is set if any of the counters overflows. This bit can be reset by SW in B0.
	1	**Buffer Overflow** Default Value: 0h This bit is set when the Tail-pointer - Head pointer > max internal trigger buffer size
	0	**Report Lost Error** Format: Enable This bit is set if the Report Logic is requested to write out the counter values before the previous report request was completed. The report request is ignored and the counter continue to count.This bit can be reset by SW in B0.

Observation Architecture Status Register 2

OASTATUS2 - Observation Architecture Status Register 2

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000 [NOVALIDPROJECTS] 0x00000001 [HSW]
Access:	R/W
Size (in bits):	32

Address: 02368h

This register is used to program the OA unit.

DWord	Bit	Description
0	31:6	**Head Pointer** Virtual address of the internal trigger based buffer that is updated by software after consuming from the report buffer. This pointer must be updated by SW for internal trigger base buffer only.
	5	**Reserved** Format: MBZ
	4	**Tail Pointer Wrap Mask** Project: HSW **Programming Notes** This bit should be set in order to program Tail Pointer Wrap Flag. This bit is for HW internal use. SW should always set this bit to 0.
	3	**Tail Pointer Wrap Flag** Project: HSW Format: U1 **Programming Notes** This bit is for HW internal use to context save /restore Tail Pointer Wrap Flag. SW should not program this bit. This bit gets programmed only when Tail Pointer Wrap Mask bit is set.
	2	**Head Pointer Wrap Mask** Project: HSW **Programming Notes** This bit should be set in order to program Head Pointer Wrap Flag. This bit is for HW internal use. SW should always set this bit to 0.

OASTATUS2 - Observation Architecture Status Register 2

1 **Head Pointer Wrap Flag**

Project:	HSW
Format:	U1

Programming Notes
This bit is for HW internal use to context save /restore Head Pointer Wrap Flag. SW should not program this bit. This bit gets programmed only when Head Pointer Wrap Mask bit is set.

0 **Memory select PPGTT/GGTT access**

Project:	HSW
Access:	RO

Value	Name
0	PPGTT
1	GGTT **[Default]**

Programming Notes	Project
When Render Engine is using PPGTT, OABUFFER must be mapped using valid PPGTT addresses.	DevHSW:GT3:A, DevHSW:GT2:B, DevHSW:GT3e:B
OABUFFER must always reside in GGTT memory. This bit must be set to '1'.	DevHSW, EXCLUDE(DevHSW:GT3:A), EXCLUDE(DevHSW:GT2:B), EXCLUDE(DevHSW:GT3e:B)

Observation Architecture Buffer

OABUFFER - Observation Architecture Buffer

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32

Address:	023B0h
Valid Projects:	HSW
Access:	R/W

This register is used to program the OA unit.

Programming Notes	Project
This MMIO must be set before the OASTATUS1 register and set after the OASTATUS2 register. This is to enable proper functionality of the overflow bit.	HSW
Report Buffer Offset Must be 16MB aligned.	HSW

DWord	Bit	Description
0	31:6	**Report Buffer Offset** Format: GraphicsAddress[31:6] This field specifies 64B aligned GFX MEM address where the chap counter values are reported.
	5	**Reserved** Project: HSW Format: MBZ
	4	**OVERRUN STATUS** Default Value: 0h Enabled Project: HSW Format: Enable This filed indicates the status of overrun for debug purpose. This bit is read only and writing to this bit will have no effect. This bit will reflect the status of overrun irrespective of Overrun Mode enabled or disabled.
	3	**Disable Overrun Mode** Project: HSW Format: Enable This field defines the mode of reporting for internal trigger/timer based reporting. When this bit is set, overrun does not lose reports but stops reporting. Based on the head and tail pointer, when

HW detects room for the report, it would resume reporting to the buffer. This mode would not set the over-run bit in the register. When this mode bit is reset, buffer overrun can happen and lose the reports while setting the buffer over-run bit.

Value	Name	Description	Project
0h	Disable **[Default]**	Counter gets written out on regular intervals, defined by the Timer Period	HSW
1h	Enable	Counter does not get written out on regular interval	HSW

2 **OA Report Trigger Select**

Value	Name	Description
0		Level Report trigger
1		Edge Report trigger

1 **Counter Stop Resume Mechanism Enable**

Project:	HSW

0 **Reserved**

Project:	HSW

Predicate Rendering Temporary Register0

MI_PREDICATE_SRC0 - Predicate Rendering Temporary Register0

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	02400h-02407h

DWord	Bit	Description
0	63:0	**MI_PREDICATE_SRC0** This register is a temporary register for Predicate Rendering. See Predicate Rendering section for more details.

Predicate Rendering Temporary Register1

MI_PREDICATE_SRC1 - Predicate Rendering Temporary Register1

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	02408h-0240Fh

DWord	Bit	Description
0	63:0	**MI_PREDICATE_SRC1** This register is a temporary register for Predicate Rendering. See Predicate Rendering section for more details.

Predicate Rendering Data Storage

MI_PREDICATE_DATA - Predicate Rendering Data Storage	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	02410h-02417h

DWord	Bit	Description
0	63:0	**MI_PREDICATE_DATA** This register is used either as computed value based off the MI_PREDICATE_SRC0 and MI_PREDICATE_SRC1 or a temporary register. See Predicate Rendering section for more details.

Predicate Rendering Data Result

MI_PREDICATE_RESULT - Predicate Rendering Data Result	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02418h

DWord	Bit	Description
0	31:1	**Reserved** Format: MBZ
	0	**MI_PREDICATE_RESULT** This bit is the result of the last MI_PREDICATE.

Predicate Rendering Data Result 1

MI_PREDICATE_RESULT_1 - Predicate Rendering Data Result 1	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0241Ch
Name:	RCS Predicate Rendering Data Result 1
ShortName:	RCS_MI_PREDICATE_RESULT_1

DWord	Bit	Description
0	31:1	**Reserved** Format: MBZ
	0	**MI_PREDICATE_RESULT_1** This bit is used to predicate MI_BATCH_BUFFER_START commands in the RCS command stream. Usage Model: MI_MATH command will be used to do some ALU operations over GPR followed by a MI_LOAD_REGISTER_REGISTER to move the result from GPR to MI_PREDICATE_RESULT_1.

Auto Draw End Offset

3DPRIM_END_OFFSET - Auto Draw End Offset	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02420h-02423h

DWord	Bit	Description
0	31:0	**End Offset** Format: U32 This register is used to store the end offset value used by the Vertex Fetch to determine when to stop processing the 3D_PRIMITIVE command. This register is valid when the End Offset Enable is set in the 3D_PRIMITIVE command.

Load Indirect Start Vertex

3DPRIM_START_VERTEX - Load Indirect Start Vertex	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02430h-02433h

DWord	Bit	Description
0	31:0	**Start Vertex** Format: U32 This register is used to store the Start Vertex of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Vertex Count

3DPRIM_VERTEX_COUNT - Load Indirect Vertex Count	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02434h-02437h

DWord	Bit	Description
0	31:0	**Vertex Count** Format: U32 This register is used to store the Vertex Count of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Instance Count

3DPRIM_INSTANCE_COUNT - Load Indirect Instance Count	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02438h-0243Bh

DWord	Bit	Description
0	31:0	**Instance Count** This register is used to store the Instance Count of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Start Instance

3DPRIM_START_INSTANCE - Load Indirect Start Instance	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0243Ch-0243Fh

DWord	Bit	Description
0	31:0	**Start Vertex** Format: U32 This register is used to store the Start Instance of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Base Vertex

3DPRIM_BASE_VERTEX - Load Indirect Base Vertex	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02440h-02443h

DWord	Bit	Description
0	31:0	**Base Vertex** Format: S31 This register is used to store the Base Vertex of the 3D_PRIMITIVE command when Load Indirect Enable is set.

VF Scratch Pad

VFSKPD - VF Scratch Pad

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02470h
Address:	02740h-02743h
Valid Projects:	HSW

DWord	Bit	Description
0	31:16	**Mask Bits** Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All bits implemented)
	15	**Reserved** Project: HSW Format: MBZ
	14:9	**Reserved** Project: All Format: MBZ
	8	**Reserved** Project: HSW Format: MBZ
	7	**Reserved** Project: HSW Format: MBZ
	6	**Reserved** Project: HSW Format: MBZ
	5	**TLB Prefectch Enable** Project: DevHSW+ Format: U1

VFSKPD - VF Scratch Pad

Value	Name	Description
0h	Disable **[Default]**	The VF will generate prefetch of TLB when it is fetching sequential vertex data and four or fewer vertex buffers are valid.
1h	Enable	VF will disable prefetch of TLB entries.

4 **Reserved**

Project:	HSW
Format:	MBZ

3 **Reserved**

Project:	HSW
Format:	MBZ

2 **Vertex Cache Implicit Disable Inhibit**

Format:	U1

Value	Name	Description
0h	**[Default]**	Allow VF to disable VS0 when Sequential index or Prim ID is a valid Element.
1h		VF never implicitly disables the vertex cache. Software must disable the VS0 Cache when required.

1 **Disable Over Fetch Cache**

Project:	HSW
Format:	MBZ This bit must be '0' always.

0 **Disable Multiple Miss Read squash**

Project:	DevHSW+
Format:	Disable

Value	Name	Description
0h	**[Default]**	Allow VF to squash reads that are to the same cacheline for vertex buffer requests.
1h		Disallow VF from squashing reads that are to the same cacheline for vertex buffer requests.

BTB Not Consumed By RCS

BTP_PRODUCE_COUNT - BTB Not Consumed By RCS

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	02480h

This register keeps track of the outstanding BTP produced by RS which are not yet consumed by Render Command Streamer.
This register is part of the render context save and restore.

Programming Notes

This register should not be programmed by SW.

DWord	Bit	Description
0	31:0	**BTP Produce Count** This register keeps track of the outstanding BTP produced by RS which are not yet consumed by Render Command Streamer. This register is part of the render context save and restore.

DX9 Constants Not Consumed By RCS

DX9CONST_PRODUCE_COUNT - DX9 Constants Not Consumed By RCS

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	02484h

This register keeps track of the outstanding DX9 Constants produced by RS which are not yet consumed by Render Command Streamer. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0	31:0	**DX9 Constants Produce Count** This register keeps track of the outstanding DX9 Constants produced by RS which are not yet consumed by Render Command Streamer. This register is part of the render context save and restore.

Gather Constants Not Consumed By RCS

GATHER_CONST_PRODUCE_COUNT - Gather Constants Not Consumed By RCS

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	0248Ch

This register keeps track of the outstanding Gather Constants produced by RS which are not yet consumed by Render Command Streamer. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0	31:0	**Gather Constants Produce Count** This register keeps track of the outstanding Gather Constants produced by RS which are not yet consumed by Render Command Streamer. This register is part of the render context save and restore.

BTP Commands Parsed By RCS

BTP_PARSE_COUNT - BTP Commands Parsed By RCS

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	02490h

This register keeps track of the BTP commands parsed by RCS prior to encountering the Draw Call in an RS enabled Batch Buffer which has BTP Pool Alloc Valid. BTP parse count should be less then equal to the BTP produce count for Command Streamer to make progress on a 3D_PRIMITIVE command. BTP Parse count is subtracted from the BTP Produce Count upon parsing 3D_PRIMITIVE command. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0	31:0	**BTP Parse Count** This register keeps track of the BTP commands parsed by RCS prior to encountering the Draw Call in an RS enabled Batch Buffer which has BTP Pool Alloc Valid. BTP parse count should be less then equal to the BTP produce count for Command Streamer to make progress on a 3D_PRIMITIVE command. BTP Parse count is subtracted from the BTP Produce Count upon parsing 3D_PRIMITIVE command.

DX9 Constants Prsed By RCS

DX9CONST_PARSE_COUNT - DX9 Constants Prsed By RCS

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	02494h

This register keeps track of the DX9 Constant commands parsed by RCS prior to encountering the Draw Call in an RS enabled Batch Buffer which has DX9 Pool Alloc Valid. DX9 parse count should be less then equal to the DX9 produce count for Command Streamer to make progress on a 3D_PRIMITIVE command. DX9 Parse count is subtracted from the DX9 Produce Count upon parsing 3D_PRIMITIVE command. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0	31:0	**DX9 Constants Produce Count** This register keeps track of the DX9 Constant commands parsed by RCS prior to encountering the Draw Call in an RS enabled Batch Buffer which has DX9 Pool Alloc Valid. DX9 parse count should be less then equal to the DX9 produce count for Command Streamer to make progress on a 3D_PRIMITIVE command. DX9 Parse count is subtracted from the DX9 Produce Count upon parsing 3D_PRIMITIVE command.

CSPREEMPT

CSPREEMPT - CSPREEMPT

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	024B0h

Programming Notes

This is for HW internal usage and must not be written by SW.

DWord	Bit	Description
0	31:16	**Mask Bits** Project: DevHSW+ Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:1	**Reserved** Project: DevHSW+ Format: MBZ
	0	**Unnamed** Project: DevHSW+ Format: Disable This is a message bit written by the cross CS in case of GT4-CBR/SFR mode of operation. To set this bit both bit[0] and bit[16] (mask) needs to be set. This bit set indicates CS in other GT has reached a preemption point. This bit gets reset by CS when preemption takes place.

Context Semaphore Sync Registers

CTX_SEMA_REG - Context Semaphore Sync Registers

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	024B4h-024BBh

This register contains the semaphore value to be compared with the value specified in the MI_SEMAPHORE_MBOX command. These registers gets context save/restored as part of Command Streamer Render Context. The register value in the command will be compared with the MMIO offset specified in the table below:

Register Number	MMIO Offset
32	0x24B4
33	0x24B8

These registers can be accessed by only Render Command Streamer in GTB mode of operation.

DWord	Bit	Description
0	31:0	**Semaphore Data** Semaphore data for synchronization between render engine and video codec engine.

GPGPU Dispatch Dimension X

GPGPU_DISPATCHDIMX - GPGPU Dispatch Dimension X

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02500h

DWord	Bit	Description
0	31:0	**Dispatch Dimension X** Format: U32 The number of thread groups to be dispatched in the X dimension (max x + 1). Value: 1,FFFFFFFFh; Name: ; Project: HSW

GPGPU Dispatch Dimension Y

GPGPU_DISPATCHDIMY - GPGPU Dispatch Dimension Y

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02504h

DWord	Bit	Description
0	31:0	**Dispatch Dimension Y** Format: U32 The number of thread groups to be dispatched in the Y dimension (max y + 1 Value: 1,FFFFFFFFh; Name: ; Project: HSW

GPGPU Dispatch Dimension Z

GPGPU_DISPATCHDIMZ - GPGPU Dispatch Dimension Z

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02508h

DWord	Bit	Description
0	31:0	**Dispatch Dimension Z** Format: U32 The number of thread groups to be dispatched in the Zdimension (max Z + 1) Value: 1,FFFFFFFFh — Name: — Project: HSW

CS General Purpose Registers 0-15

CS_GPR - CS General Purpose Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	02600h-0267Fh

This is a General Purpose Register bank of sixteen 64bit registers, which will be used as temporary storage by MI_MATH command to do ALU operations.

GPR Index	MMIO Offset
R_0	0x2600
R_1	0x2608
R_2	0x2610
R_3	0x2618
R_4	0x2620
R_5	0x2628
R_6	0x2630
R_7	0x2638
R_8	0x2640
R_9	0x2648
R_10	0x2650
R_11	0x2658
R_12	0x2660
R_13	0x2668
R_14	0x2670
R_15	0x2678

DWord	Bit	Description
0	63:0	**CS_GPR_DATA** Project: DevHSW+ This register is a temporary register for ALU operations. See MI_MATH command for more details. CS_GPR_DATA[0] of R_15 is PREDICATE_RESULT_1 and will be looked at by MI_BATCH_BUFFER_START for Predication. Programmer has to ensure that this register is updated only for updating PREDICATE_RESULT_1, when predication is enabled.

Semaphore General Sync Registers

SEMA_REG - Semaphore General Sync Registers

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32

Address: 02680h-02687h

This register contains the semaphore value to be compared with the value specifed in the MI_SEMAPHORE_MBOX command. The register value in the command will be compared with the MMIO offset specifed in the table below:

Register Number	MMIO Offset
0	0x2680
1	0x2684

DWord	Bit	Description
0	31:0	**Semaphore Data** Semaphore data for synchronization between render engine and video codec engine.

Observation Architecture Start Trigger 5

OASTARTTRIG5 - Observation Architecture Start Trigger 5

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02720h

This register provides the threshold value optionally used to define the start trigger for B7-B4 counters. Note that the value in this register must match the value in OASTARTTRIG1 to have B7-B0 start at the same time. The bit definition in this register refers to the stages in the start trigger block diagram in the Performance Counter Reporting section.

DWord	Bit	Description
0	31:16	**Threshold count** Project: HSW Format: U16 **Programming Notes** This field is for HW internal use to context save/restore threshold count that has been achieved. SW should always program this field to Zero when this register is written to.
	15:0	**Threshold Value** Format: U16 **Programming Notes** Threshold value for the compare logic within the start trigger logic for B7-B4 counters.

VF Scratch Pad

VFSKPD - VF Scratch Pad

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02470h
Address:	02740h-02743h
Valid Projects:	HSW

DWord	Bit	Description
0	31:16	**Mask Bits** Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All bits implemented)
	15	**Reserved** Project: HSW Format: MBZ
	14:9	**Reserved** Project: All Format: MBZ
	8	**Reserved** Project: HSW Format: MBZ
	7	**Reserved** Project: HSW Format: MBZ
	6	**Reserved** Project: HSW Format: MBZ
	5	**TLB Prefectch Enable** Project: DevHSW+ Format: U1

VFSKPD - VF Scratch Pad

Value	Name	Description
0h	Disable **[Default]**	The VF will generate prefetch of TLB when it is fetching sequential vertex data and four or fewer vertex buffers are valid.
1h	Enable	VF will disable prefetch of TLB entries.

4 **Reserved**

Project:	HSW
Format:	MBZ

3 **Reserved**

Project:	HSW
Format:	MBZ

2 **Vertex Cache Implicit Disable Inhibit**

Format:	U1

Value	Name	Description
0h	**[Default]**	Allow VF to disable VS0 when Sequential index or Prim ID is a valid Element.
1h		VF never implicitly disables the vertex cache. Software must disable the VS0 Cache when required.

1 **Disable Over Fetch Cache**

Project:	HSW
Format:	MBZ This bit must be '0' always.

0 **Disable Multiple Miss Read squash**

Project:	DevHSW+
Format:	Disable

Value	Name	Description
0h	**[Default]**	Allow VF to squash reads that are to the same cacheline for vertex buffer requests.
1h		Disallow VF from squashing reads that are to the same cacheline for vertex buffer requests.

Observation Architecture Report Trigger 2

OAREPORTTRIG2 - Observation Architecture Report Trigger 2

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02744h
Valid Projects:	[DevHSW+]

Description	Project
This register controls some of the Boolean logic defining Boolean/threshold report trigger 0. The bit definitions in this register refer to the stages in the report trigger block diagram in the Performance Counter Reporting section.	
Report triggers generated from OAREPORTTRIG 1-4 and OAREPORTTRIG 5-8 are ORed to form a new report trigger. Report trigger behavior can be derived by programming these two sets of OA REPORT registers with the same value. Users should be aware that while programming Timer based and Threshold Counter based triggers simultaneously for internal reporting, they should be programmed such way that they are not consecutively triggered. If programmed simultaneously, RTL pulse detection logic will have problem when these triggers occur in consecutive clock cycles.	DevHSW+

DWord	Bit	Description
0	31	**Report Trigger Enable** Format: Enable Enable Boolean/threshold report trigger 0. Users should be aware that the timer-based report logic and the Boolean report trigger logic are logically OR'd together with no buffering of report triggers. This implies that only one performance counter report will be generated for clocks where both the timer-based report logic and the Boolean report trigger logic trigger a performance counter report.
	30:24	**Reserved** Format: MBZ
	23	**Threshold Enable** Format: Enable Enable the threshold compare logic within the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	22	**Invert D Enable 0**

OAREPORTTRIG2 - Observation Architecture Report Trigger 2

		Format: Enable Invert the specified signal at the D stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	21	**Invert C Enable 1** Format: Enable Invert the specified signal at the C stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	20	**Invert C Enable 0** Format: Enable Invert the specified signal at the C stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	19	**Invert B Enable 3** Format: Enable Invert the specified signal at the B stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	18	**Invert B Enable 2** Format: Enable Invert the specified signal at the B stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	17	**Invert B Enable 1** Format: Enable Invert the specified signal at the B stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	16	**Invert B Enable 0** Format: Enable Invert the specified signal at the B stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	15	**Invert A Enable 15** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	14	**Invert A Enable 14**

OAREPORTTRIG2 - Observation Architecture Report Trigger 2

		Format: | Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	13	**Invert A Enable 13** Format: | Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	12	**Invert A Enable 12** Format: | Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	11	**Invert A Enable 11** Format: | Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	10	**Invert A Enable 10** Format: | Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	9	**Invert A Enable 9** Format: | Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	8	**Invert A Enable 8** Format: | Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	7	**Invert A Enable 7** Format: | Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	6	**Invert A Enable 6**

OAREPORTTRIG2 - Observation Architecture Report Trigger 2

		Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	5	**Invert A Enable 5** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	4	**Invert A Enable 4** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	3	**Invert A Enable 3** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	2	**Invert A Enable 2** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	1	**Invert A Enable 1** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	0	**Invert A Enable 0** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).

Observation Architecture Report Trigger 6

OAREPORTTRIG6 - Observation Architecture Report Trigger 6

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02754h

Description	Project
This register controls some of the Boolean logic defining Boolean/threshold report trigger 1. Note that Boolean report triggers 0 and 1 are logically OR'd together without buffering, this implies that only one performance counter report will be generated for clocks where both Boolean report triggers evaluate true. The bit definitions in this register refer to the stages in the report trigger block diagram in the Performance Counter Reporting section.	
Report triggers generated from OAREPORTTRIG 1-4 and OAREPORTTRIG 5-8 are ORed to form a new report trigger. Report trigger behavior can be derived by programming these two sets of OA REPORT registers with the same value. Users should be aware that while programming Timer based and Threshold Counter based triggers simultaneously for internal reporting, they should be programmed such way that they are not consecutively triggered. If programmed simultaneously, RTL pulse detection logic will have problem when these triggers occur in consecutive clock cycles.	DevHSW+

DWord	Bit	Description
0	31	**Report Trigger Enable** Enable Boolean/threshold report trigger 0. Users should be aware that the timer-based report logic and the Boolean report trigger logic are logically OR'd together with no buffering of report triggers. This implies that only one performance counter report will be generated for clocks where both the timer-based report logic and the Boolean report trigger logic trigger a performance counter report.
	30:24	**Reserved** Format: MBZ
	23	**Threshold Enable** Enable the threshold compare logic within the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	22	**Invert D Enable 0** Invert the specified signal at the D stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	21	**Invert C Enable 1** Invert the specified signal at the C stage of the Boolean/threshold report trigger 1 logic (see

OAREPORTTRIG6 - Observation Architecture Report Trigger 6		
		block diagram in the Performance Counter Reporting section).
	20	**Invert C Enable 0** Invert the specified signal at the C stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	19	**Invert B Enable 3** Invert the specified signal at the B stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	18	**Invert B Enable 2** Invert the specified signal at the B stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	17	**Invert B Enable 1** Invert the specified signal at the B stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	16	**Invert B Enable 0** Invert the specified signal at the B stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	15	**Invert A Enable 15** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	14	**Invert A Enable 14** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	13	**Invert A Enable 13** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	12	**Invert A Enable 12** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	11	**Invert A Enable 11** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	10	**Invert A Enable 10** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	9	**Invert A Enable 9** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	8	**Invert A Enable 8** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	7	**Invert A Enable 7**

OAREPORTTRIG6 - Observation Architecture Report Trigger 6		
		Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	6	**Invert A Enable 6** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	5	**Invert A Enable 5** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	4	**Invert A Enable 4** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	3	**Invert A Enable 3** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	2	**Invert A Enable 2** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	1	**Invert A Enable 1** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	0	**Invert A Enable 0** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).

Customizable Event Creation 0-0

CEC0-0 - Customizable Event Creation 0-0

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02770h
Valid Projects:	[DevHSW+]

This register is used to define custom counter event 0, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

<table>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td rowspan="4">0</td><td>31:21</td><td>Reserved
Project: HSW
Format: MBZ</td></tr>
<tr><td>20:19</td><td>Source Select
Format: U2
Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).
<table><tr><th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr><tr><td>01b</td><td>Prev Event</td><td>Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block</td><td>All</td></tr><tr><td>11b</td><td>Reserved</td><td></td><td></td></tr></table></td></tr>
<tr><td>18:3</td><td>Compare Value
Format: U16
The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.</td></tr>
<tr><td>2:0</td><td>Compare Function
Format: U3
This field selects the function used by the CEC0 comparator when comparing the compare value to the value active on the CEC0 conditioned input bus (see block diagram in the Custom Event Counters section).</td></tr>
</table>

CEC0-0 - Customizable Event Creation 0-0

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

Customizable Event Creation 1-0

CEC1-0 - Customizable Event Creation 1-0

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02778h
Valid Projects:	[DevHSW+]

This register is used to define custom counter event 1, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

<table>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td rowspan="4">0</td><td>31:21</td><td>Reserved
Project: HSW
Format: MBZ</td></tr>
<tr><td>20:19</td><td>Source Select
Format: U2
Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).
<table><tr><th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr><tr><td>01b</td><td>Prev Event</td><td>Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block</td><td>All</td></tr><tr><td>11b</td><td>Reserved</td><td></td><td></td></tr></table></td></tr>
<tr><td>18:3</td><td>Compare Value
Format: U16
The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.</td></tr>
<tr><td>2:0</td><td>Compare Function
Format: U3
This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).</td></tr>
</table>

CEC1-0 - Customizable Event Creation 1-0

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

Customizable Event Creation 2-0

CEC2-0 - Customizable Event Creation 2-0

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02780h
Valid Projects:	[DevHSW+]

This register is used to define custom counter event 2, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

<table>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td rowspan="4">0</td><td>31:21</td><td>Reserved
<table>
<tr><td>Project:</td><td>HSW</td></tr>
<tr><td>Format:</td><td>MBZ</td></tr>
</table></td></tr>
<tr><td>20:19</td><td>Source Select
<table>
<tr><td>Format:</td><td>U2</td></tr>
</table>
Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).
<table>
<tr><th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr>
<tr><td>01b</td><td>Prev Event</td><td>Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block</td><td>All</td></tr>
<tr><td>11b</td><td>Reserved</td><td></td><td></td></tr>
</table></td></tr>
<tr><td>18:3</td><td>Compare Value
<table>
<tr><td>Format:</td><td>U16</td></tr>
</table>
The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.</td></tr>
<tr><td>2:0</td><td>Compare Function
<table>
<tr><td>Format:</td><td>U3</td></tr>
</table>
This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).</td></tr>
</table>

CEC2-0 - Customizable Event Creation 2-0

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

Customizable Event Creation 3-0

CEC3-0 - Customizable Event Creation 3-0

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02788h
Valid Projects:	[DevHSW+]

This register is used to define custom counter event 3, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

<table>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td rowspan="4">0</td><td>31:21</td><td>Reserved
<table>
<tr><td>Project:</td><td>HSW</td></tr>
<tr><td>Format:</td><td>MBZ</td></tr>
</table></td></tr>
<tr><td>20:19</td><td>Source Select
<table>
<tr><td>Format:</td><td>U2</td></tr>
</table>
Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).
<table>
<tr><th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr>
<tr><td>01b</td><td>Prev Event</td><td>Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block</td><td>All</td></tr>
<tr><td>11b</td><td>Reserved</td><td></td><td></td></tr>
</table></td></tr>
<tr><td>18:3</td><td>Compare Value
<table>
<tr><td>Format:</td><td>U16</td></tr>
</table>
The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.</td></tr>
<tr><td>2:0</td><td>Compare Function
<table>
<tr><td>Format:</td><td>U3</td></tr>
</table>
This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).</td></tr>
</table>

CEC3-0 - Customizable Event Creation 3-0

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

Aggregate_Perf_Counter_A31

OAPERF_A31 - Aggregate_Perf_Counter_A31	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0278Ch
Valid Projects:	[DevHSW]

This register reflects the count value of the OA Performance counter A31

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Customizable Event Creation 4-0

CEC4-0 - Customizable Event Creation 4-0

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02790h

This register is used to define custom counter event 4, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Reserved** Project: HSW Format: MBZ
	20:19	**Source Select** Format: U2 Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). Value / Name / Description / Project: 01b / Prev Event / Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block / All 11b / Reserved / /
	18:3	**Compare Value** Format: U16 The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.
	2:0	**Compare Function** Format: U3 This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section). Value / Name / Description:

CEC4-0 - Customizable Event Creation 4-0				
		000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
		001b	Greater Than	Compare and assert output if greater than
		010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
		011b	Greater Than or Equal	Compare and assert output if greater than or equal
		100b	Less Than	Compare and assert output if less than
		101b	Not Equal	Compare and assert output if not equal
		110b	Less Than or Equal	Compare and assert output if less than or equal
		111b	Reserved	

Customizable Event Creation 5-0

CEC5-0 - Customizable Event Creation 5-0

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02798h

This register is used to define custom counter event 5, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Reserved** Project: HSW Format: MBZ
	20:19	**Source Select** Format: U2 Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). Value / Name / Description / Project: 01b / Prev Event / Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block / All 11b / Reserved / /
	18:3	**Compare Value** Format: U16 The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.
	2:0	**Compare Function** Format: U3 This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section). Value / Name / Description:

CEC5-0 - Customizable Event Creation 5-0				
		000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
		001b	Greater Than	Compare and assert output if greater than
		010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
		011b	Greater Than or Equal	Compare and assert output if greater than or equal
		100b	Less Than	Compare and assert output if less than
		101b	Not Equal	Compare and assert output if not equal
		110b	Less Than or Equal	Compare and assert output if less than or equal
		111b	Reserved	

Customizable Event Creation 6-0

CEC6-0 - Customizable Event Creation 6-0

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	027A0h

This register is used to define custom counter event 6, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Reserved** Project: HSW Format: MBZ
	20:19	**Source Select** Format: U2 Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). Value / Name / Description / Project: 01b / Prev Event / Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block / All 11b / Reserved / /
	18:3	**Compare Value** Format: U16 The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.
	2:0	**Compare Function** Format: U3 This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section). Value / Name / Description:

CEC6-0 - Customizable Event Creation 6-0				
		000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
		001b	Greater Than	Compare and assert output if greater than
		010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
		011b	Greater Than or Equal	Compare and assert output if greater than or equal
		100b	Less Than	Compare and assert output if less than
		101b	Not Equal	Compare and assert output if not equal
		110b	Less Than or Equal	Compare and assert output if less than or equal
		111b	Reserved	

Customizable Event Creation 7-0

CEC7-0 - Customizable Event Creation 7-0

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	027A8h

This register is used to define custom counter event 7, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Reserved** Project: HSW Format: MBZ
	20:19	**Source Select** Format: U2 Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). Value / Name / Description / Project: 01b / Prev Event / Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block / All 11b / Reserved / /
	18:3	**Compare Value** Format: U16 The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.
	2:0	**Compare Function** Format: U3 This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section). Value / Name / Description:

CEC7-0 - Customizable Event Creation 7-0				
		000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
		001b	Greater Than	Compare and assert output if greater than
		010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
		011b	Greater Than or Equal	Compare and assert output if greater than or equal
		100b	Less Than	Compare and assert output if less than
		101b	Not Equal	Compare and assert output if not equal
		110b	Less Than or Equal	Compare and assert output if less than or equal
		111b	Reserved	

Aggregate Perf Counter A0

OAPERF_A0 - Aggregate Perf Counter A0		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02800h	
This register reflects the count value of the OA Performance counter A0. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A1

OAPERF_A1 - Aggregate Perf Counter A1		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02804h	
Valid Projects:	[DevHSW]	
This register reflects the count value of the OA Performance counter A1. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A2

OAPERF_A2 - Aggregate Perf Counter A2		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02808h	
Valid Projects:	[DevHSW]	
This register reflects the count value of the OA Performance counter A2. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A3

OAPERF_A3 - Aggregate Perf Counter A3		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	0280Ch	
Valid Projects:	[DevHSW]	
This register reflects the count value of the OA Performance counter A3. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A5

OAPERF_A5 - Aggregate Perf Counter A5		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02814h	
Valid Projects:	[DevHSW]	
This register reflects the count value of the OA Performance counter A5. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A7

OAPERF_A7 - Aggregate Perf Counter A7		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	0281Ch	
Valid Projects:	[DevHSW]	
This register reflects the count value of the OA Performance counter A7. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A8

OAPERF_A8 - Aggregate Perf Counter A8		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02820h	
Valid Projects:	[DevHSW]	
This register reflects the count value of the OA Performance counter A8. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A9

OAPERF_A9 - Aggregate Perf Counter A9		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02824h	
Valid Projects:	[DevHSW]	
This register reflects the count value of the OA Performance counter A9. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A10

OAPERF_A10 - Aggregate Perf Counter A10		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02828h	
Valid Projects:	[DevHSW]	
This register reflects the count value of the OA Performance counter A10. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A11

OAPERF_A11 - Aggregate Perf Counter A11		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	0282Ch	
Valid Projects:	[DevHSW]	
This register reflects the count value of the OA Performance counter A11. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A12

OAPERF_A12 - Aggregate Perf Counter A12		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02830h	
Valid Projects:	[DevHSW]	
This register reflects the count value of the OA Performance counter A12. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A13

OAPERF_A13 - Aggregate Perf Counter A13		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02834h	
Valid Projects:	[DevHSW]	
This register reflects the count value of the OA Performance counter A13. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A14

OAPERF_A14 - Aggregate Perf Counter A14		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02838h	
Valid Projects:	[DevHSW]	
This register reflects the count value of the OA Performance counter A14. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A15

OAPERF_A15 - Aggregate Perf Counter A15		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	0283Ch	
Valid Projects:	[DevHSW]	
This register reflects the count value of the OA Performance counter A15. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A16

OAPERF_A16 - Aggregate Perf Counter A16		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02840h	
Valid Projects:	[DevHSW]	
This register reflects the count value of the OA Performance counter A16. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A17

OAPERF_A17 - Aggregate Perf Counter A17		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02844h	
Valid Projects:	[DevHSW]	
This register reflects the count value of the OA Performance counter A17. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A18

OAPERF_A18 - Aggregate Perf Counter A18		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02848h	
Valid Projects:	[DevHSW]	
This register reflects the count value of the OA Performance counter A9. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A21

OAPERF_A21 - Aggregate Perf Counter A21		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02854h	
Valid Projects:	[DevHSW]	
This register reflects the count value of the OA Performance counter A21. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A22

OAPERF_A22 - Aggregate Perf Counter A22		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02858h	
Valid Projects:	[DevHSW]	
This register reflects the count value of the OA Performance counter A22. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A23

OAPERF_A23 - Aggregate Perf Counter A23		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	0285Ch	
Valid Projects:	[DevHSW]	
This register reflects the count value of the OA Performance counter A23. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A24

OAPERF_A24 - Aggregate Perf Counter A24		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02860h	
Valid Projects:	[DevHSW]	
This register reflects the count value of the OA Performance counter A24. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A25

OAPERF_A25 - Aggregate Perf Counter A25		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02864h	
Valid Projects:	[DevHSW]	
This register reflects the count value of the OA Performance counter A25. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A26

OAPERF_A26 - Aggregate Perf Counter A26		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02868h	
Valid Projects:	[DevHSW]	
This register reflects the count value of the OA Performance counter A26. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A27

OAPERF_A27 - Aggregate Perf Counter A27		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	0286Ch	
Valid Projects:	[DevHSW]	
This register reflects the count value of the OA Performance counter A27. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A28

OAPERF_A28 - Aggregate Perf Counter A28		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02870h	
Valid Projects:	[DevHSW]	
This register reflects the count value of the OA Performance counter A28. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A29

OAPERF_A29 - Aggregate Perf Counter A29		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02874h	
Valid Projects:	[DevHSW]	
This register reflects the count value of the OA Performance counter A29. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A30

OAPERF_A30 - Aggregate Perf Counter A30		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02878h	
Valid Projects:	[DevHSW]	
This register reflects the count value of the OA Performance counter A30. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate_Perf_Counter_A32

OAPERF_A32 - Aggregate_Perf_Counter_A32		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02880h	
Valid Projects:	[DevHSW]	
This register reflects the count value of the OA Performance counter A32		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate_Perf_Counter_A33

OAPERF_A33 - Aggregate_Perf_Counter_A33	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02884h
Valid Projects:	[DevHSW]

This register reflects the count value of the OA Performance counter A33

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate_Perf_Counter_A34

OAPERF_A34 - Aggregate_Perf_Counter_A34	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02888h
Valid Projects:	[DevHSW]

This register reflects the count value of the OA Performance counter A34

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate_Perf_Counter_A35

OAPERF_A35 - Aggregate_Perf_Counter_A35		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	0288Ch	
Valid Projects:	[DevHSW]	
This register reflects the count value of the OA Performance counter A35		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate_Perf_Counter_A36

OAPERF_A36 - Aggregate_Perf_Counter_A36	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02890h
Valid Projects:	[DevHSW]

This register reflects the count value of the OA Performance counter A36

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate_Perf_Counter_A38

OAPERF_A38 - Aggregate_Perf_Counter_A38	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02898h
Valid Projects:	[DevHSW]

This register reflects the count value of the OA Performance counter A38

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate_Perf_Counter_A40

OAPERF_A40 - Aggregate_Perf_Counter_A40		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	028A0h	
Valid Projects:	[DevHSW]	
This register reflects the count value of the OA Performance counter A40		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate_Perf_Counter_A42

OAPERF_A42 - Aggregate_Perf_Counter_A42	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028A8h
Valid Projects:	[DevHSW]

This register reflects the count value of the OA Performance counter A42

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate_Perf_Counter_A43

OAPERF_A43 - Aggregate_Perf_Counter_A43		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	028ACh	
Valid Projects:	[DevHSW]	
This register reflects the count value of the OA Performance counter A43		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate_Perf_Counter_A44

OAPERF_A44 - Aggregate_Perf_Counter_A44	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028B0h
Valid Projects:	[DevHSW]

This register reflects the count value of the OA Performance counter A44

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Boolean_Counter_B0

OAPERF_B0 - Boolean_Counter_B0	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028B4h
Valid Projects:	[DevHSW]

This register enables the current live value of performance counter B0 to be read. Since what conditions cause B0 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Boolean_Counter_B1

OAPERF_B1 - Boolean_Counter_B1	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028B8h
Valid Projects:	[DevHSW]

This register enables the current live value of performance counter B1 to be read. Since what conditions cause B1 to increment are defined by the programming of CEC1-0/CEC1-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Boolean_Counter_B2

OAPERF_B2 - Boolean_Counter_B2	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028BCh
Valid Projects:	[DevHSW]

This register enables the current live value of performance counter B2 to be read. Since what conditions cause B2 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Boolean_Counter_B3

OAPERF_B3 - Boolean_Counter_B3	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028C0h
Valid Projects:	[DevHSW]

This register enables the current live value of performance counter B3 to be read. Since what conditions cause B3 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Boolean_Counter_B4

OAPERF_B4 - Boolean_Counter_B4	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028C4h
Valid Projects:	[DevHSW]

This register enables the current live value of performance counter B4 to be read. Since what conditions cause B4 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Boolean_Counter_B5

OAPERF_B5 - Boolean_Counter_B5	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028C8h
Valid Projects:	[DevHSW]

This register enables the current live value of performance counter B5 to be read. Since what conditions cause B5 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Boolean_Counter_B6

OAPERF_B6 - Boolean_Counter_B6	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028CCh
Valid Projects:	[DevHSW]

This register enables the current live value of performance counter B6 to be read. Since what conditions cause B6 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Boolean_Counter_B7

OAPERF_B7 - Boolean_Counter_B7	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028D0h
Valid Projects:	[DevHSW]

This register enables the current live value of performance counter B7 to be read. Since what conditions cause B7 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Depth/Early Depth TLB Partitioning Register

ZSHR - Depth/Early Depth TLB Partitioning Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000020
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	04050h

This register is used to determine the number of TLB entries from the total of 64 available to be used by the Depth partition of the TLB. The rest of the entries are used for the Early Depth/Stencil TLB.

DWord	Bit	Description
0	31:6	**Reserved** Format: MBZ
	5:0	**Number of TLB Entries Out of 64 used for Depth TLB** Default Value: 32 The rest are be used for Early Depth/Stencil TLB. Default value is 32.

Color/Depth Write FIFO Watermarks

CZWMRK - Color/Depth Write FIFO Watermarks

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	04060h

This register is directly mapped to the current Virtual Addresses in the MTTLB (Texture and constant cache TLB).

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:18	**Color Wr Burst Size** This is the maximum size of the requests burst, from the last High Watermark trip, before reevaluating the High Watermark again.
	17:16	**Reserved** Format: MBZ
	15:12	**Color Wr FIFO High Watermark** This is the number of accumulated Color writes that will trigger a Burst of Z Writes.
	11:6	**Z Wr Burst Size** This is the maximum size of the requests burst, from the last High Watermark trip, before reevaluating the High Watermark again.
	5:4	**Reserved** Format: MBZ
	3:0	**Z Wr FIFO High Watermark** This is the number of accumulated Depth writes that will trigger a Burst of Z Writes.

Main Graphic ECO Chicken Register

ECOCHK - Main Graphic ECO Chicken Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Default Value:	0x00000000
Size (in bits):	32
Address:	04090h-04093h

DWord	Bit	Description
0	31:15	**Bits Reserved for Future ECOs** Default Value: 00000000000000000000000000b Access: R/W
	14	**Global Page Fault Enable** Default Value: 0b Access: R/W Enables the fault & behavior for page faulted accesses.
	13:11	**Reserved** Default Value: 0b Access: R/W
	10	**Enable same PAT hold** Default Value: 0b Access: R/W Enable same PAT hold on B2B requests, according to setting on bit 9
	9	**Disable Same Pat hold** Default Value: 0b Access: R/W Disable new Same Pat hold for non present cycles condition. If 1, generate hold on any b2b same PAT request to midarb; If 0, generate hold on any b2b same PAT, only if thread being served in TLBPEND is to this same PAT.
	8	**Disable TLBs** Default Value: 0b Access: R/W TLBPEND collision check fix

ECOCHK - Main Graphic ECO Chicken Register

7	**Bypass Fence** Default Value: 0b Access: R/W Completely bypass the requirement to flush GAFM and GAPC on any fence/allow graphics disable event
6	**Arbitration priority order between SOL and VF** Default Value: 0b Access: R/W (gam_gafm_csr_sol_vf_pri)0 : Default setting; SOL < VF (i.e., VF has higher priority, vs. SOL) 1: SOL > VF (i.e., SOL has higher priority, vs. VF) Note: The CSunit has highest priority over VF and SOL in the GAFM, and only the relative priority of VF vs SOL is programmable.
5	**Register Fence Ack Chicken** Default Value: 0b Access: R/W In case of a GFX fence. Wait for fence to be out of GAM to send ack back to CS. Otherwise,wait only for GAPC flush.
4:3	**PPGTT Cacheability Override** Default Value: 00b Access: R/W 00 No override. ---- 01 UC (LLC/eLLC) – allocation age is don't care 0000 10 WT in LLC/eLLC – Aged "3" 0111 11 WB in LLC/eLLC – Aged "3" 1000
2:1	**Reserved** Access: R/W
0	**Reg No Flsh On Allow Done** Default Value: 0b

ECOCHK - Main Graphic ECO Chicken Register			
		Access:	R/W
		Force done signals to 1 when allow GFX is 0, and FSM is in done state. This will bypass the requirement to flush GAFM and GAPC on a cascaded special fence.	

Private PAT

PRIV_PAT - Private PAT

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	040E8h

DWord	Bit	Description
0	31:0	**Private PAT** Default Value: 00000000h Access: R/W Bit[31:16]: Reserved. Bit[15:8]: PPGTT Private PAT. (See bit[7:0] for definition.) Bit[7:6]: Reserved. Bit[5:4]: (See below.) 00b: Age is 0. 01b: Age is 1. 10b: Age is 2. 11b: Age is 3. Bit[3:2]: (See below.) 00b: Override to eLLC Only. (This setting overrides the memory_object_control_state via surface state to be eLLC target only.) 01b: eLLC only. 10b: LLC only. 11b: eLLC/LLC. Bit[1:0]: (see below): 00b: Uncached with fence. 01b: Write Combining (traditional UC). 10b: Write Through. 11b: Write Back.

Priority Field in Programmable Arbitration for Miss

MIDARB_PRIO_MISS_REGISTER - Priority Field in Programmable Arbitration for Miss		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	04204h	
DWord	**Bit**	**Description**
0	31:20	**Reserved**
	19:15	**Encoded Programmable Priority for MIDARB_GOTOFIELD_MISS3 Register**
	14:10	**Encoded Programmable Priority for MIDARB_GOTOFIELD_MISS2 Register**
	9:5	**Encoded Programmable Priority for MIDARB_GOTOFIELD_MISS1 Register**
	4:0	**Encoded Programmable Priority for MIDARB_GOTOFIELD_MISS0 Register**

Priority Field in Programmable Arbitration for Hit-NP

MIDARB_PRIO_NP_REGISTER - Priority Field in Programmable Arbitration for Hit-NP

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1

Address:	043A4h
Valid Projects:	HSW

Address:	04208h
Valid Projects:	HSW

DWord	Bit	Description
0	31:20	**Reserved**
	19:15	**Encoded Programmable Priority for MIDARB_GOTOFIELD_MISS3 Register**

Encoding	Priority 1	Priority 2	Priority 3	Priority 4
00000	CS/VF/ISC	MT_CTC	RCC	RCZ_HiZ_Stnc
00001	CS/VF/ISC	RCC	MT_CTC	RCZ_HiZ_Stnc
00010	RCC	CS/VF/ISC	MT_CTC	RCZ_HiZ_Stnc
00011	RCC	MT_CTC	CS/VF/ISC	RCZ_HiZ_Stnc
00100	MT_CTC	CS/VF/ISC	RCC	RCZ_HiZ_Stnc
00101	MT_CTC	RCC	CS/VF/ISC	RCZ_HiZ_Stnc
01000	CS/VF/ISC	MT_CTC	RCZ_HiZ_Stnc	RCC
01001	CS/VF/ISC	RCC	RCZ_HiZ_Stnc	MT_CTC
01010	RCC	CS/VF/ISC	RCZ_HiZ_Stnc	MT_CTC
01011	RCC	MT_CTC	RCZ_HiZ_Stnc	CS/VF/ISC
01100	MT_CTC	CS/VF/ISC	RCZ_HiZ_Stnc	RCC
01101	MT_CTC	RCC	RCZ_HiZ_Stnc	CS/VF/ISC
10000	CS/VF/ISC	RCZ_HiZ_Stnc	MT_CTC	RCC
10001	CS/VF/ISC	RCZ_HiZ_Stnc	RCC	MT_CTC
10010	RCC	RCZ_HiZ_Stnc	CS/VF/ISC	MT_CTC
10011	RCC	RCZ_HiZ_Stnc	MT_CTC	CS/VF/ISC

MIDARB_PRIO_NP_REGISTER - Priority Field in Programmable Arbitration for Hit-NP

		10100	MT_CTC	RCZ_HiZ_Stnc	CS/VF/ISC	RCC
		10101	MT_CTC	RCZ_HiZ_Stnc	RCC	CS/VF/ISC
		11000	RCZ_HiZ_Stnc	CS/VF/ISC	MT_CTC	RCC
		11001	RCZ_HiZ_Stnc	CS/VF/ISC	RCC	MT_CTC
		11010	RCZ_HiZ_Stnc	RCC	CS/VF/ISC	MT_CTC
		11011	RCZ_HiZ_Stnc	RCC	MT_CTC	CS/VF/ISC
		11100	RCZ_HiZ_Stnc	MT_CTC	CS/VF/ISC	RCC
		11101	RCZ_HiZ_Stnc	MT_CTC	RCC	CS/VF/ISC
		Other values	Reserved			
	14:10	**Encoded Programmable Priority for MIDARB_GOTOFIELD_NP2 Register**				
	9:5	**Encoded Programmable Priority for MIDARB_GOTOFIELD_NP1 Register**				
	4:0	**Encoded Programmable Priority for MIDARB_GOTOFIELD_NP0 Register**				

Priority Field in Programmable Arbitration for Hit

MIDARB_PRIO_HIT_REGISTER - Priority Field in Programmable Arbitration for Hit

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	043A0h

<table>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td>0</td><td>31:12</td><td>Reserved</td></tr>
<tr><td></td><td>11:9</td><td>Encoded Programmable Priority for MIDARB_GOTOFIELD_HIT3 Register
<table>
<tr><th>Encoding</th><th>Priority 1</th><th>Priority 2</th><th>Priority 3</th></tr>
<tr><td>000</td><td>CS/VF/ISC</td><td>MT/CTC</td><td>RCC</td></tr>
<tr><td>001</td><td>CS/VF/ISC</td><td>RCC</td><td>MT/CTC</td></tr>
<tr><td>010</td><td>RCC</td><td>CS/VF/ISC</td><td>MT/CTC</td></tr>
<tr><td>011</td><td>RCC</td><td>MT/CTC</td><td>CS/VF/ISC</td></tr>
<tr><td>100</td><td>MT/CTC</td><td>CS/VF/ISC</td><td>RCC</td></tr>
<tr><td>101</td><td>MT/CTC</td><td>RCC</td><td>CS/VF/ISC</td></tr>
<tr><td>110</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>111</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td></td><td>8:6</td><td>Encoded Programmable Priority for MIDARB_GOTOFIELD_HIT2 Register</td></tr>
<tr><td></td><td>5:3</td><td>Encoded Programmable Priority for MIDARB_GOTOFIELD_HIT1 Register</td></tr>
<tr><td></td><td>2:0</td><td>Encoded Programmable Priority for MIDARB_GOTOFIELD_HIT0 Register</td></tr>
</table>

Priority Field in Programmable Arbitration for Hit-NP

MIDARB_PRIO_NP_REGISTER - Priority Field in Programmable Arbitration for Hit-NP

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	043A4h
Valid Projects:	HSW
Address:	04208h
Valid Projects:	HSW

DWord	Bit	Description
0	31:20	**Reserved**
	19:15	**Encoded Programmable Priority for MIDARB_GOTOFIELD_MISS3 Register**

Encoding	Priority 1	Priority 2	Priority 3	Priority 4
00000	CS/VF/ISC	MT_CTC	RCC	RCZ_HiZ_Stnc
00001	CS/VF/ISC	RCC	MT_CTC	RCZ_HiZ_Stnc
00010	RCC	CS/VF/ISC	MT_CTC	RCZ_HiZ_Stnc
00011	RCC	MT_CTC	CS/VF/ISC	RCZ_HiZ_Stnc
00100	MT_CTC	CS/VF/ISC	RCC	RCZ_HiZ_Stnc
00101	MT_CTC	RCC	CS/VF/ISC	RCZ_HiZ_Stnc
01000	CS/VF/ISC	MT_CTC	RCZ_HiZ_Stnc	RCC
01001	CS/VF/ISC	RCC	RCZ_HiZ_Stnc	MT_CTC
01010	RCC	CS/VF/ISC	RCZ_HiZ_Stnc	MT_CTC
01011	RCC	MT_CTC	RCZ_HiZ_Stnc	CS/VF/ISC
01100	MT_CTC	CS/VF/ISC	RCZ_HiZ_Stnc	RCC
01101	MT_CTC	RCC	RCZ_HiZ_Stnc	CS/VF/ISC
10000	CS/VF/ISC	RCZ_HiZ_Stnc	MT_CTC	RCC
10001	CS/VF/ISC	RCZ_HiZ_Stnc	RCC	MT_CTC
10010	RCC	RCZ_HiZ_Stnc	CS/VF/ISC	MT_CTC
10011	RCC	RCZ_HiZ_Stnc	MT_CTC	CS/VF/ISC

MIDARB_PRIO_NP_REGISTER - Priority Field in Programmable Arbitration for Hit-NP

		10100 MT_CTC RCZ_HiZ_Stnc CS/VF/ISC RCC 10101 MT_CTC RCZ_HiZ_Stnc RCC CS/VF/ISC 11000 RCZ_HiZ_Stnc CS/VF/ISC MT_CTC RCC 11001 RCZ_HiZ_Stnc CS/VF/ISC RCC MT_CTC 11010 RCZ_HiZ_Stnc RCC CS/VF/ISC MT_CTC 11011 RCZ_HiZ_Stnc RCC MT_CTC CS/VF/ISC 11100 RCZ_HiZ_Stnc MT_CTC CS/VF/ISC RCC 11101 RCZ_HiZ_Stnc MT_CTC RCC CS/VF/ISC Other values Reserved
	14:10	**Encoded Programmable Priority for MIDARB_GOTOFIELD_NP2 Register**
	9:5	**Encoded Programmable Priority for MIDARB_GOTOFIELD_NP1 Register**
	4:0	**Encoded Programmable Priority for MIDARB_GOTOFIELD_NP0 Register**

GAC_GAM Arbitration Counters Register 0

ARB_GAC_GAM_REQCNTS0 - GAC_GAM Arbitration Counters Register 0		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043A8h	
DWord	**Bit**	**Description**
0	31:22	**Reserved**
	21:16	**Number of GAC WR requests to be accumulated before applying the arbitration**
	15:14	**Reserved**
	13:8	**Number of GAC R requests to be accumulated before applying the arbitration**
	7:6	**Reserved**
	5:0	**Number of GAC RO requests to be accumulated before applying the arbitration**

GAC_GAM Arbitration Counters Register 1

ARB_GAC_GAM_REQCNTS1 - GAC_GAM Arbitration Counters Register 1		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043ACh	
DWord	**Bit**	**Description**
0	31:22	**Reserved**
	21:16	**Number of GAC WR requests to be accumulated before applying the arbitration**
	15:14	**Reserved**
	13:8	**Number of GAC R requests to be accumulated before applying the arbitration**
	7:6	**Reserved**
	5:0	**Number of GAC RO requests to be accumulated before applying the arbitration**

Goto Field in Programmable Arbitration for Hit0

MIDARB_GOTOFIELD_HIT0 - Goto Field in Programmable Arbitration for Hit0

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	043B0h

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:14	**Goto field when request vector is 111** Determines the GOTO and priority register to be used next: Value / Name / Description 00b / / Use MIDARB_GOTOFIELD_HIT0 and MIDARB_PRIO_HIT_REGISTER[2:0] 01b / / Use MIDARB_GOTOFIELD_HIT1 and MIDARB_PRIO_HIT_REGISTER[5:3] 10b / / Use MIDARB_GOTOFIELD_HIT2 and MIDARB_PRIO_HIT_REGISTER[8:6] 11b / / Use MIDARB_GOTOFIELD_HIT3 and MIDARB_PRIO_HIT_REGISTER[11:9]
	13:12	**Goto field when request vector is 110b.**
	11:10	**Goto field when request vector is 101b.**
	9:8	**Goto field when request vector is 100b.**
	7:6	**Goto field when request vector is 011b.**
	5:4	**Goto field when request vector is 010b.**
	3:2	**Goto field when request vector is 001b.**
	1:0	**Goto field when request vector is 000b.**

Goto Field in Programmable Arbitration for Hit1

MIDARB_GOTOFIELD_HIT1 - Goto Field in Programmable Arbitration for Hit1

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	043B4h

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:14	**Goto field when request vector is 111** Determines the GOTO and priority register to be used next Value / Name / Description: 00b: Use MIDARB_GOTOFIELD_HIT0 and MIDARB_PRIO_HIT_REGISTER[2:0] 01b: Use MIDARB_GOTOFIELD_HIT1 and MIDARB_PRIO_HIT_REGISTER[5:3] 10b: Use MIDARB_GOTOFIELD_HIT2 and MIDARB_PRIO_HIT_REGISTER[8:6] 11b: Use MIDARB_GOTOFIELD_HIT3 and MIDARB_PRIO_HIT_REGISTER[11:9]
	13:12	**Goto field when request vector is 110b.**
	11:10	**Goto field when request vector is 101b.**
	9:8	**Goto field when request vector is 100b.**
	7:6	**Goto field when request vector is 011b.**
	5:4	**Goto field when request vector is 010b.**
	3:2	**Goto field when request vector is 001b.**
	1:0	**Goto field when request vector is 000b.**

Goto Field in Programmable Arbitration for Hit2

MIDARB_GOTOFIELD_HIT2 - Goto Field in Programmable Arbitration for Hit2

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	043B8h

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:14	**Goto field when request vector is 111.** Determines the GOTO and priority register to be used next Value / Name / Description: 00b / Use MIDARB_GOTOFIELD_HIT0 and MIDARB_PRIO_HIT_REGISTER[2:0] 01b / Use MIDARB_GOTOFIELD_HIT1 and MIDARB_PRIO_HIT_REGISTER[5:3] 10b / Use MIDARB_GOTOFIELD_HIT2 and MIDARB_PRIO_HIT_REGISTER[8:6] 11b / Use MIDARB_GOTOFIELD_HIT3 and MIDARB_PRIO_HIT_REGISTER[11:9]
	13:12	**Goto field when request vector is 110b.**
	11:10	**Goto field when request vector is 101b.**
	9:8	**Goto field when request vector is 100b.**
	7:6	**Goto field when request vector is 011b.**
	5:4	**Goto field when request vector is 010b.**
	3:2	**Goto field when request vector is 001b.**
	1:0	**Goto field when request vector is 000b.**

Goto Field in Programmable Arbitration for Hit3

MIDARB_GOTOFIELD_HIT3 - Goto Field in Programmable Arbitration for Hit3

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	043BCh

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:14	**Goto field when request vector is 111.** Determines the GOTO and priority register to be used next. Field for arbitration on next clock cycle for request entries of 111 corresponding to arbitration action field entry of MIDARB_PRIO_HIT_REGISTER[11:9]
	13:12	**Goto field when request vector is 110.** Field for arbitration on next clock cycle for request entries of 110 corresponding to arbitration action field entry of MIDARB_PRIO_HIT_REGISTER[11:9]
	11:10	**Goto field when request vector is 101.** Field for arbitration on next clock cycle for request entries of 101 corresponding to arbitration action field entry of MIDARB_PRIO_HIT_REGISTER[11:9]
	9:8	**Goto field when request vector is 100.** Field for arbitration on next clock cycle for request entries of 100 corresponding to arbitration action field entry of MIDARB_PRIO_HIT_REGISTER[11:9]
	7:6	**Goto field when request vector is 011.** Field for arbitration on next clock cycle for request entries of 011 corresponding to arbitration action field entry of MIDARB_PRIO_HIT_REGISTER[11:9]
	5:4	**Goto field when request vector is 010.**

Value	Name	Description
00b		Use MIDARB_GOTOFIELD_HIT0 and MIDARB_PRIO_HIT_REGISTER[2:0]
01b		Use MIDARB_GOTOFIELD_HIT1 and MIDARB_PRIO_HIT_REGISTER[5:3]
10b		Use MIDARB_GOTOFIELD_HIT2 and MIDARB_PRIO_HIT_REGISTER[8:6]
11b		Use MIDARB_GOTOFIELD_HIT3 and MIDARB_PRIO_HIT_REGISTER[11:9]

MIDARB_GOTOFIELD_HIT3 - Goto Field in Programmable Arbitration for Hit3		
		Field for arbitration on next clock cycle for request entries of 010 corresponding to arbitration action field entry of MIDARB_PRIO_HIT_REGISTER[11:9]
	3:2	**Goto field when request vector is 001.** Field for arbitration on next clock cycle for request entries of 001 corresponding to arbitration action field entry of MIDARB_PRIO_HIT_REGISTER[11:9]
	1:0	**Goto field when request vector is 000.** Field for arbitration on next clock cycle for request entries of 000 corresponding to arbitration action field entry of MIDARB_PRIO_HIT_REGISTER[11:9]

Goto Field in Programmable Arbitration for Hit-NP0

MIDARB_GOTOFIELD_NP0 - Goto Field in Programmable Arbitration for Hit-NP0

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	043C0h

DWord	Bit	Description
0	31:30	**Goto field when request vector is 1111.** Determines the GOTO and priority register to be used next. Value / Name / Description: 00b — Use MIDARB_GOTOFIELD_NP0 and MIDARB_PRIO_NP_REGISTER[4:0] 01b — Use MIDARB_GOTOFIELD_NP1 and MIDARB_PRIO_NP_REGISTER[9:5] 10b — Use MIDARB_GOTOFIELD_NP2 and MIDARB_PRIO_NP_REGISTER[14:10] 11b — Use MIDARB_GOTOFIELD_NP3 and MIDARB_PRIO_NP_REGISTER[19:15]
	29:28	**Goto field when request vector is 1110b.**
	27:26	**Goto field when request vector is 1101b.**
	25:24	**Goto field when request vector is 1100b.**
	23:22	**Goto field when request vector is 1011b.**
	21:20	**Goto field when request vector is 1010b.**
	19:18	**Goto field when request vector is 1001b.**
	17:16	**Goto field when request vector is 1000b.**
	15:14	**Goto field when request vector is 0111b.**
	13:12	**Goto field when request vector is 0110b.**
	11:10	**Goto field when request vector is 0101b.**
	9:8	**Goto field when request vector is 0100b.**
	7:6	**Goto field when request vector is 0011b.**
	5:4	**Goto field when request vector is 0010b.**
	3:2	**Goto field when request vector is 0001b.**
	1:0	**Goto field when request vector is 0000b.**

Goto Field in Programmable Arbitration for Hit-NP1

MIDARB_GOTOFIELD_NP1 - Goto Field in Programmable Arbitration for Hit-NP1

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	043C4h

DWord	Bit	Description
0	31:30	**Goto field when request vector is 1111.** Determines the GOTO and priority register to be used next. Value / Name / Description: 00b — Use MIDARB_GOTOFIELD_NP0 and MIDARB_PRIO_NP_REGISTER[4:0] 01b — Use MIDARB_GOTOFIELD_NP1 and MIDARB_PRIO_NP_REGISTER[9:5] 10b — Use MIDARB_GOTOFIELD_NP2 and MIDARB_PRIO_NP_REGISTER[14:10] 11b — Use MIDARB_GOTOFIELD_NP3 and MIDARB_PRIO_NP_REGISTER[19:15]
	29:28	**Goto field when request vector is 1110b.**
	27:26	**Goto field when request vector is 1101b.**
	25:24	**Goto field when request vector is 1100b.**
	23:22	**Goto field when request vector is 1011b.**
	21:20	**Goto field when request vector is 1010b.**
	19:18	**Goto field when request vector is 1001b.**
	17:16	**Goto field when request vector is 1000b.**
	15:14	**Goto field when request vector is 0111b.**
	13:12	**Goto field when request vector is 0110b.**
	11:10	**Goto field when request vector is 0101b.**
	9:8	**Goto field when request vector is 0100b.**
	7:6	**Goto field when request vector is 0011b.**
	5:4	**Goto field when request vector is 0010b.**
	3:2	**Goto field when request vector is 0001b.**
	1:0	**Goto field when request vector is 0000b.**

Goto Field in Programmable Arbitration for Hit-NP2

MIDARB_GOTOFIELD_NP2 - Goto Field in Programmable Arbitration for Hit-NP2

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	043C8h

DWord	Bit	Description
0	31:30	**Goto field when request vector is 1111.** Determines the GOTO and priority register to be used next. Value / Name / Description: 00b — Use MIDARB_GOTOFIELD_NP0 and MIDARB_PRIO_NP_REGISTER[4:0] 01b — Use MIDARB_GOTOFIELD_NP1 and MIDARB_PRIO_NP_REGISTER[9:5] 10b — Use MIDARB_GOTOFIELD_NP2 and MIDARB_PRIO_NP_REGISTER[14:10] 11b — Use MIDARB_GOTOFIELD_NP3 and MIDARB_PRIO_NP_REGISTER[19:15]
	29:28	**Goto field when request vector is 1110b.**
	27:26	**Goto field when request vector is 1101b.**
	25:24	**Goto field when request vector is 1100b.**
	23:22	**Goto field when request vector is 1011b.**
	21:20	**Goto field when request vector is 1010b.**
	19:18	**Goto field when request vector is 1001b.**
	17:16	**Goto field when request vector is 1000b.**
	15:14	**Goto field when request vector is 0111b.**
	13:12	**Goto field when request vector is 0110b.**
	11:10	**Goto field when request vector is 0101b.**
	9:8	**Goto field when request vector is 0100b.**
	7:6	**Goto field when request vector is 0011b.**
	5:4	**Goto field when request vector is 0010b.**
	3:2	**Goto field when request vector is 0001b.**
	1:0	**Goto field when request vector is 0000b.**

Goto Field in Programmable Arbitration for Hit-NP3

MIDARB_GOTOFIELD_NP3 - Goto Field in Programmable Arbitration for Hit-NP3

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	043CCh

DWord	Bit	Description
0	31:30	**Goto field when request vector is 1111.** Determines the GOTO and priority register to be used next. Value / Name / Description: 00b — Use MIDARB_GOTOFIELD_NP0 and MIDARB_PRIO_NP_REGISTER[4:0] 01b — Use MIDARB_GOTOFIELD_NP1 and MIDARB_PRIO_NP_REGISTER[9:5] 10b — Use MIDARB_GOTOFIELD_NP2 and MIDARB_PRIO_NP_REGISTER[14:10] 11b — Use MIDARB_GOTOFIELD_NP3 and MIDARB_PRIO_NP_REGISTER[19:15]
	29:28	**Goto field when request vector is 1110b.**
	27:26	**Goto field when request vector is 1101b.**
	25:24	**Goto field when request vector is 1100b.**
	23:22	**Goto field when request vector is 1011b.**
	21:20	**Goto field when request vector is 1010b.**
	19:18	**Goto field when request vector is 1001b.**
	17:16	**Goto field when request vector is 1000b.**
	15:14	**Goto field when request vector is 0111b.**
	13:12	**Goto field when request vector is 0110b.**
	11:10	**Goto field when request vector is 0101b.**
	9:8	**Goto field when request vector is 0100b.**
	7:6	**Goto field when request vector is 0011b.**
	5:4	**Goto field when request vector is 0010b.**
	3:2	**Goto field when request vector is 0001b.**
	1:0	**Goto field when request vector is 0000b.**

GAC_GAM RO Arbitration Register 0

ARB_RO_GAC_GAM0 - GAC_GAM RO Arbitration Register 0	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	043D0h

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 1**
	26:24	**Goto field for entry 1 when request vector is 11b**
	23:21	**Goto field for entry 1 when request vector is 10b**
	20:18	**Goto field for entry 1 when request vector is 01b**
	17:15	**Goto field for entry 1 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 01**
	11:9	**Goto field for entry 01 when request vector is 11b**
	8:6	**Goto field for entry 01 when request vector is 10b**
	5:3	**Goto field for entry 01 when request vector is 01b**
	2:0	**Goto field for entry 01 when request vector is 00b**

GAC_GAM RO Arbitration Register 1

ARB_RO_GAC_GAM1 - GAC_GAM RO Arbitration Register 1		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043D4h	
DWord	**Bit**	**Description**
0	31:28	**Reserved**
	27	**Priority for entry 3**
	26:24	**Goto field for entry 3 when request vector is 11b**
	23:21	**Goto field for entry 3 when request vector is 10b**
	20:18	**Goto field for entry 3 when request vector is 01b**
	17:15	**Goto field for entry 3 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 2**
	11:9	**Goto field for entry 2 when request vector is 11b**
	8:6	**Goto field for entry 2 when request vector is 10b**
	5:3	**Goto field for entry 2 when request vector is 01b**
	2:0	**Goto field for entry 2 when request vector is 00b**

GAC_GAM RO Arbitration Register 2

ARB_RO_GAC_GAM2 - GAC_GAM RO Arbitration Register 2	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	043D8h

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 5**
	26:24	**Goto field for entry 5 when request vector is 11b**
	23:21	**Goto field for entry 5 when request vector is 10b**
	20:18	**Goto field for entry 5 when request vector is 01b**
	17:15	**Goto field for entry 5 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 4**
	11:9	**Goto field for entry 4 when request vector is 11b**
	8:6	**Goto field for entry 4 when request vector is 10b**
	5:3	**Goto field for entry 4 when request vector is 01b**
	2:0	**Goto field for entry 4 when request vector is 00b**

GAC_GAM RO Arbitration Register 3

ARB_RO_GAC_GAM3 - GAC_GAM RO Arbitration Register 3		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043DCh	
DWord	**Bit**	**Description**
0	31:28	**Reserved**
	27	**Priority for entry 7**
	26:24	**Goto field for entry 7 when request vector is 11b**
	23:21	**Goto field for entry 7 when request vector is 10b**
	20:18	**Goto field for entry 7 when request vector is 01b**
	17:15	**Goto field for entry 7 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 6**
	11:9	**Goto field for entry 6 when request vector is 11b**
	8:6	**Goto field for entry 6 when request vector is 10b**
	5:3	**Goto field for entry 6 when request vector is 01b**
	2:0	**Goto field for entry 6 when request vector is 00b**

GAC_GAM R Arbitration Register 0

ARB_R_GAC_GAM0 - GAC_GAM R Arbitration Register 0	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	043E0h

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 1**
	26:24	**Goto field for entry 1 when request vector is 11b**
	23:21	**Goto field for entry 1 when request vector is 10b**
	20:18	**Goto field for entry 1 when request vector is 01b**
	17:15	**Goto field for entry 1 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 0**
	11:9	**Goto field for entry 0 when request vector is 11b**
	8:6	**Goto field for entry 0 when request vector is 10b**
	5:3	**Goto field for entry 0 when request vector is 01b**
	2:0	**Goto field for entry 0 when request vector is 00b**

GAC_GAM R Arbitration Register 1

ARB_R_GAC_GAM1 - GAC_GAM R Arbitration Register 1		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043E4h	
DWord	**Bit**	**Description**
0	31:28	**Reserved**
	27	**Priority for entry 3**
	26:24	**Goto field for entry 3 when request vector is 11b**
	23:21	**Goto field for entry 3 when request vector is 10b**
	20:18	**Goto field for entry 3 when request vector is 01b**
	17:15	**Goto field for entry 3 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 2**
	11:9	**Goto field for entry 2 when request vector is 11b**
	8:6	**Goto field for entry 2 when request vector is 10b**
	5:3	**Goto field for entry 2 when request vector is 01b**
	2:0	**Goto field for entry 2 when request vector is 00b**

GAC_GAM R Arbitration Register 2

ARB_R_GAC_GAM2 - GAC_GAM R Arbitration Register 2	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	043E8h

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 5**
	26:24	**Goto field for entry 5 when request vector is 11b**
	23:21	**Goto field for entry 5 when request vector is 10b**
	20:18	**Goto field for entry 5 when request vector is 01b**
	17:15	**Goto field for entry 5 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 4**
	11:9	**Goto field for entry 4 when request vector is 11b**
	8:6	**Goto field for entry 4 when request vector is 10b**
	5:3	**Goto field for entry 4 when request vector is 01b**
	2:0	**Goto field for entry 4 when request vector is 00b**

GAC_GAM R Arbitration Register 3

ARB_R_GAC_GAM3 - GAC_GAM R Arbitration Register 3	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	043ECh

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 7**
	26:24	**Goto field for entry 7 when request vector is 11b**
	23:21	**Goto field for entry 7 when request vector is 10b**
	20:18	**Goto field for entry 7 when request vector is 01b**
	17:15	**Goto field for entry 7 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 6**
	11:9	**Goto field for entry 6 when request vector is 11b**
	8:6	**Goto field for entry 6 when request vector is 10b**
	5:3	**Goto field for entry 6 when request vector is 01b**
	2:0	**Goto field for entry 6 when request vector is 00b**

GAC_GAM WR Arbitration Register 0

ARB_WR_GAC_GAM0 - GAC_GAM WR Arbitration Register 0		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043F0h	
DWord	**Bit**	**Description**
0	31:28	**Reserved**
	27	**Priority for entry 1**
	26:24	**Goto field for entry 1 when request vector is 11b**
	23:21	**Goto field for entry 1 when request vector is 10b**
	20:18	**Goto field for entry 1 when request vector is 01b**
	17:15	**Goto field for entry 1 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 0**
	11:9	**Goto field for entry 0 when request vector is 11b**
	8:6	**Goto field for entry 0 when request vector is 10b**
	5:3	**Goto field for entry 0 when request vector is 01b**
	2:0	**Goto field for entry 0 when request vector is 00b**

GAC_GAM WR Arbitration Register 1

ARB_WR_GAC_GAM1 - GAC_GAM WR Arbitration Register 1	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	043F4h

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 3**
	26:24	**Goto field for entry 3 when request vector is 11b**
	23:21	**Goto field for entry 3 when request vector is 10b**
	20:18	**Goto field for entry 3 when request vector is 01b**
	17:15	**Goto field for entry 3 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 2**
	11:9	**Goto field for entry 2 when request vector is 11b**
	8:6	**Goto field for entry 2 when request vector is 10b**
	5:3	**Goto field for entry 2 when request vector is 01b**
	2:0	**Goto field for entry 2 when request vector is 00b**

GAC_GAM WR Arbitration Register 2

ARB_WR_GAC_GAM2 - GAC_GAM WR Arbitration Register 2	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	043F8h

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 5**
	26:24	**Goto field for entry 5 when request vector is 11b**
	23:21	**Goto field for entry 5 when request vector is 10b**
	20:18	**Goto field for entry 5 when request vector is 01b**
	17:15	**Goto field for entry 5 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 4**
	11:9	**Goto field for entry 4 when request vector is 11b**
	8:6	**Goto field for entry 4 when request vector is 10b**
	5:3	**Goto field for entry 4 when request vector is 01b**
	2:0	**Goto field for entry 4 when request vector is 00b**

GAC_GAM WR Arbitration Register 3

ARB_WR_GAC_GAM3 - GAC_GAM WR Arbitration Register 3	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	043FCh

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 7**
	26:24	**Goto field for entry 7 when request vector is 11b**
	23:21	**Goto field for entry 7 when request vector is 10b**
	20:18	**Goto field for entry 7 when request vector is 01b**
	17:15	**Goto field for entry 7 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 6**
	11:9	**Goto field for entry 6 when request vector is 11b**
	8:6	**Goto field for entry 6 when request vector is 10b**
	5:3	**Goto field for entry 6 when request vector is 01b**
	2:0	**Goto field for entry 6 when request vector is 00b**

Section 0 of TLBPEND Entry

TLBPEND_SEC0 - Section 0 of TLBPEND Entry		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	04400h-04403h	
This register is directly mapped to the TLBPEND Array in the Graphic Arbiter.		
DWord	**Bit**	**Description**
0	31	**vtstatus** This bit will be used in conjunction with the ready bit to determine the stage of the translation. See table below.
	30:28	**GTT bits** Bits 3:1 of the GTT entry used to translate the Virtual Address. 000 if translation is pending.
	27:0	**Current address** The value of this field depends on the stage of the TLB translation for this entry: VA - bits 27:20 = 00, bits 19:0 = Bits 31:12 of the Virtual Address of the cycle.

Internal GAM State

INTSTATE - Internal GAM State		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04500h-04503h	
DWord	**Bit**	**Description**
0	31:0	**GAM Internal State** Default Value: 00000000h Access: RO Internal GAM State for Debug: ctrl_outst_reads_underflow ctrl_outst_reads_overflow gam_mbc_blocked_nonmbc miss_PDARB_FSM_ps[2:0] ctrl_VEBXDONEGEN_ps[3:0] ctrl_CFGFENCE_ps[4:0] ctrl_GFXFENCE_ps[3:0] ctrl_BLTFENCE_ps[2:0] ctrl_MFXFENCE_ps[2:0] ctrl_VEBXFENCE_ps[3:0] ctrl_RSFENCE_ps[2:0]

Section 1 of TLBPEND Entry

TLBPEND_SEC1 - Section 1 of TLBPEND Entry

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	04500h-04503h

This register is directly mapped to the current Virtual Addresses in the MTTLB (Texture and constant cache TLBRender Cache for Z (Depth), Hi Z, and Stencil TLB).

DWord	Bit	Description
0	31:28	**Current address** Bits 9:6 of the Virtual Address of the cycle.
	27:24	**Cacheability Control Bits** Bits 3:1 of the GTT entry used to translate the Virtual Address. 000 if translation is pending. 2 **Graphics Data Type (GFDT).** This field contains the GFDT bit for this surface when writes occur. GFDT can also be set by the GTT. The effective GFDT is the logical OR of this field with the GFDT from the GTT entry. This field is ignored for reads. 1:0 **Cacheability Control.** This field controls cacheability in the mid-level cache (MLC) and last-level cache (LLC). 00: Use cacheability control bits from GTT entry. 01: Data is not cached in LLC or MLC. 10: Data is cached in LLC but not MLC. 11: Data is cached in both LLC and MLC.
	23	**ZLR bit** Flag to indicate this is a zero length read, a read used to calculate a physical address for a write.
	22:4	**TAG** Cycle identification TAG.
	3:0	**SRC ID** Encoding of unit generating this cycle.

Value	Name
0000b	CS_RD_SRCID
0001b	VF_RD_SRCID
0010b	ISC_SRCID
0011b	MT_SRCID

TLBPEND_SEC1 - Section 1 of TLBPEND Entry			
		0100b	RCC_SRCID
		0101b	HZARB_SRCID
		0110b	RCZ_SRCID
		0111b	CTC_SRCID
		1000b	CS_WR_SRCID
		1001b	MBC_SRCID
		1010b	CS_RD_PROBE
		1011b	CS_RD_PWRCTX
		1100b	RC_R4WRCMP
		1101b	RESRVD2_SRCID
		1110b	RESRVD1_SRCID
		1111b	RESRVD0_SRCID

PPGTT Page Fault Data Registers

PP_PFD[0:31] - PPGTT Page Fault Data Registers

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	04580h

The GTT Page Fault Log entries can be read from these registers.
4580h-4583h: Fault Entry 0
...
45FCh-45FFh: Fault Entry 31

DWord	Bit	Description
0	31:12	**Fault Entry Page Address** Format: GraphicsAddress[31:12] This RO field contains the faulting page address for this Fault Log entry. This field will contain a valid fault address only if the bit in the GTT Page Fault Indication Register corresponding with the address offset of this entry is set.
	11:0	**Reserved** Format: MBZ

Fault Switch Out

FAULT_SO - Fault Switch Out		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04590h	
DWord	**Bit**	**Description**
0	31:0	**Fault Switch Out** Default Value: 00000000h Access: R/W

Section 2 of TLBPEND Entry

TLBPEND_SEC2 - Section 2 of TLBPEND Entry	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	04600h-04603h

This register is directly mapped to the current Virtual Addresses in the MTTLB (Texture and constant cache TLB).

DWord	Bit	Description
0	31:14	**Reserved**
	13	**Big Page Attribute** This entry is using a 32K page.
	12:8	**Current Address** Format: GraphicsAddress[14:10] Bits 14:10 of the Virtual Address of the cycle.
	7:0	**PAT Entry** Location of Physical Address in Physical Address Table.

Valid Bit Vector 0 for TLBPEND registers

TLBPEND_VLD0 - Valid Bit Vector 0 for TLBPEND registers	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	04700h-04703h

This register contains the valid bits for entries 0-31 of TLBPEND structure (Cycles pending TLB translation).

DWord	Bit	Description
0	31:0	**Valid bits per entry**

Valid Bit Vector 1 for TLBPEND registers

TLBPEND_VLD1 - Valid Bit Vector 1 for TLBPEND registers	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	04704h-04707h
This register contains the valid bits for entries 32-63 of TLBPEND structure (Cycles pending TLB translation).	

DWord	Bit	Description
0	31:0	**Valid bits per entry**

Ready Bit Vector 0 for TLBPEND registers

TLBPEND_RDY0 - Ready Bit Vector 0 for TLBPEND registers		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	04708h-0470Bh	
This register contains the ready bits for entries 0-31 of TLBPEND structure (Cycles pending TLB translation).		
DWord	**Bit**	**Description**
0	31:0	**Ready bits per entry**

Ready Bit Vector 1 for TLBPEND registers

TLBPEND_RDY1 - Ready Bit Vector 1 for TLBPEND registers		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	0470Ch-0470Fh	
This register contains the ready bits for entries 32-63 of TLBPEND structure (Cycles pending TLB translation).		
DWord	**Bit**	**Description**
0	31:0	**Ready bits per entry**

Valid Bit Vector 0 for MTTLB

MTTLB_VLD0 - Valid Bit Vector 0 for MTTLB	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	04780h-04783h

This register contains the valid bits for entries 0-31 of MTTLB (Texture and constant cache TLB).

DWord	Bit	Description
0	31:0	**Valid bits per entry**

Valid Bit Vector 1 for MTTLB

MTTLB_VLD1 - Valid Bit Vector 1 for MTTLB	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	04784h-04787h

This register contains the valid bits for entries 0-31 of MTTLB (Texture and constant cache TLBVertex Fetch, Instruction Cache, and Command Streamer TLB).

DWord	Bit	Description
0	31:0	**Valid bits per entry**

Valid Bit Vector 0 for MTVICTLB

VICTLB_VLD0 - Valid Bit Vector 0 for MTVICTLB	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	04788h-0478Bh

This register contains the valid bits for entries 0-31 of VICTLB (Vertex Fetch, Instruction Cache, and Command Streamer TLB).

DWord	Bit	Description
0	31:0	**Valid bits per entry**

Valid Bit Vector 1 for MTVICTLB

MTVICTLB_VLD1 - Valid Bit Vector 1 for MTVICTLB	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	0478Ch-0478Fh

This register contains the valid bits for entries 0-31 of VICTLB (Vertex Fetch, Instruction Cache, and Command Streamer TLB).

DWord	Bit	Description
0	31:0	**Valid bits per entry**

Valid Bit Vector 0 for RCZTLB

RCZTLB_VLD0 - Valid Bit Vector 0 for RCZTLB		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	04798h-0479Bh	
This register contains the valid bits for entries 0-31 of RCZTLB (Render Cache for Z (Depth), Hi Z, and Stencil TLB).		
DWord	**Bit**	**Description**
0	31:0	**Valid bits per entry**

Valid Bit Vector 1 for RCZTLB

RCZTLB_VLD1 - Valid Bit Vector 1 for RCZTLB		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	0479Ch-0479Fh	
This register contains the valid bits for entries 0-31 of RCZTLB (Render Cache for Z (Depth), Hi Z, and Stencil TLB).		
DWord	**Bit**	**Description**
0	31:0	**Valid bits per entry**

Valid Bit Vector 0 for RCC

RCCTLB_VLD_0 - Valid Bit Vector 0 for RCC

Register Space:	MMIO: 0/2/0
Project:	HSW
Default Value:	0x00000000
Size (in bits):	32
Address:	047B8h-047BBh

This register contains the valid bits for entries 0-31 of RCCTLB

DWord	Bit	Description
0	31:0	**Valid Bit Vector 0 for RCC** Default Value: 00000000h Access: RO Valid Bits per Entry

Valid Bit Vector 1 for RCC

RCCTLB_VLD_1 - Valid Bit Vector 1 for RCC	
Register Space:	MMIO: 0/2/0
Project:	HSW
Default Value:	0x00000000
Size (in bits):	32
Address:	047BCh-047BFh
This register contains the valid bits for entries 0-31 of RCCTLB	

DWord	Bit	Description
0	31:0	**Valid Bit Vector 1 for RCC** Default Value: 00000000h Access: RO Valid Bits per Entry

Valid Bit Vector 2 for RCC

RCCTLB_VLD_2 - Valid Bit Vector 2 for RCC

Register Space:	MMIO: 0/2/0
Project:	HSW
Default Value:	0x00000000
Size (in bits):	32
Address:	047C0h-047C3h

This register contains the valid bits for entries 0-31 of RCCTLB

DWord	Bit	Description
0	31:0	**Valid Bit Vector 2 for RCC** Default Value: 00000000h Access: RO Valid Bits per Entry

Valid Bit Vector 3 for RCC

RCCTLB_VLD_3 - Valid Bit Vector 3 for RCC	
Register Space:	MMIO: 0/2/0
Project:	HSW
Default Value:	0x00000000
Size (in bits):	32
Address:	047C4h-047C7h
This register contains the valid bits for entries 0-31 of RCCTLB	

DWord	Bit	Description
0	31:0	**Valid Bit Vector 3 for RCC** Default Value: 00000000h Access: RO Valid Bits per Entry

MT Virtual Page Address Registers

MTTLB_VA - MT Virtual Page Address Registers

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1

Address: 04800h-04803h

DWord	Bit	Description
0	31:12	**Address** Format: GraphicsAddress[31:12] Page virtual address.
	11:0	**Reserved** Project: HSW Format: MBZ

VIC Virtual page Address Registers

VICTLB_VA - VIC Virtual page Address Registers

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	04900h-04903h

These registers are directly mapped to the current Virtual Addresses in the VICTLB (Vertex Fetch, Instruction Cache, and Command Streamer TLB.)

DWord	Bit	Description
0	31:12	**Address** Format: GraphicsAddress[31:12] Page virtual address.
	11:0	**Reserved** Format: MBZ

RCC Virtual page Address Registers

RCCTLB_VA - RCC Virtual page Address Registers

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	04A00h-04A03h

These registers are directly mapped to the current Virtual Addresses in the RCCTLB (Render Cache for Color TLB).

DWord	Bit	Description
0	31:12	**Address** Project: All Format: GraphicsAddress[31:12] Page virtual address.
	11:0	**Reserved** Project: HSW Format: MBZ

RCZ Virtual Page Address Registers

RCZTLB_VA - RCZ Virtual Page Address Registers

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	04B00h-04B03h

These registers are directly mapped to the current Virtual Addresses in the RCZTLB (Render Cache for Z (Depth), Hi Z, and Stencil TLB).

DWord	Bit	Description
0	31:12	**Address** Format: GraphicsAddress[31:12] Page virtual address.
	11:0	**Reserved** Format: MBZ

Stream Output Num Primitives Written Counter

SO_NUM_PRIMS_WRITTEN[0:3] - Stream Output Num Primitives Written Counter

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	05200h-0521Fh

There is one 64-bit register for each of the 4 supported streams:5200h-5207h SO_NUM_PRIMS_WRITTEN0 (for Stream Out Stream #0)5208h-520Fh SO_NUM_PRIMS_WRITTEN1 (for Stream Out Stream #1)5210h-5217h SO_NUM_PRIMS_WRITTEN2 (for Stream Out Stream #2)5218h-521Fh SO_NUM_PRIMS_WRITTEN3 (for Stream Out Stream #3)These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has successfully written to a particular "stream's" Streamed Vertex Output buffers, subject to buffer overflow detection. (See the Stream Output section of the 3D pipeline volume).These registers are part of the context save and restore.

DWord	Bit	Description
0	63:0	**Num Prims Written Count** Format: U64 This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)

Stream Output Primitive Storage Needed Counters

SO_PRIM_STORAGE_NEEDED[0:3] - Stream Output Primitive Storage Needed Counters

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	RW. This register is set by the context restore.
Size (in bits):	64
Address:	05240h-0525Fh

There is one 64-bit register for each of the 4 supported streams:

5240h-5247h SO_PRIM_STORAGE_NEEDED0 (for Stream Out Stream #0)
5248h-524Fh SO_PRIM_STORAGE_NEEDED1 (for Stream Out Stream #1)
5250h-5257h SO_PRIM_STORAGE_NEEDED2 (for Stream Out Stream #2)
5258h-525Fh SO_PRIM_STORAGE_NEEDED3 (for Stream Out Stream #3)

These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has or would have written to a particular "stream's" Streamed Vertex Output buffers if all buffers had been large enough to accommodate the writes. (See the Stream Output section of the 3D pipeline volume).

These registers are part of the context save and restore.

DWord	Bit	Description
0	63:0	**Prim Storage Needed Count** Project: HSW Format: U64 This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.

Stream Output Write Offsets

SO_WRITE_OFFSET[0:3] - Stream Output Write Offsets

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	RW. This register is set by the context restore.
Size (in bits):	32
Address:	05280h-0528Fh

There is one R/W 32-bit register for each of the 4 supported stream output buffer slots:
5280h-5283h SO_WRITE_OFFSET0 (for Stream Out Buffer #0)
5284h-5287h SO_ WRITE_OFFSET1 (for Stream Out Buffer #1)
5288h-528Bh SO_ WRITE_OFFSET2 (for Stream Out Buffer #2)
528Ch-528Fh SO_ WRITE_OFFSET3 (for Stream Out Buffer #3)
These registers are used to set and track a DWord-granular Write Offset for each of the 4 Stream Output Buffer slots. Software can directly write them via MI_LOAD_REGxxx commands. The SOL stage will increment them as part of stream output processing. Software can cause them to be written to memory via MI_STORE_REGxxx commands. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

Programming Notes

- Software must ensure that no HW stream output operations can be in process or otherwise pending at the point that the MI_LOAD/STORE commands are processed. This will likely require a pipeline flush.
- The SOL stage will effectively advance the write offset by the buffer's Surface Pitch after each vertex is written (assuming no overflow is detected in any targetted SO buffer). Under "normal" conditions one would expect software to initialize the WriteOffset to some (possibly zero) multiple of Surface Pitch in order to align vertex writes to the buffer's Base Address, though it is not required to do so.

DWord	Bit	Description
0	31:2	**Write Offset** Project: HSW Format: U30 This field contains a DWord offset from the corresponding SO buffer's Base Address value. The SOL stage uses this value as a write offset when performing writes to the buffer. The SOL stage will increment this value as a part of performing stream output to the buffer. Note that the SOL stage uses the buffer's Surface Pitch to advance the Write Offset, without regard to the buffer's Base Address (see Programming Notes above).
	1:0	**Reserved** Format: MBZ

Cache Mode Register 0

CACHE_MODE_0 - Cache Mode Register 0

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000 [NOVALIDPROJECTS]
	0x00000004 [NOVALIDPROJECTS]
	0x00006000 [NOVALIDPROJECTS]
	0x00006004 [HSW]
Access:	R/W
Size (in bits):	32

Address:	07000h
Valid Projects:	HSW

Description	Project
This register is used to control the operation of the Render and Sampler L2 Caches. All reserved bits are implemented as read/write. Before changing the value of this register, GFX pipeline must be idle i.e. full flush is required. This Register is saved and restored as part of Context.	
RegisterType = MMIO_SVL	HSW

DWord	Bit	Description
0	31:16	**Masks** Format: Mask[15:0] A 1 in a bit in this field allows the modification of the corresponding bit in Bits 15:0.
	15	**Sampler L2 Disable** Project: HSW Format: Disable Value / Name / Description: 0h / **[Default]** / Sampler L2 Cache Enabled. 1h / / Sampler L2 Cache Disabled. All accesses are treated as misses.
	14:13	**Reserved** Default Value: 3h Project: HSW Format: MBZ

CACHE_MODE_0 - Cache Mode Register 0

12 **Reserved**

Project:	HSW
Format:	MBZ

11 **Reserved**

Project:	DevHSW:GT3:A
Format:	MBZ

11 **Sampler Set Remmapping for 3D Disable**

Project:	HSW, EXCLUDE(HSW:GT3:A)

Value	Name	Description
0h	Enable Set Remap **[Default]**	Set remapping for 3d enabled
1h	Disable Set Remap	Set remapping for 3d disabled

10 **Reserved**

Project:	HSW
Format:	MBZ

9 **Sampler L2 TLB Prefetch Enable**

Value	Name	Description
0h	**[Default]**	TLB Prefetch Disabled
1h		TLB Prefetch Enabled

8 **Reserved**

7:6 **Sampler L2 Request Arbitration**

Project:	HSW
Format:	U2

Value	Name	Description
00b		Round Robin
01b		Fetch are Highest Priority
10b		Constants are Highest Priority
11b		Reserved

5 **STC Eviction Policy**

Project:	HSW
Format:	Disable

If this bit is set, STCunit will have LRA as replacement policy. The default value i.e. (when this bit is reset) indicates that non-LRA eviction policy. This bit must be reset. LRA replacement policy is not supported.

Programming Notes	Project

CACHE_MODE_0 - Cache Mode Register 0

	If this bit is set to "1", bit 4 of 0x7010h must also be set to "1".	HSW

4 RCC Eviction Policy

Project:	HSW
Format:	Disable

If this bit is set, RCCunit will have LRA as replacement policy. The default value i.e. (when this bit is reset) indicates that non-LRA eviction policy. This bit must be reset. LRA replacement policy is not supported.

Programming Notes	Project
If this bit is set to "1", bit 7 of 0x7010h must also be set to "1".	HSW

3 Reserved

2 Hierarchical Z RAW Stall Optimization Disable

Project:	HSW
Format:	U1

The Hierarchical Z RAW Stall Optimization allows non-overlapping polygons in the same 8x4 pixel/sample area to be processed without stalling waiting for the earlier ones to write to Hierarchical Z buffer.

Value	Name	Description
0h	Enable	Enables the hierarchical Z RAW Stall Optimization.
1h	Disable **[Default]**	Disables the hierarchical Z RAW Stall Optimization.

Programming Notes	Project
This bit must be set to 0 to enable the Hierarchical Z RAW stall optimization.	DevHSW+

1 Disable clock gating in the pixel backend

Format:	Disable

MCL related clock gating is disabled in the pixel backend. Before setting this bit to 1, the instruction/state caches must be invalidated. [DevGT:{WKA}]

0 Render Cache Operational Flush Enable

Project:	HSW
Format:	Enable

Value	Name	Description
0h	Disable **[Default]**	Operational Flush Disabled (recommended for performance when not rendering to the front buffer)
1h	Enable	Operational Flush Enabled (required when rendering to the front buffer)

Note	Description	Project
Note:	This bit must be set to '0' (Disable).	HSW

Cache Mode Register 1

CACHE_MODE_1 - Cache Mode Register 1

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000 [NOVALIDPROJECTS]
	0x00000180 [HSW]
Access:	Read/32 bit Write Only
Size (in bits):	32
Address:	07004h
Valid Projects:	HSW

Description	Project
RegisterType: MMIO_SVL	HSW
Before changing the value of this register, GFX pipeline must be idle; i.e., full flush is required. This Register is saved and restored as part of Context.	

DWord	Bit	Description
0	31:16	**Mask Bits for 15:0** Format: Mask[15:0] Must be set to modify corresponding data bit. Reads to this field returns zero.
	15	**Reserved** Project: HSW Format: MBZ
	14	**Reserved** Project: HSW Format: MBZ
	13	**Reserved** Project: HSW
	12	**HIZ Eviction Policy** Project: All Format: U1 If this bit is set, Hizunit will have LRA as replacement policy. The default value i.e. (when this bit is reset) indicates the non-LRA eviction policy. For performance reasons, this bit must be reset. Value: 0h — **[Default]** — Non-LRA eviction Policy — Project: All

CACHE_MODE_1 - Cache Mode Register 1

1h		LRA eviction Policy	All

Programming Notes	Project
If this bit is set to "1", bit 3 of 0x7010h must also be set to "1"	HSW

11 **Reserved**

Project:	HSW
Format:	MBZ

10 **Reserved**

Project:	HSW

9 **Reserved**

Project:	All

8:7 **Sampler Cache Set XOR selection**

Project:	HSW
Format:	U2

These bits have an impact only when the Sampler cache is configured in 16 way set associative mode. If the cache is being used for immediate data or for blitter data these bits have no effect.

Value	Name	Description	Project
00b	None	No XOR.	All
01b	Scheme 1	New_set_mask[3:0] = Tiled_address[16:13]. New_set[3:0] less than or = New_set_mask[3:0] ^Old_set[3:0]. Rationale: These bits can distinguish among 16 different equivalent classes of virtual pages. These bits also represent the lsb for tile rows ranging from a pitch of 1 tile to 16 tiles.	All
10b	Scheme 2	New_set_mask[3] = Tiled_address[17] ^ Tiled_address[16]. New_set_mask[2] = Tiled_address[16] ^ Tiled_address[15]. New_set_mask[1] = Tiled_address[15] ^ Tiled_address[14]. New_set_mask[0] = Tiled_address[14] ^ Tiled_address[13]. New_set[3:0] less than or = New_set_mask[3:0] ^ Old_set[3:0]. Rationale: More bits on each XOR can give better statistical uniformity on sets and since two lsbs are taken for each tile row size, it reduces the chance of aliasing on sets.	All
11b	Scheme 3 **[Default]**	New_set_mask[3] = Tiled_address[22] ^ Tiled_address[21] ^ Tiled_address[20] ^ Tiled_address[19]. New_set_mask[2] = Tiled_address[18] ^ Tiled_address[17] ^ Tiled_address[16].	

CACHE_MODE_1 - Cache Mode Register 1

		New_set_mask[1] = Tiled_address[15] ^ Tiled_address[14]. New_set_mask[0] = Tiled_address[13]. New_set[3:0] less than or = New_set_mask[3:0] ^ Old_set[3:0]. Rationale: More bits on each XOR can give better statistical uniformity on sets and since each XOR has different bits, it reduces the chance of aliasing on sets even more.

6 **Pixel Backend sub-span collection Optimization Disable**

Project:	HSW
Format:	Disable

Value	Name	Description
0h	**[Default]**	Enables two contiguous quads to be collected as 4X2 access for RCZ interface. This allows for less bank collision and less RAM power on RCZ.
1h		Disables this optimization and therefore only one valid sub-span is sent to RCZ on the 4X2 interface.

Programming Notes	Project
This bit must be set.	HSW

5 **MCS Cache Disable**

Project:	HSW
Format:	Disable

For Programming restrictions please refer to the 3D Pipeline.

Value	Name	Description
0h	**[Default]**	MCS cache enabled. It allows RTs with MCS buffer enabled to be rendered using either MSAA compression for MSRT OR with color clear feature for non MSRT.
1h		MCS cache is disabled. Hence no MSAA compression for MSRT and no color clear for non-MSRT.

4 **Reserved**

Project:	HSW
Format:	MBZ

3 **Depth Read Hit Write-Only Optimization Disable**

Project:	HSW
Format:	Disable

Description	Project
This bit must always be reset to "0".	HSW

CACHE_MODE_1 - Cache Mode Register 1

Value	Name	Description	Project
0h	**[Default]**	Read Hit Write-only optimization is enabled in the Depth cache (RCZ).	HSW
1h		Read Hit Write-only optimization is disabled in the Depth cache (RCZ).	HSW

2	**Reserved**
Project:	HSW
1	**Reserved**
Project:	HSW
Format:	MBZ
0	**Reserved**
Project:	HSW

GT Mode Register

GT_MODE - GT Mode Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000 [HSW]
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	07008h
Valid Projects:	HSW

This Register is used to control the 6EU and 12EU configuration for GT.
Writing 0x01FF01FF to this register enables the 6EU mode.

DWord	Bit	Description
0	31:16	**Mask Bits** Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15	**EU Local Thread Checking Enable** Project: DevHSW+ This field configures the EU local thread checking. If enable the stateless access will be checked against the local thread's scratch space size and start address.

Value	Name	Description	Project
0h	Disable **[Default]**	EU local thread checking is disabled.	DevHSW+
1h	Enable	EU local thread checking is enabled.	DevHSW+

	14:13	**SFR mode** Project: DevHSW+ Format: U2

Description	Project
This field must be zero when not in GT4(SFR) configuration i.e GTB_rendermode fuse set to SFR.	
Supports SFR(50%-50%) in vertical and horizontal direction enabling each GT to render exclusive portions of the screen.	HSW

Value	Name	Description	Project

GT_MODE - GT Mode Register

0h	00 **[Default]**	No SFR	HSW
1h	01	SFR in horizontal direction	HSW
2h	10	SFR in vertical direction	HSW
3h	11	Reserved	HSW

12:11 **Cross GT Hashing mode**

Project:	HSW
Format:	U2

This field must be zero when not in GT-XE(CBR) configuration. In GT-XE (CBR) configuration, this field allows cross GT pixel block-hashing at 32X32, 32X16, or 16X32 granularity.

Value	Name	Description	Project
0h	Cross GT hashing disable. **[Default]**	Default value. In GT-XE (CBR) configuration, this value is illegal.	HSW
1h	16X32 hashing	16X32 pixel hashing across GT	HSW
2h	32X16 hashing	32X16 pixel hashing across GT	HSW
3h	32X32 hashing	32X32 pixel hashing across GT	HSW

10 **16X16 Cross Slice Hash Disable**

Project:	HSW
Format:	U1

Description	Project
This field allows to control pixel block hashing across slices.	
Supports 16X16 pixel block hashing in the checker-board pattern irrespective of MSAA. Setting this bit disables hashing and therefore HW must not send any pixels down to slice1.	HSW

Value	Name	Description	Project
0h	Enable **[Default]**	16X16 Checkerboard hashing enabled across slices	DevHSW+
1h	Disable	16X16 Checkerboard hashing disabled across slices	DevHSW+

9 **WIZ Hashing Mode High Bit**

Project:	HSW
Format:	U1

This field adds additional hashing modes in combination with the WIZ Hashing Mode field. The Value column in the table below refers to this field (high bit) and the WIZ Hashing Mode field (low bit).

This field is don't care if the Hashing Disable bit is set.

Value	Name	Description
0h	**[Default]**	8x8 Checkerboard hashing
1h		8x4 Checkerboard hashing

GT_MODE - GT Mode Register

2h		16x4 Checkerboard hashing
3h		Reserved

Programming Notes
8x4 hashing preferred for when msaa enabled

8 **Reserved**

Project:	HSW
Format:	MBZ

7 **WIZ Hashing Mode**

Project:	HSW
Format:	U1

Description	Project
This field configures the Hashing mode in Windower. This field is don't care if the Hashing Disable bit is set.	
The WIZ Hashing Mode High Bit field is combined with this field to enable additional modes.	HSW

6:3 **Reserved**

Project:	HSW
Format:	MBZ

2 **Reserved**

Format:	MBZ

1 **Reserved**

Project:	HSW
Format:	MBZ

0 **Reserved**

FBC_RT_BASE_ADDR_REGISTER

FBC_RT_BASE_ADDR_REGISTER - FBC_RT_BASE_ADDR_REGISTER

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Access:	Read/32 bit Write Only
Size (in bits):	32
Address:	07020h
Valid Projects:	HSW

This Register is saved and restored as part of Context.

DWord	Bit	Description
0	31:12	**FBC RT Base Address** Format: PPGraphicsAddress[31:12] 4KB aligned Base Address as mapped in the PPGTT or in the GGTT for the render target. This base address must be the one that is either front buffer or the back-buffer (a flip target). It must be programmed before any draw call binding that render target base address.
	11:2	**Reserved** Format: MBZ
	1	**FBC Front Buffer Target** Project: HSW Format: Enable Value / Name / Description / Project: 0h / **[Default]** / FBC is targeting the Back Buffer for compression. This buffer can be cached in the MLC/LLC, so a GFDT flush is required before FBC can begin compression. / HSW 1h / / FBC is targeting the Font Buffer for compression. This buffer cannot be cached in the MLC/LLC. FBC compression can begin after any RC flush. / HSW
	0	**PPGTT Render Target Base Address Valid for FBC** Project: HSW Access: None Format: Enable

FBC_RT_BASE_ADDR_REGISTER - FBC_RT_BASE_ADDR_REGISTER

Value	Name	Description	Project
0h	**[Default]**	Base address in this register [31:12] is not valid and therefore FBC will not get any modifications from rendering.	HSW
1h		Base address in this register [31:12] is valid and HW needs to compare the current render target base address with this base address to provide modifications to FBC.	HSW

Note:	Project
Note: Do not enable Render Command Streamer tracking for FBC. Instead insert a LRI to address 0x50380 with data 0x00000004 after the PIPE_CONTROL that follows each render submission.	HSW

SAMPLER Mode Register

SAMPLER_MODE - SAMPLER Mode Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	RenderCS
Default Value:	0x00000000
Size (in bits):	32
Trusted Type:	1
Address:	07028h
Valid Projects:	HSW

This register has bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].
To set bit0, for example, the data would be 0x0001_0001.
To clear bit0, for example, the data would be 0x0001_0000.
Note that mask bit is the data bit offset + 16.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO
	15:14	**ECO Reserved 1** Format: MBZ
	13:8	**ECO Reserved 2** Project: HSW Format: MBZ
	7:5	**ECO Reserved 3** Project: All Format: MBZ
	4:0	**Sample_d Quality Mode** Project: HSW Format: U5 This field configures the image quality mode for the sample_d message in the sampling engine. In general, performance will increase with each step of reduced quality.

Value	Name	Description	Project
00h	Disabled	Full quality is enabled, matching prior products	All
01h-1Fh		Quality degrades with each larger value, performance improves with each larger value	All

Conditional Debug Value

COND_DBG_VAL - Conditional Debug Value		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	WO	
Size (in bits):	32	
Address:	0E43Ch	
Name:	COND_DBG_VAL0	
Address:	0E448h	
Name:	COND_DBG_VAL1	
Address:	0E468h	
Name:	COND_DBG_VAL2	
Address:	0E4E4h	
Name:	COND_DBG_VAL3	
DWord	**Bit**	**Description**
0	31:0	**Condition Value** Specifies the value compared to the payload after applying the mask.

VCS Execute Condition Code Register

VCS_EXCC - VCS Execute Condition Code Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W,RO
Size (in bits):	32
Trusted Type:	1
Address:	12028h
Valid Projects:	HSW

This register contains user defined and hardware generated conditions that are used by MI_WAIT_FOR_EVENT commands. An MI_WAIT_FOR_EVENT instruction excludes the executing ring from arbitration if the selected event evaluates to a 1, while instruction is discarded if the condition evaluates to a 0. Once excluded, a ring is enabled into arbitration when the selected condition evaluates to a 0.
This register also contains control for the invalidation of indirect state pointers on context restore.

DWord	Bit	Description
0	31:16	**Mask Bits** Format: Mask[15:0] These bits serve as a write enable for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.
	15:5	**Reserved** Format: MBZ
	4:0	**User Defined Condition Codes** Project: HSW The software may signal a Stream Semaphore by setting the Mask bit and Signal Bit together to match the bit field specified in a WAIT_FOR_EVENT (Semaphore).

Video/Blitter Semaphore Sync Register

VBSYNC - Video/Blitter Semaphore Sync Register	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	12040h
This register is written by BCS, read by VCS.	

DWord	Bit	Description
0	31:0	**Semaphore Data** Semaphore data for synchronization between video codec engine and blitter engine.

Video/Render Semaphore Sync Register

VRSYNC - Video/Render Semaphore Sync Register		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	12044h	
This register is written by CS, read by VCS.		
DWord	**Bit**	**Description**
0	31:0	**Semaphore Data** Semaphore data for synchronization between video codec engine and render engine.

Video Codec/Video Enhancement Semaphore Sync Register

VVESYNC - Video Codec/Video Enhancement Semaphore Sync Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1

Address: 12048h

This register is written by VECS, read by VCS.

DWord	Bit	Description
0	31:0	**Semaphore Data** Semaphore data for synchronization between video codec engine and video enhancement engine.

VCS IDLE Max Count

VCS_PWRCTX_MAXCNT - VCS IDLE Max Count

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000 [NOVALIDPROJECTS] 0x00000040 [HSW]
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	12054h
Valid Projects:	HSW

This register contains the time in 0.64us to wait before telling power management hardware the render pipe is IDLE

DWord	Bit	Description
0	31:20	**Reserved** Format: MBZ
	19:0	**MFX IDLE Wait Time** Format: Max Count Specifies how long the command stream should wait before ensuring the pipe is IDLE and to let power management hardware know

Value	Name	Description	Project
00040h	**[Default]**	DevHSW 0x00040 * 0.64us ~ 41us wait time	HSW

Programming Notes

- This is only useable if bit 0 of the PC_PSMI_CTRL is clear.
- The value in this field *must* be greater than 1.

VCS Hardware Status Mask Register

VCS_HWSTAM - VCS Hardware Status Mask Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0xFFFFFFFF
Access:	R/W
Size (in bits):	32
Trusted Type:	1

Address:	12098h
Valid Projects:	HSW

Access: RO for Reserved Control bits

The HWSTAM register has the same format as the Interrupt Control Registers. The bits in this register are "mask" bits that prevent the corresponding bits in the Interrupt Status Register from generating a "Hardware Status Write" (PCI write cycle). Any unmasked interrupt bit (HWSTAM bit set to 0) will allow the Interrupt Status Register to be written to the ISR location (within the memory page specified by the Hardware Status Page Address Register) when that Interrupt Status Register bit changes state.

Programming Notes

- To write the interrupt to the HWSP, the corresponding IMR bit must also be clear (enabled).
- At most 1 bit can be unmasked at any given time.

DWord	Bit	Description
0	31:0	**Hardware Status Mask Register** Default Value: FFFFFFFFh Format: Array of Masks Refer to the table in the Interrupt Control Register section for bit definitions.

VCS Mode Register for Software Interface

VCS_MI_MODE - VCS Mode Register for Software Interface

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000 [NOVALIDPROJECTS] 0x00000200 [HSW]
Access:	R/W
Size (in bits):	32

Address:	1209Ch-1209Fh
Valid Projects:	HSW

The MI_MODE register contains information that controls software interface aspects of the command parser.

DWord	Bit	Description
0	31:16	**Masks** A 1 in a bit in this field allows the modification of the corresponding bit in Bits 15:0.
	15	**Suspend Flush** Mask: MMIO(0x209c)#31 Value / Name / Description: 0h / No Delay / HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well 1h / DelayFlush / Suspend flush is active
	14:12	**Reserved** Access: R/W
	11	**Invalidate UHPTR enable** If bit set H/W clears the valid bit of BCS_UHPTR (4134h, bit 0) when current active head pointer is equal to UHPTR.
	10	**Reserved** Project: HSW Format: MBZ
	9	**Ring Idle (Read Only Status bit)** Access: RO *Writes to this bit are not allowed.* Value / Name: 0 / Parser not idle

VCS_MI_MODE - VCS Mode Register for Software Interface

	1	Parser idle **[Default]**

8 — Stop Ring

Software must set this bit to force the Ring and Command Parser to Idle. Software must read a "1" in Ring Idle bit after setting this bit to ensure that the hardware is idle.

Software must clear this bit for Ring to resume normal operation.

Value	Name
0	Normal Operation
1	Parser is turned off

7:0 — Reserved

Access:	R/W

Mode Register for GAC

GAC_MODE - Mode Register for GAC

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	120A0h-120A3h
Valid Projects:	HSW

The GAC_MODE register contains information that controls configurations in the GAC.

DWord	Bit	Description
0	31:16	**Reserved** Access: WO This register has bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. To set bit0, for example, the data would be 0x0001_0001. To clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16.
	15:0	**Reserved** Access: R/W

VCS Interrupt Mask Register

VCS_IMR - VCS Interrupt Mask Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0xFFFFFFFF
Access:	R/W
Size (in bits):	32
Address:	120A8h
Valid Projects:	HSW

The IMR register is used by software to control which Interrupt Status Register bits are masked or unmasked. Unmasked bits will be reported in the IIR, possibly triggering a CPU interrupt, and will persist in the IIR until cleared by software. Masked bits will not be reported in the IIR and therefore cannot generate CPU interrupts.

DWord	Bit	Description
0	31:0	**Interrupt Mask Bits** Format: Array of interrupt mask bits Refer to the Interrupt Control Register section for bit definitions. This field contains a bit mask which selects which interrupt bits (from the ISR) are reported in the IIR.

Value	Name	Description
FFFF FFFFh	**[Default]**	
0h	Not Masked	Will be reported in the IIR
1h	Masked	Will not be reported in the IIR

VCS Error Identity Register

VCS_EIR - VCS Error Identity Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	R/WC
Size (in bits):	32
Address:	120B0h
Valid Projects:	HSW

The EIR register contains the persistent values of Hardware-Detected Error Condition bits. Any bit set in this register will cause the Master Error bit in the ISR to be set. The EIR register is also used by software to clear detected errors (by writing a 1 to the appropriate bit(s) except for the unrecoverable bits described).

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Error Identity Bits** Format: Array of Error condition bits ee the table titled Hardware-Detected Error Bits This register contains the persistent values of ESR error status bits that are unmasked via the EMR register. The logical OR of all (defined) bits in this register is reported in the Master Error bit of the Interrupt Status Register. In order to clear an error condition, software must first clear the error by writing a 1 to the appropriate bit(s) in this field. If required, software should then proceed to clear the Master Error bit of the IIR.

Value	Name	Description
0h	**[Default]**	
1h	Error occurred	Error occurred

Programming Notes
Writing a 1 to a set bit will cause that error condition to be cleared. However, the Page Table Error bit (Bit 4) cannot be cleared except by reset (i.e., it is a fatal error).

VCS Error Mask Register

VCS_EMR - VCS Error Mask Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000 [NOVALIDPROJECTS] 0x0000FFFF [HSW]
Access:	R/W
Size (in bits):	32
Address:	120B4h
Valid Projects:	HSW

The EMR register is used by software to control which Error Status Register bits are "masked" or "unmasked". "Unmasked" bits will be reported in the EIR, thus setting the Master Error ISR bit and possibly triggering a CPU interrupt, and will persist in the EIR until cleared by software. "Masked" bits will not be reported in the EIR and therefore cannot generate Master Error conditions or CPU interrupts.

Undefined or reserved bits in the Hardware Detected Error Bit Table will always return a read value of '1'

DWord	Bit	Description
0	31:16	**Reserved** Default Value: 0000h Project: HSW Format: MBZ
	15:0	**Error Mask Bits** Format: Array of error condition mask bits See the table titled Hardware-Detected Error Bits. This register contains a bit mask that selects which error condition bits (from the ESR) are reported in the EIR. **Value** / **Name** / **Description** 0000h / Not Masked / Will be reported in the EIR FFFFh / Masked **[Default]** / Will not be reported in the EIR

VCS Error Status Register

VCS_ESR - VCS Error Status Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	120B8h
Valid Projects:	HSW

The ESR register contains the current values of all Hardware-Detected Error condition bits (these are all by definition persistent). The EMR register selects which of these error conditions are reported in the persistent EIR (i.e., set bits must be cleared by software) and thereby causing a Master Error interrupt condition to be reported in the ISR.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Error Status Bits** Format: Array of error condition bits See the table titled Hardware-Detected Error Bits. This register contains the non-persistent values of all hardware-detected error condition bits.

Value	Name	Description
0h	**[Default]**	
1h	Error Condition Detected	Error Condition detected

VCS Instruction Parser Mode Register

VCS_INSTPM - VCS Instruction Parser Mode Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	120C0h-120C3h
Valid Projects:	HSW

The VCS_INSTPM register is used to control the operation of the VCS Instruction Parser. Certain classes of instructions can be disabled (ignored) - often useful for detecting performance bottlenecks. Also, "Synchronizing Flush" operations can be initiated - useful for ensuring the completion (vs. only parsing) of rendering instructions. DefaultValue=0000 0000h

Programming Notes

All reserved bits are implemented.

DWord	Bit	Description
0	31:16	**Masks** Format: Mask[15:0] These bits serve as write enables for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.
	15:11	**Reserved** Project: All Format: MBZ
	10	**Reserved** Project: HSW Format: MBZ
	9	**TLB Invalidate** Project: HSW Format: U1 If set, this bit allows the command stream engine to invalidate the MFX TLBs. This bit is valid only with the Sync flush enable. *Note: GFX soft resets do not invalidate TLBs, it is up to GFX driver to explicitly invalidate TLBs post reset./*

VCS_INSTPM - VCS Instruction Parser Mode Register

	8:7	**Reserved** Format: MBZ
	6	**Memory Sync Enable** Project: HSW If set, this bit allows the video decode engine to write out the data from the local caches to memory.
	5	**Sync Flush Enable** Project: HSW Format: Enable (Cleared by HW) This field is used to request a Sync Flush operation. The device will automatically clear this bit before completing the operation. See Sync Flush *(Programming Environment)*. Setting the Sync Flush Enable will cause a config write to MMIO register space with the address 0x4f100. **Programming Notes** The command parser must be stopped prior to issuing this command by setting the **Stop Ring** bit in register **BCS_MI_MODE**. Only after observing **Ring Idle** set in **BCS_MI_MODE** can a Sync Flush be issued by setting this bit. Once this bit becomes clear again, indicating flush complete, the command parser is re-enabled by clearing **Stop Ring**.
	4:0	**Reserved** Access: R/W Format: MBZ

Batch Buffer State Register

BB_STATE - Batch Buffer State Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS
Default Value:	0x00000000 [HSW]
Access:	RO
Size (in bits):	32
Address:	12110h
Name:	VCS Batch Buffer State Register
ShortName:	VCS_BB_STATE
Address:	1A110h
Name:	VECS Batch Buffer State Register
ShortName:	VECS_BB_STATE
Address:	22110h
Name:	BCS Batch Buffer State Register
ShortName:	BCS_BB_STATE

This register contains the attributes of the current batch buffer initiated from the Ring Buffer.

This register should not be written by software. These fields should only get written by a context restore. Software should always set these fields via the MI_BATCH_BUFFER_START command when initiating a batch buffer.
This register is saved and restored with context.

DWord	Bit	Description
0	31:7	**Reserved** Project: All Format: MBZ
	6	**2nd Level Buffer Security Indicator** Project: HSW Source: BlitterCS, VideoEnhancementCS Exists If: //BCS, VECS Format: MI_2ndBufferSecurityType If set, VECS is fetching 2nd level batch commands from a PPGTT address space. If clear, GGTT. If execlists are enabled and this is set, the batch buffer is non-secure and cannot execute privileged commands nor access privileged (GGTT) memory. It will be accessed via the PPGTT. If clear, this batch buffer is secure and will be accessed via the GGTT.

BB_STATE - Batch Buffer State Register

Value	Name	Description
0h	MIBUFFER_SECURE **[Default]**	Located in GGTT memory
1h	MIBUFFER_NONSECURE	Located in PPGTT memory

Programming Notes
When execlists are enabled, this field reflects the effective security level and may not be the same as the Buffer Security Indicator written using MI_BATCH_BUFFER_START.

6 **2nd Level Buffer Security Indicator**

Project:	HSW
Source:	VideoCS, VideoCS2
Exists If:	//VCS, VCS2

If set, VCS is fetching 2nd level batch commands from a PPGTT address space. If clear, GGTT. If execlists are enabled and this is set, the batch buffer is non-secure and cannot execute privileged commands nor access privileged (GGTT) memory. It will be accessed via the PPGTT. If clear, this batch buffer is secure and will be accessed via the GGTT. Note: When execlists are enabled this field reflects the effective security level and may not be the same as the Buffer Security Indicator written using MI_BATCH_BUFFER_START.

Value	Name	Description
0h	MIBUFFER_SECURE **[Default]**	Located in GGTT memory
1h	MIBUFFER_NONSECURE	Located in PPGTT memory

5 **1st Level Buffer Security Indicator**

Project:	HSW
Format:	MI_1stBufferSecurityType

If set, BCS is fetching 1st level batch commands from a PPGTT address space. If clear, GGTT. If execlists are enabled and this is set, the batch buffer is non-secure and cannot execute privileged commands nor access privileged (GGTT) memory. It will be accessed via the PPGTT. If clear, this batch buffer is secure and will be accessed via the GGTT.

Note: When execlists are enabled this field reflects the effective security level and may not be the same as the Buffer Security Indicator written using MI_BATCH_BUFFER_START.

Value	Name	Description
0h	MIBUFFER_SECURE **[Default]**	Located in GGTT memory
1h	MIBUFFER_NONSECURE	Located in PPGTT memory

4 **Reserved**

4 **Reserved**

Project:	All
Source:	BlitterCS

BB_STATE - Batch Buffer State Register

		Exists If:	//BCS
		Format:	MBZ
	3:0	**Reserved**	
		Project:	All
		Format:	MBZ

Pending Head Pointer Register

UHPTR - Pending Head Pointer Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02134h
Name:	RCS Pending Head Pointer Register
ShortName:	RCS_UHPTR
Address:	12134h
Name:	VCS Pending Head Pointer Register
ShortName:	VCS_UHPTR
Address:	1A134h
Name:	VECS Pending Head Pointer Register
ShortName:	VECS_UHPTR
Valid Projects:	[DevHSW+]
Address:	22134h
Name:	BCS Pending Head Pointer Register
ShortName:	BCS_UHPTR

Programming Notes

Once SW uses UHPTR to preempt the existing workload, should explicitly program MI_SET_CONTEXT to save the preempted context status before submitting the new workload. In case SW doesn't want to save the state of the preempted context, it should at the minimum program RS_PREEMPT_STATUS to 0x0 so that the register status doesn't interfere with the new workloads.

DWord	Bit	Description
0	31:3	**Head Pointer Address** Format: GraphicsAddress[31:3] **Description** (Project): This register represents the GFX address offset where execution should continue in the ring buffer following execution of an MI_ARB_CHECK command. (HSW)
	2:1	**Reserved** Format: MBZ

UHPTR - Pending Head Pointer Register

	0	**Head Pointer Valid** **Description** / **Project** This bit is set by the software to request a pre-emption. / It is reset by hardware when an MI_ARB_CHECK command is parsed by the command streamer. The hardware uses the head pointer programmed in this register at the time the reset is generated. / HSW **Value** / **Name** / **Description** 0 / InValid / No valid updated head pointer register, resume execution at the current location in the ring buffer 1 / Valid / Indicates that there is an updated head pointer programmed in this register

Batch Buffer Head Pointer Register

BB_ADDR - Batch Buffer Head Pointer Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	02140h
Name:	RCS Batch Buffer Head Pointer Register
ShortName:	RCS_BB_ADDR
Address:	12140h
Name:	VCS Batch Buffer Head Pointer Register
ShortName:	VCS_BB_ADDR
Valid Projects:	HSW
Address:	1A140h
Name:	VECS Batch Buffer Head Pointer Register
ShortName:	VECS_BB_ADDR
Address:	22140h
Name:	BCS Batch Buffer Head Pointer Register
ShortName:	BCS_BB_ADDR

This register contains the current DWord Graphics Memory Address of the last-initiated batch buffer.

Programming Notes

Programming Restriction: This register should NEVER be programmed by driver. This is for HW internal use only.

DWord	Bit	Description
0	31:2	**Batch Buffer Head Pointer** Project: DevHSW+ Format: GraphicsAddress[31:2] This field specifies the DWord-aligned Graphics Memory Address where the last initiated Batch Buffer is currently fetching commands. If no batch buffer is currently active, the Valid bit will be 0 and this field will be meaningless.
	1	**Reserved** Format: MBZ

BB_ADDR - Batch Buffer Head Pointer Register

	0	**Valid** Format: U1 **Value** / **Name** / **Description** 0h / Invalid **[Default]** / Batch buffer Invalid 1h / Valid / Batch buffer Valid

2nd Level Batch Buffer Address

BBA_LEVEL2 - 2nd Level Batch Buffer Address

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	12144h
Valid Projects:	[HSW]

This register is to read the current value of the 2nd level batch buffer address. Since the 2nd level batch buffer logic is shared with the C6 work-around batch buffer, this also shows the work-around address when it is active.

DWord	Bit	Description
0	31:2	**WA Batch Buffer Address** Format: U30 Pointer to the WA Batch Buffer Address.
	1:0	**Reserved** Format: MBZ

VCS Counter for the bit stream decode engine

VCS_CNTR - VCS Counter for the bit stream decode engine

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0xFFFFFFFF
Access:	R/W
Size (in bits):	32
Address:	12178h-1217Bh
Valid Projects:	HSW

DWord	Bit	Description
0	31:0	**Count Value** Default Value: ffffffffh Writing a Zero value to this register starts the counting. Writing a Value of FFFF FFFF to this counter stops the counter.

VCS Threshold for the counter of bit stream decode engine

VCS_THRSH - VCS Threshold for the counter of bit stream decode engine

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00150000
Access:	R/W
Size (in bits):	32
Address:	1217Ch-1217Fh
Valid Projects:	HSW

DWord	Bit	Description
0	31:0	**Threshold Value** Default Value: 00150000h The value in this register reflects the number of clocks the bit stream decode engine is expected to run. If the value is exceeded the counter is reset and an interrupt may be enabled in the device.

VCS Ring Buffer Next Context ID Register

VCS_RNCID - VCS Ring Buffer Next Context ID Register	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	12198h-1219Fh
Valid Projects:	HSW

This register contains the next ring context ID associated with the ring buffer.

Programming Notes

The current context (RCCID) register can be updated indirectly from this register on a context switch event. Note that this can only be triggered when arbitration is enabled or if the current context runs dry (head pointer becomes equal to tail pointer).

DWord	Bit	Description
0	63:0	**Context ID** See Context Descriptor for VCS.

VCS Context Sizes

VCS_CXT_SIZE - VCS Context Sizes

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000 [NOVALIDPROJECTS] 0x00040D02 [HSW]
Access:	Read/32 bit Write Only
Size (in bits):	32
Address:	121A8h
Valid Projects:	HSW

DWord	Bit	Description
0	31:21	**Reserved** Format: MBZ
	20:16	**VCS Context Size** Format: U5 Value: 4h — Name: **[Default]** — Project: HSW
	15:13	**Reserved** Format: MBZ
	12:8	**VCR Context Size** Format: U5 Value: Dh — Name: **[Default]** — Project: HSW
	7:5	**Reserved** Format: MBZ
	4:0	**Execlist Context Size** Format: U5 Value: 2h — Name: **[Default]** — Project: HSW

VCS PPGTT Directory Cacheline Valid Register

VCS_PP_DCLV - VCS PPGTT Directory Cacheline Valid Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	12220h

This register controls update of the on-chip PPGTT Directory Cache during a context restore. Bits that are set will trigger the load of the corresponding 16 directory entry group.
This register is restored with context (prior to restoring the on-chip directory cache itself). This register is also restored when switching to a context whose LRCA matches the current CCID if the **Force PD Restore** bit is set in the context descriptor. The context image of this register must be updated and maintained by SW; SW should not normally need to read this register.
This register can also effectively be used to limit the size of a processes' virtual address space. Any access by a process that requires a PD entry in a set that is not enabled in this register will cause a fatal error, and no fetch of the PD entry will be attempted.

DWord	Bit	Description
0	63:32	**Reserved** Format: MBZ
	31:0	**PPGTT Directory Cache Restore [1..32] 16 entries** Format: Enable[32] If set, the [1st..32nd] 16 entries of the directory cache are considered valid and will be brought in on context restore. If clear, these entries are considered invalid and fetch of these entries will not be attempted.

Video Mode Register

MFX_MODE - Video Mode Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS, VideoCS2
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	1229Ch
Valid Projects:	HSW

DWord	Bit	Description
0	31:16	**Mask Bits** Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:14	**Reserved** Project: HSW Format: MBZ
	13:10	**Reserved** Project: All Format: MBZ
	9	**Per-Process GTT Enable** Format: Enable Per-Process GTT BS Mode Enable **Value** / **Name** / **Description** 0h / PPGTT Disable **[Default]** / When clear, the Global GTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space. 1h / PPGTT Enable / When set, the PPGTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.
	8	**Reserved** Project: HSW

MFX_MODE - Video Mode Register

	7	**Reserved** Project: HSW Format: MBZ
	6:5	**Reserved** Project: All Format: MBZ
	4:0	**Reserved** Project: HSW Format: MBZ

VCS Reported Timestamp Count

VCS_TIMESTAMP - VCS Reported Timestamp Count

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000, 0x00000000
Access:	RO. This register is not set by the context restore.
Size (in bits):	64
Address:	12358h
Valid Projects:	HSW

This register provides an elapsed real-time value that can be used as a timestamp. This register is not reset by a graphics reset. It will maintain its value unless a full chipset reset is performed.
Note: This timestamp register reflects the value of the PCU TSC. The PCU TSC counts 10ns increments; this timestamp reflects bits 38:3 of the TSC (i.e. 80ns granularity, rolling over every 1.5 hours).

DWord	Bit	Description
0	63:36	**Reserved** Format: MBZ
	35:0	**Timestamp Value** Format: U36 This register toggles every 80 ns. The upper 28 bits are zero.

MFD Error Status

MFD_ERROR_STATUS - MFD Error Status

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12400h
Valid Projects:	HSW

This register stores the error status flags and count reports by the bit-stream decoder.
This register is not part of hardware context save and restore. Driver should read the content prior to starting a new batch/frame.

DWord	Bit	Description
0	31:16	**Number of MB Concealment** Exists If: //AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True Format: U16 This 16-bit field indicates the number of MB is concealmed by hardware. This field is clear at the start of decoding a new frame.
	31:16	**Number of Error Events** Exists If: //JPEG == True Format: U16 This 16-bit field indicates the number of error events detected during decoding the current frame. This field is clear at the start of decoding a new frame.
	15:0	**Bit-stream Error flags** Bit-stream error detected by the VLD bit-steram decoder. These flags are reset at the beginning of a frame and updated until starting of another frame. AVC CAVLC: Please refer to AVC CAVLC table for each bit field AVC CABAC: Please refer to AVC CABAC table for each bit field VC1: Please refer to VC1 table for each bit field MPEG2: Please refer to MPEG2 table for each bit field JPEG: Please refer to JPEG table for each bit field

Bitstream Output Minimal Size Padding Count Report Register

MFC_AVC_MINSIZE_PADDING_COUNT - Bitstream Output Minimal Size Padding Count Report Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12414h
Name:	VDBOX1
Valid Projects:	HSW

This register stores the count in bytes of **minimal size padding insertion. It is primarily provided for statistical data gathering.** This register is part of the context save and restore.

DWord	Bit	Description
0	31:0	**MFC AVC MinSize Padding Count** Total number of bytes in the bitstream output contributing to minimal size padding operation. This count is updated each time when the padding count is incremented.

MFD Picture Parameter

MFD_PICTURE_PARAM - MFD Picture Parameter	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	12420h
Valid Projects:	HSW

DWord	Bit	Description
0	31:0	**Reserved** Format: MBZ

MFX Pipeline Status Flags

MFX_STATUS_FLAGS - MFX Pipeline Status Flags

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12438h
Valid Projects:	HSW

This register stores the various pipeline status flags.
This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:17	**Reserved** Format: MBZ
	16	**MFX Active** Frame decoding/encoding is in progress. Set on frame_start; clear on frame_end.
	15:10	**Reserved** Format: MBZ
	9	**Streamout Enable**
	8	**Reserved**
	7	**Post Deblocking Mode Enable**
	6	**Pre Deblocking Mode Enable**
	5	**Decoder Mode Select** Value: 0 — Name: Configure the MFD Engine for VLD Mode Value: 1 — Name: Configure the MFD Engine for IT Mode
	4	**Codec Select** Value: 0 — Name: Decode Value: 1 — Name: Encode
	3:2	**Video Mode**

MFX_STATUS_FLAGS - MFX Pipeline Status Flags

		Value: 00b — Name: MPEG2 Value: 01b — Name: VC1 Value: 10b — Name: AVC Value: 11b — Name: JPEG
	1	**Decoder Short Format Mode** Value: 0 — Name: — Description: AVC/VC1 Short Format Mode is in use Value: 1 — Name: — Description: AVC/VC1 Long Format Mode is in use
	0	**Stitch Mode** Value: 0b — Name: — Description: Not in Stitch Mode Value: 1b — Name: — Description: In the Special Stitch Mode

MFX Frame Performance Count

MFX_FRAME_PERFORMANCE_CT - MFX Frame Performance Count

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12460h
Valid Projects:	HSW

This register stores the number of clock cycles spent decoding/encoding the current frame.
This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:0	**MFX Frame Performance Count** Total number of clocks between frame start and frame end. This count is incremented on crm_clk

MFX Slice Performance Count

MFX_SLICE_PERFORM_CT - MFX Slice Performance Count	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12464h
Valid Projects:	HSW

This register stores the number of clock cycles spent decoding/encoding the current slice.
This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:0	**MFX Frame Performance Count** Total number of clocks between slice start and slice end. This count is incremented on crm_clk

MFX Frame Macroblock Count

MFX_MB_COUNT - MFX Frame Macroblock Count	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12468h
Valid Projects:	HSW

This register stores the number of Macro-blocks decoded/encoded in current frame.
This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:0	**MFX Frame Macro-block Count** Total number of Macro-block decoded/encoded in current frame. This number is used with frame performance count to derive clk/mb.

MFX Frame BitStream SE/BIN Count

MFX_SE-BIN_CT - MFX Frame BitStream SE/BIN Count	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1246Ch
Valid Projects:	HSW

This register stores the number of BINs (AVC CABAC) and SEs (CAVLD, VLD) decoded in a frame.
This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:0	**MFX Frame Bit-stream SE/BIN Count** Total number of BINs/SEs decoded in current frame. This number is used with frame performance count to derive Bin/clk or SE/clk.

MFX_Memory_Latency_Count1

MFX_LAT_CT1 - MFX_Memory_Latency_Count1	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12470h
Valid Projects:	HSW

This register stores the max and min memory latency counts reported on reference read requests.
This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:24	**Max Request Count** This field indicates the maximum number of requests allowed by the memory sub-system channel.
	23:16	**Current Request Count** This field indicates the number of requests currently outstanding in the memory sub-system. This field should report with a value of zero at the end of frame; otherwise the motion compensation engine is most likely hung waiting for read data to be returned from sub-system.
	15:8	**MFX Reference picture read request - Max Latency Count in 8xMedia clock cycles** This field reports the maximum memory latency count on all reference reads requested by the motion compensation engine.
	7:0	**MFX Reference picture read request - Min Latency Count in 8xMedia clock cycles** This field reports the minimum memory latency count on all reference reads requested by the motion compensation engine.

MFX Memory Latency Count2

MFX_LAT_CT2 - MFX Memory Latency Count2	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12474h
Valid Projects:	HSW

This register stores the accumulative memory latency count on reference picture read requests.
This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:26	**Reserved** Format: MBZ
	25:0	**MFX Reference picture read request - Accumulative Memory Latency Count for the entire frame in 8xMedia clock cycles** The accumulative memory latency count of all reference reads requested by motion compensative engine per frame. This number is used with **MFX Frame Motion Comp Read Count** to derive average memory latency.

MFX Memory Latency Count3

MFX_LAT_CT3 - MFX Memory Latency Count3	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12478h
Valid Projects:	HSW

This register stores the max and min memory latency counts reported on row-stored/bit-stream read requests. Max and current requests into memory sub-system engine.
This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:24	**Max Request Count** This field indicates the maximum number of requests allowed by the memory sub-system channel.
	23:16	**Current Request Count** This field indicates the number of requests currently outstanding in the memory sub-system. This field should report with a value of zero at the end of frame; otherwise the pre-fetch engine most likely hung waiting for read data to be returned from sub-system.
	15:8	**MFX row-stored/bit-stream read request - Max Latency Count in 8xMedia clock cycles** This field reports the maximum memory latency count on all row-stored/bit-stream reads requested by the memory pre-fetch engine.
	7:0	**MFX row-stored/bit-stream read request - Min Latency Count in 8xMedia clock cycles** This field reports the minimum memory latency count on all row-stored/bit-stream reads requested by the memory pre-fetch engine.

MFX Memory Latency Count4

MFX_LAT_CT4 - MFX Memory Latency Count4	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1247Ch
Valid Projects:	HSW

This register stores the accumulative memory latency count on row-stored/bit-stream read requests.
This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:26	**Reserved** Format: MBZ
	25:0	**MFX row-stored/bit-stream read request - Accumulative Memory Latency Count for the entire frame in 8xMedia clock cycles** The accumulative memory latency count of all row-stored/bit-stream reads requested by pre-fetch engine per frame. This number is used with **Frame row-stored/bit-stream memory read count** to derive average memory latency.

MFX Frame Row-Stored/BitStream Read Count

MFX_ROW-PER-BS_COUNT - MFX Frame Row-Stored/BitStream Read Count

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12480h
Valid Projects:	HSW

This register stores the total number of row-stored/bit-stream read requests made by the pre-fetch engine per frame.
This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**MFX row-stored/bit-stream read request Count** Total number of row-stored/bit-stream read requests sent by the memory pre-fetch engine per frame.

MFX Frame Motion Comp Read Count

MFX_READ_CT - MFX Frame Motion Comp Read Count	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12484h

This register stores the total number of reference picture read requests made by the Motion Compensation engine per frame.
This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:20	**Reserved** Format: MBZ
	19:0	**MFX Frame Motion Comp CL read request Count** Total number of reference picture read requests by the motion compensation engine per frame.

MFX Frame Motion Comp Miss Count

MFX_MISS_CT - MFX Frame Motion Comp Miss Count	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12488h
Valid Projects:	HSW

This register stores the total number of cacheline hits occurred in the motion compensation cache per frame.
This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**MFX Frame Motion Comp cache miss Count** Total number of CL misses occurred in the 12KB cache of the motion compensation engine per frame. This number is used along with **MFX Frame Motion Comp Read Count** to derive motion comp cache miss/hit ratio.

Reported Bitstream Output Byte Count per Frame Register

MFC_BITSTREAM_BYTECOUNT_FRAME - Reported Bitstream Output Byte Count per Frame Register	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	124A0h
Valid Projects:	HSW

This register stores the count of bytes of the bitstream output per frame

DWord	Bit	Description
0	31:0	**MFC Bitstream Byte Count per Frame** Total number of bytes in the bitstream output per frame from the encoder. This includes header/tail/byte alignment/data bytes/EMU (emulation) bytes/cabac-zero word insertion/padding insertion. This count is updated for every time the internal bitstream counter is incremented and its reset at image start.

Reported Bitstream Output Bit Count for Syntax Elements Only Register

MFC_BITSTREAM_SE_BITCOUNT_FRAME - Reported Bitstream Output Bit Count for Syntax Elements Only Register	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	124A4h
Valid Projects:	HSW

This register stores the count of number of bits in the bitstream due to syntax elements only. This excludes header/ byte alignment /tail/EMU/CABAC-0word/padding bits but includes the stop-one-bit. This register is part of the context save and restore.

DWord	Bit	Description
0	31:0	**MFC Bitstream Syntax Element Only Bit Count** Total number of bits in the bitstream output due to syntax elements only. It includes the data bytes only. This count is updated for every time the internal bitstream counter is incremented and its reset at image start.

Reported Bitstream Output CABAC Bin Count Register

MFC_AVC_CABAC_BIN_COUNT_FRAME - Reported Bitstream Output CABAC Bin Count Register	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	124A8h
Valid Projects:	HSW

This register stores the count of number of bins per frame.

DWord	Bit	Description
0	31:0	**MFC AVC Cabac Bin Count** Total number of BINs in the bitstream output per frame from the encoder. This count is updated for every time the bin counter is incremented and its reset at image start.

MFC_AVC_CABAC_INSERTION_COUNT

AVC_CABAC_INSERTION_COUNT - MFC_AVC_CABAC_INSERTION_COUNT	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	124ACh
Valid Projects:	HSW

This register stores the count in bytes of **CABAC ZERO_WORD insertion. It is primarily provided for statistical data gathering.**

DWord	Bit	Description
0	31:0	**MFC AVC Cabac Insertion Count** Total number of bytes in the bitstream output before for the CABAC zero word insertion. This count is updated each time when the insertion count is incremented.

MFC Image Status Mask

MFC_IMAGE_STATUS_MASK - MFC Image Status Mask	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	124B4h
Valid Projects:	HSW

This register stores the image status(flags).

DWord	Bit	Description
0	31:0	**Control Mask** Control Mask for dynamic frame repeat.

MFC Image Status Control

MFC_IMAGE_STATUS_CONTROL - MFC Image Status Control

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	124B8h
Valid Projects:	HSW

This register stores the suggested data for next frame in multi-pass.

DWord	Bit	Description
0	31:24	**Cumulative slice delta QP**
	23:16	**QP Value** suggested slice QP delta value for frame level Rate control. This value can be +ve or -ve
	15	**QP-Polarity Change** Cumulative slice delta QP polarity change.
	14:13	**Num-Pass Polarity Change** Number of passes after cumulative slice delta QP polarity changes.
	12	**Reserved** Project: HSW Format: MBZ
	11:8	**Total Num-Pass**
	7:4	**Reserved** Format: MBZ
	3	**Reserved** Project: HSW Format: MBZ
	2	**Panic** Panic triggered to avoid too big packed file.
	1	**Frame Bit Count** Frame Bit count over-run/under-run flag
	0	**Max Conformance Flag** Max Macroblock conformance flag or Frame Bit count over-run/under-run

MFC QP Status Count

MFC_QUP_CT - MFC QP Status Count	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	124BCh
Valid Projects:	HSW

This register stores the suggested QP COUNTS in multi-pass.

DWord	Bit	Description
0	31:24	**Cumulative QP Adjust** Format: U8 Cumulative QP adjustment after multiple passes. If there is no need to multi-pass, this value would be zero. (This is in sign magnitude form).
	23:0	**Cumulative QP** Format: U24 Cumulative QP for all MB of a Frame (Can be used for computing average QP).

VCS_PREEMPTION_HINT_UDW

VCS_PREEMPTION_HINT_UDW - VCS_PREEMPTION_HINT_UDW

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	124C8h
Valid Projects:	HSW

This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the Batch Buffer corresponding to MI_ARB_CHECK command called Preemption Hint Address.

Programming Notes

Programming Restriction:
This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of UHPTR being sampled by a given MI_ARB_CHK in command stream.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Preempted Hint Address Upper DWORD** Format: GraphicsAddress[47:32] This field contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the batch buffer when Preemption Hint is set to Batch Buffer. This field is not valid when Preemption Hint is set to Ring Buffer.

Bitstream Output Byte Count Per Slice Report Register

MFC_BITSTREAM_BYTECOUNT_SLICE - Bitstream Output Byte Count Per Slice Report Register	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	124D0h
Valid Projects:	HSW

This register stores the count of bytes of the bitstream output. This register is part of the context save and restore.

DWord	Bit	Description
0	31:0	**MFC Bitstream Byte Count** Total number of bytes in the bitstream output from the encoder. This count is updated for every time the internal bitstream counter is incremented.

Bitstream Output Bit Count for the last Syntax Element Report Register

MFC_BITSTREAM_SE_BITCOUNT_SLICE - Bitstream Output Bit Count for the last Syntax Element Report Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	124D4h
Name:	VDBOX1
Valid Projects:	HSW

This register stores the count of number of bits in the bitstream for the last syntax element before padding. The bit count is before the byte-aligned alignment padding insertion, but includes the stop-one-bit. This register is part of the context save and restore.

DWord	Bit	Description
0	31:0	**MFC Bitstream Syntax Element Bit Count** Total number of bits in the bitstream output before padding. This count is updated each time the internal counter is incremented.

PAK_Stream-Out Report (Warnings)

PAK_WARN - PAK_Stream-Out Report (Warnings)	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	124E4h
Valid Projects:	HSW

DWord	Bit	Description
0	31:22	**Reserved** Project: All Format: MBZ
	21	**Skip Run > 8192 (AVC)**
	20	**Incorrect SkipMB (AVC and mpeg2)**
	19	**Incorrect MV difference for dual-prime MB (mpeg2)**
	18	**End of Slice signal missing on last MB of a Row(mpeg2)**
	17	**Incorrect DCT type for field picture**
	16	**MVs are not within defined range by fcode**
	15:8	**MB Y-position**
	7:0	**MB X-position**

PAK_Stream-Out Report (Errors)

PAK_ERR - PAK_Stream-Out Report (Errors)	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	124E8h
Valid Projects:	HSW

DWord	Bit	Description
0	31:22	**Reserved** Format: MBZ
	21	**Incorrect IntraMBFlag in I-slice(AVCf)**
	20	**Out of Range Symbol Code(AVC/mpeg2)**
	19	**Incorrect MBType(AVC/mpeg2**
	18	**Motion Vectors are not inside the frame boundary(mpeg2)**
	17	**Scale code is zero(mpeg2)**
	16	**Incorrect DCTtype for given motionType(mpeg2)**
	15:8	**MB Y-position**
	7:0	**MB X-position**

PAK Report Running Status

PAK_REPORT_STAT - PAK Report Running Status	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	124ECh
Valid Projects:	HSW

DWord	Bit	Description
0	31:1	**Reserved**
	0	**PAK Status** Value / Name / Description 0 / / PAK engine is IDLE 1 / / PAK engine is currently generating bit stream.

MFC_AVC Bitstream Decoding Front-End Parsing Logic Error Counter

MFC_VIN_AVD_ERROR_CNTR - MFC_AVC Bitstream Decoding Front-End Parsing Logic Error Counter

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	12804h
Valid Projects:	HSW

DWord	Bit	Description
0 avd_error_flagsR[31:0]	31:0	**Reserved** Format: MBZ

TLBPEND Control Register

GFX_PEND_TLB - TLBPEND Control Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	14040h

Max Outstanding Media pending TLB requests

DWord	Bit	Description
0	31	**Reserved** Project: HSW Format: MBZ
	30	**Reserved** Format: MBZ
	29:24	**VMX BS Limit Count** Format: U6 This is the MAX number of Allowed internal pending read requests which require a TLB read.
	23	**VMC Limit Enable bit** Format: U1 This bit is used to enable the pending TLB requests limitation function for the VMC. When set, the number of internal pending read requests which require a TLB read will not exceed the programmed counter value.
	22	**Reserved** Format: MBZ
	21:16	**VMC TLB Limit Count** Format: U6 This is the MAX number of Allowed internal pending read requests which require a TLB read.
	15	**VMXRS Limit Enable bit** Format: U1

GFX_PEND_TLB - TLBPEND Control Register

		This bit is used to enable the pending TLB requests limitation function for the VMX Row store. When set, the number of internal pending read requests which require a TLB read will not exceed the programmed counter value.
	14	**Reserved** Format: MBZ
	13:8	**VMX RS Random Accsess TLB Limit Count** Format: U6 This is the MAX number of Allowed internal pending read requests which require a TLB read.
	7	**VCS Limit Enable bit** Format: U1 This bit is used to enable the pending TLB requests limitation function for the Command Streamer. When set, the number of internal pending read requests which require a TLB read will not exceed the programmed counter value.
	6	**Reserved** Format: MBZ
	5:0	**VCS TLB Limit Count** Format: U6 This is the MAX number of Allowed internal pending read requests which require a TLB read.

GAC_GAB Arbitration Counters Register 1

GAC_ARB_CTL_REG - GAC_GAB Arbitration Counters Register 1

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00400002
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	14050h

GAC_GAB R/RO/W Arbitration Control Register

DWord	Bit	Description
0	31	**GAC write request Limit Enable** Format: U1 As long As there is no conflict between GAC and GAB ,GAC will alow whoever shows up (if media present and no GAB, let meda and vice versa). If both are present, start counting and switch when programmable no of request is expired. Allow only One GAB request and reset the counter. Counter only counts while we service a particular client and another client is present, else counter will reset.
	30	**VLF Final write Limit Enable** Format: MBZ As long as there is no conflict Between VCS MFD and VLF Final Write, GAC will allow whoever shows up (if VLF present and no VCSMFD, Let VLF and vice versa). If both are present, Start counting and when programmable no of request is expired. Allow only One VCSMFD request And counter will reset. Counter only counts while we service a particular client and another client is present, else counter will reset.
	29:24	**Write Req Limit Count** Format: U6 The value programmed determines the number of GAC/VLF Writes will allow for Each time.
	23	**GAC/GAB Cascaded Read Only Limit Enable** Format: U1 As long as there is no conflict between GAC and GAB Read Requests, GAC will allow whoever shows up (if GAC present and no GAB, Let GAC and vice versa). If both are present, Start counting and switch when programmable no of request from either side is expired (reset the counter when switch). Counter only counts while we service a particular client and other client is

GAC_ARB_CTL_REG - GAC_GAB Arbitration Counters Register 1

	present, else counter will reset.
22	**Fixed Priority Setting** Format: MBZ Once programmable counter is disabled, GAC uses the fixed arbitration setting given in this register setting. Value: 0 — Name: GAC Value: 1 — Name: GAB **[Default]**
21	**Reserved** Format: MBZ
20:16	**GAC/GAB Read Only Limit Counter Value** Format: U5 This is the Maximum number of Read requests Allowed from Each Cascaded Agent. Default 0
15	**GAC/GAB Cascaded Read Limit Enable** Format: U1 As long as there is no conflict Between GAC and GAB Read Only Requests, GAC will allow whoever shows up (if GAC present and no GAB, Let GAC and vice versa). If both are present, Start counting and switch when programmable no of request from either side is expired (reset the counter when switch). Counter only counts while we service a particular client and other client is present, else counter will reset. Default 0
14	**Default priority 0-GAC, 1-GAB** Format: MBZ Default 0
13	**Reserved** Format: MBZ
12:8	**GAC/GAB Read Limit Counter Value** Format: U5 This is the Maximum number of Read requests allowed from Each Cascaded Agent.
7:6	**Reserved** Format: MBZ
5:0	**No of Global GTT Entries Valid in PPGTT mode in TLB064** Default Value: 000010b

GAC_ARB_CTL_REG - GAC_GAB Arbitration Counters Register 1		
		Format: U6 Minimum value the PPGGTT LRA can have (effectively partitioning the TLB between PPGTT and GGTT). Currently, only 2 entries are allocated to GGTT in ASmodel. TLB64 is shared by GGTT and PPGTT entries, are 2 LRAs, the GGTT one running from 0 up to PPGTT_MIN -1 (which is 2, but could be changed if needed), and the PPGTT one running from PPGTT_MIN up to 63.

Media Arbiter Error Report Register

GAC_ERROR - Media Arbiter Error Report Register	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	140A0h
These registers are directly mapped for the Error Reporting bits.	

DWord	Bit	Description
0	31:11	**Reserved/ECO**
	10	**Invalid Page Directory entry VTD translation error** PD entry's VTD translation generated an error (HPA is not accessible for DMA read or write)valid bit is 0Hardware Status Page Fault errorHWSP's GTT translation generated a page fault (GTT entry not valid)
	9	**Reserved**
	8	**Unloaded PD error** The Cache Line containing a PD entry being accessed was marked as invalid in the last PD load cycle.
	7	**Hardware Page Directory Status Pageentry VTD translation error** The Global Hardware PStatus Page (HWSP) VTD entry's VTD translation generated an error (HPA Page is not accessible for DMA read or write)
	6	**Hardware StatusContext Page VTD translation error** A PD Context Page'entry's VTD translation generated an error (HPA is not accessible for DMA read or write)
	5	**Context TLB Page VTD translation error** A Context TLB Page's VTD translation generated an error (HPA is not accessible for DMA read or write)
	4	**Hardware Status Page VTD Fault errortranslation error** HWSP's VTD GTT translation generated a page fault (GTT entry not valid)n error
	3	**Hardware Status Page VTD translation error** The Global Hardware Status Page (HWSP's) VTD translation generated an error (HPA Page is not accessible for DMA read or write)
	2	**Reserved**
	1	**Context Page Fault Error**

GAC_ERROR - Media Arbiter Error Report Register		
		A Context Page's GTT translation generated a page fault (GTT entry not valid)
	0	**TLB Page Fault Error** A TLB Page's GTT translation generated a page fault (GTT entry not valid)

VCS Section 0 of TLBPEND Entry

VCS_TLBPEND_SEC0 - VCS Section 0 of TLBPEND Entry		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	14400h-14403h	
This register is directly mapped to the TLBPEND Array in the Graphic Arbiter.		
DWord	**Bit**	**Description**
0	31	**vtstatus** This bit will be used in conjunction with the ready bit to determine the stage of the translation. See table below.
	30:28	**GTT bits** Bits 3:1 of the GTT entry used to translate the Virtual Address. 000 if translation is pending.
	27:0	**Current address** The value of this field depends on the stage of the TLB translation for this entry: **VA** - bits 27:20 = 00, bits 19:0 = Bits 31:12 of the Virtual Address of the cycle.

VCS Section 1 of TLBPEND Entry

VCS_TLBPEND_SEC1 - VCS Section 1 of TLBPEND Entry

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1

Address: 14500h-14503h

This register is directly mapped to the current Virtual Addresses in the MTTLB (Texture and constant cache TLB).

DWord	Bit	Description
0	31:28	**Current address** Bits 9:6 of the Virtual Address of the cycle.
	27:24	**Cacheability Control Bits** Bit 26 (bit 2 within the four-bit field) is the Graphics Data Type (GFDT) bit. It is the GFDT bit for this surface when writes occur. GFDT can also be set by the GTT. The effective GFDT is the logical OR of this field with the GFDT from the GTT entry. This field is ignored for reads. Bits 25:24 (bits 1:0 within the four-bit field) contain the Cacheability Control field, which controls cacheability in the mid-level cache (MLC) and last-level cache (LLC) as described in the following table: **Value** / **Description** 00b – Use cacheability control bits from GTT entry. 01b – Data is not cached in LLC or MLC. 10b – Data is cached in LLC but not MLC. 11b – Data is cached in both LLC and MLC.
	23	**ZLR bit** Flag to indicate this is a zero length read (A read used to calculate a Physical Address for a write).
	22:4	**TAG** Cycle identification TAG.
	3:0	**SRC ID** Encoding of unit generating this cycle **Constant** / **Value** **SRCID** **VCS_RD_SRCID** – "00000" **VMC_RD_SRCID** – "00001"

VCS_TLBPEND_SEC1 - VCS Section 1 of TLBPEND Entry

VMX_RARD_SRCID	"00010"
VMX_BSRD_SRCID	"00011"
VMX_RSRD_SRCID	"00100"
VIP_RD_SRCID	"00101"
VLF_RD_SRCID	"00110"
VDS_ZLRD_SRCID	"00111"
VCS_WR_SRCID	"01000"
VMX_BSWR_SRCID	"01001"
VDS_WR_SRCID	"01010"
VOP_WR_SRCID	"01011"
VLF_RSWR_SRCID	"01100"
VLF_FDWR_SRCID	"01101"
VMX_RSWR_SRCID	"01110"
BSP_WR_SRCID	"01111"
VCR_RD_SRCID	"10001"
VCR_WR_SRCID	"10010"
VCS_RD_PROBE	"10011"

VCS Section 2 of TLBPEND Entry

VCS_TLBPEND_SEC2 - VCS Section 2 of TLBPEND Entry	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	14600h-14603h

This register is directly mapped to the current Virtual Addresses in the MTTLB (Texture and constant cache TLB).

DWord	Bit	Description
0	31:11	**Reserved**
	10:8	**Current address** Bits 11:9 of the Virtual Address of the cycle.
	7:0	**PAT entry** Location of Physical Address in Physical Address Table.

VCS Valid Bit Vector 0 for TLBPEND Registers

VCS_TLBPEND_VLD0 - VCS Valid Bit Vector 0 for TLBPEND Registers		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	14700h-14703h	
This register contains the valid bits for entries 0-31 of TLBPEND structure (Cycles pending TLB translation).		
DWord	**Bit**	**Description**
0	31:0	**Valid bits per entry**

VCS Valid Bit Vector 1 for TLBPEND Registers

VCS_TLBPEND_VLD1 - VCS Valid Bit Vector 1 for TLBPEND Registers	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	14704h-14707h

This register contains the valid bits for entries 32-63 of TLBPEND structure (Cycles pending TLB translation).

DWord	Bit	Description
0	31:0	**Valid bits per entry**

VCS Ready Bit Vector 0 for TLBPEND Registers

VCS_TLBPEND_RDY0 - VCS Ready Bit Vector 0 for TLBPEND Registers	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	14708h-1470Bh
This register contains the ready bits for entries 0-31 of TLBPEND structure (Cycles pending TLB translation).	

DWord	Bit	Description
0	31:0	**Ready bits per entry**

VCS Ready Bit Vector 1 for TLBPEND Registers

VCS_TLBPEND_RDY1 - VCS Ready Bit Vector 1 for TLBPEND Registers		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	1470Ch-1470Fh	
This register contains the ready bits for entries 32-63 of TLBPEND structure (Cycles pending TLB translation).		
DWord	**Bit**	**Description**
0	31:0	**Ready bits per entry**

Valid Bit Vector 0 for TLB064

MTTLB064_VLD0 - Valid Bit Vector 0 for TLB064	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	14780h-14783h

This register contains the valid bits for entries 0-31 of MTTLB (Texture and constant cache TLB).

DWord	Bit	Description
0	31:0	**Valid bits per entry**

Valid Bit Vector 1 for TLB064

MTTLB064_VLD1 - Valid Bit Vector 1 for TLB064	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	14784h-14787h

This register contains the valid bits for entries 0-31 of MTTLB (Texture and constant cache TLB).

DWord	Bit	Description
0	31:0	**Valid bits per entry**

Valid Bit Vector 0 for TLB132

MTTLB132_VLD0 - Valid Bit Vector 0 for TLB132	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	14788h-1478Bh

This register contains the valid bits for entries 0-31 of MTTLB (Texture and constant cache TLB).

DWord	Bit	Description
0	31:0	**Valid bits per entry**

Valid Bit Vector 1 for TLB132

MTTLB132_VLD1 - Valid Bit Vector 1 for TLB132	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1478Ch-1478Fh
This register contains the valid bits for entries 0-31 of MTTLB (Texture and constant cache TLB).	

DWord	Bit	Description
0	31:0	**Valid bits per entry**

Valid Bit Vector 0 for TLB232

MTTLB232_VLD0 - Valid Bit Vector 0 for TLB232	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	14790h-14793h
This register contains the valid bits for entries 0-31 of MTTLB (Texture and constant cache TLB).	

DWord	Bit	Description
0	31:0	**Valid bits per entry**

Valid Bit Vector 1 for TLB232

MTTLB232_VLD1 - Valid Bit Vector 1 for TLB232	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	14794h-14797h

This register contains the valid bits for entries 0-31 of MTTLB (Texture and constant cache TLB).

DWord	Bit	Description
0	31:0	**Valid bits per entry**

Valid Bit Vector 0 for TLB304

MTTLB304_VLD0 - Valid Bit Vector 0 for TLB304	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	14798h-1479Bh

This register contains the valid bits for entries 0-31 of MTTLB (Texture and constant cache TLB).

DWord	Bit	Description
0	31:0	**Valid bits per entry**

Valid Bit Vector 1 for TLB304

MTTLB304_VLD1 - Valid Bit Vector 1 for TLB304	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1479Ch-1479Fh

This register contains the valid bits for entries 0-31 of MTTLB (Texture and constant cache TLB). Default Value = 00000000h Trusted Type = 1

DWord	Bit	Description
0	31:0	**Valid bits per entry**

TLB064_VA Virtual Page Address Registers

TLB064_VA - TLB064_VA Virtual Page Address Registers

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	14800h-14803h

This register is directly mapped to the current Virtual Addresses in the TLB064 (VCS and VMC TLB).

DWord	Bit	Description
0	31:12	**Address** Format: GraphicsAddress[31:12] Page virtual address.
	11:0	**Reserved** Format: MBZ

TLB132_VA Virtual Page Address Registers

TLB132_VA - TLB132_VA Virtual Page Address Registers

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	14900h-14903h

These registers are directly mapped to the current Virtual Addresses in the TLB132 (All The Media Clients TLB). Default Value = UUUUUUUUh Trusted Type = 1

DWord	Bit	Description
0	31:12	**Address** Format: GraphicsAddress[31:12] Page virtual address.
	11:0	**Reserved** Format: MBZ

TLB232_VA Virtual Page Address Registers

TLB232_VA - TLB232_VA Virtual Page Address Registers

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	14A00h-14A03h

This register is directly mapped to the current Virtual Addresses in the TLB232 (VDS and VLF FW TLB).

DWord	Bit	Description
0	31:12	**Address** Format: GraphicsAddress[31:12] Page virtual address.
	11:0	**Reserved** Format: MBZ

TLB304_VA Virtual Page Address Registers

TLB304_VA - TLB304_VA Virtual Page Address Registers		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	14B00h-14B03h	
This register is directly mapped to the current Virtual Addresses in the TLB304 (VCR TLB).		
DWord	**Bit**	**Description**
0	31:12	**Address** Format: GraphicsAddress[31:12] Page virtual address.
	11:0	**Reserved** Format: MBZ

VECS Execute Condition Code Register

VECS_EXCC - VECS Execute Condition Code Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoEnhancementCS
Default Value:	0x00000000
Access:	R/W,RO
Size (in bits):	32
Trusted Type:	1
Address:	1A028h

This register contains user defined and hardware generated conditions that are used by MI_WAIT_FOR_EVENT commands. An MI_WAIT_FOR_EVENT instruction excludes the executing ring from arbitration if the selected event evaluates to a "1", while instruction is discarded if the condition evaluates to a "0". Once excluded a ring is enabled into arbitration when the selected condition evaluates to a "0".
This register also contains control for the invalidation of indirect state pointers on context restore.

DWord	Bit	Description
0	31:16	**Mask Bits** Format: Mask[15:0] These bits serves as a write enable for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.
	15:5	**Reserved** Format: MBZ
	4:0	**User Defined Condition Codes** Project: HSW The software may signal a Stream Semaphore by setting the Mask bit and Signal Bit together to match the bit field specified in a WAIT_FOR_EVENT (Semaphore).

Video Enhancement/Blitter Semaphore Sync Register

VEBSYNC - Video Enhancement/Blitter Semaphore Sync Register	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoEnhancementCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	1A040h

This register is written by BCS, read by VECS.

DWord	Bit	Description
0	31:0	**Semaphore Data** SeSemaphore data for synchronization between video enhancement engine and blitter engine.

Video Enhancement/Render Semaphore Sync Register

VERSYNC - Video Enhancement/Render Semaphore Sync Register	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoEnhancementCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	1A044h

This register is written by CS, read by VECS.

DWord	Bit	Description
0	31:0	**Semaphore Data** Semaphore data for synchronization between video enhancement engine and render engine.

Video Enhancement/Video Semaphore Sync Register

VEVSYNC - Video Enhancement/Video Semaphore Sync Register		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	VideoEnhancementCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	1A048h	
This register is written by CS, read by VECS.		
DWord	**Bit**	**Description**
0	31:0	**Semaphore Data** Semaphore data for synchronization between video enhancement engine and video codec engine.

VECS Sleep State and PSMI Control

VECS_PSMI_CTRL - VECS Sleep State and PSMI Control

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoEnhancementCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1

Address: 1A050h

This register is to be used to control all aspects of PSMI and power saving functions.

DWord	Bit	Description
0	31:16	**Mask Bits** Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:13	**Reserved** Project: All Format: MBZ
	12	**Reserved** Project: HSW Format: MBZ
	11:5	**Reserved** Format: MBZ
	4	**GO Indicator** Project: All Access: RO Format: GO This is a read only field. Writing to this bit is undefined. To simplify power saving and soft reset flows, the power management hardware has the ability to block all pending memory cycles of the render pipe. When GO=0, all cycles are blocked. All CPD enter/exit and RC6 enter/exit has this bit set to 0.

Value	Name	Description	Project
0h	Disable **[Default]**	All pending memory read cycles are complete. No new cycles permitted except for power context or PSMI cycles	All

	1h	Enable	Normal execution	All

3 IDLE Indicator

Default Value:	0h Render is assumed NOT IDLE coming out of reset
Project:	All
Access:	RO
Format:	IDLE

This is a read only field. Writing to this bit is undefined. This indicates what power management thinks what state the render pipe is in. That is, if set, the full handshake between render and power management has occured and most likely the render clocks are currently turned off.

2 IDLE Flush Disable

Default Value:	0h Flush Enabled
Project:	All
Format:	Disable

For normal execution, before telling the power management hardware that the render pipe is IDLE, inserts a pipelined flush after the top of the pipe (command stream) is IDLE for MAXCNT (0x2054). Setting this bit disables the flush. After MAXCNT is reached, the command streamer will immediately send the IDLE indicator to power management.

1 Reserved

Project:	All
Format:	MBZ

0 Reserved

Project:	All

VECS IDLE Max Count

VECS_PWRCTX_MAXCNT - VECS IDLE Max Count

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoEnhancementCS
Default Value:	0x00000040
Access:	R/W
Size (in bits):	32
Trusted Type:	1

Address: 1A054h

This register contains the time in 0.64us to wait before telling power management hardware the render pipe is IDLE

DWord	Bit	Description
0	31:20	**Reserved** Project: All Format: MBZ
	19:0	**MFX IDLE Wait Time** Project: All Format: Max Count Specifies how long the command stream should wait before ensuring the pipe is IDLE and to let power management hardware know

Value	Name	Description
00040h	**[Default]**	0x00040 * 0.64us ~ 41us wait time

Programming Notes
This is only useable if bit 0 of the PC_PSMI_CTRL is clear

VECS NOP Identification Register

VECS_NOPID - VECS NOP Identification Register	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoEnhancementCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	1A094h-1A097h

The VECS_NOPID register contains the Noop Identification value specified by the last MI_NOOP instruction that enabled this register to be updated.

DWord	Bit	Description
0	31:22	**Reserved**
	21:0	**Identification Number** This field contains the 22-bit Noop Identification value specified by the last MI_NOOP instruction that enabled this field to be updated.

VECS Hardware Status Mask Register

VECS_HWSTAM - VECS Hardware Status Mask Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoEnhancementCS
Default Value:	0xFFFFFFFF
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	1A098h

Access: RO for Reserved Control bits

The HWSTAM register has the same format as the Interrupt Control Registers. The bits in this register are "mask" bits that prevent the corresponding bits in the Interrupt Status Register from generating a "Hardware Status Write" (PCI write cycle). Any unmasked interrupt bit (HWSTAM bit set to 0) will allow the Interrupt Status Register to be written to the ISR location (within the memory page specified by the Hardware Status Page Address Register) when that Interrupt Status Register bit changes state.

Programming Notes

- To write the interrupt to the HWSP, the corresponding IMR bit must also be clear (enabled).
- At most 1 bit can be unmasked at any given time.

DWord	Bit	Description
0	31:0	**Hardware Status Mask Register** Default Value: FFFFFFFFh Project: All Format: Array of Masks refer to Table 4-4 in Interrupt Control Register section for bit definitions

VECS Mode Register for Software Interface

VECS_MI_MODE - VECS Mode Register for Software Interface

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoEnhancementCS
Default Value:	0x00000000 [NOVALIDPROJECTS] 0x00000200 [HSW]
Access:	R/W
Size (in bits):	32
Address:	1A09Ch-1A09Fh

The MI_MODE register contains information that controls software interface aspects of the command parser

DWord	Bit	Description
0	31:16	**Masks** A "1" in a bit in this field allows the modification of the corresponding bit in Bits 15:0
	15	**Suspend Flush** Project: All Mask: MMIO(0x209c)#31 Value / Name / Description / Project: 0h / No Delay / HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well / All 1h / Delay Flush / Suspend flush is active / All
	14:12	**Reserved** Format: MBZ
	11	**Invalidate UHPTR Enable** If bit set H/W clears the valid bit of BCS_UHPTR (4134h, bit 0) when current active head pointer is equal to UHPTR.
	10	**Reserved** Project: HSW Format: MBZ
	9	**Ring Idle (Read Only Status bit)** *Writes to this bit are not allowed.* Value / Name: 0 / Parser not idle

VECS_MI_MODE - VECS Mode Register for Software Interface

		1 — Parser idle **[Default]**
	8	**Stop Ring** 0 = Normal Operation. 1 = Parser is turned off. Software must set this bit to force the Ring and Command Parser to Idle. Software must read a "1" in Ring Idle bit after setting this bit to ensure that the hardware is idle. *Software must clear this bit for Ring to resume normal operation.*
	7:0	**Reserved** Format: MBZ

VECS Interrupt Mask Register

VECS_IMR - VECS Interrupt Mask Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoEnhancementCS
Default Value:	0xFFFFFFFF
Access:	R/W
Size (in bits):	32
Address:	1A0A8h

The IMR register is used by software to control which Interrupt Status Register bits are "masked" or "unmasked". "Unmasked" bits will be reported in the IIR, possibly triggering a CPU interrupt, and will persist in the IIR until cleared by software. "Masked" bits will not be reported in the IIR and therefore cannot generate CPU interrupts.

DWord	Bit	Description
0	31:0	**Interrupt Mask Bits** Project: All Format: Array of interrupt mask bits Refer to Table 4-4 in Interrupt Control Register section for bit definitions This field contains a bit mask which selects which interrupt bits (from the ISR) are reported in the IIR.

Value	Name	Description	Project
FFFF FFFFh	**[Default]**		
0h	Not Masked	Will be reported in the IIR	All
1h	Masked	Will not be reported in the IIR	All

VECS Error Identity Register

VECS_EIR - VECS Error Identity Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoEnhancementCS
Default Value:	0x00000000
Access:	R/WC
Size (in bits):	32
Address:	1A0B0h

The EIR register contains the persistent values of Hardware-Detected Error Condition bits. Any bit set in this register will cause the Master Error bit in the ISR to be set. The EIR register is also used by software to clear detected errors (by writing a '1' to the appropriate bit(s) except for the unrecoverable bits described).

DWord	Bit	Description
0	31:16	**Reserved** Project: All Format: MBZ
	15:0	**Error Identity Bits** Project: All Format: Array of Error condition bits See Table 1 5. Hardware-Detected Error Bits This register contains the persistent values of ESR error status bits that are unmasked via the EMR register. (See **Error! Reference source not found**.). The logical OR of all (defined) bits in this register is reported in the Master Error bit of the Interrupt Status Register. In order to clear an error condition, software must first clear the error by writing a '1' to the appropriate bit(s) in this field. If required, software should then proceed to clear the Master Error bit of the IIR.

Value	Name	Description	Project
0h	**[Default]**		
1h	Error occurred	Error occurred	All

Programming Notes

Writing a '1' to a set bit will cause that error condition to be cleared. However, the Page Table Error bit (Bit 4) can not be cleared except by reset (i.e., it is a fatal error).

VECS Error Mask Register

VECS_EMR - VECS Error Mask Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoEnhancementCS
Default Value:	0x00000000 [NOVALIDPROJECTS] 0x0000FFFF [HSW]
Access:	R/W
Size (in bits):	32
Address:	1A0B4h

The EMR register is used by software to control which Error Status Register bits are "masked" or "unmasked". "Unmasked" bits will be reported in the EIR, thus setting the Master Error ISR bit and possibly triggering a CPU interrupt, and will persist in the EIR until cleared by software. "Masked" bits will not be reported in the EIR and therefore cannot generate Master Error conditions or CPU interrupts.

Undefined or reserved bits in the Hardware Detected Error Bit Table will always return a read value of '1'

DWord	Bit	Description
0	31:16	**Reserved** Default Value: 0000h Project: HSW Format: MBZ
	15:0	**Error Mask Bits** Project: All Format: Array of error condition mask bits See Table 1 5. Hardware-Detected Error Bits This register contains a bit mask that selects which error condition bits (from the ESR) are reported in the EIR. Value / Name / Description: 0000h / Not Masked / Will be reported in the EIR FFFFh / Masked **[Default]** / Will not be reported in the EIR

VECS Error Status Register

VECS_ESR - VECS Error Status Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoEnhancementCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	1A0B8h

The ESR register contains the current values of all Hardware-Detected Error condition bits (these are all by definition "persistent"). The EMR register selects which of these error conditions are reported in the persistent EIR (i.e., set bits must be cleared by software) and thereby causing a Master Error interrupt condition to be reported in the ISR.

DWord	Bit	Description
0	31:16	**Reserved** Project: All Format: MBZ
	15:0	**Error Status Bits** Project: All Format: Array of error condition bits See Table 1 5. Hardware-Detected Error Bits This register contains the non-persistent values of all hardware-detected error condition bits.

Value	Name	Description	Project
0h	**[Default]**		
1h	Error Condition Detected	Error Condition detected	All

VECS Instruction Parser Mode Register

VECS_INSTPM - VECS Instruction Parser Mode Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoEnhancementCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	1A0C0h-1A0C3h

The VECS_INSTPM register is used to control the operation of the VECS Instruction Parser. Certain classes of instructions can be disabled (ignored) - often useful for detecting performance bottlenecks. Also, "Synchronizing Flush" operations can be initiated - useful for ensuring the completion (vs. only parsing) of rendering instructions.

Programming Notes

All reserved bits are implemented

DWord	Bit	Description
0	31:16	**Masks** Format: Mask[15:0] These bits serve as write enables for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.
	15:11	**Reserved** Project: All Format: MBZ
	10	**Reserved** Project: HSW Format: MBZ
	9	**TLB Invalidate** Project: HSW Format: U1 If set, this bit allows the command stream engine to invalidate the VEBOX TLBs. This bit is valid only with the Sync flush enable. **Programming Notes** GFX soft resets do not invalidate TLBs, it is upto

VECS_INSTPM - VECS Instruction Parser Mode Register

		GFX driver to explicitly invalidate TLBs post reset.
	8:7	**Reserved** Format: MBZ
	6	**Memory Sync Enable** Project: HSW This set, this bit allows the video decode engine to write out the data from the local caches to memory. This bit is not persistent. S/W must define this bit each time a sync flush is requested
	5	**Sync Flush Enable** Project: HSW Format: Enable (cleared by HW) This field is used to request a Sync Flush operation. The device will automatically clear this bit before completing the operation. See Sync Flush *(Programming Environment)*. Setting the Sync Flush Enable will cause a config write to MMIO register space with the address 0x4f100. **Programming Notes** The command parser must be stopped prior to issuing this command by setting the **Stop Ring** bit in register **VECS_MI_MODE**. Only after observing Ring Idle set in **VECS_MI_MODE** can a Sync Flush be issued by setting this bit. Once this bit becomes clear again, indicating flush complete, the command parser is re-enabled by clearing **Stop Ring**.
	4:0	**Reserved**

Batch Buffer State Register

BB_STATE - Batch Buffer State Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS
Default Value:	0x00000000 [HSW]
Access:	RO
Size (in bits):	32
Address:	12110h
Name:	VCS Batch Buffer State Register
ShortName:	VCS_BB_STATE
Address:	1A110h
Name:	VECS Batch Buffer State Register
ShortName:	VECS_BB_STATE
Address:	22110h
Name:	BCS Batch Buffer State Register
ShortName:	BCS_BB_STATE

This register contains the attributes of the current batch buffer initiated from the Ring Buffer.

This register should not be written by software. These fields should only get written by a context restore. Software should always set these fields via the MI_BATCH_BUFFER_START command when initiating a batch buffer.
This register is saved and restored with context.

DWord	Bit	Description
0	31:7	**Reserved** Project: All Format: MBZ
	6	**2nd Level Buffer Security Indicator** Project: HSW Source: BlitterCS, VideoEnhancementCS Exists If: //BCS, VECS Format: MI_2ndBufferSecurityType If set, VECS is fetching 2nd level batch commands from a PPGTT address space. If clear, GGTT. If execlists are enabled and this is set, the batch buffer is non-secure and cannot execute privileged commands nor access privileged (GGTT) memory. It will be accessed via the PPGTT. If clear, this batch buffer is secure and will be accessed via the GGTT.

BB_STATE - Batch Buffer State Register

Value	Name	Description
0h	MIBUFFER_SECURE **[Default]**	Located in GGTT memory
1h	MIBUFFER_NONSECURE	Located in PPGTT memory

Programming Notes
When execlists are enabled, this field reflects the effective security level and may not be the same as the Buffer Security Indicator written using MI_BATCH_BUFFER_START.

6 **2nd Level Buffer Security Indicator**

Project:	HSW
Source:	VideoCS, VideoCS2
Exists If:	//VCS, VCS2

If set, VCS is fetching 2nd level batch commands from a PPGTT address space. If clear, GGTT. If execlists are enabled and this is set, the batch buffer is non-secure and cannot execute privileged commands nor access privileged (GGTT) memory. It will be accessed via the PPGTT. If clear, this batch buffer is secure and will be accessed via the GGTT. Note: When execlists are enabled this field reflects the effective security level and may not be the same as the Buffer Security Indicator written using MI_BATCH_BUFFER_START.

Value	Name	Description
0h	MIBUFFER_SECURE **[Default]**	Located in GGTT memory
1h	MIBUFFER_NONSECURE	Located in PPGTT memory

5 **1st Level Buffer Security Indicator**

Project:	HSW
Format:	MI_1stBufferSecurityType

If set, BCS is fetching 1st level batch commands from a PPGTT address space. If clear, GGTT. If execlists are enabled and this is set, the batch buffer is non-secure and cannot execute privileged commands nor access privileged (GGTT) memory. It will be accessed via the PPGTT. If clear, this batch buffer is secure and will be accessed via the GGTT.

Note: When execlists are enabled this field reflects the effective security level and may not be the same as the Buffer Security Indicator written using MI_BATCH_BUFFER_START.

Value	Name	Description
0h	MIBUFFER_SECURE **[Default]**	Located in GGTT memory
1h	MIBUFFER_NONSECURE	Located in PPGTT memory

4 **Reserved**

4 **Reserved**

Project:	All
Source:	BlitterCS

BB_STATE - Batch Buffer State Register

		Exists If:	//BCS
		Format:	MBZ
	3:0	**Reserved**	
		Project:	All
		Format:	MBZ

Pending Head Pointer Register

UHPTR - Pending Head Pointer Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02134h
Name:	RCS Pending Head Pointer Register
ShortName:	RCS_UHPTR
Address:	12134h
Name:	VCS Pending Head Pointer Register
ShortName:	VCS_UHPTR
Address:	1A134h
Name:	VECS Pending Head Pointer Register
ShortName:	VECS_UHPTR
Valid Projects:	[DevHSW+]
Address:	22134h
Name:	BCS Pending Head Pointer Register
ShortName:	BCS_UHPTR

Programming Notes

Once SW uses UHPTR to preempt the existing workload, should explicitly program MI_SET_CONTEXT to save the preempted context status before submitting the new workload. In case SW doesn't want to save the state of the preempted context, it should at the minimum program RS_PREEMPT_STATUS to 0x0 so that the register status doesn't interfere with the new workloads.

DWord	Bit	Description
0	31:3	**Head Pointer Address** Format: GraphicsAddress[31:3] **Description** (Project): This register represents the GFX address offset where execution should continue in the ring buffer following execution of an MI_ARB_CHECK command. (HSW)
	2:1	**Reserved** Format: MBZ

UHPTR - Pending Head Pointer Register

	0	**Head Pointer Valid** **Description** / **Project** This bit is set by the software to request a pre-emption. / It is reset by hardware when an MI_ARB_CHECK command is parsed by the command streamer. The hardware uses the head pointer programmed in this register at the time the reset is generated. / HSW **Value** / **Name** / **Description** 0 / InValid / No valid updated head pointer register, resume execution at the current location in the ring buffer 1 / Valid / Indicates that there is an updated head pointer programmed in this register

Batch Buffer Head Pointer Register

BB_ADDR - Batch Buffer Head Pointer Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	02140h
Name:	RCS Batch Buffer Head Pointer Register
ShortName:	RCS_BB_ADDR
Address:	12140h
Name:	VCS Batch Buffer Head Pointer Register
ShortName:	VCS_BB_ADDR
Valid Projects:	HSW
Address:	1A140h
Name:	VECS Batch Buffer Head Pointer Register
ShortName:	VECS_BB_ADDR
Address:	22140h
Name:	BCS Batch Buffer Head Pointer Register
ShortName:	BCS_BB_ADDR

This register contains the current DWord Graphics Memory Address of the last-initiated batch buffer.

Programming Notes

Programming Restriction: This register should NEVER be programmed by driver. This is for HW internal use only.

DWord	Bit	Description
0	31:2	**Batch Buffer Head Pointer** Project: DevHSW+ Format: GraphicsAddress[31:2] This field specifies the DWord-aligned Graphics Memory Address where the last initiated Batch Buffer is currently fetching commands. If no batch buffer is currently active, the Valid bit will be 0 and this field will be meaningless.
	1	**Reserved** Format: MBZ

BB_ADDR - Batch Buffer Head Pointer Register

	0	**Valid** Format: U1 **Value** / **Name** / **Description** 0h / Invalid **[Default]** / Batch buffer Invalid 1h / Valid / Batch buffer Valid

VECS Threshold for the Counter of Video Enhancement Engine

VECS_CTR_THRSH - VECS Threshold for the Counter of Video Enhancement Engine		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	VideoEnhancementCS	
Default Value:	0x00150000	
Access:	R/W	
Size (in bits):	32	
Address:	1A17Ch	
DWord	**Bit**	**Description**
0	31:0	**Threshold Value** Default Value: 00150000h The value in this register reflects the number of clocks the bit stream decode engine is expected to run. If the value is exceeded the counter is reset and an interrupt may be enabled in the device.

VECS Context Sizes

VECS_CXT_SIZE - VECS Context Sizes

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoEnhancementCS
Default Value:	0x00040002
Access:	Read/32 bit Write Only
Size (in bits):	32
Address:	1A1A8h

This register contains the size in 64B units of the power context data separated by context buckets (section of the context image containing similar registers). It is undefined if the value is smaller than the default. If value is larger, VECS will save 0s.
This register is intended for debug purposes only and should not be modified under normal circumstances.

DWord	Bit	Description
0	31:21	**Reserved** Project: All Format: MBZ
	20:16	**VECS Context Size** Project: All Format: U5 Value: 4h — Name: **[Default]** — Project: HSW
	15:5	**Reserved** Project: All Format: MBZ
	4:0	**Execlist Context Size** Project: All Format: U5 Value: 2h — Name: **[Default]** — Project: HSW

VECS ECO Scratch Pad

VECS_ECOSKPD - VECS ECO Scratch Pad

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoEnhancementCS
Default Value:	0x00000000 [HSW]
Access:	R/W
Size (in bits):	32
Address:	1A1D0h

Chicken bits for post-silicon validation.

DWord	Bit	Description
0	31:16	**Reserved** Access: WO This register has bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. To set bit0, for example, the data would be 0x0001_0001. To clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16.
	15	**Reset Warning** This bit will be set by S/W during the following resets: • MFX only reset. • GFX reset during TDR. Value: 1 — Name: S/W indication for MFX reset in progress Value: 0 — Name: No render reset in progress
	14:11	**Reserved** Format: PBC
	10	**Reserved** Project: HSW
	9	**Reserved** Project: HSW Format: PBC

VECS_ECOSKPD - VECS ECO Scratch Pad			
	8:0	**Reserved**	
		Format:	PBC

VECS PPGTT Directory Cacheline Valid Register

VECS_PP_DCLV - VECS PPGTT Directory Cacheline Valid Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoEnhancementCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	1A220h

This register controls update of the on-chip PPGTT Directory Cache during a context restore. Bits that are set will trigger the load of the corresponding 16 directory entry group. This register is restored with context (prior to restoring the on-chip directory cache itself). This register is also restored when switching to a context whose LRCA matches the current CCID if the Force PD Restore bit is set in the context descriptor.
The context image of this register must be updated and maintained by SW; SW should not normally need to read this register.
This register can also effectively be used to limit the size of a processes' virtual address space. Any access by a process that requires a PD entry in a set that is not enabled in this register will cause a fatal error, and no fetch of the PD entry will be attempted

DWord	Bit	Description
0	63:32	**Reserved** Project: All Format: MBZ
	31:0	**PPGTT Directory Cache Restore [1..32] 16 entries** Project: All Format: Enable[32] If set, the [1st..32nd] 16 entries of the directory cache are considered valid and will be brought in on context restore. If clear, these entries are considered invalid and fetch of these entries will not be attempted.

VCES Idle Switch Delay

VECS_IDLEDLY - VCES Idle Switch Delay

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoEnhancementCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	1A23Ch

The IDLEDLY register contains an Idle Delay field which specifies the minimum number of microseconds allowed for command streamer to wait before a context is switched out leading to IDLE state in execlists mode, i.e following this context switch there is no active element available in HW to execute.
A default value of 0, means that by default, there is no restriction to wait on a context switch leading to IDLE. This register has no significance when execlists are not enabled.

DWord	Bit	Description
0	31:21	**Reserved** Project: All Format: MBZ
	20:0	**IDLE Delay** Default Value: 0h Project: All Format: U21 Minimum number of micro-seconds allowed.

Video Enhancement Mode Register

VEBOX_MODE - Video Enhancement Mode Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoEnhancementCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	1A29Ch

DWord	Bit	Description
0	31:16	**Mask Bits** Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:14	**Reserved** Project: HSW Format: MBZ
	13:10	**Reserved** Project: All Format: MBZ
	9	**Per-Process GTT Enable** Project: All Format: Enable Per-Process GTT BS Mode Enable

Value	Name	Description	Project
0h	PPGTT Disable **[Default]**	When clear, the Global GTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space in Basic Scheduler Mode.	All
1h	PPGTT Enable	When set, the PPGTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.	All

	8	**Reserved** Project: HSW

VEBOX_MODE - Video Enhancement Mode Register

	7	**Reserved** Project: HSW Format: MBZ
	6:5	**Reserved** Project: All Format: MBZ
	4:0	**Reserved** Project: HSW Format: MBZ

VECS Reported Timestamp Count

VECS_TIMESTAMP - VECS Reported Timestamp Count

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	VideoEnhancementCS
Default Value:	0x00000000, 0x00000000
Access:	RO. This register is not set by the context restore.
Size (in bits):	64
Address:	1A358h

This register provides an elapsed real-time value that can be used as a timestamp.
This register is *not* reset by a graphics reset. It will maintain its value unless a full chipset reset is performed.
Note: This timestamp register reflects the value of the PCU TSC. The PCU TSC counts 10ns increments; this timestamp reflects bits 38:3 of the TSC (i.e. 80ns granularity, rolling over every 1.5 hours).

DWord	Bit	Description
0	63:36	**Reserved** Project: All Format: MBZ
	35:0	**TimeStampValue** Project: All Format: U36 This register toggles every 80 ns. The upper 28 bits are zero.

BCS Execute Condition Code Register

BCS_EXCC - BCS Execute Condition Code Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS
Default Value:	0x00000000
Access:	R/W,RO
Size (in bits):	32
Trusted Type:	1
Address:	22028h

This register contains user defined and hardware generated conditions that are used by MI_WAIT_FOR_EVENT commands. An MI_WAIT_FOR_EVENT instruction excludes the executing ring from arbitration if the selected event evaluates to a 1, while instruction is discarded if the condition evaluates to a 0. Once excluded, a ring is enabled into arbitration when the selected condition evaluates to a 0. This register also contains control for the invalidation of indirect state pointers on context restore.

DWord	Bit	Description
0	31:16	**Mask Bits** Format: Mask[15:0] These bits serves as a write enable for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.
	15	**Reserved** Format: MBZ
	14:12	**Reserved** Project: HSW Format: MBZ
	11:5	**Reserved** Format: MBZ
	4:0	**User Defined Condition Codes** Project: HSW Format: U5 The software may signal a Stream Semaphore by setting the Mask bit and Signal Bit together to match the bit field specified in a WAIT_FOR_EVENT (Semaphore).

Blitter/Render Semaphore Sync Register

BRSYNC - Blitter/Render Semaphore Sync Register		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	BlitterCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	22040h	
This register is written by CS, read by BCS.		
DWord	**Bit**	**Description**
0	31:0	**Semaphore Data** Semaphore data for synchronization between blitter engine and render engine.

Blitter/Video Semaphore Sync Register

BVSYNC - Blitter/Video Semaphore Sync Register	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	22044h
This register is written by VCS, read by BCS.	

DWord	Bit	Description
0	31:0	**Semaphore Data** Semaphore data for synchronization between blitter engine and video codec engine.

Blitter/Video Enhancement Semaphore Sync Register

BVESYNC - Blitter/Video Enhancement Semaphore Sync Register		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	BlitterCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	22048h	
This register is written by VECS, read by BCS.		
DWord	**Bit**	**Description**
0	31:0	**Semaphore Data** Semaphore data for synchronization between blitter engine and video enhancement engine.

BCS Sleep State and PSMI Control

BCS_PSMI_CTRL - BCS Sleep State and PSMI Control

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1

Address: 22050h

This register is to be used to control all aspects of PSMI and power saving functions

DWord	Bit	Description
0	31:16	**Mask Bits** Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15	**Reserved** Project: HSW Format: MBZ
	14:13	**Reserved** Project: All Format: MBZ
	12	**Reserved** Project: HSW Format: MBZ
	11:8	**Reserved** Format: MBZ
	7	**Reserved** Project: HSW Format: MBZ
	6:5	**Reserved** Format: MBZ
	4	**GO Indicator** Project: All

BCS_PSMI_CTRL - BCS Sleep State and PSMI Control

	Access:	RO
	Format:	GO

This is a read only field. Writing to this bit is undefined. To simplify power saving and soft reset flows, the power management hardware has the ability to block all pending memory cycles of the render pipe. When GO=0, all cycles are blocked. All CPD enter/exit and RC6 enter/exit has this bit set to 0.

Value	Name	Description
0h	Disable **[Default]**	No cycles allowed coming out of IDLE. All pending memory read cycles are complete. No new cycles permitted except for power context or PSMI cycles.
1h	Enable	Normal execution

3 **IDLE Indicator**

Default Value:	0h Render is assumed NOT IDLE coming out of reset
Project:	All
Access:	RO
Format:	IDLE

This is a read only field. Writing to this bit is undefined. This indicates what power management thinks what state the render pipe is in. That is, if set, the full handshake between render and power management has occured and most likely the render clocks are currently turned off.

2 **Reserved**

Project:	All

1 **Reserved**

Project:	All
Format:	MBZ

0 **RC* IDLE Message Disable**

Project:	All
Format:	Disable FormatDesc

For GT to get in any power saving RC* states, the render pipe must let the power management hardware know when it is IDLE. If this bit is set, power management will always assume the blitter pipe is not IDLE.

Value	Name	Description	Project
0h	Enable **[Default]**	IDLE message is enabled	HSW
1h	Disable	IDLE message is disabled	HSW

BCS IDLE Max Count

BCS_PWRCTX_MAXCNT - BCS IDLE Max Count

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS
Default Value:	0x00000000 [NOVALIDPROJECTS] 0x00000040 [HSW]
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	22054h

This register contains the time in 0.64us to wait before telling power management hardware the render pipe is IDLE

DWord	Bit	Description
0	31:20	**Reserved** Project: All Format: MBZ
	19:0	**Blitter IDLE Wait Time** Project: All Format: Max Count Specifies how long the command stream should wait before ensuring the pipe is IDLE and to let power management hardware know

Value	Name	Description	Project
00040h	**[Default]**	0x00040 * 0.64us ~ 41us wait time	HSW

Programming Notes

- This is only useable if bit 0 of the PC_PSMI_CTRL is clear.
- The value in this field must be greater than 1.

BCS Hardware Status Mask Register

BCS_HWSTAM - BCS Hardware Status Mask Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS
Default Value:	0xFFFFFFFF
Access:	R/W
Size (in bits):	32
Trusted Type:	1

Address: 22098h

Access: RO for Reserved Control bits

The HWSTAM register has the same format as the Interrupt Control Registers. The bits in this register are "mask" bits that prevent the corresponding bits in the Interrupt Status Register from generating a "Hardware Status Write" (PCI write cycle). Any unmasked interrupt bit (HWSTAM bit set to 0) will allow the Interrupt Status Register to be written to the ISR location (within the memory page specified by the Hardware Status Page Address Register) when that Interrupt Status Register bit changes state.

Programming Notes

To write the interrupt to the HWSP, the corresponding IMR bit must also be clear (enabled). At most 1 bit can be unmasked at any given time.

DWord	Bit	Description
0	31:0	**Hardware Status Mask Register** Default Value: FFFFFFFFh Project: All Format: Array of Masks refer to Table 5-1 in Interrupt Control Register section for bit definitions

BCS Mode Register for Software Interface

BCS_MI_MODE - BCS Mode Register for Software Interface

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS
Default Value:	0x00000000 [NOVALIDPROJECTS]
	0x00000200 [HSW]
Access:	R/W
Size (in bits):	32
Address:	2209Ch-2209Fh

The MI_MODE register contains information that controls software interface aspects of the command parser.

DWord	Bit	Description
0	31:16	**Masks** A 1 in a bit in this field allows the modification of the corresponding bit in Bits 15:0
	15	**Suspend Flush** Project: All Mask: MMIO(0x209c)#31 Value / Name / Description: 0h / No Delay / HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well 1h / Delay Flush / Suspend flush is active
	14:12	**Reserved** Read/Write
	11	**Invalidate UHPTR enable** If bit set H/W clears the valid bit of BCS_UHPTR (4134h, bit 0) when current active head pointer is equal to UHPTR.
	10	**Reserved** Project: HSW Format: MBZ
	9	**Ring Idle (Read Only Status Bit)** *Writes to this bit are not allowed.* Value / Name: 0 / Parser not idle

BCS_MI_MODE - BCS Mode Register for Software Interface

	1	Parser idle **[Default]**

8 — Stop Ring

Software must set this bit to force the Ring and Command Parser to Idle. Software must read a 1 in Ring Idle bit after setting this bit to ensure that the hardware is idle.

Software must clear this bit for Ring to resume normal operation.

Value	Name
0	Normal Operation
1	Parser is turned off

7:2 — Reserved

Read/Write

1 — Bypass Fence Write

If set, this bit will bypass all writes during flushes, independent of programming. This includes post-sync op bits, the implicit TLB invalidate write (set in GFX_MODE[13]), and sync flush fences.

Note this is only intended for work-arounds

Value	Name
0	Normal Operation
1	Bypass

0 — Reserved

Read/Write

Mode Register for GAB

GAB_MODE - Mode Register for GAB

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	220A0h-220A3h

The GAB_MODE register
contains information that controls configurations in the GAB.

DWord	Bit	Description
0	31:16	**Reserved** Access: WO This register has bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. To set bit0, for example, the data would be 0x0001_0001. To clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16.
	15:6	**Reserved** Read/Write
	5:3	**BLB Arbitration Priority** Format: U3
	2:0	**BCS Arbitration Priority** Format: U3

BCS Interrupt Mask Register

BCS_IMR - BCS Interrupt Mask Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS
Default Value:	0xFFFFFFFF
Access:	R/W
Size (in bits):	32
Address:	220A8h

The IMR register is used by software to control which Interrupt Status Register bits are "masked" or "unmasked". "Unmasked" bits will be reported in the IIR, possibly triggering a CPU interrupt, and will persist in the IIR until cleared by software. "Masked" bits will not be reported in the IIR and therefore cannot generate CPU interrupts.

DWord	Bit	Description
0	31:0	**Interrupt Mask Bits** Project: All Format: Array of interrupt mask bits Refer to Table 5-1 in Interrupt Control Register section for bit definitions This field contains a bit mask which selects which interrupt bits (from the ISR) are reported in the IIR.

Value	Name	Description	Project
FFFF FFFFh	**[Default]**		
0h	Not Masked	Will be reported in the IIR	All
1h	Masked	Will not be reported in the IIR	All

BCS Error Identity Register

BCS_EIR - BCS Error Identity Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS
Default Value:	0x00000000
Access:	R/WC
Size (in bits):	32
Address:	220B0h

The EIR register contains the persistent values of Hardware-Detected Error Condition bits. Any bit set in this register will cause the Master Error bit in the ISR to be set. The EIR register is also used by software to clear detected errors (by writing a '1' to the appropriate bit(s) except for the unrecoverable bits described).).

DWord	Bit	Description
0	31:16	**Reserved** Project: All Format: MBZ
	15:0	**Error Identity Bits** Project: All Format: Array of Error condition bits See Table 1 5. Hardware-Detected Error Bits This register contains the persistent values of ESR error status bits that are unmasked via the EMR register. The logical OR of all (defined) bits in this register is reported in the Master Error bit of the Interrupt Status Register. To clear an error condition, software must first clear the error by writing a '1' to the appropriate bit(s) in this field. If required, software should then proceed to clear the Master Error bit of the IIR.

Value	Name	Description	Project
0h	**[Default]**		
1h	Error occurred	Error occurred	All

Programming Notes

Writing a '1' to a set bit will cause that error condition to be cleared. However, the Instruction Error bit (Bit 0) cannot be cleared except by reset (i.e., it is a fatal error).

BCS Error Mask Register

BCS_EMR - BCS Error Mask Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS
Default Value:	0x00000000 [NOVALIDPROJECTS] 0x0000FFFF [HSW]
Access:	R/W
Size (in bits):	32
Address:	220B4h

The EMR register is used by software to control which Error Status Register bits are "masked" or "unmasked". "Unmasked" bits will be reported in the EIR, thus setting the Master Error ISR bit and possibly triggering a CPU interrupt, and will persist in the EIR until cleared by software. "Masked" bits will not be reported in the EIR and therefore cannot generate Master Error conditions or CPU interrupts.

Undefined or reserved bits in the Hardware Detected Error Bit Table will always return a read value of '1'

DWord	Bit	Description
0	31:16	**Reserved** Default Value: 0000h Project: HSW Format: MBZ
	15:0	**Error Mask Bits** Project: All Format: Array of error condition mask bits See Table 1 5. Hardware-Detected Error Bits This register contains a bit mask that selects which error condition bits (from the ESR) are reported in the EIR. Value / Name / Description: 0000h / Not Masked / Will be reported in the EIR FFFFh / Masked **[Default]** / Will not be reported in the EIR

BCS Error Status Register

BCS_ESR - BCS Error Status Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	220B8h

The ESR register contains the current values of all Hardware-Detected Error condition bits (these are all by definition "persistent"). The EMR register selects which of these error conditions are reported in the persistent EIR (i.e., set bits must be cleared by software) and thereby causing a Master Error interrupt condition to be reported in the ISR.

DWord	Bit	Description
0	31:16	**Reserved** Project: All Format: MBZ
	15:0	**Error Status Bits** Project: All Format: Array of error condition bits See Table 1 5. Hardware-Detected Error Bits This register contains the non-persistent values of all hardware-detected error condition bits.

Value	Name	Description	Project
0h	**[Default]**		
1h	Error Condition Detected	Error Condition detected	All

BCS Instruction Parser Mode Register

BCS_INSTPM - BCS Instruction Parser Mode Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1

Address: 220C0h

Desc

DWord	Bit	Description
0	31:16	**Mask Bits** Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:11	**Reserved** Project: All Format: MBZ
	10	**Reserved** Project: HSW Format: MBZ
	9	**Reserved** Project: HSW Format: MBZ
	8:7	**Reserved** Project: All Format: MBZ
	6	**Memory Sync Enable** Project: HSW Format: U1 This set, this bit allows the blitter decode engine to write out the data from the local caches to memory.This bit is not persistent. S/W must define this bit each time a sync flush is requested
	5	**Sync Flush Enable**

BCS_INSTPM - BCS Instruction Parser Mode Register

		Project: HSW Format: U1 Format: Enable Cleared by HW This field is used to request a Sync Flush operation. The device will automatically clear this bit before completing the operation. See Sync Flush (Programming Environment).
	4:0	**Reserved** Project: All Format: MBZ

Batch Buffer State Register

BB_STATE - Batch Buffer State Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS
Default Value:	0x00000000 [HSW]
Access:	RO
Size (in bits):	32
Address:	12110h
Name:	VCS Batch Buffer State Register
ShortName:	VCS_BB_STATE
Address:	1A110h
Name:	VECS Batch Buffer State Register
ShortName:	VECS_BB_STATE
Address:	22110h
Name:	BCS Batch Buffer State Register
ShortName:	BCS_BB_STATE

This register contains the attributes of the current batch buffer initiated from the Ring Buffer.

This register should not be written by software. These fields should only get written by a context restore. Software should always set these fields via the MI_BATCH_BUFFER_START command when initiating a batch buffer.
This register is saved and restored with context.

DWord	Bit	Description
0	31:7	**Reserved** Project: All Format: MBZ
	6	**2nd Level Buffer Security Indicator** Project: HSW Source: BlitterCS, VideoEnhancementCS Exists If: //BCS, VECS Format: MI_2ndBufferSecurityType If set, VECS is fetching 2nd level batch commands from a PPGTT address space. If clear, GGTT. If execlists are enabled and this is set, the batch buffer is non-secure and cannot execute privileged commands nor access privileged (GGTT) memory. It will be accessed via the PPGTT. If clear, this batch buffer is secure and will be accessed via the GGTT.

BB_STATE - Batch Buffer State Register

Value	Name	Description
0h	MIBUFFER_SECURE **[Default]**	Located in GGTT memory
1h	MIBUFFER_NONSECURE	Located in PPGTT memory

Programming Notes
When execlists are enabled, this field reflects the effective security level and may not be the same as the Buffer Security Indicator written using MI_BATCH_BUFFER_START.

6 **2nd Level Buffer Security Indicator**

Project:	HSW
Source:	VideoCS, VideoCS2
Exists If:	//VCS, VCS2

If set, VCS is fetching 2nd level batch commands from a PPGTT address space. If clear, GGTT. If execlists are enabled and this is set, the batch buffer is non-secure and cannot execute privileged commands nor access privileged (GGTT) memory. It will be accessed via the PPGTT. If clear, this batch buffer is secure and will be accessed via the GGTT. Note: When execlists are enabled this field reflects the effective security level and may not be the same as the Buffer Security Indicator written using MI_BATCH_BUFFER_START.

Value	Name	Description
0h	MIBUFFER_SECURE **[Default]**	Located in GGTT memory
1h	MIBUFFER_NONSECURE	Located in PPGTT memory

5 **1st Level Buffer Security Indicator**

Project:	HSW
Format:	MI_1stBufferSecurityType

If set, BCS is fetching 1st level batch commands from a PPGTT address space. If clear, GGTT. If execlists are enabled and this is set, the batch buffer is non-secure and cannot execute privileged commands nor access privileged (GGTT) memory. It will be accessed via the PPGTT. If clear, this batch buffer is secure and will be accessed via the GGTT.

Note: When execlists are enabled this field reflects the effective security level and may not be the same as the Buffer Security Indicator written using MI_BATCH_BUFFER_START.

Value	Name	Description
0h	MIBUFFER_SECURE **[Default]**	Located in GGTT memory
1h	MIBUFFER_NONSECURE	Located in PPGTT memory

4 **Reserved**

4 **Reserved**

Project:	All
Source:	BlitterCS

BB_STATE - Batch Buffer State Register

		Exists If:	//BCS
		Format:	MBZ
	3:0	**Reserved**	
		Project:	All
		Format:	MBZ

Pending Head Pointer Register

UHPTR - Pending Head Pointer Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02134h
Name:	RCS Pending Head Pointer Register
ShortName:	RCS_UHPTR
Address:	12134h
Name:	VCS Pending Head Pointer Register
ShortName:	VCS_UHPTR
Address:	1A134h
Name:	VECS Pending Head Pointer Register
ShortName:	VECS_UHPTR
Valid Projects:	[DevHSW+]
Address:	22134h
Name:	BCS Pending Head Pointer Register
ShortName:	BCS_UHPTR

Programming Notes

Once SW uses UHPTR to preempt the existing workload, should explicitly program MI_SET_CONTEXT to save the preempted context status before submitting the new workload. In case SW doesn't want to save the state of the preempted context, it should at the minimum program RS_PREEMPT_STATUS to 0x0 so that the register status doesn't interfere with the new workloads.

DWord	Bit	Description
0	31:3	**Head Pointer Address** Format: GraphicsAddress[31:3] Description: This register represents the GFX address offset where execution should continue in the ring buffer following execution of an MI_ARB_CHECK command. Project: HSW
	2:1	**Reserved** Format: MBZ

UHPTR - Pending Head Pointer Register

	0	**Head Pointer Valid** **Description** / **Project** This bit is set by the software to request a pre-emption. / It is reset by hardware when an MI_ARB_CHECK command is parsed by the command streamer. The hardware uses the head pointer programmed in this register at the time the reset is generated. / HSW **Value** / **Name** / **Description** 0 / InValid / No valid updated head pointer register, resume execution at the current location in the ring buffer 1 / Valid / Indicates that there is an updated head pointer programmed in this register

Batch Buffer Head Pointer Register

BB_ADDR - Batch Buffer Head Pointer Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	02140h
Name:	RCS Batch Buffer Head Pointer Register
ShortName:	RCS_BB_ADDR
Address:	12140h
Name:	VCS Batch Buffer Head Pointer Register
ShortName:	VCS_BB_ADDR
Valid Projects:	HSW
Address:	1A140h
Name:	VECS Batch Buffer Head Pointer Register
ShortName:	VECS_BB_ADDR
Address:	22140h
Name:	BCS Batch Buffer Head Pointer Register
ShortName:	BCS_BB_ADDR

This register contains the current DWord Graphics Memory Address of the last-initiated batch buffer.

Programming Notes

Programming Restriction: This register should NEVER be programmed by driver. This is for HW internal use only.

DWord	Bit	Description
0	31:2	**Batch Buffer Head Pointer** Project: DevHSW+ Format: GraphicsAddress[31:2] This field specifies the DWord-aligned Graphics Memory Address where the last initiated Batch Buffer is currently fetching commands. If no batch buffer is currently active, the Valid bit will be 0 and this field will be meaningless.
	1	**Reserved** Format: MBZ

BB_ADDR - Batch Buffer Head Pointer Register

	0	**Valid** Format: U1 **Value** / **Name** / **Description** 0h / Invalid **[Default]** / Batch buffer Invalid 1h / Valid / Batch buffer Valid

BCS Watchdog Counter Threshold

BCS_CTR_THRSH - BCS Watchdog Counter Threshold

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS
Default Value:	0x00150000
Access:	R/W
Size (in bits):	32
Address:	2217Ch

DWord	Bit	Description
0	31:0	**Counter logic Threshold** Default Value: 00150000h Format: U32 This field specifies the threshold that the hardware checks against for the value of the blitter clock counter before generating an interrupt. The counter in hardware generates an interrupt when the threshold is reached, rolls over and starts counting again. The interrupt generated is the "Media Hang Notify" interrupt since this watchdog timer is intended primarily to remedy VLD hangs on the main pipeline.

Ring Buffer Current Context ID Register

BCS_RCCID - Ring Buffer Current Context ID Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	22190h-22197h

This register contains the current ring context ID associated with the ring buffer.

Programming Notes

The current context registers must not be written directly (via MMIO). The RCCID register should only be updated indirectly from RNCID.

DWord	Bit	Description
0	63:0	**Unnamed** See Context Descriptor for BCS.

BCS Ring Buffer Next Context ID Register

BCS_RNCID - BCS Ring Buffer Next Context ID Register	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	22198h-2219Fh

This register contains the *next* ring context ID associated with the ring buffer.

Programming Notes

The current context (RCCID) register can be updated indirectly from this register on a context switch event. Note that the only time a context switch can occur is when MI_ARB_CHECK enables preemption or the current context runs dry (head pointer becomes equal to tail pointer).

DWord	Bit	Description
0	63:0	**Unnamed** See Context Descriptor for BCS

BCS SW Control

BCS_SWCTRL - BCS SW Control

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1

Address: 22200h

DWord	Bit	Description
0	31:16	**Reserved** Access: WO This register has bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. To set bit0, for example, the data would be 0x0001_0001. To clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16.
	15:4	**Reserved** Project: HSW Format: MBZ
	3:2	**Reserved** Project: HSW Format: MBZ
	1	**Tile Y Destination** Project: HSW Format: U1 Programming this bit makes the HW treat all destination surfaces as Tile Y. This bit over-rides the setting of the destination format in the packet provided to the blitter command streamer. SW is required to flush the HW before changing the polarity of this bit. This bit is part of the context save/restore.
	0	**Tile Y Source**

BCS_SWCTRL - BCS SW Control

		Project: HSW Format: U1 Programming this bit makes the HW treat all source surfaces as Tile Y. This bit over-rides the setting of the source format in the packet provided to the blitter command streamer. SW is required to flush the HW before changing the polarity of this bit. This bit is part of the context save/restore.

BCS PPGTT Directory Cacheline Valid Register

BCS_PP_DCLV - BCS PPGTT Directory Cacheline Valid Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	22220h

Default Value = 0h
This register controls update of the on-chip PPGTT Directory Cache during a context restore. Bits that are set will trigger the load of the corresponding 16 directory entry group. This register is restored with context (prior to restoring the on-chip directory cache itself). This register is also restored when switching to a context whose LRCA matches the current CCID if the Force PD Restore bit is set in the context descriptor.
The context image of this register must be updated and maintained by SW; SW should not normally need to read this register.
This register can also effectively be used to limit the size of a processes' virtual address space. Any access by a process that requires a PD entry in a set that is not enabled in this register will cause a fatal error, and no fetch of the PD entry will be attempted.

DWord	Bit	Description
0	63:32	**Reserved** Format: MBZ
	31:0	**PPGTT Directory Cache Restore** Format: Enable[32] [1..32] 16 entries If set, the [1st..32nd] 16 entries of the directory cache are considered valid and will be brought in on context restore. If clear, these entries are considered invalid and fetch of these entries will not be attempted.

Blitter Mode Register

BLT_MODE - Blitter Mode Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	2229Ch

DWord	Bit	Description
0	31:16	**Mask Bits** Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:14	**Reserved** Project: HSW Format: MBZ
	13:10	**Reserved** Project: All Format: MBZ
	9	**Per-Process GTT Enable** Project: All Format: Enable Per-Process GTT BS Mode Enable Value / Name / Description / Project: 0h / PPGTT Disable **[Default]** / When clear, the Global GTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space. / All 1h / PPGTT Enable / When set, the PPGTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space. / All
	8	**Reserved** Project: All

BLT_MODE - Blitter Mode Register

	7:4	**Reserved** Project: HSW Format: MBZ
	3:1	**Reserved** Project: All Format: MBZ
	0	**Reserved** Project: HSW Format: MBZ

BCS Reported Timestamp Count

BCS_TIMESTAMP - BCS Reported Timestamp Count

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS
Default Value:	0x00000000, 0x00000000
Access:	RO. This register is not set by the context restore.
Size (in bits):	64
Address:	22358h

This register provides an elapsed real-time value that can be used as a timestamp.This register is not reset by a graphics reset. It will maintain its value unless a full chipset reset is performed.
Note: This timestamp register reflects the value of the PCU TSC. The PCU TSC counts 10ns increments; this timestamp reflects bits 38:3 of the TSC (i.e. 80ns granularity, rolling over every 1.5 hours).

DWord	Bit	Description
0	63:36	**Reserved** Project: All Format: MBZ
	35:0	**Timestamp Value** Project: All Format: U36 This register toggles every 80 ns. The upper 28 bits are zero.

GAB unit Control Register

GAB_CTL_REG - GAB unit Control Register

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS
Default Value:	0x000000BF
Access:	R/W
Size (in bits):	32
Address:	24000h

DefaultValue=FF0000BFh Trusted Type = 1

DWord	Bit	Description
0	31:9	**Reserved**
	8	**Continue after Page Fault** Value / Name / Description 1 / GAB Set / Ipon receiving a page fault when requesting an address translation, GAB will set address bit 39 to 1 and continue. 0 / GAB Hang / GAB will hang on a page fault. Default = b0.
	7:6	**PPGTT BCS TLB LRA MIN** Default Value: 10b TLB Depth Partitioning Register In PP GTT Mode.
	5:4	**GAB write request priority signal value used in GAC arbitration** Default Value: 11b
	3:2	**GAB read only request priority signal value used in GAC arbitration** Default Value: 11b
	1:0	**GAB read request priority signal value used in GAC arbitration** Default Value: 11b

GAB Error Reporting Register

GAB_ERR_REPORT - GAB Error Reporting Register		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	BlitterCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	24094h	
This register is directly mapped for the Error Reporting Register.		
DWord	**Bit**	**Description**
0	31:8	**Reserved**
	7	**HWSP GGTT fetch yields an invalid entry**
	6	**VTD fetch yields an invalid entry**
	5	**PD VTD HPA fetch yields an invalid entry**
	4	**PD fetch yields an invalid entry**
	3	**PD fetch for entry marked as invalid by BCS**
	2	**GTT fetch yields an invalid entry** Page Fault occurred in one of the GTT translations.
	1	**CTXTLB VTD fetch yields an invalid entry**
	0	**CTXTLB fetch yields an invalid entry**

BCS Section 0 of TLBPEND entry

BCS_TLBPEND_SEC0 - BCS Section 0 of TLBPEND entry		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	BlitterCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	24400h-24403h	
This register is directly mapped to the TLBPEND Array in the Graphic Arbiter.		
DWord	**Bit**	**Description**
0	31:28	**GTT bits** Bits 3:0 of the GTT entry used to translate the Virtual Address. 000 if translation is pending.
	27:0	**Current Address** The value of this field depends on the stage of the TLB translation for this entry: VA - bits 27:20 = 00, bits 19:0 = Bits 31:12 of the Virtual Address of the cycle.

BCS Section 1 of TLBPEND entry

BCS_TLBPEND_SEC1 - BCS Section 1 of TLBPEND entry

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	24500h-24503h

This register is directly mapped to the current Virtual Addresses in the MTTLB (Texture and constant cache TLB).

DWord	Bit	Description
0	31	**vtstatus** This bit will be used in conjunction with the ready bit to determine the stage of the translation. See table in section 0 register.
	30:28	**Reserved**
	27:24	**PAT entry** Location of Physical Address in Physical Address Table.
	23:22	**Reserved**
	21:20	**Surface format** Value / Name: 0xb Linear; 10b Tile X; 11b Tile Y
	19:14	**Cache line offset in page**
	13:10	**Cacheability Control Bits**
	9	**ZLR bit** indicates a zero length read
	8:2	**TAG**
	1:0	**SRC ID** 00/01=BCS; 10/11= BLB

BCS Valid Bit Vector for TLBPEND registers

BCS_TLBPEND_VLD0 - BCS Valid Bit Vector for TLBPEND registers

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	24700h-24703h

This register contains the valid bits for entries 0-31 of TLBPEND structure(Cycles pending TLB translation).

DWord	Bit	Description
0	31:0	**Valid bits per entry**

BCS Ready Bit Vector for TLBPEND Registers

BCS_TLBPEND_RDY0 - BCS Ready Bit Vector for TLBPEND Registers		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	BlitterCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	24708h-2470Bh	
This register contains the ready bits for entries 0-31 of TLBPEND structure (Cycles pending TLB translation).		
DWord	**Bit**	**Description**
0	31:0	**Ready bits per entry**

Valid Bit Vector for BCS TLB

BCSTLB_VLD - Valid Bit Vector for BCS TLB	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	24780h-24783h
This register contains the valid bits for entries 0-31 of BCS TLB.	

DWord	Bit	Description
0	31:4	**Reserved**
	3:0	**Valid bits per entry**

Valid Bit Vector for BLB TLB

BLBTLB_VLD - Valid Bit Vector for BLB TLB	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	24784h-24787h

This register contains the valid bits for entries 0-31 of BLB TLB.

DWord	Bit	Description
0	31:8	**Reserved**
	7:0	**Valid bits per entry**

Valid Bit Vector for CTX TLB

CTX_TLB_VLD - Valid Bit Vector for CTX TLB	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	24788h-2478Bh

This register contains the valid bits for entries 0-31 of CTX TLB.

DWord	Bit	Description
0	31:1	**Reserved**
	0	**Valid bits per entry**

Valid Bit Vector for PD TLB

PDTLB_VLD - Valid Bit Vector for PD TLB	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	2478Ch-2478Fh

This register contains the valid bits for entries 0-31 of PD TLB.

DWord	Bit	Description
0	31:8	**Reserved**
	7:0	**Valid bits per entry**

BCS TLB Virtual Page Address Registers

BCSTLB_VA - BCS TLB Virtual Page Address Registers

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	24800h-24803h

This register is directly mapped to the current Virtual Addresses in the BCS TLB.

DWord	Bit	Description
0	31:12	**ADDRESS** Project: HSW Format: GraphicsAddress[31:12] PAGE VIRTUAL ADDRESS.
	11:0	**RESERVED** Project: HSW Format: MBZ

BLBTLB_VA Virtual page Address Registers

BLBTLB_VA - BLBTLB_VA Virtual page Address Registers

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	24900h-24903h

This register is directly mapped to the current Virtual Addresses in the BLB TLB.

DWord	Bit	Description
0	31:12	**ADDRESS** Project: HSW Format: GraphicsAddress[31:12] PAGE VIRTUAL ADDRESS
	11:0	**RESERVED** Format: MBZ

CTXTLB_VA Virtual page Address Registers

CTXTLB_VA - CTXTLB_VA Virtual page Address Registers

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	24A00h-24A03h

This register is directly mapped to the current Virtual Addresses in the CTX TLB.

DWord	Bit	Description
0	31:12	**ADDRESS** Project: HSW Format: GraphicsAddress[31:12] PAGE VIRTUAL ADDRESS
	11:0	**RESERVED** Project: HSW Format: MBZ

PDTLB_VA Virtual page Address Registers

PDTLB_VA - PDTLB_VA Virtual page Address Registers

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BlitterCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	24B00h-24B03h

This register is directly mapped to the current Virtual Addresses in the PD TLB.

DWord	Bit	Description
0	31:12	**ADDRESS** Project: HSW Format: GraphicsAddress[31:12] PAGE VIRTUAL ADDRESS
	11:0	**RESERVED** Project: HSW Format: MBZ

VGA_CONTROL

VGA_CONTROL	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x80000000
Access:	R/W
Size (in bits):	32
Address:	41000h-41003h
Name:	VGA Control
ShortName:	VGA_CONTROL
Power:	off/on
Reset:	soft

Restriction
Restriction : VGA requires panel fitting to be enabled. VGA is always connected to pipe A. VGA can not be enabled while the display power well is powered down. VGA display should only be enabled if all display planes other than VGA are disabled.

DWord	Bit	Description
0	31	**VGA Display Disable** This bit will disable the VGA compatible display mode. It has no effect on VGA register or A0000-BFFFF memory aperture accesses which are controlled by the PCI configuration and VGA I/O register settings.

Value	Name
0b	Enable
1b	Disable **[Default]**

Note:	Project
Note: Program register 42090h bits 31:29 = 101b and bit 26 = 0b before enabling VGA display and keep them at those values while VGA display is enabled. It is safe to have those values even when VGA display is disabled.	DevHSW:GT0:X0
Note: Program register 42090h bits 31:29 = 101b and bit 26 = 1b before enabling VGA display and keep them at those values while VGA display is enabled. It is safe to have those values even when VGA display is disabled.	DevHSW:GT3:A
Note: Program register 42090h bits 31:29 = 100b, bit 26 =	DevHSW,

		0b, and bit 12 = 0b before enabling VGA display and keep them at those values while VGA display is enabled. It is safe to have those values even when VGA display is disabled. | EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A)
		Restriction: Restriction : The VGA SR01 screen off bit must be programmed when enabling and disabling VGA. See the VGA Registers document.
	30:27	**Reserved** Format: PBC
	26	**VGA Border Enable** This bit determines if the VGA border areas are included in the active display area. The border will be scaled along with the pixel data. 0b: Disable 1b: Enable
	25	**Reserved** Format: PBC
	24	**Pipe CSC Enable** This bit enables pipe color space conversion for the VGA pixel data. 0b: Disable 1b: Enable
	23:21	**Reserved** Format: PBC
	20	**Legacy 8Bit Palette En** This bit affects reads and writes to the palette through VGA I/O addresses. In the 6-bit mode, the 8-bits of data are shifted up two bits on the write (upper two bits are lost) and shifted two bits down on the read. This provides backward compatibility for original VGA programs as well as VESA VBE support for 8-bit palette. It does not affect palette accesses through the palette register MMIO path. 0b: 6 bit DAC 1b: 8 bit DAC
	19	**Reserved**
	18	**Reserved**
	17:16	**Reserved**

VGA_CONTROL

		Format: PBC
	15:12	**Reserved**
	11:8	**Reserved**
	7:6	**Blink Duty Cycle** Controls the VGA text mode blink duty cycle relative to the VGA cursor blink duty cycle.

Value	Name	Description
00b	100%	100% Duty Cycle, Full Cursor Rate
01b	25%	25% Duty Cycle, 1/2 Cursor Rate
10b	50%	50% Duty Cycle, 1/2 Cursor Rate
11b	75%	75% Duty Cycle, 1/2 Cursor Rate

	5:0	**VSYNC Blink Rate** Controls the VGA blink rate in terms of the number of VSYNCs per on/off cycle.

Programming Notes
Program with (VSYNCs/cycle)/2-1

FUSE_STRAP

FUSE_STRAP

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	42014h-42017h
Name:	Fuses and Straps
ShortName:	FUSE_STRAP
Power:	Always on
Reset:	global

This register provides readback of fuse and strap settings.
These fuses are programmed by a message from PCU to display address 0x51000 MSG_FUSE, also known as Display Fuse State Message (DFSM).

DWord	Bit	Description
0	31	**Internal Graphics Disable** This bit indicates whether internal graphics capability is disabled. When disabled, iMPH hardware will prevent internal graphics from enabling. 0b – Enable – Internal Graphics Enabled 1b – Disable – Internal Graphics Disabled
	30	**Internal Display Disable** This bit indicates whether the internal display capability is disabled. This bit does not affect display hardware directly. 0b – Enable – Internal Display Enabled 1b – Disable – Internal Display Disabled
	29	**Reserved**
	28	**Display PipeC Disable** This bit indicates whether the display pipe C capability is disabled. When disabled, display hardware will prevent the pipe C enable register bit from being set to 1b. 0b – Enable – Pipe C Capability Enabled 1b – Disable – Pipe C Capability Disabled

FUSE_STRAP

27	**Display PM Disable** This bit indicates whether the display power management FBC and DPST capability is disabled. When disabled, display hardware will prevent the FBC enable and DPST image enhancement enable register bits from being set to 1b.

Value	Name	Description
0b	Enable	PM Capability Enabled
1b	Disable	PM Capability Disabled

26	**Display eDP Disable** This bit indicates whether the display embedded DisplayPort eDP DDIA capability is disabled. When disabled, display hardware will prevent the eDP DDIA enable register bit from being set to 1b and mask the eDP DDIA present strap.

Value	Name	Description
0b	Enable	eDP Capability Enabled
1b	Disable	eDP Capability Disabled

25	**Reserved**
24	**Display CDCLK Limit** This bit indicates whether the display CD clock frequency is limited to the default frequency of if the alternate frequency is allowed. When DISPLAY_CDCLK_LIMIT = 1, display hardware will ignore the LCPLL_CTL CD Frequency Select and only allow 450 MHz. From spare fuse bit 2.

Value	Name	Description
0b	No Limit	CDCLK frequency not limited to 450 MHz, alternate frequency can be used
1b	Limit	CDCLK frequency limited to 450 MHz, alternate frequency cannot be used

23:22	**Display Spare** Spare fuses for display. From spare fuses bits 1:0.
21	**CPU Internal SSC Enabled** This bit indicates if the CPU internal SSC modulator is enabled. Fuse name SSC_ssc_misc_config_EnableIntSscMod.

Value	Name	Description
0b	Not enabled	CPU internal SSC is disabled
1b	Enabled	CPU internal SSC is enabled

20:18	**SRAM VMIN SHARED P** SRAM Shared P setting. Signal name dpr_rf_vccmin[2:0]. From FUSE_DISPLAY_RF_VMIN[25:23].
17	**SRAM VMIN KP** SRAM Keeper setting. Signal name dpr_rf_kp. From FUSE_DISPLAY_RF_VMIN[22].
16:6	**Display Cap Bits 16 6** Display capability bits which can be optionally used to inform software of the hardware

		capabilities. These bits do not control any hardware behavior.
	5:2	**Reserved** Format: MBZ
	1	**Reserved**
	0	**Display Audio Codec Disable** This bit indicates whether the display audio codec capability is disabled. When disabled, display hardware will prevent the audio codec enable register bit from being set to 1b.

Value	Name	Description
0b	Enable	Audio Codec Capability Enabled
1b	Disable	Audio Codec Capability Disabled

FUSE_STRAP2

FUSE_STRAP2	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	4201Ch-4201Fh
Name:	Fuses and Straps 2
ShortName:	FUSE_STRAP2
Power:	Always on
Reset:	global

This register provides readback of fuse and strap settings.
These fuses are programmed by a message from PCU to display address 0x51008 MSG_FUSE2, also known as Display Fuse State Message 2 (DFSM2).

DWord	Bit	Description
0	31:22	**Display Cap2 Bits 31 22** Display capability bits which can be optionally used to inform software of the hardware capabilities. These bits do not control any hardware behavior.
	21:19	**PF SRAM VCCPWMOD** PF SRAM VCCPWMOD setting. From FUSE_SAPFVCCPWMOD, FUSE_CR90 0x4168[6:4].
	18:16	**PF SRAM WLBIAS** PF SRAM WLBIAS setting. From FUSE_SAPFWLBIAS, FUSE_CR90 0x4168[9:7].
	15	**PF SRAM VCCBIASENB** PF SRAM VCCBIASENB setting. From FUSE_SAPFVCCBIASENB.
	14:11	**PF SRAM VCCBIAS** PF SRAM VCCBIAS setting. From FUSE_SAPFSRAMVCCBIAS, FUSE_CR90 0x4168[3:0].
	10	**Display Cap2 Bits 10** Display capability bits which can be optionally used to inform software of the hardware capabilities. These bits do not control any hardware behavior.
	9:0	**PF SRAM COL RED** PF SRAM column redundancy setting. From FUSE_SAPF_COL_RED.

FUSE_STRAP3

FUSE_STRAP3

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000 [HSW]
Access:	RO
Size (in bits):	32

Address:	42020h-42023h
Name:	Fuses and Straps 3
ShortName:	FUSE_STRAP3
Power:	Always on
Reset:	global

This register provides readback of fuse and strap settings.
These fuses are programmed by a message from PCU to display address 0x51004 MSG_STRAP, also known as Display Strap State Message (DSSM).

DWord	Bit	Description
0	31:5	**Reserved**
	4	**Reserved** Project: DevHSW:GT0:X0, DevHSW:GT3:A
	4	**ULT Mode** Project: DevHSW, EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A) This bit indicates whether the display operates in ULT mode or non-ULT mode. Value / Name / Description: 0b / Non-ULT / Display operates in non-ULT mode 1b / ULT / Display operates in ULT mode
	3	**Reserved**
	2	**LCPLL Unavail** This bit specifies the availability of the LCPLL. Value / Name / Description: 0b / Available / LCPLL available 1b / Not available / LCPLL not available
	1	**Reference Clock Select** This bit specifies the frequency of the display reference clocks. Value / Name / Description / Project:

FUSE_STRAP3

		0b	135MHz	SSC reference is 135 MHz. Non-SSC reference is 135 MHz. PCH is Lynxpoint or later.	
		1b	120MHz	SSC reference is 120 MHz. Non-SSC reference is 120 MHz. PCH is Pantherpoint or earlier.	DevHSW:GT0:X0, DevHSW:GT3:A
		1b	24MHz	SSC reference is 135 MHz. Non-SSC reference is 24 MHz.	DevHSW, EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A)
	0	**DisplayPort A Present** This bit specifies whether the port was present during initalization. The strap state can also be read in the DDI_BUF_CTL_A 0x64000 register bit 0.			

Value	Name	Description
0b	Not Present	Port not present
1b	Present	Port present

FUSE_STRAP4

FUSE_STRAP4	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	42024h-42027h
Name:	Fuses and Straps 4
ShortName:	FUSE_STRAP4
Valid Projects:	[DevHSW, EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A)]
Power:	Always on
Reset:	global

This register provides readback of fuse and strap settings.
These fuses are programmed by a message from PCU to display address 0x5100C MSG_FUSE3, also known as Display Fuse State Message 3 (DFSM3).

DWord	Bit	Description
0	31:22	**Display Cap4 Bits 31 22** Display capability bits which can be optionally used to inform software of the hardware capabilities. These bits do not control any hardware behavior.
	21:19	**IPS SRAM VCCPWMOD** IPS SRAM VCCPWMOD setting.
	18:16	**IPS SRAM WLBIAS** IPS SRAM WLBIAS setting.
	15	**IPS SRAM VCCBIASENB** IPS SRAM VCCBIASENB setting.
	14:11	**IPS SRAM VCCBIAS** IPS SRAM VCCBIAS setting.
	10	**Display Cap4 Bits 10** Display capability bits which can be optionally used to inform software of the hardware capabilities. These bits do not control any hardware behavior.
	9:0	**IPS SRAM COL RED** IPS SRAM column redundancy setting.

DE_POWER1

DE_POWER1

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000 [HSW]
Access:	RO
Size (in bits):	32
Address:	42400h-42403h
Name:	Display Engine Power 1
ShortName:	DE_POWER1
Power:	Always on
Reset:	global

DWord	Bit	Description
0	31	**Power Well State** This field indicates the status of the display power well. Value: 0b = Off; 1b = On
	30	**Display Pipes Enabled** Project: DevHSW, EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A) This field indicates if any display pipes are enabled. Value: 0b = Disabled (All display pipes disabled); 1b = Enabled (One or more display pipes enabled)
	29	**Display Power Down Allowed** Project: DevHSW, EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A) This field indicates the current setting of the display power down allow register bit in LCPLL_CTL. When allowed, the PCU can save the display context and power down display power wells. Value: 0b = Not allowed (Display power down not allowed); 1b = Allowed (Display power down allowed)
	30:28	**Reserved** Project: DevHSW:GT0:X0, DevHSW:GT3:A Format: MBZ

DE_POWER1

28 — IPS Status

Project:	DevHSW, EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A)

This field indicates the status of IPS.

Value	Name	Description
0b	Disabled	IPS disabled
1b	Enabled	IPS enabled

27:26 — SRD Status

This field indicates the live status of the SRD link on eDP DDI-A.

Value	Name	Description
00b	Full Off	Link is fully off. DDI-A lanes are disabled and most memory reads are disabled.
01b	Full On	Link is fully on. Normal operation.
10b	Standby	Link is in standby. Most memory reads are disabled.
11b	Reserved	Reserved

25 — Reserved

Project:	DevHSW:GT0:X0, DevHSW:GT3:A
Format:	MBZ

25 — KVM Session Status

Project:	DevHSW, EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A)

This field indicates the status of KVM session.

Value	Name	Description
0b	Disabled	KVM session disabled
1b	Enabled	KVM session enabled

24:13 — Reserved

Format:	MBZ

12:10 — Enabled Panel Fitters

The total number of panel fitters enabled.
Each 3x3 panelfitter will add 1 to the total. Each 7x5 panelfitter will add 2 to the total.

9:8 — Reserved

Format:	MBZ

7:4 — Transmit Lanes Enabled

The total number of DDI lanes enabled.

3 — Reserved

Format:	MBZ

2:0 — Enabled DPLLs

The total number of Display PLLs enabled.

DE_POWER2

DE_POWER2	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	42404h-42407h
Name:	Display Engine Power 2
ShortName:	DE_POWER2
Power:	Always on
Reset:	global

DWord	Bit	Description
0	31:0	**DE bandwidth counter** This counter increments on every cache line put arriving at the DE. The bandwidth is estimated by taking the difference between two reads at a known interval. The counter is only reset at boot time or by writing a new value.

FBC_CFB_BASE

FBC_CFB_BASE	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	43200h-43203h
Name:	FBC Compressed Buffer Address
ShortName:	FBC_CFB_BASE
Power:	Always on
Reset:	soft

Restriction
Restriction : The contents of this register must not be changed while compression is enabled.

DWord	Bit	Description
0	31:28	**Reserved** Format: MBZ
	27:12	**CFB Offset Address** This register specifies offset of the Compressed Frame Buffer from the base of stolen memory. **Restriction** Restriction : The buffer must be 4K byte aligned.
	11:0	**Reserved** Format: MBZ

FBC_CTL

FBC_CTL

Register Space:	MMIO: 0/2/0
Project:	DevHSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	43208h-4320Bh
Name:	FBC Control
ShortName:	FBC_CTL
Power:	Always on
Reset:	soft

FBC is tied to primary plane A.

Restriction

Restriction : The contents of this register must not be changed, except the enable bit, while compression is enabled.

Frame Buffer Compression is only supported with 16bpp and 32bpp 8:8:8 primary plane source pixel formats. It is not supported with any other format. The 16bpp format requires the compression ratio to be set to 2:1 or 4:1.

Frame Buffer Compression is only supported with surfaces of less than 4096 pixels x 4096 lines. Only the first 2048 lines will be compressed.

DWord	Bit	Description
0	31	**Enable FBC** This bit is used to globally enable FBC function at the next Vertical Blank start.

Value	Name
0b	Disable
1b	Enable

Workaround	Project
Workaround (WaFbcAsynchFlipDisableFbcQueue) : Display register 420B0h bit 22 must be set to 1b for the entire time that Frame Buffer Compression is enabled.	
Workaround (WaFbcDisableDpfcClockGating) : Display register 46500h bit 23 must be set to 1b for the entire time that Frame Buffer	DevHSW:GT0:X0, DevHSW:GT3:A

	Compression is enabled.	
	Workaround : Prior to HSW B stepping, FBC is not supported with 180 degree rotation on the primary display plane. Disable FBC when using 180 degree rotation.	DevHSW:GT0:X0, DevHSW:GT3:A
	Workaround : Frame buffer compression can only be enabled after the primary plane has been enabled for one or more vertical blanks and must be disabled before disabling the primary plane.	DevHSW:GT0:X0, DevHSW:GT3:A, DevHSW:GT3:B

30:29 Reserved

Format:	MBZ

28 CPU Fence Enable

Value	Name	Description
0b	No CPU Disp Buf	Display Buffer is not in a CPU fence. No modifications are allowed from CPU to the Display Buffer.
1b	CPU Disp Buf	Display Buffer exists in a CPU fence.

27:25 Reserved

Format:	MBZ

24:16 Reserved

15 Reserved

14:11 Reserved

Format:	MBZ

10 Reserved

9:8 Reserved

7:6 Compression Limit

Description	Project
This register sets a minimum limit on compression. This determines the maximum size of the compressed frame buffer. Display lines that do not meet the compression limit will not be compressed, so the best compression will be achieved with a 1:1 ratio. Compression Ratio 1, Pixel Format 16 bpp - Not Supported Compression Ratio 1, Pixel Format 32 bpp - Supported (CFB=FB) Compression Ratio 1/2, Pixel Format 16 bpp - Supported (CFB=FB) Compression Ratio 1/2, Pixel Format 32 bpp - Supported (CFB=1/2 FB) Compression Ratio 1/4, Pixel Format 16 bpp - Supported (CFB=1/2 FB) Compression Ratio 1/4, Pixel Format 32 bpp - Supported (CFB=1/4 FB)	

FBC_CTL

FB = Frame Buffer Size CFB = Compressed Frame Buffer Size		
The compressed frame buffer does not need to be allocated beyond 2048 lines.		DevHSW, EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A)

Value	Name	Description
00b	1:1	Compressed buffer is the same size as the uncompressed buffer.
01b	2:1	Compressed buffer is one half the size of the uncompressed buffer.
10b	4:1	Compressed buffer is one quarter the size of the uncompressed buffer.
11b	Reserved	Reserved

5:4 **Write Back Watermark**

The compressed data write back engine waits for this number of entries to be ready before writing the data out to memory.

Value	Name	Description
00b	4	4 entries
01b	8	8 entries
10b	16	16 entries
11b	32	32 entries

3:0 **CPU Fence Number**

Value	Name
0000b	Fence 0

Restriction
Restriction : This field must be programmed to 0000b.

IPS_CTL

IPS_CTL	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank OR pipe disabled
Address:	43408h-4340Bh
Name:	IPS Control
ShortName:	IPS_CTL
Valid Projects:	[DevHSW, EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A)]
Power:	Always on
Reset:	soft

IPS is tied to the pipe A output before the panel fitter.

Restriction
Restriction : IPS is only supported with 8:8:8 pipe pixel formats. It is not supported with any other format. IPS is supported only on ULT devices.

DWord	Bit	Description
0	31	**Enable IPS** This bit is used to enable the IPS function. **Value** / **Name**: 0b – Disable; 1b – Enable **Note:** For stepping prior to HSW E0 IPS enable should happen outside of the vblank region. — Project: DevHSW, EXCLUDE(DevHSW:GT3:B), EXCLUDE(DevHSW:GT3:C), EXCLUDE(DevHSW:GT3:D) **Note:** Do not read or write the pipe palette/gamma data while GAMMA_MODE is configured for split gamma and IPS_CTL has IPS enabled.

IPS_CTL

		Restriction Restriction : IPS is supported only on ULT devices.
	30:27	**Spare 30 27** Spare bits
	26:24	**Spare 26 24** Spare bits
	23:12	**Spare 23 12** Spare bits
	11:7	**IPS Programmable Watermark Value** This field sets the IPS programmable watermark value in lines from empty.
	6	**IPS Programmable Watermark Enable** This field enables the programmable IPS watermark to be used in low power states. **Value** / **Name** 0b – Disable 1b – Enable
	5	**Reserved**
	4	**Reserved**
	3	**Reserved**
	2	**Reserved**
	1	**Reserved**
	0	**Reserved**

IPS_STATUS

IPS_STATUS	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/WC
Size (in bits):	32
Address:	43410h-43413h
Name:	IPS Status
ShortName:	IPS_STATUS
Valid Projects:	[DevHSW, EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A)]
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31	**Full Frame** Access: R/WC This bit is set if the full frame fit into the compressed buffer. Write 1b to to clear the bit.
	30	**Pixel Count Mismatch** Access: R/WC This bit is set if the wrong number of pixels is decompressed for a line. Write 1b to to clear the bit.
	29:12	**Reserved** Format: MBZ
	11:0	**Last Comp Amount** Access: RO This field indicates the compression amount of the last frame.

Display Engine Interrupt Bit Definition

Display Engine Interrupt Bit Definition		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	44000h-4400Fh	
Name:	Display Engine Interrupts	
ShortName:	DE_INTERRUPT	
Power:	Always on	
Reset:	soft	
The Display Engine Interrupt Control Registers all share the same bit definitions from this table. The DE_IIR and GT_IIR and PM_IIR are ORed together to generate the Display interrupt.		
DWord	**Bit**	**Description**
0	31	**Master Interrupt Control** This bit exists only in the DEIER Display Engine Interrupt Enable Register. This is the master control for Display interrupts. This bit must be set to 1b for any interrupts to propagate to the system.
	30	**Error Interrupts Combined** The ISR is an active high level while any of the Error Interrupt bits are set.
	29	**GSE** The ISR is an active high pulse on the GSE system level event.
	28	**PCH Display interrupt event** The ISR is an active high level while there is an interrupt being generated by the PCH Display. It will stay asserted until the interrupts in the PCH Display are all cleared.
	27	**DisplayPort A Hotplug** The ISR gives the live state of the Digital Port A HPD pin when the HPD input is enabled. The IIR is set if a short or long pulse is detected when HPD input is enabled.
	26	**AUX Channel A** The ISR is an active high pulse on the AUX DDI A done event. This event will not occur for SRD AUX done.
	25	**DPST histogram event** The ISR is an active high pulse on the DPST histogram event.
	24	**DPST phase in event** The ISR is an active high pulse on the DPST phase in event.

Display Engine Interrupt Bit Definition		
	23:21	**Unused Int 23 21** These interrupts are currently unused.
	20	**Audio Codec Interrupts Combined** The ISR is an active high level while any of the Audio Codec Interrupt bits are set.
	19	**SRD Interrupts Combined** The ISR is an active high level while any of the SRD_IIR bits are set.
	18:16	**Unused Int 18 16** These interrupts are currently unused.
	15	**GTC CPU Interrupts Combined** The ISR is an active high level while any of the GTC_CPU_IIR bits are set.
	14	**Sprite Plane Flip Done C** The ISR is an active high pulse when a sprite plane flip is done. A flip is an update of the plane surface address value through MMIO or a command streamer.
	13	**Primary Plane Flip Done C** The ISR is an active high pulse when a primary plane flip is done. A flip is an update of the plane surface address value through MMIO or a command streamer.
	12	**Line Compare Pipe C** The ISR is an active high pulse on the scan line event of the timing generator attached to the Pipe C planes.
	11	**Vsync Pipe C** The ISR is an active high level for the duration of the vertical sync of the timing generator attached to the Pipe C planes.
	10	**Vblank Pipe C** The ISR is an active high level for the duration of the vertical blank of the timing generator attached to the Pipe C planes. **Note:** **Note:** Do not enable and unmask this interrupt if the associated pipe is disabled. Do not leave this interrupt enabled and unmasked after the associated pipe is disabled.
	9	**Sprite Plane Flip Done B** The ISR is an active high pulse when a sprite plane flip is done. A flip is an update of the plane surface address value through MMIO or a command streamer.
	8	**Primary Plane Flip Done B** The ISR is an active high pulse when a primary plane flip is done. A flip is an update of the plane surface address value through MMIO or a command streamer.
	7	**Line Compare Pipe B** The ISR is an active high pulse on the scan line event of the timing generator attached to the Pipe B planes.
	6	**Vsync Pipe B** The ISR is an active high level for the duration of the vertical sync of the timing generator attached to the Pipe B planes.
	5	**Vblank Pipe B**

Display Engine Interrupt Bit Definition		
		The ISR is an active high level for the duration of the vertical blank of the timing generator attached to the Pipe B planes. **Note:** **Note:** Do not enable and unmask this interrupt if the associated pipe is disabled. Do not leave this interrupt enabled and unmasked after the associated pipe is disabled.
	4	**Sprite Plane Flip Done A** The ISR is an active high pulse when a sprite plane flip is done. A flip is an update of the plane surface address value through MMIO or a command streamer.
	3	**Primary Plane Flip Done A** The ISR is an active high pulse when a primary plane flip is done. A flip is an update of the plane surface address value through MMIO or a command streamer.
	2	**Line Compare Pipe A** The ISR is an active high pulse on the scan line event of the timing generator attached to the Pipe A planes.
	1	**Vsync Pipe A** The ISR is an active high level for the duration of the vertical sync of the timing generator attached to the Pipe A planes.
	0	**Vblank Pipe A** The ISR is an active high level for the duration of the vertical blank of the timing generator attached to the Pipe A planes. **Note:** **Note:** Do not enable and unmask this interrupt if the associated pipe is disabled. Do not leave this interrupt enabled and unmasked after the associated pipe is disabled.

GT Interrupts

GT_INTERRUPT - GT Interrupts		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	44010h-4401Fh	
Power:	Always on	
Reset:	soft	
DWord	**Bit**	**Description**
0	31:0	**GT_Interrupt** Format: GT Interrupt Bit Definition

Power Management Interrupts

PM_INTERRUPT - Power Management Interrupts		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	44020h-4402Fh	
Power:	Always on	
Reset:	soft	
DWord	**Bit**	**Description**
0	31:0	**Interrupts** Format: **Power Management Interrupt Bit Definition**

HOTPLUG_CTL

HOTPLUG_CTL

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	44030h-44033h
Name:	Hot Plug Control
ShortName:	HOTPLUG_CTL
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31:5	**Reserved**
	4	**DDI A HPD Input Enable** Description: This field controls the state of the hot plug detect buffer for port A. The buffer state is independent of whether the port is enabled or not. Project: (blank) Description: The DDI A HPD input must be enabled in both North Display Engine Registers HOTPLUG_CTL and South Display Engine Registers SHOTPLUG_CTL. Project: DevHSW:ULT Value 0b, Name Disable, Description: Buffer disabled. Value 1b, Name Enable, Description: Buffer enabled. Hot plugs can be detected.
	3:2	**Reserved**
	1:0	**DDI A HPD Status** Access: R/WC This field reflects the hot plug detect status on port A. This bit is used for either monitor hotplug/unplug or for notification of a sink event. When HPD input is enabled and either a long or short pulse is detected, one of these bits will set and the hotplug IIR will be set (if unmasked in the IMR). The hotplug ISR gives the live state of the HPD pin. These are sticky bits, cleared by writing 1s to both of them. The short pulse duration is programmed in HPD_PULSE_CNT.

HOTPLUG_CTL

Value	Name	Description
00b	Not Detected	Digital port hot plug event not detected
1Xb	Long Pulse	Digital port long pulse hot plug event detected
X1b	Short Pulse	Digital port short pulse hot plug event detected

Programming Notes
Due to the possibility of back to back HPD events it is recommended that software filters the value read from the ISR.

HPD_PULSE_CNT

HPD_PULSE_CNT	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x000007CE
Access:	R/W
Size (in bits):	32
Address:	44034h-44037h
Name:	HPD Pulse count
ShortName:	HPD_PULSE_CNT
Power:	Always on
Reset:	global

This register is on the chip reset, not the FLR or display debug reset.

Restriction
Restriction : This register must be programmed properly before enabling DDI HPD detection.

DWord	Bit	Description
0	31:17	**Reserved** Format: MBZ
	16:0	**DP ShortPulse Count** Default Value: 007CEh 2000 microseconds These bits define the duration of the pulse defined as a short pulse for DisplayPort HPD. The value is in number of microseconds minus 2.

HPD_FILTER_CNT

HPD_FILTER_CNT	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x000001F2
Access:	R/W
Size (in bits):	32
Address:	44038h-4403Bh
Name:	HPD Filter count
ShortName:	HPD_FILTER_CNT
Power:	Always on
Reset:	global

This register is on the chip reset, not the FLR or display debug reset.

Restriction
Restriction : This register must be programmed properly before enabling DDI HPD detection.

DWord	Bit	Description
0	31:17	**Reserved** Format: MBZ
	16:0	**HPD Filter Count** Default Value: 001F2h 500 microseconds These bits define the duration of the filter for DDI HPD. The value is in number of microseconds minus 2.

ERR_INT

ERR_INT

Register Space:	MMIO: 0/2/0
Project:	DevHSW
Source:	PRM
Default Value:	0x00000000
Access:	R/WC
Size (in bits):	32
Address:	44040h-44043h
Name:	Error Interrupts
ShortName:	ERR_INT
Power:	Always on
Reset:	soft

These are sticky bits, cleared by writing 1b to them.
All the Error Interrupt bits are ORed together to go to the Display Engine ISR Error Interrupts Combined bit.

DWord	Bit	Description
0	31	**Poison Status** This bit is set upon receiving the poison message.

Value	Name	Description
0b	Not Detected	Event not detected
1b	Detected	Event detected

	30	**Reserved**

Format:	MBZ

	29	**Invalid GTT page table entry** This bit is set upon receiving the iMPH interrupt message with bit 1 set.

Value	Name	Description
0b	Not Detected	Event not detected
1b	Detected	Event detected

	28	**Invalid page table entry data** This bit is set upon receiving the iMPH interrupt message with bit 0 set.

Value	Name	Description
0b	Not Detected	Event not detected
1b	Detected	Event detected

	27:24	**Reserved**

Format:	MBZ

ERR_INT

23 Sprite GTT Fault Status C

This bit is set when a GTT fault is detected for this sprite plane.

Value	Name	Description
0b	Not Detected	Event not detected
1b	Detected	Event detected

22 Primary GTT Fault Status C

This bit is set when a GTT fault is detected for this primary plane.

Value	Name	Description
0b	Not Detected	Event not detected
1b	Detected	Event detected

21 Cursor GTT Fault Status C

This bit is set when a GTT fault is detected for this cursor plane.

Value	Name	Description
0b	Not Detected	Event not detected
1b	Detected	Event detected

20 Sprite GTT Fault Status B

This bit is set when a GTT fault is detected for this sprite plane.

Value	Name	Description
0b	Not Detected	Event not detected
1b	Detected	Event detected

19 Primary GTT Fault Status B

This bit is set when a GTT fault is detected for this primary plane.

Value	Name	Description
0b	Not Detected	Event not detected
1b	Detected	Event detected

18 Cursor GTT Fault Status B

This bit is set when a GTT fault is detected for this cursor plane.

Value	Name	Description
0b	Not Detected	Event not detected
1b	Detected	Event detected

17 Sprite GTT Fault Status A

This bit is set when a GTT fault is detected for this sprite plane.

Value	Name	Description
0b	Not Detected	Event not detected
1b	Detected	Event detected

16 Primary GTT Fault Status A

This bit is set when a GTT fault is detected for this primary plane.

ERR_INT

Value	Name	Description
0b	Not Detected	Event not detected
1b	Detected	Event detected

15 **Cursor GTT Fault Status A**
This bit is set when a GTT fault is detected for this cursor plane.

Value	Name	Description
0b	Not Detected	Event not detected
1b	Detected	Event detected

14 **Reserved**

Format:	MBZ

13 **MMIO Cycle Not Claimed**
This bit is set when a MMIO read or write cycle is not claimed. This can occur on an attempted access to an undefined address or to an address in a powered down power well.

Value	Name	Description
0b	Not Detected	Event not detected
1b	Detected	Event detected

12:9 **Reserved**

Format:	MBZ

8 **Reserved**

7 **Reserved**

6 **Pipe FIFO Underrun C**
This bit is set when the pipe FIFO underrun signal is high on the timing generator attached to the Pipe C planes.

Value	Name	Description
0b	Not Detected	Event not detected
1b	Detected	Event detected

5 **Reserved**

4 **Reserved**

3 **Pipe FIFO Underrun B**
This bit is set when the pipe FIFO underrun signal is high on the timing generator attached to the Pipe B planes.

Value	Name	Description
0b	Not Detected	Event not detected
1b	Detected	Event detected

2 **Reserved**

1 **Reserved**

0 **Pipe FIFO Underrun A**

ERR_INT		
		This bit is set when the pipe FIFO underrun signal is high on the timing generator attached to the Pipe A planes.

Value	Name	Description
0b	Not Detected	Event not detected
1b	Detected	Event detected

DE_RRMR

DE_RRMR	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	44050h-44053h
Name:	Render Response Mask
ShortName:	DE_RRMR
Power:	Always on
Reset:	soft

See the render response message definition table to find the source event for each bit.

The render response message is sent from the display engine to the render command streamer (CS) or blitter command streamer (BCS). The message is used to inform CS and BCS of certain display events.

This register is used to control which render response message bits are masked or unmasked.
Unmasked bits will cause a render response message to be sent and will be reported in that message.
Masked bits will not be reported and will not cause a render response message to be sent.

Vertical blank events occur periodically while the associated display pipe timing generator is running and will be reported in a render response to CS or BCS (depending on DE_RR_DEST destination selection) if un-masked here.

Scanline events occur after they have been initiated through MMIO writes or LRI to the Display Load Scan Lines register.
A flip event will be reported in a render response to CS if un-masked here and the Display Load Scanline source is CS.
A flip event will be reported in a render response to BCS if un-masked here and the Display Load Scanline source is BCS.

Flip done events occur after they have been initiated through MI_DISPLAY_FLIP or MMIO write to the primary or sprite plane surface address registers.
A flip event will be reported in a render response to CS if un-masked here and the flip source is CS.
A flip event will be reported in a render response to BCS if un-masked here and the flip source is BCS.

Programming Notes
Programming this register can be done through MMIO or a command streamer LOAD_REGISTER_IMMEDIATE (LRI) command.

DE_RRMR

When using LRI care must be taken to follow all the programming rules for LRI targetting the display engine. Unmasked events will wake GT as they occur, so for improved power savings it is recommended to only unmask events that are required.

Restriction
Restriction : Events must be unmasked prior to waiting for them with a MI_WAIT_FOR_EVENT ring command, or in the case of flips or scanlines, prior to starting the flip or loading the scanline.

DWord	Bit	Description
0	31	**Reserved** Format: MBZ
	30:0	**DE RRMR** Format: **Display Engine Render Response Message Bit Definition** This field contains a bit mask which selects which events cause and are reported in the render response message.

Value	Name	Description
0b	Not Masked	Not Masked - will cause a message to be sent and will be reported in that message
1b	Masked	Masked - will not cause a message to be sent or be reported in a message
0070EF2Fh	All Masked **[Default]**	

TIMESTAMP_CTR

TIMESTAMP_CTR	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/WC
Size (in bits):	32
Address:	44070h-44073h
Name:	Time Stamp Counter
ShortName:	TIMESTAMP_CTR
Power:	Always on
Reset:	global

The register is not reset by a FLR or display debug reset.

DWord	Bit	Description
0	31:0	**TIMESTAMP Counter** This field increments every microsecond. The value in this field is latched in the Pipe Flip TIMESTAMP registers when flips occur, and in the Pipe Frame TIMESTAMP registers at start of vertical blank. The register value will reset if any value is written to it. The register is not reset by a FLR or display debug reset.

Restriction	Project
Restriction : The CDCLK_FREQ register must be programmed with the correct value in order for the time stamp to run at the correct rate.	DevHSW:GT3:A

Audio Codec Interrupt Bit Definition

Audio Codec Interrupt Bit Definition	
Register Space:	MMIO: 0/2/0
Project:	DevHSW
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	44080h-4408Fh
Name:	Audio Interrupts
ShortName:	AUD_INTERRUPT
Power:	Always on
Reset:	soft

The Audio Codec Interrupt Control Registers all share the same bit definitions from this table.
All Audio Codec ISR bits are ORed together to go to Display Engine ISR Audio_Codec_Interrupts_Combined.

DWord	Bit	Description
0	31	**Audio Power State change DDI D** The ISR is an active high pulse when there is a power state change for audio for DDI D.
	30	**Audio Power State change DDI C** The ISR is an active high pulse when there is a power state change for audio for DDI C.
	29	**Audio Power State change DDI B** The ISR is an active high pulse when there is a power state change for audio for DDI B.
	28:11	**Unused Int 28 11** These interrupts are currently unused.
	10	**Audio CP Request Pipe C** The ISR is an active high level indicating content protection is requested by audio azalia verb programming for pipe C. It is valid after the Audio_CP_Change_Pipe_C event has occurred.
	9	**Audio CP Change Pipe C** The ISR is an active high pulse when there is a change in the protection request from audio azalia verb programming for pipe C.
	8:7	**Unused Int 8 7** These interrupts are currently unused.
	6	**Audio CP Request Pipe B** The ISR is an active high level indicating content protection is requested by audio azalia verb programming for pipe B. It is valid after the Audio_CP_Change_Pipe_B event has occurred.
	5	**Audio CP Change Pipe B** The ISR is an active high pulse when there is a change in the protection request from audio azalia verb programming for pipe B.

Audio Codec Interrupt Bit Definition		
	4:3	**Unused Int 4 3** These interrupts are currently unused.
	2	**Audio CP Request Pipe A** The ISR is an active high level indicating content protection is requested by audio azalia verb programming for pipe A. It is valid after the Audio_CP_Change_Pipe_A event has occurred.
	1	**Audio CP Change Pipe A** The ISR is an active high pulse when there is a change in the protection request from audio azalia verb programming for pipe A.
	0	**Unused Int 0** These interrupts are currently unused.

ARB_CTL

ARB_CTL

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x16661056
Access:	R/W
Size (in bits):	32
Address:	45000h-45003h
Name:	Display Arbitration Control 1
ShortName:	ARB_CTL
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31	**Reserved**
	30	**Reserved**
	29	**Reserved**
	28:26	**HP Queue Watermark** Default Value: 101b 6 The value in this register indicates the number of entries the high priority queue should have before it can be read. The value is zero based.
	25:24	**LP Write Request Limit** The value in this register indicates the maximum number of back to back LP write requests that will be accepted from a single client before re-arbitrating. Value / Name: 00b: 1 01b: 2 10b: 4 **[Default]** 11b: 8
	23:20	**TLB Request Limit** The value in this register indicates the maximum number of TLB requests that can be made in an arbitration loop. Zero is not a valid programming. Value / Name: 0110b: 6 **[Default]** [1,15]

ARB_CTL

19:16	**TLB Request InFlight Limit** The value in this register indicates the maximum number of TLB (or VTd) requests that can be in flight at any given time. Zero is not a valid programming. **Value** / **Name** 0110b: 6 **[Default]** [1,15]
15	**FBC Watermark Disable** Setting this bit disables the FBC watermarks. **Value** / **Name** 0b: Enable 1b: Disable
14:13	**Tiled Address Swizzling** DRAM configuration registers show if memory address swizzling is needed. **Value** / **Name** / **Description** 00b / No Display / No display request address swizzling 01b / Enable / Enable display request address bit[6] swizzling for tiled surfaces 10b / Reserved / 11b / Reserved /
12:8	**HP Page Break Limit** The value in this register represents the maximum number of page breaks allowed in a HP request chain. Zero is not a valid programming. **Value** / **Name** 10000b: 16 **[Default]** [1,31]
7	**Reserved**
6:0	**HP Data Request Limit** The value in this register represents the maximum number of cachelines allowed in a HP request chain. **Value** / **Name** 1010110b: 86 **[Default]** [1,127] **Restriction** Restriction : This value must always be programmed greater than 8.

ARB_CTL2

ARB_CTL2

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000600
Access:	R/W
Size (in bits):	32
Address:	45004h-45007h
Name:	Display Arbitration Control 2
ShortName:	ARB_CTL2
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31	**Reserved**
	30:12	**Reserved** Format: MBZ
	11	**Reserved**
	10:9	**Inflight LP Read Request Limit** The value in this register represents the maximum number of LP read request transactions that can be inflight at any given time. Value / Name / Description: 00b / 1 LP / 1 LP inflight transactions limit 01b / 2 LP / 2 LP inflight transactions limit 10b / 3 LP / 3 LP inflight transactions limit 11b / 4 LP **[Default]** / 4 LP inflight transactions limit
	8	**Reserved** Format: MBZ
	7	**Reserved**
	6	**Reserved** Format: MBZ
	5:4	**Inflight HP Read Request Limit** The value in this register represents the maximum number of HP read request transactions that can be inflight at any given time. Value / Name / Description

ARB_CTL2

		00b	128 HP	128 HP inflight transactions limit
		01b	64 HP	64 HP inflight transactions limit
		10b	32 HP	32 HP inflight transactions limit
		11b	16 HP	16 HP inflight transactions limit
	3:2	**Reserved**		
		Format:		MBZ
	1:0	**RTID FIFO Watermark** The value in this register represents the watermark value for the RTID FIFO. HP transactions will start only when the FIFO level is above or equal the watermark		

Value	Name	Description
00b	8 RTIDs	8 RTIDs available in FIFO
01b	16 RTIDs	16 RTIDs available in FIFO
10b	32 RTIDs	32 RTIDs available in FIFO
11b	Reserved	Reserved

WM_PIPE

WM_PIPE		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00783818	
Access:	R/W	
Size (in bits):	32	
Address:	45100h-45103h	
Name:	Pipe A Watermarks	
ShortName:	WM_PIPE_A	
Power:	Always on	
Reset:	soft	
Address:	45104h-45107h	
Name:	Pipe B Watermarks	
ShortName:	WM_PIPE_B	
Power:	Always on	
Reset:	soft	
Address:	45200h-45203h	
Name:	Pipe C Watermarks	
ShortName:	WM_PIPE_C	
Power:	Always on	
Reset:	soft	
These are the watermark values which are used for requesting data. There is one instance of this register format per each pipe A/B/C.		
DWord	**Bit**	**Description**
0	31:23	**Reserved**
	22:16	**Pipe Primary Watermark** Default Value: 1111000b Number in 64Bs of data in FIFO below which the Pipe Primary Plane stream will generate requests to memory
	15	**Reserved**
	14:8	**Pipe Sprite Watermark** Default Value: 0111000b

WM_PIPE		
		Number in 64Bs of data in FIFO below which the Pipe Sprite Plane stream will generate requests to memory
	7:6	**Reserved**
	5:0	**Pipe Cursor Watermark** Default Value: 011000b Number in 64Bs of data in FIFO below which the Pipe Cursor Plane stream will generate requests to memory

WM_LP

WM_LP	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	45108h-4510Bh
Name:	Low Power 1 Watermarks
ShortName:	WM_LP1
Power:	Always on
Reset:	soft
Address:	4510Ch-4510Fh
Name:	Low Power 2 Watermarks
ShortName:	WM_LP2
Power:	Always on
Reset:	soft
Address:	45110h-45113h
Name:	Low Power 3 Watermarks
ShortName:	WM_LP3
Power:	Always on
Reset:	soft

These are Low Power watermark values which will be used when display is in a LP state.
There is one instance of this register format per each LP level 1,2,3.

DWord	Bit	Description
0	31	**Enabled** Enables this LP watermark. This bit allows the associated LP state to be used. **Value** / **Name**: 1b – Enable; 0b – Disable **Restriction**: Restriction : The watermark line time registers for all enabled pipes must be programmed with the correct values prior to enabling.

<table>
<tr><th colspan="3">WM_LP</th></tr>
<tr><td></td><td>30:24</td><td>Latency
<table>
<tr><th>Description</th><th>Project</th></tr>
<tr><td>If the power negotiation is using actual latency values, this field contains the microsecond latency value associated with this LP watermark. Example: 0000101b = 5 microseconds.

Else, this field contains the integer value of the name of the latency level associated with this LP watermark. Example: 0000011b = level 3</td><td>DevHSW:GT0:X0, DevHSW:GT3:A</td></tr>
<tr><td>If the power negotiation is using actual latency values, this field contains two times the microsecond latency value associated with this LP watermark. Example: 0000101b = 2.5 microseconds.

Else, this field contains two times the integer value of the name of the latency level associated with this LP watermark. Example: 0000100b = level 2.</td><td>DevHSW, EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A)</td></tr>
</table></td></tr>
<tr><td></td><td>23:20</td><td>FBC LP Watermark
Number of equivalent lines of the primary display for this watermark</td></tr>
<tr><td></td><td>19:18</td><td>Reserved</td></tr>
<tr><td></td><td>17:8</td><td>LP Primary Watermark
Number in 64Bs of data in the display data buffer below which the Primary Plane stream will wake memory.</td></tr>
<tr><td></td><td>7:0</td><td>LP Cursor Watermark
Number in 64Bs of data in the display data buffer below which the Cursor Plane stream will wake memory.</td></tr>
</table>

WM_LP_SPR

WM_LP_SPR	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	45120h-45123h
Name:	Low Power 1 Sprite Watermarks
ShortName:	WM_LP1_SPR
Power:	Always on
Reset:	soft
Address:	45124h-45127h
Name:	Low Power 2 Sprite Watermarks
ShortName:	WM_LP2_SPR
Power:	Always on
Reset:	soft
Address:	45128h-4512Bh
Name:	Low Power 3 Sprite Watermarks
ShortName:	WM_LP3_SPR
Power:	Always on
Reset:	soft

This is the Low Power Sprite watermark value which will be used when display is in a LP state.
There is one instance of this register format per each LP level 1,2,3.

DWord	Bit	Description
0	31:10	**Reserved**
	9:0	**LP Sprite Watermark** Number in 64Bs of data in the display data buffer below which the Sprite Plane stream will wake memory.

WM_MISC

WM_MISC

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	45260h-45263h
Name:	Watermark Miscellaneous
ShortName:	WM_MISC
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31:19	**Reserved** Format: PBC
	18	**Reserved**
	17:4	**Reserved**
	3:2	**Reserved** Format: PBC
	1	**Reserved**
	0	**Data Buffer Partitioning** This bit controls the data buffer partitioning when between sprite and primay during low power states. Value / Name / Description: 0b / 1/2 / Sprite has 1/2 and primary has 1/2 of the buffer 1b / 5/6 / Sprite has 5/6 and primary has 1/6 of the buffer **Restriction** Restriction : The 5/6 setting is for use only when Frame Buffer Compression is enabled on the primary plane, or when the primary plane is disabled.

WM_LINETIME

WM_LINETIME	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000 [HSW]
Access:	R/W
Size (in bits):	32
Address:	45270h-45273h
Name:	Pipe A Watermark Line Time
ShortName:	WM_LINETIME_A
Power:	Always on
Reset:	soft
Address:	45274h-45277h
Name:	Pipe B Watermark Line Time
ShortName:	WM_LINETIME_B
Power:	Always on
Reset:	soft
Address:	45278h-4527Bh
Name:	Pipe C Watermark Line Time
ShortName:	WM_LINETIME_C
Power:	Always on
Reset:	soft

There is one instance of this register format per each pipe A,B,C.

Restriction
Restriction : The line time value must be programmed before enabling any display low power watermark.

DWord	Bit	Description
0	31:25	**Reserved**
	24:16	**Reserved** Project: DevHSW:GT0:X0, DevHSW:GT3:A
	24:16	**IPS Line Time** Project: DevHSW, EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A) The IPS line time for the current screen resolution in units of 0.125us. This value needs to be programmed before enabling IPS.

WM_LINETIME		
		IPS line time in microseconds = Pipe horizontal total number of pixels / CD clock frequency in MHz. Multiply by 8 to get units of 0.125us and round to nearest integer. This field is ignored for pipe B and pipe C. It only needs to be programmed for pipe A.
	15:9	**Reserved**
	8:0	**Line Time** The line time for the current screen resolution in units of 0.125us. **Programming Notes** Line time in microseconds = Pipe horizontal total number of pixels / pixel rate in MHz. Multiply by 8 to get units of 0.125us and round to nearest integer. Program the smallest line time when using multiple refresh rates. **Restriction** Restriction : Maximum supported line time is 63.875us (111111111b).

PWR_WELL_CTL1

PWR_WELL_CTL1

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	45400h-45403h
Name:	Power Well Control 1
ShortName:	PWR_WELL_CTL1
Power:	Always on
Reset:	global

This register is used for BIOS power well control.
This register is on the ungated clock and the chip reset, not the FLR or display debug reset.

DWord	Bit	Description
0	31	**BIOS Power Well Request** This bit will request the power well to enable or disable. Value / Name: 0b – Disable 1b – Enable Restriction: Restriction : This bit must not be changed while the power well enable/disable is currently in progress, as indicated by the power well state.
	30	**Power Well State** Access: RO This field indicates the status of the power well. Value / Name: 0b – Disabled 1b – Enabled
	29:0	**Reserved** Format: MBZ

PWR_WELL_CTL2

PWR_WELL_CTL2

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	45404h-45407h
Name:	Power Well Control 2
ShortName:	PWR_WELL_CTL2
Power:	Always on
Reset:	global

This register is used for driver power well control.
This register is on the ungated clock and the chip reset, not the FLR or display debug reset.

DWord	Bit	Description
0	31	**Driver Power Well Request** This bit will request the power well to enable or disable. Value / Name: 0b – Disable 1b – Enable Restriction: Restriction : This bit must not be changed while the power well enable/disable is currently in progress, as indicated by the power well state.
	30	**Power Well State** Access: RO This field indicates the status of the power well. Value / Name: 0b – Disabled 1b – Enabled
	29:0	**Reserved** Format: MBZ

SPLL_CTL

SPLL_CTL

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	46020h-46023h
Name:	SPLL Control
ShortName:	SPLL_CTL
Power:	Always on
Reset:	soft

The S PLL can drive the DDI ports at certain fixed frequencies for DisplayPort and FDI.
The PLL will automatically adjust for the reference frequency based on the reference select straps.

DWord	Bit	Description
0	31	**PLL Enable** This bit will enable or disable the PLL. Value / Name: 0b – Disable 1b – Enable Restriction: Restriction : This must not be changed while any port clock select is direct to this PLL.
	30	**Reserved** Format: MBZ
	29:28	**Reference Select** Select between PLL references. 01b – SSC – CPU internal SSC when CPU Internal SSC is fused enabled, else the PCH SSC reference. 10b – Non-SSC – Non-Spread reference – Restriction : Do not select on ULT. The 24 MHz reference (ULT Non-spread) is not supported with SPLL.

SPLL_CTL

		Programming Notes Spread reference is recommended. **Restriction** Restriction : This must not be changed while this PLL is enabled.
	27:26	**Frequency Select** Select between PLL frequencies. **Value** / **Name** / **Description** 00b / 810 MHz / 810 MHz (DisplayPort 1.62 GHz bit clock) 01b / 1350 MHz / 1350 MHz (FDI and DisplayPort 2.7 GHz bit clock) 11b / Reserved / Reserved
	25:0	**Reserved** Format: MBZ

WRPLL_CTL

WRPLL_CTL	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00202418
Access:	R/W
Size (in bits):	32
Address:	46040h-46043h
Name:	WRPLL Control 1
ShortName:	WRPLL_CTL1
Power:	Always on
Reset:	soft
Address:	46060h-46063h
Name:	WRPLL Control 2
ShortName:	WRPLL_CTL2
Power:	Always on
Reset:	soft

The WR PLL can drive the DDI ports at programmable frequencies for HDMI, DVI, DisplayPort, and FDI.

There are two instances of this register format to support the two WR PLLs.

The dividers must be programmed depending on the frequency of the selected reference. Check the FUSE_STRAP3 Reference_Clock_Select to find the frequency of the SSC and Non-SSC references.

Divider programming details are in the Display WRPLL clock frequency programming spreadsheet.

Programming Notes

The following formula is for reference only. Always follow the spreadsheet or algorithm to achieve the best quality.
Symbol or TMDS Frequency = (Reference Frequency / Reference Divider) * (Feedback Divider / Post Divider)

DWord	Bit	Description
0	31	**PLL Enable** This bit will enable or disable the PLL.

Value	Name
0b	Disable
1b	Enable

WRPLL_CTL

Restriction
Restriction : This must not be changed while any port clock select is directed to this PLL.

30 **Reserved**

Format:	MBZ

29:28 **Reference Select**

Select between PLL references.

Value	Name	Description
01b	PCH SSC	PCH Spread reference
10b	Special	On Non-ULT parts this selects the Non-SSC reference. On ULT parts this selects CPU internal SSC when CPU Internal SSC is fused enabled, else this selects the PCH SSC reference.
11b	LCPLL 2700	LCPLL 2700 MHz output

Programming Notes
Spread references are recommended for DisplayPort. PCH SSC is required for FDI. LCPLL 2700 MHz output is recommended for HDMI and DVI without clock bending. PCH SSC is required for HDMI and DVI with clock bending.

Restriction
Restriction : This must not be changed while this PLL is enabled.

27:24 **Reserved**

Format:	MBZ

23:16 **Feedback Divider**

Default Value:	20h 32

Feedback divider (VCO divider) value for the desired output frequency.
This is in a 7.1 format where the upper 7 bits represent the integer value and the lowest bit represents the fractional value.
This is the N value (N*2, 2*N, N2, or 2N when considering the entire 8 bits as a whole).

Restriction
Restriction : This must not be changed while this PLL is enabled.

15:14 **Reserved**

Format:	MBZ

13:8 **Post Divider**

Default Value:	24h 36

Post divider value for the desired output frequency.
This is the P value.

WRPLL_CTL

		Restriction Restriction : This must not be changed while this PLL is enabled.
	7:0	**Reference Divider** Default Value: 18h 24 Reference divider value for the desired output frequency. This is in a 7.1 format where the upper 7 bits represent the integer value and the lowest bit represents the fractional value. This is the R value (R*2, 2*R, R2, or 2R when considering the entire 8 bits as a whole). **Restriction** Restriction : This must not be changed while this PLL is enabled.

PORT_CLK_SEL

PORT_CLK_SEL	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0xE0000000
Access:	R/W
Size (in bits):	32
Address:	46100h-46103h
Name:	DDIA Port Clock Select
ShortName:	PORT_CLK_SEL_DDIA
Power:	Always on
Reset:	soft
Address:	46104h-46107h
Name:	DDIB Port Clock Select
ShortName:	PORT_CLK_SEL_DDIB
Power:	Always on
Reset:	soft
Address:	46108h-4610Bh
Name:	DDIC Port Clock Select
ShortName:	PORT_CLK_SEL_DDIC
Power:	Always on
Reset:	soft
Address:	4610Ch-4610Fh
Name:	DDID Port Clock Select
ShortName:	PORT_CLK_SEL_DDID
Power:	Always on
Reset:	soft
Address:	46110h-46113h
Name:	DDIE Port Clock Select
ShortName:	PORT_CLK_SEL_DDIE
Valid Projects:	[DevHSW, EXCLUDE(DevHSW:GT0:X0)]
Power:	Always on
Reset:	soft

PORT_CLK_SEL

This register maps the PLL to the port. There is one instance of this register format per DDI A/B/C/D/E.

This register maps the PLL to the port.
There is one instance of this register format per DDI A/B/C/D/E.

DWord	Bit	Description
0	31:29	**Port Clock Select** Select which PLL to use for this port. **Value / Name / Description** 000b / LCPLL 2700 / Select LCPLL 2700 MHz output (DisplayPort 5.4 GHz bit clock) **ULX devices do not support 5.4 GHz bit clock** 001b / LCPLL 1350 / Select LCPLL 1350 MHz output (DisplayPort 2.7 GHz bit clock 010b / LCPLL 810 / Select LCPLL 810 MHz output (DisplayPort 1.62 GHz bit clock) 011b / SPLL / Select SPLL (DisplayPort or FDI) 100b / WRPLL1 / Select WRPLL1 (HDMI, DVI, DisplayPort, or FDI) 101b / WRPLL2 / Select WRPLL2 (HDMI, DVI, DisplayPort, or FDI) 110b / Reserved / Reserved 111b / None **[Default]** / No PLL selected. Clock is disabled for this port. **Restriction** Restriction : This must not be changed while the port is enabled or any transcoder/pipe directed to the port is enabled.
	28:0	**Reserved** Format: MBZ

CDCLK_FREQ

CDCLK_FREQ	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x000001C1
Access:	R/W
Size (in bits):	32
Address:	46200h-46203h
Name:	CD Clock Frequency
ShortName:	CDCLK_FREQ
Valid Projects:	[DevHSW, EXCLUDE(DevHSW:GT0:X0)]
Power:	Always on
Reset:	global

DWord	Bit	Description
0	31:10	**Reserved** Format: MBZ
	9:0	**CDclk frequency** Default Value: 01 1100 0001b 450MHz Program this field to the CD clock frequency minus one. This is used to generate a divided down clock for miscellaneous timers in display. The CD clock frequency is selected in LCPLL_CTL. **Restriction** / **Project** Restriction : The CDCLK_FREQ register must be programmed with the correct value in order for the time stamp to run at the correct rate. The register value is ignored on other steppings. This register must be programmed again after FLR. / DevHSW:GT3:A

NDE_RSTWRN_OPT

NDE_RSTWRN_OPT

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000 [HSW]
Access:	R/W
Size (in bits):	32
Address:	46408h-4640Bh
Name:	North Display Reset Warn Options
ShortName:	NDE_RSTWRN_OPT
Power:	Always on
Reset:	global

This register is used to control the display behavior on receiving a Reset Warning.

DWord	Bit	Description
0	31:7	**Reserved** Format: MBZ
	6	**Reserved**
	5	**Reserved**
	4	**RST PCH Handshake En** This field enables the handshake with PCH display when processing the reset. This applies to all types of DE resets. By default it is disabled and the north display will not wait for south display to acknowledge the reset. The PCH display BDF is enabled by setting RCBA + 0x3428 bit 0 = 1b. 0:31:0 Root Complex Base Address Value: 0b = Disable; 1b = Enable Restriction : BIOS must set this to 1b after the PCH display BDF has been enabled and before enabling any function in the PCH display.
	3	**Reserved** Project: DevHSW, EXCLUDE(DevHSW:GT0:X0)
	3	**Reserved**

NDE_RSTWRN_OPT			
		Project:	DevHSW:GT0:X0
	2:0	**Reserved**	

BLC_PWM_CTL

BLC_PWM_CTL

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x60000000 [HSW]
Access:	R/W
Size (in bits):	32
Address:	48250h-48253h
Name:	Backlight PWM Control
ShortName:	BLC_PWM_CTL
Power:	Always on
Reset:	soft

This register controls the first backlight PWM and phase in logic. It can be used to drive the PWM pin on the CPU or on the PCH.

DWord	Bit	Description
0	31	**PWM Enable** This bit enables the PWM counter logic. Value / Name: 0b Disable; 1b Enable Programming Notes:
	30:29	**Transcoder Select** This field selects which transcoder vertical blank will be used for PWM phase in and backlight blinking. 00b Transcoder A — Use transcoder A - backlight blinking only 01b Transcoder B — Use transcoder B - backlight blinking only 10b Transcoder C — Use transcoder C - backlight blinking only 11b Transcoder EDP **[Default]** — Use transcoder EDP - phase ins or backlight blinking
	28	**Blinking Enable** This bit enables backlight blinking on the selected port. When enabled, the backlight will be driven on at the programmed brightness during vertical blank and driven off during vertical active.

Value	Name
0b	Disable
1b	Enable

Restriction
Restriction : This should not be used when driving the PCH PWM pin due to inherent delays in transmitting the brighness value to the PCH.

27 **Reserved**

Project:	DevHSW:GT0:X0, DevHSW:GT3:A

27 **PWM Granularity**

Project:	DevHSW, EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A)

This field controls the granularity (minimum increment) of the PWM backlight control counter when PWM1 is driving the CPU PWM pin (utility pin). This field is not used when PWM1 is driving the PCU PWM pin.

Value	Name	Description
0b	128	PWM frequency adjustment on 128 clock increments
1b	8	PWM frequency adjustment on 8 clock increments

26 **Phase In Interrupt Status**

Access:	R/WC

This bit will be set by hardware when a Phase-In interrupt has occurred.
Clear this bit by writing a '1', which will reset the interrupt generation.

Value	Name
0b	Phase-In interrupt has not occurred
1b	Phase-In interrupt has occurred

25 **Phase In Enable**

Phase In is no longer supported.

Value	Name
0b	Disable

24 **Phase In Interrupt Enable**

Setting this bit enables an interrupt to be generated when the PWM phase in is completed.

23:16 **Phase In time base**

This field determines the number of VBLANK events that pass before one increment occurs.

Value	Name	Description
00h	Invalid	
01h-FFh	Count	VBlank Count

Restriction

BLC_PWM_CTL		
		Restriction : A value of 0 is invalid.
	15:8	**Phase In Count** This field determines the number of increment events in this phase in. The read value indicates the number of increment events remaining to fully apply a phase-in request as hardware automatically decrements this value. **Restriction** Restriction : Write to this register only when hardware-phase-ins are disabled. A value of 0 is invalid.
	7:0	**Phase In Increment** This field indicates the amount to adjust the PWM duty cycle register on each increment event. This is a two's complement number.

BLC_PWM_DATA

BLC_PWM_DATA	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	48254h-48257h
Name:	Backlight PWM Data
ShortName:	BLC_PWM_DATA
Power:	Always on
Reset:	soft
Address:	48354h-48357h
Name:	Backlight PWM 2 Data
ShortName:	BLC_PWM2_DATA
Power:	Always on
Reset:	soft

Restriction
Restriction : This register must be written only as a full 32-bit dword. Byte or word writes are not supported.

DWord	Bit	Description
0	31:16	**Backlight Frequency** This field determines the number of time base events in total for a complete cycle of modulated backlight control. This field is programmed based on the frequency of the clock that is being used and the desired PWM frequency. This value represents the period of the PWM stream in CD clocks multiplied by 128 (default increment) or 8 (alternate increment selected by BLC_PWM*_CTL PWM_ Granularity). This field is only used when the PWM is driven to a pin on the CPU. For PWM driven to the PCH pin, program the frequency in the PCH register. The CPU pin will be driven when UTIL_PIN_CTRL is enabled and selecting this PWM.
	15:0	**Backlight Duty Cycle** This field determines the number of time base events for the active portion of the PWM backlight control. A value of zero will turn the backlight off. A value equal to the backlight modulation frequency field will be full on. Updates will take affect at the end of the current PWM cycle.

BLC_PWM_DATA		
		When driving the PWM to the pin on the CPU, this value represents the active time of the PWM stream in CD clocks multiplied by 128 (default increment) or 8 (alternate increment selected by BLC_PWM*_CTL PWM_Granularity). When driving the PWM to the pin on the CPU, this value represents the active time of the PWM stream in PCH clock periods (clock source and frequency depends on SKU) multiplied by an increment (increment is either 128 or 16, depending on the SKU). The CPU pin will be driven when UTIL_PIN_CTRL is enabled and selecting this PWM. **Restriction** Restriction : This should never be larger than the frequency field.

BLM_HIST_CTL

BLM_HIST_CTL

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	48260h-48263h
Name:	Image Enhancement Control
ShortName:	BLM_HIST_CTL
Power:	Always on
Reset:	soft

The Image Enhancement function is tied to pipe EDP.

DWord	Bit	Description
0	31	**IE Histogram Enable** This bit enables the Image Enhancement histogram logic to collect data. The collected data will be valid after a histogram event has occurred. Value: 0b = Disable; 1b = Enable
	30:28	**Reserved**
	27	**IE Modification Table Enable** This bit enables the Image Enhancement modification table. When enabled, modifications begin after the next vertical blank. Value: 0b = Disable; 1b = Enable
	26:25	**Reserved**
	24	**Histogram Mode Select** Value: 0b = YUV (YUV Luma Mode); 1b = HSV (HSV Intensity Mode)
	23:16	**Sync to Phase In Count** This field indicates the phase in count number on which the Image Enhancement table will be

BLM_HIST_CTL

		loaded if the Sync to Phase in is enabled.
	15	**IE Table Value Format** This field indicates what format is used for the image enhancement table values. **Value** / **Name** / **Description** 0b / 1.9 / 1 integer and 9 fractional bits 1b / 2.8 / 2 integer and 8 fractional bits
	14:13	**Enhancement mode** **Value** / **Name** / **Description** 00b / Direct / Direct look up mode 01b / Additive / Additive mode 10b / Multiplicative / Multiplicative mode 11b / Reserved / Reserved
	12	**Sync to Phase In** Setting this bit enables the double buffered registers to be loaded on the phase in count value specified instead of the next vblank.
	11	**Bin Register Function Select** This field indicates what data is being written to or read from the bin data register. **Value** / **Name** / **Description** 0b / TC / Threshold Count. A read from the bin data register returns that bin's threshold value from the most recent vblank load event (guardband threshold trip). Valid range for the Bin Index is 0 to 31. 1b / IE / Image Enhancement Value. Valid range for the Bin Index is 0 to 32
	10:7	**Reserved**
	6:0	**Bin Register Index** This field indicates the bin number whose data can be accessed through the bin data register. This value is automatically incremented by a read or a write to the bin data register if the busy bit is not set.

BLM_HIST_BIN

BLM_HIST_BIN	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Image Enhancement: Next vblank if in normal mode, or on phase in Sync event frame if it is enabled
Address:	48264h-48267h
Name:	Image Enhancement Bin Data
ShortName:	BLM_HIST_BIN
Power:	Always on
Reset:	soft

Access to this address are steered to the correct register by programming the Bin Register Function Select and the Bin Register Index.

DWord	Bit	Description
0	31	**Busy Bit** If (BLM_HIST_CTL:Bin Register Function Select = Threshold Count) {This is a read only bit. If set, the engine is busy and the rest of the register is undefined. If clear, the register contains valid data.} Else (Image Enhancement) {This bit is reserved.}
	30:22	**Reserved**
	21:0	**Bin Count or Correction Factor** If (BLM_HIST_CTL:Bin Register Function Select = Threshold Count) {Bits 21:0 are read only bits. They indicate the total number of pixels in this bin. The bin value is updated when guardband interrupt delay is met, and is not valid until after a histogram event has occurred. The bin value will stop incrementing once the maximum has been reached.} Else (Image Enhancement) {Bits 21:10 are reserved and should be written as zeroes. Bits 9:0 are R/W double-buffered and program the correction value for this bin. Writes to this register are double buffered on the next vblank if in normal mode, or on the phase in Sync event frame if it is enabled. The value written here is the 10bit corrected channel value for the lowest point of the bin. }

Note:	Project

BLM_HIST_BIN			
		Note: Prior to HSW C step, the histogram count may be slightly incorrect in some cases. The recommendation is to accept the histogram bin results if the sum of the bins is less than the expected pixels in a frame plus a threshold, otherwise ignore the result and start a new histogram. The threshold should be determined experimentally from the image quality results with different screen resolutions.	DevHSW, EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A), EXCLUDE(DevHSW:GT3:B)

BLM_HIST_GUARD

BLM_HIST_GUARD

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank

Address:	48268h-4826Bh
Name:	Histogram Threshold Guardband
ShortName:	BLM_HIST_GUARD
Power:	Always on
Reset:	soft

Updates take place at the start of vertical blank.

DWord	Bit	Description
0	31	**Histogram Interrupt enable** Value / Name / Description: 0b / Disable / Disabled 1b / Enable / This generates a histogram interrupt once a Histogram event occurs.
	30	**Histogram Event status** Access: R/WC When a Histogram event has occurred, this will get set by the hardware. For any more Histogram events to occur, clear this bit by writing a '1'. Value / Name / Description: 0b / Not Occurred / Histogram event has not occurred 1b / Occured / Histogram event has occurred **Note:** **Note:** The Histogram Event status may not clear if it is written with a 1b to clear it and the Histogram Interrupt enable field is changed from 0b to 1b in the same MMIO write. To guarantee the event status is cleared, separate the single MMIO write into two writes.
	29:22	**Guardband Interrupt Delay** An interrupt is always generated after this many consecutive frames of the guardband threshold being surpassed.

BLM_HIST_GUARD		
		This value is double buffered on start of vblank. **Restriction** Restriction : A value of 0 is invalid.
	21:0	**Threshold Guardband** This value is used to determine the guardband for the threshold interrupt generation. This single value is used for all the segments. This value is double buffered on start of vblank

BLC_PWM2_CTL

BLC_PWM2_CTL

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x60000000 [HSW]
Access:	R/W
Size (in bits):	32
Address:	48350h-48353h
Name:	Backlight PWM 2 Control
ShortName:	BLC_PWM2_CTL
Power:	Always on
Reset:	soft

This register controls the second backlight PWM. It can be used to drive the PWM pin on the CPU or on the PCH.

DWord	Bit	Description
0	31	**PWM2 Enable** This bit enables the PWM counter logic. Value / Name: 0b Disable; 1b Enable Restriction : Program the frequency and duty cycle before enabling PWM.
	30:29	**Transcoder Select** This field selects which transcoder vertical blank will be used for PWM phase in and backlight blinking. 00b Transcoder A - Use transcoder A - backlight blinking only 01b Transcoder B - Use transcoder B - backlight blinking only 10b Transcoder C - Use transcoder C - backlight blinking only 11b Transcoder EDP **[Default]** - Use transcoder EDP - phase ins or backlight blinking
	28	**Blinking Enable** This bit enables backlight blinking on the selected port. When enabled, the backlight will be driven on at the programmed brightness during vertical blank and driven off during vertical active. Value / Name

BLC_PWM2_CTL

		0b: Disable 1b: Enable **Restriction** Restriction : This should not be used when driving the PCH PWM pin due to inherent delays in transmitting the brighness value to the PCH.
	27	**Reserved** Project: DevHSW:GT0:X0, DevHSW:GT3:A
	27	**PWM Granularity** Project: DevHSW, EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A) This field controls the granularity (minimum increment) of the PWM backlight control counter when PWM2 is driving the CPU PWM pin (utility pin). This field is not used when PWM2 is driving the PCU PWM pin. **Value** / **Name** / **Description** 0b / 128 / PWM frequency adjustment on 128 clock increments 1b / 8 / PWM frequency adjustment on 8 clock increments
	26:0	**Reserved**

BLC_PWM_DATA

BLC_PWM_DATA	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	48254h-48257h
Name:	Backlight PWM Data
ShortName:	BLC_PWM_DATA
Power:	Always on
Reset:	soft
Address:	48354h-48357h
Name:	Backlight PWM 2 Data
ShortName:	BLC_PWM2_DATA
Power:	Always on
Reset:	soft

Restriction
Restriction : This register must be written only as a full 32-bit dword. Byte or word writes are not supported.

DWord	Bit	Description
0	31:16	**Backlight Frequency** This field determines the number of time base events in total for a complete cycle of modulated backlight control. This field is programmed based on the frequency of the clock that is being used and the desired PWM frequency. This value represents the period of the PWM stream in CD clocks multiplied by 128 (default increment) or 8 (alternate increment selected by BLC_PWM*_CTL PWM_ Granularity). This field is only used when the PWM is driven to a pin on the CPU. For PWM driven to the PCH pin, program the frequency in the PCH register. The CPU pin will be driven when UTIL_PIN_CTRL is enabled and selecting this PWM.
	15:0	**Backlight Duty Cycle** This field determines the number of time base events for the active portion of the PWM backlight control. A value of zero will turn the backlight off. A value equal to the backlight modulation frequency field will be full on. Updates will take affect at the end of the current PWM cycle.

BLC_PWM_DATA		
		When driving the PWM to the pin on the CPU, this value represents the active time of the PWM stream in CD clocks multiplied by 128 (default increment) or 8 (alternate increment selected by BLC_PWM*_CTL PWM_Granularity). When driving the PWM to the pin on the CPU, this value represents the active time of the PWM stream in PCH clock periods (clock source and frequency depends on SKU) multiplied by an increment (increment is either 128 or 16, depending on the SKU). The CPU pin will be driven when UTIL_PIN_CTRL is enabled and selecting this PWM. **Restriction** Restriction : This should never be larger than the frequency field.

BLC_MISC_CTL

BLC_MISC_CTL

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	48360h-48363h
Name:	Backlight Miscellaneous Control
ShortName:	BLC_MISC_CTL
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31:1	**Reserved**
	0	**PWM Pin Select** This field selects which PWM will drive the CPU PWM pin (Utility Pin) and which will drive the PCH PWM pin. **Value** / **Name** / **Description** 0b / PWM1-PCH PWM2-CPU / PWM1 will drive the PCH PWM pin, and PWM2 will drive the CPU PWM pin (utility pin). 1b / PWM1-CPU PWM2-PCH / PWM1 will drive the CPU PWM pin (utility pin), and PWM2 will drive the PCH PWM pin. **Restriction** Restriction : The field should only be changed when both PWMs are disabled.

UTIL_PIN_CTL

UTIL_PIN_CTL	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	48400h-48403h
Name:	Utility Pin Control
ShortName:	UTIL_PIN_CTL
Power:	Always on
Reset:	soft

This register controls the display utility pin. The nominal supply is 1 Volt and can be level shifted depending on usage. The maximum switching frequency is 100 KHz.

DWord	Bit	Description
0	31	**Util Pin Enable** This bit enables the utility pin. Value / Name: 0b – Disable 1b – Enable
	30:29	**Transcoder Select** This bit selects which transcoder will be used when the utility pin is outputting timing related signals. Value / Name: 00b – Transcoder A 01b – Transcoder B 10b – Transcoder C 11b – Transcoder EDP Restriction : The field should only be changed when the utility pin is disabled or not configured to use any timing signals.
	28	**Reserved**
	27:24	**Util Pin Mode** This bit configures the utility pin mode of operation.

UTIL_PIN_CTL

Value	Name	Description
0000b	Data	Output the Util_Pin_Output_Data value.
0001b	PWM	Output from the backlight PWM circuit. The choice between PWM1 and PWM2 is made in BLC_MISC_CTL.
0100b	Vblank	Output the vertical blank.
0101b	Vsync	Output the vertical sync.
Others	Reserved	Reserved

Restriction
Restriction : The field should only be changed when the utility pin is disabled.

23 **Util Pin Output Data**

This bit selects what the value to drive as an output when in the data mode.

Value	Name
0b	0
1b	1

22 **Util Pin Output Polarity**

This bit inverts the polarity of the pin output.

Value	Name
0b	Not inverted
1b	Inverted

21:0 **Reserved**

CSC_COEFF

CSC_COEFF		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000	
Access:	Double Buffered	
Size (in bits):	192	
Double Buffer Update Point:	Start of vertical blank after armed	
Double Buffer Armed By:	Write to CSC_MODE	
Address:	49010h-49027h	
Name:	Pipe A CSC Coefficients	
ShortName:	CSC_COEFF_A_*	
Power:	Always on	
Reset:	soft	
Address:	49110h-49127h	
Name:	Pipe B CSC Coefficients	
ShortName:	CSC_COEFF_B_*	
Power:	off/on	
Reset:	soft	
Address:	49210h-49227h	
Name:	Pipe C CSC Coefficients	
ShortName:	CSC_COEFF_C_*	
Power:	off/on	
Reset:	soft	

DWord	Bit	Description
0	31:16	**RY** Format: CSC COEFFICIENT FORMAT
	15:0	**GY** Format: CSC COEFFICIENT FORMAT
1	31:16	**BY** Format: CSC COEFFICIENT FORMAT
	15:0	**Reserved**

CSC_COEFF		
		Format: MBZ
2	31:16	**RU** Format: CSC COEFFICIENT FORMAT
	15:0	**GU** Format: CSC COEFFICIENT FORMAT
3	31:16	**BU** Format: CSC COEFFICIENT FORMAT
	15:0	**Reserved** Format: MBZ
4	31:16	**RV** Format: CSC COEFFICIENT FORMAT
	15:0	**GV** Format: CSC COEFFICIENT FORMAT
5	31:16	**BV** Format: CSC COEFFICIENT FORMAT
	15:0	**Reserved** Format: MBZ

CSC_MODE

CSC_MODE	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank
Address:	49028h-4902Bh
Name:	Pipe A CSC Mode
ShortName:	CSC_MODE_A
Power:	Always on
Reset:	soft
Address:	49128h-4912Bh
Name:	Pipe B CSC Mode
ShortName:	CSC_MODE_B
Power:	off/on
Reset:	soft
Address:	49228h-4922Bh
Name:	Pipe C CSC Mode
ShortName:	CSC_MODE_C
Power:	off/on
Reset:	soft

Writes to this register arm CSC registers for this pipe.

DWord	Bit	Description
0	31:2	**Reserved**
	1	**CSC Position** Selects the CSC position in the pipe. This is ignored when split gamma mode is selected in the pipe config register. Value / Name / Description: 0b / CSC After / CSC is after gamma 1b / CSC Before / CSC is before gamma
	0	**Reserved** Format: MBZ

CSC_PREOFF

CSC_PREOFF	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000, 0x00000000, 0x00000000
Access:	Double Buffered
Size (in bits):	96
Double Buffer Update Point:	Start of vertical blank after armed
Double Buffer Armed By:	Write to CSC_MODE

Address:	49030h-4903Bh
Name:	Pipe A CSC Pre-Offsets
ShortName:	CSC_PREOFF_A_*
Power:	Always on
Reset:	soft

Address:	49130h-4913Bh
Name:	Pipe B CSC Pre-Offsets
ShortName:	CSC_PREOFF_B_*
Power:	off/on
Reset:	soft

Address:	49230h-4923Bh
Name:	Pipe C CSC Pre-Offsets
ShortName:	CSC_PREOFF_C_*
Power:	off/on
Reset:	soft

The pre-offset is intended to remove an offset from 0 on the Y or RGB channels and to convert UV channels from excess 0.5 to 2's complement as they enter pipe color space conversion (CSC).

DWord	Bit	Description
0	31:13	**Reserved** Format: MBZ
	12:0	**PreCSC High Offset** This value is used to give an offset to the high color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).

CSC_PREOFF		
1	31:13	**Reserved** Format: MBZ
	12:0	**PreCSC Medium Offset** This value is used to give an offset to the medium color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
2	31:13	**Reserved** Format: MBZ
	12:0	**PreCSC Low Offset** This value is used to give an offset to the low color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).

CSC_POSTOFF

CSC_POSTOFF	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000, 0x00000000, 0x00000000
Access:	Double Buffered
Size (in bits):	96
Double Buffer Update Point:	Start of vertical blank after armed
Double Buffer Armed By:	Write to CSC_MODE
Address:	49040h-4904Bh
Name:	Pipe A CSC Post-Offsets
ShortName:	CSC_POSTOFF_A_*
Power:	Always on
Reset:	soft
Address:	49140h-4914Bh
Name:	Pipe B CSC Post-Offsets
ShortName:	CSC_POSTOFF_B_*
Power:	off/on
Reset:	soft
Address:	49240h-4924Bh
Name:	Pipe C CSC Post-Offsets
ShortName:	CSC_POSTOFF_C_*
Power:	off/on
Reset:	soft

The post-offset is intended to add an offset from 0 on the Y or RGB channels and to convert UV channels from 2's complement to excess 0.5 as they exit pipe color space conversion (CSC).

DWord	Bit	Description
0	31:13	**Reserved** Format: MBZ
	12:0	**PostCSC High Offset** This value is used to give an offset to the high color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).

CSC_POSTOFF		
1	31:13	**Reserved** Format: MBZ
	12:0	**PostCSC Medium Offset** This value is used to give an offset to the medium color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
2	31:13	**Reserved** Format: MBZ
	12:0	**PostCSC Low Offset** This value is used to give an offset to the low color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).

CGE_CTRL

CGE_CTRL	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank
Address:	49080h-49083h
Name:	Pipe A Color Gamut Enhancement Control
ShortName:	CGE_CTRL_A
Power:	Always on
Reset:	soft
Address:	49180h-49183h
Name:	Pipe B Color Gamut Enhancement Control
ShortName:	CGE_CTRL_B
Power:	off/on
Reset:	soft
Address:	49280h-49283h
Name:	Pipe C Color Gamut Enhancement Control
ShortName:	CGE_CTRL_C
Power:	off/on
Reset:	soft

DWord	Bit	Description
0	31	**CGE Enable** This bit enables the Color Gamut Enhancement logic. Value: 0b — Name: Disable Value: 1b — Name: Enable
	30:0	**Reserved** Format: MBZ

CGE_WEIGHT

CGE_WEIGHT	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000
Access:	R/W
Size (in bits):	160
Address:	49090h-490A3h
Name:	Pipe A Color Gamut Enhancement Weights
ShortName:	CGE_WEIGHT_A_*
Power:	Always on
Reset:	soft
Address:	49190h-491A3h
Name:	Pipe B Color Gamut Enhancement Weights
ShortName:	CGE_WEIGHT_B_*
Power:	off/on
Reset:	soft
Address:	49290h-492A3h
Name:	Pipe C Color Gamut Enhancement Weights
ShortName:	CGE_WEIGHT_C_*
Power:	off/on
Reset:	soft

These are the weights contained in the lookup up table (LUT) used in pipe color gamut enhancement.
LUT index 0 contains the weight for the least saturated colors, and LUT index 16 contains the weight for the most saturated colors.
Weight values can range from 00000b (100% of the enhanced output color is from the pipe gamma and CSC output corrected color) to 100000b (100% of the enhanced output color is from the pipe gamma and CSC input color).

Restriction
Restriction : The weight values should only be changed while color gamut enhancement is disabled, otherwise screen artifacts may show temporarily.

DWord	Bit	Description
0	31:30	**Reserved** Format: MBZ

CGE_WEIGHT		
	29:24	**CGE Weight Index 3** This is the weight value for this color gamut enhancement LUT index.
	23:22	**Reserved** Format: MBZ
	21:16	**CGE Weight Index 2** This is the weight value for this color gamut enhancement LUT index.
	15:14	**Reserved** Format: MBZ
	13:8	**CGE Weight Index 1** This is the weight value for this color gamut enhancement LUT index.
	7:6	**Reserved** Format: MBZ
	5:0	**CGE Weight Index 0** This is the weight value for this color gamut enhancement LUT index.
1	31:30	**Reserved** Format: MBZ
	29:24	**CGE Weight Index 7** This is the weight value for this color gamut enhancement LUT index.
	23:22	**Reserved** Format: MBZ
	21:16	**CGE Weight Index 6** This is the weight value for this color gamut enhancement LUT index.
	15:14	**Reserved** Format: MBZ
	13:8	**CGE Weight Index 5** This is the weight value for this color gamut enhancement LUT index.
	7:6	**Reserved** Format: MBZ
	5:0	**CGE Weight Index 4** This is the weight value for this color gamut enhancement LUT index.
2	31:30	**Reserved** Format: MBZ
	29:24	**CGE Weight Index 11** This is the weight value for this color gamut enhancement LUT index.
	23:22	**Reserved** Format: MBZ
	21:16	**CGE Weight Index 10**

CGE_WEIGHT		
		This is the weight value for this color gamut enhancement LUT index.
	15:14	**Reserved** Format: MBZ
	13:8	**CGE Weight Index 9** This is the weight value for this color gamut enhancement LUT index.
	7:6	**Reserved** Format: MBZ
	5:0	**CGE Weight Index 8** This is the weight value for this color gamut enhancement LUT index.
3	31:30	**Reserved** Format: MBZ
	29:24	**CGE Weight Index 15** This is the weight value for this color gamut enhancement LUT index.
	23:22	**Reserved** Format: MBZ
	21:16	**CGE Weight Index 14** This is the weight value for this color gamut enhancement LUT index.
	15:14	**Reserved** Format: MBZ
	13:8	**CGE Weight Index 13** This is the weight value for this color gamut enhancement LUT index.
	7:6	**Reserved** Format: MBZ
	5:0	**CGE Weight Index 12** This is the weight value for this color gamut enhancement LUT index.
4	31:6	**Reserved** Format: MBZ
	5:0	**CGE Weight Index 16** This is the weight value for this color gamut enhancement LUT index.

PAL_LGC – Pipe A-C Legacy Palettes 0-255

PAL_LGC	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	4A000h-4A3FFh
Name:	Pipe A Legacy Palette
ShortName:	PAL_LGC_A_*
Power:	Always on
Reset:	soft
Address:	4A800h-4ABFFh
Name:	Pipe B Legacy Palette
ShortName:	PAL_LGC_B_*
Power:	off/on
Reset:	soft
Address:	4B000h-4B3FFh
Name:	Pipe C Legacy Palette
ShortName:	PAL_LGC_C_*
Power:	off/on
Reset:	soft
There are 256 instances of this register format per display pipe.	

Note:
Note: Do not read or write the pipe palette/gamma data while GAMMA_MODE is configured for split gamma and IPS_CTL has IPS enabled.

Restriction
Restriction : This register must be written only as a full 32 bit dword. Byte or word writes are not supported.

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:16	**Red Legacy Palette Entry**

PAL_LGC		
		Default Value: UUh Red legacy palette entry value.
	15:8	**Green Legacy Palette Entry** Default Value: UUh Green legacy palette entry value.
	7:0	**Blue Legacy Palette Entry** Default Value: UUh Blue legacy palette entry value.

PAL_PREC_INDEX

PAL_PREC_INDEX	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	4A400h-4A403h
Name:	Pipe A Precision Palette Index
ShortName:	PAL_PREC_INDEX_A
Power:	Always on
Reset:	soft
Address:	4AC00h-4AC03h
Name:	Pipe B Precision Palette Index
ShortName:	PAL_PREC_INDEX_B
Power:	off/on
Reset:	soft
Address:	4B400h-4B403h
Name:	Pipe C Precision Palette Index
ShortName:	PAL_PREC_INDEX_C
Power:	off/on
Reset:	soft

This index controls access to the array of precision palette data values.

DWord	Bit	Description
0	31	**Precision Palette Format** This field selects the format of the precision palette data. Value / Name / Description: 0b / Non-split / 10 bpc or 12 bpc gamma format 1b / Split / Split gamma format **Restriction** Restriction : It must be set when reading or writing precision palette entries for split gamma mode. It must be cleared before programming the legacy palette.

PAL_PREC_INDEX

	30:16	**Reserved** Format: MBZ
	15	**Index Auto Increment** This field enables the index auto increment. **Value** / **Name** / **Description** 0b / No Increment / Do not automatically increment the index value. **Restriction** Restriction : Index auto increment mode is not supported and must not be enabled.
	14:10	**Reserved** Format: MBZ
	9:0	**Index Value** This field indicates the data location to be accessed through the data register. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set. When automatically incrementing, the current automatically calculated index value can be read here, and the index will roll over to 0 after reaching the end of the allowed range. **Value** / **Name** [0,1023]

PAL_PREC_DATA

PAL_PREC_DATA	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	4A404h-4A407h
Name:	Pipe A Precision Palette Data
ShortName:	PAL_PREC_DATA_A
Power:	Always on
Reset:	soft
Address:	4AC04h-4AC07h
Name:	Pipe B Precision Palette Data
ShortName:	PAL_PREC_DATA_B
Power:	off/on
Reset:	soft
Address:	4B404h-4B407h
Name:	Pipe C Precision Palette Data
ShortName:	PAL_PREC_DATA_C
Power:	off/on
Reset:	soft

These are the precision palette entries used for the 10 bpc, split, and 12 bpc gamma.
The Precision Palette Index Value indicates the precision palette location to be accessed through this register.

Programming Notes

For 10 bpc, program with the color 10 bit palette entry fraction value.

For 12 bpc gamma odd indexes, program with the upper 10 bits of the color palette entry fraction value.
For 12 bpc gamma even indexes, program the MSbs with the lower 6 bits of the color palette entry fraction value, then program all 0s in the LSbs.

For split gamma indexes 0 to 511, program with the first gamma (before CSC) color 10 bit palette entry fraction value.
For split gamma indexes 512 to 1023, program with the second gamma (after CSC) color 10 bit palette entry fraction value.

PAL_PREC_DATA

Note:
Note: Do not read or write the pipe palette/gamma data while GAMMA_MODE is configured for split gamma and IPS_CTL has IPS enabled.

Restriction
Restriction : This register must be written only as a full 32 bit dword. Byte or word writes are not supported.

DWord	Bit	Description
0	31:30	**Reserved**
	29:20	**Red Precision Palette Entry** Default Value: UUUUUUUUUUb Red precision palette entry value.
	19:10	**Green Precision Palette Entry** Default Value: UUUUUUUUUUb Green precision palette entry value.
	9:0	**Blue Precision Palette Entry** Default Value: UUUUUUUUUUb Blue precision palette entry value.

PAL_GC_MAX

PAL_GC_MAX	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00010000, 0x00010000, 0x00010000
Access:	R/W
Size (in bits):	96
Address:	4A410h-4A41Bh
Name:	Pipe A Gamma Correction Max
ShortName:	PAL_GC_MAX_A_*
Power:	Always on
Reset:	soft
Address:	4AC10h-4AC1Bh
Name:	Pipe B Gamma Correction Max
ShortName:	PAL_GC_MAX_B_*
Power:	off/on
Reset:	soft
Address:	4B410h-4B41Bh
Name:	Pipe C Gamma Correction Max
ShortName:	PAL_GC_MAX_C_*
Power:	off/on
Reset:	soft

DWord	Bit	Description
0	31:17	**Reserved** Format: MBZ
	16:0	**Red Max GC Point** Default Value: 10000000000000000b Format: U1.16 The 513th entry for the red color channel of the 12 bit interpolated gamma correction. This value is represented in a 1.16 format with 1 integer and 16 fractional bits. **Restriction** Restriction : The value should always be programmed to be less than or equal to 1.0.
1	31:17	**Reserved**

PAL_GC_MAX

		Format: MBZ
	16:0	**Green Max GC Point** Default Value: 10000000000000000b Format: U1.16 The 513th entry for the green color channel of the 12 bit interpolated gamma correction. This value is represented in a 1.16 format with 1 integer and 16 fractional bits. **Restriction** Restriction : The value should always be programmed to be less than or equal to 1.0.
2	31:17	**Reserved** Format: MBZ
	16:0	**Blue Max GC Point** Default Value: 10000000000000000b Format: U1.16 The 513th entry for the blue color channel of the 12 bit interpolated gamma correction. This value is represented in a 1.16 format with 1 integer and 16 fractional bits. **Restriction** Restriction : The value should always be programmed to be less than or equal to 1.0.

PAL_EXT_GC_MAX

PAL_EXT_GC_MAX	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x0007FFFF, 0x0007FFFF, 0x0007FFFF
Access:	R/W
Size (in bits):	96
Address:	4A420h-4A42Bh
Name:	Pipe A Extended Gamma Correction Max
ShortName:	PAL_EXT_GC_MAX_A_*
Power:	Always on
Reset:	soft
Address:	4AC20h-4AC2Bh
Name:	Pipe B Extended Gamma Correction Max
ShortName:	PAL_EXT_GC_MAX_B_*
Power:	off/on
Reset:	soft
Address:	4B420h-4B42Bh
Name:	Pipe C Extended Gamma Correction Max
ShortName:	PAL_EXT_GC_MAX_C_*
Power:	off/on
Reset:	soft

Note:	Project
Note: The values must be programmed to be less than 4.0 when pipe CSC is enabled and pipe gamma is placed before pipe CSC or split gamma is used.	DevHSW:GT0:X0

DWord	Bit	Description
0	31:19	**Reserved** Format: MBZ
	18:0	**Red Ext Max GC Point** Default Value: 11111111111111111b Format: U3.16 The extended point for red color channel gamma correction. This value is represented in a 3.16 format with 3 integer and 16 fractional bits.

PAL_EXT_GC_MAX

1	31:19	**Reserved** Format: MBZ
	18:0	**Green Ext Max GC Point** Default Value: 11111111111111111b Format: U3.16 The extended point for green color channel gamma correction. This value is represented in a 3.16 format with 3 integer and 16 fractional bits.
2	31:19	**Reserved** Format: MBZ
	18:0	**Blue Ext Max GC Point** Default Value: 11111111111111111b Format: U3.16 The extended point for blue color channel gamma correction. This value is represented in a 3.16 format with 3 integer and 16 fractional bits.

SWF – Software Flags 0-36

SWF	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	4F000h-4F08Fh
Name:	Software Flags
ShortName:	SWF_*
Power:	Always on
Reset:	soft

These registers are used as scratch pad data storage space and have no direct effect on hardware operation. There are 36 instances of this register format.

DWord	Bit	Description
0	31:0	**Software Flags** Software flags

GTSCRATCH

GTSCRATCH	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	4F100h-4F11Fh
Name:	GT Scratchpad
ShortName:	GTSCRATCH_*
Power:	Always on
Reset:	soft

There are 8 instances of this register format.

Restriction
Restriction : These registers are used by hardware and must not be used by software.

DWord	Bit	Description
0	31:0	**GT Sratchpad** GT Scratchpad

PIPE_HTOTAL

PIPE_HTOTAL	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	60000h-60003h
Name:	Pipe A Horizontal Total
ShortName:	PIPE_HTOTAL_A
Power:	off/on
Reset:	soft
Address:	61000h-61003h
Name:	Pipe B Horizontal Total
ShortName:	PIPE_HTOTAL_B
Power:	off/on
Reset:	soft
Address:	62000h-62003h
Name:	Pipe C Horizontal Total
ShortName:	PIPE_HTOTAL_C
Power:	off/on
Reset:	soft
Address:	6F000h-6F003h
Name:	Pipe EDP Horizontal Total
ShortName:	PIPE_HTOTAL_EDP
Power:	Always on
Reset:	soft

There is one instance of this register for each pipe A/B/C/EDP.

Restriction
Restriction : This register should not be changed while the pipe or port are enabled.

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ

PIPE_HTOTAL		
	28:16	**Horizontal Total** This field specifies Horizontal Total size. This should be equal to the sum of the horizontal active and the horizontal blank sizes. This field is programmed to the number of pixels desired minus one. **Restriction** Restriction : This register must always be programmed to the same value as the Horizontal Blank End.
	15:13	**Reserved** Format: MBZ
	12:0	**Horizontal Active** This field specifies Horizontal Active Display size. The first horizontal active display pixel is considered pixel number 0. This field is programmed to the number of pixels desired minus one. **Restriction** Restriction : The minimum horizontal active display size is 64 pixels. In HDMI modes the minimum is 256 pixels. This register must always be programmed to the same value as the Horizontal Blank Start. In FDI mode bit 12 must not be set.

PIPE_HBLANK

PIPE_HBLANK	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	60004h-60007h
Name:	Pipe A Horizontal Blank
ShortName:	PIPE_HBLANK_A
Power:	off/on
Reset:	soft
Address:	61004h-61007h
Name:	Pipe B Horizontal Blank
ShortName:	PIPE_HBLANK_B
Power:	off/on
Reset:	soft
Address:	62004h-62007h
Name:	Pipe C Horizontal Blank
ShortName:	PIPE_HBLANK_C
Power:	off/on
Reset:	soft
Address:	6F004h-6F007h
Name:	Pipe EDP Horizontal Blank
ShortName:	PIPE_HBLANK_EDP
Power:	Always on
Reset:	soft

There is one instance of this register for each pipe A/B/C/EDP.

Restriction
Restriction : This register should not be changed while the pipe or port are enabled.

DWord	Bit	Description
0	31:29	**Reserved**
	28:16	**Horizontal Blank End**

PIPE_HBLANK		
		This field specifies Horizontal Blank End position relative to the horizontal active display start. **Restriction** Restriction : The minimum horizontal blank size is 32 pixels. For HDMI Audio transmission the minimum is 138 pixels. This register must always be programmed to the same value as the Horizontal Total.
	15:13	**Reserved**
	12:0	**Horizontal Blank Start** This field specifies the Horizontal Blank Start position relative to the horizontal active display start. **Restriction** Restriction : This register must always be programmed to the same value as the Horizontal Active. In FDI mode bit 12 must not be set.

PIPE_HSYNC

PIPE_HSYNC	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	60008h-6000Bh
Name:	Pipe A Horizontal Sync
ShortName:	PIPE_HSYNC_A
Power:	off/on
Reset:	soft
Address:	61008h-6100Bh
Name:	Pipe B Horizontal Sync
ShortName:	PIPE_HSYNC_B
Power:	off/on
Reset:	soft
Address:	62008h-6200Bh
Name:	Pipe C Horizontal Sync
ShortName:	PIPE_HSYNC_C
Power:	off/on
Reset:	soft
Address:	6F008h-6F00Bh
Name:	Pipe EDP Horizontal Sync
ShortName:	PIPE_HSYNC_EDP
Power:	Always on
Reset:	soft

There is one instance of this register for each pipe A/B/C/EDP.

Restriction
Restriction : This register should not be changed while the pipe or port are enabled.

DWord	Bit	Description	
0	31:29	**Reserved**	
		Format:	MBZ

PIPE_HSYNC

	28:16	**Horizontal Sync End** This field specifies the Horizontal Sync End position relative to the horizontal active display start. It is programmed with HorizontalActive+FrontPorch+Sync-1 **Restriction** Restriction : This value must be greater than the horizontal sync start and less than Horizontal Total.
	15:13	**Reserved** Format: MBZ
	12:0	**Horizontal Sync Start** This field specifies the Horizontal Sync Start position relative to the horizontal active display start. It is programmed with HorizontalActive + FrontPorch - 1 **Restriction** Restriction : This value must be greater than Horizontal Active. In HDMI modes the minimum gap between horizontal blank start and horizontal sync start is 16 pixels.

PIPE_VTOTAL

PIPE_VTOTAL	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6000Ch-6000Fh
Name:	Pipe A Vertical Total
ShortName:	PIPE_VTOTAL_A
Power:	off/on
Reset:	soft
Address:	6100Ch-6100Fh
Name:	Pipe B Vertical Total
ShortName:	PIPE_VTOTAL_B
Power:	off/on
Reset:	soft
Address:	6200Ch-6200Fh
Name:	Pipe C Vertical Total
ShortName:	PIPE_VTOTAL_C
Power:	off/on
Reset:	soft
Address:	6F00Ch-6F00Fh
Name:	Pipe EDP Vertical Total
ShortName:	PIPE_VTOTAL_EDP
Power:	Always on
Reset:	soft
There is one instance of this register for each pipe A/B/C/EDP.	

Note:
Note: When the PIPE_DDI_FUNC_CTL EDP input selection is B, the PIPE_VTOTAL_B must be programmed with the PIPE_VTOTAL_EDP value. When the PIPE_DDI_FUNC_CTL EDP input selection is C, the PIPE_VTOTAL_C must be programmed with the PIPE_VTOTAL_EDP value.

PIPE_VTOTAL

Restriction
Restriction : This register should not be changed while the pipe or port are enabled.

DWord	Bit	Description
0	31:29	**Reserved**
	28:16	**Vertical Total** This field specifies Vertical Total size. This should be equal to the sum of the vertical active and the vertical blank sizes. For progressive display modes, this field is programmed to the number of lines desired minus one. For interlaced display modes, this field is programmed with the number of lines desired minus two. The vertical counter is incremented on the leading edge of the horizontal sync. Both even and odd vertical totals are supported. **Restriction** Restriction : This register must always be programmed to the same value as the Vertical Blank End.
	15:12	**Reserved**
	11:0	**Vertical Active** This field specifies Vertical Active Display size. The first vertical active display line is considered line number 0. This field is programmed to the number of lines desired minus one. **Restriction** Restriction : When using the internal panel fitting logic, the minimum vertical active area must be seven lines. This register must always be programmed to the same value as the Vertical Blank Start.

PIPE_VBLANK

PIPE_VBLANK	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	60010h-60013h
Name:	Pipe A Vertical Blank
ShortName:	PIPE_VBLANK_A
Power:	off/on
Reset:	soft
Address:	61010h-61013h
Name:	Pipe B Vertical Blank
ShortName:	PIPE_VBLANK_B
Power:	off/on
Reset:	soft
Address:	62010h-62013h
Name:	Pipe C Vertical Blank
ShortName:	PIPE_VBLANK_C
Power:	off/on
Reset:	soft
Address:	6F010h-6F013h
Name:	Pipe EDP Vertical Blank
ShortName:	PIPE_VBLANK_EDP
Power:	Always on
Reset:	soft

There is one instance of this register for each pipe A/B/C/EDP.

Restriction
Restriction : This register should not be changed while the pipe or port are enabled.

DWord	Bit	Description
0	31:29	**Reserved**
	28:16	**Vertical Blank End**

PIPE_VBLANK		
		This field specifies Vertical Blank End position relative to the vertical active display start. **Restriction** Restriction : This register must always be programmed to the same value as the Vertical Total. The minimum vertical blank size is 5 lines. With SRD/PSR and/or DisplayPort VDIP GMP the minimum is 8 lines.
	15:13	**Reserved**
	12:0	**Vertical Blank Start** This field specifies the Vertical Blank Start position relative to the vertical active display start. **Restriction** Restriction : This register must always be programmed to the same value as the Vertical Active.

PIPE_VSYNC

PIPE_VSYNC	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	60014h-60017h
Name:	Pipe A Vertical Sync
ShortName:	PIPE_VSYNC_A
Power:	off/on
Reset:	soft
Address:	61014h-61017h
Name:	Pipe B Vertical Sync
ShortName:	PIPE_VSYNC_B
Power:	off/on
Reset:	soft
Address:	62014h-62017h
Name:	Pipe C Vertical Sync
ShortName:	PIPE_VSYNC_C
Power:	off/on
Reset:	soft
Address:	6F014h-6F017h
Name:	Pipe EDP Vertical Sync
ShortName:	PIPE_VSYNC_EDP
Power:	Always on
Reset:	soft

There is one instance of this register for each pipe A/B/C/EDP.

Restriction
Restriction : This register should not be changed while the pipe or port are enabled.

DWord	Bit	Description
0	31:29	**Reserved**
	28:16	**Vertical Sync End**

PIPE_VSYNC		
		This field specifies the Vertical Sync End position relative to the vertical active display start. It is programmed with VerticalActive+FrontPorch+Sync-1 **Restriction** Restriction : This value must be greater than the vertical sync start and less than Vertical Total.
	15:13	**Reserved**
	12:0	**Vertical Sync Start** This field specifies the Vertical Sync Start position relative to the vertical active display start. It is programmed with VerticalActive+FrontPorch-1 **Restriction** Restriction : This value must be greater than Vertical Active.

PIPE_SRCSZ

PIPE_SRCSZ	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank
Address:	6001Ch-6001Fh
Name:	Pipe A Source Image Size
ShortName:	PIPE_SRCSZ_A
Power:	Always on
Reset:	soft
Address:	6101Ch-6101Fh
Name:	Pipe B Source Image Size
ShortName:	PIPE_SRCSZ_B
Power:	off/on
Reset:	soft
Address:	6201Ch-6201Fh
Name:	Pipe C Source Image Size
ShortName:	PIPE_SRCSZ_C
Power:	off/on
Reset:	soft

There is one instance of this register for each pipe A/B/C.

Programming Notes

In VGA display mode, this register is ignored and the VGA size from the VGA registers is used instead.

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28:16	**Horizontal Source Size** This field specifies Horizontal Source Size. This determines the horizontal size of the image created by the display planes. This field is programmed to the number of pixels desired minus one.

PIPE_SRCSZ		
		Restriction Restriction : This register must always be programmed to the same value as the Horizontal Active, except when panel fitting is enabled. Horizontal source sizes larger than 4096 pixels can not be used when Frame Buffer Compression or Panel Fitting are enabled.
	15:12	**Reserved** Format: MBZ
	11:0	**Vertical Source Size** This field specifies Vertical Source Size. This determines the vertical size of the image created by the display planes. This field is programmed to the number of lines desired minus one. **Restriction** Restriction : This register must always be programmed to the same value as the Vertical Active, except when panel fitting is enabled.

PIPE_VSYNCSHIFT

PIPE_VSYNCSHIFT	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	60028h-6002Bh
Name:	Pipe A Vertical Sync Shift
ShortName:	PIPE_VSYNCSHIFT_A
Power:	off/on
Reset:	soft
Address:	61028h-6102Bh
Name:	Pipe B Vertical Sync Shift
ShortName:	PIPE_VSYNCSHIFT_B
Power:	off/on
Reset:	soft
Address:	62028h-6202Bh
Name:	Pipe C Vertical Sync Shift
ShortName:	PIPE_VSYNCSHIFT_C
Power:	off/on
Reset:	soft
Address:	6F028h-6F02Bh
Name:	Pipe EDP Vertical Sync Shift
ShortName:	PIPE_VSYNCSHIFT_EDP
Power:	Always on
Reset:	soft

There is one instance of this register for each pipe A/B/C/EDP.

Restriction
Restriction : This register should not be changed while the pipe or port are enabled.

DWord	Bit	Description
0	31:13	**Reserved**
	12:0	**Second Field VSync Shift**

PIPE_VSYNCSHIFT		
		This value specifies the vertical sync alignment for the start of the interlaced second field, expressed in terms of the absolute pixel number relative to the horizontal active display start. This value will only be used if the transcoder is programmed to an interlaced mode. Typically, the interlaced second field vertical sync should start one pixel after the point halfway between successive horizontal syncs, so the value of this register should be programmed = horizontal sync start - floor[horizontal total / 2] Calculate using the actual horizontal sync start and horizontal total values and not the minus one values programmed into the registers. This vertical sync shift only occurs during the interlaced second field. In all other cases the vertical sync start position is aligned with horizontal sync start.

PIPE_MULT

PIPE_MULT	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6002Ch-6002Fh
Name:	Pipe A Multiply
ShortName:	PIPE_MULT_A
Power:	off/on
Reset:	soft
Address:	6102Ch-6102Fh
Name:	Pipe B Multiply
ShortName:	PIPE_MULT_B
Power:	off/on
Reset:	soft
Address:	6202Ch-6202Fh
Name:	Pipe C Multiply
ShortName:	PIPE_MULT_C
Power:	off/on
Reset:	soft
There is one instance of this register for each pipe A/B/C.	

Restriction
Restriction : This register should not be changed while the pipe or port are enabled.

DWord	Bit	Description
0	31:3	**Reserved**
	2:0	**Multiplier** This field specifies the data multiplier value used by HDMI and DVI.

Value	Name	Description
000b	X1	Multiply by 1
001b	X2	Multiply by 2
011b	X4	Multiply by 4

PIPE_MULT				
		Others	Reserved	Reserved

DATAM

DATAM	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Sending next MSA
Double Buffer Armed By:	Writing the LINKN
Address:	60030h-60033h
Name:	Pipe A Data M Value 1
ShortName:	PIPE_DATAM1_A
Power:	off/on
Reset:	soft
Address:	61030h-61033h
Name:	Pipe B Data M Value 1
ShortName:	PIPE_DATAM1_B
Power:	off/on
Reset:	soft
Address:	62030h-62033h
Name:	Pipe C Data M Value 1
ShortName:	PIPE_DATAM1_C
Power:	off/on
Reset:	soft
Address:	6F030h-6F033h
Name:	Pipe EDP Data M Value 1
ShortName:	PIPE_DATAM1_EDP
Power:	Always on
Reset:	soft
Address:	6F038h-6F03Bh
Name:	Pipe EDP Data M Value 2
ShortName:	PIPE_DATAM2_EDP

DATAM

Power: Always on

Reset: soft

There is one instance of this register for each pipe A/B/C.
There are two instances of this register for pipe EDP to support dynamic refresh rate switching.

DWord	Bit	Description
0	31	**Reserved** Format: MBZ
	30:25	**TU or VCpayload Size** In DisplayPort SST mode this field is the size of the transfer unit, minus one. Typically it is programmed with a value of 63 for TU size of 64. In DisplayPort MST mode this field is the Virtual Channel payload size, minus one. **Restriction** Restriction : In DisplayPort MST mode the Virtual Channel payload size must not be programmed greater than 62 (resulting payload size of 63). In DisplayPort MST mode the Virtual Channel payload size must not be changed while the Virtual Channel is enabled, even after a transcoder has been disabled.
	24	**Reserved** Format: MBZ
	23:0	**Data M value** This field is the data M value for internal use.

DATAN

DATAN	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Sending next MSA
Double Buffer Armed By:	Writing the LINKN
Address:	60034h-60037h
Name:	Pipe A Data N Value 1
ShortName:	PIPE_DATAN1_A
Power:	off/on
Reset:	soft
Address:	61034h-61037h
Name:	Pipe B Data N Value 1
ShortName:	PIPE_DATAN1_B
Power:	off/on
Reset:	soft
Address:	62034h-62037h
Name:	Pipe C Data N Value 1
ShortName:	PIPE_DATAN1_C
Power:	off/on
Reset:	soft
Address:	6F034h-6F037h
Name:	Pipe EDP Data N Value 1
ShortName:	PIPE_DATAN1_EDP
Power:	Always on
Reset:	soft
Address:	6F03Ch-6F03Fh
Name:	Pipe EDP Data N Value 2
ShortName:	PIPE_DATAN2_EDP

DATAN

Power: Always on

Reset: soft

There is one instance of this register for each pipe A/B/C.
There are two instances of this register for pipe EDP to support dynamic refresh rate switching.

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:0	**Data N value** This field is the data N value for internal use.

LINKM

LINKM	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Sending next MSA
Double Buffer Armed By:	Writing the LINKN
Address:	60040h-60043h
Name:	Pipe A Link M Value 1
ShortName:	PIPE_LINKM1_A
Power:	off/on
Reset:	soft
Address:	61040h-61043h
Name:	Pipe B Link M Value 1
ShortName:	PIPE_LINKM1_B
Power:	off/on
Reset:	soft
Address:	62040h-62043h
Name:	Pipe C Link M Value 1
ShortName:	PIPE_LINKM1_C
Power:	off/on
Reset:	soft
Address:	6F040h-6F043h
Name:	Pipe EDP Link M Value 1
ShortName:	PIPE_LINKM1_EDP
Power:	Always on
Reset:	soft
Address:	6F048h-6F04Bh
Name:	Pipe EDP Link M Value 2
ShortName:	PIPE_LINKM2_EDP

LINKM

Power: Always on

Reset: soft

There is one instance of this register for each pipe A/B/C.
There are two instances of this register for pipe EDP to support dynamic refresh rate switching.

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:0	**Link M value** This field is the link M value for external transmission in the Main Stream Attributes.

LINKN

LINKN	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Sending next MSA
Address:	60044h-60047h
Name:	Pipe A Link N Value 1
ShortName:	PIPE_LINKN1_A
Power:	off/on
Reset:	soft
Address:	61044h-61047h
Name:	Pipe B Link N Value 1
ShortName:	PIPE_LINKN1_B
Power:	off/on
Reset:	soft
Address:	62044h-62047h
Name:	Pipe C Link N Value 1
ShortName:	PIPE_LINKN1_C
Power:	off/on
Reset:	soft
Address:	6F044h-6F047h
Name:	Pipe EDP Link N Value 1
ShortName:	PIPE_LINKN1_EDP
Power:	Always on
Reset:	soft
Address:	6F04Ch-6F04Fh
Name:	Pipe EDP Link N Value 2
ShortName:	PIPE_LINKN2_EDP
Power:	Always on

LINKN

Reset: soft

There is one instance of this register for each pipe A/B/C.
There are two instances of this register for pipe EDP to support dynamic refresh rate switching.

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:0	**Link N value** This field is the link N value for external transmission in the Main Stream Attributes and VB-ID.

VIDEO_DIP_CTL

VIDEO_DIP_CTL	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	60200h-60203h
Name:	Pipe A Video Data Island Packet Control
ShortName:	VIDEO_DIP_CTL_A
Power:	off/on
Reset:	soft
Address:	61200h-61203h
Name:	Pipe B Video Data Island Packet Control
ShortName:	VIDEO_DIP_CTL_B
Power:	off/on
Reset:	soft
Address:	62200h-62203h
Name:	Pipe C Video Data Island Packet Control
ShortName:	VIDEO_DIP_CTL_C
Power:	off/on
Reset:	soft
Address:	6F200h-6F203h
Name:	Pipe EDP Video Data Island Packet Control
ShortName:	VIDEO_DIP_CTL_EDP
Valid Projects:	[DevHSW, EXCLUDE(DevHSW:GT0:X0)]
Power:	Always on
Reset:	soft
Each type of Video DIP will be sent once each frame while it is enabled.	

Restriction
Restriction : Pipe EDP going to DDI A supports only VSC DIP.

DWord	Bit	Description
0	31:21	**Reserved**

VIDEO_DIP_CTL

20	**VDIP Enable VSC** This bit enables the output of the Video Stream Configuration DIP. **Value** / **Name** 0b – Disable VSC DIP 1b – Enable VSC DIP **Restriction** Restriction : VSC can only be enabled with DisplayPort. Restriction : VSC should be enabled prior to enabling PSR.
19:17	**Reserved**
16	**VDIP Enable GCP** This bit enables the output of the General Control Packet (GCP) DIP. GCP is different from other DIPs in that much of the payload is automatically reflected in the packet, and therefore there is a VIDEO_DIP_GCP register instead of DIP data buffers for GCP. **Value** / **Name** 0b – Disable GCP DIP 1b – Enable GCP DIP **Restriction** GCP is only supported with HDMI 12 BPC mode. GCP must be enabled prior to enabling PIPE_DDI_FUNC_CTL for HDMI 12 BPC mode and disabled after disabling PIPE_DDI_FUNC_CTL.
15:13	**Reserved**
12	**VDIP Enable AVI** This bit enables the output of the Auxiliary Video Information DIP. **Value** / **Name** 0b – Disable AVI DIP 1b – Enable AVI DIP **Restriction** Restriction : Only enable with HDMI.
11:9	**Reserved**
8	**VDIP Enable VS** This bit enables the output of the Vendor Specific (VS) DIP. **Value** / **Name** 0b – Disable VS DIP 1b – Enable VS DIP

VIDEO_DIP_CTL

		Restriction Restriction : Only enable with HDMI.
	7:5	**Reserved**
	4	**VDIP Enable GMP** This bit enables the output of the Gamut Metadata Packet (GMP) DIP. GMP can be enabled with either DisplayPort or HDMI. **Value** / **Name** 0b – Disable GMP DIP 1b – Enable GMP DIP **Restriction** Restriction : GMP is not supported on transcoder EDP going to DDI A.
	3:1	**Reserved**
	0	**VDIP Enable SPD** This bit enables the output of the Source Product Description (SPD) DIP. **Value** / **Name** 0b – Disable SPD DIP 1b – Enable SPD DIP **Restriction** Restriction : Only enable with HDMI.

VIDEO_DIP_GCP

VIDEO_DIP_GCP

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	60210h-60213h
Name:	Pipe A Video Data Island Packet GCP
ShortName:	VIDEO_DIP_GCP_A
Power:	off/on
Reset:	soft
Address:	61210h-61213h
Name:	Pipe B Video Data Island Packet GCP
ShortName:	VIDEO_DIP_GCP_B
Power:	off/on
Reset:	soft
Address:	62210h-62213h
Name:	Pipe C Video Data Island Packet GCP
ShortName:	VIDEO_DIP_GCP_C
Power:	off/on
Reset:	soft

DWord	Bit	Description
0	31:3	**Reserved** Format: MBZ
	2	**GCP color indication** 0b – Don't Indicate – Don't indicate color depth. CD and PP bits in GCP set to zero. 1b – Indicate – Indicate color depth using CD bits in GCP. The color depth value comes from the PIPE_DDI_FUNC_CTL register. **Restriction** Restriction : This bit must be set when in HDMI deep color (12 BPC) mode.

VIDEO_DIP_GCP

	1	**GCP default phase enable** GCP default phase indicates that video timings meet alignment requirements such that the following conditions are met: 1. Htotal is an even number 2. Hactive is an even number 3. Front and back porches for Hsync are even numbers 4. Vsync always starts on an even-numbered pixel within a line in interlaced modes (starting counting with 0)

Value	Name	Description
0b	Clear	Default phase bit in GCP is cleared.
1b	Set	Default phase bit in GCP is set.

Restriction
Restriction : Do not set this bit if these requirements are not met.

	0	**Reserved**

VIDEO_DIP_DATA

VIDEO_DIP_DATA	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	60220h-6023Fh
Name:	Pipe A Video Data Island Packet AVI Data
ShortName:	VIDEO_DIP_AVI_DATA_A_*
Power:	off/on
Reset:	soft
Address:	60260h-6027Fh
Name:	Pipe A Video Data Island Packet VS Data
ShortName:	VIDEO_DIP_VS_DATA_A_*
Power:	off/on
Reset:	soft
Address:	602A0h-602BFh
Name:	Pipe A Video Data Island Packet SPD Data
ShortName:	VIDEO_DIP_SPD_DATA_A_*
Power:	off/on
Reset:	soft
Address:	602E0h-602FFh
Name:	Pipe A Video Data Island Packet GMP Data
ShortName:	VIDEO_DIP_GMP_DATA_A_*
Power:	off/on
Reset:	soft
Address:	60320h-60343h
Name:	Pipe A Video Data Island Packet VSC Data
ShortName:	VIDEO_DIP_VSC_DATA_A_*
Power:	off/on
Reset:	soft
Address:	61220h-6123Fh

VIDEO_DIP_DATA	
Name:	Pipe B Video Data Island Packet AVI Data
ShortName:	VIDEO_DIP_AVI_DATA_B_*
Power:	off/on
Reset:	soft
Address:	61260h-6127Fh
Name:	Pipe B Video Data Island Packet VS Data
ShortName:	VIDEO_DIP_VS_DATA_B_*
Power:	off/on
Reset:	soft
Address:	612A0h-612BFh
Name:	Pipe B Video Data Island Packet SPD Data
ShortName:	VIDEO_DIP_SPD_DATA_B_*
Power:	off/on
Reset:	soft
Address:	612E0h-612FFh
Name:	Pipe B Video Data Island Packet GMP Data
ShortName:	VIDEO_DIP_GMP_DATA_B_*
Power:	off/on
Reset:	soft
Address:	61320h-61343h
Name:	Pipe B Video Data Island Packet VSC Data
ShortName:	VIDEO_DIP_VSC_DATA_B_*
Power:	off/on
Reset:	soft
Address:	62220h-6223Fh
Name:	Pipe C Video Data Island Packet AVI Data
ShortName:	VIDEO_DIP_AVI_DATA_C_*
Power:	off/on
Reset:	soft
Address:	62260h-6227Fh
Name:	Pipe C Video Data Island Packet VS Data
ShortName:	VIDEO_DIP_VS_DATA_C_*
Power:	off/on
Reset:	soft
Address:	622A0h-622BFh

VIDEO_DIP_DATA

Name:	Pipe C Video Data Island Packet SPD Data
ShortName:	VIDEO_DIP_SPD_DATA_C_*
Power:	off/on
Reset:	soft
Address:	622E0h-622FFh
Name:	Pipe C Video Data Island Packet GMP Data
ShortName:	VIDEO_DIP_GMP_DATA_C_*
Power:	off/on
Reset:	soft
Address:	62320h-62343h
Name:	Pipe C Video Data Island Packet VSC Data
ShortName:	VIDEO_DIP_VSC_DATA_C_*
Power:	off/on
Reset:	soft
Address:	6F320h-6F343h
Name:	Pipe EDP Video Data Island Packet VSC Data
ShortName:	VIDEO_DIP_VSC_DATA_EDP_*
Valid Projects:	[DevHSW, EXCLUDE(DevHSW:GT0:X0)]
Power:	Always on
Reset:	soft

There are multiple instances of this register format per DIP type and per pipe.

DWord	Bit	Description
0	31:0	**Video DIP DATA** This field contains the video DIP data to be transmitted. **Restriction** Restriction : Data should be loaded before enabling the transmission through the DIP type enable bit.

VIDEO_DIP_ECC

VIDEO_DIP_ECC	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	60240h-60247h
Name:	Pipe A Video Data Island Packet AVI ECC
ShortName:	VIDEO_DIP_AVI_ECC_A_*
Power:	off/on
Reset:	soft
Address:	60280h-60287h
Name:	Pipe A Video Data Island Packet VS ECC
ShortName:	VIDEO_DIP_VS_ECC_A_*
Power:	off/on
Reset:	soft
Address:	602C0h-602C7h
Name:	Pipe A Video Data Island Packet SPD ECC
ShortName:	VIDEO_DIP_SPD_ECC_A_*
Power:	off/on
Reset:	soft
Address:	60300h-60313h
Name:	Pipe A Video Data Island Packet GMP ECC
ShortName:	VIDEO_DIP_GMP_ECC_A_*
Power:	off/on
Reset:	soft
Address:	60344h-6034Fh
Name:	Pipe A Video Data Island Packet VSC ECC
ShortName:	VIDEO_DIP_VSC_ECC_A_*
Power:	off/on
Reset:	soft
Address:	61240h-61247h

VIDEO_DIP_ECC	
Name:	Pipe B Video Data Island Packet AVI ECC
ShortName:	VIDEO_DIP_AVI_ECC_B_*
Power:	off/on
Reset:	soft
Address:	61280h-61287h
Name:	Pipe B Video Data Island Packet VS ECC
ShortName:	VIDEO_DIP_VS_ECC_B_*
Power:	off/on
Reset:	soft
Address:	612C0h-612C7h
Name:	Pipe B Video Data Island Packet SPD ECC
ShortName:	VIDEO_DIP_SPD_ECC_B_*
Power:	off/on
Reset:	soft
Address:	61300h-61313h
Name:	Pipe B Video Data Island Packet GMP ECC
ShortName:	VIDEO_DIP_GMP_ECC_B_*
Power:	off/on
Reset:	soft
Address:	61344h-6134Fh
Name:	Pipe B Video Data Island Packet VSC ECC
ShortName:	VIDEO_DIP_VSC_ECC_B_*
Power:	off/on
Reset:	soft
Address:	62240h-62247h
Name:	Pipe C Video Data Island Packet AVI ECC
ShortName:	VIDEO_DIP_AVI_ECC_C_*
Power:	off/on
Reset:	soft
Address:	62280h-62287h
Name:	Pipe C Video Data Island Packet VS ECC
ShortName:	VIDEO_DIP_VS_ECC_C_*
Power:	off/on
Reset:	soft
Address:	622C0h-622C7h

VIDEO_DIP_ECC

Name:	Pipe C Video Data Island Packet SPD ECC
ShortName:	VIDEO_DIP_SPD_ECC_C_*
Power:	off/on
Reset:	soft
Address:	62300h-62313h
Name:	Pipe C Video Data Island Packet GMP ECC
ShortName:	VIDEO_DIP_GMP_ECC_C_*
Power:	off/on
Reset:	soft
Address:	62344h-6234Fh
Name:	Pipe C Video Data Island Packet VSC ECC
ShortName:	VIDEO_DIP_VSC_ECC_C_*
Power:	off/on
Reset:	soft
Address:	6F344h-6F34Fh
Name:	Pipe EDP Video Data Island Packet VSC ECC
ShortName:	VIDEO_DIP_VSC_ECC_EDP_*
Valid Projects:	[DevHSW, EXCLUDE(DevHSW:GT0:X0)]
Power:	Always on
Reset:	soft

There are multiple instances of this register format per DIP type and per pipe.

DWord	Bit	Description
0	31:0	**Video DIP ECC** This field contains the video DIP ECC value for read back.

PIPE_DDI_FUNC_CTL

PIPE_DDI_FUNC_CTL	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00030000 [HSW]
Access:	R/W
Size (in bits):	32
Address:	60400h-60403h
Name:	Pipe A DDI Function Control
ShortName:	PIPE_DDI_FUNC_CTL_A
Power:	off/on
Reset:	soft
Address:	61400h-61403h
Name:	Pipe B DDI Function Control
ShortName:	PIPE_DDI_FUNC_CTL_B
Power:	off/on
Reset:	soft
Address:	62400h-62403h
Name:	Pipe C DDI Function Control
ShortName:	PIPE_DDI_FUNC_CTL_C
Power:	off/on
Reset:	soft
Address:	6F400h-6F403h
Name:	Pipe EDP DDI Function Control
ShortName:	PIPE_DDI_FUNC_CTL_EDP
Power:	Always on
Reset:	soft

There is one Pipe DDI Function Control per each pipe A/B/C/EDP.

DWord	Bit	Description
0	31	**Pipe DDI Function Enable** This bit enables the pipe DDI function.

Value	Name
0b	Disable

PIPE_DDI_FUNC_CTL

1b	Enable

30:28 **DDI Select**

These bits determine which DDI port this pipe will connect to.
It is not valid to enable and direct more than one pipe to one DDI, except when using DisplayPort multistreaming.
These bits are ignored by pipe EDP since it can only connect to DDI A (EDP DDI).

Value	Name	Description	Project
000b	None	No port connected	
001b	DDI B	DDI B	
010b	DDI C	DDI C	
011b	DDI D	DDI D	HSW
011b	Reserved	Reserved. DDI D is not supported for ULT and must not be selected.	DevHSW:ULT
100b	DDI E	DDI E	
Others	Reserved	Reserved	

Restriction
Restriction : This field must not be changed while the function is enabled.

27 **Reserved**

Format:	MBZ

26:24 **Pipe DDI Mode Select**

This field determines the mode of operation.
HDMI mode enables a null packet (32 bytes of a value of 0) to be sent when Vsync=1, and also enables preambles and guardbands prior to the null packets, in accordance with the HDMI specification.
DVI mode will function as HDMI if DIP packets or audio are enabled.

Value	Name	Description	Project
000b	HDMI	Function in HDMI mode	
001b	DVI	Function in DVI mode	
010b	DP SST	Function in DisplayPort SST mode	
011b	DP MST	Function in DisplayPort MST mode	DevHSW, EXCLUDE(DevHSW:GT0:X0)
100b	FDI	Function in FDI mode	
Others	Reserved	Reserved	

Restriction
Restriction : This field must not be changed while the function is enabled. The DisplayPort mode (SST or MST) selected here must match the mode selected in the DisplayPort Transport Control register for the transport attached to this pipe. Only DDI E is allowed to operate in FDI mode.

PIPE_DDI_FUNC_CTL

	Pipe EDP and DDI A can only function in DP SST mode. DDI E can only function in DP SST mode or FDI mode.
23	**Reserved** Format: MBZ
22:20	**Bits Per Color** This field selects the number of bits per color output on the DDI connected to this transcoder. Dithering should be enabled when selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer.

Value	Name	Description
000b	8 bpc	8 bits per color
001b	10 bpc	10 bits per color (not supported by HDMI or DVI)
010b	6 bpc	6 bits per color (not supported by HDMI or DVI)
011b	12 bpc	12 bits per color
Others	Reserved	Reserved

Restriction
Restriction : This field must not be changed while the function is enabled. 10 bpc and 6 bpc are not supported by HDMI or DVI.

19:18	**Reserved** Format: MBZ
17:16	**Sync Polarity** Indicates the polarity of Hsync and Vsync.

Value	Name	Description
00b	Low	VS and HS are active low (inverted)
01b	VS Low, HS High	VS is active low (inverted), HS is active high
10b	VS High, HS Low	VS is active high, HS is active low (inverted)
11b	High **[Default]**	VS and HS are active high

15	**Reserved** Format: MBZ
14:12	**EDP Input Select** These bits determine the input to pipe EDP. The always on input is from planes A (primary/sprite/cursor A) immediately after color correction (gamma, CSC, CGE) and before MBM and panel fitting. The always on input can be used in the low power mode when the power well is powered down. The on/off inputs are from planes A/B/C immediately after MBM and panel fitting. These bits are ignored by pipes A/B/C.

PIPE_DDI_FUNC_CTL

Value	Name	Description
000b	A - Always On	Planes A through the always on power well. Cannot use MBM or panel fitting.
100b	A - On/Off	Planes A or VGA through the on/off power well.
101b	B - On/Off	Planes B through the on/off power well.
110b	C - On/Off	Planes C through the on/off power well.
Others	Reserved	Reserved

Note:
Note: When the EDP input selection is B, the PIPE_VTOTAL_B must be programmed with the PIPE_VTOTAL_EDP value. When the EDP input selection is C, the PIPE_VTOTAL_C must be programmed with the PIPE_VTOTAL_EDP value.

Restriction
Restriction : The on/off inputs can only be used when the power well is powered up. This field must not be changed while the function is enabled. It is not valid to have the same planes driving multiple enabled pipes. MBM and panel fitting cannot be used when using the Always On path.

11 **Reserved**

Project:	DevHSW, EXCLUDE(DevHSW:GT0:X0)
Format:	MBZ

11 **Reserved**

Project:	DevHSW:GT0:X0

10 **Reserved**

Format:	MBZ

9 **Reserved**

8 **DP VC Payload Allocate**

This bit enables DisplayPort Virtual Channel payload allocation.
This bit is ignored by pipe EDP since it does not support multistreaming.

Value	Name
0b	Disable
1b	Enable

7:6 **Reserved**

Format:	MBZ

5 **Reserved**

4 **BFI enable**

This bit enables black frame insertion on this pipe.

PIPE_DDI_FUNC_CTL

Value	Name
0b	Disable
1b	Enable

3:1 **DP Port Width Selection**

This bit selects the number of lanes to be enabled on the DDI link for DisplayPort or FDI.
This field is ignored for HDMI and DVI which always use all 4 lanes.

Value	Name	Description
000b	x1	x1 Mode
001b	x2	x2 Mode
011b	x4	x4 Mode (not allowed with DDI-E, some restrictions with DDI-A)
Others	Reserved	Reserved

Restriction	Project
Restriction : When in DisplayPort or FDI modes the value selected here must match the value selected in the DDI Buffer Control register for the DDI attached to this pipe. This field must not be changed while the DDI is enabled.	
Restriction : DDI E is not supported. DDI A (EDP) only supports x1 and x2.	DevHSW:GT0:X0
Restriction : DDI E only supports x1 and and x2 when DDI_BUF_CTL_A DDIA Lane Capability Control is set to DDIA x2, otherwise DDI E is not supported. DDI A (EDP) supports x1, x2, and x4 when DDI_BUF_CTL_A DDIA Lane Capability Control is set to DDIA x4, otherwise DDI A only supports x1 and x2.	DevHSW, EXCLUDE(DevHSW:GT0:X0)

0 **Reserved**

Format:	MBZ

PIPE_MSA_MISC

PIPE_MSA_MISC	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank
Address:	60410h-60413h
Name:	Pipe A MSA Misc
ShortName:	PIPE_MSA_MISC_A
Power:	off/on
Reset:	soft
Address:	61410h-61413h
Name:	Pipe B MSA Misc
ShortName:	PIPE_MSA_MISC_B
Power:	off/on
Reset:	soft
Address:	62410h-62413h
Name:	Pipe C MSA Misc
ShortName:	PIPE_MSA_MISC_C
Power:	off/on
Reset:	soft
Address:	6F410h-6F413h
Name:	Pipe EDP MSA Misc
ShortName:	PIPE_MSA_MISC_EDP
Power:	Always on
Reset:	soft
There is one instance of this register per each transcoder A/B/C/EDP. This register selects what value will be sent in the DisplayPort Main Stream Attribute (MSA) Miscellaneous (MISC) fields. The MSA MISC fields are mostly used to indicate the color encoding format and need to be programmed to indicate color space, bits per color, etc.	

PIPE_MSA_MISC

Programming Notes

See the DisplayPort specification for the details on what to program in these fields.

DWord	Bit	Description
0	31:16	**MSA Unused** This field selects the value that will be sent in the DisplayPort MSA unused fields. **Programming Notes** This should be usually programmed with all 0s.
	15:8	**MSA MISC1** This field selects the value that will be sent in the DisplayPort MSA MISC1 field.
	7:0	**MSA MISC0** This field selects the value that will be sent in the DisplayPort MSA MISC0 field. **Restriction** Restriction : Before enabling DisplayPort, bit 0 should always be set to 1 to indicate link clock and stream clock are synchronous.

PIPE_MSA_MISC

PIPE_MSA_MISC	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank
Address:	60410h-60413h
Name:	Pipe A MSA Misc
ShortName:	PIPE_MSA_MISC_A
Power:	off/on
Reset:	soft
Address:	61410h-61413h
Name:	Pipe B MSA Misc
ShortName:	PIPE_MSA_MISC_B
Power:	off/on
Reset:	soft
Address:	62410h-62413h
Name:	Pipe C MSA Misc
ShortName:	PIPE_MSA_MISC_C
Power:	off/on
Reset:	soft
Address:	6F410h-6F413h
Name:	Pipe EDP MSA Misc
ShortName:	PIPE_MSA_MISC_EDP
Power:	Always on
Reset:	soft
There is one instance of this register per each transcoder A/B/C/EDP. This register selects what value will be sent in the DisplayPort Main Stream Attribute (MSA) Miscellaneous (MISC) fields. The MSA MISC fields are mostly used to indicate the color encoding format and need to be programmed to indicate color space, bits per color, etc.	

PIPE_MSA_MISC

Programming Notes

See the DisplayPort specification for the details on what to program in these fields.

DWord	Bit	Description
0	31:16	**MSA Unused** This field selects the value that will be sent in the DisplayPort MSA unused fields. **Programming Notes** This should be usually programmed with all 0s.
	15:8	**MSA MISC1** This field selects the value that will be sent in the DisplayPort MSA MISC1 field.
	7:0	**MSA MISC0** This field selects the value that will be sent in the DisplayPort MSA MISC0 field. **Restriction** Restriction : Before enabling DisplayPort, bit 0 should always be set to 1 to indicate link clock and stream clock are synchronous.

DDI_BUF_CTL

DDI_BUF_CTL	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000 [HSW]
Access:	R/W
Size (in bits):	32
Address:	64000h-64003h
Name:	DDI A Buffer Control
ShortName:	DDI_BUF_CTL_A
Power:	Always on
Reset:	soft
Address:	64100h-64103h
Name:	DDI B Buffer Control
ShortName:	DDI_BUF_CTL_B
Power:	Always on
Reset:	soft
Address:	64200h-64203h
Name:	DDI C Buffer Control
ShortName:	DDI_BUF_CTL_C
Power:	Always on
Reset:	soft
Address:	64300h-64303h
Name:	DDI D Buffer Control
ShortName:	DDI_BUF_CTL_D
Power:	Always on
Reset:	soft
Address:	64400h-64403h
Name:	DDI E Buffer Control
ShortName:	DDI_BUF_CTL_E
Valid Projects:	[DevHSW, EXCLUDE(DevHSW:GT0:X0)]
Power:	Always on
Reset:	soft

DDI_BUF_CTL

There is one DDI Buffer Control per each DDI A/B/C/D/E.

DWord	Bit	Description
0	31	**DDI Buffer Enable** This bit enables the DDI buffer. Value: 0b = Disable; 1b = Enable
	30:28	**Reserved** Format: MBZ
	27:24	**DP Vswing Emp Sel** These bits are used to select the voltage swing and emphasis for DisplayPort and FDI. This field is ignored for HDMI and DVI. The values programmed in DDI_BUF_TRANS determine the voltage swing and emphasis for each selection. Value: 0000b-1000b; Name: Select 0 - Select 8; Description: Select from buffer translations 0 through 8. Valid with all DDIs. Restriction : Correct values must be programmed in DDI Buffer Translation registers before enabling the DDI. (Project:) Restriction : Only the 0dB selections can be used for DDI C. (Project: DevHSW:GT0:X0)
	23:17	**Reserved** Format: MBZ
	16	**Port Reversal** This field enables lane reversal within the port. Lane reversal swaps the data on the lanes as they are output from the port. Value: 0b = Not reversed; 1b = Reversed **Programming Notes** DDI B, C, and D reversal always swaps the four lanes, so lane 0 is swapped with lane 3, and lane 1 is swapped with lane 2. If DDIA Lane Capability Control selects DDIA x2, then DDI A reversal swaps the two lanes, so lane 0 is swapped with lane 1. If DDIA Lane Capability Control selects DDIA x4, then DDI A reversal swaps the four lanes, so lane 0 is swapped with lane 3, and lane 1 is swapped with lane 2.

DDI_BUF_CTL

Restriction	Project
Restriction : This field must not be changed while the DDI is enabled. DDI E does not support reversal.	
Restriction : Reversal is not supported.	DevHSW:GT0:X0

15:8 **Reserved**

Format:	MBZ

7 **Reserved**

Project:	DevHSW:GT0:X0
Format:	MBZ

7 **DDI Idle Status**

Project:	DevHSW, EXCLUDE(DevHSW:GT0:X0)
Access:	RO

This bit indicates when the DDI buffer is idle.

Value	Name
0b	Buffer Not Idle
1b	Buffer Idle

6:5 **Reserved**

Format:	MBZ

4 **Reserved**

Project:	DevHSW:GT0:X0
Format:	MBZ

4 **DDIA Lane Capability Control**

Project:	DevHSW, EXCLUDE(DevHSW:GT0:X0)

This bit selects how lanes are shared between DDI A and DDI E.
This field is only used in the DDI A instance of this register.
See the DDI A and DDI E lane mapping table in the Introduction section.

Value	Name	Description
0b	DDIA x2	DDI A supports 2 lanes and DDI E supports 2 lanes
1b	DDIA x4	DDI A supports 4 lanes and DDI E is not used

Restriction
Restriction : This field must be programmed at system boot based on board configuration and may not be changed afterwards.

3:1 **DP Port Width Selection**

This bit selects the number of lanes to be enabled on the DDI link for DisplayPort or FDI.
This field is ignored for HDMI and DVI which always use all 4 lanes.

Value	Name	Description

000b	x1	x1 Mode
001b	x2	x2 Mode
011b	x4	x4 Mode (not allowed with DDI E, some restrictions with DDI A)
Others	Reserved	Reserved

Restriction	Project
Restriction : When in DisplayPort or FDI modes the value selected here must match the value selected in the Pipe DDI Function Control registers for the pipes attached to this DDI. This field must not be changed while the DDI is enabled.	
Restriction : DDI E is not supported. DDI A (EDP) only supports x1 and x2.	DevHSW:GT0:X0
Restriction : DDI E only supports x1 and and x2 when DDI_BUF_CTL_A DDIA Lane Capability Control is set to DDIA x2, otherwise DDI E is not supported. DDI A (EDP) supports x1, x2, and x4 when DDI_BUF_CTL_A DDIA Lane Capability Control is set to DDIA x4, otherwise DDI A only supports x1 and x2.	DevHSW, EXCLUDE(DevHSW:GT0:X0)

0

Init Display Detected

Access:	RO

Strap indicating whether a display was detected on this port during initialization.
It signifies the level of the port detect pin at boot.
This bit is only informative. It does not prevent this port from being enabled in hardware.
This field only indicates the DDIA detection.
DDIB detection is read from SFUSE_STRAP 0xC2014 bit 2.
DDIC detection is read from SFUSE_STRAP 0xC2014 bit 1.
DDID detection is read from SFUSE_STRAP 0xC2014 bit 0.

Value	Name	Description
0b	Not Detected	Digital display not detected during initialization
1b	Detected	Digital display detected during initialization

DDI_AUX_CTL

DDI_AUX_CTL

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x000300E1
Access:	R/W
Size (in bits):	32
Address:	64010h-64013h
Name:	DDI A AUX Channel Control
ShortName:	DDI_AUX_CTL_A
Power:	Always on
Reset:	soft

Restriction

Restriction : DDI A AUX channel transactions must not be sent while SRD is enabled. SRD must be completely disabled before a DDI A AUX channel transaction can be sent.

DWord	Bit	Description
0	31	**Send Busy** Access: R/W Set Writing this bit with 1b initiates the transaction, when read this bit will be a 1b until the transmission completes. The transaction is completed when the response is received or when a timeout occurs. This is a sticky bit. Write a 1b to this bit to set it and initiate the transaction. Hardware will clear it when the transaction completes. **Restriction** Restriction : Do not change any fields while Send Busy is asserted. Do not write a 1b again until transaction completes.
	30	**Done** Access: R/WC A sticky bit that indicates the transaction has completed. Write a 1 to this bit to clear the event Value: 0b — Name: Not done Value: 1b — Name: Done
	29	**Interrupt on Done**

DDI_AUX_CTL

	Access:	R/W

Enable an interrupt when the transaction completes or times out.

Value	Name
0b	Enable
1b	Disable

28 Time out error

Access:	R/WC

A sticky bit that indicates the transaction has timed out.
Write a 1 to this bit to clear the event.

Value	Name
0b	Not error
1b	Error

27:26 Time out timer value

Access:	R/W

Used to determine how long to wait for receiver response before timing out.

Value	Name
00b	400us
01b	600us
10b	800us
11b	1600us

25 Receive error

Access:	R/WC

A sticky bit that indicates that the data received was corrupted, not in multiples of a full byte, or more than 20 bytes.
Write a 1 to this bit to clear the event.

Value	Name
0b	Not Error
1b	Error

24:20 Message Size

Access:	Write/Read Status

The value written to this field indicates the total number bytes to transmit (including the header).
The value read from this field indicates the number of bytes received, including the header, in the last transaction transaction.
Sync/Stop are not part of the message or the message size.
Reads of this field will give the response message size.
The read value will not be valid while Send/Busy bit 31 is asserted.

Restriction

		Restriction : Message sizes of 0 or >20 are not allowed. Reads and writes are valid only when the done bit is set and timeout or receive error has not occurred.
	19:16	**Precharge Time** Default Value: 0011b 6us Access: R/W Used to determine the precharge time for the Aux Channel. During this time the Aux Channel will drive the SYNC pattern. Every microsecond gives one additional SYNC pulse beyond the hard coded 26 SYNC pulses. The value is the number of microseconds times 2. Default is 3 decimal which gives 6us of precharge which is 6 extra SYNC pulses for a total of 32.
	15	**Reserved**
	14:11	**Reserved**
	10:0	**2X Bit Clock divider** Default Value: 00 1110 0001b 225 This field is used to determine the 2X bit clock the Aux Channel logic runs on. This value divides the input clock frequency down to 2X bit clock rate. It should be programmed to get as close as possible to the ideal rate of 2MHz. The input clock is the cdclk. Default is 225 decimal which divides the default 450 MHz cdclk input clock to become 2MHz bit clock. **Restriction** Restriction : The default value only works with cdclk 450 MHz. It must be programmed if the CD clock frequency is changed.

DDI_AUX_DATA

DDI_AUX_DATA	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	Write/Read Status
Size (in bits):	32
Address:	64014h-64027h
Name:	DDI A AUX Channel Data
ShortName:	DDI_AUX_DATA_A_*
Power:	Always on
Reset:	soft

There are 5 instances of this register format per AUX channel.

DWord	Bit	Description
0	31:0	**AUX CH DATA** This field contains a DWord of the AUX message. Writes to this register give the data to transmit during the transaction. The MSbyte is transmitted first. Reads to this register will give the response data after transaction complete. The read value will not be valid while the Aux Channel Control Register Send/Busy bit is asserted.

DP_TP_CTL

DP_TP_CTL	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	64040h-64043h
Name:	DDI A DisplayPort Transport Control
ShortName:	DP_TP_CTL_A
Power:	Always on
Reset:	soft
Address:	64140h-64143h
Name:	DDI B DisplayPort Transport Control
ShortName:	DP_TP_CTL_B
Power:	off/on
Reset:	soft
Address:	64240h-64243h
Name:	DDI C DisplayPort Transport Control
ShortName:	DP_TP_CTL_C
Power:	off/on
Reset:	soft
Address:	64340h-64343h
Name:	DDI D DisplayPort Transport Control
ShortName:	DP_TP_CTL_D
Power:	off/on
Reset:	soft
Address:	64440h-64443h
Name:	DDI E DisplayPort Transport Control
ShortName:	DP_TP_CTL_E
Valid Projects:	[DevHSW, EXCLUDE(DevHSW:GT0:X0)]
Power:	off/on
Reset:	soft

DP_TP_CTL

DWord	Bit	Description
0	31	**Transport Enable** This bit enables the DisplayPort transport function. Value: 0b = Disable; 1b = Enable
	30:28	**Reserved** Format: MBZ
	27	**Transport Mode Select** This bit selects between DisplayPort SST and MST modes of operation. This bit is ignored by DDI A (EDP) and DDI E since they do not support multistreaming. Value: 0b = SST mode (DisplayPort SST mode); 1b = MST mode (DisplayPort MST mode) Restriction : The DisplayPort mode (SST or MST) selected here must match the mode selected in the Pipe DDI Function Control registers for the pipes attached to this transport. FDI does not support MST mode. This field must not be changed while the DDI function is enabled.
	26	**Reserved** Format: MBZ
	25	**Force ACT** This bit forces DisplayPort MST ACT to be sent one time at the next link frame boundary. After ACT is sent, as indicated in the ACT sent status bit, this bit can be cleared and set again to send ACT again. This bit is ignored by DDI A (EDP) and DDI E since they do not support multistreaming. Value: 0b = Do not force (Do not force ACT to be sent); 1b = Force (Force ACT to be sent one time)
	24:19	**Reserved** Format: MBZ
	18	**Enhanced Framing Enable** This bit selects enhanced framing for DisplayPort SST or FDI. Hardware internally enables enhanced framing for DisplayPort MST. Value: 0b = Disabled

DP_TP_CTL

1b	Enabled

Restriction

Restriction : In DisplayPort MST mode this bit must be set to Disabled.
This field must not be changed while the DDI function is enabled.

17:16 Reserved

Format:	MBZ

15 FDI Auto Train Enable

This bit enables FDI auto-training on this port.

Value	Name
0b	Disable
1b	Enable

Programming Notes

See the mode set enable sequence for usage.

Restriction

Restriction : Do not change this bit while the port is enabled.
This bit must not be set when the DDI Function is not in FDI mode.

14:11 Reserved

Format:	MBZ

10:8 DP Link Training Enable

These bits are used for DisplayPort link initialization as defined in the DisplayPort specification. DP_TP_STATUS has an indication that the required number of idle patterns has been sent.

Value	Name	Description
000b	Pattern 1	Training Pattern 1 enabled
001b	Pattern 2	Training Pattern 2 enabled
010b	Idle	Idle Pattern enabled
011b	Normal	Link not in training: Send normal pixels
100b	Pattern 3	Training Pattern 3 enabled
Others	Reserved	Reserved

Restriction

Restriction : When enabling the port, it must be turned on with pattern 1 enabled.
When retraining a link, the port must be disabled, then re-enabled with pattern 1 enabled.

7 Reserved

6 Alternate SR Enable

This bit enables the DisplayPort Alternate Scrambler Reset, intended for use only with embedded

DP_TP_CTL

DisplayPort receivers.

Value	Name
0b	Disable
1b	Enable

Restriction
Restriction : This field must not be changed while the DDI function is enabled.

5:0 **Reserved**

Format:	MBZ

DP_TP_STATUS

DP_TP_STATUS	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	64144h-64147h
Name:	DDI B DisplayPort Transport Status
ShortName:	DP_TP_STATUS_B
Power:	off/on
Reset:	soft
Address:	64244h-64247h
Name:	DDI C DisplayPort Transport Status
ShortName:	DP_TP_STATUS_C
Power:	off/on
Reset:	soft
Address:	64344h-64347h
Name:	DDI D DisplayPort Transport Status
ShortName:	DP_TP_STATUS_D
Power:	off/on
Reset:	soft
Address:	64444h-64447h
Name:	DDI E DisplayPort Transport Status
ShortName:	DP_TP_STATUS_E
Valid Projects:	[DevHSW, EXCLUDE(DevHSW:GT0:X0)]
Power:	off/on
Reset:	soft

There is one DisplayPort Transport Status register per each DDI B/C/D/E. DDI A does not have a status register.

DWord	Bit	Description	
0	31:28	**Reserved**	
		Format:	MBZ
	27	**Idle Link Frame Status**	

DP_TP_STATUS

	Access:	R/WC

This bit indicates if a link frame boundary has been sent in idle pattern.
This is a sticky bit, cleared by writing 1b to it.

Value	Name
0b	Idle link frame not sent
1b	Idle link frame sent

26 Active Link Frame Status

Access:	R/WC

This bit indicates if a link frame boundary has been sent in active (at least one VC enabled).
This is a sticky bit, cleared by writing 1b to it.

Value	Name
0b	Active link frame not sent
1b	Active link frame sent

25 Min Idles Sent

Access:	RO

This bit indicates that the minimum required number of idle patterns has been sent when DP_TP_CTL is set to send idle patterns.
This bit will clear itself when DP_TP_CTL is not longer set to send idle patterns.

Value	Name
0b	Min idles not sent
1b	Min idles sent

24 ACT Sent Status

Access:	R/WC

This bit indicates if DisplayPort MST ACT has been sent.
This is a sticky bit, cleared by writing 1b to it.

Value	Name
0b	ACT not sent
1b	ACT sent

23 Mode Status

Access:	RO

This bit indicates what mode the transport is currently in.

Value	Name	Description
0b	SST	Single-stream mode
1b	MST	Multi-stream mode

22:18 Reserved

Format:	MBZ

17:16 Streams Enabled

DP_TP_STATUS

	Access:	RO

This field indicates the number of streams (pipes, transcoders, ddi slices) enabled on this port during multistream operation.
This field should be ignored in single stream mode.

Value	Name	Description
00b	Zero	Zero streams enabled
01b	One	One stream enabled
10b	Two	Two streams enabled
11b	Three	Three streams enabled

15:13 Reserved

Format:	MBZ

12 FDI Auto Train Done

Access:	RO

This bit indicates when FDI auto-training completes on this port.

Value	Name	Description
0b	Not Done	Auto-training is not complete or not started
1b	Done	Auto-training is complete

11:10 Reserved

Format:	MBZ

9:8 Payload Mapping VC2

Access:	RO

This field indicates which pipe (transcoder,ddi slice) is mapped to Virtual Channel 2 during multistream operation.
This field should be ignored if the number of streams enabled is less than three.
This field should be ignored in single stream mode.

Value	Name	Description
00b	A	Pipe A mapped to this VC
01b	B	Pipe B mapped to this VC
10b	C	Pipe C mapped to this VC
11b	Reserved	Reserved

7:6 Reserved

Format:	MBZ

5:4 Payload Mapping VC1

Access:	RO

This field indicates which pipe (transcoder,ddi slice) is mapped to Virtual Channel 1 during multistream operation.
This field should be ignored if the number of streams enabled is less than two.

DP_TP_STATUS

This field should be ignored in single stream mode.

Value	Name	Description
00b	A	Pipe A mapped to this VC
01b	B	Pipe B mapped to this VC
10b	C	Pipe C mapped to this VC
11b	Reserved	Reserved

3:2 **Reserved**

Format:	MBZ

1:0 **Payload Mapping VC0**

Access:	RO

This field indicates which pipe (transcoder,ddi slice) is mapped to Virtual Channel 0 during multistream operation.
This field should be ignored if the number of streams enabled is less than one.
This field should be ignored in single stream mode.

Value	Name	Description
00b	A	Pipe A mapped to this VC
01b	B	Pipe B mapped to this VC
10b	C	Pipe C mapped to this VC
11b	Reserved	Reserved

SRD_CTL

SRD_CTL	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00100001
Access:	R/W
Size (in bits):	32
Address:	64800h-64803h
Name:	SRD Control
ShortName:	SRD_CTL
Power:	Always on
Reset:	soft

SRD is tied to DDI A (EDP). SRD is also known as Panel Self Refresh (PSR).

Programming Notes
To use FBC modification tracking for idleness calculations when FBC is disabled, program FBC_CTL CPU Fence Enable bit 28, FBC_CONTROL_SA_REGISTER, FBC_CPU_FENCE_OFFSET_REGISTER, FBC_RT_BASE_ADDR_REGISTER, and BLITTER_TRACKING_REGISTER as they are programmed when FBC is enabled.
Cursor front buffer modifications are not tracked in hardware. If the cursor front buffer is modified, touch (write without changing) any cursor register to trigger the PSR idleness tracking.

Note:	Project
Note: FBC modification tracking for PSR idleness requires additional render command ring programming to add a LOAD_REGISTER_IMMEDIATE (LRI) to address 0x50340 with data 0x0000FFFF before the LRI to 0x50380 used for FBC tracking following render submission.	DevHSW:GT0:X0, DevHSW:GT3:A, DevHSW:GT3:B

Restriction
Restriction : Only the SRD Enable field can be changed while SRD is enabled. The other fields must not be changed while SRD is enabled.

DWord	Bit	Description
0	31	**SRD Enable** This bit enables the Self Refreshing Display function. Updates will take place at the start of the next vertical blank. The port will send SRD VDMs while enabled.

SRD_CTL

When idleness conditions have been met for the programmed number of idle frames, hardware will enter SRD (sleep) and can disable the link and stop fetching data from memory. When activity occurs, hardware will exit SRD (wake) and re-enable the link and resume fetching data from memory.

Value	Name
0b	Disable
1b	Enable

Restriction
Restriction : SRD must not be enabled when the PSR Setup time from DPCD 00071h is greater than the time for vertical blank minus one line.
Restriction : SRD must not be enabled together with Interlacing or Black Frame Insertion (BFI) on the same pipe.

30:28 **Reserved**

Format:	MBZ

27 **Link Ctrl**

This field controls the behavior of the link when in SRD (sleeping).
The timing generator and pixel data fetches are disabled when the link is disabled.
Only pixel data fetches are disabled when the link is in standby.

Value	Name	Description
0b	Disable	Link is disabled when in SRD (sleeping)
1b	Standby	Link is in standby when in SRD (sleeping)

Note:	Project
Note: Prior to HSW B stepping, Link standby mode is not supported. Use link disable mode instead.	DevHSW:GT0:X0, DevHSW:GT3:A
Note: Prior to HSW D stepping, FBC and SRD (PSR) link disable are not supported together. Disable one or the other.	DevHSW:GT0:X0, DevHSW:GT3:A, DevHSW:GT3:B, DevHSW:GT3:C
Note: Prior to HSW D stepping, IPS and SRD (PSR) link disable are not supported together. Disable one or the other.	DevHSW:GT3:B, DevHSW:GT3:C

26:25 **Reserved**

24:20 **Max Sleep Time**

Default Value:	00001b 1/8 second

This field is the maximum time to spend in SRD (sleeping).
It is programmed in increments of approximately 1/8 a second.
Programming all 1s gives ~3.875 seconds.

Restriction

SRD_CTL

	Restriction : Programming all 0s is invalid.
19:13	**Reserved** Format: MBZ
12	**Reserved**
11	**TP2 TP3 Select** This field controls whether TP1 is followed by TP2 or TP3 for training the link on exiting SRD (waking). Value / Name / Description 0b / TP2 / Use TP1 followed by TP2 1b / TP3 / Use TP1 followed by TP3
10	**Reserved** Format: MBZ
9:8	**TP2 TP3 Time** This field selects the TP2 or TP3 time when training the link on exiting SRD (waking). Value / Name 00b / 500us 01b / 100us 10b / 2.5ms 11b / 0us (Skip TP2/TP3)
7:6	**Reserved** Format: MBZ
5:4	**TP1 Time** This field selects the TP1 time when training the link on exiting SRD (waking). Value / Name 00b / 500us 01b / 100us 10b / 2.5ms 11b / 0us (Skip TP1)
3:0	**Idle Frames** Default Value: 0001b 1 idle frame This field is the number of idle frames required before entering SRD (sleeping).

SRD_AUX_CTL

SRD_AUX_CTL

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x000300E1
Access:	R/W
Size (in bits):	32
Address:	64810h-64813h
Name:	SRD AUX Channel Control
ShortName:	SRD_AUX_CTL
Power:	Always on
Reset:	soft

Restriction

Restriction : This register must be programmed prior to enabling SRD and must not be changed while SRD is enabled.
SRD AUX channel transactions must not be sent while DDI A AUX is being used. SRD must be completely disabled before a DDI A AUX channel transaction can be sent.

DWord	Bit	Description
0	31:28	**Reserved**
	27:26	**Time out timer value** This field is used to determine how long to wait for receiver response before timing out. Value / Name: 00b – 400us 01b – 600us 10b – 800us 11b – 1600us
	25	**Reserved**
	24:20	**Message Size** The value written to this field indicates the total number bytes to transmit (including the header). The value read from this field indicates the number of bytes received, including the header, in the last transaction transaction. Sync/Stop are not part of the message or the message size. Reads of this field will give the response message size. The read value will not be valid while Send/Busy bit 31 is asserted.

	Restriction Restriction : Message sizes of 0 or >20 are not allowed. Reads and writes are valid only when the done bit is set and timeout or receive error has not occurred.
19:16	**Precharge Time** Default Value: 0011b 6us Used to determine the precharge time for the Aux Channel. During this time the Aux Channel will drive the SYNC pattern. Every microsecond gives one additional SYNC pulse beyond the hard coded 26 SYNC pulses. The value is the number of microseconds times 2. Default is 3 decimal which gives 6us of precharge which is 6 extra SYNC pulses for a total of 32.
15:12	**Reserved**
11	**Interrupt on Error** Enable an interrupt when the transaction completes with a receive error or times out. **Value** / **Name** 0b – Disable 1b – Enable
10:0	**2X Bit Clock divider** Default Value: 00 1110 0001b 225 This field is used to determine the 2X bit clock the Aux Channel logic runs on. This value divides the input clock frequency down to 2X bit clock rate. It should be programmed to get as close as possible to the ideal rate of 2MHz. The input clock is the cdclk. Default is 225 decimal which divides the default 450 MHz cdclk input clock to become 2MHz bit clock. **Restriction** Restriction : The default value only works with cdclk 450 MHz. It must be programmed if the CD clock frequency is changed.

SRD_AUX_DATA

SRD_AUX_DATA	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	Write/Read Status
Size (in bits):	32
Address:	64814h-64827h
Name:	SRD AUX Channel Data
ShortName:	SRD_AUX_DATA_*
Power:	Always on
Reset:	soft

There are 5 instances of this register format.

Restriction
Restriction : This register must be programmed prior to enabling SRD and must not be changed while SRD is enabled.

DWord	Bit	Description
0	31:0	**SRD AUX CH DATA** This field contains a dword of the SRD AUX data to be transmitted in the SRD AUX message. The most significant byte is transmitted first. Reads to this register will give the response data after transaction complete.

SRD_IMR

SRD_IMR	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x03030307
Access:	R/W
Size (in bits):	32
Address:	64834h-64837h
Name:	SRD Interrupt Mask
ShortName:	SRD_IMR
Power:	Always on
Reset:	soft

See the SRD interrupt bit definition to find the source event for each interrupt bit.

DWord	Bit	Description
0	31:0	**Interrupt Mask Bits** This field contains a bit mask which selects which SRD events are reported int the SRD_IIR.

Value	Name
0b	Not Masked
1b	Masked
03030307h	All interrupts masked **[Default]**

SRD_IIR

SRD_IIR	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x03030307
Access:	R/WC
Size (in bits):	32
Address:	64838h-6483Bh
Name:	SRD Interrupt Identity
ShortName:	SRD_IIR
Power:	Always on
Reset:	soft

See the SRD interrupt bit definition to find the source event for each interrupt bit.

DWord	Bit	Description
0	31:0	**Interrupt Identity Bits** This field holds the persistent values of the SRD interrupt bits which are unmasked by the SRD_IMR. Bits set in this register will propagate to the SRD interrupt in the Display Engine Miscellaneous Interrupts. Bits set in this register will remain set (persist) until the interrupt condition is cleared by writing a '1' to the appropriate bits

Value	Name
0b	Condition Not Detected
1b	Condition Detected
03030307h	All interrupts masked **[Default]**

SRD_STATUS

SRD_STATUS

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	64840h-64843h
Name:	SRD Status
ShortName:	SRD_STATUS
Power:	Always on
Reset:	soft

SRD is tied to DDI A (EDP).

DWord	Bit	Description
0	31:29	**SRD State** Access: RO This field indicates the live state of SRD

Value	Name	Description
000b	IDLE	Reset state
001b	SRDONACK	Wait for TG/Stream to send on frame of data after SRD conditions are met
010b	SRDENT	SRD entry
011b	BUFOFF	Wait for buffer turn off (transcoder EDP only)
100b	BUFON	Wait for buffer turn on (transcoder EDP only)
101b	AUXACK	Wait for AUX to acknowledge on SRD exit (transcoder EDP only)
110b	SRDOFFACK	Wait for TG/Stream to acknowledge the SRD VDM exit
Others	Reserved	Reserved

	28	**Reserved** Format: MBZ
	27:26	**Link Status** Access: RO This field indicates the live status of the link.

Value	Name	Description
00b	Full Off	Link is fully off

SRD_STATUS

01b	Full On	Link is fully on
10b	Standby	Link is in standby
11b	Reserved	Reserved

25 **Reserved**

Format:	MBZ

24:20 **Max Sleep Time Counter**

Access:	RO

This field provides the live status of the sleep time counter.

19:16 **SRD Entry Count**

Access:	RO

The value in this register represents the number of times SRD has been entered (gone to sleep). The count will increment with each entry. After reaching the maximum count value the counter will rollover and continue from 0.

15 **Aux Error**

Access:	RO

This field indicates an error on the last SRD AUX handshake.

Value	Name	Description
0b	No Error	AUX had no error
1b	Error	AUX error (receive error or timeout) occured (transcoder EDP only)

14:13 **Reserved**

Format:	MBZ

12 **Sending Aux**

Access:	RO

This field indicates if the SRD AUX handshake is currently being sent.

Value	Name	Description
0b	Not Sending	Not sending AUX handshake
1b	Sending	Sending AUX handshake (transcoder EDP only)

11:10 **Reserved**

Format:	MBZ

9 **Sending Idle**

Access:	RO

This field indicates if idles are currently being sent.

Value	Name	Description
0b	Not Sending	Not sending idle
1b	Sending	Sending idle (transcoder EDP only)

SRD_STATUS

	8	**Sending TP2 TP3** Access: RO This field indicates if TP2 or TP3 is currently being sent. **Value** / **Name** / **Description** 0b / Not Sending / Not sending TP2 or TP3 1b / Sending / Sending TP2 or TP3 (transcoder EDP only)
	7:5	**Reserved** Format: MBZ
	4	**Sending TP1** Access: RO This field indicates if TP1 is currently being sent. **Value** / **Name** / **Description** 0b / Not Sending / Not sending TP1 1b / Sending / Sending TP1 (transcoder EDP only)
	3:0	**Idle Frame Counter** Access: RO This field provides the live status of the idle frame counter.

DDI_BUF_TRANS

DDI_BUF_TRANS	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000
Access:	R/W
Size (in bits):	640
Address:	64E00h-64E4Fh
Name:	DDI A Buffer Translation
ShortName:	DDI_BUF_TRANS_A_*
Power:	Always on
Reset:	global
Address:	64E60h-64EAFh
Name:	DDI B Buffer Translation
ShortName:	DDI_BUF_TRANS_B_*
Power:	Always on
Reset:	global
Address:	64EC0h-64F0Fh
Name:	DDI C Buffer Translation
ShortName:	DDI_BUF_TRANS_C_*
Power:	Always on
Reset:	global
Address:	64F20h-64F6Fh
Name:	DDI D Buffer Translation
ShortName:	DDI_BUF_TRANS_D_*
Power:	Always on
Reset:	global
Address:	64F80h-64FCFh
Name:	DDI E Buffer Translation
ShortName:	DDI_BUF_TRANS_E_*
Valid Projects:	[DevHSW, EXCLUDE(DevHSW:GT0:X0)]

DDI_BUF_TRANS

Power: Always on

Reset: global

These registers define the DDI buffer settings required for different voltage swing and emphasis selections.

In DisplayPort or FDI mode the DDI Buffer Control register programming will select which of these registers is used to drive the buffer.
In HDMI or DVI mode the HDMI/DVI translation registers are automatically selected.

For each DDI A/B/C/D/E there are 10 instances of this 2 DWord register format.
The first 9 instances (18 Dwords) are entries 0-8 which are used for DisplayPort and FDI.
The last instance (2 Dwords) is entry 9 which is used for HDMI and DVI.

Programming Notes
The recommended values are listed below this table.

Note:	Project
Note: The read value from these registers is incorrect and should be ignored.	DevHSW:GT0:X0

Restriction
Restriction : These registers must be programmed with valid values prior to enabling DDI_BUF_CTL.

DWord	Bit	Description
0	31:0	**Sel0 Trans 1** Format: **DDI Buffer Translation 1 Format**
1	31:0	**Sel0 Trans 2** Format: **DDI Buffer Translation 2 Format**
2	31:0	**Sel1 Trans 1** Format: **DDI Buffer Translation 1 Format**
3	31:0	**Sel1 Trans 2** Format: **DDI Buffer Translation 2 Format**
4	31:0	**Sel2 Trans 1** Format: **DDI Buffer Translation 1 Format**
5	31:0	**Sel2 Trans 2** Format: **DDI Buffer Translation 2 Format**
6	31:0	**Sel3 Trans 1** Format: **DDI Buffer Translation 1 Format**
7	31:0	**Sel3 Trans 2** Format: **DDI Buffer Translation 2 Format**
8	31:0	**Sel4 Trans 1**

DDI_BUF_TRANS		
		Format: DDI Buffer Translation 1 Format
9	31:0	**Sel4 Trans 2** Format: DDI Buffer Translation 2 Format
10	31:0	**Sel5 Trans 1** Format: DDI Buffer Translation 1 Format
11	31:0	**Sel5 Trans 2** Format: DDI Buffer Translation 2 Format
12	31:0	**Sel6 Trans 1** Format: DDI Buffer Translation 1 Format
13	31:0	**Sel6 Trans 2** Format: DDI Buffer Translation 2 Format
14	31:0	**Sel7 Trans 1** Format: DDI Buffer Translation 1 Format
15	31:0	**Sel7 Trans 2** Format: DDI Buffer Translation 2 Format
16	31:0	**Sel8 Trans 1** Format: DDI Buffer Translation 1 Format
17	31:0	**Sel8 Trans 2** Format: DDI Buffer Translation 2 Format
18	31:0	**Sel9 HDMI DVI Trans 1** Format: DDI Buffer Translation 1 Format
19	31:0	**Sel9 HDMI DVI Trans 2** Format: DDI Buffer Translation 2 Format

AUD_CONFIG

AUD_CONFIG

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	65000h-65003h
Name:	Audio Configuration Transcoder A
ShortName:	AUD_TCA_CONFIG
Power:	off/on
Reset:	soft
Address:	65100h-65103h
Name:	Audio Configuration Transcoder B
ShortName:	AUD_TCB_CONFIG
Power:	off/on
Reset:	soft
Address:	65200h-65203h
Name:	Audio Configuration Transcoder C
ShortName:	AUD_TCC_CONFIG
Power:	off/on
Reset:	soft

This register configures the audio output.
There is one instance of this register per transcoder A/B/C.

DWord	Bit	Description
0	31:30	**Reserved**
	29	**N value Index** Value / Name / Description 0b / HDMI **[Default]** / N value read on bits 27:20 and 15:4 reflects HDMI N value. Bits 27:20 and 15:4 are programmable to any N value. Default h7FA6. 1b / DisplayPort / N value read on bits 27:20 and 15:4 reflects DisplayPort N value. Set this bit to 1 before programming N value register. When this bit is set to 1, 27:20 and 15:4 will reflect the current N value. Default is h8000.
	28	**N programming enable**

AUD_CONFIG

		This bit enables programming of N values for non-CEA modes. Please note that the transcoder to which audio is attached must be disabled when changing this field.
	27:20	**Upper N value** These are bits [19:12] of programmable N values for non-CEA modes. Bit 29 of this register must also be written in order to enable programming. Please note that the transcoder to which audio is attached must be disabled when changing this field. See bit 29 description for default values.
	19:16	**Pixel Clock HDMI** This is the target frequency of the CEA/HDMI video mode to which the audio stream is added. This value is used for generating N_CTS packets. This refers to only HDMI Pixel clock and does not refer to DisplayPort Link clock. DisplayPort Link clock does not require this programming. Note: The transcoder on which audio is attached must be disabled when changing this field.
	15:4	**Lower N value** These are bits [11:0] of programmable N values for non-CEA modes. Bit 29 of this register must also be written in order to enable programming. Please note that the transcoder to which audio is attached must be disabled when changing this field. See bit 29 description for default values
	3	**Reserved**
	2:0	**Reserved**

Value	Name	Description
0b	**[Default]**	
0000b	25.2 / 1.001 MHz	25.2 / 1.001 MHz
0001b	25.2 MHz	25.2 MHz (Program this value for pixel clocks not listed in this field)
0010b	27 MHz	27 MHz
0011b	27 * 1.001 MHz	27 * 1.001 MHz
0100b	54 MHz	54 MHz
0101b	54 * 1.001 MHz	54 * 1.001 MHz
0110b	74.25 / 1.001 MHz	74.25 / 1.001 MHz
0111b	74.25 MHz	74.25 MHz
1000b	148.5 / 1.001 MHz	148.5 / 1.001 MHz
1001b	148.5 MHz	148.5 MHz
Others	Reserved	Reserved

AUD_MISC_CTRL

AUD_MISC_CTRL	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000044
Access:	R/W
Size (in bits):	32
Address:	65010h-65013h
Name:	Audio Converter 1 Misc Control
ShortName:	AUD_C1_MISC_CTRL
Power:	off/on
Reset:	soft
Address:	65110h-65113h
Name:	Audio Converter 2 Misc Control
ShortName:	AUD_C2_MISC_CTRL
Power:	off/on
Reset:	soft
Address:	65210h-65213h
Name:	Audio Converter 3 Misc Control
ShortName:	AUD_C3_MISC_CTRL
Power:	off/on
Reset:	soft
There is one instance of this register per audio converter 1/2/3.	

DWord	Bit	Description
0	31:9	**Reserved** Format: MBZ
	8	**Reserved**
	7:4	**Output Delay** Default Value: 0100b The number of samples between when the sample is received from the HD Audio link and when it appears as an analog signal at the pin.
	3	**Reserved** Format: MBZ

AUD_MISC_CTRL

2 — Sample Fabrication EN bit

Access:	R/W

This bit indicates whether internal fabrication of audio samples is enabled during a link underrun.

Value	Name	Description
0b	Disable	Audio fabrication disabled
1b	Enable **[Default]**	Audio fabrication enabled

1 — Pro Allowed

Access:	R/W

By default, the audio device is configured to consumer mode and does not allow the mode to be changed to professional mode by an HD Audio verb. When Pro is allowed by setting this configuration bit, the HD Audio codec allows a verb to set the device into professional mode.
Note: Setting this configuration bit does not change the default Pro bit value to be 1. Pro must be set to 1 through the normal process, using a verb.

Value	Name	Description
0b	Consumer **[Default]**	Consumer use only
1b	Professional	Professional use allowed

0 — Reserved

Format:	MBZ

AUD_VID_DID

AUD_VID_DID	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x80862807
Access:	RO
Size (in bits):	32
Address:	65020h-65023h
Name:	Audio Vendor ID / Device ID Read Only
ShortName:	AUD_VID_DID_RO
Power:	off/on
Reset:	soft

These values are returned from the device as the Vendor ID/ Device ID response to a Get Root Node command.

DWord	Bit	Description
0	31:16	**Vendor ID** Default Value: 8086h Used to identify the codec within the PnP system. This field is hardwired within the device.
	15:0	**Device ID** Default Value: 2807h Haswell Constant used to identify the codec within the PnP system. This field is set by the device hardware.

AUD_RID

AUD_RID	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00100000
Access:	RO
Size (in bits):	32
Address:	65024h-65027h
Name:	Audio Revision ID Read Only
ShortName:	AUD_RID_RO
Power:	off/on
Reset:	soft

These values are returned from the device as the Revision ID response to a Get Root Node command.

DWord	Bit	Description
0	31:24	**Reserved**
	23:20	**Major Revision** Default Value: 1h The major revision number (left of the decimal) of the HD Audio Spec to which the codec is fully compliant. This field is hardwired within the device.
	19:16	**Minor Revision** Default Value: 0h The minor revision number (rights of the decimal) or dot number of the HD Audio Spec to which the codec is fully compliant. This field is hardwired within the device.
	15:8	**Revision ID** Default Value: 00h The vendor revision number for this given Device ID. This field is hardwired within the device.
	7:0	**Stepping ID** Default Value: 00h An optional vendor stepping number within the given Revision ID. This field is hardwired within the device.

AUD_M_CTS_ENABLE

<table>
<tr><th colspan="3">AUD_M_CTS_ENABLE</th></tr>
<tr><td colspan="3">Register Space: MMIO: 0/2/0
Project: HSW
Source: PRM
Default Value: 0x00000000
Access: R/W
Size (in bits): 32</td></tr>
<tr><td colspan="3">Address: 65028h-6502Bh
Name: Audio M and CTS Programming Enable Transcoder A
ShortName: AUD_TCA_M_CTS_ENABLE
Power: off/on
Reset: soft</td></tr>
<tr><td colspan="3">Address: 65128h-6512Bh
Name: Audio M and CTS Programming Enable Transcoder B
ShortName: AUD_TCB_M_CTS_ENABLE
Power: off/on
Reset: soft</td></tr>
<tr><td colspan="3">Address: 65228h-6522Bh
Name: Audio M and CTS Programming Enable Transcoder C
ShortName: AUD_TCC_M_CTS_ENABLE
Power: off/on
Reset: soft</td></tr>
<tr><td colspan="3">There is one instance of this register per transcoder A/B/C.</td></tr>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td rowspan="3">0</td><td>31:22</td><td>Reserved</td></tr>
<tr><td>21</td><td>CTS M value Index
<table>
<tr><th>Value</th><th>Name</th><th>Description</th></tr>
<tr><td>0b</td><td>CTS [Default]</td><td>CTS value read on bits 19:0 reflects CTS value. Bit 19:0 is programmable to any CTS value. default is 0</td></tr>
<tr><td>1b</td><td>M</td><td>M value read on bits 19:0 reflects DisplayPort M value. Set this bit to 1 before programming M value register. When this is set to 1 19:0 will reflect the current M value</td></tr>
</table></td></tr>
<tr><td>20</td><td>Enable CTS or M prog
When set will enable CTS or M programming.</td></tr>
</table>

AUD_M_CTS_ENABLE		
	19:0	**CTS programming** These are bits [19:0] of programmable CTS values for non-CEA modes. Bit 21 of this register must also be written in order to enable programming. Please note that the transcoder to which audio is attached must be disabled when changing this field.

AUD_PWRST

AUD_PWRST	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x0FFFFFFF
Access:	RO
Size (in bits):	32
Address:	6504Ch-6504Fh
Name:	Audio Power State Read Only
ShortName:	AUD_PWRST_RO
Power:	off/on
Reset:	soft

These values are returned from the device as the Power State response to a Get Audio Function Group command.

DWord	Bit	Description
0	31:28	**Reserved**
	27:26	**Func Grp Dev PwrSt Curr** Format: **Audio Power State Format** Function Group Device current power state
	25:24	**Func Grp Dev PwrSt Set** Format: **Audio Power State Format** Function Group Device power state that was set
	23:22	**Converter3 Widget PwrSt Curr** Format: **Audio Power State Format** Converor3 Widget current power state
	21:20	**Converter3 Widget PwrSt Req** Format: **Audio Power State Format** Converor3 Widget power state that was requested by audio software
	19:18	**Convertor2 Widget PwrSt Curr** Format: **Audio Power State Format** Converor2 Widget current power state

AUD_PWRST

	17:16	**Convertor2 Widget PwrSt Req** Format: **Audio Power State Format** Converter2 Widget power state that was requested by audio software
	15:14	**Convertor1 Widget PwrSt Curr** Format: **Audio Power State Format** Converter1 Widget current power state
	13:12	**Convertor1 Widget PwrSt Req** Format: **Audio Power State Format** Converter1 Widget power state that was requested by audio software
	11:10	**PinD Widget PwrSt Curr** Format: **Audio Power State Format** PinD Widget current power stateFor DP MST this represents Device3 power state
	9:8	**PinD Widget PwrSt Set** Format: **Audio Power State Format** PinD Widget power state that was setFor DP MST this represents Device3 power state
	7:6	**PinC Widget PwrSt Curr** Format: **Audio Power State Format** PinC Widget current power stateFor DP MST this represents Device2 power state
	5:4	**PinC Widget PwrSt Set** Format: **Audio Power State Format** PinC Widget power state that was setFor DP MST this represents Device2 power state
	3:2	**PinB Widget PwrSt Curr** Format: **Audio Power State Format** PinB Widget current power stateFor DP MST this represents Device1 power state
	1:0	**PinB Widget PwrSt Set** Format: **Audio Power State Format** PinB Widget power state that was setFor DP MST this represents Device1 power state

AUD_EDID_DATA

AUD_EDID_DATA	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	65050h-65053h
Name:	Audio EDID Data Block Transcoder A
ShortName:	AUD_TCA_EDID_DATA
Power:	off/on
Reset:	soft
Address:	65150h-65153h
Name:	Audio EDID Data Block Transcoder B
ShortName:	AUD_TCB_EDID_DATA
Power:	off/on
Reset:	soft
Address:	65250h-65253h
Name:	Audio EDID Data Block Transcoder C
ShortName:	AUD_TCC_EDID_DATA
Power:	off/on
Reset:	soft

These registers contain the HDMI/DP data block from the EDID. The graphics driver reads the EDID and writes the structure to these registers. The vendor specific data block may be longer than 8 bytes, but the driver must not write more than 48 bytes to the buffer. The EDID format is Version 3 within the CEA-861B specification. The HDMI/DP Vendor Specific Data Block is described in version 1.1 of the HDMI specification.

These values are returned from the device as the HDMI/DP Vendor Specific Data Block response to a Get HDMI/DP Widget command.

Writing sequence: Video software sets ELD invalid, and sets the ELD access address to 0, or to the desired DWORD to be written.

Video software writes ELD data 1 DWORD at a time. The ELD access address autoincrements with each DWORD write, wrapping around to address 0 when the max buffer address size of 0xF has been reached. Please note that software must write an entire DWORD at a time.

Please note that the audio driver checks the valid bit with each byte read of the ELD. This means that the video driver can unilaterally write ELD irrespective of audio driver ELD read status.

Reading sequence: Video software sets the ELD access address to 0, or to the desired DWORD to be read.

AUD_EDID_DATA

Video software reads ELD data 1 DWORD at a time. The ELD access address autoincrements with each DWORD read, wrapping around to address 0 when the max buffer address size of 0xF has been reached.
There is one instance of this register per transcoder A/B/C.

DWord	Bit	Description
0	31:0	**EDID Data Block** Please note that the contents of this buffer are not cleared when ELD is disabled. The contents of this buffer are cleared during FLR.

AUD_INFOFR

AUD_INFOFR	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	65054h-65057h
Name:	Audio Widget Data Island Packet Transcoder A
ShortName:	AUD_TCA_INFOFR
Power:	off/on
Reset:	soft
Address:	65154h-65157h
Name:	Audio Widget Data Island Packet Transcoder B
ShortName:	AUD_TCB_INFOFR
Power:	off/on
Reset:	soft
Address:	65254h-65257h
Name:	Audio Widget Data Island Packet Transcoder C
ShortName:	AUD_TCC_INFOFR
Power:	off/on
Reset:	soft

When the IF type or dword index is not valid, the contents of the DIP will return all 0s. These values are programmed by the audio driver in an HDMI/DP Widget Set command. They are returned one byte at a time from the device on the HD audio bus as the HDMI/DP DIP response to a Get HDMI/DP Widget command. To fetch a specific byte, the audio driver should send an HDMI/DP Widget HDMI/DP DIP Index Pointer Set command to set the index, then fetch the indexed byte using the HDMI/DP DIP get.

Video software reads DIP data 1 DWORD at a time. The DIP access address auto increments with each DWORD write, wrapping around to address 0 when the max buffer address size of 0xF has been reached. There is one instance of this register per transcoder A/B/C.

DWord	Bit	Description
0	31:0	**Data Island Packet Data** This reflects the contents of the DIP indexed by the DIP access address. The contents of this buffer are cleared during function reset or HD audio link reset.

AUD_PIN_PIPE_CONN_ENTRY_LNGTH

AUD_PIN_PIPE_CONN_ENTRY_LNGTH	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000001
Access:	RO
Size (in bits):	32
Address:	650A8h-650ABh
Name:	Audio Connection List Entry and Length Transcoder A
ShortName:	AUD_TCA_PIN_PIPE_CONN_ENTRY_LNGTH_RO
Power:	off/on
Reset:	soft
Address:	651A8h-651ABh
Name:	Audio Connection List Entry and Length Transcoder B
ShortName:	AUD_TCB_PIN_PIPE_CONN_ENTRY_LNGTH_RO
Power:	off/on
Reset:	soft
Address:	652A8h-652ABh
Name:	Audio Connection List Entry and Length Transcoder C
ShortName:	AUD_TCC_PIN_PIPE_CONN_ENTRY_LNGTH_RO
Power:	off/on
Reset:	soft

These values are returned from the device as the Connection List Length response to a Get Pin Widget command or Get Device Widget command if DP MST.
There is one instance of this register per transcoder A/B/C.

DWord	Bit	Description
0	31:16	**Reserved**
	15:8	**Connection List Entry** Connection to Convertor Widget Node 0x03
	7	**Long Form** This bit indicates whether the items in the connection list are long form or short form. This bit is hardwired to 0 (items in connection list are short form)
	6:0	**Connection List Length** Default Value: 0000001b

AUD_PIN_PIPE_CONN_ENTRY_LNGTH		
		This field indicates the number of items in the connection list. If this field is 2, there is only one hardwired input possible, which is read from the Connection List, and there is no Connection Select Control.

AUD_PIPE_CONN_SEL_CTRL

AUD_PIPE_CONN_SEL_CTRL	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00030303
Access:	RO
Size (in bits):	32
Address:	650ACh-650AFh
Name:	Audio Pipe Connection Select Control
ShortName:	AUD_PIN_PIPE_CONN_SEL_CTRL_RO
Power:	off/on
Reset:	soft

These values are returned from the device as the Connection List Length response to a Get Pin Widget command or Get Device Widget command for DP MST.

DWord	Bit	Description
0	31:24	**Reserved**
	23:16	**Connection select Control D** Default Value: 03h Connection Index Currently Set [Default 0x00], Port D Widget is set to 0x02
	15:8	**Connection select Control C** Default Value: 03h Connection Index Currently Set [Default 0x00], Port C Widget is set to 0x01
	7:0	**Connection select Control B** Default Value: 03h Connection Index Currently Set [Default 0x00], Port B Widget is set to 0x00

AUD_DIP_ELD_CTRL_ST

AUD_DIP_ELD_CTRL_ST

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00005400
Access:	R/W
Size (in bits):	32
Address:	650B4h-650B7h
Name:	Audio DIP and ELD Status Transcoder A
ShortName:	AUD_TCA_DIP_ELD_CTRL_ST
Power:	off/on
Reset:	soft
Address:	651B4h-651B7h
Name:	Audio DIP and ELD Status Transcoder B
ShortName:	AUD_TCB_DIP_ELD_CTRL_ST
Power:	off/on
Reset:	soft
Address:	652B4h-652B7h
Name:	Audio Control State for DIP and ELD Transcoder C
ShortName:	AUD_TCC_DIP_ELD_CTRL_ST
Power:	off/on
Reset:	soft

There is one instance of this register per transcoder A/B/C.

DWord	Bit	Description
0	31	**Reserved** Format: MBZ
	30:29	**DIP Port Select** Access: RO This read-only bit reflects which port is used to transmit the DIP data. This can only change when DIP is disabled. If one or more audio-related DIP packets is enabled and audio is enabled on a digital port, these bits will reflect the digital port to which audio is directed. For DP MST, this is the device select/pipe select. **Value** / **Name** / **Description** 00b / Reserved **[Default]** / Reserved

AUD_DIP_ELD_CTRL_ST

01b	Digital Port B	Digital Port B
10b	Digital Port C	Digital Port C
11b	Digital Port D	Digital Port D

28:25 **Reserved**

Format:	MBZ

24:21 **DIP type enable status**

Access:	RO

These bits reflect the DIP types enabled. It can be updated while the port is enabled. Within 2 vblank periods, the DIP is guaranteed to have been transmitted. Disabling a DIP type results in setting the contents of that DIP buffer to zero. A reserved setting reflects a disabled DIP.

Value	Name	Description
0000b	**[Default]**	
XXX0b	Disable	Audio DIP disabled
XXX1b	Enable	Audio DIP enabled
XX0Xb	Disable	Generic 1 (ACP) DIP disabled
XX1Xb	Enable	Generic 1 (ACP) DIP enabled
X0XXb	Disable	Generic 2 DIP disabled
X1XXb	Enable	Generic 2 DIP enabled, can be used by ISRC1 or ISRC2
1XXXb	Reserved	Reserved

20:18 **DIP buffer index**

This field is used during read of different DIPs, and during read or write of ELD data. These bits are used as an index to their respective DIP or ELD buffers. When the index is not valid, the contents of the DIP will return all 0s.

Value	Name	Description
0000b	**[Default]**	
000b	Audio	Audio DIP (31 bytes of address space, 31 bytes of data)
001b	Gen 1	Generic 1 (ACP) Data Island Packet (31 bytes of address space, 31 bytes of data)
010b	Gen 2	Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data)
011b	Gen 3	Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data)
Others	Reserved	Reserved

17:16 **DIP transmission frequency**

Access:	RO

These bits reflect the frequency of DIP transmission for the DIP buffer type designated in bits 20:18. When writing DIP data, this value is also latched when the first DW of the DIP is written.

When read, this value reflects the DIP transmission frequency for the DIP buffer designated in bits 20:18.

Value	Name	Description
00b	Disable **[Default]**	Disabled
01b	Reserved	Reserved
10b	Send Once	Send Once
11b	Best Effort	Best effort (Send at least every other vsync)

15 **Reserved**

Format:	MBZ

14:10 **ELD buffer size**

Default Value:	10101b
Access:	RO

This field reflects the size of the ELD buffer in DWORDs (84 Bytes of ELD)

9:5 **ELD access address**
Selects the DWORD address for access to the ELD buffer (84 bytes). The value wraps back to zero when incremented past the max addressing value 0x1F. This field change takes effect immediately after being written. The read value indicates the current access address.

4 **ELD ACK**
Acknowledgement from the audio driver that ELD read has been completed

3:0 **DIP access address**
Selects the DWORD address for access to the DIP buffers. The value wraps back to zero when it incremented past the max addressing value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.

AUD_PIN_ELD_CP_VLD

AUD_PIN_ELD_CP_VLD

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000 [HSW]
Access:	R/W
Size (in bits):	32
Address:	650C0h-650C3h
Name:	Audio Pin ELD and CP Ready Status
ShortName:	AUD_PIN_ELD_CP_VLD
Power:	off/on
Reset:	soft

This register is used for handshaking between the audio and video drivers for interrupt management.
[DevHSW-X0] For each port, ELD and content protection readiness is sent by the display software to the audio software via an unsolicited response when the ELD or CP ready bit is set. Display software sets these bits as part of enabling the respective audio-enabled digital port. These bits are port based (TranscoderA was portB, TranscoderB was portC and TranscoderC was portD in HSW X0).
[DevHSW-A0+] For each transcoder, ELD and content protection readiness is sent by the display software to the audio software via an unsolicited response when the ELD or CP ready bit is set. Display software sets these bits as part of enabling the respective audio-enabled digital device/transcoder. To support DP MST, these bits are transcoder based and harfware will use it appropriately to send the status to the audio driver using device widgets. Both HDMI and DP1.1 will also be transcoder based as shown below.

DWord	Bit	Description
0	31:12	**Reserved**
	11	**Reserved** Project: DevHSW:GT0:X0
	11	**Audio InactiveC** Project: DevHSW, EXCLUDE(DevHSW:GT0:X) Inactive: When this bit is set, a digital display sink device has been attached but not active for streaming audio. This bit is not defined for HSW-X0. Value / Name / Description: 0b / Disable **[Default]** / Device is active for streaming audio data 1b / Enable / Device is connected but not active
	10	**Audio Output EnableD** Project: DevHSW:GT0:X0 This bit directs audio to this port. When enabled and audio data is available, the audio data will

be combined with the video data and sent over this port. The audio unit uses the status of this bit to indicate presence of the HDMI/DP output to the audio driver. This bit is pipe based for DP MST and represents Device3

Value	Name	Description
0b	Disable **[Default]**	No Audio output
1b	Valid	Audio is enabled

10 **Audio Output EnableC**

Project:	DevHSW, EXCLUDE(DevHSW:GT0:X)

This bit directs audio to the device connected to this transcoder. When enabled along with Inactive set to 0and audio data is available, the audio data will be combined with the video data and sent over this transcoder. The audio unit uses the status of this bit to indicate presence of the HDMI/DP output to the audio driver.

Value	Name	Description
0b	Disable **[Default]**	No Audio output
1b	Valid	Audio is enabled

Note:
Note: Whenever audio PD bit is turned ON any pipe (which can be found out from the AUD_PIN_ELD_CP_VLD register 0x650C0), program 0x46508 register bit 14 to 1.

9 **CP ReadyD**

Project:	DevHSW:GT0:X0

This R/W bit reflects the state of CP request from the audio unit. When an audio CP request has been serviced, it must be reset to 1 by the video software to indicate that the CP request has been serviced.
This is port based in HSW-X0.

Value	Name	Description
0b	Pending or Not Ready **[Default]**	CP request pending or not ready to receive requests
1b	Ready	CP request ready

9 **CP ReadyC**

Project:	DevHSW, EXCLUDE(DevHSW:GT0:X)

This R/W bit reflects the state of CP request from the audio unit. When an audio CP request has been serviced, it must be reset to 1 by the video software to indicate that the CP request has been serviced. This is transcoder based on HSW-A0+

Value	Name	Description
0b	Pending or Not Ready **[Default]**	CP request pending or not ready to receive requests
1b	Ready	CP request ready

8 **ELD validD**

Project:	DevHSW:GT0:X0

This R/W bit reflects the state of the ELD data written to the ELD RAM. After writing the ELD data,

AUD_PIN_ELD_CP_VLD

the video software must set this bit to 1 to indicate that the ELD data is valid. At audio codec initialization, or on a hotplug event, this bit is set to 0 by the video software. This bit is reflected in the audio pin complex widget as the ELD valid status bit.
This is port based in HSW-X0.

Value	Name	Description
0b	Invalid **[Default]**	ELD data invalid (default, when writing ELD data, set 0 by software)
1b	Valid	ELD data valid (Set by video software only)

8 **ELD validC**

Project:	DevHSW, EXCLUDE(DevHSW:GT0:X)

This R/W bit reflects the state of the ELD data written to the ELD RAM. After writing the ELD data, the video software must set this bit to 1 to indicate that the ELD data is valid. At audio codec initialization, or on a hotplug event, this bit is set to 0 by the video software. This bit is reflected in the audio pin complex widget as the ELD valid status bit. This is transcoder based on HSW-A0+

Value	Name	Description
0b	Invalid **[Default]**	ELD data invalid (default, when writing ELD data, set 0 by software)
1b	Valid	ELD data valid (Set by video software only)

7 **Reserved**

Project:	DevHSW:GT0:X0

7 **Audio InactiveB**

Project:	DevHSW, EXCLUDE(DevHSW:GT0:X)

Inactive: When this bit is set, a digital display sink device has been attached but not active for streaming audio.

Value	Name	Description
0b	Disable **[Default]**	Device is active for streaming audio data
1b	Enable	Device is connected but not active

6 **Audio Output EnableC**

Project:	DevHSW:GT0:X0

This bit directs audio to this port. When enabled and audio data is available, the audio data will be combined with the video data and sent over this port. The audio unit uses the status of this bit to indicate presence of the HDMI/DP output to the audio driver. This bit is pipe based for DP MST and represents Device2. This is port based on HSW-X0.

Value	Name	Description
0b	Disable **[Default]**	No audio output
1b	Enable	Audio is enabled

6 **Audio Output EnableB**

Project:	DevHSW, EXCLUDE(DevHSW:GT0:X)

This bit directs audio to the device connected to this transcoder. When enabled along with Inactive set to 0 and audio data is available, the audio data will be combined with the video data

and sent over this transcoder. The audio unit uses the status of this bit to indicate presence of the HDMI/DP output to the audio driver. This is transcoder based on HSW-A0+.

Value	Name	Description
0b	Disable **[Default]**	No audio output
1b	Enable	Audio is enabled

Note:
Note: Whenever audio PD bit is turned ON any pipe (which can be found out from the AUD_PIN_ELD_CP_VLD register 0x650C0), program 0x46508 register bit 14 to 1.

5 **CP ReadyC**

Project:	DevHSW:GT0:X0

See CP_ReadyD description.

Value	Name	Description
0b	Not Ready **[Default]**	CP request pending or not ready to receive requests
1b	Ready	CP request ready

5 **CP ReadyB**

Project:	DevHSW, EXCLUDE(DevHSW:GT0:X)

See CP_ReadyD description.

Value	Name	Description
0b	Not Ready **[Default]**	CP request pending or not ready to receive requests
1b	Ready	CP request ready

4 **ELD validC**

Project:	DevHSW:GT0:X0

See ELD_validD descripion.

Value	Name	Description
0b	Invalid **[Default]**	ELD data invalid (default, when writing ELD data, set 0 by software)
1b	Valid	ELD data valid (Set by video software only)

4 **ELD validB**

Project:	DevHSW, EXCLUDE(DevHSW:GT0:X)

See ELD_validD descripion.

Value	Name	Description
0b	Invalid **[Default]**	ELD data invalid (default, when writing ELD data, set 0 by software)
1b	Valid	ELD data valid (Set by video software only)

3 **Reserved**

Project:	DevHSW:GT0:X0

3 **Audio InactiveA**

Project:	DevHSW, EXCLUDE(DevHSW:GT0:X)

Inactive: When this bit is set, a digital display sink device has been attached but not active for streaming audio.

Value	Name	Description
0b	Disable **[Default]**	Device is active for streaming audio data
1b	Enable	Device is connected but not active

2 **Audio Output EnableB**

Project:	DevHSW:GT0:X0

This bit directs audio to this port. When enabled and audio data is available, the audio data will be combined with the video data and sent over this port. The audio unit uses the status of this bit to indicate presence of the HDMI/DP output to the audio driver. This bit is pipe based for DP MST and represents Device1. This is port based for HSW-X0.

Value	Name	Description
0b	Disable **[Default]**	No audio output
1b	Enable	Audio is enabled

2 **Audio Output EnableA**

Project:	DevHSW, EXCLUDE(DevHSW:GT0:X)

This bit directs audio to the device connected to this transcoder. When enabled along with Inactive set to 0 and audio data is available, the audio data will be combined with the video data and sent over this transcoder. The audio unit uses the status of this bit to indicate presence of the HDMI/DP output to the audio driver. This is transcoder based for HSW-A0+

Value	Name	Description
0b	Disable **[Default]**	No audio output
1b	Enable	Audio is enabled

Note:
Note: Whenever audio PD bit is turned ON any pipe (which can be found out from the AUD_PIN_ELD_CP_VLD register 0x650C0), program 0x46508 register bit 14 to 1.

1 **CP ReadyB**

Project:	DevHSW:GT0:X0

See CP_ReadyD description.

Value	Name	Description
0b	Not Ready **[Default]**	CP request pending or not ready to receive requests
1b	Ready	CP request ready

1 **CP ReadyA**

Project:	DevHSW, EXCLUDE(DevHSW:GT0:X)

See CP_ReadyD description.

Value	Name	Description
0b	Not Ready **[Default]**	CP request pending or not ready to receive requests

AUD_PIN_ELD_CP_VLD

		1b: Ready — CP request ready
	0	**ELD validB** Project: DevHSW:GT0:X0 See ELD_validD descripion. 0b: Invalid **[Default]** — ELD data invalid (default, when writing ELD data, set 0 by software) 1b: Valid — ELD data valid (Set by video software only)
	0	**ELD validA** Project: DevHSW, EXCLUDE(DevHSW:GT0:X) See ELD_validD descripion. 0b: Invalid **[Default]** — ELD data invalid (default, when writing ELD data, set 0 by software) 1b: Valid — ELD data valid (Set by video software only)

GTC_CPU_CTL

GTC_CPU_CTL

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x0000010E
Access:	R/W
Size (in bits):	32
Address:	67000h-67003h
Name:	Global Time Code CPU Control
ShortName:	GTC_CPU_CTL
Valid Projects:	[DevHSW, EXCLUDE(DevHSW:GT0:X0)]
Power:	off/on
Reset:	soft

Note:	Project
Note: GTC registers must not be read or written.	DevHSW:GT0:X0

DWord	Bit	Description
0	31	**GTC CPU Slave Enable** This bit enables the slave GTC. When enabled, the slave uses periodic GTC messages received from PCH over CSYNC to update its GTC value. If this bit is set but the PCH GTC controller is disabled, the slave GTC runs independently with no forced synchronization to PCH GTC controller. **Value / Name:** 0b = Disable; 1b = Enable **Restriction:** Restriction : The DDA M/N settings must be programmed to valid values before enabling this bit.
	30:29	**Reserved**
	28	**Reserved**
	27:25	**Reserved**
	24	**Maintenance Phase Enable** This bit is used to transition from lock acquisition to lock maintenance phase. The CPU GTC slave can generate an interrupt every time it receives a GTC update message from the PCH.

Check for lock status by reading the slave lock field in the GTC_CPU_MISC register.
Set this bit to 1b after making the determination that lock requirement has been satisfied.
If it is determined that CPU GTC slave is no longer locked while in maintenance mode, clear this bit and attempt to achieve lock again.

Value	Name	Description
0b	Lock	Lock acquisition phase
1b	Maintain	Lock maintenance phase

Programming Notes
Maintenance interval for sending GTC updates is 11ms instead of 10ms.

23:21	**Reserved**
20:11	**Reserved**
10:1	**Reference Clock Freq**

Default Value:	1 0000 111b 135

This field is used to indicate the frequency of the reference clock used by the GTC slave and aux decoder.
Hardware uses this value to divide down the GTC reference clock as needed to implement 1MHz aux signaling frequency.
The input clock is the non-SSC reference. The frequency can be found in the FUSE_STRAP3 register.

0	**Reserved**

GTC_CPU_MISC

GTC_CPU_MISC

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00400000
Access:	R/W
Size (in bits):	32
Address:	67004h-67007h
Name:	Global Time Code CPU Miscellaneous
ShortName:	GTC_CPU_MISC
Valid Projects:	[DevHSW, EXCLUDE(DevHSW:GT0:X0)]
Power:	off/on
Reset:	soft

Note:	Project
Note: GTC registers must not be read or written.	DevHSW:GT0:X0

DWord	Bit	Description
0	31:24	**Reserved**
	23:22	**CPU GTC Lock Compare Value** This field programs the threshold used to determine whether to set the lock status bit following comparison between the slave and master GTC values.
	21:16	**Reserved**
	15:6	**Reserved**
	5:0	**Update Message Delay** This field is the absolute delay in nanoseconds between the GTC aux sync point event in PCH and the corresponding sync point seen by the CPU GTC slave. It represents the delay between the GTC values in PCH and CPU due to fixed propagation delay of GTC update message. It is only applied to the GTC value sampled for audio. It is not factored directly in the CPU slave GTC update computation or reflected in the GTC local registers.

Value	Name	Description
00b	30ns	Difference between master/slave is less than 30ns
01b	50ns **[Default]**	Difference between master/slave is less than 50ns (default)
10b	100ns	Difference between master/slave is less than 100ns
11b	200ns	Difference between master/slave is less than 200ns

GTC_CPU_DDA_M

GTC_CPU_DDA_M	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	67010h-67013h
Name:	Global Time Code CPU DDA M Value
ShortName:	GTC_CPU_DDA_M
Valid Projects:	[DevHSW, EXCLUDE(DevHSW:GT0:X0)]
Power:	off/on
Reset:	soft

Note:	Project
Note: GTC registers must not be read or written.	DevHSW:GT0:X0

DWord	Bit	Description
0	31:24	**Reserved**
	23:0	**GTC DDA M** This field is the M value of the GTC DDA. The ratio of M to N programmed depends on the GTC reference clock. The DDA programmed values are related by the following formula: 1/(accumulator increment)=Reference Clock * DDA_M / DDA_N.

GTC_CPU_DDA_N

GTC_CPU_DDA_N

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000 [HSW:GT1.5,HSW:GT2,HSW:GT3:A,HSW:GT3E,HSW:ULT2,HSW:ULT3]
Access:	R/W
Size (in bits):	32
Address:	67014h-67017h
Name:	Global Time Code CPU DDA N Value
ShortName:	GTC_CPU_DDA_N
Valid Projects:	[DevHSW, EXCLUDE(DevHSW:GT0:X0)]
Power:	off/on
Reset:	soft

Note:	Project
Note: GTC registers must not be read or written.	DevHSW:GT0:X0

DWord	Bit	Description
0	31:26	**GTC Accum Inc** Project: DevHSW:GT3:A Format: U5.1 This field is the GTC accumulator increment value in nanoseconds each time the DDA trips. It is programmed in 5.1 fixed point binary format where the LSB represents 0.5ns increment.
	31:24	**GTC Accum Inc** Project: DevHSW, EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A) Format: U7.1 This field is the GTC accumulator increment value in nanoseconds each time the DDA trips. It is programmed in 7.1 fixed point binary format where the LSB represents 0.5ns increment.
	25:24	**Reserved** Project: DevHSW:GT3:A
	23:0	**GTC DDA N** This field is the N value of the GTC DDA. The ratio of M to N programmed depends on the GTC reference clock and should not result in any accumulation error in any 10ms interval period. The DDA programmed values are related by the following formula: 1/(accumulator increment)=Reference Clock * DDA_M / DDA_N.

GTC_CPU_LIVE

GTC_CPU_LIVE	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	67020h-67023h
Name:	Global Time Code CPU Live Value
ShortName:	GTC_CPU_LIVE
Valid Projects:	[DevHSW, EXCLUDE(DevHSW:GT0:X0)]
Power:	off/on
Reset:	soft

Note:	Project
Note: GTC registers must not be read or written.	DevHSW:GT0:X0

DWord	Bit	Description
0	31:0	**GTC CPU Live** This field contains the live current value of the GTC. It is inactive when the CPU GTC function is disabled. It does not reflect the message update delay adjustment.

GTC_CPU_REMOTE_CURR

GTC_CPU_REMOTE_CURR	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	67024h-67027h
Name:	Global Time Code CPU Remote Current Value
ShortName:	GTC_CPU_REMOTE_CURR
Valid Projects:	[DevHSW, EXCLUDE(DevHSW:GT0:X0)]
Power:	off/on
Reset:	soft

Note:	Project
Note: GTC registers must not be read or written.	DevHSW:GT0:X0

DWord	Bit	Description
0	31:0	**GTC Remote Current Value** This field contains the last PCH GTC value received via the GTC update message. It represents the value of the (remote) PCH GTC at the Aux sync point at time of transmission of the message over CSYNC. The PCH GTC controller sends periodic updates of its GTC value to the CPU GTC slave.

GTC_CPU_LOCAL_CURR

GTC_CPU_LOCAL_CURR	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	67028h-6702Bh
Name:	Global Time Code CPU Local Current Value
ShortName:	GTC_CPU_LOCAL_CURR
Valid Projects:	[DevHSW, EXCLUDE(DevHSW:GT0:X0)]
Power:	off/on
Reset:	soft

Note:	Project
Note: GTC registers must not be read or written.	DevHSW:GT0:X0

DWord	Bit	Description
0	31:0	**GTC Local Current Value** This field contains the last CPU GTC value sampled at the Aux sync point of the GTC update message received from PCH GTC controller.

GTC_CPU_REMOTE_PREV

GTC_CPU_REMOTE_PREV

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	6702Ch-6702Fh
Name:	Global Time Code CPU Remote Previous Value
ShortName:	GTC_CPU_REMOTE_PREV
Valid Projects:	[DevHSW, EXCLUDE(DevHSW:GT0:X0)]
Power:	off/on
Reset:	soft

Note:	Project
Note: GTC registers must not be read or written.	DevHSW:GT0:X0

DWord	Bit	Description
0	31:0	**GTC Remote Previous Value** This field contains the second to last PCH GTC value received via the GTC update message. It represents the value of the (remote) PCH GTC at the Aux sync point at time of transmission of the message over CSYNC. The PCH GTC controller sends periodic updates of its GTC value to the CPU GTC slave.

GTC_CPU_LOCAL_PREV

GTC_CPU_LOCAL_PREV	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	67030h-67033h
Name:	Global Time Code CPU Local Previous Value
ShortName:	GTC_CPU_LOCAL_PREV
Valid Projects:	[DevHSW, EXCLUDE(DevHSW:GT0:X0)]
Power:	off/on
Reset:	soft

Note:	Project
Note: GTC registers must not be read or written.	DevHSW:GT0:X0

DWord	Bit	Description
0	31:0	**GTC Local Previous Value** This field contains the second to last CPU GTC value sampled at the Aux sync point of the GTC update message received from PCH GTC controller.

GTC_CPU_IMR

GTC_CPU_IMR

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x0000000F
Access:	R/W
Size (in bits):	32
Address:	67054h-67057h
Name:	Global Time Code CPU Interrupt Mask
ShortName:	GTC_CPU_IMR
Valid Projects:	[DevHSW, EXCLUDE(DevHSW:GT0:X0)]
Power:	off/on
Reset:	soft

See the GTC CPU interrupt bit definition table to find the source event for each interrupt bit.

Note:	Project
Note: GTC registers must not be read or written.	DevHSW:GT0:X0

DWord	Bit	Description
0	31:0	**Interrupt Mask Bits** This field contains a bit mask which selects which GTC CPU events are reported int the GTC CPU IIR.

Value	Name
0b	Not Masked
1b	Masked
00000000Fh	All interrupts masked **[Default]**

GTC_CPU_IIR

GTC_CPU_IIR	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/WC
Size (in bits):	32
Address:	67058h-6705Bh
Name:	Global Time Code CPU Interrupt Identity
ShortName:	GTC_CPU_IIR
Valid Projects:	[DevHSW, EXCLUDE(DevHSW:GT0:X0)]
Power:	off/on
Reset:	soft

See the GTC CPU interrupt bit definition to find the source event for each interrupt bit.

Note:	Project
Note: GTC registers must not be read or written.	DevHSW:GT0:X0

DWord	Bit	Description
0	31:0	**Interrupt Identity Bits** This field holds the persistent values of the GTC CPU interrupt bits which are unmasked by the GTC_CPU_IMR. Bits set in this register will propagate to the GTC_CPU interrupt in the Display Engine Miscellaneous Interrupts. Bits set in this register will remain set (persist) until the interrupt condition is cleared by writing a '1' to the appropriate bits.

Value	Name
0b	Condition Not Detected
1b	Condition Detected

PF_PWR_GATE

PF_PWR_GATE	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank after armed
Double Buffer Armed By:	Write to PF_WIN_SZ
Address:	68060h-68063h
Name:	PF 0 Power Gate Control
ShortName:	PF_PWR_GATE_0
Power:	off/on
Reset:	soft
Address:	68860h-68863h
Name:	PF 1 Power Gate Control
ShortName:	PF_PWR_GATE_1
Power:	off/on
Reset:	soft
Address:	69060h-69063h
Name:	PF 2 Power Gate Control
ShortName:	PF_PWR_GATE_2
Power:	off/on
Reset:	soft

DWord	Bit	Description
0	31	**Reserved**
	30:5	**Reserved** Format: MBZ
	4:3	**Settling Time** Time for RAMs in a given filter group to settle after they are powered up. Value: 00b — Name: 32 cdclks — Description: 80ns

01b	64 cdclks	160ns
10b	96 cdclks	240ns
11b	128 cdcclks	320ns

2 **Reserved**

Format:	MBZ

1:0 **SLPEN Delay**

Delay between sleep enables of individual banks of RAMs.

Value	Name	Description
00b	8 cdclks	20ns
01b	16 cdclks	40ns
10b	24 cdclks	60ns
11b	32 cdclks	80ns

PF_WIN_POS

PF_WIN_POS	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank after armed
Double Buffer Armed By:	Write to PF_WIN_SZ
Address:	68070h-68073h
Name:	PF 0 Window Position
ShortName:	PF_WIN_POS_0
Power:	off/on
Reset:	soft
Address:	68870h-68873h
Name:	PF 1 Window Position
ShortName:	PF_WIN_POS_1
Power:	off/on
Reset:	soft
Address:	69070h-69073h
Name:	PF 2 Window Position
ShortName:	PF_WIN_POS_2
Power:	off/on
Reset:	soft

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28:16	**XPOS** The X coordinate in pixels of the upper left most pixel of the panel fitted display window. **Restriction** Restriction : The X position must not be programmed to be 1 (28:16=0 0000 0000 0001b).
	15:12	**Reserved**

PF_WIN_POS			
		Format:	MBZ
	11:0	**YPOS** The Y coordinate in lines of the upper left most pixel of the panel fitter display window. **Restriction** Restriction : LSB must be zero for interlaced modes.	

PF_WIN_SZ

PF_WIN_SZ	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank
Address:	68074h-68077h
Name:	PF 0 Window Size
ShortName:	PF_WIN_SZ_0
Power:	off/on
Reset:	soft
Address:	68874h-68877h
Name:	PF 1 Window Size
ShortName:	PF_WIN_SZ_1
Power:	off/on
Reset:	soft
Address:	69074h-69077h
Name:	PF 2 Window Size
ShortName:	PF_WIN_SZ_2
Power:	off/on
Reset:	soft

Coordinates are determined with a value of (0,0) being the upper left corner of the display device (rotation does not affect this).
Writes to this register arm PF registers on this pipe.

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28:16	**XSIZE** The horizontal size in pixels of the desired panel fitted window.
	15:12	**Reserved** Format: MBZ

PF_WIN_SZ		
	11:0	**YSIZE** The vertical size in pixels of the desired panel fitted window. **Restriction** Restriction : LSB must be zero for interlaced modes.

PF_CTRL

PF_CTRL	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank after armed
Double Buffer Armed By:	Write to PF_WIN_SZ
Address:	68080h-68083h
Name:	PF 0 Control
ShortName:	PF_CTRL_0
Power:	off/on
Reset:	soft
Address:	68880h-68883h
Name:	PF 1 Control
ShortName:	PF_CTRL_1
Power:	off/on
Reset:	soft
Address:	69080h-69083h
Name:	PF 2 Control
ShortName:	PF_CTRL_2
Power:	off/on
Reset:	soft
There are three panel fitters: Panel fitter 0 is always 7x5 filter capable. Panel fitter 1 defaults to 3x3 filter capable. It can be changed to 7x5 filter capable if Panel fitter 2 is disabled and PF1 7x5 Reconfig Enable is selected. Panel fitter 2 is always 3x3 filter capable. Any of the three panel fitters can be assigned to any pipe. A 3x3 capable filter can support pipe horizontal source sizes less than or equal to 2048 pixels. A 7x5 capable filter can support pipe horizontal source sizes of less than or equal to 4096 pixels. When the pipe	

PF_CTRL

horizontal source size is greater than 2048 pixels, the filter will automatically switch to a 3x3 filter mode.

It is recommended to use a 7x5 capable filter for best image quality with interlaced display.

Restriction

Restriction : A 3x3 capable filter must not be enabled when the pipe horizontal source size is greater than 2048 pixels.
A 7x5 capable filter must not be enabled when the pipe horizontal source size is greater than 4096 pixels.

The panel fitter can not be enabled while the display power well is powered down.

Down scaling is only supported up to 1.125 (pipe source size / panel fitter window size) in each direction.

When using panel fitter down scaling (pipe source size is larger than panel fitter window size) the maximum supported pixel rate will be reduced by the down scale amount and the watermark for planes on the same pipe has to increase by the down scale amount.

DWord	Bit	Description
0	31	**Enable Pipe Scaler** Value: 0b – Disable; 1b – Enable **Note:** When moving a panel fitter from a disabled pipe to an enabled pipe, change Pipe Select first to move the panel fitter to the enabled pipe before changing Enable Pipe Scaler to enable it.
	30:29	**Pipe Select** This bit determines which display pipe this panel fitter will connect to. Value: 00b – Name: Pipe A – Description: Pipe A Value: 01b – Name: Pipe B – Description: Pipe B Value: 10b – Name: Pipe C – Description: Pipe C Value: 11b – Name: Reserved – Description: Reserved **Restriction** Restriction : Do not enable and connect more than one panel fitter to a pipe.
	28	**Reserved**
	27	**Reserved**
	26:25	**Reserved**
	24:23	**FILTER SELECT**

PF_CTRL

Selects filter coefficients. The medium coefficients will provide an unfiltered image when the scale factor is 1:1.

Value	Name
00b, 01b	Medium
10b	Edge Enhance
11b	Edge Soften

22 PF1 7x5 Reconfig Enable

This field enables panel fitter 1 to reconfigure to be 7x5 filter capable.
This can only be enabled while panel fitter 2 is completely disabled.
This field only applies to panel fitter 1.

Value	Name	Description
0b	Disable	Disable panel fitter 1 reconfiguration to 7x5 capable
1b	Enable	Enable panel fitter 1 reconfiguration to 7x5 capable

21 Reserved

20 Reserved

19:18 Reserved

Format:	MBZ

17 Reserved

16:0 Reserved

Format:	MBZ

DISPIO_CR_TX_BMU_CR4

DISPIO_CR_TX_BMU_CR4

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6C01Ch-6C01Fh
Name:	Display IO TXBMU CR4
ShortName:	DISPIO_CR_TX_BMU_CR4

DWord	Bit	Description
0	31:26	**Reserved** Format: MBZ
	25	**tx_icomp_ovrd_en** Load ICOMP override: EDP port. 0b: allow bits 30:0 to updated with msg channel value on a write 1b: allow bits 30:0 to be updated with status on a write
	24	**tx_icomp_ovrd_en_edp2** Load ICOMP override: EDP+ port. 0b: allow bits 30:0 to updated with msg channel value on a write 1b: allow bits 30:0 to be updated with status on a write
	23:18	**tx_icomp_rd_ovrd_15** TX ICOMP RD/OVRD - Lane 15
	17:12	**tx_icomp_rd_ovrd_14** TX ICOMP RD/OVRD - Lane 14
	11:6	**tx_icomp_rd_ovrd_13** TX ICOMP RD/OVRD - Lane 13
	5:0	**tx_icomp_rd_ovrd_12** TX ICOMP RD/OVRD - Lane 12

PIPE_MSA_MISC

PIPE_MSA_MISC	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank
Address:	60410h-60413h
Name:	Pipe A MSA Misc
ShortName:	PIPE_MSA_MISC_A
Power:	off/on
Reset:	soft
Address:	61410h-61413h
Name:	Pipe B MSA Misc
ShortName:	PIPE_MSA_MISC_B
Power:	off/on
Reset:	soft
Address:	62410h-62413h
Name:	Pipe C MSA Misc
ShortName:	PIPE_MSA_MISC_C
Power:	off/on
Reset:	soft
Address:	6F410h-6F413h
Name:	Pipe EDP MSA Misc
ShortName:	PIPE_MSA_MISC_EDP
Power:	Always on
Reset:	soft
There is one instance of this register per each transcoder A/B/C/EDP. This register selects what value will be sent in the DisplayPort Main Stream Attribute (MSA) Miscellaneous (MISC) fields. The MSA MISC fields are mostly used to indicate the color encoding format and need to be programmed to indicate color space, bits per color, etc.	

PIPE_MSA_MISC

Programming Notes

See the DisplayPort specification for the details on what to program in these fields.

DWord	Bit	Description
0	31:16	**MSA Unused** This field selects the value that will be sent in the DisplayPort MSA unused fields. **Programming Notes** This should be usually programmed with all 0s.
	15:8	**MSA MISC1** This field selects the value that will be sent in the DisplayPort MSA MISC1 field.
	7:0	**MSA MISC0** This field selects the value that will be sent in the DisplayPort MSA MISC0 field. **Restriction** Restriction : Before enabling DisplayPort, bit 0 should always be set to 1 to indicate link clock and stream clock are synchronous.

PIPE_SCANLINE

PIPE_SCANLINE

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	70000h-70003h
Name:	Pipe A Scan Line
ShortName:	PIPE_SCANLINE_A
Power:	Always on
Reset:	soft
Address:	71000h-71003h
Name:	Pipe B Scan Line
ShortName:	PIPE_SCANLINE_B
Power:	off/on
Reset:	soft
Address:	72000h-72003h
Name:	Pipe C Scan Line
ShortName:	PIPE_SCANLINE_C
Power:	off/on
Reset:	soft

This register enables the read back of the pipe vertical line counter.
The value increments at the leading edge of HSYNC.
The value resets to line zero at the first active line of the display.
In interlaced display timings, the scan line counter provides the current line in the field. One field can have a total number of lines that is one greater than the other field.

DWord	Bit	Description
0	31	**Current Field** This is an indication of the current display field.

Value	Name	Description
0b	Odd	First field (odd field)
1b	Even	Second field (even field)

DWord	Bit	Description
	30:13	**Reserved**

PIPE_SCANLINE		
	12:0	**Line Counter for Display** This is an indication of the current display scan line. **Programming Notes** The line count value is from the display output timing generator, representing the scan line currently being output to a receiver. Due to buffering within the display engine, the line being fetched (read) from the frame buffer is not directly linked to the line being output. It is possible for the fetched line to be hundreds of lines ahead of the timing generator output line.

PIPE_SCANLINECOMP

PIPE_SCANLINECOMP	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000 [HSW]
Access:	R/W
Size (in bits):	32
Address:	70004h-70007h
Name:	Pipe A Scan Line Compare
ShortName:	PIPE_SCANLINECOMP_A
Power:	Always on
Reset:	soft
Address:	71004h-71007h
Name:	Pipe B Scan Line Compare
ShortName:	PIPE_SCANLINECOMP_B
Power:	off/on
Reset:	soft
Address:	72004h-72007h
Name:	Pipe C Scan Line Compare
ShortName:	PIPE_SCANLINECOMP_C
Power:	off/on
Reset:	soft

This register is used to initiate a display scan line compare.
This MMIO driven scan line compare can not be used at the same time as the command streamer driven scan line compare on the same pipe.

When this register is written with the Initiate Compare bit set to 1b, the Display Engine (DE) will start comparing the display pipe or primary plane (selectable) current scan line value (current scan line) with the start scan line value (current scan line >= start scan line) and the end scan line value (current scan line <= end scan line) to decide if the pipe scan line is inside or outside the scan line window of interest.
DE will wait until the current scan line is either outside (Inclusive mode) or inside (Exclusive mode) the scan line window, then trigger a scan line event and stop any further comparing.

The scan line event can cause display to send a scan line compare response to the command streamer, (used for releasing a MI_WAIT_FOR_EVENT on scan line window), if unmasked in the DERRMR mask register 0x44050.
The scan line event can also cause display to generate a scan line compare interrupt, if the interrupt registers are

PIPE_SCANLINECOMP

configured for that.

The value programmed should be the desired value - 1, so for scan line 0, the value programmed is vertical total, and for scan line 1, the value programmed is 0.
The programmable range can include the vertical blank.
In interlaced display timings, the current scan line is the current line of the current interlaced field.

Either MMIO or a MI_LOAD_REGISTER_IMM command can be used to unmask the scan line render response 0x44050. That can be done anytime before programming this register.

There is one instance of this register format per each pipe A/B/C.

Restriction
Restriction : A new scan line compare must not be started until after the previous compare has finished. The end scan line value must be greater than or equal to the start scan line value. When using LRI care must be taken to follow all the programming rules for LRI targetting the display engine.

DWord	Bit	Description
0	31	**Initiate Compare** This field initiates the scan line compare. When this register is written with this bit set to 1b, the display engine will do one complete comparison cycle, trigger a scan line event, then stop comparing. **Value** / **Name** 0b – Do nothing 1b – Initiate compare **Restriction** Restriction : Do not write this register again until after any previous scan line compare has completed.
	30	**Inclusive Exclusive Select** This field selects whether the scan line compare is done in inclusive mode, where display triggers the scan line event when outside the scan line window, or inclusive mode, where display triggers when inside the window. **Value** / **Name** / **Description** 0b / Exclusive / Exclusive mode: trigger scan line event when inside the scan line window 1b / Inclusive / Inclusive mode: trigger scan line event when outside the scan line window
	29	**Counter Select** Project: DevHSW, EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A) This field selects whether the scan line compare is done using the pipe timing generator scanline counter or the primary plane scanline counter. The pipe timing generator counts the scanlines being output from display. The primary plane counts the scanlines being fetched from the frame buffer.

PIPE_SCANLINECOMP

Value	Name	Description
0b	Timing generator	Use the scanline count from the pipe timing generator
1b	Primary plane	Use the scanline count from the primary plane

Programming Notes
Due to buffering within the display engine, the line being fetched from the frame buffer is not directly linked to the line being output. It is possible for the fetched line to be hundreds of lines ahead of the timing generator output line. The primary plane scanline count more closely represents what data is currently being fetched by the primary plane.

29	**Reserved** Project: DevHSW:GT0:X0, DevHSW:GT3:A
28:16	**Start Scan Line** This field specifies the starting scan line number of the scan line window.
15	**Render Response Destination** This bit indicates what destination to send the scan line event render response to.

Value	Name	Description
0b	CS	Send scan line event response to CS
1b	BCS	Send scan line event response to BCS

14:13	**Reserved**
12:0	**End Scan Line** This field specifies the ending scan line number of the scan line window.

PIPE_CONF

PIPE_CONF	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank OR pipe disabled
Address:	70008h-7000Bh
Name:	Pipe A Configuration
ShortName:	PIPE_CONF_A
Power:	off/on
Reset:	soft
Address:	71008h-7100Bh
Name:	Pipe B Configuration
ShortName:	PIPE_CONF_B
Power:	off/on
Reset:	soft
Address:	72008h-7200Bh
Name:	Pipe C Configuration
ShortName:	PIPE_CONF_C
Power:	off/on
Reset:	soft
Address:	7F008h-7F00Bh
Name:	Pipe EDP Configuration
ShortName:	PIPE_CONF_EDP
Power:	Always on
Reset:	soft

There is one instance of this register format per each pipe timing generator A/B/C/EDP.

DWord	Bit	Description
0	31	**Pipe Enable** Setting this bit to the value of one, turns on this pipe. Turning the pipe off disables the timing generator and synchronization pulses to the display will

PIPE_CONF

not be maintained.
Enabling the pipe may be internally delayed for one frame while the display data buffers are re-configured.

Value	Name
0b	Disable
1b	Enable

Restriction
Restriction : Pipe timing registers must contain valid values before this bit is enabled.

30 **Pipe State**

Access:	RO

This read only bit indicates the actual state of the pipe.

Value	Name
0b	Disabled
1b	Enabled

29:23 **Reserved**

22:21 **Interlaced Mode**
These bits control the pipe interlaced mode.

Value	Name	Description
00b	PF-PD	Progressive Fetch with Progressive Display
01b	PF-ID	Progressive Fetch with Interlaced Display
11b	IF-ID	Interlaced Fetch with Interlaced Display
Others	Reserved	Reserved

Restriction
Restriction : VGA display modes do not work while in interlaced fetch modes. Progressive Fetch with Interlaced Display requires 7x5 capable panel fitter to be enabled and a horizontal source size of less than or equal to 2048 pixels.

20 **Refresh Rate Switch**
This bit switches display to an alternate refresh rate used for low power.
Link and data M/N 1 values are used for normal settings, M/N 2 values for low power settings.

Value	Name
0b	Normal
1b	Low Power

Restriction
Restriction : Refresh rate switching is only supported on pipe EDP.

19:16 **Reserved**

PIPE_CONF

15:14 Display Rotation Info

This field indicates to internal KVMR screen capture that the display has been rotated through software or hardware rotation.

Select the closest value if the rotation is not an exact multiple of 90 degrees.

Hardware rotation of the display output is controlled through the plane control registers, not through this field.

Value	Name	Description
00b	None	No rotation on this pipe
01b	90	90 degree rotation on this pipe
10b	180	180 degree rotation on this pipe
11b	270	270 degree rotation on this pipe

Restriction
Restriction : This field must be programmed in order for internal KVMR screen capture to work correctly when display is rotated by software or hardware.

13:12 Reserved

Format:	MBZ

11 Pipe output color space select

This field indicates the output color space.

This field affects the values of the pipe border and some capture functions.

This field does not affect the planes, pipe CSC, or ports.

Value	Name
0b	RGB
1b	YUV

Restriction
Restriction : This field must be set to match the color space that will be output from the pipe CSC or output from the planes if they pipe CSC is bypassed.

10 xvYCC Color Range Limit

This field limits the color range of the port outputs to 1 to 254 for 8-bit components, 4 to 1019 for 10bit components, and 16 to 4079 for 12-bit components.

Values outside of the range will be clamped to fit within the range.

Value	Name	Description
0b	Full	Do not limit the range
1b	Limit	Limit range

9:5 Reserved

Format:	MBZ

4 Dithering enable

This field enables dithering.

PIPE_CONF

		Value / **Name** 0b — Disable 1b — Enable
	3:2	**Dithering type** This field selects the dithering type. **Value** / **Name** / **Description** 00b — Spatial — Spatial 01b — ST1 — Spatio-Temporal 1 10b — ST2 — Spatio-Temporal 2 11b — Temporal — Temporal
	1:0	**Reserved** Format: MBZ

PIPE_FRMCNT

PIPE_FRMCNT	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	70040h-70043h
Name:	Pipe A Frame Count
ShortName:	PIPE_FRMCNT_A
Power:	Always on
Reset:	soft
Address:	71040h-71043h
Name:	Pipe B Frame Count
ShortName:	PIPE_FRMCNT_B
Power:	off/on
Reset:	soft
Address:	72040h-72043h
Name:	Pipe C Frame Count
ShortName:	PIPE_FRMCNT_C
Power:	off/on
Reset:	soft
There is one instance of this register format per each set of display planes A/B/C.	

DWord	Bit	Description
0	31:0	**Pipe Frame Counter** Provides read back of the display pipe frame counter. This counter increments on every start of vertical blank and rolls over back to 0 after (2^32)-1 frames.

PIPE_FLIPCNT

PIPE_FLIPCNT	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	70044h-70047h
Name:	Pipe A Flip Count
ShortName:	PIPE_FLIPCNT_A
Power:	Always on
Reset:	soft
Address:	71044h-71047h
Name:	Pipe B Flip Count
ShortName:	PIPE_FLIPCNT_B
Power:	off/on
Reset:	soft
Address:	72044h-72047h
Name:	Pipe C Flip Count
ShortName:	PIPE_FLIPCNT_C
Power:	off/on
Reset:	soft

There is one instance of this register format per each set of display planes A/B/C.

DWord	Bit	Description
0	31:0	**Pipe Flip Counter** This field provides read back of the display pipe flip counter. The counter increments on the start of each flip to the primary plane of this pipe. The start of flip is when the plane surface address is updated, not when the flip completes. The flip can be through command streamer asynchronous and synchronous flips or MMIO writes to the primary plane surface address. It rolls over back to 0 after (2^32)-1 flips.

PIPE_FRMTMSTMP

PIPE_FRMTMSTMP	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	70048h-7004Bh
Name:	Pipe A Frame Time Stamp
ShortName:	PIPE_FRMTMSTMP_A
Power:	Always on
Reset:	soft
Address:	71048h-7104Bh
Name:	Pipe B Frame Time Stamp
ShortName:	PIPE_FRMTMSTMP_B
Power:	off/on
Reset:	soft
Address:	72048h-7204Bh
Name:	Pipe C Frame Time Stamp
ShortName:	PIPE_FRMTMSTMP_C
Power:	off/on
Reset:	soft

There is one instance of this register format per each set of display planes A/B/C.

DWord	Bit	Description
0	31:0	**Pipe Frame Time Stamp** This field provides read back of the display pipe frame time stamp. The time stamp value is sampled at every start of vertical blank. The TIMESTAMP_CTR register has the current time stamp value.

PIPE_FLIPTMSTMP

PIPE_FLIPTMSTMP	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	7004Ch-7004Fh
Name:	Pipe A Flip Time Stamp
ShortName:	PIPE_FLIPTMSTMP_A
Power:	Always on
Reset:	soft
Address:	7104Ch-7104Fh
Name:	Pipe B Flip Time Stamp
ShortName:	PIPE_FLIPTMSTMP_B
Power:	off/on
Reset:	soft
Address:	7204Ch-7204Fh
Name:	Pipe C Flip Time Stamp
ShortName:	PIPE_FLIPTMSTMP_C
Power:	off/on
Reset:	soft

There is one instance of this register format per each set of display planes A/B/C.

DWord	Bit	Description
0	31:0	**Pipe Flip Time Stamp** This field provides read back of the display pipe flip time stamp. The time stamp value is sampled on the start of each flip to the primary plane of this pipe. The start of flip is when the plane surface address is updated, not when the flip completes. The flip can be through command streamer asynchronous and synchronous flips or MMIO writes to the primary plane surface address. The TIMESTAMP_CTR register has the current time stamp value.

CUR_CTL

CUR_CTL	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to CUR_BASE or cursor not enabled
Address:	70080h-70083h
Name:	Cursor A Control
ShortName:	CUR_CTL_A
Power:	Always on
Reset:	soft
Address:	71080h-71083h
Name:	Cursor B Control
ShortName:	CUR_CTL_B
Power:	off/on
Reset:	soft
Address:	72080h-72083h
Name:	Cursor C Control
ShortName:	CUR_CTL_C
Power:	off/on
Reset:	soft

The cursor is enabled by programming a valid cursor mode in the cursor mode select fields.
The cursor is disabled by programming all 0s in the cursor mode select fields.

DWord	Bit	Description
0	31:27	**Reserved**
	26	**Gamma Enable** This bit enables pipe gamma correction for the cursor pixel data. In VGA pop-up operation, the cursor data will always bypass gamma.

Value	Name

CUR_CTL

	0b	Disable
	1b	Enable

25 Reserved

24 Pipe CSC Enable

This bit enables pipe color space conversion for the cursor pixel data.

Value	Name
0b	Disable
1b	Enable

23:16 Reserved

15 180 Rotation

This mode causes the cursor image to be rotated 180 degrees.
In addition to setting this bit, the cursor position must be adjusted to match the physical orientation of the display.

Value	Name
0b	No rotation
1b	180 degree rotation

Restriction
Restriction : Only 32 bits per pixel cursors can be rotated. This field must be zero when the cursor format is 2 bits per pixel.

14 Trickle Feed Enable

Value	Name
0b	Enable
1b	Disable

Restriction
Restriction : Do not program this field to 1b.

13:12 Reserved

11:10 Force Alpha Plane Select

This field selects which planes the cursor alpha value will be forced for. It is used together with the Force Alpha Value field.

Value	Name	Description
00b	Disable	Disable alpha forcing
01b	Sprite	Enable alpha forcing where cursor overlaps sprite pixels
10b	Primary	Enable alpha forcing where cursor overlaps primary pixels
11b	Both	Enable alpha forcing where cursor overlaps either sprite or primary pixels.

9:8 Force Alpha Value

CUR_CTL

This field controls the behavior of cursor when alpha blending onto certain plane pixels.
It is used together with the Force Alpha Plane Select field.

Value	Name	Description
00b	Disable	Cursor pixels alpha blend normally over any plane.
01b	50	Cursor pixels with alpha >= 50% are made fully opaque where they overlap the selected plane(s). Cursor pixels with alpha < 50% are made fully transparent where they overlap the selected plane(s).
10b	75	Cursor pixels with alpha >= 75% are made fully opaque where they overlap the selected plane(s). Cursor pixels with alpha < 75% are made fully transparent where they overlap the selected plane(s).
11b	100	Cursor pixels with alpha = 100% are made fully opaque where they overlap the selected plane(s). Cursor pixels with alpha < 100% are made fully transparent where they overlap the selected plane(s).

Restriction
Restriction : Force Alpha is only for use with ARGB cursor formats.

7:6 **Reserved**

5:0 **Cursor Mode Select**

This field selects the cursor mode.
Cursor is disabled when the selection is 000000b and enabled when the selection is any other value.
The cursor vertical size can be overriden by the size reduction mode.

Value	Name	Description
000000b	Disable	Cursor is disabled
000010b	128x128 32bpp AND/INV	128x128 32bpp AND/INVERT
000011b	256x256 32bpp AND/INV	256x256 32bpp AND/INVERT
000100b	64x64 2bpp 3-color	64x64 2bpp Indexed 3-color and transparency
000101b	64x64 2bpp 2-color	64x64 2bpp Indexed AND/XOR 2-color
000110b	64x64 2bpp 4-color	64x64 2bpp Indexed 4-color
000111b	64x64 32bpp AND/INV	64x64 32bpp AND/INVERT
100010b	128x128 32bpp ARGB	128x128 32bpp ARGB (8:8:8:8 MSB-A:R:G:B)
100011b	256x256 32bpp ARGB	256x256 32bpp ARGB (8:8:8:8 MSB-A:R:G:B)
100100b	64x64 32bpp AND/XOR	64x64 32bpp AND/XOR
100101b	128x128 32bpp AND/XOR	128x128 32bpp AND/XOR
100110b	256x256 32bpp AND/XOR	256x256 32bpp AND/XOR
100111b	64x64 32bpp ARGB	64x64 32bpp ARGB (8:8:8:8 MSB-A:R:G:B)
Others	Reserved	Reserved

CUR_CTL

Programming Notes
INVERT, XOR, and alpha blends may not look as expected when the plane underlying the cursor is YUV or extended range RGB. Out of range RGB values will be clamped prior to alpha blending, INVERT, or XOR with cursor. It is recommended to use Force Alpha when cursor is alpha blending onto an plane of a different color space or extended gamut.
The AND/INVERT format uses the most significant byte (MSB) to control the color. If MSB is 0xFF: Cursor is opaque. Show cursor color from three least significant bytes. If MSB is 0x00: Cursor is transparent. Three least significant bytes must be zero. If MSB is not 0x00 or 0xFF: Cursor inverts the color of the surface underneath.
The AND/XOR format uses the most significant byte (MSB) to control the color. If MSB is 0xFF: Cursor is opaque. Show cursor color from three least significant bytes. If MSB is 0x00: Cursor is transparent. Three least significant bytes must be zero. If MSB is not 0x00 or 0xFF: The three least significant bytes are XOR'd with the color of the surface underneath.

Note:	Project
Note: When RC6 and package C-states >= C3 are enabled, register 45280h bits 2:0 must be set to 111b the entire time that all display planes are disabled. That setting will impact power when planes are enabled, so the recommended sequence is to add programming to write register 45280h bits 2:0 = 111b just prior to disabling the last display plane, and write register 45280h bits 2:0 = 000b one vertical blank after the first display plane is enabled. First and last display plane refer to the entire set of planes, primary A/B/C, sprite A/B/C, and cursor A/B/C.	DevHSW:GT0:X0, DevHSW:GT3:A, DevHSW:GT3:B
Note: Register 45280h bits 2:0 must be set to 111b the entire time that any display planes (primary, sprite, cursor) are enabled on a pipe that is not enabled. That setting will impact power, so the recommended sequence is to write register 45280h bits 2:0 = 111b just prior to enabling the first display plane on the disabled pipe, then restore 45280h bits 2:0 one vertical blank after the pipe is enabled.	
Note: An alternative procedure is needed before enabling planes (primary, sprite, cursor) when transitioning from no pipes or a single pipe enabled to multiple pipes enabled. Refer to the Display Mode Set Sequence enable sequences for details.	

CUR_BASE

CUR_BASE	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled
Address:	70084h-70087h
Name:	Cursor A Base Address
ShortName:	CUR_BASE_A
Power:	Always on
Reset:	soft
Address:	71084h-71087h
Name:	Cursor B Base Address
ShortName:	CUR_BASE_B
Power:	off/on
Reset:	soft
Address:	72084h-72087h
Name:	Cursor C Base Address
ShortName:	CUR_BASE_C
Power:	off/on
Reset:	soft

Writes to this register arm cursor registers for this pipe.

DWord	Bit	Description
0	31:12	**Cursor Base 31 12** Format: GraphicsAddress[31:12] This field specifies bits 31:12 of the graphics address of the base of the cursor for hi-res mode. When performing 180 degree rotation, this address does not need to change, hardware will internally offset to start from the last pixel of the last line of the cursor. **Note:** **Note:** To prevent false VT-d type 6 errors, use 64KB address alignment and allocate an extra 2 Page Table Entries (PTEs) beyond the end of the displayed surface.

CUR_BASE		
		Only the PTEs will be used, not the pages themselves. **Restriction** Restriction : The cursor surface address must be 4K byte aligned. The cursor must be in linear memory, it cannot be tiled.
	11:3	**Reserved**
	2	**Reserved**
	1:0	**Reserved**

CUR_POS

CUR_POS	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled
Address:	70088h-7008Bh
Name:	Cursor A Position
ShortName:	CUR_POS_A
Power:	Always on
Reset:	soft
Address:	71088h-7108Bh
Name:	Cursor B Position
ShortName:	CUR_POS_B
Power:	off/on
Reset:	soft
Address:	72088h-7208Bh
Name:	Cursor C Position
ShortName:	CUR_POS_C
Power:	off/on
Reset:	soft

This register specifies the screen position of the cursor.
The origin of the cursor position is always the upper left corner of the display pipe source image area.
When performing 180 degree rotation, the cursor image is rotated by hardware, but the position is not, so it should be adjusted if it is desired to maintain the same apparent position on a physically rotated display.

Restriction
Restriction : The cursor must have at least a single pixel positioned over the pipe source area.

DWord	Bit	Description
0	31	**Y Position Sign** This specifies the sign of the vertical position of the cursor upper left corner.
	30:28	**Reserved**

CUR_POS		
		Format: MBZ
	27:16	**Y Position Magnitude** This specifies the magnitude of the vertical position of the cursor upper left corner in lines.
	15	**X Position Sign** This specifies the sign of the horizontal position of the cursor upper left corner.
	14:13	**Reserved** Format: MBZ
	12:0	**X Position Magnitude** This specifies the magnitude of the horizontal position of the cursor upper left corner in pixels.

CUR_PAL

CUR_PAL	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled
Address:	70090h-7009Fh
Name:	Cursor A Palette
ShortName:	CUR_PAL_A_*
Power:	Always on
Reset:	soft
Address:	71090h-7109Fh
Name:	Cursor B Palette
ShortName:	CUR_PAL_B_*
Power:	off/on
Reset:	soft
Address:	72090h-7209Fh
Name:	Cursor C Palette
ShortName:	CUR_PAL_C_*
Power:	off/on
Reset:	soft

The cursor palette provides color information when using the indexed cursor modes.
There are 4 instances of this register format per cursor.
The table below describes how the cursor mode and index value will select between the cursor palette colors, AND/XOR, transparency, and destination invert.

Index Value	2 color mode	3 color mode	4 color mode
00	CUR_PAL 0	CUR_PAL 0	CUR_PAL 0
01	CUR_PAL 1	CUR_PAL 1	CUR_PAL 1
10	Transparent	Transparent	CUR_PAL 2
11	Invert Destination	CUR_PAL 3	CUR_PAL 3

DWord	Bit	Description
0	31:24	**Reserved**
	23:16	**Palette Red** This field is the cursor palette red value
	15:8	**Palette Green** This field is the cursor palette green value.
	7:0	**Palette Blue** This field is the cursor palette blue value.

CUR_FBC_CTL

CUR_FBC_CTL	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to CUR_BASE or cursor not enabled
Address:	700A0h-700A3h
Name:	Cursor A FBC Control
ShortName:	CUR_FBC_CTL_A
Power:	Always on
Reset:	soft
Address:	710A0h-710A3h
Name:	Cursor B FBC Control
ShortName:	CUR_FBC_CTL_B
Power:	off/on
Reset:	soft
Address:	720A0h-720A3h
Name:	Cursor C FBC Control
ShortName:	CUR_FBC_CTL_C
Power:	off/on
Reset:	soft

DWord	Bit	Description
0	31	**Size Reduction Enable** This enables cursor size reduction logic. The cursor engine will fetch and display the programmed reduced number of lines, then go transparent for the rest of the frame.

Value	Name
0b	Disable
1b	Enable

CUR_FBC_CTL		
		Restriction Restriction : Cursor size reduction is not allowed with 2bpp cursor formats or cursor 180 degree rotation. The reduced scan lines field must be programmed with a valid value when cursor size reduction is enabled.
	30:8	**Reserved**
	7:0	**Reduced Scan Lines** This specifies the number of scan lines of cursor data to fetch and display when cursor size reduction is enabled. The value programmed is the size minus one. **Restriction** Restriction : The minimum size is 8 lines, programmed as 07h. The maximum size can not be greater than the normal size when size reduction is not enabled.

PLANE_SURFLIVE

PLANE_SURFLIVE	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	700ACh-700AFh
Name:	Cursor A Live Base Address
ShortName:	CUR_SURFLIVE_A
Power:	Always on
Reset:	soft
Address:	701ACh-701AFh
Name:	Primary A Live Base Address
ShortName:	PRI_SURFLIVE_A
Power:	Always on
Reset:	soft
Address:	701BCh-701BFh
Name:	Primary A Left Eye Live Base Address
ShortName:	PRI_LEFT_SURFLIVE_A
Power:	Always on
Reset:	soft
Address:	702ACh-702AFh
Name:	Sprite A Live Base Address
ShortName:	SPR_SURFLIVE_A
Power:	Always on
Reset:	soft
Address:	702BCh-702BFh
Name:	Sprite A Left Eye Live Base Address
ShortName:	SPR_LEFT_SURFLIVE_A
Power:	Always on
Reset:	soft
Address:	710ACh-710AFh

PLANE_SURFLIVE	
Name:	Cursor B Live Base Address
ShortName:	CUR_SURFLIVE_B
Power:	off/on
Reset:	soft
Address:	711ACh-711AFh
Name:	Primary B Live Base Address
ShortName:	PRI_SURFLIVE_B
Power:	off/on
Reset:	soft
Address:	711BCh-711BFh
Name:	Primary B Left Eye Live Base Address
ShortName:	PRI_LEFT_SURFLIVE_B
Power:	off/on
Reset:	soft
Address:	712ACh-712AFh
Name:	Sprite B Live Base Address
ShortName:	SPR_SURFLIVE_B
Power:	off/on
Reset:	soft
Address:	712BCh-712BFh
Name:	Sprite B Left Eye Live Base Address
ShortName:	SPR_LEFT_SURFLIVE_B
Power:	off/on
Reset:	soft
Address:	720ACh-720AFh
Name:	Cursor C Live Base Address
ShortName:	CUR_SURFLIVE_C
Power:	off/on
Reset:	soft
Address:	721ACh-721AFh
Name:	Primary C Live Base Address
ShortName:	PRI_SURFLIVE_C
Power:	off/on
Reset:	soft
Address:	721BCh-721BFh

PLANE_SURFLIVE

Name:	Primary C Left Eye Live Base Address
ShortName:	PRI_LEFT_SURFLIVE_C
Power:	off/on
Reset:	soft
Address:	722ACh-722AFh
Name:	Sprite C Live Base Address
ShortName:	SPR_SURFLIVE_C
Power:	off/on
Reset:	soft
Address:	722BCh-722BFh
Name:	Sprite C Left Eye Live Base Address
ShortName:	SPR_LEFT_SURFLIVE_C
Power:	off/on
Reset:	soft

There is one instance of this register for each plane.

DWord	Bit	Description
0	31:0	**Live Surface Base Address** This gives the live value of the surface base address as being currently used for the plane.

PRI_CTL

PRI_CTL	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to PRI_SURF or primary plane not enabled
Address:	70180h-70183h
Name:	Primary A Control
ShortName:	PRI_CTL_A
Power:	Always on
Reset:	soft
Address:	71180h-71183h
Name:	Primary B Control
ShortName:	PRI_CTL_B
Power:	off/on
Reset:	soft
Address:	72180h-72183h
Name:	Primary C Control
ShortName:	PRI_CTL_C
Power:	off/on
Reset:	soft

DWord	Bit	Description
0	31	**Primary Plane Enable** Format: Enable When this bit is set, the primary plane will generate pixels for display. When cleared to zero, primary plane memory fetches cease and plane output is transparent. 0b: Disable

1b	Enable

Note:	Project
Note: When RC6 and package C-states >= C3 are enabled, register 45280h bits 2:0 must be set to 111b the entire time that all display planes are disabled. That setting will impact power when planes are enabled, so the recommended sequence is to add programming to write register 45280h bits 2:0 = 111b just prior to disabling the last display plane, and write register 45280h bits 2:0 = 000b one vertical blank after the first display plane is enabled. First and last display plane refer to the entire set of planes, primary A/B/C, sprite A/B/C, and cursor A/B/C.	DevHSW:GT0:X0, DevHSW:GT3:A, DevHSW:GT3:B
Note: Register 45280h bits 2:0 must be set to 111b the entire time that any display planes (primary, sprite, cursor) are enabled on a pipe that is not enabled. That setting will impact power, so the recommended sequence is to write register 45280h bits 2:0 = 111b just prior to enabling the first display plane on the disabled pipe, then restore 45280h bits 2:0 one vertical blank after the pipe is enabled.	
Note: An alternative procedure is needed before enabling planes (primary, sprite, cursor) when transitioning from no pipes or a single pipe enabled to multiple pipes enabled. Refer to the Display Mode Set Sequence enable sequences for details.	

30

Gamma Enable

This bit enables pipe gamma correction for the plane pixel data.

Value	Name
0b	Disable
1b	Enable

29:26

Source Pixel Format

This field selects the source pixel format for the primary plane.
The 8-bpp indexed format will always use the pipe palette.
Before entering the blender, each source format is converted to the pipe pixel format.
Alpha values are ignored.

Value	Name	Description
0010b	8-bit Indexed	8-bit Indexed
0101b	16-bit BGRX 5:6:5	16-bit BGRX (5:6:5 MSB-R:G:B)
0110b	32-bit BGRX 8:8:8	32-bit BGRX (8:8:8:8 MSB-X:R:G:B)
1000b	32-bit RGBX 10:10:10	32-bit RGBX (2:10:10:10 MSB-X:B:G:R)
1001b	32-bit XR_BIAS RGBX 10:10:10	32-bit Extended Range Bias RGBX (2:10:10:10 MSB-X:B:G:R)
1010b	32-bit BGRX 10:10:10	32-bit BGRX (2:10:10:10 MSB-X:R:G:B)

1100b	64-bit RGBX FP	64-bit RGBX Floating Point(16:16:16:16 MSB-X:B:G:R)
1110b	32-bit RGBX 8:8:8	32-bit RGBX (8:8:8:8 MSB-X:B:G:R)
Others	Reserved	Reserved

Note:	Project
Note: When using the 64-bit format, the plane output on each color channel has one quarter amplitude. It can be brought up to full amplitude by using pipe gamma correction or pipe color space conversion to multiply the plane output by four.	DevHSW:GT0:X0, DevHSW:GT3:A

25 **Reserved**

24 **Pipe CSC Enable**

This bit enables pipe color space conversion for the plane pixel data.

Value	Name
0b	Disable
1b	Enable

23:16 **Reserved**

15 **180 Display Rotation**

This mode causes the plane image to be rotated 180 degrees.

Value	Name
0b	No rotation
1b	180 degree rotation

14 **Trickle Feed Enable**

Value	Name
0b	Enable
1b	Disable

Restriction
Restriction : Do not program this field to 1b.

13:11 **Reserved**

10 **Tiled Surface**

This bit indicates that the surface data is in tiled memory.
The tile pitch is specified in bytes in the plane stride register.
This bit may be updated through MMIO writes or through a command streamer initiated synchronous flip.

Value	Name
0b	Linear memory
1b	X-Tiled memory

PRI_CTL

		Restriction Restriction : Y tiling is not supported.
	9	**Async Address Update Enable** This bit will enable asynchronous updates of the plane surface address when written by MMIO (MMIO asynchronous flips). The surface address will change with the next plane TLB request or when start of vertical blank is reached. Updates during vertical blank may not complete until after the first few active lines are displayed. **Value** / **Name** / **Description** 0b / Sync / Surface Address MMIO writes will update synchronous to start of vertical blank 1b / Async / Surface Address MMIO writes will update asynchronously **Restriction** Restriction : No command streamer initiated flips to this plane are allowed when this bit is enabled. Each surface address write must be followed by a wait for flip done indication before writing the surface address register again. Linear memory does not support async updates.
	8	**Reserved** Format: MBZ
	7:6	**Reserved**
	5:0	**Reserved** Format: MBZ

PRI_STRIDE

PRI_STRIDE	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to PRI_SURF or primary plane not enabled
Address:	70188h-7018Bh
Name:	Primary A Stride
ShortName:	PRI_STRIDE_A
Power:	Always on
Reset:	soft
Address:	71188h-7118Bh
Name:	Primary B Stride
ShortName:	PRI_STRIDE_B
Power:	off/on
Reset:	soft
Address:	72188h-7218Bh
Name:	Primary C Stride
ShortName:	PRI_STRIDE_C
Power:	off/on
Reset:	soft

DWord	Bit	Description
0	31:16	**Reserved**
	15:6	**Stride** This field specifies the stride bits 15:6 for the plane. This value is used to determine the line to line increment for the plane data fetches. This field is programmed in units of 64 bytes. This register may be updated through MMIO writes or through command streamer initiated flips. **Restriction**

PRI_STRIDE		
		Restriction : When using linear memory, this must be at least 64 byte aligned. When using tiled memory, this must be at least 512 byte aligned. The stride is limited to a maximum of 32K bytes.
	5:0	**Reserved**

PRI_SURF

PRI_SURF	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of left or right eye vertical blank (selectable), pipe not enabled, or next plane line request if asynchronous flip
Address:	7019Ch-7019Fh
Name:	Primary A Base Address
ShortName:	PRI_SURF_A
Power:	Always on
Reset:	soft
Address:	7119Ch-7119Fh
Name:	Primary B Base Address
ShortName:	PRI_SURF_B
Power:	off/on
Reset:	soft
Address:	7219Ch-7219Fh
Name:	Primary C Base Address
ShortName:	PRI_SURF_C
Power:	off/on
Reset:	soft

Writes to this register arm primary registers for this pipe.
A write to this register is considered a flip and can cause a flip done interrupt if the interrupt registers are configured for that. The values in this register may be updated through MMIO writes or through command streamer initiated flips.
Synchronous updates (synchronous command streamer flips or synchronous MMIO writes) will update the plane surface values at the start of the next vertical blank.
Asynchronous updates (asynchronous command streamer flips or asynchronous MMIO writes) will update the plane surface values at the next TLB request or at the start of the next vertical blank.

Note:
After a command streamer initiated flip (MI_DISPLAY_FLIP) to this display plane, an MMIO read of this register will cause hardware to revert to using the last base address that was written to this register through MMIO,

effectively undoing the command streamer flip. To prevent this from causing an incorrect base address to be displayed, the first MMIO read of this register following a command streamer flip should be preceded by a MMIO write with the desired base address. The desired base address typically is the live base address found in the associated live base address register.

DWord	Bit	Description
0	31:12	**Surface Base Address** Format: GraphicsAddress[31:12] This address specifies the surface base address bits 31:12. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. **Note:** To prevent false VT-d type 6 errors, use 256KB address alignment and allocate an extra 128 Page Table Entries (PTEs) beyond the end of the displayed surface. Only the PTEs will be used, not the pages themselves. **Restriction** It must be at least 4KB aligned. When performing asynchronous flips and the display surface is in tiled memory, this address must be 256KB aligned.
	11:4	**Reserved**
	3	**Ring Flip Source** This bit indicates if the source of the last ring flip was CS or BCS. Value: 0b — Name: CS Value: 1b — Name: BCS
	2	**Reserved**
	1:0	**Reserved**

PRI_OFFSET

PRI_OFFSET	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled
Address:	701A4h-701A7h
Name:	Primary A Offset
ShortName:	PRI_OFFSET_A
Power:	Always on
Reset:	soft
Address:	711A4h-711A7h
Name:	Primary B Offset
ShortName:	PRI_OFFSET_B
Power:	off/on
Reset:	soft
Address:	721A4h-721A7h
Name:	Primary C Offset
ShortName:	PRI_OFFSET_C
Power:	off/on
Reset:	soft

This register specifies the panning for the plane surface.
The start position is specified in this register as a (x, y) offset from the beginning of the surface.
When performing 180 rotation, hardware will internally add the plane size to the offsets so the plane will start displaying from the bottom right corner of the image.

Restriction
Restriction : The plane size + offset must not exceed the maximum supported plane size.

DWord	Bit	Description
0	31:28	**Reserved** Format: MBZ
	27:16	**Start Y Position**

PRI_OFFSET		
		The vertical offset in lines of the beginning of the active display plane relative to the display surface.
	15:13	**Reserved** Format: MBZ
	12:0	**Start X Position** The horizontal offset in pixels of the beginning of the active display plane relative to the display surface.

PRI_LEFT_SURF

PRI_LEFT_SURF	
Register Space:	MMIO: 0/2/0
Project:	DevHSW
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of left or right eye vertical blank (selectable) or pipe not enabled; after armed
Double Buffer Armed By:	Write to PRI_SURF or primary plane not enabled
Address:	701B0h-701B3h
Name:	Primary A Left Eye Base Address
ShortName:	PRI_LEFT_SURF_A
Power:	Always on
Reset:	soft
Address:	711B0h-711B3h
Name:	Primary B Left Eye Base Address
ShortName:	PRI_LEFT_SURF_B
Power:	off/on
Reset:	soft
Address:	721B0h-721B3h
Name:	Primary C Left Eye Base Address
ShortName:	PRI_LEFT_SURF_C
Power:	off/on
Reset:	soft

Workaround

Workaround : After a command streamer initiated flip (MI_DISPLAY_FLIP) to this display plane, a MMIO read of this register will cause hardware to revert to using the last base address that was written to this register through MMIO, effectively undoing the command streamer flip. To prevent this from causing an incorrect base address to be displayed, the first MMIO read of this register following a command streamer flip should be preceded by a MMIO write with the desired base address. The desired base address typically is the live base address found in the associated live base address register.

Restriction

PRI_LEFT_SURF

Restriction : This register must be programmed with a valid address prior to enabling stereo 3D on this pipe.

Restriction : This register must not be updated asynchronously.

DWord	Bit	Description
0	31:12	**Left Surface Base Address** Format: GraphicsAddress[31:12] This address specifies the stereo 3D left eye surface base address bits 31:12. **Restriction** Restriction : This surface must have the same stride, tiling, and panning offset parameters as the right eye surface and meet all the same restrictions.
	11:0	**Reserved**

SPR_CTL

SPR_CTL	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to SPR_SURF or sprite not enabled

Address:	70280h-70283h
Name:	Sprite A Control
ShortName:	SPR_CTL_A
Power:	Always on
Reset:	soft

Address:	71280h-71283h
Name:	Sprite B Control
ShortName:	SPR_CTL_B
Power:	off/on
Reset:	soft

Address:	72280h-72283h
Name:	Sprite C Control
ShortName:	SPR_CTL_C
Power:	off/on
Reset:	soft

DWord	Bit	Description
0	31	**Sprite Enable** Format: Enable When this bit is set, the sprite plane will generate pixels for display. When cleared to zero, sprite plane memory fetches cease and sprite output is transparent. 0b – Disable 1b – Enable

SPR_CTL

Note:	Project
Note: When RC6 and package C-states >= C3 are enabled, register 45280h bits 2:0 must be set to 111b the entire time that all display planes are disabled. That setting will impact power when planes are enabled, so the recommended sequence is to add programming to write register 45280h bits 2:0 = 111b just prior to disabling the last display plane, and write register 45280h bits 2:0 = 000b one vertical blank after the first display plane is enabled. First and last display plane refer to the entire set of planes, primary A/B/C, sprite A/B/C, and cursor A/B/C.	DevHSW:GT0:X0, DevHSW:GT3:A, DevHSW:GT3:B
Note: Register 45280h bits 2:0 must be set to 111b the entire time that any display planes (primary, sprite, cursor) are enabled on a pipe that is not enabled. That setting will impact power, so the recommended sequence is to write register 45280h bits 2:0 = 111b just prior to enabling the first display plane on the disabled pipe, then restore 45280h bits 2:0 one vertical blank after the pipe is enabled.	
Note: An alternative procedure is needed before enabling planes (primary, sprite, cursor) when transitioning from no pipes or a single pipe enabled to multiple pipes enabled. Refer to the Display Mode Set Sequence enable sequences for details.	

30 **Pipe Gamma Enable**

This bit enables pipe gamma correction for the sprite pixel data.

Value	Name
0b	Disable
1b	Enable

29 **Reserved**

Format:	MBZ

28 **YUV Range Correction Disable**

Setting this bit disables the YUV range correction logic inside the sprite.
The range correction logic is used to expand the compressed range YUV to full range YUV.
The Y channel is expanded from the 8 bit +16 to +235 range to full range. The U and V channels are expanded from the 8 bit -112 to +112 range to full range.
Extended range values will be preserved after the expansion.
This bit has no effect on RGB source pixel formats since they automatically bypass range correction.

Value	Name
0b	Enable
1b	Disable

27:25 **Source Pixel Format**

This field selects the source pixel format for the sprite plane.

Before entering the blender, each source format is converted to the pipe pixel format.
Alpha values are ignored.
YUV 4:2:2 byte order is programmed separately.
YUV 4:4:4 byte order is not programmable.
RGB color order is programmed separately, except RGB XR_BIAS byte order is not programmable.

Value	Name	Description
000b	YUV 16-bit 4:2:2	YUV 16-bit 4:2:2 packed
001b	RGB 32-bit 2:10:10:10	RGB 32-bit 2:10:10:10
010b	RGB 32-bit 8:8:8:8	RGB 32-bit 8:8:8:8
011b	RGB 64-bit 16:16:16:16	RGB 64-bit 16:16:16:16 Floating Point
100b	YUV 32-bit 4:4:4	YUV 32-bit 4:4:4 packed (8:8:8:8 MSB-X:Y:U:V)
101b	RGB 32-bit XR_BIAS 10:10:10	RGB 32-bit Extended Range Bias RGBX (2:10:10:10 MSB-X:B:G:R)
Others	Reserved	Reserved

Note:	Project
Note: When using the 64-bit format, the sprite output on each color channel has one quarter amplitude. It can be brought up to full amplitude by using sprite internal gamma correction, pipe gamma correction, or pipe color space conversion to multiply the sprite output by four.	
Note: When using YUV formats and the sprite internal CSC is disabled, the sprite output will not have a 1/2 offset on the U and V channels. An offset on U and V channels is typically required by receivers. It can be added using the pipe CSC. If pipe CSC is already in use for RGB to YUV conversion, then the sprite internal CSC can be used to convert the sprite output to RGB, and the sprite can be sent through the pipe CSC, programmed for RGB to YUV conversion with pipe CSC post-offset of +1/2. If pipe CSC is not already in use, then the sprite output can be kept as YUV, and the sprite can be sent through the pipe CSC, programmed for 1:1 pass through with pipe CSC post-offset of +1/2. On later steppings a register bit is added to allow the 1/2 offset to be preserved within the sprite. See the note in the Sprite YUV to RGB CSC Dis field.	DevHSW:GT0:X0, DevHSW:GT3:A, DevHSW:GT3:B

24 **Pipe CSC Enable**
This bit enables pipe color space conversion for the plane pixel data.
This is separate from the color conversion logic within the sprite plane.

Value	Name
0b	Disable
1b	Enable

23 Reserved

Format:	MBZ

22 Sprite Source Key Enable

This bit enables source color keying. Sprite pixel values that match (within range) the key will become transparent.

Source key can not be enabled if destination key is enabled.

Value	Name
0b	Disable
1b	Enable

21 Reserved

Format:	MBZ

20 RGB Color Order

This field is used to select the color order when using RGB data formats, except RGB 32-bit XR_BIAS 10:10:10.

For other formats, this field is ignored.

Value	Name	Description
0b	BGRX	BGRX (MSB-X:R:G:B)
1b	RGBX	RGBX (MSB-X:B:G:R)

19 Sprite YUV to RGB CSC Dis

This bit controls the sprite internal YUV to RGB color space conversion.

RGB source pixel formats automatically bypass the sprite internal color space conversion.

Value	Name	Description
0b	Enable	YUV pixel data goes through the sprite color conversion
1b	Disable	YUV pixel data bypasses the sprite color conversion

Note:	Project
Note: When using YUV formats and the sprite internal CSC is disabled, the sprite output will default to not having a 1/2 offset on the U and V channels. An offset on U and V channels is typically required by receivers. The 1/2 offset can be preserved by setting register 420B0h (pipe A), 420B4h (pipe B), 420B8h (pipe C) bit 30 to 1b.	DevHSW, EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A), EXCLUDE(DevHSW:GT3:B)

18 Sprite YUV to RGB CSC Format

This bit specifies the source YUV format for the sprite internal YUV to RGB color space conversion operation.

This field is ignored when source data is RGB.

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Value	Name	Description
0b	BT.601	ITU-R Recommendation BT.601
1b	BT.709	ITU-R Recommendation BT.709

17:16 **YUV 422 Byte Order**

This field is used to select the byte order when using YUV 4:2:2 data formats.
For other formats, this field is ignored.

Value	Name	Description
00b	YUYV	YUYV (8:8:8:8 MSB-V:Y2:U:Y1)
01b	UYVY	UYVY (8:8:8:8 MSB-Y2:V:Y1:U)
10b	YVYU	YVYU (8:8:8:8 MSB-U:Y2:V:Y1)
11b	VYUY	VYUY (8:8:8:8 MSB-Y2:U:Y1:V)

15 **180 Display Rotation**

This mode causes the plane image to be rotated 180 degrees.
In addition to setting this bit, adjust the plane position to match the physical orientation of the display.

Value	Name
0b	No rotation
1b	180 degree rotation

14 **Trickle Feed Enable**

Value	Name
0b	Enable
1b	Disable

Restriction
Restriction : Do not program this field to 1b.

13 **Sprite Gamma Disable**

This bit controls sprite internal gamma correction.

Value	Name
1b	Disable
0b	Enable

12:11 **Reserved**

10 **Tiled Surface**

This bit indicates that the surface data is in tiled memory.
The tile pitch is specified in bytes in the stride register.
This bit may be updated through MMIO writes or through a command streamer initiated synchronous flip.

Value	Name
0b	Linear memory

SPR_CTL

		1b: X-Tiled memory
		Restriction: Restriction : Y tiling is not supported.
	9:8	**Reserved** Format: MBZ
	7:6	**Reserved**
	5:3	**Reserved** Format: MBZ
	2	**Sprite Destination Key** This bit enables the destination key function. When blending together sprite and primary planes, if the primary plane pixel matches the key value, then the sprite pixel is output, otherwise the primary pixel is output. 0b: Disable 1b: Enable **Restriction**: Restriction : Destination Key can not be enabled if source key is enabled.
	1:0	**Reserved** Format: MBZ

SPR_STRIDE

SPR_STRIDE	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to SPR_SURF or sprite not enabled
Address:	70288h-7028Bh
Name:	Sprite A Stride
ShortName:	SPR_STRIDE_A
Power:	Always on
Reset:	soft
Address:	71288h-7128Bh
Name:	Sprite B Stride
ShortName:	SPR_STRIDE_B
Power:	off/on
Reset:	soft
Address:	72288h-7228Bh
Name:	Sprite C Stride
ShortName:	SPR_STRIDE_C
Power:	off/on
Reset:	soft

DWord	Bit	Description
0	31:15	**Reserved**
	14:6	**Stride** This field specifies the stride bits 14:6 for the sprite. This value is used to determine the line to line increment for the sprite data fetches. This field is programmed in units of 64 bytes This register may be updated through MMIO writes or through a command streamer initiated synchronous flip. **Restriction**

SPR_STRIDE		
		Restriction : When using linear memory, this must be at least 64 byte aligned. When using tiled memory, this must be at least 512 byte aligned. The stride is limited to a maximum of 16K bytes.
	5:0	**Reserved**

SPR_POS

SPR_POS	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to SPR_SURF or sprite not enabled
Address:	7028Ch-7028Fh
Name:	Sprite A Position
ShortName:	SPR_POS_A
Power:	Always on
Reset:	soft
Address:	7128Ch-7128Fh
Name:	Sprite B Position
ShortName:	SPR_POS_B
Power:	off/on
Reset:	soft
Address:	7228Ch-7228Fh
Name:	Sprite C Position
ShortName:	SPR_POS_C
Power:	off/on
Reset:	soft

This register specifies the screen position of the sprite.
The origin of the sprite position is always the upper left corner of the display pipe source image area.
When performing 180 degree rotation, the sprite image is rotated by hardware, but the position is not, so it must be adjusted if it is desired to maintain the same apparent position on a physically rotated display.

Restriction
Restriction : The sprite must be completely contained within the pipe source area. Pipe source size >= sprite position + sprite size.

DWord	Bit	Description

SPR_POS		
0	31:28	**Reserved** Format: MBZ
	27:16	**Y Position** This specifies the vertical position of the sprite upper left corner in lines.
	15:13	**Reserved** Format: MBZ
	12:0	**X Position** This specifies the horizontal position of the sprite upper left corner in pixels.

SPR_SIZE

SPR_SIZE	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to SPR_SURF or sprite not enabled
Address:	70290h-70293h
Name:	Sprite A Size
ShortName:	SPR_SIZE_A
Power:	Always on
Reset:	soft
Address:	71290h-71293h
Name:	Sprite B Size
ShortName:	SPR_SIZE_B
Power:	off/on
Reset:	soft
Address:	72290h-72293h
Name:	Sprite C Size
ShortName:	SPR_SIZE_C
Power:	off/on
Reset:	soft
This register specifies the size of the sprite.	

Restriction
Restriction : The sprite must be completely contained within the pipe source area. Pipe source size >= sprite position + sprite size.

DWord	Bit	Description
0	31:28	**Reserved** Format: MBZ
	27:16	**Height**

<table>
<tr><th colspan="3">SPR_SIZE</th></tr>
<tr><td></td><td></td><td>This specifies the height of the sprite in lines.
The value in the register is the height minus one.
<table><tr><th>Restriction</th></tr><tr><td>Restriction : The height must be at least one line.</td></tr></table></td></tr>
<tr><td></td><td>15:13</td><td>Reserved
<table><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td></td><td>12:0</td><td>Width
This specifies the width of the sprite in pixels.
The value in the register is the width minus one.
<table><tr><th>Restriction</th></tr><tr><td>Restriction : The width (prior to minus one) must be even when a YUV 4:2:2 source pixel format is used.
The width must be at least one pixel.
This should be less than or equal to the stride in pixels.</td></tr></table></td></tr>
</table>

SPR_KEYVAL

SPR_KEYVAL	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled
Address:	70294h-70297h
Name:	Sprite A Key Color Value
ShortName:	SPR_KEYVAL_A
Power:	Always on
Reset:	soft
Address:	71294h-71297h
Name:	Sprite B Key Color Value
ShortName:	SPR_KEYVAL_B
Power:	off/on
Reset:	soft
Address:	72294h-72297h
Name:	Sprite C Key Color Value
ShortName:	SPR_KEYVAL_C
Power:	off/on
Reset:	soft

For source key when sprite source is YUV, this register specifies the source key YUV minimum color value to be used together with the YUV maximum color value and the color channel enable bits to determine if the sprite matches the source key color range.
For source key when sprite source is RGB, this register specifies the source key RGB color value to be used together with the color channel enable bits to determine if the sprite matches the source key color.
For destination key, this register specifies the destination key RGB color value to be used together with the RGB mask bits to determine if the primary matches the destination key color.
A key match can only occur for positive pixel values in the 0 to 1 range. Extended range pixel values will not match.

DWord	Bit	Description
0	31:24	**Reserved**

SPR_KEYVAL			
		Format:	MBZ
	23:16	**V R Min Dest Key Value** Specifies the color key minimum value for the sprite V channel source key, the compare value for sprite Red channel source key, or the compare value for the primary Red channel destination key.	
	15:8	**Y G Min Dest Key Value** Specifies the color key minimum value for the sprite Y channel source key, the compare value for sprite Green channel source key, or the compare value for the primary Green channel destination key.	
	7:0	**U B Min Dest Key Value** Specifies the color key minimum value for the sprite U channel source key, the compare value for sprite Blue channel source key, or the compare value for the primary Blue channel destination key.	

SPR_KEYMSK

SPR_KEYMSK	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled
Address:	70298h-7029Bh
Name:	Sprite A Key Mask
ShortName:	SPR_KEYMSK_A
Power:	Always on
Reset:	soft
Address:	71298h-7129Bh
Name:	Sprite B Key Mask
ShortName:	SPR_KEYMSK_B
Power:	off/on
Reset:	soft
Address:	72298h-7229Bh
Name:	Sprite C Key Mask
ShortName:	SPR_KEYMSK_C
Power:	off/on
Reset:	soft

For source key, this register specifies which channels to perform key color checking on. A disabled channel will match on the full range.

For destination key, this register specifies the key mask to be used with the color value bits to determine if the primary plane pixels match the key. A zero bit in the mask indicates that the corresponding bit match failure should be ignored when determining if the pixel matches.

Restriction
Restriction : Source key and destination key are mutually exclusive modes of operation, they can not be used simultaneously. For the function that is not enabled, the associated bits in this register should be programmed to zeroes.

DWord	Bit	Description

SPR_KEYMSK

0	31:27	**Reserved** Format: MBZ
	26	**V R Source Key Channel Enable** Enables the V/Red channel for source key color comparison. Value: 0b — Name: Disable Value: 1b — Name: Enable
	25	**Y G Source Key Channel Enable** Enables the Y/Green channel for source key color comparison. Value: 0b — Name: Disable Value: 1b — Name: Enable
	24	**U B Source Key Channel Enable** Enables the U/Blue channel for source key color comparison. Value: 0b — Name: Disable Value: 1b — Name: Enable
	23:16	**R Dest Key Mask Value** Specifies the destination color key mask for the Red channel
	15:8	**G Dest Key Mask Value** Specifies the destination color key mask for the Green channel
	7:0	**B Dest Key Mask Value** Specifies the destination color key mask for the Blue channel

SPR_SURF

SPR_SURF	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of left or right eye vertical blank (selectable) or pipe not enabled
Address:	7029Ch-7029Fh
Name:	Sprite A Base Address
ShortName:	SPR_SURF_A
Power:	Always on
Reset:	soft
Address:	7129Ch-7129Fh
Name:	Sprite B Base Address
ShortName:	SPR_SURF_B
Power:	off/on
Reset:	soft
Address:	7229Ch-7229Fh
Name:	Sprite C Base Address
ShortName:	SPR_SURF_C
Power:	off/on
Reset:	soft

Writes to this register arm sprite registers for this pipe.
A write to this register is considered a flip and can cause a flip done interrupt if the interrupt registers are configured for that. The values in this register may be updated through MMIO writes or through command streamer initiated flips.
Synchronous updates (synchronous command streamer flips or synchronous MMIO writes) will update the plane surface values at the start of the next vertical blank.

Note:
After a command streamer initiated flip (MI_DISPLAY_FLIP) to this display plane, an MMIO read of this register will cause hardware to revert to using the last base address that was written to this register through MMIO, effectively undoing the command streamer flip. To prevent this from causing an incorrect base address to be displayed, the first MMIO read of this register following a command streamer flip should be preceded by a

SPR_SURF

MMIO write with the desired base address. The desired base address typically is the live base address found in the associated live base address register.

Restriction
Restriction : Asynchronous updates are not supported by sprite.

DWord	Bit	Description
0	31:12	**Surface Base Address** Format: GraphicsAddress[31:12] This address specifies the surface base address bits 31:12. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. **Note:** To prevent false VT-d type 6 errors, use 128KB address alignment and allocate an extra 64 Page Table Entries (PTEs) beyond the end of the displayed surface. Only the PTEs will be used, not the pages themselves. **Restriction** Restriction : It must be at least 4KB aligned.
	11:4	**Reserved**
	3	**Ring Flip Source** This bit indicates if the source of the last ring flip was CS or BCS. Value: 0b — Name: CS Value: 1b — Name: BCS
	2	**Reserved**
	1:0	**Reserved**

SPR_KEYMAX

SPR_KEYMAX	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled
Address:	702A0h-702A3h
Name:	Sprite A Key Color Max
ShortName:	SPR_KEYMAX_A
Power:	Always on
Reset:	soft
Address:	712A0h-712A3h
Name:	Sprite B Key Color Max
ShortName:	SPR_KEYMAX_B
Power:	off/on
Reset:	soft
Address:	722A0h-722A3h
Name:	Sprite C Key Color Max
ShortName:	SPR_KEYMAX_C
Power:	off/on
Reset:	soft

For source key when sprite source is YUV, this register specifies the source key YUV maximum color value to be used together with the YUV minimum color value and the color channel enable bits to determine if the sprite matches the source key color range.

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:16	**V Source Key Max Value** Specifies the color key maximum value for the sprite V channel source key
	15:8	**Y Source Key Max Value** Specifies the color key maximum value for the sprite Y channel source key

SPR_KEYMAX		
	7:0	**U Source Key Max Value** Specifies the color key maximum value for the sprite U channel source key

SPR_OFFSET

SPR_OFFSET	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled
Address:	702A4h-702A7h
Name:	Sprite A Offset
ShortName:	SPR_OFFSET_A
Power:	Always on
Reset:	soft
Address:	712A4h-712A7h
Name:	Sprite B Offset
ShortName:	SPR_OFFSET_B
Power:	off/on
Reset:	soft
Address:	722A4h-722A7h
Name:	Sprite C Offset
ShortName:	SPR_OFFSET_C
Power:	off/on
Reset:	soft

This register specifies the panning for the sprite surface.
The start position is specified in this register as a (x, y) offset from the beginning of the surface.
When performing 180 rotation, hardware will internally add the sprite size to the offsets so the sprite will start displaying from the bottom right corner of the image.

Restriction
Restriction : The sprite size + offset must not exceed the maximum supported sprite size.

DWord	Bit	Description
0	31:28	**Reserved** Format: MBZ
	27:16	**Start Y Position**

SPR_OFFSET		
		The vertical offset in lines of the beginning of the active display plane relative to the display surface.
	15:13	**Reserved** Format: MBZ
	12:0	**Start X Position** The horizontal offset in pixels of the beginning of the active display plane relative to the display surface. **Restriction** Restriction : This offset must be even pixel aligned for YUV 4:2:2 formats.

SPR_LEFT_SURF

SPR_LEFT_SURF	
Register Space:	MMIO: 0/2/0
Project:	DevHSW
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of left or right eye vertical blank (selectable) or pipe not enabled; after armed
Double Buffer Armed By:	Write to SPR_SURF or sprite not enabled
Address:	702B0h-702B3h
Name:	Sprite A Left Eye Base Address
ShortName:	SPR_LEFT_SURF_A
Power:	Always on
Reset:	soft
Address:	712B0h-712B3h
Name:	Sprite B Left Eye Base Address
ShortName:	SPR_LEFT_SURF_B
Power:	off/on
Reset:	soft
Address:	722B0h-722B3h
Name:	Sprite C Left Eye Base Address
ShortName:	SPR_LEFT_SURF_C
Power:	off/on
Reset:	soft

Workaround

Workaround : After a command streamer initiated flip (MI_DISPLAY_FLIP) to this display plane, a MMIO read of this register will cause hardware to revert to using the last base address that was written to this register through MMIO, effectively undoing the command streamer flip. To prevent this from causing an incorrect base address to be displayed, the first MMIO read of this register following a command streamer flip should be preceded by a MMIO write with the desired base address. The desired base address typically is the live base address found in the associated live base address register.

Restriction

SPR_LEFT_SURF

Restriction : This register must be programmed with a valid address prior to enabling stereo 3D on this pipe.

DWord	Bit	Description
0	31:12	**Left Surface Base Address** Format: GraphicsAddress[31:12] This address specifies the stereo 3D left eye surface base address bits 31:12. **Restriction** Restriction : This surface must have the same stride, tiling, and panning offset parameters as the right eye surface and meet all the same restrictions.
	11:0	**Reserved**

SPR_GAMC

SPR_GAMC	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000
Access:	R/W
Size (in bits):	512
Address:	70400h-7043Fh
Name:	Sprite A Gamma Correction
ShortName:	SPR_GAMC_A_*
Power:	Always on
Reset:	soft
Address:	71400h-7143Fh
Name:	Sprite B Gamma Correction
ShortName:	SPR_GAMC_B_*
Power:	off/on
Reset:	soft
Address:	72400h-7243Fh
Name:	Sprite C Gamma Correction
ShortName:	SPR_GAMC_C_*
Power:	off/on
Reset:	soft

These registers are used to determine the characteristics of the gamma correction for the sprite pixel data pre-blending.
Additional gamma correction can be done in the display pipe gamma if desired.

The gamma correction curve is represented by specifying a set of gamma entry reference points spaced equally along the curve for values between -1 and 1.
For extended values there is an extended gamma entry reference point at the maximum alowed input value.

All input values are clamped to the greater than -3.0 and less than 3.0 range before the gamma calculation.

* For input values greater than or equal to 0 and less than 1.0, the input value is used to linearly interpolate between two adjacent points of the first 17 gamma entries to create the result value.

SPR_GAMC

The first 16 entries are stored in SPR_GAMC with 10 bits per color in an unsigned 0.10 format with 0 integer and 10 fractional.
The 17th entry is stored in the SPR_GAMC16 register with 11 bits per color in an unsigned 1.10 format with 1 integer and 10 fractional bits.

* For input values greater than or equal to 1.0 and less than 3.0, the input value is used to linearly interpolate between the 17th and 18th gamma entries to create the result value.
The 18th entry is stored in the SPR_GAMC17 register with 12 bits per color in an unsigned 2.10 format with 2 integer and 10 fractional bits.

* For negative input values, gamma is mirrored along the X-axis, giving the same result as positive input values, except for a negative sign
When gamma input may be negative, the first gamma point should be programmed to a value of 0.0 in order to have a symmetric mirroring.

Gamma correction can be enabled or disabled through the sprite control register.
See Pipe Gamma for an example gamma curve diagram.

Programming Notes

To program the gamma correction entries, calculate the desired gamma curve for inputs from 0 to 3.0.
For inputs of 0 to 1.0, multiply the input value by 16 to find the gamma entry number, then store the desired gamma result in that entry.
For inputs greater than 1.0 and less than or equal to 3.0, store the result for an input of 3.0 in the 18th gamma entry (SRP_GAMC17).

Restriction

Restriction : The gamma curve must be flat or increasing, never decreasing.
The gamma correction registers should only be updated when the sprite is off, otherwise screen artifacts may show temporarily.

DWord	Bit	Description
0	31:30	**Reserved** Format: MBZ
	29:0	**GAMC0** Default Value: 00000000h Format: SPR_GAMC REFERENCE POINT FORMAT
1	31:30	**Reserved** Format: MBZ
	29:0	**GAMC1** Default Value: 04010040h Format: SPR_GAMC REFERENCE POINT FORMAT
2	31:30	**Reserved**

SPR_GAMC

		Format: MBZ
	29:0	**GAMC2** Default Value: 08020080h Format: SPR_GAMC REFERENCE POINT FORMAT
3	31:30	**Reserved** Format: MBZ
	29:0	**GAMC3** Default Value: 0C0300C0h Format: SPR_GAMC REFERENCE POINT FORMAT
4	31:30	**Reserved** Format: MBZ
	29:0	**GAMC4** Default Value: 10040100h Format: SPR_GAMC REFERENCE POINT FORMAT
5	31:30	**Reserved** Format: MBZ
	29:0	**GAMC5** Default Value: 14050140h Format: SPR_GAMC REFERENCE POINT FORMAT
6	31:30	**Reserved** Format: MBZ
	29:0	**GAMC6** Default Value: 18060180h Format: SPR_GAMC REFERENCE POINT FORMAT
7	31:30	**Reserved** Format: MBZ
	29:0	**GAMC7** Default Value: 1C0701C0h Format: SPR_GAMC REFERENCE POINT FORMAT
8	31:30	**Reserved** Format: MBZ
	29:0	**GAMC8** Default Value: 20080200h Format: SPR_GAMC REFERENCE POINT FORMAT
9	31:30	**Reserved**

SPR_GAMC

		Format: MBZ
	29:0	**GAMC9** Default Value: 24090240h Format: SPR_GAMC REFERENCE POINT FORMAT
10	31:30	**Reserved** Format: MBZ
	29:0	**GAMC10** Default Value: 280A0280h Format: SPR_GAMC REFERENCE POINT FORMAT
11	31:30	**Reserved** Format: MBZ
	29:0	**GAMC11** Default Value: 2C0B02C0h Format: SPR_GAMC REFERENCE POINT FORMAT
12	31:30	**Reserved** Format: MBZ
	29:0	**GAMC12** Default Value: 300C0300h Format: SPR_GAMC REFERENCE POINT FORMAT
13	31:30	**Reserved** Format: MBZ
	29:0	**GAMC13** Default Value: 340D0340h Format: SPR_GAMC REFERENCE POINT FORMAT
14	31:30	**Reserved** Format: MBZ
	29:0	**GAMC14** Default Value: 380E0380h Format: SPR_GAMC REFERENCE POINT FORMAT
15	31:30	**Reserved** Format: MBZ
	29:0	**GAMC15** Default Value: 3C0F03C0h Format: SPR_GAMC REFERENCE POINT FORMAT

SPR_GAMC16

SPR_GAMC16	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000400, 0x00000400, 0x00000400
Access:	R/W
Size (in bits):	96
Address:	70440h-7044Bh
Name:	Sprite A Gamma Correction Point 16
ShortName:	SPR_GAMC16_A_*
Power:	Always on
Reset:	soft
Address:	71440h-7144Bh
Name:	Sprite B Gamma Correction Point 16
ShortName:	SPR_GAMC16_B_*
Power:	off/on
Reset:	soft
Address:	72440h-7244Bh
Name:	Sprite C Gamma Correction Point 16
ShortName:	SPR_GAMC16_C_*
Power:	off/on
Reset:	soft

These registers are used to determine the 17th reference point (point 16 when counting from 0) for sprite gamma correction.
The values are represented in an unsigned 1.10 format with 1 integer and 10 fractional bits.
See SPR_GAMC for sprite gamma programming information.

Restriction
Restriction : The value should always be programmed to be less than or equal to 1.0.

DWord	Bit	Description
0	31:11	**Reserved** Format: MBZ
	10:0	**GAMC16R** Default Value: 00000400h

SPR_GAMC16		
		Format: U1.10 This value specifies the 17th reference point that is used for the red color channel sprite gamma correction.
1	31:11	**Reserved** Format: MBZ
	10:0	**GAMC16G** Default Value: 00000400h Format: U1.10 This value specifies the 17th reference point that is used for the green color channel sprite gamma correction.
2	31:11	**Reserved** Format: MBZ
	10:0	**GAMC16B** Default Value: 00000400h Format: U1.10 This value specifies the 17th reference point that is used for the blue color channel sprite gamma correction.

SPR_GAMC17

SPR_GAMC17	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000C00, 0x00000C00, 0x00000C00
Access:	R/W
Size (in bits):	96
Address:	7044Ch-70457h
Name:	Sprite A Gamma Correction Point 17
ShortName:	SPR_GAMC17_A_*
Power:	Always on
Reset:	soft
Address:	7144Ch-71457h
Name:	Sprite B Gamma Correction Point 17
ShortName:	SPR_GAMC17_B_*
Power:	off/on
Reset:	soft
Address:	7244Ch-72457h
Name:	Sprite C Gamma Correction Point 17
ShortName:	SPR_GAMC17_C_*
Power:	off/on
Reset:	soft

These registers are used to determine the 18th reference point (point 17 when counting from 0) for sprite gamma correction.
The values are represented in an unsigned 2.10 format with 2 integer and 10 fractional bits.
See SPR_GAMC for sprite gamma programming information.

Restriction
Restriction : The value should always be programmed to be less than or equal to 3.0.

DWord	Bit	Description
0	31:12	**Reserved** Format: MBZ
	11:0	**GAMC17R** Default Value: 00000C00h

SPR_GAMC17		
		Format: U2.10 This value specifies the 18th reference point that is used for the red color channel sprite gamma correction.
1	31:12	**Reserved** Format: MBZ
	11:0	**GAMC17G** Default Value: 00000C00h Format: U2.10 This value specifies the 18th reference point that is used for the green color channel sprite gamma correction.
2	31:12	**Reserved** Format: MBZ
	11:0	**GAMC17B** Default Value: 00000C00h Format: U2.10 This value specifies the 18th reference point that is used for the blue color channel sprite gamma correction.

SFUSE_STRAP

SFUSE_STRAP

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	C2014h-C2017h
Name:	South Fuses and Straps
ShortName:	SFUSE_STRAP
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31:8	**Reserved**
	7	**Internal Display Capability Disable** This bit indicates whether the internal display capability is disabled. When disabled, PCH display hardware will prevent all PCH display functionality and put clocks inside the display partition into their lowest power state. The CPU display will not work due to GMBUS, DP AUX, panel power sequencing, and hot plugs being disabled. Must use external graphics for display. From dtfus_core_capintdispdis. **Value** / **Name** 0b — Enable 1b — Disable
	6	**CRT DAC Capability Disable** Project: DevLPT:H This bit indicates whether the CRT DAC (VGA port) display capability is disabled. When disabled, PCH display hardware will prevent the CRT DAC (VGA port) DAC_CTL enable register bit from being set to 1b, force pcdclk to come from raw clock, and force the pixel clock to be gated off. Other ports on the CPU display will continue to work. From dtfus_core_capintgfxdis. **Value** / **Name** 0b — Enable 1b — Disable
	6	**Reserved**

SFUSE_STRAP

	Project:	DevLPT:LP

5 Reserved

Format:	MBZ

4 Lane Reversal Strap

Project:	DevLPT:H

This bit indicates the state of the DMI/FDI lane reversal strap.

Value	Name
0b	Not Reversed
1b	Reversed

4 Reserved

Project:	DevLPT:LP

3 Reserved

Format:	MBZ

2 Digital Port B Present Strap

This bit indicates the state of the digital port B present strap.
The strap is set if DDPB_CTRLDATA pin is 1b at rising edge of PCH_PWROK.

Value	Name
0b	Not Present
1b	Present

1 Digital Port C Present Strap

This bit indicates the state of the digital port C present strap.
The strap is set if DDPC_CTRLDATA pin is 1b at rising edge of PCH_PWROK.

Value	Name
0b	Not Present
1b	Present

0 Reserved

Project:	DevLPT:LP

0 Digital Port D Present Strap

Project:	DevLPT:H

This bit indicates the state of the digital port D present strap.
The strap is set if DDPD_CTRLDATA pin is 1b at rising edge of PCH_PWROK.

Value	Name
0b	Not Present
1b	Present

South Display Engine Interrupt Bit Definition

South Display Engine Interrupt Bit Definition

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32

Address:	C4000h-C400Fh
Name:	South Display Engine Interrupts
ShortName:	SDE_INTERRUPT
Power:	Always on
Reset:	soft

South Display Engine (SDE) interrupt bits come from events within the south display engine.
The SDE_IIR bits are ORed together to generate the South/PCH Display Interrupt Event which will appear in the North Display Engine Interrupt Control Registers.
Only the rising edge of the PCH Display interrupt will cause the North Display IIR (DEIIR) PCH Display Interrupt event bit to be set, so all PCH Display Interrupts, including back to back interrupts, must be cleared in the SDEIIR before a new PCH Display Interrupt can cause the DEIIR to be set.
The South Display Engine Interrupt Control Registers all share the same bit definitions from this table.

DWord	Bit	Description
0	31:28	**Reserved** Format: MBZ
	27	**AUX Channel D** This is an active high pulse on the AUX D done event
	26	**AUX Channel C** This is an active high pulse on the AUX C done event
	25	**AUX Channel B** This is an active high pulse on the AUX B done event
	24	**Reserved** Format: MBZ
	23	**DisplayPort/HDMI/DVI D Hotplug** The ISR is an active high level representing the Digital Port D hotplug line when the Digital Port D hotplug detect input is enabled. The unmasked IIR is set on either a short or long pulse detection status in the Digital Port Hot Plug Control Register. Restriction : The DDI D HPD pin is not connected in the package for LP parts — Project: DevLPT:LP

South Display Engine Interrupt Bit Definition

		and should not be used.
	22	**DisplayPort/HDMI/DVI C Hotplug** The ISR is an active high level representing the Digital Port C hotplug line when the Digital Port C hotplug detect input is enabled. The unmasked IIR is set on either a short or long pulse detection status in the Digital Port Hot Plug Control Register.
	21	**DisplayPort/HDMI/DVI B Hotplug** The ISR is an active high level representing the Digital Port B hotplug line when the Digital Port B hotplug detect input is enabled. The unmasked IIR is set on either a short or long pulse detection status in the Digital Port Hot Plug Control Register.
	20	**Reserved** Format: MBZ
	19	**CRT Hotplug** Project: DevLPT:H The ISR is an active high level representing the ORed together blue and green channel detection status as of the last detection cycle. The unmasked IIR is set on the rising or falling edges of the blue or green channel detection status in the Analog Port CRT DAC Control Register.
	19	**Reserved** Project: DevLPT:LP Format: MBZ
	18	**Reserved** Format: MBZ
	17	**Gmbus** This is an active high pulse when any of the events unmasked events in GMBUS4 Interrupt Mask register occur.
	16	**South Error Interrupts Combined** This is an active high level while any of the South Error Interrupt bits are set.
	15	**GTC PCH Interrupts Combined** The ISR is an active high level while any of the GTC_PCH_IIR bits are set.
	14:1	**Reserved** Format: MBZ
	0	**FDI RX Interrupts Combined A** Project: DevLPT:H This is an active high level while any of the FDI_RX_ISR bits are set for transcoder A.
	0	**Reserved**

South Display Engine Interrupt Bit Definition

Project:	DevLPT:LP
Format:	MBZ

SHOTPLUG_CTL

SHOTPLUG_CTL

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	C4030h-C4033h
Name:	South Hot Plug Control
ShortName:	SHOTPLUG_CTL
Power:	Always on
Reset:	soft

Description	Project
The DDI-A HPD Input Enable is found in the North Display Engine registers.	DevLPT:H

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28	**DDI A HPD Input Enable** Project: DevLPT:LP Controls the state of the HPD buffer for the digital port A. The HPD status is found in the North Display Engine registers. Value / Name / Description: 0b / Disable / Buffer disabled 1b / Enable / Buffer enabled.
	28	**Reserved** Project: DevLPT:H Format: MBZ
	27:21	**Reserved** Format: MBZ
	20	**DDI D HPD Input Enable** Controls the state of the HPD buffer for the digital port D. Value / Name / Description: 0b / Disable / Buffer disabled

SHOTPLUG_CTL

1b	Enable	Buffer enabled.

Restriction	Project
Restriction : On LP parts the DDI D HPD should not be used as the pins are not connected in the package.	DevLPT:LP

19:18 **Reserved**

Format:	MBZ

17:16 **DDI D HPD Status**

Access:	R/WC

This field reflects the hot plug detect status on port D. This bit is used for either monitor hotplug/unplug or for notification of a sink event.
When HPD input is enabled and either a long or short pulse is detected, one of these bits will set and the hotplug IIR will be set (if unmasked in the IMR).
The hotplug ISR gives the live state of the HPD pin. Due to the possibility of back to back HPD events it is recommended that software filters the value read from the ISR.
These are sticky bits, cleared by writing 1s to both of them.
The short pulse duration is programmed in SHPD_PULSE_CNT.

Value	Name	Description
00b	No Detect	Digital port hot plug event not detected
X1b	Short Detect	Digital port short pulse hot plug event detected
1Xb	Long Detect	Digital port long pulse hot plug event detected

Restriction	Project
Restriction : On LP parts the DDI D HPD should not be used as the pins are not connected in the package.	DevLPT:LP

15:13 **Reserved**

Format:	MBZ

12 **DDI C HPD Input Enable**

Controls the state of the HPD buffer for the digital port C.

Value	Name	Description
0b	Disable	Buffer disabled
1b	Enable	Buffer enabled.

11:10 **Reserved**

Format:	MBZ

9:8 **DDI C HPD Status**

Access:	R/WC

This field reflects the hot plug detect status on port C. This bit is used for either monitor hotplug/unplug or for notification of a sink event.
When HPD input is enabled and either a long or short pulse is detected, one of these bits will set

and the hotplug IIR will be set (if unmasked in the IMR).
The hotplug ISR gives the live state of the HPD pin. Due to the possibility of back to back HPD events it is recommended that software filters the value read from the ISR.
These are sticky bits, cleared by writing 1s to both of them.
The short pulse duration is programmed in SHPD_PULSE_CNT.

Value	Name	Description
00b	No Detect	Digital port hot plug event not detected
X1b	Short Detect	Digital port short pulse hot plug event detected
1Xb	Long Detect	Digital port long pulse hot plug event detected

7:5 **Reserved**

Format:	MBZ

4 **DDI B HPD Input Enable**

Controls the state of the HPD buffer for the digital port B.

Value	Name	Description
0b	Disable	Buffer disabled
1b	Enable	Buffer enabled.

3:2 **Reserved**

Format:	MBZ

1:0 **DDI B HPD Status**

Access:	R/WC

This field reflects the hot plug detect status on port B. This bit is used for either monitor hotplug/unplug or for notification of a sink event.
When HPD input is enabled and either a long or short pulse is detected, one of these bits will set and the hotplug IIR will be set (if unmasked in the IMR).
The hotplug ISR gives the live state of the HPD pin. Due to the possibility of back to back HPD events it is recommended that software filters the value read from the ISR.
These are sticky bits, cleared by writing 1s to both of them.
The short pulse duration is programmed in SHPD_PULSE_CNT.

Value	Name	Description
00b	No Detect	Digital port hot plug event not detected
X1b	Short Detect	Digital port short pulse hot plug event detected
1Xb	Long Detect	Digital port long pulse hot plug event detected

SHPD_PULSE_CNT

SHPD_PULSE_CNT	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x000007CE
Access:	R/W
Size (in bits):	32
Address:	C4034h-C4037h
Name:	South HPD Pulse count DDI B
ShortName:	SHPD_PULSE_CNT
Power:	Always on
Reset:	global
Address:	C4044h-C4047h
Name:	South HPD Pulse count DDI C
ShortName:	SHPD_PULSE_CNT_C
Valid Projects:	[DevLPT:LP]
Power:	Always on
Reset:	global
Address:	C4048h-C404Bh
Name:	South HPD Pulse count DDI D
ShortName:	SHPD_PULSE_CNT_D
Valid Projects:	[DevLPT:LP]
Power:	Always on
Reset:	global

Description	Project
This register must be programmed properly before enabling DDI HPD detection. This register is on the chip reset, not the FLR or display debug reset.	
There is one instance of this register per DDI B, C, D.	DevLPT:LP
There is one instance of this register that applies to all DDI B, C, D.	DevLPT:H

DWord	Bit	Description	
0	31:17	**Reserved**	
		Format:	MBZ
	16:0	**ShortPulse Count**	

SHPD_PULSE_CNT

Default Value:	007CEh 2000 microseconds

Description	Project
These bits define the duration of the pulse defined as a short pulse for DDI HPD. The value is the number of microseconds minus 2. The default value of 0x007CE = 2,000 microseconds (2 milliseconds) is for Displayport. For HDMI or DVI it should be programmed to 0x1869E = 100,000 microseconds (100 milliseconds).	
0xC2004 bits 10:8 allow pulse length to be overriden to 100ms for individual DDIs B/C/D	DevLPT:H

SHPD_FILTER_CNT

SHPD_FILTER_CNT	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x000001F2
Access:	R/W
Size (in bits):	32
Address:	C4038h-C403Bh
Name:	South HPD Filter count
ShortName:	SHPD_FILTER_CNT
Power:	Always on
Reset:	global

This register must be programmed properly before enabling DDI HPD detection.
This register is on the chip reset, not the FLR or display debug reset.

DWord	Bit	Description
0	31:17	**Reserved** Format: MBZ
	16:0	**HPD Filter Count** Default Value: 001F2h 500 microseconds These bits define the duration of the filter for DDI HPD. The value is the number of microseconds minus 2. The default value of 0x001F2 = 500 microseconds

SERR_INT

SERR_INT

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/WC
Size (in bits):	32
Address:	C4040h-C4043h
Name:	South Error Interrupts
ShortName:	SERR_INT
Power:	Always on
Reset:	soft

These are sticky bits, cleared by writing 1 to them. All the South Error Interrupt bits are ORed together to go to the South Display Engine ISR Error Interrupts Combined bit.

DWord	Bit	Description
0	31	**South Poison Status** This bit is set upon receiving the poison message. Value / Name / Description: 0b / Not Detected / Event not detected 1b / Detected / Event detected
	30:1	**Reserved**
	0	**Reserved** Project: DevLPT:H
	0	**Reserved** Project: DevLPT:LP Format: MBZ

GPIO_CTL

GPIO_CTL	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000808
Access:	R/W
Size (in bits):	32
Address:	C5010h-C5013h
Name:	GPIO Control 0
ShortName:	GPIO_CTL_0
Valid Projects:	[DevLPT:H]
Power:	Always on
Reset:	soft
Address:	C501Ch-C501Fh
Name:	GPIO Control 3
ShortName:	GPIO_CTL_3
Power:	Always on
Reset:	soft
Address:	C5020h-C5023h
Name:	GPIO Control 4
ShortName:	GPIO_CTL_4
Power:	Always on
Reset:	soft
Address:	C5024h-C5027h
Name:	GPIO Control 5
ShortName:	GPIO_CTL_5
Valid Projects:	[DevLPT:H]
Power:	Always on
Reset:	soft
The register controls a pair of pins that can be used for general purpose control, but usually is designated for specific functions according to the requirements of the device and the system that the device is in. Each pin of the two pin pair is designated as a clock or data for descriptive purposes. See the table at the beginning of this section to determine which pins/registers are supported and their intended functions. Board design variations are possible and would affect the usage of these pins.	

GPIO_CTL

There are multiple instances of this register to support each of the GPIO pin pairs.

DWord	Bit	Description
0	31:13	**Reserved** Format: MBZ
	12	**GPIO Data In** Default Value: Ub Undefined (read only depends on I/O pin) Access: RO This is the value that is sampled on the GPIO_Data pin as an input. This bit is undefined at reset.
	11	**GPIO Data Value** Default Value: 1b Access: R/W This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if GPIO DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Data DIRECTION VALUE contains a value that will configure the pin as an output. The default of '1' mimics the I2C external pull-ups.
	10	**GPIO Data Mask** Access: WO This is a mask bit to determine whether the GPIO DATA VALUE bit should be written into the register. This value is not stored and when read returns 0. **Value** / **Name** / **Description** 0b / No Write / Do NOT write GPIO Data Value bit 1b / Write / Write GPIO Data Value bit.
	9	**GPIO Data Direction Value** Access: R/W This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if GPIO Data DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO DATA VALUE bit. **Value** / **Name** / **Description** 0b / Input / Pin is configured as an input 1b / Output / Pin is configured as an output
	8	**GPIO Data Direction Mask** Access: WO This is a mask bit to determine whether the GPIO Data DIRECTION VALUE bit should be written into the register. This value is not stored and when read always returns 0.

GPIO_CTL

Value	Name	Description
0b	No Write	Do NOT write GPIO Data Direction Value bit
1b	Write	Write GPIO Data Direction Value bit

7:5 **Reserved**

Format:	MBZ

4 **GPIO Clock Data In**

Default Value:	Ub Undefined (read only depends on I/O pin)
Access:	RO

This is the value that is sampled on the GPIO Clock pin as an input.
This bit is undefined at reset.

3 **GPIO Clock Data Value**

Default Value:	1b
Access:	R/W

This is the value that should be place on the GPIO Clk pin as an output.
This value is only written into the register if GPIO Clock DATA MASK is also asserted.
The value will appear on the pin if this data value is actually written to this register and the GPIO Clock DIRECTION VALUE contains a value that will configure the pin as an output.
The default of '1' mimics the I2C external pull-ups.

2 **GPIO Clock Data Mask**

Access:	WO

This is a mask bit to determine whether the GPIO Clock DATA VALUE bit should be written into the register. This value is not stored and when read always returns 0.

Value	Name	Description
0b	No Write	Do NOT write GPIO Clock Data Value bit
1b	Write	Write GPIO Clock Data Value bit

1 **GPIO Clock Direction Value**

Access:	R/W

This is the value that should be used to define the output enable of the GPIO Clock pin.
This value is only written into the register if GPIO Clock DIRECTION MASK is also asserted.
The value that will appear on the pin is defined by what is in the register for the GPIO Clock DATA VALUE bit.

Value	Name	Description
0b	Input	Pin is configured as an input and the output driver is set to tri-state
1b	Output	Pin is configured as an output

0 **GPIO Clock Direction Mask**

Access:	WO

<table>
<tr><th colspan="3">GPIO_CTL</th></tr>
<tr><td></td><td></td><td>This is a mask bit to determine whether the GPIO Clock DIRECTION VALUE bit should be written into the register. This value is not stored and when read returns 0.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th></tr>
<tr><td>0b</td><td>No Update</td><td>Do NOT write GPIO Clock Direction Value bit</td></tr>
<tr><td>1b</td><td>Update</td><td>Write GPIO Clock Direction Value bit</td></tr>
</table></td></tr>
</table>

GMBUS0

GMBUS0

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	C5100h-C5103h
Name:	GMBUS0 Clock/Port Select
ShortName:	GMBUS0
Power:	Always on
Reset:	soft

The GMBUS0 register controls the clock rate of the serial bus and the device the controller is connected to.
This register should be configured before the first data valid bit is set.

DWord	Bit	Description
0	31:12	**Reserved** Format: MBZ
	11	**Reserved**
	10:8	**GMBUS Rate Select** These two bits select the rate that the GMBUS will run at. It also defines the AC timing parameters used. It should only be changed between transfers when the GMBUS is idle. Value / Name / Description: 000b / 100 KHz / 100 KHz 001b / 50 KHz / 50 KHz Others / Reserved / Reserved
	7:3	**Reserved** Format: MBZ
	2:0	**Pin Pair Select** This field selects a GMBUS pin pair for use in the GMBUS communication. Use the GPIO Pin Usage table above to determine which pin pairs are available for a particular device and the intended function of that pin pair. Note that it is not a straight forward mapping of port numbers to pair select numbers. Value / Name / Description / Project: 000b / None / None (Disabled) /

GMBUS0					
		010b	DAC DDC	DDC for Analog monitor (VGA/CRT DAC)	DevLPT:H
		100b	DDIC	DDC for HDMI/DVI port C	
		101b	DDIB	DDC for HDMI/DVI port B	
		110b	DDID	DDC for HDMI/DVI port D	DevLPT:H
		111b	Reserved	Reserved	

GMBUS1

GMBUS1

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W Protect
Size (in bits):	32
Address:	C5104h-C5107h
Name:	GMBUS1 Command/Status
ShortName:	GMBUS1
Power:	Always on
Reset:	soft

This register lets the software indicate to the GMBUS controller the slave device address, register index, and indicate when the data write is complete.
When the SW_CLR_INT bit is asserted, all writes to the GMBUS2, GMBUS3, and GMBUS4 registers are discarded. The GMBUS1 register writes to any other bit except the SW_CLR_INT are also lost. Reads to these registers always work normally regardless of the state of the SW_CLR_INT bit.

Note:

Note: On ULT systems with ISCLK PLL shutdown enabled, display register C2020h bit 12 must be set to 1b before sending a GMBUS transaction. If no other feature requires register C2020h bit 12, it can be cleared to 0b after the GMBUS transaction is complete. To save power, register C2020h bit 12 must be cleared to 0b when internal graphics is put in the D3 device power state.

DWord	Bit	Description
0	31	**Software Clear Interrupt** Access: R/W (SW_CLR_INT) This bit must be clear for normal operation. Setting the bit then clearing it acts as local reset to the GMBUS controller. This bit is commonly used by software to clear a BUS_ERROR when a slave device delivers a NACK.

Value	Name	Description
0b	Clear HW_RDY	If this bit is written as a zero when its current state is a one, will clear the HW_RDY bit and allows register writes to be accepted to the GMBUS registers (Write Protect Off). This bit is cleared to zero when an event causes the HW_RDY bit transition to occur.
1b	Assert	Asserted by software after servicing the GMBUS interrupt.

GMBUS1

	HW_RDY	Setting this bit causes the INT status bit to be cleared. Setting (1) this bit also asserts the HW_RDY bit (until this bit is written with a 0). When this bit is set, no writes to GMBUS registers will cause the contents to change with the exception of this bit which can be written.

30 **Software Ready**

(SW_RDY) Data handshake bit used in conjunction with HW_RDY bit.

Value	Name	Description
0b	De-Assert	De-asserted via the assertion event for HW_RDY bit
1b	SW Assert	When asserted by software, results in de-assertion of HW_RDY bit

29 **Enable Timeout**

(ENT) Enables timeout for slave response.

When this bit is enabled and the slave device response has exceeded the timeout period, the GMBUS Slave Stall Timeout Error interrupt bit is set.

Value	Name	Description
0b	Disable	Disable timeout counter
1b	Enable	Enable timeout counter

28 **Reserved**

Format:	MBZ

27:25 **Bus Cycle Select**

GMBUS cycle will always consist of a START followed by Slave Address, followed by an optional read or write data phase.

A read cycle with an index will consist of a START followed by a Slave Address a WRITE indication and the INDEX and then a RESTART with a Slave Address and an optional read data phase.

The GMBUS cycle will terminate either with a STOP or by entering a wait state. The WAIT state is exited by generating a STOP or by starting another GMBUS cycle.

This can only cause a STOP to be generated if a GMBUS cycle is generated, the GMBUS is currently in a data phase, or it is in a WAIT phase:

Note that the three bits can be decoded as follows:

27 = STOP generated

26 = INDEX used

25 = Cycle ends in a WAIT

Value	Name	Description
000b	No cycle	No GMBUS cycle is generated
001b	No Index, No Stop, Wait	GMBUS cycle is generated without an INDEX, with no STOP, and ends with a WAIT
010b	Reserved	Reserved
011b	Index, No Stop, Wait	GMBUS cycle is generated with an INDEX, with no STOP, and ends with a WAIT
100b	Gen Stop	Generates a STOP if currently in a WAIT or after the completion of

GMBUS1

		the current byte if active
101b	No Index, Stop	GMBUS cycle is generated without an INDEX and with a STOP
110b	Reserved	Reserved
111b	Index, Stop	GMBUS cycle is generated with an INDEX and with a STOP

24:16 Total Byte Count

Format:	MBZ

This determines the total number of bytes to be transferred during the DATA phase of a GMBUS cycle.
The DATA phase can be prematurely terminated by generating a STOP while in the DATA phase (see Bus Cycle Select).
Do not change the value of this field during GMBUS cycles transactions.

15:8 8 bit Slave Register Index

(INDEX) This field specifies the 8-bits of index to be used for the generated bus write transaction or the index used for the WRITE portion of the WRITE/READ pair.
It only has an effect if the enable Index bit is set.
Do not change this field during a GMBUS transaction.

7:0 Slave Address And Direction

Bits 7:1 = 7-bit GMBUS Slave Address (SADDR): When a GMBUS cycle is to be generated using the Bus Cycle Select field, this field specifies the value of the slave address that is to be sent out.
For use with 10-bit slave address devices, set this value to 11110XXb (where the last two bits (XX) are the two MSBs of the 10-bit address) and the slave direction bit to a write. This is followed by the first data byte being the 8 LSBs of the 10-bit slave address.

Bit 0 = Slave Direction Bit: When a GMBUS cycle is to be generated based on the Bus Cycle Select, this bit determines if the operation will be a read or a write. A read operation with the index enabled will perform a write with just the index followed by a re-start and a read. A 1 indicates that a Read from the slave device operation is to be performed. A 0 indicates that a Write to the slave device operation is to be performed.

Value	Name	Description
00000001b	General	General Call Address
00000000b	Start	Start Bye
0000001Xb	CBUS	CBUS Address
11110XXXb	10-bit	10-Bit addressing
Others	Reserved	Reserved

GMBUS2

GMBUS2

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000800
Access:	R/W Protect
Size (in bits):	32
Address:	C5108h-C510Bh
Name:	GMBUS2 Status
ShortName:	GMBUS2
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15	**INUSE** Software wishing to arbitrate for the GMBUS resource can poll this bit until it reads a zero and will then own usage of the GMBUS controller. This bit has no effect on the hardware, and is only used as semaphore among various independent software threads that don't know how to synchronize their use of this resource that may need to use the GMBUS logic. Writing a one to this bit is software's indication that the software use of this resource is now terminated and it is available for other clients.
	14	**Hardware Wait Phase** Access: RO (HW_WAIT_PHASE) Once in a WAIT_PHASE, the software can now choose to generate a STOP cycle or a repeated start (RESTART) cycle followed by another GMBUS transaction on the GMBUS.

Value	Name	Description
0b	GMBUS is Acquired	Read operation that contains a zero in this bit position indicates that the GMBUS engine is now acquired and the subsequent reads of this register will now have this bit set. Writing a 0 to this bit has no effect.
1b	GMBUS in Use	Read operation that contains a one for this bit indicates that the GMBUS is currently allocated to someone else and "In use". Once set, a write of a 1 to this bit indicates that the software has relinquished the GMBUS resource and will reset the value of this bit to a 0.

GMBUS2

Value	Name	Description
0b	No Wait	The GMBUS engine is not in a wait phase.
1b	Wait	Set when GMBUS engine is in wait phase. Wait phase is entered at the end of the current transaction when that transaction is selected not to terminate with a STOP.

13 **Slave Stall Timeout Error**

Access:	RO

This bit indicates that a slave stall timeout has occurred. It is tied to the Enable Timeout (ENT) bit.

Value	Name	Description
0b	No Slave Timeout	No slave timeout has occurred
1b	Slave Timeout	A slave acknowledge timeout has occurred

12 **GMBUS Interrupt Status**

Access:	RO

This bit indicates that an event that causes a GMBUS interrupt has occurred.

Value	Name	Description
0b	No Interrupt	The conditions that could cause a GMBUS interrupt have not occurred or this bit has been cleared by software assertion of the SW_CLR_INT bit.
1b	Interrupt	GMBUS interrupt event occurred. This interrupt must have been one of the types enabled in the GMBUS4 register

11 **Hardware Ready**

Access:	RO

(HW_RDY) This provides a method of detecting when the current software client routine can proceed with the next step in a sequence of GMBUS operations.
This data handshake bit is used in conjunction with the SW_RDY bit.
When this bit is asserted by the GMBUS controller, it results in the de-assertion of the SW_RDY bit.
This bit resumes to normal operation when the SW_CLR_INT bit is written to a 0.

Value	Name	Description
0b	0	Condition required for assertion has not occurred or when this bit is a one and: - SW_RDY bit has been asserted - During a GMBUS read transaction, after the each read of the data register - During a GMBUS write transaction, after each write of the data register - SW_CLR_INT bit has been cleared
1b	1 **[Default]**	This bit is asserted under the following conditions: - After a reset or when the transaction is aborted by the setting of the SW_CLR_INT bit - When an active GMBUS cycle has terminated with a STOP - When during a GMBUS write transaction, the data register needs and can

GMBUS2

		accept another four bytes of data - During a GMBUS read transaction, this bit is asserted when the data register has four bytes of new data or the read transaction DATA phase is complete and the data register contains the last few bytes of the read data

10 NAK Indicator

Access:	RO

Value	Name	Description
0b	No bus error	No bus error has been detected or SW_CLR_INT has been written as a zero since the last bus error
1b	No Ack	Set by hardware if any expected device acknowledge is not received from the slave within the timeout

9 GMBUS Active

Access:	RO

(GA) This is a status bit that indicates whether the GMBUS controller is in an IDLE state or not.

Value	Name	Description
0b	Idle	The GMBUS controller is currently IDLE
1b	Active	This indicates that the bus is in START, ADDRESS, INDEX, DATA, WAIT, or STOP Phase. Set when GMBUS hardware is not IDLE.

8:0 Current Byte Count

Access:	RO

Can be used to determine the number of bytes currently transmitted/received by the GMBUS controller hardware.

Hardware sets it to zero at the start of a GMBUS transaction data transfer and incremented after the completion of each byte of the data phase.

Note that because reads have internal storage, the byte count on a read operation may be ahead of the data that has been accepted from the data register.

GMBUS3

GMBUS3	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W Protect
Size (in bits):	32
Double Buffer Update Point:	HW_RDY
Address:	C510Ch-C510Fh
Name:	GMBUS3 Data Buffer
ShortName:	GMBUS3
Power:	Always on
Reset:	soft

This is the data read/write register. This register is double buffered.
Bit 0 is the first bit sent or read, bit 7 is the 8th bit sent or read, all the way through bit 31 being the 32nd bit sent or read.
For GMBUS write operations with a non-zero byte count, this register should be written with the data before the GMBUS cycle is initiated.
For byte counts that are greater than four bytes, this register will be written with subsequent data only after the HW_RDY status bit is set indicating that the register is now ready for additional data.
For GMBUS read operations, software should wait until the HW_RDY bit indicates that the register contains the next set of valid read data before reading this register.

DWord	Bit	Description
0	31:24	**Data Byte 3**
	23:16	**Data Byte 2**
	15:8	**Data Byte 1**
	7:0	**Data Byte 0**

GMBUS4

GMBUS4

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	C5110h-C5113h
Name:	GMBUS4 Interrupt Mask
ShortName:	GMBUS4
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31:5	**Reserved** Format: MBZ
	4:0	**Interrupt Mask** This field specifies which GMBUS interrupts events may contribute to the setting of GMBUS interrupt status bit in the second level interrupt status register. For writes, the HW Ready (HWRDY) interrupt indicates that software can write the next DWORD. It does NOT mean that the transfer of data to the slave device has completed. The IDLE or HW wait interrupt may be used to detect the end of writing data to the slave device. The HWRDY interrupt may be used for gmbus write cycles only to detect when to write the next DWORD after the first two DWORDs have been written to GMBUS3. For reads, the HWRDY interrupt indicates the arrival of the next dword.

Value	Name	Description
0b		
0XXXXb	Slave stall TO Disable	Disable Slave stall timeout interrupt
1XXXXb	Slave stall TO Enable	Enable Slave stall timeout interrupt
X0XXXb	NAK Disable	Disable NAK interrupt
X1XXXb	NAK Enable	Enable NAK interrupt
XX0XXb	Idle Disable	Disable Idle interrupt
XX1XXb	Idle Enable	Enable Idle interrupt

GMBUS4				
		XXX0Xb	HW Wait Disable	Disable Hardware wait (cycle without a stop has completed) Interrupt
		XXX1Xb	HW Wait Enable	Enable Hardware wait (cycle without a stop has completed) Interrupt
		XXXX0b	HW Ready Disable	Disable Hardware ready (Data has been transferred) interrupt
		XXXX1b	HW Ready Enable	Enable Hardware ready (Data has been transferred) interrupt

GMBUS5

GMBUS5	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	C5120h-C5123h
Name:	GMBUS5 2 Byte Index
ShortName:	GMBUS5
Power:	Always on
Reset:	soft

This register provides a method for the software indicate to the GMBUS controller the 2 byte device index.

DWord	Bit	Description
0	31	**2 Byte Index Enable** When this bit is asserted (1), then bits 15:0 are used as the index. Bits 15:8 are used in the first byte which is the most significant index bits. The slave index in the GMBUS1<15:8> are ignored. Bits 7:0 are used in the second byte which is the least significant index bits.
	30:16	**Reserved** Format: MBZ
	15:0	**2 Byte Slave Index** This is the 2 byte index used in all GMBUS accesses when bit 31 is asserted (1).

SBI_ADDR

SBI_ADDR		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	C6000h-C6003h	
Name:	SBI Address	
ShortName:	SBI_ADDR	
Power:	Always on	
Reset:	PLTRST#	

DWord	Bit	Description
0	31:16	**Address Offset** Register address offset. Program the upper 8 bits with the Target ID and the lower 8 bits with the Register Start.
	15:11	**Reserved** Format: MBZ
	10:8	**Base Address Register** Base Address Register (BAR). Always program to 000b.
	7:0	**Routing ID** Routing ID (RID). Always program to 00h.

SBI_DATA

SBI_DATA		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	Write/Read Status	
Size (in bits):	32	
Address:	C6004h-C6007h	
Name:	SBI Data	
ShortName:	SBI_DATA	
Power:	Always on	
Reset:	PLTRST#	
DWord	**Bit**	**Description**
0	31:0	**Data** Register data associated with the addressed register. With a write on the Sideband interface, the content of this register is delivered to the addressed register when the Sideband access is triggered. With a read on the Sideband interface, the hardware updates the content of this register with the return value of the addressed register upon read completion of the triggered Sideband access. The read value is only meaningful when the status bit SBI_CTL_STAT Busy is 0b (Ready).

SBI_CTL_STAT

SBI_CTL_STAT

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	C6008h-C600Bh
Name:	SBI Control and Status
ShortName:	SBI_CTL_STAT
Power:	Always on
Reset:	PLTRST#

DWord	Bit	Description
0	31:17	**Reserved** Format: MBZ
	16	**Reserved** Project: DevLPT:LP Format: MBZ
	16	**Destination ID Select** Project: DevLPT:H This field selects between the two endpoints accessible by display. Value / Name / Description 0b / iCLK / Addressed endpoint is iCLK, ID = 0xED 1b / mPHY / Addressed endpoint is mPHY, ID = 0xD6
	15:8	**Opcode** This is the opcode sent in the sideband message. Value / Name / Description / Project 02h / IORd / IO Read - use for mPHYIP access. / DevLPT:H 03h / IOWr / IO Write - use for mPHYIP access. / DevLPT:H 06h / CRRd / Read Private Control Register - use for iCLKIP access / 07h / CRWr / Write Private Control Register - use for iCLKIP access / Others / Reserved / Reserved /
	7:3	**Reserved**

SBI_CTL_STAT

	Format:	MBZ

2:1 Response Status

Access:	RO

This field gives the response status from hardware for the previously completed transaction.
The value is only meaningful when the status bit Busy is 0b.

Value	Name	Description
00b	Successful	Previous transaction was successful
01b	Unsuccessful	Previous transaction was unsuccessful or not supported
Others	Reserved	Reserved

0 Busy

Access:	Write/Read Status

Software sets this bit to trigger an sideband access using the current contents of registers SBI_ADDR, SBI_DATA, and SBI_CTL_STAT.
Software must not change the contents of these registers while this BUSY bit is set.
Access on the sideband is always handled by the hardware as a non-posted transaction.
Hardware updates this bit to reflect the status of the previous transaction, keeping it at the Busy state while the transaction is in progress and clearing it when the transaction completes.
Software must wait for this bit to clear to Ready prior to starting a new transaction.

Value	Name	Description
0b	Ready	The Display sideband interface is read for a new transaction
1b	Busy	The Display sideband interface is busy with the previous transaction.

PIXCLK_GATE

PIXCLK_GATE	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	C6020h-C6023h
Name:	Pixel Clock Gate
ShortName:	PIXCLK_GATE
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31:1	**Reserved** Format: MBZ
	0	**Pixel Clock UnGate** This field controls the pixel clock gate. The display pixel clock must be gated prior to disabling the clock, and kept gated until after the clock is enabled and the warmup period has passed.

Value	Name	Description
0b	Gate	Gate the pixel clock
1b	Ungate	Ungate the pixel clock

GTCCLK_EN

GTCCLK_EN	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	C6030h-C6033h
Name:	GTC Clock Enable
ShortName:	GTCCLK_EN
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31:1	**Reserved** Format: MBZ
	0	**GTC Clock Enable** This field controls the GTC clock enable. The GTC clock must be enabled prior to enabling GTC, then wait for 40us for warmup, then GTC can be enabled. The clock must be kept enabled until after GTC is disabled. 0b – Disable – Disable the GTC clock 1b – Enable – Enable the GTC clock

RAWCLK_FREQ

RAWCLK_FREQ

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000800
Access:	R/W
Size (in bits):	32
Address:	C6204h-C6207h
Name:	Rawclk Frequency
ShortName:	RAWCLK_FREQ
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31:15	**Reserved** Format: MBZ
	14:10	**Reserved** Project: DevLPT:H Format: MBZ
	14:10	**Deglitch Amount** Default Value: 00010b 2 clks Project: DevLPT:LP This field specifies the deglitch amount for GTC.
	9:0	**Rawclk frequency** Description / Project: Program this field to match the rawclk frequency. This is used to generate a divided down clock for miscellaneous timers in display. Raw Clock = 125 MHz — DevLPT:H Raw Clock = 24 MHz — DevLPT:LP Value / Name: 0000000000b — 0

PP_STATUS

PP_STATUS

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x08000000
Access:	RO
Size (in bits):	32
Address:	C7200h-C7203h
Name:	Panel Power Status
ShortName:	PP_STATUS
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31	**Panel Power On Status** Software is responsible for enabling the embedded panel display only at the correct point as defined in the mode set sequence. This bit will become "0" only after the panel power down sequencing is completed. **Value / Name / Description** 0b / Off / Indicates that the panel power down sequencing has completed. A power cycle delay may be currently active. 1b / On / Indicates that the panel is currently powered up or is currently in the power down sequence.
	30	**Reserved** Format: MBZ
	29:28	**Power Sequence Progress** **Value / Name / Description** 00b / None / Indicates that the panel is not in a power sequence 01b / Power Up / Indicates that the panel is in a power up sequence (may include power cycle delay) 10b / Power Down / Indicates that the panel is in a power down sequence 11b / Reserved / Reserved
	27	**Power Cycle Delay Active** Power cycle delays occur after a panel power down sequence or after a hardware reset. On reset, a power cycle delay will occur using the default value for the timing.

PP_STATUS

		Value / **Name** / **Description** 0b / Not Active / A power cycle delay is not currently active 1b / Active **[Default]** / A power cycle delay is currently active
	26:4	**Reserved** Format: MBZ
	3:0	**Reserved**

PP_CONTROL

PP_CONTROL

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	C7204h-C7207h
Name:	Panel Power Control
ShortName:	PP_CONTROL
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31:16	**Reserved**
	15:4	**Reserved** Format: MBZ
	3	**VDD Override** This bit is used to force on VDD for the embedded DisplayPort panel so AUX transactions can occur without enabling the panel power sequence. This is intended for panels that require VDD to be asserted before accessing AUX port on the receiver. When software clears this bit from '1' to '0' (disable VDD override) it must ensure that T4 power cycle delay is met before setting this bit to '1' again. Value / Name / Description: 0b / Not Force / Panel VDD controlled by Panel Power Sequence state machine 1b / Force / Force panel VDD on
	2	**Backlight Enable** Enabling this bit enables the panel backlight when hardware is in the correct panel power sequence state. The backlight should be enabled and disabled only at the correct points as defined in the mode set sequence. Value / Name / Description: 0b / Disable / Backlight disabled 1b / Enable / Backlight enabled
	1	**Power Down on Reset**

PP_CONTROL

Enabling this bit causes the panel to power down on reset warning or FLR.
If the panel is not on during a reset event, this bit is ignored.

Value	Name	Description
0b	Do not Run	Do not run panel power down sequence when reset is detected
1b	Run	Run panel power down sequence when reset is detected

0

Power State Target
This bit sets the panel power state target. It can be written at any time and takes effect at the completion of any current power cycle.

Value	Name	Description
0b	Off	The panel power state target is off. If the panel is either on or in a power on sequence, a power off sequence is started as soon as the panel reaches the power on state. This may include a power cycle delay. If the panel is currently off, there is no change of the power state or sequencing done.
1b	On	The panel power state target is on. If the panel is in either the off state or a power off sequence, and all pre-conditions are met, a power on sequence is started as soon as the panel reaches the power off state. This may include a power cycle delay. If the panel is currently on, there is no change of the power state or sequencing done.

Note:
Note: On ULT systems with ISCLK PLL shutdown enabled, display register C2020h bit 12 must be set to 1b before setting panel power state target to "On". If no other feature requires register C2020h bit 12, it can be cleared to 0b after the panel power state target has been set to "Off" and the panel power status indicates the panel is off and the power cycle delay is not active. To save power, register C2020h bit 12 must be cleared to 0b when internal graphics is put in the D3 device power state.

PP_ON_DELAYS

PP_ON_DELAYS	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	C7208h-C720Bh
Name:	Panel Power On Sequencing Delays
ShortName:	PP_ON_DELAYS
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28:16	**Power up delay** Programmable value of panel power sequencing delay during panel power up. Software programs this field with the time delay for the eDP T3 time value; the time from the source enabling panel power to when the sink HPD and AUX channel are ready. Software controls when AUX channel transactions start, so this is just used as a timer. The time unit used is the 100us timer.
	15:13	**Reserved** Format: MBZ
	12:0	**Power on to backlight on** Power on to backlight enable delay. Programmable value of panel power sequencing delay during panel power up. Software programs this field with a value of 1b to get the minimum delay from hardware. Software controls the source valid video data output and backlight enable after this delay has been met. Hardware will not allow the backlight to enable until after this delay and the power up delay (eDP T3) have passed. The time unit used is the 100us timer.

PP_OFF_DELAYS

PP_OFF_DELAYS	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	C720Ch-C720Fh
Name:	Panel Power Off Sequencing Delays
ShortName:	PP_OFF_DELAYS
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28:16	**Power Down delay** Programmable value of panel power sequencing delay during power down. Software programs this field with the time delay for the eDP T10 time value; the time from source ending valid video data to source disabling panel power. Software controls the source valid video data output, so this together with T9 is only used as a step towards the final power down delay. The time unit used is the 100us timer.
	15:13	**Reserved** Format: MBZ
	12:0	**Backlight off to power down** Power backlight off to power down delay. Programmable value of panel power sequencing delay during power down. Software programs this field with the time delay for the eDP T9 time value; the time from backlight disable to source ending valid video data. Software controls the backlight disable and source valid video data output, so this together with T10 is only used as a step towards the final power down delay. The time unit used is the 100us timer.

PP_DIVISOR

PP_DIVISOR

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00186906
Access:	R/W
Size (in bits):	32
Address:	C7210h-C7213h
Name:	Panel Power Cycle Delay and Reference Divisor
ShortName:	PP_DIVISOR
Power:	Always on
Reset:	soft

This register programs the reference divisor and controls how long the panel must remain in a power off condition once powered down.

DWord	Bit	Description
0	31:8	**Reference divider** This field provides the value of the divider used for the creation of the panel timer reference clock. The output of the divider is used as the time base (100 us) for all other timers. The value of zero must not be used. The value should be (100 * Ref clock frequency in MHz / 2) - 1. **Reference Clock Frequency** / **Decimal Value** / **Hex Value to Program** 125 MHz / 6249d / 001869h 24 MHz / 1199d / 0004AFh **Value** / **Name** / **Project** 001869h / 125 MHz **[Default]** / DevLPT:H 0004AFh / 24 MHz **[Default]** / DevLPT:LP
	7:5	**Reserved** Format: MBZ
	4:0	**Power Cycle Delay** Default Value: 6h 500 mS Power cycle delay. Programmable value of time panel must remain in a powered down state after powering down. This provides the time delay for the eDP T12 time value; the shortest time from panel power

PP_DIVISOR		
		disable to power enable. If a panel power on sequence is attempted during this delay, the power on sequence will not commence until the delay is complete. The time unit used is the 100 ms timer. This register needs to be programmed to a "+1" value. For instance to achieve 400 ms, program a value of 5. Writing a value of 0 selects no delay or is used to abort the delay if it is active. For devices coming out of reset, the timer will be set to the default value and the count down will begin after the de-assertion of reset. Even if the panel is not enabled, the count happens after reset.

SBLC_PWM_CTL1

SBLC_PWM_CTL1

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	C8250h-C8253h
Name:	South BLM Control 1
ShortName:	SBLC_PWM_CTL1
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31	**PWM PCH Enable** This bit enables the PWM counter logic in the PCH. Disabled PWM will drive 0, which can be inverted to 1 with the polarity bit.

Value	Name	Description
0b	Disable	PCH PWM disabled
1b	Enable	PCH PWM enabled

Restriction
Restriction : Program the frequency and duty cycle before enabling PWM.

DWord	Bit	Description
	30	**PWM PCH Override Enable** This bit enables PWM messages from CPU to PCH to be overriden by the SBLC_PWM_CTL2 Backlight Duty Cycle Override value.

Value	Name	Description
0b	Disable	Override disabled (CPU display controls PWM duty cycle)
1b	Enable	Override enabled (Override register value controls PWM duty cycle)

DWord	Bit	Description
	29	**Backlight Polarity** This field controls the polarity of the PWM signal.

Value	Name	Description
0b	High	Active High
1b	Low	Active Low

DWord	Bit	Description
	28:0	**Reserved**

SBLC_PWM_CTL1			
		Format:	MBZ

SBLC_PWM_CTL2

<table>
<tr><th colspan="3">SBLC_PWM_CTL2</th></tr>
<tr><td colspan="3">Register Space: MMIO: 0/2/0
Project: HSW
Source: PRM
Default Value: 0x00000000
Access: R/W
Size (in bits): 32</td></tr>
<tr><td colspan="3">Address: C8254h-C8257h
Name: South BLM Control 2
ShortName: SBLC_PWM_CTL2
Power: Always on
Reset: soft</td></tr>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td rowspan="2">0</td><td>31:16</td><td>Backlight Modulation Frequency
<table>
<tr><th>Description</th><th>Project</th></tr>
<tr><td>This field determines the number of time base events in total for a complete cycle of modulated backlight control.
This field is normally set once during initialization based on the frequency of the clock that is being used and the desired PWM frequency.
This value represents the period of the PWM stream in clock periods multiplied by 128 (default increment) or 16 (alternate increment selected in SCHICKEN_2 bit 5).</td><td></td></tr>
<tr><td>PWM clock is 135 MHz, non-spread, 100ppm</td><td>DevLPT:H</td></tr>
<tr><td>PWM clock is 24 MHz, non-spread, <100ppm</td><td>DevLPT:LP</td></tr>
</table></td></tr>
<tr><td>15:0</td><td>Backlight Duty Cycle Override
This value overrides the CPU control of PWM duty cycle when the PWM PCH Override Enable bit is set.
This field determines the number of time base events for the active portion of the PWM backlight control.
This should never be larger than the frequency field.
A value of zero will turn the backlight off. A value equal to the backlight modulation frequency field will be full on.
When written, the new value will take affect at the end of the current PWM cycle.
This value represents the active time of the PWM stream in clock periods multiplied by 128 (default increment) or 16 (alternate increment selected in SCHICKEN_2 bit 5).</td></tr>
</table>

HTOTAL

HTOTAL		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	E0000h-E0003h	
Name:	Transcoder A Horizontal Total	
ShortName:	TRANS_HTOTAL_A	
Power:	Always on	
Reset:	soft	

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28:16	**Horizontal Total** This field specifies Horizontal Total size. This should be equal to the sum of the horizontal active and the horizontal blank sizes. This field is programmed to the number of pixels desired minus one. This register must always be programmed to the same value as the Horizontal Blank End.
	15:12	**Reserved** Format: MBZ
	11:0	**Horizontal Active** This field specifies Horizontal Active Display size. Note that the first horizontal active display pixel is considered pixel number 0. This field is programmed to the number of pixels desired minus one. The minimum horizontal active display size is 64 pixels. This register must always be programmed to the same value as the Horizontal Blank Start.

HBLANK

HBLANK	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	E0004h-E0007h
Name:	Transcoder A Horizontal Blank
ShortName:	TRANS_HBLANK_A
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28:16	**Horizontal Blank End** This field specifies Horizontal Blank End position relative to the horizontal active display start. The minimum horizontal blank size is 32 pixels. This register must always be programmed to the same value as the Horizontal Total.
	15:13	**Reserved** Format: MBZ
	12:0	**Horizontal Blank Start** This field specifies the Horizontal Blank Start position relative to the horizontal active display start. This register must always be programmed to the same value as the Horizontal Active.

HSYNC

HSYNC

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	E0008h-E000Bh
Name:	Transcoder A Horizontal Sync
ShortName:	TRANS_HSYNC_A
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28:16	**Horizontal Sync End** This field specifies the Horizontal Sync End position relative to the horizontal active display start. It is programmed with HorizontalActive+FrontPorch+Sync-1. This value must be greater than the horizontal sync start and less than Horizontal Total. Value: 0b — Name:
	15:13	**Reserved** Format: MBZ
	12:0	**Horizontal Sync Start** This field specifies the Horizontal Sync Start position relative to the horizontal active display start. It is programmed with HorizontalActive+FrontPorch-1. This value must be greater than Horizontal Active. Value: 0b — Name:

VTOTAL

VTOTAL	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	E000Ch-E000Fh
Name:	Transcoder A Vertical Total
ShortName:	TRANS_VTOTAL_A
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28:16	**Vertical Total** This field specifies Vertical Total size. This should be equal to the sum of the vertical active and the vertical blank sizes. For progressive display modes, this field is programmed to the number of lines desired minus one. For interlaced display modes, this field is programmed with the number of lines desired minus two. The vertical counter is incremented on the leading edge of the horizontal sync. Both even and odd vertical totals are supported. This register must always be programmed to the same value as the Vertical Blank End.
	15:12	**Reserved** Format: MBZ
	11:0	**Vertical Active** This field specifies Vertical Active Display size. Note that the first vertical active display line is considered line number 0. This field is programmed to the number of lines desired minus one. This register must always be programmed to the same value as the Vertical Blank Start.

VBLANK

VBLANK		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	E0010h-E0013h	
Name:	Transcoder A Vertical Blank	
ShortName:	TRANS_VBLANK_A	
Power:	Always on	
Reset:	soft	

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28:16	**Vertical Blank End** This field specifies Vertical Blank End position relative to the vertical active display start. The minimum vertical blank size is 5 lines. This register must always be programmed to the same value as the Vertical Total.
	15:13	**Reserved** Format: MBZ
	12:0	**Vertical Blank Start** This field specifies the Vertical Blank Start position relative to the vertical active display start. This register must always be programmed to the same value as the Vertical Active

VSYNC

VSYNC	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	E0014h-E0017h
Name:	Transcoder A Vertical Sync
ShortName:	TRANS_VSYNC_A
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28:16	**Vertical Sync End** This field specifies the Vertical Sync End position relative to the vertical active display start. It is programmed with VerticalActive+FrontPorch+Sync-1. This value must be greater than the vertical sync start and less than Vertical Total.
	15:13	**Reserved** Format: MBZ
	12:0	**Vertical Sync Start** This field specifies the Vertical Sync Start position relative to the vertical active display start. It is programmed with VerticalActive+FrontPorch-1. This value must be greater than Vertical Active.

VSYNCSHIFT

VSYNCSHIFT		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	E0028h-E002Bh	
Name:	Transcoder A Vertical Sync Shift	
ShortName:	TRANS_VSYNCSHIFT_A	
Power:	Always on	
Reset:	soft	

DWord	Bit	Description
0	31:13	**Reserved** Format: MBZ
	12:0	**Second Field VSync Shift** This value specifies the vertical sync alignment for the start of the interlaced second field, expressed in terms of the absolute pixel number relative to the horizontal active display start. This value will only be used if the transcoder is in an interlaced mode. Typically, the interlaced second field vertical sync should start one pixel after the point halfway between successive horizontal syncs, so the value of this register should be programmed to: (horizontal sync start - floor[horizontal total / 2]) (Calculations uses the actual horizontal sync start and horizontal total values and not the minus one values programmed into the registers) This vertical sync shift only occurs during the interlaced second field. In all other cases the vertical sync start position is aligned with horizontal sync start.

DAC_CTL

DAC_CTL

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00040000
Access:	R/W
Size (in bits):	32
Address:	E1100h-E1103h
Name:	Analog Port CRT DAC Control
ShortName:	DAC_CTL
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31	**Port Enable** This bit enables or disables the analog port CRT DAC and syncs outputs. The CRT DAC capability disable fuse (SFUSE_STRAP but 6) can override so that this port can not be enabled. **Value / Name / Description** 0b / Disable / Disable the analog port DAC and disable output of syncs 1b / Enable / Enable the analog port DAC and enable output of syncs
	30:26	**Reserved** Format: MBZ
	25:24	**CRT HPD Channel Status** Access: RO These bits indicate which color channels were found to be attached on the last hot plug detection cycle. These bits go to the SDE_ISR CRT hot plug register bit. **Value / Name / Description** 00b / None / No channels attached 01b / Blue / Blue channel only is attached 10b / Green / Green channel only is attached 11b / Both / Both blue and green channel attached
	23	**CRT HPD Enable** Hot plug detection is used to set status bits on the connection or disconnection of a CRT to the analog port CRT DAC.

DAC_CTL

Value	Name	Description
0b	Disable	CRT hot plug detection is disabled
1b	Enable	CRT hot plug detection is enabled

22 **CRT HPD Activation Period**

This bit sets the activation period for the CRT hot plug circuit.

Value	Name	Description
0b	64 rawclk	64 rawclk periods
1b	128 rawclk	128 rawclk periods

21 **CRT HPD Warmup Time**

This bit sets the warmup time for the CRT hot plug circuit.

Value	Name	Description
0b	4ms	Approximately 4ms
1b	8ms	Approximately 8ms

20 **CRT HPD Sampling Period**

This bit determines the length of time between sampling periods when the transcoder is disabled.

Value	Name	Description
0b	2 seconds	Approximately 2 seconds
1b	4 seconds	Approximately 4 seconds

19:18 **CRT HPD Voltage Value**

Value to drive to the DAC to determine whether the analog port is connected to a CRT.

Value	Name	Description
00b	0x90	0x90
01b	0xA0 **[Default]**	0xA0
10b	0xB0	0xB0
11b	0xC0	0xC0

17 **Reserved**

Format:	MBZ

16 **Force CRT HPD Trigger**

Triggers a CRT hotplug/unplug detection cycle independent of the hot plug detection enable bit.
This bit is automatically cleared after the detection is completed.
The result of this trigger is reflected in the CRT Hot Plug Detection Status.
Software must reset status after a force CRT detect trigger.

Value	Name	Description
0b	No Trigger	No Trigger
1b	Force Trigger	Force Trigger

15:5 **Reserved**

DAC_CTL

	Format:	MBZ
4	**VSYNC Polarity Control** The output VSYNC polarity is controlled by this bit. This is used to implement display modes that require inverted polarity syncs and to set the disabled state of the VSYNC signal.	

Value	Name	Description
0b	Low	Active Low
1b	High	Active High

3	**HSYNC Polarity Control** The output HSYNC polarity is controlled by this bit. This is used to implement display modes that require inverted polarity syncs and to set the disabled state of the HSYNC signal.	

Value	Name	Description
0b	Low	Active Low
1b	High	Active High

2:0	**Reserved**	
	Format:	MBZ

DP_AUX_CTL

DP_AUX_CTL	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x0003003F
Access:	R/W Special
Size (in bits):	32
Address:	E4110h-E4113h
Name:	DisplayPort B AUX Channel Control
ShortName:	DP_AUX_CTL_B
Power:	Always on
Reset:	soft
Address:	E4210h-E4213h
Name:	DisplayPort C AUX Channel Control
ShortName:	DP_AUX_CTL_C
Power:	Always on
Reset:	soft
Address:	E4310h-E4313h
Name:	DisplayPort D AUX Channel Control
ShortName:	DP_AUX_CTL_D
Power:	Always on
Reset:	soft

Restriction	Project
Restriction : On LP parts the DisplayPort D AUX Channel should not be used as the pins are not connected in the package.	DevLPT:LP

DWord	Bit	Description
0	31	**Send Busy** Access: R/W Set Writing this bit with 1b initiates the transaction, when read this bit will be a 1b until the transmission completes. The transaction is completed when the response is received or when a timeout occurs. Do not write a 1b again until transaction completes. This is a sticky bit. Write a 1b to this bit to set it and initiate the transaction. Hardware will clear it when the transaction completes.

DP_AUX_CTL

Value	Name
0b	Not Busy
1b	Send or Busy

Programming Notes
It is recommended to retry at least 3 times after any failed transaction. Do not change any fields while Send/Busy bit 31 is asserted.

Note:
Note: On ULT systems with ISCLK PLL shutdown enabled, display register C2020h bit 12 must be set to 1b before sending an AUX Channel transaction. If no other feature requires register C2020h bit 12, it can be cleared to 0b after the AUX Channel transaction is complete. To save power, register C2020h bit 12 must be cleared to 0b when internal graphics is put in the D3 device power state.

30 **Done**

Access:	R/WC

A sticky bit that indicates the transaction has completed.
Write a 1 to this bit to clear the event.

Value	Name	Description
0b	Not done	Transaction not done
1b	Done	Transaction done

29 **Interrupt on Done**

Enable an interrupt in the hotplug status register when the transaction completes or times out.

Value	Name	Description
0b	Disable	Disable interrupt on done
1b	Enable	Enable interrupt on done

28 **Time out error**

Access:	R/WC

A sticky bit that indicates the transaction has timed out.
Write a 1 to this bit to clear the event.

Value	Name	Description
0b	No error	No time out error
1b	Error	Time out error

27:26 **Time out timer value**

Used to determine how long to wait for receiver response before timing out.

Value	Name	Description
00b	400us	400us
01b	600us	600us

DP_AUX_CTL

10b	800us	800us
11b	1600us	1600us

25 Receive error

Access:	R/WC

A sticky bit that indicates that the data received was corrupted, not in multiples of a full byte, or more than 20 bytes.
Write a 1 to this bit to clear the event.

Value	Name	Description
0b	No error	No receive error
1b	Error	Receive error

24:20 Message Size

This field is used to indicate the total number bytes to transmit (including the header).
It also indicates the number of bytes received in a transaction (including the header).
This field is valid only when the done bit is set, and if timeout or receive error has not occurred.
Sync/Stop patterns are not counted as part of the message or the message size.
Reads of this field will give the response message size. The read value will not be valid while Send/Busy bit 31 is asserted.
Message sizes of 0 or >20 are not allowed.

Value	Name
00000b	0 bytes

19:16 Precharge Time

Default Value:	0011b 6us

Used to determine the precharge time for the Aux Channel drivers. During this time the Aux Channel will drive the SYNC pattern.
Every microsecond gives one additional SYNC pulse beyond the hard coded 26 SYNC pulses.
The value is the number of microseconds times 2.
Default is 3 decimal, which gives 6us of precharge, which is 6 extra SYNC pulses for a total of 32.

15 Reserved

14 Reserved

13 Reserved

12 Reserved

11 Reserved

10:0 2X Bit Clock divider

This field determines the 2X bit clock the Aux Channel logic runs on.
This value divides the input clock frequency down to 2X bit clock rate. It should be programmed to get as close as possible to the ideal rate of 2 MHz.
The input clock is the raw clock.

Value	Name	Project

DP_AUX_CTL

03Fh	125 MHz **[Default]**	DevLPT:H
048h	Note	DevLPT:H
00Ch	24 MHz **[Default]**	DevLPT:LP

Note:	Project
Note: On LPT:H use a divider value of 63 decimal (03Fh). If there is a failure, retry at least 3 times with 63, then retry at least 3 times with 72 decimal (048h).	DevLPT:H

DP_AUX_DATA

DP_AUX_DATA	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	Write/Read Status
Size (in bits):	32
Address:	E4114h-E4127h
Name:	DisplayPort B AUX Channel Data
ShortName:	DP_AUX_DATA_B_*
Power:	Always on
Reset:	soft
Address:	E4214h-E4227h
Name:	DisplayPort C AUX Channel Data
ShortName:	DP_AUX_DATA_C_*
Power:	Always on
Reset:	soft
Address:	E4314h-E4327h
Name:	DisplayPort D AUX Channel Data
ShortName:	DP_AUX_DATA_D_*
Power:	Always on
Reset:	soft
There are 5 instances of this register format per AUX channel.	

DWord	Bit	Description
0	31:0	**AUX CH DATA** This field contains a DWord of the AUX message. Writes to this register give the data to transmit during the transaction. The MSbyte is transmitted first. Reads to this register will give the response data after transaction complete. The read value will not be valid while the Aux Channel Control Register Send/Busy bit is asserted.

GTC_CTL

GTC_CTL

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x0400010E
Access:	R/W
Size (in bits):	32
Address:	E7000h-E7003h
Name:	Global Time Code Control
ShortName:	GTC_CTL
Power:	Always on
Reset:	soft

<table>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td>0</td><td>31</td><td>GTC Function Enable
<table>
<tr><th>Description</th><th>Project</th></tr>
<tr><td>This bit enables the PCH GTC counter and periodic PCH update messages to the GTC slave in the CPU.
Software must enable this bit before enabling GTC controller operation on a port with a GTC capable device.</td><td></td></tr>
<tr><td>The GTC clock must be enabled in GTCLK_EN and warmed up for 40us prior to enabling GTC.</td><td>DevLPT:LP</td></tr>
</table>
<table>
<tr><th>Value</th><th>Name</th><th>Description</th></tr>
<tr><td>0b</td><td>Disable</td><td>GTC Disabled</td></tr>
<tr><td>1b</td><td>Enable</td><td>GTC Enabled</td></tr>
</table>
<table>
<tr><th>Note:</th></tr>
<tr><td>Note: On ULT systems with ISCLK PLL shutdown enabled, display register C2020h bit 12 must be set to 1b before enabling GTC. If no other feature requires register C2020h bit 12, it can be cleared to 0b after GTC is disabled. To save power, register C2020h bit 12 must be cleared to 0b when internal graphics is put in the D3 device power state.</td></tr>
</table></td></tr>
<tr><td></td><td>30:29</td><td>Master Select
This field shall be set by software designate the GTC master. The PCH GTC controller is master by default; however it may designate an attached GTC device as the master. This occurs in response to request from designated GTC sink to act as master. Only one remote GTC sink may act as master.</td></tr>
</table>

GTC_CTL

When operating as a slave, the GTC controller of the designated port will transition from writing GTCs periodically to the remote GTC sink to reading GTCs periodically from the remote GTC sink. The GTC controller must be returned to lock acquisition phase before changing this register field.
Slave mode only

Value	Name	Description
00b	Master	GTC controller is master
01b	PortB	GTC controller is slave to GTC sink on port B
10b	PortC	GTC controller is slave to GTC sink on port C
11b	PortD	GTC controller is slave to GTC sink on port D

28 **Reserved**

27:26 **CPU Update Interval**
This field programs the interval period used by GTC master to update the GTC slave in the CPU. During lock acquisition with remote GTC sink device software should program this value to 1ms or less.
After remote sink lock done bit has been detected and at the time software enables maintenance phase enable bit, this bit should be set to 10ms.

Value	Name	Description
00b	0.5ms	Send update every 0.5ms
01b	1ms **[Default]**	Send update every 1ms
10b	2ms	Send update every 2ms
11b	10ms	Send update every 10ms

25:13 **Reserved**

12:11 **Reserved**

Project:	DevLPT:LP
Format:	MBZ

12:11 **Reserved**

Project:	DevLPT:H

10:1 **Reference Clock Freq**

Description	Project
This field is used to indicate the frequency of the reference clock used by aux encoder/decoder to transmit update messages from PCH to CPU. Hardware shall use this value to divide down the GTC reference clock as needed to implement 1MHz aux signaling frequency.	
Reference clock is 135 MHz	DevLPT:H
Reference clock is 96 MHz	DevLPT:LP

Value	Name	Project

GTC_CTL				
		0001 0000 111b	135 MHz **[Default]**	DevLPT:H
		0000 1100 000b	96 MHz **[Default]**	DevLPT:LP
	0	**Reserved**		

GTC_MISC

GTC_MISC

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00434A00
Access:	R/W
Size (in bits):	32
Address:	E7004h-E7007h
Name:	Global Time Code Miscellaneous
ShortName:	GTC_MISC
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31:24	**GTC Lock Status** Access: RO This field stores the history of the last 8 compare results to determine if GTC slave is tracking remote GTC master. The LSB indicates the most recent compare result. The MSB indicates the oldest compare result. The LSB is set if the difference between master and slave GTC is less than the GTC lock compare value. When a new comparison is complete, the LSB is updated with the result and the previous results are shifted towards the MSB and the old MSB is dropped.
	23:22	**CPU GTC Lock Compare Value** This field programs the threshold used to determine whether to set the lock status bit following comparison between the slave and master GTC values.

Value	Name	Description
00b	30ns	Difference between master/slave is less than 30ns
01b	50ns **[Default]**	Difference between master/slave is less than 50ns
10b	100ns	Difference between master/slave is less than 100ns
11b	200ns	Difference between master/slave is less than 200ns

DWord	Bit	Description
	21:12	**Reserved** Project: DevLPT:H
	21:12	**GTC Update Message Delay** Default Value: 00110100b 52 nanoseconds

GTC_MISC

		Project: DevLPT:LP In master mode this field is used to program the absolute delay in nanoseconds between the GTC at the aux sync point event in PCH and the corresponding GTC value at the capture point. It represents the delay between the GTC values at the aux sync point and capture point introduced due to synchronization and glitch suppression.
	11:8	**Min Lock Duration** Default Value: 1010b 10ms This field determines the minimum duration in milliseconds of lock acquisition phase after which software is notified through interrupt. The GTC interrupt enable and mask register programming must be enabled beforehand. Software may also poll the interrupt identity bit in IIR.
	7:0	**Max Lock Timeout** This field determines the minimum duration in 1ms increments of lock acquisition phase after which software is notified through interrupt that GTC was unable to achieve lock with remote GTC sync. Default programming of "0000" disables hardware timeout error notification.

GTC_DDA_M

GTC_DDA_M		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	E7010h-E7013h	
Name:	Global Time Code DDA M Value	
ShortName:	GTC_DDA_M	
Power:	Always on	
Reset:	soft	
DWord	**Bit**	**Description**
0	31:24	**Reserved**
	23:0	**GTC DDA M** This field is used to program the M value of the GTC DDA. The ratio of M to N programmed depends on the GTC reference clock. The DDA programmed values are related by the following formula: 1/(accumulator increment)=Reference Clock * DDA_M / DDA_N

GTC_DDA_N

GTC_DDA_N		
Register Space:	MMIO: 0/2/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	E7014h-E7017h	
Name:	Global Time Code DDA N Value	
ShortName:	GTC_DDA_N	
Power:	Always on	
Reset:	soft	

DWord	Bit	Description
0	31:26	**GTC Accum Inc** Format: U5.1 This field is used to program the GTC accumulator increment value in nanoseconds each time the DDA trips. It should be programmed in 5.1 fixed point binary format where the LSB represents 0.5ns increment.
	25:24	**Reserved**
	23:0	**GTC DDA N** This field is used to program the N value of the GTC DDA. The ratio of M to N programmed depends on the GTC reference clock and should not result in any accumulation error in any 10ms interval period. The DDA programmed values are related by the following formula: 1/(accumulator increment)= Reference Clock * DDA_M / DDA_N

GTC_PCH_IMR

GTC_PCH_IMR

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	E7054h-E7057h
Name:	Global Time Code Interrupt Mask
ShortName:	GTC_PCH_IMR
Power:	Always on
Reset:	soft

See the GTC PCH interrupt bit definition table to find the source event for each interrupt bit.

DWord	Bit	Description
0	31:0	**Interrupt Mask Bits** This field contains a bit mask which selects which GTC PCH events are reported in the GTC PCH IIR.

Value	Name	Description
0b	Not Masked	Not Masked - will be reported in the GTC_PCH_IIR
1b	Masked	Masked - will not be reported in the GTC_PCH_IIR

GTC_PCH_IIR

GTC_PCH_IIR	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/WC
Size (in bits):	32
Address:	E7058h-E705Bh
Name:	Global Time Code Interrupt Identity
ShortName:	GTC_PCH_IIR
Power:	Always on
Reset:	soft

See the GTC PCH interrupt bit definition table to find the source event for each interrupt bit.

DWord	Bit	Description
0	31:0	**Interrupt Identity Bits** This field holds the persistent values of the GTC PCH interrupt bits which are unmasked by the GTC_PCH_IMR. Bits set in this register will propagate to the combined GTC_PCH interrupt in the SDE_ISR. Bits set in this register will remain set (persist) until the interrupt condition is cleared by writing a '1' to the appropriate bits.

Value	Name	Description
0b	Condition Not Detected	Interrupt Condition Not Detected
1b	Condition Detected	Interrupt Condition Detected

GTC_SLAVE_RX_PREV

GTC_SLAVE_RX_PREV	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	E7078h-E707Bh
Name:	Global Time Code RX Previous Value
ShortName:	GTC_SLAVE_RX_PREV
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31:0	**GTC RX Previous** This field contains the previous GTC value read from remote GTC sink. It is transferred from the GTC_PORT_RX_VALUE register of port designated as master when the current value is updated. This register is valid only when GTC controller is operating as a slave to remote GTC master. Slave mode only

GTC_SLAVE_TX_PREV

GTC_SLAVE_TX_PREV	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	E707Ch-E707Fh
Name:	Global Time Code TX Previous Value
ShortName:	GTC_SLAVE_TX_PREV
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31:0	**GTC TX Previous** This field contains the previous local GTC value sampled at Aux sync point. It is transferred from the GTC_PORT_TX_VALUE register of port designated as master when the current value is updated. This register is valid only when GTC controller is operating as a slave to remote GTC master. Slave mode only

GTC_PORT_CTL

GTC_PORT_CTL	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	E70B0h-E70B3h
Name:	Global Time Code Port B Control
ShortName:	GTC_PORT_CTL_B
Power:	Always on
Reset:	soft
Address:	E70C0h-E70C3h
Name:	Global Time Code Port C Control
ShortName:	GTC_PORT_CTL_C
Power:	Always on
Reset:	soft
Address:	E70D0h-E70D3h
Name:	Global Time Code Port D Control
ShortName:	GTC_PORT_CTL_D
Power:	Always on
Reset:	soft
There is one instance of this register per port B, C, and D.	

DWord	Bit	Description
0	31	**Port GTC Enable** This bit enables the GTC controller to start lock acquisition phase with remote GTC sink connected to this port. The Maintenance_phase_enable bit must be initially written as '0' when this bit is set. This bit has no effect if the GTC controller is disabled.

Value	Name	Description
0b	Disable	GTC synchronization with remote sink disabled
1b	Enable	GTC synchronization with remote sink enabled

Programming Notes

GTC_PORT_CTL

When this port is enabled software must use the associated GTC Update Complete interrupt to determine that a hardware periodic update was completed prior to intiating a read from GTC remote slave.

Restriction	Project
Restriction : Prior to the LPT:H:B1 and LPT:LP:A1 steppings, Global Time Code hardware initiated periodic updates to remote GTC slave is not supported.	DevLPT:H, EXCLUDE(DevLPT:H:A), EXCLUDE(DevLPT:H:B0), EXCLUDE(DevLPT:LP:A0)

30:25 **Reserved**

24 **Maintenance Phase Enable**

This bit is used by software to transition from lock acquisition to lock maintenance phase.
The GTC controller generates an interrupt at the end of the lock phase as determined by lock acquisition duration field.
Software shall read the sink device GTC lock done bit. If set, software shall set this bit to '1' after first writing the GTC skew value to the RX GTC skew DPCD offset with GTC skew enable bit set to '1'.

Value	Name	Description
0b	Lock	Lock acquisition phase—the controller writes or reads GTC every 1ms
1b	Maintain	Lock maintenance phase—the controller writes or reads GTC every 10ms

23:2 **Reserved**

1 **GTC Port TX Lock Done**

This bit indicates the GTC controller operating in slave mode has achieved lock with the remote GTC sink.
This bit shall be written by software based on hardware compare results between GTC controller in slave mode and remote GTC master.
This bit shall be cleared by software when GTC controller is returned to lock acquisition phase.
Slave mode only

Value	Name	Description
0b	NoLock	GTC TX slave not locked
1b	Lock	GTC TX slave lock achieved

0 **GTC Port RX Lock Done**

This bit indicates the remote GTC sink has achieved lock.
This bit shall be written by software after reading remote GTC sink DPCD register.
This bit shall be cleared by software when GTC controller is reset from lock maintenance mode to lock acquisition mode or when the controller is disabled.

Value	Name	Description
0b	NoLock	GTC RX slave not locked
1b	Lock	GTC RX slave lock achieved

GTC_PORT_RX_CURR

GTC_PORT_RX_CURR	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	E70B4h-E70B7h
Name:	Global Time Code Port B RX Current Value
ShortName:	GTC_PORT_RX_CURR_B
Power:	Always on
Reset:	soft
Address:	E70C4h-E70C7h
Name:	Global Time Code Port C RX Current Value
ShortName:	GTC_PORT_RX_CURR_C
Power:	Always on
Reset:	soft
Address:	E70D4h-E70D7h
Name:	Global Time Code Port D RX Current Value
ShortName:	GTC_PORT_RX_CURR_D
Power:	Always on
Reset:	soft
There is one instance of this register per port B, C, and D.	

DWord	Bit	Description
0	31:0	**GTC Port RX Current** This field contains the remote sink GTC value at the Aux sync point of the response message from the remote GTC sink. It is updated by hardware following a read of the remote sink GTC DPCD register.

GTC_PORT_TX_CURR

GTC_PORT_TX_CURR	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	E70B8h-E70BBh
Name:	Global Time Code Port B TX Current Value
ShortName:	GTC_PORT_TX_CURR_B
Power:	Always on
Reset:	soft
Address:	E70C8h-E70CBh
Name:	Global Time Code Port C TX Current Value
ShortName:	GTC_PORT_TX_CURR_C
Power:	Always on
Reset:	soft
Address:	E70D8h-E70DBh
Name:	Global Time Code Port D TX Current Value
ShortName:	GTC_PORT_TX_CURR_D
Power:	Always on
Reset:	soft
There is one instance of this register per port B, C, and D.	

DWord	Bit	Description
0	31:0	**GTC Port TX Current** This field contains the local GTC value sampled at the Aux sync point of the response message from remote GTC sink following software read of remote sink GTC DPCD register when PCH GTC controller is operating as master. When PCH GTC controller is operating as a slave this field contains the local GTC value sampled at the Aux sync point of the response message. In both master and slave mode this register is updated by hardware.

GTC_PORT_CTL

GTC_PORT_CTL	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	E70B0h-E70B3h
Name:	Global Time Code Port B Control
ShortName:	GTC_PORT_CTL_B
Power:	Always on
Reset:	soft
Address:	E70C0h-E70C3h
Name:	Global Time Code Port C Control
ShortName:	GTC_PORT_CTL_C
Power:	Always on
Reset:	soft
Address:	E70D0h-E70D3h
Name:	Global Time Code Port D Control
ShortName:	GTC_PORT_CTL_D
Power:	Always on
Reset:	soft
There is one instance of this register per port B, C, and D.	

DWord	Bit	Description
0	31	**Port GTC Enable** This bit enables the GTC controller to start lock acquisition phase with remote GTC sink connected to this port. The Maintenance_phase_enable bit must be initially written as '0' when this bit is set. This bit has no effect if the GTC controller is disabled.

Value	Name	Description
0b	Disable	GTC synchronization with remote sink disabled
1b	Enable	GTC synchronization with remote sink enabled

Programming Notes

GTC_PORT_CTL

When this port is enabled software must use the associated GTC Update Complete interrupt to determine that a hardware periodic update was completed prior to intiating a read from GTC remote slave.

Restriction	Project
Restriction : Prior to the LPT:H:B1 and LPT:LP:A1 steppings, Global Time Code hardware initiated periodic updates to remote GTC slave is not supported.	DevLPT:H, EXCLUDE(DevLPT:H:A), EXCLUDE(DevLPT:H:B0), EXCLUDE(DevLPT:LP:A0)

30:25 Reserved

24 Maintenance Phase Enable

This bit is used by software to transition from lock acquisition to lock maintenance phase.
The GTC controller generates an interrupt at the end of the lock phase as determined by lock acquisition duration field.
Software shall read the sink device GTC lock done bit. If set, software shall set this bit to '1' after first writing the GTC skew value to the RX GTC skew DPCD offset with GTC skew enable bit set to '1'.

Value	Name	Description
0b	Lock	Lock acquisition phase—the controller writes or reads GTC every 1ms
1b	Maintain	Lock maintenance phase—the controller writes or reads GTC every 10ms

23:2 Reserved

1 GTC Port TX Lock Done

This bit indicates the GTC controller operating in slave mode has achieved lock with the remote GTC sink.
This bit shall be written by software based on hardware compare results between GTC controller in slave mode and remote GTC master.
This bit shall be cleared by software when GTC controller is returned to lock acquisition phase.
Slave mode only

Value	Name	Description
0b	NoLock	GTC TX slave not locked
1b	Lock	GTC TX slave lock achieved

0 GTC Port RX Lock Done

This bit indicates the remote GTC sink has achieved lock.
This bit shall be written by software after reading remote GTC sink DPCD register.
This bit shall be cleared by software when GTC controller is reset from lock maintenance mode to lock acquisition mode or when the controller is disabled.

Value	Name	Description
0b	NoLock	GTC RX slave not locked
1b	Lock	GTC RX slave lock achieved

GTC_PORT_RX_CURR

GTC_PORT_RX_CURR	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	E70B4h-E70B7h
Name:	Global Time Code Port B RX Current Value
ShortName:	GTC_PORT_RX_CURR_B
Power:	Always on
Reset:	soft
Address:	E70C4h-E70C7h
Name:	Global Time Code Port C RX Current Value
ShortName:	GTC_PORT_RX_CURR_C
Power:	Always on
Reset:	soft
Address:	E70D4h-E70D7h
Name:	Global Time Code Port D RX Current Value
ShortName:	GTC_PORT_RX_CURR_D
Power:	Always on
Reset:	soft
There is one instance of this register per port B, C, and D.	

DWord	Bit	Description
0	31:0	**GTC Port RX Current** This field contains the remote sink GTC value at the Aux sync point of the response message from the remote GTC sink. It is updated by hardware following a read of the remote sink GTC DPCD register.

GTC_PORT_TX_CURR

GTC_PORT_TX_CURR	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	E70B8h-E70BBh
Name:	Global Time Code Port B TX Current Value
ShortName:	GTC_PORT_TX_CURR_B
Power:	Always on
Reset:	soft
Address:	E70C8h-E70CBh
Name:	Global Time Code Port C TX Current Value
ShortName:	GTC_PORT_TX_CURR_C
Power:	Always on
Reset:	soft
Address:	E70D8h-E70DBh
Name:	Global Time Code Port D TX Current Value
ShortName:	GTC_PORT_TX_CURR_D
Power:	Always on
Reset:	soft
There is one instance of this register per port B, C, and D.	

DWord	Bit	Description
0	31:0	**GTC Port TX Current** This field contains the local GTC value sampled at the Aux sync point of the response message from remote GTC sink following software read of remote sink GTC DPCD register when PCH GTC controller is operating as master. When PCH GTC controller is operating as a slave this field contains the local GTC value sampled at the Aux sync point of the response message. In both master and slave mode this register is updated by hardware.

GTC_PORT_CTL

GTC_PORT_CTL	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	E70B0h-E70B3h
Name:	Global Time Code Port B Control
ShortName:	GTC_PORT_CTL_B
Power:	Always on
Reset:	soft
Address:	E70C0h-E70C3h
Name:	Global Time Code Port C Control
ShortName:	GTC_PORT_CTL_C
Power:	Always on
Reset:	soft
Address:	E70D0h-E70D3h
Name:	Global Time Code Port D Control
ShortName:	GTC_PORT_CTL_D
Power:	Always on
Reset:	soft
There is one instance of this register per port B, C, and D.	

DWord	Bit	Description
0	31	**Port GTC Enable** This bit enables the GTC controller to start lock acquisition phase with remote GTC sink connected to this port. The Maintenance_phase_enable bit must be initially written as '0' when this bit is set. This bit has no effect if the GTC controller is disabled.

Value	Name	Description
0b	Disable	GTC synchronization with remote sink disabled
1b	Enable	GTC synchronization with remote sink enabled

Programming Notes

GTC_PORT_CTL

When this port is enabled software must use the associated GTC Update Complete interrupt to determine that a hardware periodic update was completed prior to intiating a read from GTC remote slave.

Restriction	Project
Restriction : Prior to the LPT:H:B1 and LPT:LP:A1 steppings, Global Time Code hardware initiated periodic updates to remote GTC slave is not supported.	DevLPT:H, EXCLUDE(DevLPT:H:A), EXCLUDE(DevLPT:H:B0), EXCLUDE(DevLPT:LP:A0)

30:25 **Reserved**

24 **Maintenance Phase Enable**

This bit is used by software to transition from lock acquisition to lock maintenance phase.
The GTC controller generates an interrupt at the end of the lock phase as determined by lock acquisition duration field.
Software shall read the sink device GTC lock done bit. If set, software shall set this bit to '1' after first writing the GTC skew value to the RX GTC skew DPCD offset with GTC skew enable bit set to '1'.

Value	Name	Description
0b	Lock	Lock acquisition phase—the controller writes or reads GTC every 1ms
1b	Maintain	Lock maintenance phase—the controller writes or reads GTC every 10ms

23:2 **Reserved**

1 **GTC Port TX Lock Done**

This bit indicates the GTC controller operating in slave mode has achieved lock with the remote GTC sink.
This bit shall be written by software based on hardware compare results between GTC controller in slave mode and remote GTC master.
This bit shall be cleared by software when GTC controller is returned to lock acquisition phase.
Slave mode only

Value	Name	Description
0b	NoLock	GTC TX slave not locked
1b	Lock	GTC TX slave lock achieved

0 **GTC Port RX Lock Done**

This bit indicates the remote GTC sink has achieved lock.
This bit shall be written by software after reading remote GTC sink DPCD register.
This bit shall be cleared by software when GTC controller is reset from lock maintenance mode to lock acquisition mode or when the controller is disabled.

Value	Name	Description
0b	NoLock	GTC RX slave not locked
1b	Lock	GTC RX slave lock achieved

GTC_PORT_RX_CURR

GTC_PORT_RX_CURR	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	E70B4h-E70B7h
Name:	Global Time Code Port B RX Current Value
ShortName:	GTC_PORT_RX_CURR_B
Power:	Always on
Reset:	soft
Address:	E70C4h-E70C7h
Name:	Global Time Code Port C RX Current Value
ShortName:	GTC_PORT_RX_CURR_C
Power:	Always on
Reset:	soft
Address:	E70D4h-E70D7h
Name:	Global Time Code Port D RX Current Value
ShortName:	GTC_PORT_RX_CURR_D
Power:	Always on
Reset:	soft
There is one instance of this register per port B, C, and D.	

DWord	Bit	Description
0	31:0	**GTC Port RX Current** This field contains the remote sink GTC value at the Aux sync point of the response message from the remote GTC sink. It is updated by hardware following a read of the remote sink GTC DPCD register.

GTC_PORT_TX_CURR

GTC_PORT_TX_CURR	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	E70B8h-E70BBh
Name:	Global Time Code Port B TX Current Value
ShortName:	GTC_PORT_TX_CURR_B
Power:	Always on
Reset:	soft
Address:	E70C8h-E70CBh
Name:	Global Time Code Port C TX Current Value
ShortName:	GTC_PORT_TX_CURR_C
Power:	Always on
Reset:	soft
Address:	E70D8h-E70DBh
Name:	Global Time Code Port D TX Current Value
ShortName:	GTC_PORT_TX_CURR_D
Power:	Always on
Reset:	soft
There is one instance of this register per port B, C, and D.	

DWord	Bit	Description
0	31:0	**GTC Port TX Current** This field contains the local GTC value sampled at the Aux sync point of the response message from remote GTC sink following software read of remote sink GTC DPCD register when PCH GTC controller is operating as master. When PCH GTC controller is operating as a slave this field contains the local GTC value sampled at the Aux sync point of the response message. In both master and slave mode this register is updated by hardware.

TRANS_CONF

TRANS_CONF

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank OR transcoder disabled

Address:	F0008h-F000Bh
Name:	Transcoder A Config
ShortName:	TRANS_CONF_A
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31	**Transcoder Enable** Setting this bit to the value of one, turns on the transcoder. Turning the transcoder off disables the timing generator and synchronization pulses to the display will not be maintained. Transcoder timing registers must contain valid values before this bit is enabled. **Value / Name / Description** 0b / Disable / Disabled 1b / Enable / Enabled
	30	**Transcoder State** Access: RO This read only bit indicates the actual state of the transcoder. Since there can be some delay between disabling the transcoder and the transcoder actually shutting off, this bit indicates the true current state of the transcoder. **Value / Name / Description** 0b / Disabled / Transcoder is disabled 1b / Enabled / Transcoder is enabled
	29:24	**Reserved** Format: MBZ
	23:21	**Interlaced Mode** These bits are used for control of the transcoder interlaced mode.

TRANS_CONF

Value	Name	Description
000b	Progressive	Progressive
011b	Interlaced	Interlaced (north display must also be set to interlaced)
Others	Reserved	Reserved

20:0 **Reserved**

Format:	MBZ

FDI_RX_CTL

FDI_RX_CTL

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000040
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Depends on bit

Address:	F000Ch-F000Fh
Name:	FDI A RX Control
ShortName:	FDI_RX_CTL_A
Power:	Always on
Reset:	soft

The FDI Receiver only operates in 8 bit per color mode.
The FDI Receiver only operates in composite sync mode.

DWord	Bit	Description
0	31	**FDI Rx Enable** Disabling this port will put it in its lowest power state. Value / Name / Description: 0b / Disable / Disable the FDI Rx interface 1b / Enable / Enable the FDI Rx interface
	30:28	**Reserved** Format: MBZ
	27	**FS error correction enable** This bit enables the Fill Start error correction over FDI. Value / Name / Description: 0b / Disable / Disable FS Error Correction 1b / Enable / Enable FS Error Correction
	26	**FE error correction enable** This bit enables the Fill End error correction over FDI. Value / Name / Description: 0b / Disable / Disable FE Error Correction 1b / Enable / Enable FE Error Correction

FDI_RX_CTL

25 — FS error reporting enable

This bit enables the FS error reporting over FDI.

Value	Name	Description
0b	Disable	Disable FS Error Reporting
1b	Enable	Enable FS Error Reporting

24 — FE error reporting enable

This bit enables the FE error reporting over FDI.

Value	Name	Description
0b	Disable	Disable FE Error Reporting
1b	Enable	Enable FE Error Reporting

23:20 — Reserved

Format:	MBZ

19 — Port Width Selection

These bits select the number of lanes to be enabled on the link.
Port width change must be done as a part of mode set.
Locked once port is enabled. Updates when the port is disabled then re-enabled

Value	Name	Description
0b	x1 Mode	x1 Mode
1b	x2 Mode	x2 Mode
Others	Reserved	Reserved

18:17 — Reserved

Format:	MBZ

16 — Polarity Reversal

This bit allows FDI to work with polarity reversal. It must be set before the link is enabled.

Value	Name	Description
0b	Not Reversed	Polarity not reversed.
1b	Polarity Reversed	Polarity reversed.

15 — Link reversal strap override

FDI link automatically follows the DMI link reversal setting. This bit overrides that to the opposite of what DMI is set to.
It must be set before the link is enabled in order to take effect.

Value	Name	Description
0b	Not Overriden	Link reversal strap not overriden
1b	Overriden	Link reversal strap overriden.

14 — DMI Link reversal status

Access:	RO

This bit reflects the DMI link reversal strap.

FDI_RX_CTL

Value	Name	Description
0b	Not Reversed	Link not reversed
1b	Reversed	Link reversed.

13 FDI PLL enable

Format:	Enable

This bit enables the FDI PLL.

Restriction
Restriction : **After enabling the FDI PLL, software must wait for a warmup period before enabling the link. See the mode set sequence for more detail.**

12:11 Reserved

Format:	MBZ

10 FDI Auto Train

This bit enables FDI auto-training on this port.

Value	Name	Description
0b	Disable	Disable FDI auto-training
1b	Enable	Enable FDI auto-training

9:8 Reserved

7 Reserved

6 Enhanced Framing Enable

This bit selects enhanced framing.
Locked once port is enabled. Updates when the port is disabled then re-enabled

Value	Name	Description
0b	Disable	Enhanced framing disabled
1b	Enable **[Default]**	Enhanced framing enabled

5 Reserved

Format:	MBZ

4 Rawclk to PCDCLK selection

This bit switches PCH display clocking between the raw clock and PCDCLK.

Value	Name	Description
0b	Rawclk	Raw clock used
1b	PCDCLK	PCDCLK used

Restriction
Restriction : **This bit may be changed only at certain times. See the mode set sequence for more detail.**

3:0 Reserved

Format:	MBZ

FDI_RX_MISC

FDI_RX_MISC

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00200080
Access:	R/W
Size (in bits):	32
Address:	F0010h-F0013h
Name:	FDI A RX Miscellaneous
ShortName:	FDI_RX_MISC_A
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31:28	**Reserved** Format: MBZ
	27:26	**FDI RX Pwrdn Lane1** Default Value: 00h These bits control the power management state of the FDI Rx PHY.
	25:24	**FDI RX Pwrdn Lane0** Default Value: 00h These bits control the power management state of the FDI Rx PHY.
	23:22	**Reserved** Format: MBZ
	21:20	**TP1 to TP2 Time** These bits select the number of link clocks to count before transitioning from TP1 to TP2 during auto training. Value / Name / Description: 10b / 48 **[Default]** / 48 clocks 11b / 64 / 64 clocks **Note:** **Note:** This register must be written with the default TP1 to TP2 time before enabling FDI.

FDI_RX_MISC

	19	**Reserved** Format: MBZ
	18:16	**Bit Lock Timeout Time** These bits select the number of link clocks to count before timing out on bit lock during auto training.

Value	Name	Description
000b	128 **[Default]**	128 clocks
001b	256	256 clocks
010b	384	384 clocks
011b	512	512 clocks
100b	640	640 clocks
101b	768	768 clocks
110b	896	896 clocks
111b	1024	1024 clocks

	15:13	**Reserved** Format: MBZ
	12:0	**FDI Delay** This field specifies latency as relative delay with respect to the dot clock required for active data over the FDI interface to reach the timing generator FIFO in the transcoder.

Value	Name	Description
80h	80h **[Default]**	Default
90h	90h	Required for all FDI configurations

Note:
Note: Program 90h when FDI is used.

FDI_RX_IIR

FDI_RX_IIR

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/WC
Size (in bits):	32
Address:	F0014h-F0017h
Name:	FDI A RX Interrupt Identity
ShortName:	FDI_RX_IIR_A
Power:	Always on
Reset:	soft

See the interrupt bit definition table to find the source event for each interrupt bit.

DWord	Bit	Description
0	31:0	**Interrupt Identity Bits** This field holds the persistent values of the FDI_RX interrupt bits which are unmasked by the FDI_RX_IMR. Bits set in this register will propagate to the combined FDI_RX interrupt in the SDE_ISR. Bits set in this register will remain set (persist) until the interrupt condition is cleared by writing a '1' to the appropriate bits.

Value	Name	Description
0b	Condition Not Detected	Interrupt Condition Not Detected
1b	Condition Detected	Interrupt Condition Detected

FDI_RX_IMR

FDI_RX_IMR	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	F0018h-F001Bh
Name:	FDI A RX Interrupt Mask
ShortName:	FDI_RX_IMR_A
Power:	Always on
Reset:	soft

See the interrupt bit definition table to find the source event for each interrupt bit.

DWord	Bit	Description
0	31:0	**Interrupt Mask Bits** This field contains a bit mask which selects which FDI_RX events are reported in the FDI_RX_IIR.

Value	Name	Description
0b	Not Masked	Not Masked - will be reported in the FDI_RX_IIR
1b	Masked	Masked - will not be reported in the FDI_RX_IIR

FDI_RX_TUSIZE

FDI_RX_TUSIZE

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x7E000000
Access:	R/W
Size (in bits):	32
Address:	F0030h-F0033h
Name:	FDI A RX TU Size 1
ShortName:	FDI_RX_TUSIZE_1_A
Power:	Always on
Reset:	soft

Restriction

Restriction : The FDI Receiver TU size must be programmed to match the TU size used by the FDI Transmitter.

DWord	Bit	Description
0	31	**Reserved** Format: MBZ
	30:25	**TU Size** This field is the size of the transfer unit for FDI, minus one. Value: 111111b — Name: 63 **[Default]** [1,63]
	24:0	**Reserved** Format: MBZ

Graphics Memory Fence Table Registers 0-15

FENCE - Graphics Memory Fence Table Register	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	100000h-100007h
Name:	FENCE_0
Address:	100008h-10000Fh
Name:	FENCE_1
Address:	100010h-100017h
Name:	FENCE_2
Address:	100018h-10001Fh
Name:	FENCE_3
Address:	100020h-100027h
Name:	FENCE_4
Address:	100028h-10002Fh
Name:	FENCE_5
Address:	100030h-100037h
Name:	FENCE_6
Address:	100038h-10003Fh
Name:	FENCE_7
Address:	100040h-100047h
Name:	FENCE_8
Address:	100048h-10004Fh
Name:	FENCE_9
Address:	100050h-100057h
Name:	FENCE_10
Address:	100058h-10005Fh
Name:	FENCE_11

FENCE - Graphics Memory Fence Table Register

Address:	100060h-100067h
Name:	FENCE_12
Address:	100068h-10006Fh
Name:	FENCE_13
Address:	100070h-100077h
Name:	FENCE_14
Address:	100078h-10007Fh
Name:	FENCE_15

The graphics device performs address translation from linear space to tiled space for a CPU access to graphics memory (See Memory Interface Functions chapter for information on these memory layouts) using the fence registers. Note that the fence registers are used only for CPU accesses to gfx memory. Graphics rendering/display pipelines use Per Surface Tiling (PST) parameters (found in SURFACE_STATE - see the Sampling Engine chapter) to access tiled gfx memory.

The intent of tiling is to locate graphics data that are close (in X and Y surface axes) in one physical memory page while still locating some amount of line oriented data sequentially in memory for display efficiency. All 3D rendering is done such that the QWords of any one span are all located in the same memory page, improving rendering performance. Applications view surfaces as linear, hence when the cpu access a surface that is tiled, the gfx hardware must perform linear to tiled address conversion and access the correct physical memory location(s) to get the data.

Tiled memory is supported for rendering and display surfaces located in graphics memory. A tiled memory surface is a surface that has a width and height that are subsets of the tiled region's pitch and height. The device maintains the constants required by the memory interface to perform the address translations. Each tiled region can have a different pitch and size. The CPU-memory interface needs the surface pitch and tile height to perform the address translation. It uses the GMAddr (PCI-BAR) offset address to compare with the fence start and end address, to determine if the rendering surface is tiled. The tiled address is generated based on the tile orientation determined from the matching fence register. Fence ranges are at least 4 KB aligned. Note that the fence registers are used only for CPU accesses to graphics memory.

A Tile represents 4 KB of memory. Tile height is 8 rows for X major tiles and 32 rows for Y major tiles. Tile Pitch is 512Bs for X major tiles and 128Bs for Y major tiles. The surface pitch is programmed in 128B units such that the pitch is an integer multiple of "tile pitch".

Engine restrictions on tile surface usage are detailed in Surface Placement Restrictions (Memory Interface Functions). Note that X major tiles can be used for Sampler, Color, Depth, motion compensation references and motion compensation destination, Display, Overlay, GDI Blt source and destination surfaces. Y major tiles can be used for Sampler, depth, color and motion compensation assuming they do not need to be displayed. GDI Blit operations, overlay and display cannot used Tiled Y orientations.

A "PST" graphics surface that will also be accessed via fence needs its base address to be tile row aligned. Hardware handles the flushing of any pending cycles when software changes the fence upper/lower bounds. Fence Table Registers occupy the address range specified above. Each Fence Table Register has the following format.

FENCE registers are not reset by a graphics reset. They will maintain their values unless a full chipset reset is performed.

<table>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td>0</td><td>63:44</td><td>Fence Upper Bound
<table>
<tr><td>Project:</td><td>All</td></tr>
<tr><td>Format:</td><td>GraphicsAddress[31:12]</td></tr>
</table>
Bits 31:12 of the ending Graphics Address of the fence region. Fence regions must be aligned to a 4KB page. This address represents the last 4KB page of the fence region (Upper Bound is included in the fence region).
Graphics Address is the offset within GMADR space.</td></tr>
<tr><td></td><td>43:42</td><td>Reserved
<table>
<tr><td>Format:</td><td>MBZ</td></tr>
</table></td></tr>
<tr><td></td><td>41:32</td><td>Fence Pitch
<table>
<tr><td>Project:</td><td>All</td></tr>
<tr><td>Format:</td><td>U10-1 Width in 128 bytes</td></tr>
</table>
This field specifies the width (pitch) of the fence region in multiple of "tile width". For Tile X this field must be programmed to a multiple of 512B ("003" is the minimum value) and for Tile Y this field must be programmed to a multiple of 128B ("000" is the minimum value).

000h = 128B
001h = 256B
...
3FFh = 128KB</td></tr>
<tr><td></td><td>31:12</td><td>Fence Lower Bound
<table>
<tr><td>Project:</td><td>All</td></tr>
<tr><td>Format:</td><td>GraphicsAddress[31:12]</td></tr>
</table>
Bits 31:12 of the starting Graphics Address of the fence region. Fence regions must be aligned to 4KB. This address represents the first 4KB page of the fence region (Lowe Bound is included in the fence region).
Graphics Address is the offset within GMADR space.</td></tr>
<tr><td></td><td>11:2</td><td>Reserved
<table>
<tr><td>Project:</td><td>All</td></tr>
<tr><td>Format:</td><td>MBZ</td></tr>
</table></td></tr>
<tr><td></td><td>1</td><td>Tile Walk
<table>
<tr><td>Project:</td><td>All</td></tr>
</table>
This field specifies the spatial ordering of QWords within tiles.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr>
<tr><td>0h</td><td>MI_TILE_XMAJOR</td><td>Consecutive SWords (32 Bytes) sequenced in the X direction</td><td>All</td></tr>
<tr><td>1h</td><td>MI_TILE_YMAJOR</td><td>Consecutive OWords (16 Bytes) sequenced in the Y direction</td><td>All</td></tr>
</table></td></tr>
</table>

FENCE - Graphics Memory Fence Table Register

	0	**Fence Valid** Project: All Format: MI_FenceValid This field specifies whether or not this fence register defines a fence region.

Value	Name	Project
0h	MI_FENCE_INVALID	All
1h	MI_FENCE_VALID	All

LCPLL_CTL

LCPLL_CTL

Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000 [HSW]
Access:	R/W
Size (in bits):	32
Address:	130040h-130043h
Name:	LCPLL Control
ShortName:	LCPLL_CTL
Power:	Always on
Reset:	global

Description	Project
This register is also known as GT Scratchpad 0 or GTSP0. The LC PLL drives the display core clock (CDCLK) and the core display 2X clock (CD2XCLK). The LC PLL can drive the DDI ports at fixed frequencies for DisplayPort. The LC PLL will automatically adjust for the reference frequency based on the reference select straps.	
This register is reset by the device 2 FLR.	DevHSW:GT0:X0, DevHSW:GT3:A
This register is not reset by the device 2 FLR.	DevHSW, EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A)

Restriction	Project
Restriction : This register can be written, but the programming will not affect the PLL.	DevHSW:GT0:X0

DWord	Bit	Description
0	31	**PLL Disable** This bit will enable or disable the PLL. Value / Name: 0b – Enable 1b – Disable Restriction : After reset, this must not be changed while CD and CD2X clocks are enabled.

LCPLL_CTL

	30	**PLL Lock** Project: DevHSW, EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A) Access: RO This read only bit indicates the status of the PLL lock. **Value** / **Name** 0b: Not locked or not enabled 1b: Locked
	30	**Reserved** Project: DevHSW:GT0:X0, DevHSW:GT3:A Format: MBZ
	29:28	**Reference Select** Select between PLL references. **Value** / **Name** / **Description** 00b / Non-SSC / Non-Spread reference 01b / Reserved / Reserved **Restriction** Restriction : This must not be changed while this PLL is enabled.
	27:26	**CD Frequency Select** Project: DevHSW, EXCLUDE(DevHSW:GT0:X0) Select between frequencies for CD clock. CD2X clock is always twice the frequency of CD clock. When the fuse DISPLAY_CDCLK_LIMIT = 1, display hardware will ignore the CD Frequency Select and only allow 450 MHz. The CD Frequency should only be changed when following Display Sequences for Changing CD Clock Frequency. **Value** / **Name** / **Description** 00b / 450 MHz / 450 MHz CD clock 01b / Alternate / Non-ULT and Non-ULX: 540 MHz CD clock. **ULT: Not supported. Do not select.** ULX: 337.5 MHz CD clock. 10b / Reserved / Reserved 11b / Reserved / Reserved **Restriction** / **Project** Restriction : The CD clock frequency selected here must be programmed into the CDCLK_FREQ register. / DevHSW:GT3:A
	27:25	**Reserved** Project: DevHSW:GT0:X0

LCPLL_CTL

	Format:	MBZ

25 **CD Clock Disable**

Project:	DevHSW, EXCLUDE(DevHSW:GT0:X0)

This bit will enable or disable the CD clock for the Display Engine.

Value	Name
0b	Enable
1b	Disable

Restriction	Project
Restriction : Do not disable the clock on these steppings.	DevHSW:GT0:X0, DevHSW:GT3:A, DevHSW:GT3:B

24 **Root CD2X Clock Disable**

This bit will enable or disable the root of the CD2X clock for the Display Engine. This is the source of both the CD2X and CD clock within display.

Value	Name
0b	Enable
1b	Disable

Restriction	Project
Restriction : Do not disable the clock on these steppings.	DevHSW:GT0:X0, DevHSW:GT3:A, DevHSW:GT3:B

23 **CD2X Clock Disable**

Project:	DevHSW, EXCLUDE(DevHSW:GT0:X0)

This bit will enable or disable the CD2X clock for the Display Engine.

Value	Name
0b	Enable
1b	Disable

Restriction	Project
Restriction : Do not disable the clock on these steppings.	DevHSW:GT0:X0, DevHSW:GT3:A, DevHSW:GT3:B

23 **Reserved**

Project:	DevHSW:GT0:X0
Format:	MBZ

22 **Display Power Down Allow**

Project:	DevHSW, EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A)

This field indicates to the PCU that it is allowed to power down all display power wells. When allowed, the PCU can save the display context and power down display power wells.

LCPLL_CTL

Value	Name	Description
0b	Do not allow	Do not allow display power down
1b	Allow	Allow display power down

Restriction
Restriction : This field should only be changed as part of the display sequence for package C8.

21 **CD Source Select**

Project:	DevHSW, EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A)

This bit selects the source for CD clock.

Value	Name	Description
0b	LCPLL	CD clock source is LCPLL
1b	Fclk	CD clock source is Fclk

Restriction
Restriction : This field should only be changed as part of the display sequence for package C8.

20 **CD Source Switching**

Project:	DevHSW, EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A)
Access:	RO

This read only bit indicates when the CD clock source switch from LCPLL to Fclk is in progress.

Value	Name	Description
0b	Not in progress	CD clock source switch to Fclk not in progress
1b	In progress	CD clock source switch to Fclk in progress

22:19 **Reserved**

Project:	DevHSW:GT0:X0, DevHSW:GT3:A
Format:	MBZ

19 **CD Source Fclk**

Project:	DevHSW, EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A)
Access:	RO

This read only bit indicates when the CD clock source switch from LCPLL to Fclk is done.

Value	Name	Description
0b	Not done	CD clock source switch to Fclk not done
1b	Done	CD clock source switch to Fclk done

18:6 **Reserved**

Format:	MBZ

5 **Write Once Dev3 SID**

Project:	DevHSW, EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A),

	EXCLUDE(DevHSW:GT3:B)
Access:	RO

This read only bit indicates the write once status for register sid_0_3_0_pci_sid.

Value	Name
0b	Not written
1b	Written

4 **Write Once Dev3 SVID**

Project:	DevHSW, EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A), EXCLUDE(DevHSW:GT3:B)
Access:	RO

This read only bit indicates the write once status for register svid_0_3_0_pci_svid.

Value	Name
0b	Not written
1b	Written

3 **Write Once Dev3 Next**

Project:	DevHSW, EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A), EXCLUDE(DevHSW:GT3:B)
Access:	RO

This read only bit indicates the write once status for register pid_0_3_0_pci_next.

Value	Name
0b	Not written
1b	Written

2 **Write Once Dev2 SUBID**

Project:	DevHSW, EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A), EXCLUDE(DevHSW:GT3:B)
Access:	RO

This read only bit indicates the write once status for register sid2_0_2_0_pci_subid.

Value	Name
0b	Not written
1b	Written

1 **Write Once Dev2 SUBVID**

Project:	DevHSW, EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A), EXCLUDE(DevHSW:GT3:B)
Access:	RO

This read only bit indicates the write once status for register svid2_0_2_0_pci_subvid.

Value	Name
0b	Not written

LCPLL_CTL

		1b: Written
	5:0	**Reserved** Project: DevHSW:GT0:X0, DevHSW:GT3:A, DevHSW:GT3:B Format: MBZ
	0	**Write Once Dev2 SMISCISEL** Project: DevHSW, EXCLUDE(DevHSW:GT0:X0), EXCLUDE(DevHSW:GT3:A), EXCLUDE(DevHSW:GT3:B) Access: RO This read only bit indicates the write once status for register swsci_0_2_0_pci_smiscisel. 0b: Not written 1b: Written

Global Capabilities, Minor and Major Version

GCAP_VMIN_VMAJ - Global Capabilities, Minor and Major Version

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x01002001
Access:	RO
Size (in bits):	32
Address:	00000h-00003h

DWord	Bit	Description
0	31:24	**Major Version** Value / Name / Description 01h / **[Default]** / Indicates major revision number 1 of the High Definition Audio specification, for specification version '1.0.' Should be reset to '01h' **Programming Notes** Should be hardwired to "01h".
	23:16	**Minor version** Value / Name / Description 00h / **[Default]** / Indicates minor revision number 00h of the High Definition Audio specification, for specification version '1.0.' Reset to '00h' **Programming Notes** Should be hardwired to "00h".
	15:12	**Output Streams** Value / Name / Description 0010b / **[Default]** / [All] A value of 0000b indicates that there are no Output Streams supported. A value of maximum 15 output streams are supported. [DevHSW] Two streams for HSW **Programming Notes** Should be hardwired to "0010b".
	11:8	**Input Streams** Value / Name / Description / Project 0000b / / A value of 0000b indicates that there are no Input Streams supported. A maximum of 15 input streams are supported. / All

GCAP_VMIN_VMAJ - Global Capabilities, Minor and Major Version

Programming Notes
Should be hardwired to "0000b".

7:3 **BiDirectional Streams**

Value	Name	Description
0000b		A value of 0000b indicates that there are no Input Streams supported. A maximum of 15 input streams are supported.

Programming Notes
Should be hardwired to "0000b".

2:1 **Number of SDO Signal**

Software can enable the use of striping by setting the appropriate bit in the Stream Buffer Descriptor.

Value	Name	Description	Project
00b	**[Default]**	Indicates that one SDO line is supported	HSW
01b		Indicates that two SDO lines are supported.	
10b		Indicates that four SDO lines are supported.	
11b	Reserved		

0 **64 Addr Support**

Value	Name	Description
1b	**[Default]**	Indicates that 64 bit addressing is supported by the controller for BDL addresses, data buffer addresses, and command buffer addresses.
0b		Indicates that only 32-bit addressing is available. We support 64 bit addresses but the 64:39 are zeros.

Programming Notes
Must be hardwired to "1b".

Output Payload and Input payload Capability

OUTPAY_INPAY - Output Payload and Input payload Capability

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x003C001D
Access:	RO
Size (in bits):	32
Address:	00004h-00007h

DWord	Bit	Description
0	31:16	**Input Payload** Indicates the total input payload available on the link. This does not include bandwidth used for command and control. This measurement is in 16-bit Word quantities per 48-kHz frame. The default link clock speed of 24.000 MHz provides 500 bits per frame, or 31.25 Words. 36 bits (2.25 Words) are used for command and control, leaving 29 words for payload. This measurement is on a per-codec basis.

Value	Name	Description
003Ch	**[Default]**	
0-FFh		0000h: 0 Words 0001h: 1 Word payload ... 0003Ch: 60 Word payload [Default] ... 00FFh: 255 Word payload

DWord	Bit	Description
	15:0	**Output payload** Indicates the total output payload available on the link. This does not include bandwidth used for command and control. This measurement is in 16-bit Word quantities per 48-kHz frame. The default link clock speed of 24.000 MHz (the data is double pumped) provides 1000 bits per frame, or 62.5 Words in total. Forty bits (2.5 Words) are used for command and control, leaving 60 Words available for data payload. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines.

Value	Name	Description
001Dh	**[Default]**	

OUTPAY_INPAY - Output Payload and Input payload Capability				
		0-FFh	OUTPAY	0000h: 0 Words 0001h: 1 Word payload ... 003Ch: 60 Word payload ... 00FFh: 255 Word payload

Global Control

GCTL - Global Control

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	00008h-0000Bh

DWord	Bit	Description
0	31:9	**Reserved** Format: MBZ
	8	**UNSOL** Value / Name / Description: 0b / Disable **[Default]** / Unsolicited responses are not accepted, and dropped on the floor. 1b / Enable / Unsolicited Responses from the codecs are accepted by the controller and placed into the Response Input Ring Buffer. **Programming Notes** This should be programmed to 1 by the driver.
	7:2	**Reserved** Format: MBZ
	1	**FCNTRL** Access: R/W Set Value / Name / Description: 0b / Disable **[Default]** / Flush is completed 1b / Enable / Flush Initiated **Programming Notes** Writing a 1 to this bit initiates a flush. When the flush completion is received by the controller, hardware sets the Flush Status bit and clears this Flush Control bit. Before a flush cycle is initiated, the DMA Position Buffer must be programmed with a valid memory address by software, but the DMA Position Buffer bit 0 need not be set to enable the position reporting mechanism. Also, all streams must be stopped (the associated RUN bit must be 0).

GCTL - Global Control

When the flush is initiated, the controller will flush pipelines to memory to guarantee that the hardware is ready to transition to a D3 state. Setting this bit is not a critical step in the power state transition if the content of the FIFOs is not critical.

0 **CRST**

Value	Name	Description
0b	Disable **[Default]**	Enter Reset State-Writing a 0 to this bit causes the Intel HD Audio controller to be reset. All state machines, FIFO's and non Suspend well memory mapped configuration registers (except ECAP and PCI Configuration Registers) in the controller will be reset. The Intel HD Audio link RESET# signal will be asserted and all other link signals will be driven to their "reset" values. After the hardware has completed sequencing into the reset state, it will report a 0 in this bit. Software must read a 0 from this bit to verify that the controller is in reset.
1b	Enable	Exit Reset State- Writing a 1 to this bit causes the controller to exit its reset state and de-assert the Intel HD Audio link RESET# signal. Software is responsible for setting/clearing this bit such that the minimum Intel HD Audio link RESET# signal assertion pulse width specification is met. When the controller hardware is ready to begin operation, it will report a 1 in this bit. Software must read a 1 from this bit before accessing any controller registers. The CRST# bit defaults to a 0 after hardware reset, therefore software needs to write a 1 to this bit to begin operation.

Programming Notes

Note that the CORB/RIRB RUN bits and all Stream RUN bits must be verified cleared to zero before CRST# is written to 0 (asserted) in order to assure a clean re-start. When setting or clearing CRST#, software must ensure that minimum link timing requirements (minimum RESET# assertion
time, etc.) are met. When CRST# is 0 indicating that the controller is in reset, writes to all Intel HD Audio memory mapped registers are ignored as if the device is not present. The only exception is the Global Control register containing the CRST# bit itself. The Global Control register is write-able as a DWord, Word, or Byte even when CRST# is 0 if the byte enable for the byte containing the CRST# bit (Byte Enable 0) is active. If Byte Enable 0 is not active, writes to the Global Control register will be ignored when CRST# is 0. When CRST# is 0, reads to Intel HD Audio memory mapped registers will return their default value except for registers that are not reset with PLTRST# or on a D3hot -> D0 transition.

Wake Enable and Wake Status

WAKEEN_WAKESTS - Wake Enable and Wake Status

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0000Ch-0000Fh

DWord	Bit	Description
0	31:17	**Reserved** Format: MBZ
	16	**SDIWAKE** Default Value: 0b Access: R/WC **Programming Notes** Flag bits that indicate which SDI signal(s) received a "State Change" event. The bits are cleared by writing 1's to them. These bits are in the Suspend well and only cleared on a power-on reset. Software must not make assumptions about the reset state of these bits and must set them appropriately.
	15:1	**Reserved** Format: MBZ
	0	**SDIWEN** Value / Name / Description: 0b / Disable **[Default]** / SDI is disabled 1b / Enable / SDI is enabled to generate wake event. **Programming Notes** Bits which control which SDI signal(s) may generate a wake event. A '1' bit in the bit mask indicates that the associated SDIN signal is enabled to generate a wake. These bits are in the Suspend well and only cleared on a power-on reset. Software must not make assumptions about the reset state of these bits and must set them appropriately.

Global Status

GSTS - Global Status

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000002
Access:	R/W
Size (in bits):	32
Address:	00010h-00013h

DWord	Bit	Description
0	31:2	**Reserved** Format: MBZ
	1	**FSTS** Default Value: 0bh Access: R/WC **Programming Notes** This bit is set to a 1 by the hardware to indicate that the flush cycle initiated when the FCNTRL bit was set has completed. Software must write a 1 to clear this bit before the next time FCNTRL is set.
	0	**Reserved** Format: MBZ

Output/Input Stream Payload Capability

OUTSTRMPAY_INSTRMPAY - Output/Input Stream Payload Capability

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000030
Access:	RO
Size (in bits):	32
Address:	00018h-0001Bh

DWord	Bit	Description
0	31:16	**INSTRMPAY** **Value** / **Name** / **Description** 0000h / **[Default]** / 0 word 1-00FFh / / 1 word payload - 255 word payload **Programming Notes** Input Stream Payload Capability (INSTRMPAY): Indicates maximum number of words per frame for any single input stream. This measurement is in 16 bit word quantities per 48 kHz frame. 24 Words (48B) is the maximum supported, therefore a value of 18h is reported in this register. Software must ensure that a format which would cause more words per frame than indicated is not programmed into the Input Stream Descriptor register.
	15:0	**OUTSTRMPAY** **Value** / **Name** / **Description** 0-00FFh / / 0 words - 255 word payload 0030h / **[Default]** /

Interrupt Control

INTCTL - Interrupt Control

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	00020h-00023h

DWord	Bit	Description
0	31	**Global Interrupt Enable** Value / Name / Description: 0h / Disable **[Default]** / GIE is disabled 1h / Enable / GIE is enabled **Programming Notes** Global bit to enable device interrupt generation. When set to 1 the Intel HD Audio function is enabled to generate an interrupt. This control is in addition to any bits in the bus specific address space, such as the Interrupt Enable bit in the PCI Configuration Space. This bit is not affected by controller reset.
	30	**Controller Interrupt Enable** Value / Name / Description: 0h / Disable **[Default]** / CIE is disabled 1h / Enable / CIE is enabled **Programming Notes** Thsi bit Enables the general interrupt for controller functions. When set to 1 (and GIE is enabled), the controller generates an interrupt when the CIS bit gets set. This bit is not affected by controller reset.
	29:3	**Reserved** Format: MBZ
	2	**Reserved** Project: HSW
	1:0	**Stream Interrupt Enable** Project: HSW

INTCTL - Interrupt Control

Value	Name	Description
00b	Disable **[Default]**	All stream interrupts disabled
01b	Stream 1 Enable	Output Stream 1 interrupt enabled
10b	Stream 2 Enable	Output Stream 2 interrupt enabled
11b	Both Enable	Both streams interrupt enabled

Programming Notes

When set to 1 the individual Streams are enabled to generate an interrupt when the corresponding stream status bits get set. A stream interrupt will be caused as a result of a buffer with IOC=1 in the BDL entry being completed, or as a result of a FIFO error (underrun or overrun) occurring. Control over the generation of each of these sources is in the associated Stream Descriptor.

The streams are numbered and the SIE bits assigned sequentially, based on their order in the register set.

Bit 0: Output Stream 1

Bit 1: Output Stream 2

Interrupt Status

INTSTS - Interrupt Status

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W Variant
Size (in bits):	32
Address:	00024h-00027h

DWord	Bit	Description
0	31	**Global Interrupt Status** Access: RO **Value / Name / Description** 0b / Off **[Default]** / Interrupt off 1b / On / Interrupt on **Programming Notes** This bit is an OR of all of the interrupt status bits in this register.
	30	**Controller Interrupt Status** **Value / Name / Description** 0b / Off **[Default]** / Interrupt off 1b / On / Interrupt on **Programming Notes** Status of general controller interrupt. A 1 indicates that an interrupt condition occurred due to a Response Interrupt, a Response Buffer Overrun Interrupt, CORB Memory Error Interrupt, Error Present Interrupt (Intel Reserved), or a SDIN State Change event. The exact cause can be determined by interrogating other registers. Note that a HW interrupt will not be generated unless the corresponding enable bit is set. This bit is an OR of all of the stated interrupt status bits for this register.
	29:3	**Reserved** Format: MBZ
	2	**Reserved** Project: HSW
	1	**Stream Interrupt Status 2**

INTSTS - Interrupt Status

Value	Name	Description
0	Off **[Default]**	Stream interrupt off
1	On	Stream interrupt On

Programming Notes

A '1' indicates that an interrupt condition occurred on the corresponding Stream. Note that a HW interrupt will not be generated unless the corresponding enable bit is set. This bit is an OR of all of an individual stream's interrupt
status bits.
The streams are numbered and the SIS bits assigned sequentially, based on their order in the register set.
Bit 1: Output Stream 2

0 **Stream Interrupt Status 1**

Value	Name	Description
0	Off **[Default]**	Stream interrupt off
1	On	Stream interrupt On

Programming Notes

A '1' indicates that an interrupt condition occurred on the corresponding Stream. Note that a HW interrupt will not be generated unless the corresponding enable bit is set. This bit is an OR of all of an individual stream's interrupt
status bits.
The streams are numbered and the SIS bits assigned sequentially, based on their order in the register set.
Bit 0: Output Stream 1

Wall Clock Counter

WALCLK - Wall Clock Counter

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO Variant
Size (in bits):	32
Address:	00030h-00033h

DWord	Bit	Description
0	31:0	**Wall Clock Counter** Default Value: 0h Wall Clock Counter (Counter): 32 bit counter that is incremented on each link BCLK (24MHz) period and rolls over from FFFF_FFFFh to 0000_0000h. This counter will roll over to zero with a period of approximately 179 seconds. This counter is enabled when the controller is out of reset (CRST is 1). Software uses this counter to synchronize between multiple controllers. Will be reset on controller reset.

Stream Synchronization

SSYNC - Stream Synchronization

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	00038h-0003Bh

DWord	Bit	Description
0	31:2	**Reserved** Project: HSW Format: MBZ
	1	**Stream Synchronization Bit 2** when set to 1, block data from being sent on or received from the link. Each bit controls the associated Stream Descriptor; bit 0 corresponds to the first Stream Descriptor, etc. To synchronously start a set of DMA engines, the bits in the SSYNC register are first set to a 1. The RUN bits for the associated Stream Descriptors are then set to a 1 to start the DMA engines. Value / Name / Description: 0b / Disable **[Default]** / Sync Disabled for the stream 2 1b / Enable / Sync Enabled for the stream 2 **Programming Notes** When all streams are ready (FIFORDY=1), the associated SSYNC bits can all be set to 0 at the same time, and transmission or reception of bits to or from the link will begin together at the start of the next full link frame. To synchronously stop streams, first the bits are set in the SSYNC register, and then the individual RUN bits in the Stream Descriptors are cleared by software. The streams are numbered and the SSYNC bits assigned sequentially, based on their order in the register set. Bit 1: Output Stream 2
	0	**Stream Synchronization Bit 1** when set to 1, block data from being sent on or received from the link. Each bit controls the associated Stream Descriptor; bit 0 corresponds to the first Stream Descriptor, etc. To synchronously start a set of DMA engines, the bits in the SSYNC register are first set to a 1. The RUN bits for the associated Stream Descriptors are then set to a 1 to start the DMA engines. Value / Name / Description: 0b / Disable **[Default]** / Sync Disabled for the stream 1

SSYNC - Stream Synchronization

1b	Enable	Sync Enabled for the stream 1

Programming Notes

When all streams are ready (FIFORDY=1), the associated SSYNC bits can all be set to 0 at the same time, and transmission or reception of bits to or from the link will begin together at the start of the next full link frame.

To synchronously stop streams, first the bits are set in the SSYNC register, and then the individual RUN bits in the Stream Descriptors are cleared by software. The streams are numbered and the SSYNC bits assigned sequentially, based on their order in the register set.

Bit 0: Output Stream 1

CORB (Command Output Ring Buffer)- Lower Base Address

CORBLBASE - CORB (Command Output Ring Buffer)- Lower Base Address

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	00040h-00043h

DWord	Bit	Description
0	31:7	**CORBLBASE** Default Value: 0h Lower address of the Command Output Ring Buffer, allowing the CORB Base Address to be assigned on any 128-B boundary. **Programming Notes** This field must not be written when the DMA engine is running or the DMA transfer may be corrupted.
	6:0	**CORBLBASE LOWER BITS** Default Value: 0h Access: RO CORB Lower Base Unimplemented Bits: Hardwired to 0. This requires the CORB to be allocated with 128-byte granularity to allow for cache line fetch optimizations.

CORB (Command Output Ring Buffer)- Upper Base Address

CORBUBASE - CORB (Command Output Ring Buffer)- Upper Base Address

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	00044h-00047h

DWord	Bit	Description
0	31:0	**CORBUBASE** Upper 32 bits of address of the Command Output Ring Buffer. **Programming Notes** This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.

CORB Read/Write Pointers

CORBRWP - CORB Read/Write Pointers

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	00048h-0004Bh

DWord	Bit	Description
0	31	**CORB Read Pointer Reset** Access: R/W Variant Value / Name / Description: 0b – Clear_Reset **[Default]** – See ProgramminNotes 1b – Set_Reset – See ProgrammingNotes **Programming Notes** Software writes a 1 to this bit to reset the CORB Read Pointer to 0 and clear any residual pre-fetched commands in the CORB hardware buffer within the Intel Audio controller. The hardware will physically update this bit to 1 when the CORB Pointer reset is complete. Software must read a 1 to verify that the reset completed correctly. Software must clear this bit back to 0 and read back the 0 to verify that the clear completed correctly. The CORB DMA engine must be stopped prior to resetting the Read Pointer or else DMA transfer may be corrupted.
	30:24	**Reserved** Format: MBZ
	23:16	**CORB Read Pointer** Default Value: 00h Access: RO Variant **Programming Notes** Software reads this field to determine how many commands it can write to the CORB without over-running. The value read indicates the CORB Read Pointer offset in Dword granularity. The offset entry read from this field has been successfully fetched by the DMA controller and may be over-written by software. Supports 256 CORB entries (256 x 4B=1KB). This field may be read while the DMA engine is running.
	15:8	**Reserved**

CORBRWP - CORB Read/Write Pointers

		Format: MBZ
	7:0	**CORB Write Pointer** Default Value: 00h Access: R/W **Programming Notes** Software writes the last valid CORB entry offset into this field in Dword granularity. The DMA engine fetches commands from the CORB until the Read Pointer matches the Write Pointer. Supports 256 CORB entries (256 x 4B=1KB). This field may be written while the DMA engine is running.

CORB Control_Status_Size

CORBCTL_STS_SIZE - CORB Control_Status_Size

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00420000
Access:	R/W
Size (in bits):	32
Address:	0004Ch-0004Fh

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:20	**CORB Size Capability** Default Value: 4h Access: RO **Programming Notes** The default value, 0100b, indicates that the PCH only supports a CORB size of 256 CORB entries (1024B).
	19:18	**Reserved** Format: MBZ
	17:16	**CORB SIZE** Default Value: 10b Access: RO **Programming Notes** The default value, 0100b, indicates that the PCH only supports a CORB size of 256 CORB entries (1024B).
	15:9	**Reserved** Format: MBZ
	8	**CMEI** Default Value: 0b **Programming Notes** **Memory Error (CMEI):** Hardwired to '0' as memory errors are not tracked.

CORBCTL_STS_SIZE - CORB Control_Status_Size

7:2	**Reserved** Format: MBZ
1	**Enable CORB DMA Engine** Access: R/W Variant

Value	Name	Description
0b	DMA Stop	See ProgramminNotes
1b	DMA Run	See ProgramminNotes

Programming Notes
After SW writes a 0 to this bit, the HW may not stop immediately. The hardware will physically update the bit to a 0 when the DMA engine is truly stopped. SW must read a 0 from this bit to verify that the DMA is truly stopped.

0	**Memory Error Interrupt Enable** Access: R/W

Value	Name	Description
0b	Disable **[Default]**	Disable MEI
1b	Enable	Enable MEI

Programming Notes
The access to this bit field is RW but no functionality as memory errors are not tracked.

RIRB (Response Input Ring Buffer)-Lower Base Address

RIRBLBASE - RIRB (Response Input Ring Buffer)-Lower Base Address

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	00050h-00053h

DWord	Bit	Description
0	31:7	**RIRBLBASE** Default Value: 0h **Programming Notes** Lower address of the Response Input Ring Buffer (RIRBLBASE) allows the RIRB Base Address to be assigned on any 128-B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.
	6:0	**RIRBLBASE LOWER BITS** Default Value: 0h Access: RO **Programming Notes** Hardwired to 0 to force 128-byte buffer alignment for cache line fetch optimizations.

RIRB (Response Input Ring Buffer)-Upper Base Address

RIRBUBASE - RIRB (Response Input Ring Buffer)-Upper Base Address

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	00054h-00057h

DWord	Bit	Description
0	31:0	**RIRBUBASE** Default Value: 0h **Programming Notes** Upper 32 bits of address of the Response Input Ring Buffer. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.

RIRB Write Pointer and Interrupt Count

RIRBWP_RINTCNT - RIRB Write Pointer and Interrupt Count

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	00058h-0005Bh

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:16	**Response Interrupt Count** Access: RO The DMA engine should be stopped when changing this field or else an interrupt may be lost. Note that each Response occupies 2 Dwords in the RIRB. This is compared to the total number of responses that have been returned, as opposed to the number of frames in which there were responses. If more than one codec responds in one frame, then the count is increased by the number of responses received in the frame.

Value	Name	Description
00000001b		1 Response sent to RIRB
00000010b-11111111b		2 - 255 Response sent to RIRB
00000000b	**[Default]**	256 Responses sent to RIRB

	15	**RIRB Write Pointer Reset** Default Value: 0b Access: WO

Programming Notes

Software writes a 1 to this bit to reset the RIRB Write Pointer to 0's. The RIRB DMA engine must be stopped prior to resetting the Write Pointer or else DMA transfer may be corrupted. This bit will always be read as 0.

	14:8	**Reserved** Format: MBZ
	7:0	**RIRB Write Pointer** Default Value: 00h

RIRBWP_RINTCNT - RIRB Write Pointer and Interrupt Count		
		Access: RO Variant): Indicates the last valid RIRB entry written by the DMA controller. Software reads this field to determine how many responses it can read from the RIRB. The value read indicates the RIRB Write Pointer offset in 2 Dword RIRB entry units (since each RIRB entry is 2 Dwords long). Supports up to 256 RIRB entries (256 x 8B=2KB). This field may be read while the DMA engine is running.

RIRB Control, Status and Size

RIRBCTL_STS_SIZE - RIRB Control, Status and Size

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00420000
Access:	R/W
Size (in bits):	32
Address:	0005Ch-0005Fh

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:20	**RIRB Size Capability** Default Value: 4h Access: RO **Programming Notes** Default of 0100b indicates that the dHDA only supports a RIRB size of 256 RIRB entries (2048B).
	19:18	**Reserved** Format: MBZ
	17:16	**RIRB Size** Default Value: 10b Access: RO **Programming Notes** Thsi bit field is hardwired to 10b which sets the RIRB size to 256 entries (2048B).
	15:11	**Reserved** Format: MBZ
	10	**Response Overrun Interrupt Status** Access: R/WC

Value	Name	Description
0b	No_Overrun **[Default]**	See ProgramminNotes
1b	Overrun	See ProgramminNotes

RIRBCTL_STS_SIZE - RIRB Control, Status and Size

Programming Notes
Hardware sets this bit to a 1 when the RIRB DMA engine is not able to write the incoming responses to memory before additional incoming responses overrun the internal FIFO. When the overrun occurs, the hardware will drop the responses which overrun the buffer. An interrupt may be generated if the Response Overrun Interrupt Control bit is set. Note that this status bit is set even if an interrupt is not enabled for this event. Software clears this flag by writing a 1 to this bit.

9 **Reserved**

Format:	MBZ

8 **Response Interrupt**

Access:	R/WC

Value	Name	Description
0b	Disable **[Default]**	See Programming Notes
1b	Enable	See Programming Notes

Programming Notes
Hardware sets this bit to a 1 when an interrupt has been generated after N number of Responses are sent to the RIRB buffer OR when an empty Response slot is encountered on all SDI[x] inputs (whichever occurs first). **Note:** This status bit is set even if an interrupt is not enabled for this event. Software clears this flag by writing a 1 to this bit.

7:3 **Reserved**

Format:	MBZ

2 **Response Overrun Interrupt Control**

Access:	R/W

Value	Name	Description
0b	Disable **[Default]**	See Programming Notes
1b	Enable	See Programming Notes

Programming Notes
If this bit is set (and GIE and CIE are enabled), the hardware will generate an interrupt when the Response Overrun Interrupt Status bit is set.

1 **RIRB DMA Enable**

Access:	R/W Variant

Value	Name	Description
0b	DMA STOP **[Default]**	See Programming Notes

RIRBCTL_STS_SIZE - RIRB Control, Status and Size

1b	DMA RUN	See Programming Notes

Programming Notes

After SW writes a 0 to this bit, the HW may not stop immediately. The hardware will physically update the bit to a 0 when the DMA engine is truly stopped. SW must read a 0 from this bit to verify that the DMA is truly stopped.

0 **Response Interrupt Control**

Access:	R/W

Value	Name	Description
0b	Disable Interrupt **[Default]**	See Programming Notes
1b	Generate Interrupt	See Programming Notes

Programming Notes

When generating an interrupt: 1b, (if GIE and CIE are enabled) after N number of Responses are sent to the RIRB buffer OR when an empty Response slot is encountered on all SDI_x inputs (whichever occurs first). The N counter is reset when the interrupt is generated.

Immediate Command Output Interface

ICOI - Immediate Command Output Interface

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	00060h-00063h

DWord	Bit	Description
0	31:0	**Immediate Command Write** Default Value: 0h **Programming Notes** The command to be sent to the codec via the Immediate Command mechanism is written to this register. The command stored in this register is sent out over the link during the next available frame after a 1 is written to the ICB bit.

Immediate Response Input Interface

IRII - Immediate Response Input Interface

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO Variant
Size (in bits):	32
Address:	00064h-00067h

DWord	Bit	Description
0	31:0	**Immediate Response Read** Default Value: 0h This register contains the response received from a codec resulting from a command sent via the Immediate Command mechanism. If multiple codecs responded in the same frame, there is no guarantee as to which response will be latched. Therefore broadcast-type commands must not be issued via the Immediate Command mechanism.

Immediate Command Status

ICS - Immediate Command Status

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	00068h-0006Bh

DWord	Bit	Description
0	31:2	**Reserved** Format: MBZ
	1	**Immediate Result Valid** Access: R/WC

Value	Name	Description
0b	Response_Read **[Default]**	See ProgrammingNotes
1b	Response_Avilable	See ProgrammingNotes

Programming Notes

This bit is set to a '1' by hardware when a new response is latched into the IRR register. This is a status flag indicating that software may read the response from the Immediate Response register. Software must clear this bit (by writing a one to it) before issuing a new command so that the software may determine when a new response has arrived.

	0	**Immediate Command Busy** Access: R/W Set

Value	Name	Description
0b	Command_Done **[Default]**	See ProgrammingNotes
1b	Command_Avilable	See ProgrammingNotes

Programming Notes

When this bit as read as a 0 it indicates that a new command may be issued using the Immediate Command mechanism. When this bit transitions from a 0 to a 1 (via software writing a 1), the controller issues the command currently stored in the Immediate Command register to the codec over the link. When the corresponding response is latched into the Immediate Response

ICS - Immediate Command Status		
		register, the controller hardware sets the IRV flag and clears the ICB bit back to 0. **Note:** While the CORB/RIRB mechanism is operating an Immediate Command must not be issued, otherwise the responses conflict. This must be enforced by software.

DMA Position Lower Base Address

DPLBASE - DMA Position Lower Base Address

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	00070h-00073h

DWord	Bit	Description
0	31:7	**DMA Position Lower Base Address** Default Value: 0000000h Lower 32 bits of the DMA Position Buffer Base Address. This register field must not be written when any DMA engine is running or the DMA transfer may be corrupted. This same address is used by the Flush Control, and must be programmed with a valid value before the FLCNRTL bit is set.
	6:1	**DPLBASE LOWER BITS** Default Value: 0h DPIB Lower Base Address Unimplemented Bits: Hardwired to 0 to force 128-byte buffer alignment for cache line fetch optimizations. These are RO bits.
	0	**DMA Position Buffer Enable** 0b – Disable **[Default]** – See ProgramminNotes 1b – Enable – See ProgramminNotes **Programming Notes** When this bit is set to a '1', the controller will write the DMA positions of each of the DMA engines to the buffer in main memory periodically (typically once/frame). Software can use this value to know what data in memory is valid data. The controller must guarantee that the values in the DMA Position Buffer that the software can read represent positions in the stream for which valid data exists in the Stream's DMA buffer. This has particular relevance in systems which support isochronous transfer; the stream positions in the software-visible memory buffer must represent stream data which has reached the Global Observation point.

DMA Position Upper Base Address

DPUBASE - DMA Position Upper Base Address		
Register Space:	MMIO: 0/3/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	00074h-00077h	
DWord	**Bit**	**Description**
0	31:0	**DPUBASE** Default Value: 00000000h DMA Position Upper Base Address: Upper 32 bits of address of the DMA Position Buffer Base Address. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.

Output Stream Descriptor Control and Status

SDCTL_STS - Output Stream Descriptor Control and Status

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00040000
Access:	R/W
Size (in bits):	32
Address:	00080h-00083h
Name:	Output Stream Descriptor 1 Control and Status
ShortName:	SDCTL_STS_1
Address:	000A0h-000A3h
Name:	Output Stream Descriptor 2 Control and Status
ShortName:	SDCTL_STS_2
Address:	000C0h-000C3h
Name:	Output Stream Descriptor 3 Control and Status
ShortName:	SDCTL_STS_3

DWord	Bit	Description
0	31:30	**Reserved** Format: MBZ
	29	**FIFO Ready** Access: RO Variant For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link. This bit defaults to 0 on reset because the FIFO is cleared on a reset. Value / Name / Description 0b / Disable **[Default]** / See Description 1b / Enable / See Description
	28	**Descriptor Error** Default Value: 0b Access: RO Hardwired to '0'. No memory errors are tracked.
	27	**FIFO Error** Default Value: 0b

SDCTL_STS - Output Stream Descriptor Control and Status

Access:	R/WC

Programming Notes

Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled.
For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.

26 **Buffer Completion Interrupt Status**

Default Value:	0b
Access:	R/WC

Programming Notes

This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor.
It remains active until software clears it by writing a 1 to this bit position.

25:24 **Reserved**

Format:	MBZ

23:20 **Stream Number**

Access:	R/W

This value reflects the Tag associated with the data being transferred on the link.
When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Value	Name	Description
0000b	Reserved **[Default]**	Indicates Unused
0001b	Stream 1	
0010b-1111b	Stream 2- Stream 15	

19 **Bidirectional Direction Control**

Default Value:	0b
Access:	RO

This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.

18 **Traffic Priority**

Default Value:	1b
Access:	RO

Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.

17:16 **Stripe Control**

SDCTL_STS - Output Stream Descriptor Control and Status

Default Value:	00b
Access:	RO

For output streams it controls the number of SDO signals to stripe data across. Only one SDO is supported in dHDA. Therefore it is hardwired to 0's.

15:5 **Reserved**

Format:	MBZ

4 **Error Interrupt Enable**

Access:	R/W

Implemented as RW but no functionality as memory errors are not tracked.

Value	Name	Description
0h	Disable **[Default]**	See Description
1h	Enable	See Description

3 **FIFO Error Interrupt Enable**

Access:	R/W

This bit controls whether the occurrence of a FIFO error (under-run for output) will cause an interrupt or not.
If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.

Value	Name	Description
0h	Disable **[Default]**	See Description
1h	Enable	See Description

2 **Interrupt On Completion Enable**

Access:	R/W

This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor.
If this bit is not set, bit 2 in the Status register will be set, but the interrupt will not occur.

Value	Name	Description
0h	Disable **[Default]**	See Description
1h	Enable	See Description

1 **Stream Run**

Access:	R/W

When set to 1 the DMA engine associated with this output stream will be enabled to transfer data in the main memory to FIFO. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set.
When cleared to 0 the DMA engine associated with this output stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped.

Value	Name	Description

0h	Disable **[Default]**	See Description
1h	Enable	See Description

Programming Notes

Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.

0 **Stream Reset**

Default Value:	0b
Access:	R/W Variant

Programming Notes

Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit.
Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

Output Stream Descriptor Link Position in Current Buffer

SDLPIB - Output Stream Descriptor Link Position in Current Buffer

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO Variant
Size (in bits):	32
Address:	00084h-00087h
Name:	Output Stream Descriptor 1 Link Position in Current Buffer
ShortName:	SDLPIB_1
Address:	000A4h-000A7h
Name:	Output Stream Descriptor 2 Link Position in Current Buffer
ShortName:	SDLPIB_2
Address:	000C4h-000C7h
Name:	Output Stream Descriptor 3 Link Position in Current Buffer
ShortName:	SDLPIB_3

DWord	Bit	Description
0	31:0	**cLink Position in Buffer** Default Value: 00000000h Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

Output Stream Descriptor Cyclic Buffer Length

SDCBL - Output Stream Descriptor Cyclic Buffer Length

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	00088h-0008Bh
Name:	Output Stream Descriptor 1 Cyclic Buffer Length
ShortName:	SDCBL_1
Address:	000A8h-000ABh
Name:	Output Stream Descriptor 2 Cyclic Buffer Length
ShortName:	SDCBL_2
Address:	000C8h-000CBh
Name:	Output Stream Descriptor 3 Cyclic Buffer Length
ShortName:	SDCBL_3

DWord	Bit	Description
0	31:0	**Cyclic Buffer Length** Default Value: 00000000h): Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. **Programming Notes** Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is '0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

Output Stream Descriptor Last Valid Index

SDLVI - Output Stream Descriptor Last Valid Index

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0008Ch-0008Fh
Name:	Output Stream Descriptor 1 Last Valid Index
ShortName:	SDLVI_1
Address:	000ACh-000AFh
Name:	Output Stream Descriptor 2 Last Valid Index
ShortName:	SDLVI_2
Address:	000CCh-000CFh
Name:	Output Stream Descriptor 3 Last Valid Index
ShortName:	SDLVI_3

DWord	Bit	Description
0	31:8	**Reserved** Format: MBZ
	7:0	**Last Valid Index** Default Value: 00h Access: R/W **Programming Notes** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1; i.e., there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'.

Output Stream Descriptor FIFO Data and Format

SDFIFOD_FMT - Output Stream Descriptor FIFO Data and Format

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x000000C0
Access:	R/W
Size (in bits):	32
Address:	00090h-00093h
Name:	Output Stream Descriptor 1 FIFO Data and Format
ShortName:	SDFIFOD_FMT_1
Address:	000B0h-000B3h
Name:	Output Stream Descriptor 2 FIFO Data and Format
ShortName:	SDFIFOD_FMT_2
Address:	000D0h-000D3h
Name:	Output Stream Descriptor 3 FIFO Data and Format
ShortName:	SDFIFOD_FMT_3

DWord	Bit	Description
0	31	**Reserved** Format: MBZ
	30	**Sample Base Rate** Access: R/W

Value	Name	Description
0h	48 **[Default]**	48 kHz
1h	44.1	44.1 kHz

29:27	**Sample Base Rate Multiple** Access: R/W

Value	Name	Description
000b	**[Default]**	48 kHz/44.1 kHz or less
001b	x2	96 kHz, 88.2 kHz, 32 kHz
010b	x3	144 kHz
011b	x4	192 kHz, 176.4 kHz

SDFIFOD_FMT - Output Stream Descriptor FIFO Data and Format

	100b-111b	Reserved	N/A

26:24 **Sample Base Rate Divisor**

Access:	R/W

Value	Name	Description
000b	Divide by 1 **[Default]**	48 kHz, 44.1 kHz
001b	Divide by 2	24 kHz, 22.05 kHz
010b	Divide by 3	16 kHz, 32 kHz
011b	Divide by 4	11.025 kHz)
100b	Divide by 5	9.6 kHz
101b	Divide by 6	8 kHz
110b	Divide by 7	6.875 kHz
111b	Divide by 8	6 kHz

23 **Reserved**

Format:	MBZ

22:20 **Bits per Sample**

Access:	R/W

Value	Name	Description
000b	8 bits **[Default]**	The data will be packed in memory in 8-bit containers on 16-bit boundaries
0001b	16 bits	The data will be packed in memory in 16-bit containers on 16-bit boundaries
010b	20 bits	The data will be packed in memory in 32-bit containers on 32- bit boundaries
011b	24 bits	The data will be packed in memory in 32-bit containers on 32- bit boundaries
100b	32 bits	The data will be packed in memory in 32-bit containers on 32- bit boundaries
101b-111b	Reserved	N/A

19:16 **Number of Channels**

Access:	R/W

Number of channels in each frame of the stream.

Value	Name	Description
0000b-1111b	1-16	0000b = 1 channel in each frame of the stream. **[Default]** 0001b = 2 channels in each frame of the stream. ...

SDFIFOD_FMT - Output Stream Descriptor FIFO Data and Format

		1111b = 16 channels in each frame of the stream.
15:0	**FIFO Size** Default Value: 00C0h Access: R/W Variant Indicates the maximum number of bytes that could be fetched by the controller at one time. This is the maximum number of bytes that may have been DMA'd into memory but not yet transmitted on the link, and is also the maximum possible value that the PICB count will increase by at one time. It depends on what the Stream parameters are programmed as default.	

Output Stream Descriptor Buffer Descriptor List Pointer Lower

SDBDPL - Output Stream Descriptor Buffer Descriptor List Pointer Lower

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	00098h-0009Bh
Name:	Output Stream Descriptor 1 Buffer Descriptor List Pointer Lower
ShortName:	SDBDPL_1
Address:	000B8h-000BBh
Name:	Output Stream Descriptor 2 Buffer Descriptor List Pointer Lower
ShortName:	SDBDPL_2
Address:	000D8h-000DBh
Name:	Output Stream Descriptor 3 Buffer Descriptor List Pointer Lower
ShortName:	SDBDPL_3

DWord	Bit	Description
0	31:7	**Buffer Descriptor List Lower Base Address** Default Value: 0000000h Access: R/W Variant Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is '0' or DMA transfers may be corrupted.
	6:1	**BDLLBASE LOWER BITS** Default Value: 00h Access: RO Hardwired to 0. Forces alignment on 128B boundaries.
	0	**Reserved**

Output Stream Descriptor Buffer Descriptor List Pointer Upper

SDBDPU - Output Stream Descriptor Buffer Descriptor List Pointer Upper

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0009Ch-0009Fh
Name:	Output Stream Descriptor 1 Buffer Descriptor List Pointer Upper
ShortName:	SDBDPU_1
Address:	000BCh-000BFh
Name:	Output Stream Descriptor 2 Buffer Descriptor List Pointer Upper
ShortName:	SDBDPU_2
Address:	000DCh-000DFh
Name:	Output Stream Descriptor 3 Buffer Descriptor List Pointer Upper
ShortName:	SDBDPU_3

DWord	Bit	Description
0	31:0	**Buffer Descriptor List Upper Base Address** Upper 32-bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is '0' or the DMA transfer may be corrupted.

Output Stream Descriptor Control and Status

SDCTL_STS - Output Stream Descriptor Control and Status

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00040000
Access:	R/W
Size (in bits):	32
Address:	00080h-00083h
Name:	Output Stream Descriptor 1 Control and Status
ShortName:	SDCTL_STS_1
Address:	000A0h-000A3h
Name:	Output Stream Descriptor 2 Control and Status
ShortName:	SDCTL_STS_2
Address:	000C0h-000C3h
Name:	Output Stream Descriptor 3 Control and Status
ShortName:	SDCTL_STS_3

DWord	Bit	Description
0	31:30	**Reserved** Format: MBZ
	29	**FIFO Ready** Access: RO Variant For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link. This bit defaults to 0 on reset because the FIFO is cleared on a reset. 0b – Disable **[Default]** – See Description 1b – Enable – See Description
	28	**Descriptor Error** Default Value: 0b Access: RO Hardwired to '0'. No memory errors are tracked.
	27	**FIFO Error** Default Value: 0b

SDCTL_STS - Output Stream Descriptor Control and Status

Access:	R/WC

Programming Notes

Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled.
For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.

26 **Buffer Completion Interrupt Status**

Default Value:	0b
Access:	R/WC

Programming Notes

This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor.
It remains active until software clears it by writing a 1 to this bit position.

25:24 **Reserved**

Format:	MBZ

23:20 **Stream Number**

Access:	R/W

This value reflects the Tag associated with the data being transferred on the link.
When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Value	Name	Description
0000b	Reserved **[Default]**	Indicates Unused
0001b	Stream 1	
0010b-1111b	Stream 2- Stream 15	

19 **Bidirectional Direction Control**

Default Value:	0b
Access:	RO

This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.

18 **Traffic Priority**

Default Value:	1b
Access:	RO

Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.

17:16 **Stripe Control**

SDCTL_STS - Output Stream Descriptor Control and Status

Default Value:	00b
Access:	RO

For output streams it controls the number of SDO signals to stripe data across. Only one SDO is supported in dHDA. Therefore it is hardwired to 0's.

15:5 **Reserved**

Format:	MBZ

4 **Error Interrupt Enable**

Access:	R/W

Implemented as RW but no functionality as memory errors are not tracked.

Value	Name	Description
0h	Disable **[Default]**	See Description
1h	Enable	See Description

3 **FIFO Error Interrupt Enable**

Access:	R/W

This bit controls whether the occurrence of a FIFO error (under-run for output) will cause an interrupt or not.
If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.

Value	Name	Description
0h	Disable **[Default]**	See Description
1h	Enable	See Description

2 **Interrupt On Completion Enable**

Access:	R/W

This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor.
If this bit is not set, bit 2 in the Status register will be set, but the interrupt will not occur.

Value	Name	Description
0h	Disable **[Default]**	See Description
1h	Enable	See Description

1 **Stream Run**

Access:	R/W

When set to 1 the DMA engine associated with this output stream will be enabled to transfer data in the main memory to FIFO. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set.
When cleared to 0 the DMA engine associated with this output stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped.

Value	Name	Description

SDCTL_STS - Output Stream Descriptor Control and Status

0h	Disable **[Default]**	See Description
1h	Enable	See Description

Programming Notes

Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.

0 **Stream Reset**

Default Value:	0b
Access:	R/W Variant

Programming Notes

Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit.
Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

Output Stream Descriptor Link Position in Current Buffer

SDLPIB - Output Stream Descriptor Link Position in Current Buffer

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO Variant
Size (in bits):	32
Address:	00084h-00087h
Name:	Output Stream Descriptor 1 Link Position in Current Buffer
ShortName:	SDLPIB_1
Address:	000A4h-000A7h
Name:	Output Stream Descriptor 2 Link Position in Current Buffer
ShortName:	SDLPIB_2
Address:	000C4h-000C7h
Name:	Output Stream Descriptor 3 Link Position in Current Buffer
ShortName:	SDLPIB_3

DWord	Bit	Description
0	31:0	**cLink Position in Buffer** Default Value: 00000000h Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

Output Stream Descriptor Cyclic Buffer Length

SDCBL - Output Stream Descriptor Cyclic Buffer Length

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	00088h-0008Bh
Name:	Output Stream Descriptor 1 Cyclic Buffer Length
ShortName:	SDCBL_1
Address:	000A8h-000ABh
Name:	Output Stream Descriptor 2 Cyclic Buffer Length
ShortName:	SDCBL_2
Address:	000C8h-000CBh
Name:	Output Stream Descriptor 3 Cyclic Buffer Length
ShortName:	SDCBL_3

DWord	Bit	Description
0	31:0	**Cyclic Buffer Length** Default Value: 00000000h): Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. **Programming Notes** Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is '0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

Output Stream Descriptor Last Valid Index

SDLVI - Output Stream Descriptor Last Valid Index

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0008Ch-0008Fh
Name:	Output Stream Descriptor 1 Last Valid Index
ShortName:	SDLVI_1
Address:	000ACh-000AFh
Name:	Output Stream Descriptor 2 Last Valid Index
ShortName:	SDLVI_2
Address:	000CCh-000CFh
Name:	Output Stream Descriptor 3 Last Valid Index
ShortName:	SDLVI_3

DWord	Bit	Description
0	31:8	**Reserved** Format: MBZ
	7:0	**Last Valid Index** Default Value: 00h Access: R/W **Programming Notes** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1; i.e., there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'.

Output Stream Descriptor FIFO Data and Format

SDFIFOD_FMT - Output Stream Descriptor FIFO Data and Format

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x000000C0
Access:	R/W
Size (in bits):	32
Address:	00090h-00093h
Name:	Output Stream Descriptor 1 FIFO Data and Format
ShortName:	SDFIFOD_FMT_1
Address:	000B0h-000B3h
Name:	Output Stream Descriptor 2 FIFO Data and Format
ShortName:	SDFIFOD_FMT_2
Address:	000D0h-000D3h
Name:	Output Stream Descriptor 3 FIFO Data and Format
ShortName:	SDFIFOD_FMT_3

DWord	Bit	Description
0	31	**Reserved** Format: MBZ
	30	**Sample Base Rate** Access: R/W

Value	Name	Description
0h	48 **[Default]**	48 kHz
1h	44.1	44.1 kHz

29:27	**Sample Base Rate Multiple** Access: R/W

Value	Name	Description
000b	**[Default]**	48 kHz/44.1 kHz or less
001b	x2	96 kHz, 88.2 kHz, 32 kHz
010b	x3	144 kHz
011b	x4	192 kHz, 176.4 kHz

SDFIFOD_FMT - Output Stream Descriptor FIFO Data and Format

	100b-111b	Reserved	N/A

26:24 **Sample Base Rate Divisor**

Access:	R/W

Value	Name	Description
000b	Divide by 1 **[Default]**	48 kHz, 44.1 kHz
001b	Divide by 2	24 kHz, 22.05 kHz
010b	Divide by 3	16 kHz, 32 kHz
011b	Divide by 4	11.025 kHz)
100b	Divide by 5	9.6 kHz
101b	Divide by 6	8 kHz
110b	Divide by 7	6.875 kHz
111b	Divide by 8	6 kHz

23 **Reserved**

Format:	MBZ

22:20 **Bits per Sample**

Access:	R/W

Value	Name	Description
000b	8 bits **[Default]**	The data will be packed in memory in 8-bit containers on 16-bit boundaries
0001b	16 bits	The data will be packed in memory in 16-bit containers on 16-bit boundaries
010b	20 bits	The data will be packed in memory in 32-bit containers on 32- bit boundaries
011b	24 bits	The data will be packed in memory in 32-bit containers on 32- bit boundaries
100b	32 bits	The data will be packed in memory in 32-bit containers on 32- bit boundaries
101b-111b	Reserved	N/A

19:16 **Number of Channels**

Access:	R/W

Number of channels in each frame of the stream.

Value	Name	Description
0000b-1111b	1-16	0000b = 1 channel in each frame of the stream. **[Default]** 0001b = 2 channels in each frame of the stream. ...

SDFIFOD_FMT - Output Stream Descriptor FIFO Data and Format

				1111b = 16 channels in each frame of the stream.
	15:0	**FIFO Size**		
		Default Value:		00C0h
		Access:		R/W Variant
		Indicates the maximum number of bytes that could be fetched by the controller at one time. This is the maximum number of bytes that may have been DMA'd into memory but not yet transmitted on the link, and is also the maximum possible value that the PICB count will increase by at one time. It depends on what the Stream parameters are programmed as default.		

Output Stream Descriptor Buffer Descriptor List Pointer Lower

SDBDPL - Output Stream Descriptor Buffer Descriptor List Pointer Lower

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	00098h-0009Bh
Name:	Output Stream Descriptor 1 Buffer Descriptor List Pointer Lower
ShortName:	SDBDPL_1
Address:	000B8h-000BBh
Name:	Output Stream Descriptor 2 Buffer Descriptor List Pointer Lower
ShortName:	SDBDPL_2
Address:	000D8h-000DBh
Name:	Output Stream Descriptor 3 Buffer Descriptor List Pointer Lower
ShortName:	SDBDPL_3

DWord	Bit	Description
0	31:7	**Buffer Descriptor List Lower Base Address** Default Value: 0000000h Access: R/W Variant Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is '0' or DMA transfers may be corrupted.
	6:1	**BDLLBASE LOWER BITS** Default Value: 00h Access: RO Hardwired to 0. Forces alignment on 128B boundaries.
	0	**Reserved**

Output Stream Descriptor Buffer Descriptor List Pointer Upper

SDBDPU - Output Stream Descriptor Buffer Descriptor List Pointer Upper

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0009Ch-0009Fh
Name:	Output Stream Descriptor 1 Buffer Descriptor List Pointer Upper
ShortName:	SDBDPU_1
Address:	000BCh-000BFh
Name:	Output Stream Descriptor 2 Buffer Descriptor List Pointer Upper
ShortName:	SDBDPU_2
Address:	000DCh-000DFh
Name:	Output Stream Descriptor 3 Buffer Descriptor List Pointer Upper
ShortName:	SDBDPU_3

DWord	Bit	Description
0	31:0	**Buffer Descriptor List Upper Base Address** Upper 32-bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is '0' or the DMA transfer may be corrupted.

Output Stream Descriptor Control and Status

SDCTL_STS - Output Stream Descriptor Control and Status

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00040000
Access:	R/W
Size (in bits):	32
Address:	00080h-00083h
Name:	Output Stream Descriptor 1 Control and Status
ShortName:	SDCTL_STS_1
Address:	000A0h-000A3h
Name:	Output Stream Descriptor 2 Control and Status
ShortName:	SDCTL_STS_2
Address:	000C0h-000C3h
Name:	Output Stream Descriptor 3 Control and Status
ShortName:	SDCTL_STS_3

DWord	Bit	Description
0	31:30	**Reserved** Format: MBZ
	29	**FIFO Ready** Access: RO Variant For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link. This bit defaults to 0 on reset because the FIFO is cleared on a reset. 0b – Disable **[Default]** – See Description 1b – Enable – See Description
	28	**Descriptor Error** Default Value: 0b Access: RO Hardwired to '0'. No memory errors are tracked.
	27	**FIFO Error** Default Value: 0b

SDCTL_STS - Output Stream Descriptor Control and Status

Access:	R/WC

Programming Notes

Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled.
For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.

26 **Buffer Completion Interrupt Status**

Default Value:	0b
Access:	R/WC

Programming Notes

This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor.
It remains active until software clears it by writing a 1 to this bit position.

25:24 **Reserved**

Format:	MBZ

23:20 **Stream Number**

Access:	R/W

This value reflects the Tag associated with the data being transferred on the link.
When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Value	Name	Description
0000b	Reserved **[Default]**	Indicates Unused
0001b	Stream 1	
0010b-1111b	Stream 2- Stream 15	

19 **Bidirectional Direction Control**

Default Value:	0b
Access:	RO

This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.

18 **Traffic Priority**

Default Value:	1b
Access:	RO

Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.

17:16 **Stripe Control**

SDCTL_STS - Output Stream Descriptor Control and Status

Default Value:	00b
Access:	RO

For output streams it controls the number of SDO signals to stripe data across. Only one SDO is supported in dHDA. Therefore it is hardwired to 0's.

15:5 **Reserved**

Format:	MBZ

4 **Error Interrupt Enable**

Access:	R/W

Implemented as RW but no functionality as memory errors are not tracked.

Value	Name	Description
0h	Disable **[Default]**	See Description
1h	Enable	See Description

3 **FIFO Error Interrupt Enable**

Access:	R/W

This bit controls whether the occurrence of a FIFO error (under-run for output) will cause an interrupt or not.
If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.

Value	Name	Description
0h	Disable **[Default]**	See Description
1h	Enable	See Description

2 **Interrupt On Completion Enable**

Access:	R/W

This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor.
If this bit is not set, bit 2 in the Status register will be set, but the interrupt will not occur.

Value	Name	Description
0h	Disable **[Default]**	See Description
1h	Enable	See Description

1 **Stream Run**

Access:	R/W

When set to 1 the DMA engine associated with this output stream will be enabled to transfer data in the main memory to FIFO. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set.
When cleared to 0 the DMA engine associated with this output stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped.

Value	Name	Description

SDCTL_STS - Output Stream Descriptor Control and Status

0h	Disable **[Default]**	See Description
1h	Enable	See Description

Programming Notes

Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.

0 **Stream Reset**

Default Value:	0b
Access:	R/W Variant

Programming Notes

Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit.
Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

Output Stream Descriptor Link Position in Current Buffer

SDLPIB - Output Stream Descriptor Link Position in Current Buffer

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO Variant
Size (in bits):	32
Address:	00084h-00087h
Name:	Output Stream Descriptor 1 Link Position in Current Buffer
ShortName:	SDLPIB_1
Address:	000A4h-000A7h
Name:	Output Stream Descriptor 2 Link Position in Current Buffer
ShortName:	SDLPIB_2
Address:	000C4h-000C7h
Name:	Output Stream Descriptor 3 Link Position in Current Buffer
ShortName:	SDLPIB_3

DWord	Bit	Description
0	31:0	**cLink Position in Buffer** Default Value: 00000000h Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

Output Stream Descriptor Cyclic Buffer Length

SDCBL - Output Stream Descriptor Cyclic Buffer Length

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	00088h-0008Bh
Name:	Output Stream Descriptor 1 Cyclic Buffer Length
ShortName:	SDCBL_1
Address:	000A8h-000ABh
Name:	Output Stream Descriptor 2 Cyclic Buffer Length
ShortName:	SDCBL_2
Address:	000C8h-000CBh
Name:	Output Stream Descriptor 3 Cyclic Buffer Length
ShortName:	SDCBL_3

DWord	Bit	Description
0	31:0	**Cyclic Buffer Length** Default Value: 00000000h): Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. **Programming Notes** Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is '0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

Output Stream Descriptor Last Valid Index

SDLVI - Output Stream Descriptor Last Valid Index

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0008Ch-0008Fh
Name:	Output Stream Descriptor 1 Last Valid Index
ShortName:	SDLVI_1
Address:	000ACh-000AFh
Name:	Output Stream Descriptor 2 Last Valid Index
ShortName:	SDLVI_2
Address:	000CCh-000CFh
Name:	Output Stream Descriptor 3 Last Valid Index
ShortName:	SDLVI_3

DWord	Bit	Description
0	31:8	**Reserved** Format: MBZ
	7:0	**Last Valid Index** Default Value: 00h Access: R/W **Programming Notes** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1; i.e., there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'.

Output Stream Descriptor FIFO Data and Format

SDFIFOD_FMT - Output Stream Descriptor FIFO Data and Format

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x000000C0
Access:	R/W
Size (in bits):	32
Address:	00090h-00093h
Name:	Output Stream Descriptor 1 FIFO Data and Format
ShortName:	SDFIFOD_FMT_1
Address:	000B0h-000B3h
Name:	Output Stream Descriptor 2 FIFO Data and Format
ShortName:	SDFIFOD_FMT_2
Address:	000D0h-000D3h
Name:	Output Stream Descriptor 3 FIFO Data and Format
ShortName:	SDFIFOD_FMT_3

DWord	Bit	Description
0	31	**Reserved** Format: MBZ
	30	**Sample Base Rate** Access: R/W

Value	Name	Description
0h	48 **[Default]**	48 kHz
1h	44.1	44.1 kHz

DWord	Bit	Description
	29:27	**Sample Base Rate Multiple** Access: R/W

Value	Name	Description
000b	**[Default]**	48 kHz/44.1 kHz or less
001b	x2	96 kHz, 88.2 kHz, 32 kHz
010b	x3	144 kHz
011b	x4	192 kHz, 176.4 kHz

SDFIFOD_FMT - Output Stream Descriptor FIFO Data and Format

	100b-111b	Reserved	N/A

26:24 Sample Base Rate Divisor

Access:	R/W

Value	Name	Description
000b	Divide by 1 **[Default]**	48 kHz, 44.1 kHz
001b	Divide by 2	24 kHz, 22.05 kHz
010b	Divide by 3	16 kHz, 32 kHz
011b	Divide by 4	11.025 kHz)
100b	Divide by 5	9.6 kHz
101b	Divide by 6	8 kHz
110b	Divide by 7	6.875 kHz
111b	Divide by 8	6 kHz

23 Reserved

Format:	MBZ

22:20 Bits per Sample

Access:	R/W

Value	Name	Description
000b	8 bits **[Default]**	The data will be packed in memory in 8-bit containers on 16-bit boundaries
0001b	16 bits	The data will be packed in memory in 16-bit containers on 16-bit boundaries
010b	20 bits	The data will be packed in memory in 32-bit containers on 32- bit boundaries
011b	24 bits	The data will be packed in memory in 32-bit containers on 32- bit boundaries
100b	32 bits	The data will be packed in memory in 32-bit containers on 32- bit boundaries
101b-111b	Reserved	N/A

19:16 Number of Channels

Access:	R/W

Number of channels in each frame of the stream.

Value	Name	Description
0000b-1111b	1-16	0000b = 1 channel in each frame of the stream. **[Default]** 0001b = 2 channels in each frame of the stream. ...

SDFIFOD_FMT - Output Stream Descriptor FIFO Data and Format

				1111b = 16 channels in each frame of the stream.
	15:0	**FIFO Size**		
		Default Value:		00C0h
		Access:		R/W Variant
		Indicates the maximum number of bytes that could be fetched by the controller at one time. This is the maximum number of bytes that may have been DMA'd into memory but not yet transmitted on the link, and is also the maximum possible value that the PICB count will increase by at one time. It depends on what the Stream parameters are programmed as default.		

Output Stream Descriptor Buffer Descriptor List Pointer Lower

SDBDPL - Output Stream Descriptor Buffer Descriptor List Pointer Lower

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	00098h-0009Bh
Name:	Output Stream Descriptor 1 Buffer Descriptor List Pointer Lower
ShortName:	SDBDPL_1
Address:	000B8h-000BBh
Name:	Output Stream Descriptor 2 Buffer Descriptor List Pointer Lower
ShortName:	SDBDPL_2
Address:	000D8h-000DBh
Name:	Output Stream Descriptor 3 Buffer Descriptor List Pointer Lower
ShortName:	SDBDPL_3

DWord	Bit	Description
0	31:7	**Buffer Descriptor List Lower Base Address** Default Value: 0000000h Access: R/W Variant Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is '0' or DMA transfers may be corrupted.
	6:1	**BDLLBASE LOWER BITS** Default Value: 00h Access: RO Hardwired to 0. Forces alignment on 128B boundaries.
	0	**Reserved**

Output Stream Descriptor Buffer Descriptor List Pointer Upper

SDBDPU - Output Stream Descriptor Buffer Descriptor List Pointer Upper

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0009Ch-0009Fh
Name:	Output Stream Descriptor 1 Buffer Descriptor List Pointer Upper
ShortName:	SDBDPU_1
Address:	000BCh-000BFh
Name:	Output Stream Descriptor 2 Buffer Descriptor List Pointer Upper
ShortName:	SDBDPU_2
Address:	000DCh-000DFh
Name:	Output Stream Descriptor 3 Buffer Descriptor List Pointer Upper
ShortName:	SDBDPU_3

DWord	Bit	Description
0	31:0	**Buffer Descriptor List Upper Base Address** Upper 32-bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is '0' or the DMA transfer may be corrupted.

Extended Mode 4

EM4 - Extended Mode 4

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000004
Access:	R/W
Size (in bits):	32
Address:	0100Ch-0100Fh

DWord	Bit	Description
0	31:18	**Reserved** Format: MBZ
	17:0	**MVALUE** Default Value: 00004h This is the M Value programming for the DDA. This M value is used to convert the 450MHz to 24MHz. Default value is 4

Extended Mode 5

EM5 - Extended Mode 5		
Register Space:	MMIO: 0/3/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x0000004B	
Access:	R/W	
Size (in bits):	32	
Address:	01010h-01013h	
DWord	**Bit**	**Description**
0	31:18	**Reserved** Format: MBZ
	17:0	**NVALUE** Default Value: 0004Bh This is the N Value programming for the DDA. This N value is used to convert the 450MHz to 24MHz. Default value is 75.

DMA Position in Buffer

DPIB - DMA Position in Buffer

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO Variant
Size (in bits):	32
Address:	01084h-01087h
Name:	Position in Buffer for DMA1
ShortName:	DPIB_1
Address:	010A4h-010A7h
Name:	Position in Buffer for DMA2
ShortName:	DPIB_2
Address:	010C4h-010C7h
Name:	Position in Buffer for DMA3
ShortName:	DPIB_3

DWord	Bit	Description
0	31:0	**DMA Position in Buffer** Default Value: 00h Indicates the number of bytes "processed" by the corresponding DMA engine from the beginning of the BDL.

Wall Clock Counter Alias

WALCLKA - Wall Clock Counter Alias	
Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO Variant
Size (in bits):	32
Address:	02030h-02033h

DWord	Bit	Description
0	31:0	**COUNTERA** This is an alias of the WALCK register. 32 bit counter that is incremented on each link BCLK period and rolls over from FFFF_FFFFh to 0000_0000h. This counter will roll over to zero with a period of approximately 179 seconds. **Programming Notes** This counter is enabled while the BCLK bit is set to 1. Software uses this counter to synchronize between multiple controllers. Will be reset on controller reset.

Output Stream Descriptor Link Position in Current Buffer Alias

SDLPIBA - Output Stream Descriptor Link Position in Current Buffer Alias

Register Space:	MMIO: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	RO Variant
Size (in bits):	32
Address:	02084h-02087h
Name:	Output Stream Descriptor 1 Link Position in Current Buffer Alias
ShortName:	SDLPIBA_1
Address:	020A4h-020A7h
Name:	Output Stream Descriptor 2 Link Position in Current Buffer Alias
ShortName:	SDLPIBA_2
Address:	020C4h-020C7h
Name:	Output Stream Descriptor 3 Link Position in Current Buffer Alias
ShortName:	SDLPIBA_3

DWord	Bit	Description
0	31:0	**Link Position in Buffer Alias** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

Value	Name
0h	Disable **[Default]**
1h	Enable

Vendor Defined ID and Device ID

VID_DID - Vendor Defined ID and Device ID

Register Space:	PCI: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x0C0C8086
Access:	RO
Size (in bits):	32
Address:	00000h-00003h
Power:	Always on
Reset:	global

DWord	Bit	Description
0	31:16	**Device ID** Access: RO Audio device ID Value: 0C0Ch; Name: **[Default]**; Project: HSW
	15:0	**Vendor ID** Default Value: 8086h Access: RO Intel is the Vendor

Command and Status

CMD_STS - Command and Status

Register Space:	PCI: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00100000
Access:	R/W
Size (in bits):	32
Address:	00004h-00007h
Power:	Always on
Reset:	global

DWord	Bit	Description
0	31	**Detected Parity Error** Default Value: 0b Access: RO Not implemented. Hardwired to 0.
	30	**SERR# Status** Default Value: 0b Access: RO Not implemented. Hardwired to 0.
	29	**Received Master Abort** Default Value: 0b Access: RO Not implemented. Hardwired to 0.
	28	**Received Target Abort** Default Value: 0b Access: RO Not implemented. Hardwired to 0.
	27	**Signaled Target-Abort** Default Value: 0b Access: RO Not implemented. Hardwired to 0.

CMD_STS - Command and Status

26:25	**DEVSEL# Timing Status** Default Value: 0b Access: RO Does not apply. Hardwired to 00b.
24	**Master Data Parity Error** Default Value: 0b Access: RO Not implemented. Hardwired to 0.
23	**Fast Back to Back Capable** Default Value: 0b Access: RO Does not apply. Hardwired to 0.
22	**Reserved** Format: MBZ
21	**66 MHz Capable** Default Value: 0b Access: RO Does not apply. Hardwired to 0.
20	**Capabilities List Exists** Default Value: 1b Access: RO Indicates dHDA contains a capabilities list. The first item is pointed to by looking at configuration offset 34h.
19	**Interrupt Status** Access: RO Reflects the state of the INTx# signal at the input of the enable/disable circuit. Note that this bit is not set by an MSI.

Value	Name	Description
0b	Cleared **[Default]**	This bit is a 0 after the interrupt is cleared (independent of the state of the Interrupt Disable bit in the command register).
1b	Asserted	The INTx# is asserted.

18:11	**Reserved**

CMD_STS - Command and Status

	Format:	MBZ

10 Interrupt Disable

Access:	R/W

Enables the device to assert an INTx#. Note that this bit does not affect the generation of MSI's.

Value	Name	Description
0b	Cleared **[Default]**	When cleared, the INTx# signal may be asserted
1b	Deasserted	When set, the Intel HD Audio controller's INTx# signal will be deasserted

9 Fast Back to Back Enable

Default Value:	0b
Access:	RO

Not implemented. Hardwired to 0.

8 SERR Enable

Default Value:	0b
Access:	R/W

Functionality not implemented. This bit is R/W to pass PCIe compliance testing.

7 Wait Cycle Control

Default Value:	0b
Access:	RO

Not implemented. Hardwired to 0.

6 Parity Error Response

Default Value:	0b
Access:	R/W

Functionality not implemented. This bit is R/W to pass PCIe compliance testing.

5 VGA Palette Snoop

Default Value:	0b
Access:	RO

Not implemented. Hardwired to 0.

4 Memory Write and Invalidate Enable

Default Value:	0b
Access:	RO

Not implemented. Hardwired to 0.

CMD_STS - Command and Status

	3	**Special Cycle Enable** Default Value: 0b Access: RO Not implemented. Hardwired to 0.
	2	**Bus Master Enable** Access: R/W Controls standard PCI Express bus mastering capabilities for Memory and IO, reads and writes. Note that this also controls MSI generation since MSI are essentially Memory writes. 0b – Disable **[Default]** 1b – Enable
	1	**Reserved** Default Value: 0b Access: R/W Format: MBZ
	0	**I/O Space** Default Value: 0b Access: RO The Intel HD Audio controller does not implement IO Space, therefore this bit is hardwired to 0.

CLASS

CLASS	
Register Space:	PCI: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x04030000
Access:	RO
Size (in bits):	32
Address:	00008h-0000Bh
Name:	Revision ID, Programming Interface, Sub Class Code and Base Class Code
ShortName:	CLASS
Power:	Always on
Reset:	global

DWord	Bit	Description
0	31:24	**Base Class Code** Default Value: 04h Access: RO This register indicates that the function implements a multimedia device.
	23:16	**Sub Class Code** Default Value: 03h Access: RO This indicates the device is an Intel HD Audio audio device, in the context of a multimedia device.
	15:8	**Programming Interface** Default Value: 00h Access: RO Value assigned to the Intel HD Audio controller.
	7:0	**Revision ID** Default Value: 00h Access: RO Indicates the device specific revision identifier.

CLS

CLS		
Register Space:	PCI: 0/3/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	0000Ch-0000Fh	
Name:	Cache Line Size, Latency Timer, Header Type and Built in Self Test	
ShortName:	CLS	
Power:	Always on	
Reset:	global	

DWord	Bit	Description
0	31:8	**Reserved** Format: MBZ
	7:0	**Cache Line Size** Default Value: 00h Access: R/W Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the Display HD Audio. The cacheline size is always 64B.

Display HD Audio Lower Base Address

DHDALBAR - Display HD Audio Lower Base Address

Register Space:	PCI: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000004
Access:	R/W
Size (in bits):	32
Address:	00010h-00013h
Power:	Always on
Reset:	global

DWord	Bit	Description
0	31:14	**Lower Base Address** Default Value: 0000h Access: R/W Lower Base Address (MBA): Base address for the Intel HD Audio controller's memory mapped configuration registers. 16 Kbytes are requested by hardwiring bits 13:4 to 0's.
	13:4	**ADM** Default Value: 0000000000b Access: RO Hardwired to 0.
	3	**Prefetchable** Default Value: 0b Access: RO Indicates that this BAR is NOT prefetchable.
	2:1	**Address Range** Default Value: 10b Access: RO Indicates that this BAR can be located anywhere in 64-bit address space.
	0	**Space Type** Default Value: 0b Access: RO Indicates that this BAR is located in memory space.

Display HD Audio Upper Base Address

DHDAUBAR - Display HD Audio Upper Base Address		
Register Space:	PCI: 0/3/0	
Project:	HSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	00014h-00017h	
Power:	Always on	
Reset:	global	

DWord	Bit	Description
0	31:0	**Upper Base Address** Default Value: 00000000h Access: R/W Upper 32 bits of the Base address for the Intel HD Audio controller's memory mapped configuration registers.

Subsystem Vendor ID and SubSystem ID

SVID_SID - Subsystem Vendor ID and SubSystem ID

Register Space:	PCI: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W Once
Size (in bits):	32
Address:	0002Ch-0002Fh
Power:	Always on
Reset:	global

DWord	Bit	Description
0	31:16	**Subsystem ID** Default Value: 0000h Access: R/W Once No functionality.
	15:0	**Subsystem Vendor ID** Default Value: 0000h Access: R/W Once No functionality

Capabilities Pointer

CAPPTR - Capabilities Pointer

Register Space:	PCI: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000050
Access:	RO
Size (in bits):	32
Address:	00034h-00037h
Power:	Always on
Reset:	global

DWord	Bit	Description
0	31:8	**Reserved** Format: MBZ
	7:0	**Capability Pointer** Default Value: 50h Access: RO Indicates that the first capability pointer offset is offset 50h (Power Management Capability).

Interrupt Line and Interrupt Pin

INTLN_INTPN - Interrupt Line and Interrupt Pin

Register Space:	PCI: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000100
Access:	R/W
Size (in bits):	32
Address:	0003Ch-0003Fh
Power:	Always on
Reset:	global

DWord	Bit	Description
0	31:12	**Reserved** Format: MBZ
	11:8	**Interrupt Pin** Default Value: 01h Access: RO Interrupt Pin A
	7:0	**Interrupt Line** Default Value: 00h Access: R/W Indicates to software the interrupt line that the interrupt pin is connected to. This register is not affected by FLR.

Power Management Capability ID and Capabilities

PID_PC - Power Management Capability ID and Capabilities

Register Space:	PCI: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00026001
Access:	RO
Size (in bits):	32
Address:	00050h-00053h
Power:	Always on
Reset:	global

DWord	Bit	Description
0	31:27	**PME Support** Default Value: 0h Access: RO PME# cannot be generated.
	26	**D2 Support** Default Value: 0b Access: RO Currently not supported.
	25	**D1 Support** Default Value: 0b Access: RO Currently not supported.
	24:22	**Aux Current** Default Value: 000b Access: RO Currently not supported.
	21	**Device Specific Initialization** Default Value: 0b Access: RO None requered.

PID_PC - Power Management Capability ID and Capabilities

	20	**Reserved** Format: MBZ
	19	**PME Clock** Default Value: 0b Access: RO Does not apply.
	18:16	**Version** Default Value: 010b Access: RO Indicates Revision 1.1 of the PCI Power Management Spec.
	15:8	**Next Capability** Default Value: 60h Access: RO Points to the next capability structure (MSI).
	7:0	**Cap ID** Default Value: 01h Access: RO Indicates this is a PCI power management capability.

Power Management Control and Status

PCS - Power Management Control and Status

Register Space:	PCI: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	00054h-00057h
Power:	Always on
Reset:	global

DWord	Bit	Description
0	31:24	**Data** Default Value: 00h Access: RO Does not apply.
	23	**Bus Power/Clock Control Enable** Default Value: 0b Access: RO Does not apply.
	22	**B2/B3 Support** Default Value: 0b Access: RO Does not apply.
	21:16	**Reserved** Format: MBZ
	15	**PME Status** Default Value: 0b Access: RO PME# cannot be generated.
	14:9	**Reserved** Format: MBZ

PCS - Power Management Control and Status

	8	**PME Enable** Default Value: 0b Access: RO PME# cannot be generated.
	7:2	**Reserved** Format: MBZ
	1:0	**Power State** Default Value: 0b Access: R/W Sets the current power state of dHDA. If software attempts to write a value other than 00 (D0) or 11 (D3HOT) to this field, data is discarded and no state change occurs. When in D3HOT, dHDA's configuration space is available, but MMIO space is not and interrupts are blocked.

MSI Cap ID and Message Control

MID_MMC - MSI Cap ID and Message Control

Register Space:	PCI: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00007005
Access:	R/W
Size (in bits):	32
Address:	00060h-00063h
Power:	Always on
Reset:	global

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23	**64b Address Capability** Default Value: 0b Access: RO 32 bit message address.
	22:20	**Multiple Message Enable** Default Value: 000b Access: RO Hardwired to 0 (there is only 1 message).
	19:17	**Multiple Message Capable** Default Value: 000b Access: RO Hardwired to 0 (there is only 1 message).
	16	**MSI Enable** Default Value: 0b Access: R/W Variant If set an MSI is generated instead of INTx#. MSI Cap ID and Message Control
	15:8	**Next Capability** Default Value: 70h

MID_MMC - MSI Cap ID and Message Control

		Access: RO Points to the PCI Express capability structure. MSI Cap ID and Message Control
	7:0	**Cap ID** Default Value: 05h Access: RO Indicates that this pointer is a MSI capability.

MSI Message Base Address

MMA - MSI Message Base Address

Register Space:	PCI: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	00064h-00067h
Power:	Always on
Reset:	global

DWord	Bit	Description
0	31:2	**Message Lower Address** Default Value: 00000000h Access: R/W Lower Address used for MSI Message.
	1:0	**Reserved** Format: MBZ

MSI Message Data

MMD - MSI Message Data

Register Space:	PCI: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	00068h-0006Bh
Power:	Always on
Reset:	global

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Message Data** Default Value: 0000h Access: R/W Data used for MSI Message.

PCI Express Cap ID and Control

PXID_PXC - PCI Express Cap ID and Control

Register Space:	PCI: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00910010
Access:	RO
Size (in bits):	32
Address:	00070h-00073h
Power:	Always on
Reset:	global

DWord	Bit	Description
0	31:30	**Reserved** Format: MBZ
	29:25	**Interrupt Message Number** Access: RO Hardwired to 0.
	24	**Slot Implemented** Default Value: 0h Access: RO Hardwired to 0.
	23:20	**Device/Port Type** Default Value: 9h Access: RO Indicates Root Complex Integrated Endpoint.
	19:16	**Capability Version** Default Value: 1h Access: RO Indicates version #1 PCI Express capability.
	15:8	**Next Capability** Default Value: 00h Access: RO

PXID_PXC - PCI Express Cap ID and Control

		Indicates this is the last structure in the list.
	7:0	**Cap ID** Default Value: 10h Access: RO Indicates this is a PCI Express capability structure.

Device Capabilities

DEVCAP - Device Capabilities

Register Space:	PCI: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x10000FC0
Access:	RO
Size (in bits):	32
Address:	00074h-00077h
Power:	Always on
Reset:	global

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28	**Function Level Reset** Default Value: 1b Access: RO dHDA supports FLR capability.
	27:26	**Captured Slot Power Limit Scale** Default Value: 00b Access: RO Hardwired to 0.
	25:18	**Captured Slot Power Limit Value** Default Value: 00h Access: RO Hardwired to 0.
	17:15	**Reserved** Format: MBZ
	14	**Power Indicator Present** Default Value: 0b Access: RO Hardwired to 0.

DEVCAP - Device Capabilities

	13	**Attention Indicator Present** Default Value: 0b Access: RO Hardwired to 0.
	12	**Reserved** Format: MBZ
	11:9	**Endpoint L1 Acceptable Latency** Default Value: 111b Access: RO **Programming Notes** Max value not valid.
	8:6	**Endpoint L0s Acceptable Latency** Default Value: 111b Access: RO **Programming Notes** Max value not valid.
	5	**Extended Tag Field Support** Default Value: 0b Access: RO Indicates 5 bit tag supported.
	4:3	**Phantom Functions Supported** Default Value: 00b Access: RO Phantom functions unsupported.
	2:0	**Max Payload Size Supported** Access: RO **Value** / **Name**: 000b **Programming Notes** 128B maximum payload size capability.

Device Control and Status

DEVC_DEVS - Device Control and Status

Register Space:	PCI: 0/3/0
Project:	HSW
Source:	PRM
Default Value:	0x00000800
Access:	R/W
Size (in bits):	32
Address:	00078h-0007Bh
Power:	Always on
Reset:	global

DWord	Bit	Description
0	31:22	**Reserved** Format: MBZ
	21	**Transactions Pending** Default Value: 0b Access: RO A 1 indicates that the dHDA has issued Non-Posted requests which have not been completed. A 0 indicates that Completions for all Non-Posted Requests have been received.
	20	**AUX Power Detected** Default Value: 0b Access: RO Hardwired to 0 (no AUX power source).
	19	**Unsupported Request Detected** Default Value: 0b Access: RO Not implemented.
	18	**Fatal Error Detected** Default Value: 0b Access: RO Not implemented.
	17	**Non-Fatal Error Detected**

DEVC_DEVS - Device Control and Status

		Default Value: 0b Access: RO Not implemented.
	16	**Correctable Error Detected** Default Value: 0b Access: RO Not implemented.
	15	**Initiate FLR** Default Value: 0b Access: R/W When set, initiates function level reset. Value stays as '1' until FLR complete, at which point the value transitions back to '0'. Writes of '0' have no effect.
	14:12	**Max Read Request Size** Default Value: 000b Access: RO Hardwired to 000 enabling 128 B maximum read request size.
	11	**No Snoop Enable** Default Value: 1b Access: R/W When set, dHDA may use non-snooped transactions where appropriate. Not affected by FLR.
	10	**Auxiliary Power PM Enable** Default Value: 0b Access: RO dHDA does not draw AUX power.
	9	**Phantom Functions Enable** Default Value: 0b Access: RO Hardwired to 0.
	8	**Extended Tag Field Enable** Default Value: 0b Access: RO

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		Hardwired to 0.
	7:5	**Max Payload Size** Default Value: 00b Access: RO Hardwired to 000 indicating 128B.
	4	**Enable Relaxed Ordering** Default Value: 0b Access: RO Hardwired to 0.
	3	**Unsupported Request Reporting Enable** Default Value: 0b Access: R/W Not implemented. This bit is RW for PCIe compliance.
	2	**Fatal Error Reporting Enable** Default Value: 0b Access: R/W Not implemented. This bit is RW for PCIe compliance.
	1	**Non-Fatal Error Reporting Enable** Default Value: 0b Access: R/W Not implemented. This bit is RW for PCIe compliance.
	0	**Correctable Error Reporting Enable** Default Value: 0b Access: R/W Not implemented. This bit is RW for PCIe compliance.