Intel Open Source Graphics Programmer's Reference Manual (PRM) for the 2013 Intel® Core™ Processor Family, including Intel HD Graphics, Intel Iris™ Graphics and Intel Iris Pro Graphics

Volume 2a: Command Reference: Enumerations (Haswell)

12/18/2013

Copyright

Command Reference: Enumerations

Table of Contents

3D_Color_Buffer_Blend_Factor

3D_Color_Buffer_Blend_Factor

Source: PRM

Size (in bits): 5

Value	Name
00h	Reserved
01h	BLENDFACTOR_ONE
02h	BLENDFACTOR_SRC_COLOR
03h	BLENDFACTOR_SRC_ALPHA
04h	BLENDFACTOR_DST_ALPHA
05h	BLENDFACTOR_DST_COLOR
06h	BLENDFACTOR_SRC_ALPHA_SATURATE
07h	BLENDFACTOR_CONST_COLOR
08h	BLENDFACTOR_CONST_ALPHA
09h	BLENDFACTOR_SRC1_COLOR
0Ah	BLENDFACTOR_SRC1_ALPHA
0Bh-10h	Reserved
11h	BLENDFACTOR_ZERO
12h	BLENDFACTOR_INV_SRC_COLOR
13h	BLENDFACTOR_INV_SRC_ALPHA
14h	BLENDFACTOR_INV_DST_ALPHA
15h	BLENDFACTOR_INV_DST_COLOR
16h	Reserved
17h	BLENDFACTOR_INV_CONST_COLOR
18h	BLENDFACTOR_INV_CONST_ALPHA
19h	BLENDFACTOR_INV_SRC1_COLOR
1Ah	BLENDFACTOR_INV_SRC1_ALPHA

3D_Color_Buffer_Blend_Function

3D_Color_Buffer_Blend_Function	
Source:	PRM
Size (in bits):	3

Value	Name	Description
0	BLENDFUNCTION_ADD	BLENDFUNCTION_ADD
1	BLENDFUNCTION_SUBTRACT	BLENDFUNCTION_SUBTRACT
2	BLENDFUNCTION_REVERSE_SUBTRACT	BLENDFUNCTION_REVERSE_SUBTRACT
3	BLENDFUNCTION_MIN	BLENDFUNCTION_MIN
4	BLENDFUNCTION_MAX	BLENDFUNCTION_MAX
5 - 7	Reserved	

3D_Compare_Function

3D_Compare_Function		
Source:	PRM	
Size (in bits):	3	
Value	**Name**	**Description**
0h	COMPAREFUNCTION_ALWAYS	Always pass
1h	COMPAREFUNCTION_NEVER	Never pass
2h	COMPAREFUNCTION_LESS	Pass if the value is less than the reference
3h	COMPAREFUNCTION_EQUAL	Pass if the value is equal to the reference
4h	COMPAREFUNCTION_LEQUAL	Pass if the value is less than or equal to the reference
5h	COMPAREFUNCTION_GREATER	Pass if the value is greater than the reference
6h	COMPAREFUNCTION_NOTEQUAL	Pass if the value is not equal to the reference
7h	COMPAREFUNCTION_GEQUAL	Pass if the value is greater than or equal to the reference

3D_Logic_Op_Function

3D_Logic_Op_Function

Source: PRM

Size (in bits): 4

Value	Name	Description
0h	LOGICOP_CLEAR	BLACK; all 0's
1h	LOGICOP_NOR	NOTMERGEPEN; NOT (S OR D)
2h	LOGICOP_AND_INVERTED	MASKNOTPEN; (NOT S) AND D
3h	LOGICOP_COPY_INVERTED	NOTCOPYPEN; NOT S
4h	LOGICOP_AND_REVERSE	MASKPENNOT; S AND NOT D
5h	LOGICOP_INVERT	NOT; NOT D
6h	LOGICOP_XOR	XORPEN; S XOR D
7h	LOGICOP_NAND	NOTMASKPEN; NOT (S AND D)
8h	LOGICOP_AND	MASKPEN; S AND D
9h	LOGICOP_EQUIV	NOTXORPEN; NOT (S XOR D)
Ah	LOGICOP_NOOP	NOP; D
Bh	LOGICOP_OR_INVERTED	MERGENOTPEN; (NOT S) OR D
Ch	LOGICOP_COPY	COPYPEN; S
Dh	LOGICOP_OR_REVERSE	MERGEPENNOT; S OR NOT D
Eh	LOGICOP_OR	MERGEPEN; S OR D
Fh	LOGICOP_SET	WHITE; all 1's

3D_Prim_Topo_Type

3D_Prim_Topo_Type

Project: HSW

Source: RenderCS

Size (in bits): 6

The following table defines the encoding of the Primitive Topology Type field. See 3D Pipeline for details, programming restrictions, diagrams and a discussion of the basic primitive types.

Value	Name	Description	Programming Notes	Project
00h	Reserved			All
01h	3DPRIM_POINTLIST			All
02h	3DPRIM_LINELIST			All
03h	3DPRIM_LINESTRIP			All
04h	3DPRIM_TRILIST			All
05h	3DPRIM_TRISTRIP			All
06h	3DPRIM_TRIFAN			All
07h	3DPRIM_QUADLIST	The QUADLIST topology is converted to POLYGON topology at the beginning of the 3D pipeline.		All
08h	3DPRIM_QUADSTRIP	The QUADSTRIP topology is converted to POLYGON topology at the beginning of the 3D pipeline.		All
09h	3DPRIM_LINELIST_ADJ			All
0Ah	3DPRIM_LISTSTRIP_ADJ			All
0Bh	3DPRIM_TRILIST_ADJ			All
0Ch	3DPRIM_TRISTRIP_ADJ			All
0Dh	3DPRIM_TRISTRIP_REVERSE			All
0Eh	3DPRIM_POLYGON			All
0Fh	3DPRIM_RECTLIST			All
10h	3DPRIM_LINELOOP	The LINELOOP topology is converted to LINESTRIP topology at the beginning of the 3D pipeline.		All
11h	3DPRIM_POINTLIST _BF			All
12h	3DPRIM_LINESTRIP_CONT			All
13h	3DPRIM_LINESTRIP_BF			All
14h	3DPRIM_LINESTRIP_CONT_BF			All

3D_Prim_Topo_Type

15h	Reserved			All
16h	3DPRIM_TRIFAN_NOSTIPPLE			All
17h-1Fh	Reserved			All
20h	3DPRIM_PATCHLIST_1	List of 1-vertex patches		HSW
21h	3DPRIM_PATCHLIST_2			HSW
22h	3DPRIM_PATCHLIST_3			HSW
23h	3DPRIM_PATCHLIST_4			HSW
24h	3DPRIM_PATCHLIST_5			HSW
25h	3DPRIM_PATCHLIST_6			HSW
26h	3DPRIM_PATCHLIST_7			HSW
27h	3DPRIM_PATCHLIST_8			HSW
28h	3DPRIM_PATCHLIST_9			HSW
29h	3DPRIM_PATCHLIST_10			HSW
2ah	3DPRIM_PATCHLIST_11			HSW
2bh	3DPRIM_PATCHLIST_12			HSW
2ch	3DPRIM_PATCHLIST_13			HSW
2dh	3DPRIM_PATCHLIST_14			HSW
2eh	3DPRIM_PATCHLIST_15			HSW
2fh	3DPRIM_PATCHLIST_16			HSW
30h	3DPRIM_PATCHLIST_17			HSW
31h	3DPRIM_PATCHLIST_18			HSW
32h	3DPRIM_PATCHLIST_19			HSW
33h	3DPRIM_PATCHLIST_20			HSW
34h	3DPRIM_PATCHLIST_21			HSW
35h	3DPRIM_PATCHLIST_22			HSW
36h	3DPRIM_PATCHLIST_23			HSW
37h	3DPRIM_PATCHLIST_24			HSW
38h	3DPRIM_PATCHLIST_25			HSW
39h	3DPRIM_PATCHLIST_26			HSW
3ah	3DPRIM_PATCHLIST_27			HSW
3bh	3DPRIM_PATCHLIST_28			HSW
3ch	3DPRIM_PATCHLIST_29			HSW
3dh	3DPRIM_PATCHLIST_30			HSW
3eh	3DPRIM_PATCHLIST_31			HSW
3Fh	3DPRIM_PATCHLIST_32	List of 32-vertex patches		HSW

3D_Vertex_Component_Control

3D_Vertex_Component_Control

Project: HSW

Source: RenderCS

Size (in bits): 3

Value	Name	Description	Project
0	VFCOMP_NOSTORE	Don't store this component. (Not valid for Component 0, but can be used for Component 1-3). Once this setting is used for a component, all higher-numbered components (if any) MUST also use this setting. (I.e., no holes within any particular vertex element). Also, there are no 'holes' allowed in the destination vertex: NOSTORE components must be overwritten by subsequent components unless they are the trailing DWords of the vertex. Software must explicitly chose some value (probably 0) to be written into DWords that would otherwise be 'holes'.	HSW
1	VFCOMP_STORE_SRC	Store corresponding component from format-converted source element. Storing a component that is not included in the Source Element Format results in an UNPREDICTABLE value being stored. Software should used the STORE_0 or STORE_1 encoding to supply default components.Within a VERTEX_ELEMENT_STATE structure, if a Component Control field is set to something other than VFCOMP_STORE_SRC, no higher-numbered Component Control fields may be set to VFCOMP_STORE_SRC. In other words, only trailing components can be set to something other than VFCOMP_STORE_SRC.	All
2	VFCOMP_STORE_0	Store 0 (interpreted as 0.0f if accessed as a float value)	All
3	VFCOMP_STORE_1_FP	Store 1.0f	All
4	VFCOMP_STORE_1_INT	Store 0x1	All
5	VFCOMP_STORE_VID	Store Vertex ID (as U32)	HSW
6	VFCOMP_STORE_IID	Store Instance ID (as U32)	HSW
7	VFCOMP_STORE_PID	Store Primitive ID (as U32) [DevHSW+] Software can no longer use this encoding as PrimitiveID is passed down the FF pipeline - see explanation above.	All

AddrMode

AddrMode

Project:	HSW
Source:	EuIsa
Size (in bits):	1

Addressing Mode
This field determines the addressing method of the operand. Normally the destination operand and each source operand each have a distinct addressing mode field.
When it is cleared, the register address of the operand is directly provided by bits in the instruction word. It is called a direct register addressing mode. When it is set, the register address of the operand is computed based on the address register value and an address immediate field in the instruction word. This is referred to as a register-indirect register addressing mode.
This field applies to the destination operand and the first source operand, src0. Support for src1 is device dependent. See Table XX (Indirect source addressing support available in device hardware) in ISA Execution Environment for details.

Programming Notes
Instructions with 3 source operands use Direct Addressing.

Value	Name	Description
0	Direct	'Direct' register addressing
1	Indirect	'Register-Indirect' (or in short 'Indirect'). Register-indirect register addressing

ChanEn

ChanEn

Project: HSW

Source: EuIsa

Size (in bits): 1

Description	Project
Channel Enables Four channel enables are defined for controlling which channels will be written into the destination region. These channel mask bits are applied in a modulo-four manner to all ExecSize channels. There is 1-bit Channel Enable for each channel within the group of 4. If the bit is cleared, the write for the corresponding channel is disabled. If the bit is set, the write is enabled. Mnemonic for the bit being set for the group of 4 is *x*, *y*, *z*, and *w*, respectively, where *x* corresponds to Channel 0 in the group and *w* corresponds to channel 3 in the group. This field only applies to destination operand. This field is only present in Align16 mode.	HSW

Value	Name
0	Write Disabled
1	Write Enabled **[Default]**

ChanSel

ChanSel

Project:	HSW
Source:	EuIsa
Size (in bits):	2

Channel Select
This field controls the channel swizzle for a source operand. The normally sequential channel assignment can be altered by explicitly identifying neighboring data elements for each channel. Out of the 8-bit field, 2 bits are assigned for each channel within the group of 4. ChanSel[1:0], [3.2], [5.4] and [7,6] are for channel 0 (*x*), 1 (*y*), 2 (*z*), and 3 (*w*) in the group, respectively.
For example with an execution size of 8, r0.0<4>.zywz:f would assign the channels as follows: Chan0 = Data2, Chan1 = Data1, Chan2 = Data3, Chan3 = Data2; Chan4 = Data6, Chan5 = Data5, Chan6 = Data7, Chan7 = Data6.
This field only applies to source operand.
This field is only present in Align16 mode. It is not present for an immediate source operand.
The 2-bit Channel Selection field for each channel within the group of 4 is defined as the following.

Value	Name	Description
00b	x	Channel 0 is selected for the corresponding execution channel
01b	y	Channel 1 is selected for the corresponding execution channel
10b	z	Channel 2 is selected for the corresponding execution channel
11b	w	Channel 3 is selected for the corresponding execution channel

CondModifier

CondModifier

Project: HSW

Source: EuIsa

Size (in bits): 4

Conditional Modifier
This field sets the flag register based on the internal conditional signals output from the execution pipe such as sign, zero, overflow and NaNs, etc. If this field is set to 0000, no flag registers are updated. Flag registers are not updated for instructions with embedded compares.
This field may also be referred to as the flag destination control field.
This field applies to all instructions except send, sendc, and math.

Value	Name	Description
0000b	None **[Default]**	Do Not modify Flag Register
0001b	.z	Zero
0001b	.e	Equal
0010b	.nz	NotZero
0010b	.ne	NotEqual
0011b	.g	Greater-than
0100b	.ge	Greater-than-or-equal
0101b	.l	Less-than
0110b	.le	Less-than-or-equal
0111b	Reserved	
1000b	.o	Overflow
1001b	.u	Unordered with Computed NaN
1110b-1111b	Reserved	

DataType

DataType

Project: HSW

Source: EuIsa

Size (in bits): 3

Operand Data Type

Value	Name	Description	Project
000b	UD **[Default]**	Unsigned Doubleword integer	
001b	D	signed Doubleword integer	
010b	UW	Unsigned Word integer	
011b	W	signed Word integer	
100b	UB	Unsigned Byte integer	
101b	B	signed Byte integer	
110b	DF	Double precision (64-bit) Float	HSW
111b	F	single precision Float	

DepCtrl

DepCtrl

Project: HSW

Source: EuIsa

Size (in bits): 2

Destination Dependency Control
This field selectively disables destination dependency check and clear for this instruction.
When it is set to 00, normal destination dependency control is performed for the instruction hardware checks for destination hazards to ensure data integrity. Specifically, destination register dependency check is conducted before the instruction is made ready for execution. After the instruction is executed, the destination register scoreboard will be cleared when the destination operands retire.
When bit 10 is set (NoDDClr), the destination register scoreboard will NOT be cleared when the destination operands retire. When bit 11 is set (NoDDChk), hardware does not check for destination register dependency before the instruction is made ready for execution. NoDDClr and NoDDChk are not mutual exclusive.
When this field is not all-zero, hardware does not protect against destination hazards for the instruction. This is typically used to assemble data in a fine grained fashion (e.g. matrix-vector compute with dot-product instructions), where the data integrity is guaranteed by software based on the intended usage of instruction sequences.

Value	Name	Description
00b	None **[Default]**	Destination dependency checked and cleared (normal)
01b	NoDDClr	Destination dependency checked but not cleared
10b	NoDDChk	Destination dependency not checked but cleared
11b	NoDDClr, NoDDChk	Destination dependency not checked and not cleared

EU_OPCODE

EU_OPCODE

Project: HSW
Source: EuIsa
Size (in bits): 7

Value	Name	Project
40h	add	
4Eh	addc	HSW
5h	and	
0Ch	asr	
42h	avg	
18h	bfe	HSW
19h	bfi1	HSW
1Ah	bfi2	HSW
17h	bfrev	HSW
23h	brc	HSW
21h	brd	HSW
28h	break	
2Ch	call	
2Bh	calla	HSW+
4Dh	cbit	HSW
10h	cmp	
11h	cmpn	
29h	cont	
0Ah	dim	HSW
57h	dp2	
56h	dp3	
54h	dp4	
55h	dph	
24h	else	
25h	endif	
14h	f16to32	HSW
13h	f32to16	HSW
4Bh	fbh	HSW

EU_OPCODE		
4Ch	fbl	HSW
43h	frc	
2Ah	halt	
22h	if	HSW
0h	illegal	
20h	jmpi	
59h	line	
5Ch	lrp	
4Ah	lzd	
48h	mac	
49h	mach	
5Bh	mad	
38h	math	
1h	mov	
3h	movi	
41h	mul	
7Eh	nop	
4h	not	
6h	or	
5Ah	pln	
2Dh	ret	
45h	rndd	
46h	rnde	
44h	rndu	
47h	rndz	
50h	sad2	
51h	sada2	
2h	sel	
31h	send	
32h	sendc	
33h	sends	
34h	sendsc	
9h	shl	
8h	shr	
4Fh	subb	HSW

EU_OPCODE		
30h	wait	
27h	while	HSW
7h	xor	

ExecSize

ExecSize

Project: HSW

Source: EuIsa

Size (in bits): 3

Execution Size
This field determines the number of channels operating in parallel for this instruction.
The size cannot exceed the maximum number of channels allowed for the given data type.

Restriction
Restriction : An operand's Width must be less-than-or-equal to ExecSize

Value	Name	Programming Notes	Project
000b	1 Channel (Scalar operation) **[Default]**		
001b	2 Channels		
010b	4 Channels		
011b	8 Channels		
100b	16 Channels	Restriction : 4-byte or smaller data types. Excludes DF, Q, and UQ types.	
101b	32 Channels	Restriction : 2-byte or 1-byte data types. Excludes D, DF, F, Q, UD, and UQ types.	HSW
110b-111b	Reserved		

FC

FC			
Project:	HSW		
Source:	EuIsa		
Size (in bits):	4		
Math Function Control			
Value	**Name**	**Description**	**Project**
0000b	Reserved		
0001b	INV (reciprocal)		
0010b	LOG		
0011b	EXP		
0100b	SQRT		
0101b	RSQ		
0110b	SIN		
0111b	COS		
1000b	Reserved		
1001b	FDIV		
1010b	POW		
1011b	INT DIV BOTH	Return Quotient and Remainder	
1100b	INT DIV QUOTIENT	Return Quotient Only	
1101b	INT DIV REMAINDER	Return Remainder	
1110b-1111b	Reserved		HSW

HorzStride

HorzStride

Project:	HSW
Source:	EuIsa
Size (in bits):	2

Horizontal Stride
This field provides the distance in unit of data elements between two adjacent data elements within a row (horizontal) in the register region for the operand.
This field applies to both destination and source operands.
This field is not present for an immediate source operand.

Value	Name
00b	0 elements
01b	1 elements
10b	2 elements
11b	4 elements

Performance Counter Report Formats

Performance Counter Report Formats

Project: **HSW**

Source: PRM

Size (in bits): 3

Value	Description	Project
001b	**HSW** Write 128 Bytes containing: RPT_ID, TIME_STAMP, the A-Cntr 0-12 counters, and the A-Cntr 13-28 counters. A-Cntr 4 | A-Cntr 3 | A-Cntr 2 | A-Cntr 1 | A-Cntr 0 | TIME_STAMP | RPT_ID A-Cntr 12 | A-Cntr 11 | A-Cntr 10 | A-Cntr 9 | A-Cntr 8 | A-Cntr 7 | A-Cntr 6 | A-Cntr 5 A-Cntr 20 | A-Cntr 19 | A-Cntr 18 | A-Cntr 17 | A-Cntr 16 | A-Cntr 15 | A-Cntr 14 | A-Cntr 13 A-Cntr 28 | A-Cntr 27 | A-Cntr 26 | A-Cntr 25 | A-Cntr 24 | A-Cntr 23 | A-Cntr 22 | A-Cntr 21	HSW
010b	**HSW** Write 128 Bytes containing: RPT_ID, TIME_STAMP, and the A-Cntr 0-12 counters B-Cntr 0-7 counters. C-Cntr 0-8 counters. A-Cntr 4 | A-Cntr 3 | A-Cntr 2 | A-Cntr 1 | A-Cntr 0 | TIME_STAMP | RPT_ID A-Cntr 12 | A-Cntr 11 | A-Cntr 10 | A-Cntr 9 | A-Cntr 8 | A-Cntr 7 | A-Cntr 6 | A-Cntr 5 B-Cntr 7 | B-Cntr 6 | B-Cntr 5 | B-Cntr 4 | B-Cntr 3 | B-Cntr 2 | B-Cntr 1 | B-cntr 0 C-Cntr 7 | C-Cntr 6 | C-Cntr 5 | C-Cntr 4 | C-Cntr 3 | C-Cntr 2 | C-Cntr 1 | C-Cntr 0	
011b	**HSW** Write 192 Bytes containing: RPT_ID, TIME_STAMP, the A-Cntr 0-28 counters, B-Cntr 0-8 counters, and the C-Cntr 0-8 counters A-Cntr 4 | A-Cntr 3 | A-Cntr 2 | A-Cntr 1 | A-Cntr 0 | TIME_STAMP | RPT_ID A-Cntr 12 | A-Cntr 11 | A-Cntr 10 | A-Cntr 9 | A-Cntr 8 | A-Cntr 7 | A-Cntr 6 | A-Cntr 5 A-Cntr 20 | A-Cntr 19 | A-Cntr 18 | A-Cntr 17 | A-Cntr 16 | A-Cntr 15 | A-Cntr 14 | A-Cntr 13 A-Cntr 28 | A-Cntr 27 | A-Cntr 26 | A-Cntr 25 | A-Cntr 24 | A-Cntr 23 | A-Cntr 22 | A-Cntr 21 B-Cntr 7 | B-Cntr 6 | B-Cntr 5 | B-Cntr 4 | B-Cntr 3 | B-Cntr 2 | B-Cntr 1 | B-Cntr 0	

	C-Cntr 7	C-Cntr 6	C-Cntr 5	C-Cntr 4	C-Cntr 3	C-Cntr 2	C-Cntr 1	C-Cntr 0

100b **HSW**

Write 64 Bytes containing: RPT_ID, TIME_STAMP, the B-Cntr 0-3 counters, and the C-Cntr 0-7 counters.

B-Cntr 3	B-Cntr 2	B-Cntr 1	B-Cntr 0	Reserved	TIME_STAMP		RPT_ID
C-Cntr 7	C-Cntr 6	C-Cntr 5	C-Cntr 4	C-Cntr 3	C-Cntr 2	C-Cntr 1	C-Cntr 0

101b **HSW**

Write 256 bytes containing: RPT_ID, TIME_STAMP, the A-Cntr 0-44 counters, the B-Cntr 0-7 counters, and the C-Cntr 0-7 counters

A-Cntr 4	A-Cntr 3	A-Cntr 2	A-Cntr 1	A-Cntr 0	TIME_STAMP		RPT_ID
A-Cntr 12	A-Cntr 11	A-Cntr 10	A-Cntr 9	A-Cntr 8	A-Cntr 7	A-Cntr 6	A-Cntr 5
A-Cntr 20	A-Cntr 19	A-Cntr 18	A-Cntr 17	A-Cntr 16	A-Cntr 15	A-Cntr 14	A-Cntr 13
A-Cntr 28	A-Cntr 27	A-Cntr 26	A-Cntr 25	A-Cntr 24	A-Cntr 23	A-Cntr 22	A-Cntr 21
A-Cntr 36	A-Cntr 35	A-Cntr 34	A-Cntr 33	A-Cntr 32	A-Cntr 31	A-Cntr 30	A-Cntr 29
A-Cntr 44	A-Cntr 43	A-Cntr 42	A-Cntr 41	A-Cntr 40	A-Cntr 39	A-Cntr 38	A-Cntr 37
B-Cntr 7	B-Cntr 6	B-Cntr 5	B-Cntr 4	B-Cntr 3	B-Cntr 2	B-Cntr 1	B-Cntr 0
C-Cntr 7	C-Cntr 6	C-Cntr 5	C-Cntr 4	C-Cntr 3	C-Cntr 2	C-Cntr 1	C-Cntr 0

110b **HSW**

Write 64 bytes containing RPT_ID, TIME_STAMP, the B-Cntr 0-3 counters, and the C-Cntr 0-7 counters, and the A-Cntr 29-44

B-Cntr 3	B-Cntr 2	B-Cntr 1	B-Cntr 0	Reserved	TIME_STAMP		RPT_ID
C-Cntr 7	C-Cntr 6	C-Cntr 5	C-Cntr 4	C-Cntr 3	C-Cntr 2	C-Cntr 1	C-Cntr 0
A-Cntr 36	A-Cntr 35	A-Cntr 34	A-Cntr 33	A-Cntr 32	A-Cntr 31	A-Cntr 30	A-Cntr 29
A-Cntr 44	A-Cntr 43	A-Cntr 42	A-Cntr 41	A-Cntr 40	A-Cntr 39	A-Cntr 38	A-Cntr 37

111b **HSW**

Write 64 Bytes containing: RPT_ID, TIME_STAMP, the C-Cntr 0-3 counters, and the B-Cntr 0-7 counters.

Performance Counter Report Formats

	C-Cntr 3	C-Cntr 2	C-Cntr 1	C-Cntr 0	Reserved	TIME_STAMP		RPT_ID
	B-Cntr 7	B-Cntr 6	B-Cntr 5	B-Cntr 4	B-Cntr 3	B-Cntr 2	B-Cntr 1	B-Cntr 0

PredCtrl

PredCtrl

Project: HSW

Source: EuIsa

Size (in bits): 4

Value	Name	Project	Exists If
0000b	No Predication (normal) **[Default]**		
0001b	Sequential Flag Channel Mapping		
0010b	Replication swizzle .x		(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align16')
0010b	.anyv (any from f0.0-f0.1 on the same channel)		(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align1')
0011b	Replication swizzle .y		(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align16')
0011b	.allv (all of f0.0-f0.1 on the same channel)		(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align1')
0100b	Replication swizzle .z		(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align16')
0100b	.any2h (any in group of 2 channels)		(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align1')
0101b	Replication swizzle .w		(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align16')
0101b	.all2h (all in group of 2 channels)		(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align1')
0110b	.any4h		
0111b	.all4h		
1000b-1111b	Reserved		(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align16')
1000b	.any8h (any in group of 8 channels)		(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align1')
1001b	.all8h (all in group of 8 channels)		(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align1')
1010b	.any16h (any in group of 16 channels)		(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align1')
1011b	.all16h (all in group of 16 channels)		(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align1')
1100b	.any32h (any in group of 32 channels)	HSW	(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align1')

PredCtrl			
1101b	.all32h (all in group of 32 channels)	HSW	(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align1')
1110b-1111b	Reserved	HSW	(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align1')

QtrCtrl

QtrCtrl

Project: HSW

Source: EuIsa

Size (in bits): 2

Quarter Control
This field provides explicit control for ARF selection.
This field combined with ExecSize determines which channels are used for the ARF registers.
Along with NibCtrl, 1/8 DMask/VMask and ARF can be selected.

Programming Notes	Project
NibCtrl is only allowed for SIMD4 instructions with a DF (Double Float) source or destination type.	HSW

Value	Name	Description	Programming Notes	Project	Exists If
00b	1Q **[Default]**	Use first quarter for DMask/VMask. Use first half for everything else.			([ExecSize]=='8') AND ([NibCtrl]=='0')
01b	2Q	Use second quarter for DMask/VMask. Use second half for everything else.			([ExecSize]=='8') AND ([NibCtrl]=='0')
10b	3Q	Use third quarter for DMask/VMask. Use first half for everything else.			([ExecSize]=='8') AND ([NibCtrl]=='0')
11b	4Q	Use fourth quarter for DMask/VMask. Use second half for everything else.			([ExecSize]=='8') AND ([NibCtrl]=='0')
0	1H	Use first half for DMask/VMask. Use all channels for everything else.			([ExecSize]=='16') AND ([NibCtrl]=='0')
2	2H	Use second half for DMask/VMask. Use all channels for everything else.	Only allowed for SIMD16 instruction in Single Program Flow mode (SPF=1)		([ExecSize]=='16') AND ([NibCtrl]=='0')
0	1N	Use first 1/8th for DMask/VMask and ARF.		HSW	([ExecSize]=='4') AND ([NibCtrl]=='0')
0	2N	Use second 1/8th for DMask/VMask and ARF.		HSW	([ExecSize]=='4') AND ([NibCtrl]=='1')
1	3N	Use third 1/8th for DMask/VMask and ARF.		HSW	([ExecSize]=='4') AND ([NibCtrl]=='0')

QtrCtrl					
1	4N	Use fourth 1/8th for DMask/VMask and ARF.		HSW	([ExecSize]=='4') AND ([NibCtrl]=='1')
2	5N	Use fifth 1/8th for DMask/VMask and ARF.		HSW	([ExecSize]=='4') AND ([NibCtrl]=='0')
2	6N	Use sixth 1/8th for DMask/VMask and ARF.		HSW	([ExecSize]=='4') AND ([NibCtrl]=='1')
3	7N	Use seventh 1/8th for DMask/VMask and ARF.		HSW	([ExecSize]=='4') AND ([NibCtrl]=='0')
3	8N	Use eighth 1/8th for DMask/VMask and ARF.		HSW	([ExecSize]=='4') AND ([NibCtrl]=='1')

RegFile

RegFile

Project: HSW

Source: EuIsa

Size (in bits): 2

Value	Name	Description	Programming Notes	Project
00b	ARF	Architecture Register File	Restriction : Only allowed for src0 or destination	
01b	GRF	General Register File - allowed for any source or destination		
10b	Reserved			HSW
11b	IMM	Immediate operand	Restriction : Only allowed for the last source operand. Not allowed for the destination operand or for any other source operand. Note that for flow control instructions requiring two offsets, regfile of source0 is required to be immediate since the 64b for immediates occupy the DW2 and DW3	

RepCtrl

RepCtrl

Project:	HSW
Source:	EuIsa
Size (in bits):	1

Replicate Control
This field is only present in three-source instructions, for each of the three source operands. It controls replication of the starting channel to all channels in the execution size. This is applicable to 32b datatypes. 16b and 64b datatypes cannot use the replicate control.

Value	Name
0	No replication
1	Replicate across all channels

SFID

SFID

Project: HSW

Source: EuIsa

Size (in bits): 4

The following table lists the assignments (encodings) of the Shared Function and Fixed Function IDs used within the GPE. A Shared Function is a valid target of a message initiated via a 'send' instruction. A Fixed Function is an identifiable unit of the 3D or Media pipeline. Note that the Thread Spawner is both a Shared Function and Fixed Function.

Note: The initial intention was to combine these two ID namespaces, so that (theoretically) an agent (such as the Thread Spawner) that served both as a Shared Function and Fixed Function would have a single, unique 4-bit ID encoding. However, this combination is not a requirement of the architecture.

Programming Notes	Project
SFID_DP_DC1 is an extension of SFID_DP_DC0 to allow for more message types. They act as a single logical entity.	DevHSW+

Value	Name	Description	Programming Notes	Project
0000b	SFID_NULL	Null		
0001b	Reserved	Reserved		
0010b	SFID_SAMPLER	Sampler		
0011b	SFID_GATEWAY	Message Gateway		
0100b	SFID_DP_SAMPLER	Sampler Cache Data Port		HSW
0101b	SFID_DP_RC	Render Cache Data Port		
0110b	SFID_URB	URB		
0111b	SFID_SPAWNER	Thread Spawner		
1000b	SFID_VME	Video Motion Estimation		
1001b	SFID_DP_CC	Constant Cache Data Port		HSW
1010b	SFID_DP_DC0	Data Cache Data Port		HSW
1011b	SFID_PI	Pixel Interpolator		HSW
1100b	SFID_DP_DC1	Data Cache Data Port 1	SFID_DP_DC1 is an extension of SFID_DP_DC0 to allow for more message types. They act as a single logical entity.	DevHSW+
1101b	SFID_CRE	Check and		DevHSW+

SFID				
		Refinement Engine		
1110b-1111b	Reserved			

SIMD Mode

SIMD Mode

Project: HSW
Source: PRM
Size (in bits): 2

Value	Name	Project
0	SIMD4x2	HSW
1	SIMD8	All
2	SIMD16	All
3	SIMD32/64	All

SrcIndex

SrcIndex		
Project:	HSW	
Source:	EuIsa	
Size (in bits):	5	

Value	Name	Description
0	000000000000	dir | <0;1,0>
1	000000000010	(-) | dir | <0;1,0>
2	000000010000	dir | <0;>.zx
3	000000010010	(-) | dir | <0;>.zx
4	000000011000	dir | <0;>.wx
5	000000100000	dir | <0;>.xy
6	000000101000	dir | <0;>.yy
7	000001001000	dir | <0;4,1>
8	000001010000	dir | <0;>.zz
9	000001110000	dir | <0;>.zw
10	000001111000	dir | <0;8,4> / dir | <0;>.ww
11	001100000000	dir | <4;>.xx
12	001100000010	(-) | dir | <4;>.xx
13	001100001000	dir | <4;>.yx
14	001100010000	dir | <4;>.zx
15	001100010010	(-) | dir | <4;>.zx
16	001100100000	dir | <4;>.xy
17	001100101000	dir | <4;>.yy
18	001100111000	dir | <4;>wy
19	001101000000	dir | <4;4,0>
20	001101000010	(-) | dir | <4;4,0>
21	001101001000	dir | <4;>.yz
22	001101010000	dir | <4;>.zz
23	001101100000	dir | <4;>.xw
24	001101101000	dir | <4;>.yw
25	001101110000	dir | <4;>.zw
26	001101110001	(abs) | dir | <4;>.zw
27	001101111000	dir | <4;>.ww

SrcIndex		
28	010001101000	dir | <8;8,1>
29	010001101001	(abs) | dir | <8;8,1>
30	010001101010	(-) | dir | <8;8,1>
31	010110001000	dir | <16;16,1>

SrcMod

SrcMod	
Project:	HSW
Source:	EuIsa
Size (in bits):	2

Source Modifier
This field specifies the numeric modification of a source operand. The value of each data element of a source operand can optionally have its absolute value taken and/or its sign inverted prior to delivery to the execution pipe. The absolute value is prior to negate such that a guaranteed negative value can be produced.
This field only applies to source operand. It does not apply to destination.
This field is not present for an immediate source operand.

Value	Name	Description
00b	No modification	
01b	abs	Absolute value
10b	negate	Negate
11b	negate of abs	Negate of the absolute (forced negative value)

SURFACE_FORMAT

SURFACE_FORMAT

Project: HSW

Source: PRM

Size (in bits): 9

The following table indicates the supported surface formats and the 9-bit encoding for each. Note that some of these formats are used not only by the Sampling Engine, but also by the Data Port and the Vertex Fetch unit.

Value	Name	Bits Per Element (BPE)	Description
000h	R32G32B32A32_FLOAT	128	
001h	R32G32B32A32_SINT	128	
002h	R32G32B32A32_UINT	128	
003h	R32G32B32A32_UNORM	128	
004h	R32G32B32A32_SNORM	128	
005h	R64G64_FLOAT	128	
006h	R32G32B32X32_FLOAT	128	
007h	R32G32B32A32_SSCALED	128	
008h	R32G32B32A32_USCALED	128	
020h	R32G32B32A32_SFIXED	128	
021h	R64G64_PASSTHRU	128	
040h	R32G32B32_FLOAT	96	
041h	R32G32B32_SINT	96	
042h	R32G32B32_UINT	96	
043h	R32G32B32_UNORM	96	
044h	R32G32B32_SNORM	96	
045h	R32G32B32_SSCALED	96	
046h	R32G32B32_USCALED	96	
050h	R32G32B32_SFIXED	96	
080h	R16G16B16A16_UNORM	64	
081h	R16G16B16A16_SNORM	64	
082h	R16G16B16A16_SINT	64	
083h	R16G16B16A16_UINT	64	
084h	R16G16B16A16_FLOAT	64	
085h	R32G32_FLOAT	64	

SURFACE_FORMAT			
086h	R32G32_SINT	64	
087h	R32G32_UINT	64	
088h	R32_FLOAT_X8X24_TYPELESS	64	
089h	X32_TYPELESS_G8X24_UINT	64	
08Ah	L32A32_FLOAT	64	
08Bh	R32G32_UNORM	64	
08Ch	R32G32_SNORM	64	
08Dh	R64_FLOAT	64	
08Eh	R16G16B16X16_UNORM	64	
08Fh	R16G16B16X16_FLOAT	64	
090h	A32X32_FLOAT	64	
091h	L32X32_FLOAT	64	
092h	I32X32_FLOAT	64	
093h	R16G16B16A16_SSCALED	64	
094h	R16G16B16A16_USCALED	64	
095h	R32G32_SSCALED	64	
096h	R32G32_USCALED	64	
0A0h	R32G32_SFIXED	64	
0A1h	R64_PASSTHRU	64	
0C0h	B8G8R8A8_UNORM	32	
0C1h	B8G8R8A8_UNORM_SRGB	32	
0C2h	R10G10B10A2_UNORM	32	
0C3h	R10G10B10A2_UNORM_SRGB	32	
0C4h	R10G10B10A2_UINT	32	
0C5h	R10G10B10_SNORM_A2_UNORM	32	
0C7h	R8G8B8A8_UNORM	32	
0C8h	R8G8B8A8_UNORM_SRGB	32	
0C9h	R8G8B8A8_SNORM	32	
0CAh	R8G8B8A8_SINT	32	
0CBh	R8G8B8A8_UINT	32	
0CCh	R16G16_UNORM	32	
0CDh	R16G16_SNORM	32	
0CEh	R16G16_SINT	32	
0CFh	R16G16_UINT	32	
0D0h	R16G16_FLOAT	32	

SURFACE_FORMAT

0D1h	B10G10R10A2_UNORM	32	
0D2h	B10G10R10A2_UNORM_SRGB	32	
0D3h	R11G11B10_FLOAT	32	
0D6h	R32_SINT	32	
0D7h	R32_UINT	32	
0D8h	R32_FLOAT	32	
0D9h	R24_UNORM_X8_TYPELESS	32	
0DAh	X24_TYPELESS_G8_UINT	32	
0DDh	L32_UNORM	32	
0DEh	A32_UNORM	32	
0DFh	L16A16_UNORM	32	
0E0h	I24X8_UNORM	32	
0E1h	L24X8_UNORM	32	
0E2h	A24X8_UNORM	32	
0E3h	I32_FLOAT	32	
0E4h	L32_FLOAT	32	
0E5h	A32_FLOAT	32	
0E6h	X8B8_UNORM_G8R8_SNORM	32	
0E7h	A8X8_UNORM_G8R8_SNORM	32	
0E8h	B8X8_UNORM_G8R8_SNORM	32	
0E9h	B8G8R8X8_UNORM	32	
0EAh	B8G8R8X8_UNORM_SRGB	32	
0EBh	R8G8B8X8_UNORM	32	
0ECh	R8G8B8X8_UNORM_SRGB	32	
0EDh	R9G9B9E5_SHAREDEXP	32	
0EEh	B10G10R10X2_UNORM	32	
0F0h	L16A16_FLOAT	32	
0F1h	R32_UNORM	32	
0F2h	R32_SNORM	32	
0F3h	R10G10B10X2_USCALED	32	
0F4h	R8G8B8A8_SSCALED	32	
0F5h	R8G8B8A8_USCALED	32	
0F6h	R16G16_SSCALED	32	
0F7h	R16G16_USCALED	32	
0F8h	R32_SSCALED	32	

SURFACE_FORMAT			
0F9h	R32_USCALED	32	
100h	B5G6R5_UNORM	16	
101h	B5G6R5_UNORM_SRGB	16	
102h	B5G5R5A1_UNORM	16	
103h	B5G5R5A1_UNORM_SRGB	16	
104h	B4G4R4A4_UNORM	16	
105h	B4G4R4A4_UNORM_SRGB	16	
106h	R8G8_UNORM	16	
107h	R8G8_SNORM	16	
108h	R8G8_SINT	16	
109h	R8G8_UINT	16	
10Ah	R16_UNORM	16	
10Bh	R16_SNORM	16	
10Ch	R16_SINT	16	
10Dh	R16_UINT	16	
10Eh	R16_FLOAT	16	
10Fh	A8P8_UNORM_PALETTE0	16	
110h	A8P8_UNORM_PALETTE1	16	
111h	I16_UNORM	16	
112h	L16_UNORM	16	
113h	A16_UNORM	16	
114h	L8A8_UNORM	16	
115h	I16_FLOAT	16	
116h	L16_FLOAT	16	
117h	A16_FLOAT	16	
118h	L8A8_UNORM_SRGB	16	
119h	R5G5_SNORM_B6_UNORM	16	
11Ah	B5G5R5X1_UNORM	16	
11Bh	B5G5R5X1_UNORM_SRGB	16	
11Ch	R8G8_SSCALED	16	
11Dh	R8G8_USCALED	16	
11Eh	R16_SSCALED	16	
11Fh	R16_USCALED	16	
122h	P8A8_UNORM_PALETTE0	16	
123h	P8A8_UNORM_PALETTE1	16	

SURFACE_FORMAT			
124h	A1B5G5R5_UNORM	16	
125h	A4B4G4R4_UNORM	16	
126h	L8A8_UINT	16	
127h	L8A8_SINT	16	
140h	R8_UNORM	8	
141h	R8_SNORM	8	
142h	R8_SINT	8	
143h	R8_UINT	8	
144h	A8_UNORM	8	
145h	I8_UNORM	8	
146h	L8_UNORM	8	
147h	P4A4_UNORM_PALETTE0	8	
148h	A4P4_UNORM_PALETTE0	8	
149h	R8_SSCALED	8	
14Ah	R8_USCALED	8	
14Bh	P8_UNORM_PALETTE0	8	
14Ch	L8_UNORM_SRGB	8	
14Dh	P8_UNORM_PALETTE1	8	
14Eh	P4A4_UNORM_PALETTE1	8	
14Fh	A4P4_UNORM_PALETTE1	8	
150h	Y8_UNORM	8	
152h	L8_UINT	8	
153h	L8_SINT	8	
154h	I8_UINT	8	
155h	I8_SINT	8	
180h	DXT1_RGB_SRGB	0	
181h	R1_UNORM	1	
182h	YCRCB_NORMAL	0	
183h	YCRCB_SWAPUVY	0	
184h	P2_UNORM_PALETTE0	2	
185h	P2_UNORM_PALETTE1	2	
186h	BC1_UNORM	0	(DXT1)
187h	BC2_UNORM	0	(DXT2/3)
188h	BC3_UNORM	0	(DXT4/5)
189h	BC4_UNORM	0	

SURFACE_FORMAT

18Ah	BC5_UNORM	0	
18Bh	BC1_UNORM_SRGB	0	(DXT1_SRGB)
18Ch	BC2_UNORM_SRGB	0	(DXT2/3_SRGB)
18Dh	BC3_UNORM_SRGB	0	(DXT4/5_SRGB)
18Eh	MONO8	1	
18Fh	YCRCB_SWAPUV	0	
190h	YCRCB_SWAPY	0	
191h	DXT1_RGB	0	
192h	FXT1	0	
193h	R8G8B8_UNORM	24	
194h	R8G8B8_SNORM	24	
195h	R8G8B8_SSCALED	24	
196h	R8G8B8_USCALED	24	
197h	R64G64B64A64_FLOAT	256	
198h	R64G64B64_FLOAT	192	
199h	BC4_SNORM	0	
19Ah	BC5_SNORM	0	
19Bh	R16G16B16_FLOAT	48	
19Ch	R16G16B16_UNORM	48	
19Dh	R16G16B16_SNORM	48	
19Eh	R16G16B16_SSCALED	48	
19Fh	R16G16B16_USCALED	48	
1A1h	BC6H_SF16	0	
1A2h	BC7_UNORM	0	
1A3h	BC7_UNORM_SRGB	0	
1A4h	BC6H_UF16	0	
1A5h	PLANAR_420_8	0	
1A8h	R8G8B8_UNORM_SRGB	24	
1A9h	ETC1_RGB8	0	
1AAh	ETC2_RGB8	0	
1ABh	EAC_R11	0	
1ACh	EAC_RG11	0	
1ADh	EAC_SIGNED_R11	0	
1AEh	EAC_SIGNED_RG11	0	
1AFh	ETC2_SRGB8	0	

SURFACE_FORMAT			
1B0h	R16G16B16_UINT	48	
1B1h	R16G16B16_SINT	48	
1B2h	R32_SFIXED	32	
1B3h	R10G10B10A2_SNORM	32	
1B4h	R10G10B10A2_USCALED	32	
1B5h	R10G10B10A2_SSCALED	32	
1B6h	R10G10B10A2_SINT	32	
1B7h	B10G10R10A2_SNORM	32	
1B8h	B10G10R10A2_USCALED	32	
1B9h	B10G10R10A2_SSCALED	32	
1BAh	B10G10R10A2_UINT	32	
1BBh	B10G10R10A2_SINT	32	
1BCh	R64G64B64A64_PASSTHRU	256	
1BDh	R64G64B64_PASSTHRU	192	
1C0h	ETC2_RGB8_PTA	0	
1C1h	ETC2_SRGB8_PTA	0	
1C2h	ETC2_EAC_RGBA8	0	
1C3h	ETC2_EAC_SRGB8_A8	0	
1C8h	R8G8B8_UINT	24	
1C9h	R8G8B8_SINT	24	
1FFh	RAW	0	

Texture Coordinate Mode

Texture Coordinate Mode

Project: HSW

Source: PRM

Size (in bits): 3

Value	Name	Description	Project
0h	WRAP	Map is repeated in the U direction	All
1h	MIRROR	Map is mirrored in the U direction	All
2h	CLAMP	Map is clamped to the edges of the accessed map	All
3h	CUBE	For cube-mapping, filtering in edges access adjacent map faces	All
4h	CLAMP_BORDER	Map is infinitely extended with the border color	All
5h	MIRROR_ONCE	Map is mirrored once about origin, then clamped	All
7h	Reserved		All

ThreadCtrl

ThreadCtrl

Project: HSW

Source: EuIsa

Size (in bits): 2

Thread Control
This field provides explicit control for thread switching.

Value	Name	Description	Project
00b	Normal	Up to the GEN execution units to manage thread switching. This is the normal (and unnamed) mode. In this mode, for example, if the current instruction cannot proceed due to operand dependencies, the EU switches to the next available thread to fill the compute pipe. In another example, if the current instruction is ready to go, however, there is another thread with higher priority that also has an instruction ready, the EU switches to that thread. Execution may or may not be preempted by another thread following this instruction.	
01b	Atomic	Prevent any thread switch immediately following this instruction. Always execute the next instruction (which may not be next sequentially if the current instruction branches). The next instruction gets highest priority in the thread arbitration for the execution pipelines.	HSW
10b	Switch	A forced thread switch occurs after the current instruction is executed and before the next instruction. In addition, a long delay (longer than the execution pipe latency) is introduced for the current thread. Particularly, the instruction queue of the current thread is flushed after the current instruction is dispatched for execution. Switch is designed primarily as a safety feature in case there are race conditions for certain instructions. Force a switch to another thread after this instruction and before the next instruction.	
11b	Reserved		

VertStride

VertStride

Project: HSW

Source: EuIsa

Size (in bits): 4

Vertical Stride

The field provides the vertical stride of the register region in unit of data elements for an operand.

Encoding of this field provides values of 0 or powers of 2, ranging from 1 to 32 elements. Larger values are not supported due to the restriction that a source operand must reside within two adjacent 256-bit registers (64 bytes total).

Special encoding 1111b (0xF) is only valid when the operand is in register-indirect addressing mode (AddrMode = 1). If this field is set to 0xF, one or more sub-registers of the address registers may be used to compute the addresses. Each address sub-register provides the origin for a row of data element. The number of address sub-registers used is determined by the division of ExecSize of the instruction by the Width fields of the operand.

This field only applies to source operand. It does not apply to destination.

This field is not present for an immediate source operand.

Programming Notes	Project
For Align16 access mode, only encodings of 0000, 0010 and 0011 are allowed. Other codes are reserved.	HSW
Note 1: Vertical Stride larger than 32 is not allowed due to the restriction that a source operand must reside within two adjacent 256-bit registers (64 bytes total).	
Note 2: In Align16 access mode, as encoding 0xF is reserved, only single-index indirect addressing is supported.	
Note 3: If indirect address is supported for src1, encoding 0xF is reserved for src1 ◆ only single-index indirect addressing is supported.	
Note 4: Encoding 0010 applies for QWord-size operands.	DevHSW+

Value	Name	Programming Notes
0000b	0 elements	
0001b	1 element	Restriction : Align1 mode only.
0010b	2 elements	
0011b	4 elements	
0100b	8 elements	Restriction : Align1 mode only.
0101b	16 elements	Restriction : Applies to byte or word operand only. Align1 mode only.
0110b	32 elements	Restriction : Applies to byte operand only. Align1 mode only.
0111b-1110b	Reserved	
1111b	VxH or Vx1 mode	Restriction : Only valid for register-indirect addressing in Align1 mode.

Width

Width

Project: HSW

Source: EuIsa

Size (in bits): 3

This field specifies the number of elements in the horizontal dimension of the region for a source operand. This field cannot exceed the ExecSize field of the instruction.
This field only applies to source operand. It does not apply to destination.
This field is not present for an immediate source operand.

Programming Notes
Note that with ExecSize of 32, because the maximum Width is 16, there are at least two rows in a source region.

Value	Name
000b	1 elements
001b	2 elements
010b	4 elements
011b	8 elements
100b	16 elements
101b-111b	Reserved