Intel® OpenSource HD Graphics Programmer's Reference Manual (PRM)
Volume 3 Part 2: PCI Registers (Ivy Bridge)

For the 2012 Intel® Core™ Processor Family

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Contents

1. PCI Device 2 Configuration Space

The following table is ordered by register start offset.

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Vendor Identification	VID2	00h	01h	8086h	RO;
Device Identification	DID2	02h	03h	0152h	RO-V; RO-FW;
PCI Command	PCICMD2	04h	05h	0000h	RW; RO;
PCI Status	PCISTS2	06h	07h	0090h	RO; RO-V;
Revision Identification	RID2	08h	08h	00h	RO-FW;
Class Code	CC	09h	0Bh	030000h	RO-V; RO;
Cache Line Size	CLS	0Ch	0Ch	00h	RO;
Master Latency Timer	MLT2	0Dh	0Dh	00h	RO;
Header Type	HDR2	0Eh	0Eh	00h	RO;
Graphics Translation Table, Memory Mapped Range Address	GTTMMADR	10h	17h	0000000000000004h	RO; RW;
Graphics Memory Range Address	GMADR	18h	1Fh	000000000000000Ch	RW; RO; RW-L;
I/O Base Address	IOBAR	20h	23h	00000001h	RW; RO;
Subsystem Vendor Identification	SVID2	2Ch	2Dh	0000h	RW-O;
Subsystem Identification	SID2	2Eh	2Fh	0000h	RW-O;
Video BIOS ROM Base Address	ROMADR	30h	33h	00000000h	RO;
Capabilities Pointer	CAPPOINT	34h	34h	90h	RO-V;
Interrupt Line	INTRLINE	3Ch	3Ch	00h	RW;
Interrupt Pin	INTRPIN	3Dh	3Dh	01h	RO;
Minimum Grant	MINGNT	3Eh	3Eh	00h	RO;
Maximum Latency	MAXLAT	3Fh	3Fh	00h	RO;
Capability Identifier	CAPID0	40h	41h	0009h	RO;
Capabilities Control	CAPCTRL0	42h	43h	010Ch	RO;
Capabilities A	CAPID0_A	44h	47h	00000000h	RO-FW; RO-KFW;
Capabilities B	CAPID0_B	48h	4Bh	00000000h	RO-FW;
Mirror of GMCH Graphics Control Register	MGGC0	50h	51h	0028h	RO-V;
Device Enable	DEVEN0	54h	57h	0000209Fh	RO-V;
Base Data of Stolen Memory	BDSM	5Ch	5Fh	00000000h	RO-V;
Hardware Scratch Read Write	HSRW	60h	61h	0000h	RW;
Multi Size Aperture Control	MSAC	62h	62h	02h	RW; RW-K;
VTd Status	VTD_STATUS	63h	63h	00h	RO-VFW;
Capabilities List Control	CAPL	7Fh	7Fh	00h	RW;
Message Signaled Interrupts Capability ID	MSI_CAPID	90h	91h	D005h	RO;
Message Control	MC	92h	93h	0000h	RO; RW;
Message Address	MA	94h	97h	00000000h	RW; RO;
Message Data	MD	98h	99h	0000h	RW;
Advanced Features Capabilities Identifier and Next Pointer	AFCIDNP	A4h	A5h	0013h	RO;
Advanced Features Length and Capabilities	AFLC	A6h	A7h	0306h	RO;

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Advanced Features Control	AFCTL	A8h	A8h	00h	RW1S;
Advanced Features Status	AFSTS	A9h	A9h	00h	RO;
Power Management Capabilities ID	PMCAPID	D0h	D1h	A401h	RO;
Power Management Capabilities	PMCAP	D2h	D3h	0022h	RO;
Power Management Control/Status	PMCS	D4h	D5h	0000h	RO; RW;
Software SMI	SWSMI	E0h	E1h	0000h	RW;
Graphics System Event	GSE	E4h	E7h	00000000h	RW;
Software SCI	SWSCI	E8h	E9h	0000h	RW-O; RW;
ASL Storage	ASLS	FCh	FFh	00000000h	RW;

1.1 VID2 - Vendor Identification

B/D/F/Type:	0/2/0/PCI
Address Offset:	0-1h
Default Value:	8086h
Access:	RO;
Size:	16 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

Bit	Access	Default Value	RST/PWR	Description
15:0	RO	8086h	Uncore	Vendor Identification Number (VID): PCI standard identification for Intel.

1.2 DID2 - Device Identification

B/D/F/Type:	0/2/0/PCI
Address Offset:	2-3h
Default Value:	0152h
Access:	RO-V; RO-FW;
Size:	16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

This register is a 16-bit value assigned to the IVB graphics device.

Bit	Access	Default Value	RST/PWR	Description
15:4	RO-FW	015h	Uncore	Device Identification Number MSB (DID_MSB): This is the upper part of a 16-bit value assigned to the Graphics device. Changed the default value from 010h to 015h.

1.3 PCICMD2 - PCI Command

B/D/F/Type: 0/2/0/PCI

Address Offset: 4-5h

Default Value: 0000h

Access: RW; RO;

Size: 16 bits

BIOS Optimal Default: 00h

This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD Register in the IGD disables the IGD PCI-compliant master accesses to main memory.

Bit	Access	Default Value	RST/PWR	Description
15:11	RO	0h		Reserved (RSVD).
10	RW	0b	FLR, Uncore	Interrupt Disable (INTDIS): This bit disables the device from asserting INTx#. 0: Enable the assertion of this device's INTx# signal. 1: Disable the assertion of this device's INTx# signal, so that DO_INTx messages are not sent to DMI.
9	RO	0b	Uncore	Fast Back-to-Back (FB2B): Not Implemented. Hardwired to 0.
8	RO	0b	Uncore	SERR Enable (SERRE): Not Implemented. Hardwired to 0.
7	RO	0b	Uncore	Address/Data Stepping Enable (ADSTEP): Not Implemented. Hardwired to 0.
6	RO	0b	Uncore	Parity Error Enable (PERRE): Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that do not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.
5	RO	0b	Uncore	Video Palette Snooping (VPS): This bit is hardwired to 0 to disable snooping.
4	RO	0b	Uncore	Memory Write and Invalidate Enable (MWIE): Hardwired to 0. The IGD does not support memory write and invalidate commands.
3	RO	0b	Uncore	Special Cycle Enable (SCE): This bit is hardwired to 0. The IGD ignores Special cycles.

Bit	Access	Default Value	RST/PWR	Description
2	RW	0b	FLR, Uncore	Bus Master Enable (BME): 0: Disable IGD bus mastering. 1: Enable the IGD to function as a PCI-compliant master.
1	RW	0b	FLR, Uncore	Memory Access Enable (MAE): This bit controls the IGD's response to memory space accesses. 0: Disable. 1: Enable.
0	RW	0b	FLR, Uncore	I/O Access Enable (IOAE): This bit controls the IGD's response to I/O space accesses. 0: Disable. 1: Enable.

1.4 PCISTS2 - PCI Status

B/D/F/Type: 0/2/0/PCI

Address Offset: 6-7h

Default Value: 0090h

Access: RO; RO-V;

Size: 16 bits

BIOS Optimal Default: 0h

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant master abort and PCI compliant target abort.

PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

Bit	Access	Default Value	RST/PWR	Description
15	RO	0b	Uncore	Detected Parity Error (DPE): The IGD does not detect parity errors. This bit is hardwired to 0.
14	RO	0b	Uncore	Signaled System Error (SSE): The IGD never asserts SERR#, thus this bit is hardwired to 0.
13	RO	0b	Uncore	Received Master Abort Status (RMAS): The IGD never gets a Master Abort, thus this bit is hardwired to 0.
12	RO	0b	Uncore	Received Target Abort Status (RTAS): The IGD never gets a Target Abort, thus this bit is hardwired to 0.

Bit	Access	Default Value	RST/PWR	Description
11	RO	0b	Uncore	Signaled Target Abort Status (STAS): Hardwired to 0. The IGD does not use target abort semantics.
10:9	RO	00b	Uncore	DEVSEL Timing (DEVT): N/A. This field is hardwired to 00b.
8	RO	0b	Uncore	Master Data Parity Error Detected (DPD): Since Parity Error Response is hardwired to disabled (and the IGD does not do any parity detection), this bit is hardwired to 0.
7	RO	1b	Uncore	Fast Back-to-Back (FB2B): Hardwired to 1. The IGD accepts fast back-to-back when the transactions are not to the same agent.
6	RO	0b	Uncore	User Defined Format (UDF): Hardwired to 0.
5	RO	0b	Uncore	66 MHz PCI Capable (C66): N/A - Hardwired to 0.
4	RO	1b	Uncore	Capability List (CLIST): This bit is set to 1 to indicate that the register at 34h provides an offset into the function's PCI Configuration Space containing a pointer to the list's first item.
3	RO-V	0b	Uncore	Interrupt Status (INTSTS): This bit reflects the state of the interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, is the device's INTx# signal asserted.
2:0	RO	0h		Reserved (RSVD).

1.5 RID2 - Revision Identification

B/D/F/Type:	0/2/0/PCI
Address Offset:	8h
Default Value:	00h
Access:	RO-FW;
Size:	8 bits

This register contains the revision number for Device #2 Functions 0.

These bits are read only and writes to this register have no effect.

For the A-0 Stepping, the register value is 00h.

Bit	Access	Default Value	RST/PWR	Description
7:4	RO-FW	0h	Uncore	Revision Identification Number MSB (RID_MSB): Four MSB of RID.
3:0	RO-FW	0h	Uncore	Revision Identification Number LSB (RID_LSB): Four LSB of RID.

1.6 CC - Class Code

B/D/F/Type:	0/2/0/PCI
Address Offset:	9-Bh
Default Value:	030000h
Access:	RO-V; RO;
Size:	24 bits

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

Bit	Access	Default Value	RST/PWR	Description
23:16	RO-V	03h	Uncore	Base Class Code (BCC): This is an 8-bit value that indicates the base class code. When MGGC0[VAMEN] is 0 this code is 03h, indicating a Display Controller. When MGGC0[VAMEN] is 1 this code is value 04h, indicating a Multimedia Device.
15:8	RO-V	00h	Uncore	Sub-Class Code (SUBCC): When MGGC0[VAMEN] is 0 this value is determined based on Device 0 GGC register, GMS and IVD fields.

Bit	Access	Default Value	RST/PWR	Description
				00h: VGA compatible. 80h: Non VGA (GMS = "00h" or IVD = "1b"). When MGGC0[VAMEN] is 1, this value is 80h, indicating other multimedia device.
7:0	RO	00h	Uncore	Programming Interface (PI): When MGGC0[VAMEN] is 0 this value is 00h, indicating a Display Controller. When MGGC0[VAMEN] is 1 this value is 00h, indicating a NOP.

1.7 CLS - Cache Line Size

B/D/F/Type:	0/2/0/PCI
Address Offset:	Ch
Default Value:	00h
Access:	RO;
Size:	8 bits

The IGD does not support this register as a PCI slave.

Bit	Access	Default Value	RST/PWR	Description
7:0	RO	00h	Uncore	Cache Line Size (CLS): This field is hardwired to 0s. The IGD as a PCI-compliant master does not use the Memory Write and Invalidate command and, in general, does not perform operations based on cache line size.

1.8 MLT2 - Master Latency Timer

B/D/F/Type:	0/2/0/PCI
Address Offset:	Dh
Default Value:	00h
Access:	RO;
Size:	8 bits

The IGD does not support programming the master latency timer because it does not perform bursts.

Bit	Access	Default Value	RST/PWR	Description
7:0	RO	00h	Uncore	Master Latency Timer Count Value (MLTCV): Hardwired to 0s.

1.9 HDR2 - Header Type

B/D/F/Type:	0/2/0/PCI
Address Offset:	Eh
Default Value:	00h
Access:	RO;
Size:	8 bits

This register contains the Header Type of the IGD.

Bit	Access	Default Value	RST/PWR	Description
7	RO	0b	Uncore	Multi Function Status (MFUNC): Indicates if the device is a Multi-Function Device. This field is hardwired to 0, as graphics is a single function.
6:0	RO	00h	Uncore	Header Code (H): This 7-bit value indicates the Header Code for the IGD. This code has the value 00h, indicating a type 0 configuration space format.

1.10 GTTMMADR - Graphics Translation Table, Memory Mapped Range Address

B/D/F/Type:	0/2/0/PCI
Address Offset:	10-17h
Default Value:	0000000000000004h
Access:	RO; RW;
Size:	64 bits

This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. The range requires 4 MB combined for MMIO and Global GTT aperture, with 2 MB of that used by MMIO and 2 MB used by GTT. GTTADR begins at (GTTMMADR + 2 MB) while the MMIO base address will be the same as GTTMMADR.

For the Global GTT, this range is defined as a memory BAR in graphics device config space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT memory area.

The device snoops writes to this region in order to invalidate any cached translations within the various TLB's implemented on-chip.

The allocation is for 4 MB and the base address is defined by bits [38:22].

Bit	Access	Default Value	RST/PWR	Description
63:39	RW	0000000h	FLR, Uncore	Reserved for Memory Base Address (RSVDRW):

Bit	Access	Default Value	RST/PWR	Description
				Must be set to 0 since addressing above 512 GB is not supported.
38:22	RW	00000h	FLR, Uncore	Memory Base Address (MBA): Set by the OS, these bits correspond to address signals [38:22]. 4 MB combined for MMIO and Global GTT table aperture (2 MB for MMIO and 2 MB for GTT).
21:4	RO	00000h	Uncore	Address Mask (ADM): Hardwired to 0s to indicate at least 4 MB address range.
3	RO	0b	Uncore	Prefetchable Memory (PREFMEM): Hardwired to 0 to prevent prefetching.
2:1	RO	10b	Uncore	Memory Type (MEMTYP): 00: Indicate 32-bit base address. 01: Reserved. 10: Indicate 64-bit base address. 11: Reserved.
0	RO	0b	Uncore	Memory/IO Space (MIOS): Hardwired to 0 to indicate memory space.

1.11 GMADR - Graphics Memory Range Address

B/D/F/Type:	0/2/0/PCI
Address Offset:	18-1Fh
Default Value:	0000000000000000Ch
Access:	RW; RO; RW-L;
Size:	64 bits

GMADR is the PCI aperture used by software to access tiled GFX surfaces in a linear fashion.

Bit	Access	Default Value	RST/PWR	Description
63:39	RW	0000000h	FLR, Uncore	Reserved for Memory Base Address (RSVDRW): Must be set to 0 since addressing above 512GB is not supported.
38:29	RW	0000000000b	FLR, Uncore	Memory Base Address (MBA): Memory Base Address (MBA): Set by the OS, these bits correspond to address signals [38:29].
28	RW-L	0b	FLR, Uncore	512MB Address Mask (ADMSK512): This bit is either part of the Memory Base Address (R/W) or part of the

Bit	Access	Default Value	RST/PWR	Description
				Address Mask (RO), depending on the value of MSAC[2:1]. See MSAC (Dev2, Func 0, offset 62h) for details.
27	RW-L	0b	FLR, Uncore	256 MB Address Mask (ADMSK256): This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO), depending on the value of MSAC[2:1]. See MSAC (Dev 2, Func 0, offset 62h) for details.
26:4	RO	000000h	Uncore	Address Mask (ADM): Hardwired to 0s to indicate at least 128MB address range.
3	RO	1b	Uncore	Prefetchable Memory (PREFMEM): Hardwired to 1 to enable prefetching.
2:1	RO	10b	Uncore	Memory Type (MEMTYP): 00b: indicates 32-bit address. 10b: Indicates 64-bit address.
0	RO	0b	Uncore	Memory/IO Space (MIOS): Hardwired to 0 to indicate memory space.

1.12 IOBAR - I/O Base Address

B/D/F/Type:	0/2/0/PCI
Address Offset:	20-23h
Default Value:	00000001h
Access:	RW; RO;
Size:	32 bits
BIOS Optimal Default:	00000h

This register is the Base offset of the I/O registers within Device #2. Bits 15:6 are programmable, allowing the I/O Base to be located anywhere in 16-bit I/O Address Space. Bits 2:1 are fixed and return 0s; bit 0 is hardwired to a 1 indicating that 8 bytes of I/O space are decoded. Access to the 8Bs of IO space is allowed in PM state D0 when IO Enable (PCICMD bit 0) is set. Access is disallowed in PM states D1-D3 or if IO Enable is clear or if Device #2 is turned off or if Internal graphics is disabled through the fuse or fuse override mechanisms.

Note that access to this I/O BAR is independent of VGA functionality within Device #2.

If access to this I/O BAR is allowed then all 8, 16, or 32 bit I/O cycles from IA cores that fall within the 8B are claimed.

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	0h		Reserved (RSVD).
15:6	RW	000h	FLR, Uncore	I/O Base Address (IOBASE):

Bit	Access	Default Value	RST/PWR	Description
				Set by the OS, these bits correspond to address signals [15:6].
5:3	RO	0h		Reserved (RSVD).
2:1	RO	00b	Uncore	Memory Type (MEMTYPE): Hardwired to 0s to indicate 32-bit address.
0	RO	1b	Uncore	Memory / I/O Space (MIOS): Hardwired to 1 to indicate I/O space.

1.13 SVID2 - Subsystem Vendor Identification

B/D/F/Type:	0/2/0/PCI
Address Offset:	2C-2Dh
Default Value:	0000h
Access:	RW-O;
Size:	16 bits

This register uniquely identifies the subsystem where the PCI device resides.

Bit	Access	Default Value	RST/PWR	Description
15:0	RW-O	0000h	Uncore	Subsystem Vendor ID (SUBVID): This value identifies the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read-Only. This register can only be cleared by a Reset.

1.14 SID2 - Subsystem Identification

B/D/F/Type:	0/2/0/PCI
Address Offset:	2E-2Fh
Default Value:	0000h
Access:	RW-O;
Size:	16 bits

This register uniquely identifies the subsystem where the PCI device resides.

Bit	Access	Default Value	RST/PWR	Description
15:0	RW-O	0000h	Uncore	Subsystem Identification (SUBID): This value identifies a particular subsystem. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read-Only. This register can only be cleared by a Reset.

1.15 ROMADR - Video BIOS ROM Base Address

B/D/F/Type:	0/2/0/PCI
Address Offset:	30-33h
Default Value:	00000000h
Access:	RO;
Size:	32 bits
BIOS Optimal Default:	000h

The IGD does not use a separate BIOS ROM, therefore this register is hardwired to 0s.

Bit	Access	Default Value	RST/PWR	Description
31:18	RO	0000h	Uncore	ROM Base Address (RBA): Hardwired to 0s.
17:11	RO	00h	Uncore	Address Mask (ADMSK): Hardwired to 0s to indicate 256 KB address range.
10:1	RO	0h		Reserved (RSVD).
0	RO	0b	Uncore	ROM BIOS Enable (RBE): 0: ROM not accessible.

1.16 CAPPOINT - Capabilities Pointer

B/D/F/Type:	0/2/0/PCI
Address Offset:	34h
Default Value:	90h
Access:	RO-V;
Size:	8 bits

This register points to a linked list of capabilities implemented by this device.

Bit	Access	Default Value	RST/PWR	Description
7:0	RO-V	90h	Uncore	Capabilities Pointer Value (CPV): This field is an offset into the function's PCI Configuration Space for the first item in the New Capabilities Linked List, the MSI Capabilities ID registers at address 90h or the Power Management capability at D0h. This value is determined by the configuration in CAPL[0].

1.17 INTRLINE - Interrupt Line

B/D/F/Type:	0/2/0/PCI
Address Offset:	3Ch
Default Value:	00h
Access:	RW;
Size:	8 bits

This 8-bit register communicates interrupt line routing information. It is read/write and must be implemented by the device. POST software writes the routing information into this register as it initializes and configures the system.

The value in this register tells which input of the system interrupt controller(s) the device's interrupt pin is connected to. The device itself does not use this value, rather it is used by device drivers and operating systems to determine interrupt priority and vector information.

Bit	Access	Default Value	RST/PWR	Description
7:0	RW	00h	Uncore	Interrupt Connection (INTCON): Communicates interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The register value indicates to which input of the system interrupt controller the device's interrupt pin is connected.

1.18 INTRPIN - Interrupt Pin

B/D/F/Type:	0/2/0/PCI
Address Offset:	3Dh
Default Value:	01h
Access:	RO;
Size:	8 bits

This register tells which interrupt pin the device uses. The Integrated Graphics Device uses INTA#.

Bit	Access	Default Value	RST/PWR	Description
7:0	RO	01h	Uncore	Interrupt Pin (INTPIN): As a single function device, the IGD specifies INTA# as its interrupt pin. 01h: INTA#.

1.19 MINGNT - Minimum Grant Value

B/D/F/Type:	0/2/0/PCI
Address Offset:	3Eh
Default Value:	00h
Access:	RO;
Size:	8 bits

The Integrated Graphics Device has no requirement for the settings of Latency Timers.

Bit	Access	Default Value	RST/PWR	Description
7:0	RO	00h	Uncore	Minimum Grant Value (MGV): The IGD does not burst as a PCI-compliant master.

1.20 MAXLAT - Maximum Latency

B/D/F/Type:	0/2/0/PCI
Address Offset:	3Fh
Default Value:	00h
Access:	RO;
Size:	8 bits

The Integrated Graphics Device has no requirement for the settings of Latency Timers.

Bit	Access	Default Value	RST/PWR	Description
7:0	RO	00h	Uncore	Maximum Latency Value (MLV): The IGD has no specific requirements for how often it needs to access the PCI bus.

1.21 CAPID0 - Capability Identifier

B/D/F/Type:	0/2/0/PCI
Address Offset:	40-41h
Default Value:	0009h
Access:	RO;
Size:	16 bits

Control of bits in this register is only required for customer-visible SKU differentiation.

Bit	Access	Default Value	RST/PWR	Description
15:8	RO	00h	Uncore	Next Capability Pointer (NEXT_CAP): This field is hardwired to 00h indicating the end of the capabilities linked list.
7:0	RO	09h	Uncore	Capability Identifier (CAP_ID): This field has the value 1001b to identify the CAP_ID assigned by the PCI SIG for vendor-dependent capability pointers.

1.22 CAPCTRL0 - Capabilities Control

B/D/F/Type:	0/2/0/PCI
Address Offset:	42-43h
Default Value:	010Ch
Access:	RO;
Size:	16 bits
BIOS Optimal Default:	0h

Control of bits in this register is only required for customer visible SKU differentiation.

Bit	Access	Default Value	RST/PWR	Description
15:12	RO	0h		Reserved (RSVD).
11:8	RO	1h	Uncore	CAPID Version (CAPID_VER): This field has the value 0001b to identify the first revision of the CAPID register definition.
7:0	RO	0Ch	Uncore	CAPID Length (CAPIDLEN): This field has the value 0Ch to indicate the structure length (12 bytes).

1.23 CAPID0_A - Capabilities A

B/D/F/Type: 0/2/0/PCI

Address Offset: 44-47h

Default Value: 00000000h

Access: RO-FW; RO-KFW;

Size: 32 bits

BIOS Optimal Default: 000000h

Control of bits in this register is only required for customer-visible SKU differentiation.

Bit	Access	Default Value	RST/PWR	Description
31	RO-KFW	0b	Uncore	PEG60 Disable (PEG60D): 0: Device 6 Function 0 and associated memory spaces are accessible. 1: Device 6 Function 0 and associated memory and I/O spaces are disabled by hardwiring the D6F0EN field, bit 13 of the Device Enable register, (DEVEN Dev 0 Offset 54h) to 0.
30	RO-KFW	0b	Uncore	PEG12 Disable (PEG12D): 0: Device 1 Function 2 and associated memory spaces are accessible. 1: Device 1 Function 2 and associated memory and I/O spaces are disabled by hardwiring the D1F2EN field, bit 1 of the Device Enable register, (DEVEN Dev 0 Offset 54h) to 0.
29	RO-KFW	0b	Uncore	PEG11 Disable (PEG11D): 0: Device 1 Function 1 and associated memory spaces are accessible. 1: Device 1 Function 1 and associated memory and I/O spaces are disabled by hardwiring the D1F1EN field, bit 2 of the Device Enable register, (DEVEN Dev 0 Offset 54h) to 0.
28	RO-KFW	0b	Uncore	PEG10 Disable (PEG10D): 0: Device 1 Function 0 and associated memory spaces are accessible. 1: Device 1 Function 0 and associated memory and I/O spaces are disabled by hardwiring the D1F0EN field, bit 3 of the Device Enable register, (DEVEN Dev 0 Offset 54h) to 0.
27	RO-FW	0b	Uncore	PCI Express Link Width Upconfig Disable (PELWUD): 0: Link width upconfig is supported. The CPU advertises upconfig capability using the data rate symbol in its TS2 training ordered sets during Configuration.Complete. The CPU responds to link width upconfigs initiated by the downstream device. 1: Link width upconfig is NOT supported. The CPU does not advertise upconfig capability using the data rate field in TS2 training ordered sets during

Bit	Access	Default Value	RST/PWR	Description
				Configuration.Complete. The CPU does not respond to link width upconfigs initiated by the downstream device.
26	RO-FW	0b	Uncore	DMI Width (DW): 0: DMI x4. 1: DMI x2.
25	RO-FW	0b	Uncore	ECC Disable (ECCDIS): 0: ECC capable. 1: Not ECC capable.
24	RO-FW	0b	Uncore	Force DRAM ECC Enabled (FDEE): 0: DRAM ECC optional via software. 1: DRAM ECC enabled. MCHBAR C0MISCCTL bit [0] and C1MISCCTL bit [0] forced to 1 and Read-Only. NOTE: FDEE and ECCDIS must not both be 1.
23	RO-KFW	0b	Uncore	VTd Disable (VTDD): 0: Enable VTd. 1: Disable VTd.
22	RO-FW	0b	Uncore	DMI Gen 2 Disable (DMIG2DIS): 0: Capable of running DMI in Gen 2 mode. 1: Not capable of running DMI in Gen 2 mode.
21	RO-FW	0b	Uncore	PEG Gen 2 Disable (PEGG2DIS): 0: Can run any of the PEG controllers in Gen 2 mode. 1: Cannot run any of the PEG controllers in Gen 2 mode.
20:19	RO-FW	00b	Uncore	DDR Size (DDRSZ): This field defines the maximum allowed memory size per channel. 00b: Unlimited (16GB per channel) 01b: Maximum 8GB per channel 10b: Maximum 2GB per channel 11b: Maximum 0.5GB per channel
18	RO-FW	0b	Uncore	Spare (SPARE18).
17	RO-FW	0b	Uncore	Disable 1N Mode (D1NM): 0: Part can support 1n mode timings on the DDR interface. 1: Part cannot support 1n mode. The only supported timings are 2n or greater.
15	RO-KFW	0b	Uncore	Camarillo Device Disable (CDD):

Bit	Access	Default Value	RST/PWR	Description
				0: Camarillo Device enabled. 1: Camarillo Device disabled
14	RO-FW	0b	Uncore	2 DIMMS per Channel Disable (DDPCD): Allows Dual Channel operation but only supports 1 DIMM per channel. 0: 2 DIMMs per channel enabled. 1: 2 DIMMs per channel disabled. This setting hardwires bits 2 and 3 of the rank population field for each channel to zero (MCHBAR offset 260h, bits 22-23 for channel 0 and MCHBAR offset 660h, bits 22-23 for channel 1).
13	RO-FW	0b	Uncore	X2APIC Enabled (X2APIC_EN): Extended Interrupt Mode. 0: Hardware does not support Extended APIC mode. 1: Hardware supports Extended APIC mode.
12	RO-FW	0b	Uncore	Performance Dual Channel Disable (PDCD): 0: Capable of Dual Channels. 1: Not Capable of Dual Channels - only single channel capable.
11	RO-KFW	0b	Uncore	Internal Graphics Disable (IGD): 0: There is a graphics engine within this CPU. Internal Graphics Device (Device 2) is enabled and all of its memory and I/O spaces are accessible. Configuration cycles to Device 2 are completed within the CPU. All non-SMM memory and I/O accesses to VGA are handled based on Memory and I/O enables of Device 2 and I/O registers within Device 2 and VGA Enable of the PCI to PCI bridge control register in Devices 1 and 6 (If PCI Express GFX attach is supported). A selected amount of Graphics Memory space is pre-allocated from the main memory based on Graphics Mode Select (GMS in the GGC Register). Graphics Memory is pre-allocated above TSEG Memory. 1: There is no graphics engine within this CPU. Internal Graphics Device (Device 2) and all of its memory and I/O functions are disabled. Configuration cycle targeted to Device 2 are passed on to DMI. In addition, all clocks to internal graphics logic are turned off. All non-SMM memory and I/O accesses to VGA are handled based on VGA Enable of the PCI to PCI bridge control register in Devices 1 and 6. DEVEN [4:3] (Device 0, offset 54h) has no meaning. Device 2 Functions 0 and 1 are disabled and hidden.
9:8	RO-FW	00b	Uncore	Capability Device ID (CDID): Identifier assigned to the core/primary PCI device.
7:4	RO-FW	0h	Uncore	Compatibility Rev ID (CRID): This 4-bit value is the revision identification number for the Host Device 0. For the A-0 Stepping, this value is 00h.
3	RO-FW	0b	Uncore	DDR Overclocking (DDR_OVERCLOCK): Indicates support for DDR Overclocking.

Bit	Access	Default Value	RST/PWR	Description
2	RO-FW	0b	Uncore	IA Overclocking Enabled by DSKU (OC_ENABLED_DSKU): The default constant (non-fuse) value is zero. When the VDM sets this bit, we will apply OC if OC_CTL_SSKU points to DSKU.
1	RO-FW	0b	Uncore	On-die DDR write Vref generation allowed (DDR_WRTVREF): Allow on-die DDR write Vref generation. PCODE will update this field with the value ofFUSE_DDR_WRTVREF.
0	RO-FW	0b	Uncore	DDR3L (1.35V DDR) operation allowed (DDR3L_EN): Allow DDR3L (1.35V DDR) operation. PCODE updates this field with the value ofFUSE_DDR3L_EN.

1.24 CAPID0_B - Capabilities B

B/D/F/Type: 0/2/0/PCI

Address Offset: 48-4Bh

Default Value: 00000000h

Access: RO-FW;

Size: 32 bits

BIOS Optimal Default: 00h

Control of bits in this register is only required for customer-visible SKU differentiation.

Bit	Access	Default Value	RST/PWR	Description
30	RO-FW	0b	Uncore	IA Overclocking is controlled by SSKU rather than DSKU (OC_CTL_SSKU): PCODE updates this field with the value of FUSE_OC_CTL_SSKU and then applies SSKU overrides. IA Overclocking is controlled by SSKU rather than DSKU.
29	RO-FW	0b	Uncore	IA Overclocking Enabled by SSKU (OC_ENABLED_SSKU): PCODE updates this field with the value of FUSE_OC_ENABLED_SSKU. 0: Over-clocking is Disabled. 1: Over-clocking is Enabled. If over-clocking is enabled, FUSE_OC_BINS contains how many bits of over-clocking are supported, with the following encoding: 0h: Overclocking is disabled. 1h: Max 1 bin of overclocking is allowed. 2h: Max 2 bins of overclocking are allowed. 3h: Max 3 bins of overclocking are allowed. 4h: Max 4 bins of overclocking are allowed.

Bit	Access	Default Value	RST/PWR	Description
				5h: Max 5 bins of overclocking are allowed. 6h: Max 6 bins of overclocking are allowed. 7h: Overclocking is not limited. If overclocking is not enabled, FUSE_OC_BINS is meaningless, and should be 0.
28	RO-FW	0b	Uncore	SMT Capability (SMT): This setting indicates whether the CPU is SMT capable.
27:25	RO-FW	000b	Uncore	Cache Size Capability (CACHESZ): This setting indicates the supporting cache sizes.
24	RO-FW	0b	Uncore	Soft Bin Capability (SOFTBIN): CPU is Soft Bin capable via FUSE_SSKU_SOFT_BIN_EN and if it is enabled by the PCH. Both the Mask and Value are needed to enable this feature. If enabled, PCODE uses the final resolved values in CAPID.D-G (except CAPID0_E[31:12]) for frequency/branding instead of the baseline non-SSKU fused values.
23:21	RO-FW	000b	Uncore	DDR3 Maximum Frequency Capability with 100 Memory (PLL_REF100_CFG): DDR3 Maximum Frequency Capability with 100 Memory. PCODE updates this field with the value of FUSE_PLL_REF100_CFG and then applies SSKU overrides. Maximum allowed memory frequency with 100 MHz ref clk. Also serves as defeature. Unlike 133 MHz ref fuses, this is a normal 3-bit field: 0: 100 MHz ref disabled. 1: Up to DDR-1400 (7 x 200). 2: Up to DDR-1600 (8 x 200). 3: Up to DDR-1800 (9 x 200). 4: Up to DDR-2000 (10 x 200). 5: Up to DDR-2200 (11 x 200). 6: Up to DDR-2400 (12 x 200). 7: No limit (but still limited by %MAX_DDR_FREQ200 to 2600).
20	RO-FW	0b	Uncore	PCIe Gen 3 Disable (PEGG3_DIS): IVB: PCIe Gen 3 Disable. PCODE updates this field with the value of FUSE_PEGG3_DIS and then applies SSKU overrides. This is a defeature fuse; an un-programmed device should have PCIe Gen 3 capabilities enabled. 0: Capable of running any of the Gen 3-compliant PEG controllers in Gen 3 mode (Devices 0/1/0, 0/1/1, 0/1/2). 1: Not capable of running any of the PEG controllers in Gen 3 mode.

Bit	Access	Default Value	RST/PWR	Description
19	RO-FW	0b	Uncore	Package Type (PKGTYP): This setting indicates the CPU Package Type.
18	RO-FW	0b	Uncore	Additive Graphics Enabled (ADDGFXEN): 0: Additive Graphics Disabled. 1: Additive Graphics Enabled.
17	RO-FW	0b	Uncore	Additive Graphics Capable (ADDGFXCAP): 0 - Capable of Additive Graphics 1 - Not capable of Additive Graphics
16	RO-FW	0b	Uncore	PCIe lane control x16/x8 (PEGX16D): 0: Capable of x16 PEGPort 1: Not Capable of x16 PEG port, instead PEG is limited to x8 and below. Causes PEG port to enable and train logical lanes 7:0 only. Logical lanes 15:8 are powered down (unless in use by the other PEG port or the embedded Display Port), and the Max Link Width field of the Link Capability register reports x8 instead of x16. (In the case of lane reversal, lanes 15:8 are active and lanes 7:0 are powered down.)
15:12	RO-FW	0h	Uncore	Reserved for Future Capabilities (SPARE15_12): Reserved for future capabilities.
6:4	RO-FW	000b	Uncore	DDR3 Maximum Frequency Capability (DMFC): PCODE updates this field with the value of FUSE_DMFC, and then applies SSKU overrides. Maximum allowed memory frequency with 133 MHz ref clk. This is a reversed 3-bit field: 7: Up to DDR-1066 (4 x 266). 6: Up to DDR-1333 (5 x 266). 5: Up to DDR-1600 (6 x 266). 4: Up to DDR-1866 (7 x 266). 3: Up to DDR-2133 (8 x 266). 2: Up to DDR-2400 (9 x 266). 1: Up to DDR-2666 (10 x 266). 0: Up to DDR-2933 (11 x 266). This is a **reserved** fuse value, not currently supported.
3	RO-FW	0b	Uncore	Reserved for Future Capabilities (SPARE3): Reserved for future capabilities
2	RO-FW	0b	Uncore	Reserved for Future Capabilities (SPARE2): Reserved for future capabilities

Bit	Access	Default Value	RST/PWR	Description
1	RO-FW	0b	Uncore	Dual PEG Force x1 when VGA Enabled (DPEGFX1): This bit has no effect on Device 1 unless Device 1 is configured for at least two ports via the PEG0CFGSEL strap. This bit always applies to Device 6. 0: All PEG port widths do not depend on their respective BCTRL[VGAEN]. 1: Each PEG port width is limited to x1 operation when its respective BCTRL[VGAEN] is set to 1b.
0	RO-FW	0b	Uncore	Single PEG Force x1 when VGA Enabled (SPEGFX1): This bit has no effect on Device 1 unless Device 1 is configured for a single port via the PEG0CFGSEL strap. This bit always applies to Device 6. 0: PEG10 and PEG60 widths do not depend on their respective BCTRL[VGAEN]. 1: PEG10 and PEG60 widths are limited to x1 operation when their respective BCTRL[VGAEN] is set to 1b.

1.25 MGGC0 - Mirror of GMCH Graphics Control Register

B/D/F/Type: 0/2/0/PCI

Address Offset: 50-51h

Default Value: 0028h

Access: RO-V;

Size: 16 bits

BIOS Optimal Default: 00h

All bits in this register are LT lockable.

Bit	Access	Default Value	RST/PWR	Description
15	RO	0h		Reserved (RSVD).
14	RO-V	0b	Uncore	Versatile Acceleration Mode Enable (VAMEN): Enables the use of the iGFXenbines for Versatile Acceleration. 1: iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 048000h. 0: iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h.
13:10	RO	0h		Reserved (RSVD).
9:8	RO-V	0h	Uncore	GTT Graphics Memory Size (GGMS): This field selects the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS

<table>
<tr><th>Bit</th><th>Access</th><th>Default Value</th><th>RST/PWR</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td></td><td>needs to allocate a contiguous memory chunk. Hardware derives the base of GSM from DSM using only the GSM size programmed in the register.

Hardware functionality in case of programming this value to Reserved is not guaranteed.

<table><tr><th>Encoding</th><th>Description</th></tr><tr><td>1h</td><td>1MB of Preallocated Memory</td></tr><tr><td>3h</td><td>Reserved</td></tr><tr><td>2h</td><td>2MB of Preallocated Memory</td></tr><tr><td>0h</td><td>No Preallocated Memory</td></tr></table></td></tr>
<tr><td>7:3</td><td>RO-V</td><td>05h</td><td>Uncore</td><td>Graphics Mode Select (GMS):

This field selects the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.

This register is also LT lockable.

Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled.

BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0.

<table><tr><th>Encoding</th><th>Description</th></tr><tr><td>5h</td><td>32 MB</td></tr><tr><td>6h</td><td>48 MB</td></tr><tr><td>7h</td><td>64 MB</td></tr><tr><td>8h</td><td>128 MB</td></tr><tr><td>9h</td><td>256 MB</td></tr><tr><td>Ah</td><td>96 MB</td></tr><tr><td>Bh</td><td>160 MB</td></tr><tr><td>Ch</td><td>224 MB</td></tr><tr><td>Dh</td><td>352 MB</td></tr><tr><td>0h</td><td>0MB</td></tr><tr><td>1h</td><td>32MB</td></tr><tr><td>2h</td><td>64MB</td></tr><tr><td>3h</td><td>96MB</td></tr><tr><td>4h</td><td>128MB</td></tr><tr><td>Eh</td><td>448MB</td></tr><tr><td>Fh</td><td>480MB</td></tr><tr><td>10h</td><td>512MB</td></tr><tr><td>Other</td><td>Reserved</td></tr><tr><td>0h</td><td>0MB</td></tr><tr><td>1h</td><td>32MB</td></tr><tr><td>2h</td><td>64MB</td></tr><tr><td>3h</td><td>96MB</td></tr><tr><td>4h</td><td>128MB</td></tr><tr><td>5h</td><td>160MB</td></tr><tr><td>6h</td><td>192MB</td></tr><tr><td>7h</td><td>224MB</td></tr><tr><td>8h</td><td>256MB</td></tr><tr><td>9h</td><td>288MB</td></tr></table></td></tr>
</table>

Bit	Access	Default Value	RST/PWR	Description	
				Ah	320MB
				Bh	352MB
				Ch	384MB
				Dh	416MB
				Eh	448MB
				Fh	480MB
				10h	512MB
				Other	Reserved
2	RO	0h		Reserved (RSVD).	
1	RO-V	0b	Uncore	IGD VGA Disable (IVD): 0: Enable. Device 2 (IGD) claims VGA memory and I/O cycles. The Sub-Class Code within Device 2 Class Code register is 00. 1: Disable. Device 2 (IGD) does not claim VGA memory or I/O cycles. The Sub-Class Code field within Device 2 function 0 Class Code register is 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field (bits 7:3 of this register) pre-allocates no memory. This bit MUST be set to 1 if Device 2 is disabled, either via a fuse or a fuse override (CAPID0_A[IGD] = 1) or via a register (DEVEN[3] = 0). This register is locked by LT lock.	
				Encoding	Description
				0b	Enable
				1b	Disable
				0b	Enable
				1b	Disable
				0b	Enable
				1b	Disable
0	RO-V	0b	Uncore	GGC Lock (GGCLCK): When set to 1b, this bit locks all bits in this register.	

1.26 DEVEN0 - Device Enable

B/D/F/Type: 0/2/0/PCI

Address Offset: 54-57h

Default Value: 0000209Fh

Access: RO-V;

Size: 32 bits

BIOS Optimal Default: 000000h

Supports enabling or disabling PCI devices and functions within the CPU package. The table below the bit definitions describes the behavior of all combinations of transactions to devices controlled by this register.

All the bits in this register are LT Lockable.

Bit	Access	Default Value	RST/PWR	Description
31:15	RO	0h		Reserved (RSVD).
14	RO-V	0b	Uncore	Chap Enable (D7EN): 0: Bus 0 Device 7 is disabled and not visible. 1: Bus 0 Device 7 is enabled and visible. Non-production BIOS code should provide a setup option to enable Bus 0 Device 7. When enabled, Bus 0 Device 7 must be initialized in accord with standard PCI device initialization procedures.
				Encoding / **Description** 0b / Device 7 disabled. 1b / Device 7 enabled.
13	RO-V	1b	Uncore	PEG60 Enable (D6F0EN): 0: Bus 0 Device 6 Function 0 is disabled and hidden. 1: Bus 0 Device 6 Function 0 is enabled and visible. This bit is set to 0 and remains 0 if PEG60 capability is disabled.
				Encoding / **Description** 0b / Device 6 disabled. 1b / Device 6 enabled. 0b / Device 6 disabled. 1b / Device 6 enabled. 0b / Device 6 disabled. 1b / Device 6 enabled. 0b / Device 6 disabled. 1b / Device 6 enabled. 0b / Device 6 disabled. 1b / Device 6 enabled. 0b / Device 6 disabled. 1b / Device 6 enabled. 0b / Device 6 disabled. 1b / Device 6 enabled. 0b / Device 6 disabled. 1b / Device 6 enabled. 0b / Device 6 disabled. 1b / Device 6 enabled.
12:8	RO	0h		Reserved (RSVD).
7	RO-V	1b	Uncore	Device 4 Enable (D4EN): 0: Bus 0 Device 4 is disabled and not visible. 1: Bus 0 Device 4 is enabled and visible. This bit is set to 0 and remains 0 if Device 4 capability is disabled.
6:5	RO	0h		Reserved (RSVD).
4	RO-V	1b	Uncore	Internal Graphics Engine (D2EN): 0: Bus 0 Device 2 is disabled and hidden. 1: Bus 0 Device 2 is enabled and visible.

Bit	Access	Default Value	RST/PWR	Description
				This bit is set to 0 and remains 0 if Device 2 capability is disabled.
3	RO-V	1b	Uncore	PEG10 Enable (D1F0EN): 0: Bus 0 Device 1 Function 0 is disabled and hidden. 1: Bus 0 Device 1 Function 0 is enabled and visible. This bit is set to 0 and remains 0 if PEG10 capability is disabled.
2	RO-V	1b	Uncore	PEG11 Enable (D1F1EN): 0: Bus 0 Device 1 Function 1 is disabled and hidden. 1: Bus 0 Device 1 Function 1 is enabled and visible. This bit is set to 0 and remains 0 if: - PEG11 capability is disabled by fuses, OR - PEG11 is disabled by strap (PEG0CFGSEL).
1	RO-V	1b	Uncore	PEG12 Enable (D1F2EN): 0: Bus 0 Device 1 Function 2 is disabled and hidden. 1: Bus 0 Device 1 Function 2 is enabled and visible. This bit is set to 0 and remains 0 if: - PEG12 capability is disabled by fuses, OR - PEG12 is disabled by strap (PEG0CFGSEL).
0	RO-V	1b	Uncore	Host Bridge (D0EN): Bus 0 Device 0 Function 0 cannot be disabled and is therefore hardwired to 1.

1.27 BDSM - Base Data of Stolen Memory

B/D/F/Type:	0/2/0/PCI
Address Offset:	5C-5Fh
Default Value:	00000000h
Access:	RO-V;
Size:	32 bits
BIOS Optimal Default:	00000h

This register contains the base address of graphics data stolen DRAM memory. The BIOS determines the base of graphics data stolen memory by subtracting the graphics data stolen memory size (PCI Device 0 offset 52 bits 7:4) from TOLUD (PCI Device 0 offset BC bits 31:20).

Bit	Access	Default Value	RST/PWR	Description
31:20	RO-V	000h	Uncore	Graphics Base of Stolen Memory (BDSM): This register contains bits 31 to 20 of the base address of stolen DRAM memory. The BIOS determines the base of graphics stolen memory by subtracting the graphics stolen memory size (PCI Device 0 offset 52 bits 6:4) from TOLUD (PCI Device 0 offset BC bits 31:20).
19:1	RO	0h		Reserved (RSVD).
0	RO-V	0b	Uncore	Lock (LOCK): This bit locks all writeable settings in this register, including itself.

1.28 HSRW - Hardware Scratch Read Write

B/D/F/Type:	0/2/0/PCI
Address Offset:	60-61h
Default Value:	0000h
Access:	RW;
Size:	16 bits

This register is reserved as a hardware scratchpad.

Bit	Access	Default Value	RST/PWR	Description
15:0	RW	0000h	FLR, Uncore	Reserved R/W (ReservedRW): Reserved for future use.

1.29 MSAC - Multi Size Aperture Control

B/D/F/Type:	0/2/0/PCI
Address Offset:	62h
Default Value:	02h
Access:	RW; RW-K;
Size:	8 bits
BIOS Optimal Default:	0h

This register determines the size of the graphics memory aperture in function 0 and in the trusted space. Only the system BIOS writes this register based on pre-boot address allocation efforts, but the graphics may read this register to determine the correct aperture size. The system BIOS needs to save this value on boot so that it can reset it correctly during S3 resume.

Note: This register is LT locked. It becomes read-only when trusted environment is launched.

Bit	Access	Default Value	RST/PWR	Description
7:4	RW	0h	Uncore	Reserved R/W (RSVDRW): Scratch Bits Only. Have no physical effect on hardware.
3:3	RO	0h		Reserved (RSVD).
2	RW-K	0b	Uncore	Untrusted Aperture Size High (LHSASH): This field is used with LHSASL. The description below is for both fields (LHSASH & LHSASL). 11b: Bits [28:27] of GMADR are RO, allowing 512 MB of GMADR. 10b: Illegal Programming. 01b: Bit [28] of GMADR is RW but bit [27] of GMADR is RO, allowing 256 MB of GMADR. 00b: Bits [28:27] of GMADR are RW, allowing 128 MB of GMADR.
1	RW-K	1b	Uncore	Untrusted Aperture Size Low (LHSASL): This field is used with LHSASH. The description below is for both fields (LHSASH & LHSASL). 11b: Bits [28:27] of GMADR are RO, allowing 512 MB of GMADR. 10b: Illegal Programming. 01b: Bit [28] of GMADR is RW but bit [27] of GMADR is RO, allowing 256 MB of GMADR. 00b: Bits [28:27] of GMADR are RW, allowing 128 MB of GMADR.
0:0	RO	0h		Reserved (RSVD).

1.30 VTD_STATUS - VTd Status

B/D/F/Type: 0/2/0/PCI

Address Offset: 63h

Default Value: 00h

Access: RO-VFW;

Size: 8 bits

BIOS Optimal Default: 00h

This register contains indicator bits for Graphics VTd mode.

Bit	Access	Default Value	RST/PWR	Description
7:1	RO	0h		Reserved (RSVD).
0	RO-VFW	0b	Uncore	GFX VTd Active (VTACT): Reflects whether GFX VTd Mode is active, 1 if active, 0 if inactive.

1.31 MSI_CAPID - Message Signaled Interrupts Capability ID

B/D/F/Type:	0/2/0/PCI
Address Offset:	90-91h
Default Value:	D005h
Access:	RO;
Size:	16 bits

When a device supports MSI it can generate an interrupt request to the processor by writing a predefined data item (a message) to a predefined memory address. Reporting this capability's existence can be disabled by setting MSICH (CAPL[0] @ 7Fh). In that case, walking this linked list skips this capability and instead goes directly to the PCI PM capability.

Bit	Access	Default Value	RST/PWR	Description
15:8	RO	D0h	Uncore	Pointer to Next Capability (POINTNEXT): This field is a pointer to the next item in the capabilities list, which is the Power Management capability.
7:0	RO	05h	Uncore	Capability ID (CAPID): 05h: Identifies this linked list item (capability structure) as being for MSI registers.

1.32 MC - Message Control

B/D/F/Type:	0/2/0/PCI
Address Offset:	92-93h
Default Value:	0000h
Access:	RO; RW;
Size:	16 bits
BIOS Optimal Default:	00h

System software can modify bits in this register, but the device is prohibited from doing so. If the device writes the same message multiple times, only one of those messages is guaranteed to be serviced. If all of them must be serviced, the device must not generate the same message again until the driver services the earlier one.

Bit	Access	Default Value	RST/PWR	Description
15:8	RO	0h		Reserved (RSVD).
7	RO	0b	Uncore	64 Bit Capable (CAP64B): Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message Address register and is not able to generate a 64-bit memory address.
6:4	RW	000b	FLR,	Multiple Message Enable (MME):

Bit	Access	Default Value	RST/PWR	Description
			Uncore	System software programs this field to indicate the actual number of messages allocated to this device. This number will be less than or equal to the number actually requested. The encoding is the same as for the MMC field below.
3:1	RO	000b	Uncore	Multiple Message Capable (MMC): System software reads this field to determine the number of messages requested by this device. Value: Number of requests 000: 1 All of the following are reserved in this implementation: 001: 2 010: 4 011: 8 100: 16 101: 32 110: Reserved 111: Reserved
0	RW	0b	FLR, Uncore	MSI Enable (MSIEN): Controls this device's ability to generate MSIs.

1.33 MA - Message Address

B/D/F/Type:	0/2/0/PCI
Address Offset:	94-97h
Default Value:	00000000h
Access:	RW; RO;
Size:	32 bits

This register contains the Message Address for MSIs sent by the device.

Bit	Access	Default Value	RST/PWR	Description
31:2	RW	00000000h	FLR, Uncore	Message Address (MESSADD): Used by system software to assign an MSI address to the device. The device handles an MSI by writing the padded contents of the MD register to this address.
1:0	RO	00b	Uncore	Force Dword Align (FDWORD): Hardwired to 0 so that addresses assigned by system software are always aligned on a DWORD address boundary.

1.34 MD - Message Data

B/D/F/Type:	0/2/0/PCI
Address Offset:	98-99h
Default Value:	0000h
Access:	RW;
Size:	16 bits

This register contains the Message Data for MSIs sent by the device.

Bit	Access	Default Value	RST/PWR	Description
15:0	RW	0000h	FLR, Uncore	Message Data (MESSDATA): Base message data pattern assigned by system software and used to handle an MSI from the device. When the device must generate an interrupt request, it writes a 32-bit value to the memory address in the MA register. The upper 16 bits are always set to 0. The lower 16 bits are supplied by this register.

1.35 AFCIDNP - Advanced Features Capabilities Identifier and Next Pointer

B/D/F/Type:	0/2/0/PCI
Address Offset:	A4-A5h
Default Value:	0013h
Access:	RO;
Size:	16 bits

When this capability is linked into the list, the second function of the Internal Graphics Device can be reset independently of the first function.

Bit	Access	Default Value	RST/PWR	Description
15:8	RO	00h	Uncore	NEXT_PTR (NEXT_PTR): This field is a pointer to the next item in the capabilities list. If this is the final capability in the list then this field must be 00h.
7:0	RO	13h	Uncore	CAP_ID (CAP_ID): A value of 13h identifies that this PCI Function is capable of Advanced Features.

1.36 AFLC - Advanced Features Length and Capabilities

B/D/F/Type:	0/2/0/PCI
Address Offset:	A6-A7h
Default Value:	0306h
Access:	RO;
Size:	16 bits
BIOS Optimal Default:	00h

See the July 27th 2006 Engineering Change Notice for Conventional PCI Advanced Capabilities.

Bit	Access	Default Value	RST/PWR	Description
15:10	RO	0h		Reserved (RSVD).
9	RO	1b	Uncore	FLR Capability (FLR_CAP): Indicates support for Function Level Reset (FLR).
8	RO	1b	Uncore	TXP Capability (TXP_CAP): Indicates support for the Transactions Pending bit.
7:0	RO	06h	Uncore	Capability Length (CAP_LEN): The Advanced Features capability structure requires 6 bytes of configuration space.

1.37 AFCTL - Advanced Features Control

B/D/F/Type: 0/2/0/PCI

Address Offset: A8h

Default Value: 00h

Access: RW1S;

Size: 8 bits

BIOS Optimal Default: 00h

Bit	Access	Default Value	RST/PWR	Description
7:1	RO	0h		Reserved (RSVD).
0	RW1S	0b	FLR, Uncore	Initiate Function Level Reset (INIT_FLR): A write of 1b initiates Function Level Reset (FLR). FLR requirements are defined in the PCI Express Base Specification. Registers and state information that do not apply to conventional PCI are exempt from the FLR requirements given there. Once written 1, FLR will be initiated. During FLR, a read returns 1s since device 2 reads abort. Once FLR completes, hardware clears the bit to 0. The following sequence is required in order to initiate the FLR for 0/2/0 PCI: 1. Write MMIO 0x45010=0x00000002 2. Write MMIO 0xC2004=0x00000005 3. Read MMIO 0xC7204, modify bit 0=0, write back to MMIO 0xC7204 4. Poll for MMIO 0xC7200 bit 31=0 and bits 29:28=00. Timeout and continue if poll not complete after 5 seconds. 5. Write MMIO 0xD0100=0x00000002 6. Write 1b to INIT_FLR The above MMIO register addresses are offsets from the 0/2/0 PCI config register offset 0x10, GTTMMADR, bits 38:22 Memory Base Address (MBA).

1.38 AFSTS - Advanced Features Status

B/D/F/Type:	0/2/0/PCI
Address Offset:	A9h
Default Value:	00h
Access:	RO;
Size:	8 bits
BIOS Optimal Default:	00h

See the July 27th 2006 Engineering Change Notice for Conventional PCI Advanced Capabilities.

Bit	Access	Default Value	RST/PWR	Description
7:1	RO	0h		Reserved (RSVD).
0	RO	0b	Uncore	Transactions Pending (TP): 1: The Function has issued one or more non-posted transactions that have not been completed, including non-posted transactions that a target has terminated with Retry. 0: All non-posted transactions are complete.

1.39 PMCAPID - Power Management Capabilities ID

B/D/F/Type:	0/2/0/PCI
Address Offset:	D0-D1h
Default Value:	A401h
Access:	RO;
Size:	16 bits

This register contains the PCI Power Management Capability ID and the next capability pointer.

Bit	Access	Default Value	RST/PWR	Description
15:8	RO	A4h	Uncore	Next Capability Pointer (NEXT_PTR): This field points to the next item in the capabilities list.
7:0	RO	01h	Uncore	Capability Identifier (CAP_ID): SIG defines this ID, 01h for power management.

1.40 PMCAP - Power Management Capabilities

B/D/F/Type: 0/2/0/PCI

Address Offset: D2-D3h

Default Value: 0022h

Access: RO;

Size: 16 bits

BIOS Optimal Default: 0h

This register provides information on the capabilities of functions related to power management.

Bit	Access	Default Value	RST/PWR	Description
15:11	RO	00h	Uncore	PME Support (PMES): This field indicates the power states in which the IGD may assert PME#. It is hardwired to 0 to indicate that the IGD does not assert the PME# signal.
10	RO	0b	Uncore	D2 Support (D2): The D2 power management state is not supported. This bit is hardwired to 0.
9	RO	0b	Uncore	D1 Support (D1): The D1 power management state is not supported. This bit is hardwired to 0.
8:6	RO	0h		Reserved (RSVD).
5	RO	1b	Uncore	Device Specific Initialization (DSI): This bit is hardwired to 1 to indicate that special initialization of the IGD is required before a generic class device driver uses it.
4	RO	0h		Reserved (RSVD).
3	RO	0b	Uncore	PME Clock (PMECLK): Hardwired to 0 to indicate that IGD does not support PME# generation.
2:0	RO	010b	Uncore	Version (VER): Hardwired to 010b to indicate that four bytes of power management registers are implemented and that this device complies with revision 1.1 of the PCI Power Management Interface Specification.

1.41 PMCS - Power Management Control/Status

B/D/F/Type: 0/2/0/PCI

Address Offset: D4-D5h

Default Value: 0000h

Access: RO; RW;

Size: 16 bits

BIOS Optimal Default: 00h

Bit	Access	Default Value	RST/PWR	Description
15	RO	0b	Uncore	PME Status (PMESTS): This bit is 0 to indicate that IGD does not support PME# generation from D3 (cold).
14:13	RO	00b	Uncore	Data Scale (DSCALE): The IGD does not support data register. This field always returns 00b when read; writes have no effect.
12:9	RO	0h	Uncore	Data Select (DSEL): The IGD does not support data register. This field always returns 0h when read; writes have no effect.
8	RO	0b	Uncore	PME Enable (PME_EN): This bit is 0 to indicate that PME# assertion from D3 (cold) is disabled.
7:2	RO	0h		Reserved (RSVD).
1:0	RW	00b	FLR, Uncore	Power State (PWRSTAT): This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operations must complete normally on the bus but the data is discarded and no state change occurs. On a transition from D3 to D0 the graphics controller is optionally reset to initial values. Behavior of the graphics controller in supported states is detailed in the BSpec power management section. Bits [1:0] Power state: 00b: D0 Default 01b: D1 Not Supported 10b: D2 Not Supported 11b: D3

1.42 SWSMI - Software SMI

B/D/F/Type:	0/2/0/PCI
Address Offset:	E0-E1h
Default Value:	0000h
Access:	RW;
Size:	16 bits

Bit	Access	Default Value	RST/PWR	Description
15:8	RW	00h	Uncore	Software Scratch Bits (SWSB).
7:1	RW	00h	Uncore	Software Flag (SWF): Indicates caller and SMI function desired, as well as return result.
0	RW	0b	Uncore	GMCH Software SMI Event (GSSMIE): When 1 this bit triggers an SMI. Software must write 0 to clear this bit. SMI is triggered only if SWSCI[SMISCISEL] is set to select SMI.

1.43 GSE - Graphics System Event

B/D/F/Type:	0/2/0/PCI
Address Offset:	E4-E7h
Default Value:	00000000h
Access:	RW;
Size:	32 bits

This register can be accessed by either Byte, Word, or Dword PCI config cycles. Writing this register causes the Graphics System Event (Display Interrupt) if enabled.

Bit	Access	Default Value	RST/PWR	Description
31:24	RW	00h	Uncore	GSE Scratch Trigger 3 (GSE3): When written, this scratch byte triggers an interrupt when GSE is enabled in the display register and the Display B Event is enabled in IER and unmasked in IMR etc. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
23:16	RW	00h	Uncore	GSE Scratch Trigger 2 (GSE2): When written, this scratch byte triggers an interrupt when GSE is enabled in the isplay register and the Display B Event is enabled in IER and unmasked in IMR etc. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
15:8	RW	00h	Uncore	GSE Scratch Trigger 1 (GSE1): When written, this scratch byte triggers an interrupt when GSE is enabled in the

Bit	Access	Default Value	RST/PWR	Description
				display register and the Display B Event is enabled in IER and unmasked in IMR etc. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
7:0	RW	00h	Uncore	GSE Scratch Trigger 0 (GSE0): When written, this scratch byte triggers an interrupt when GSE is enabled in the display register and the Display B Event is enabled in IER and unmasked in IMR etc. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.

1.44 SWSCI - Software SCI

B/D/F/Type:	0/2/0/PCI
Address Offset:	E8-E9h
Default Value:	0000h
Access:	RW-O; RW;
Size:	16 bits

This register serves 2 purposes:
1. Support selection of SMI or SCI event source (SMISCISEL - bit15).
2. SCI Event trigger (GSSCIE - bit 0).
To generate a software SCI event, software (System BIOS/Graphics driver) should program bit 15 (SMISCISEL) to 1. This is typically programmed once (assuming SMIs are never triggered). On a 0 to 1 subsequent transition in bit 0 of this register (caused by a software write operation), the CPU sends a single SCI message down the DMI link to PCH. PCH then sets the DMISCI bit in its TCO1_STS register and the TCOSCI_STS bit in its GPE0 register on receiving this message from DMI. The corresponding SCI event handler in the BIOS must be defined as an _Lxx method, indicating level trigger to the operating system.

Once written as 1, software must write 0 to this bit to clear it, and all other write transitions (1->0, 0->0, 1->1) or if bit 15 is 0 do not cause the CPU to send an SCI message to the DMI link.

To generate a software SMI event, software should program bit 15 to 0 and trigger SMI via writes to the SWSMI register (See the SWSMI register for programming details).

Bit	Access	Default Value	RST/PWR	Description
15	RW-O	0b	Uncore	SMI or SCI event select (SMISCISEL): 0 = SMI (default) 1 = SCI If the selected event source is SMI, SMI trigger and associated scratch bits accesses are performed via the SWSMI register at offset E0h. If the SCI event source is selected, the rest of the bits in this register provide SCI trigger capability and associated SW scratch pad area.
14:1	RW	00000000000000b	Uncore	Software scratch bits (SCISB): Software scratch bits (read/write bits not used by hardware).

Bit	Access	Default Value	RST/PWR	Description
0	RW	0b	Uncore	Software SCI Event (GSSCIE): If the SCI event is selected (SMISCISEL = 1), on a 0 to 1 transition of the GSSCIE bit, a SCI message is sent via DMI link to ICH to cause the TCOSCI_STS bit in its GPE0 register to be set to 1. Software must write a 0 to clear this bit.

1.45 ASLS - ASL Storage

B/D/F/Type:	0/2/0/PCI
Address Offset:	FC-FFh
Default Value:	00000000h
Access:	RW;
Size:	32 bits

This software scratch register only needs to be read/write accessible. The exact bit register usage must be worked out in common between System BIOS and driver software, but storage for switching/indicating up to six devices is possible with this amount.

For each device, the ASL control method requires two bits for _DOD (BIOS detectable yes or no, VGA/NonVGA), one bit for _DGS (enable/disable requested), and two bits for _DCS (enabled now/disabled now, connected or not).

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00000000h	Uncore	Device Switching Storage (DSS): Software controlled usage to support device switching.

Revision History

Revision Number	Description	Revision Date
1.0	First 2012 OpenSource edition	May 2012

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