Intel® Iris® Plus Graphics and UHD Graphics Open Source

Programmer's Reference Manual

For the 2019 10th Generation Intel Core™ Processors based on the "Ice Lake" Platform

Volume 14: Workarounds

January 2020, Revision 1.0

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Workarounds

Release	Gen11-GT_ICLLP
Impact	hang
Lineage	220166154
Title	[GEN11LP] VTd issue: concurrent IOTLB invalidation & Context Cache invalidation results in missing ack
Bspec_wa_details	On a IOTLB invalidation HW also does a Context Entry invalidation (unnecessarily). If a Context Cache Inv is also received at the same time. HW does not give the Acks correctly. WA: Disable Context entry invalidation on IOTLB invalidation request. 4080 [7] = 1 Enables Pre Gen11 Behaviors (IOTLB will not invalidate Context and function).
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	data_corruption
Lineage	220579888
Title	3DSTATE_3D_MODE is not implementing modify enables correctly
Bspec_wa_details	The mask bits are not implemented properly on 3DSTATE_3D_MODE. Driver must always program bits 31:16 of DW1 a value of 0xFFFF. This means if it is only updating 1 field, it must update all the fields to the correct value.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	data_corruption
Lineage	220856683
Title	Clone from gen10lp: Input Coverage = INNER is incorrectly ANDing sample masks
Bspec_wa_details	Starting in CNL, while designing CPS and depth coverage mode for input coverage for conservative rasterization implementation changed. Especially input coverage mode = INNER started ANDing sample mask to conservative rast mask. This results in the mis-match wrt to the spec. WA for ICL is to have PS compiler logically OR input coverage mask to infer if a pixel is fully covered when INPUT_COVERAGE_MASK_MODE = INNER
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-Display_ICL
Impact	data_corruption
Lineage	220884772
Title	Incorrect plane CSC coefficients for sRGB to Bt2020
Bspec_wa_details	SDR planes PLANE_COLOR_CTL Plane CSC Mode 100b, RGB709 to RGB2020, uses hardcoded R-Y coefficient of 0.75 instead of 0.625, resulting in incorrect BT2020 color conversion. WA: Limit RGB709 to RGB2020 conversion to the HDR capable planes.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	data_corruption
Lineage	1207137018
Title	3D Tiled-YF surface corruption in MIP tail LODs because of X-adjacent RCC cacheline composition
Bspec_wa_details	RCC cacheline is composed of X-adjacent 64B fragments instead of memory adjacent. This causes a single 128B cacheline to straddle multiple LODs inside the Tile-YF MIPtail for 3D surfaces (beyond a certain slot number) , leading to corruption when CCS is enabled for these LODs and RT is later bound as texture. WA: If RENDER_SURFACE_STATE.Surface Type = 3D and RENDER_SURFACE_STATE.Auxiliary Surface Mode != AUX_NONE and RENDER_SURFACE_STATE.Tiled ResourceMode is Tile-YF or Tile-YS, Set the value of RENDER_SURFACE_STATE.Mip Tail Start LOD to a mip that larger than those present in the surface (i.e. 15)
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-Display_ICL
Impact	data_corruption
Lineage	1209455881
Title	Gunit reporting FLR completion before receiving FLR exit message from GT
Bspec_wa_details	BIOS Write GTTMMADR offset x10_1014 bit 13 = 1
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	hang
Lineage	1209644611
Title	Blitter restriction - hang if fast copy engine used with certain small/odd sizes; fall back to legacy blitter for these
Bspec_wa_details	WaName: DisallowOddSizedSmallFCBlits FC Blitter cannot handle a blit whose y-height%4 == 3 and y-height <= 8. This causes a system hang. WA: These blits must be detected and sent to the legacy blitter engine, not the fast copy engine.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	hang
Lineage	1305657336
Title	OVR Issue where initialize that follows the restart is not deferred causing an invalid page to be allotted for storing the tokens
Bspec_wa_details	OVR Issue if pocs_ovr_restart is asserted within 256 clks after the ctx restore is done. WA: The WA could be to do a page pool size mmio write with a value of 0 followed by 256 noops before any page pool restart.
Sku	ALL
Stepping_impacted	B0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-Display_ICLLP
Impact	data_corruption
Lineage	1405510057
Title	ICL: HDMI 10bpc w/ YUV420 will fail with resolutions that have a remainder of 2 when divided by 8
Bspec_wa_details	Do not enable YUV420 10bpc with HDMI with horizontal blank size mod 8 remainder is 2. Use cases covered: 720x480@60/120/240 with Hblank 138, 1280x720@60/120 with Hblank 370, 2560x1080@100 with Hblank 410.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-Display_ICLLP
Impact	data_corruption
Lineage	1405528356
Title	Display underrun with VRR and transcoder port sync.
Bspec_wa_details	Display underrun with VRR and transcoder port sync. WA: When using VRR, TRANS_VRR_CTL Pipeline Full Override must be set to Programmed Pipeline Full Line Count and the FrameStart to Pipeline Full LineCount must be configured.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-Display_ICLLP
Impact	
Lineage	1405529773
Title	HDMI symbol mismatch with 10bpc and 4x pixel repeat
Bspec_wa_details	WA: Do not enable HDMI with 10bpc and pixel repeat 4x.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	data_corruption, performance
Lineage	1405543622
Title	Incorrect default GAPZ arbiter register value.
Bspec_wa_details	Register B004 bits [27:22] select the priority of arbitration among RCZ, STC and HiZ in the GAPZ. The priority requested by the Z team is RR(RCZ, STC) < HiZ. However, the default value of this register puts the priority scheme at RCA < STC < HiZ which has been seen to reduce performance in some cases. WA : During driver boot, reprogram the value of this register to '111111b.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	A0
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	data_corruption
Lineage	1405586840
Title	[GEN11-LP] : MCR Unit: MCR unit to allow the read to go to disabled banks during a multicast request by CS to L3 Banks
Bspec_wa_details	In the case of a configuration where L3 banks are disabled, reads to L3 bank registers may return zeros instead of the value of the register. The HW does not direct the read based on the banks being disabled. SW must maintain a copy externally to track the value in the case a read/modify write is needed.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-Display_ICLLP
Impact	data_corruption
Lineage	1405595945
Title	Gen11 Add alpha blending source pixel bypass and destination bypass for plane alpha blending
Bspec_wa_details	Display workaround #1153: Alpha blending with alpha=00 or FF still passes through the alpha math and rounding logic, causing small differences compared to a fully transparent or opaque plane, which can create a visible transition at the edge of the plane in some situations. For per-pixel alpha, set bit 7=1 in 0x70038 (pipe A), 0x71038 (pipe B), 0x72038 (pipe C) to enable hardware to bypass the alpha math and rounding for per-pixel values 00 and FF. This register is double-buffered. These bits can remain set. For plane alpha (AKA constant alpha), disable plane alpha if the plane alpha value would be set to FF, and disable the plane if the plane alpha value would be set to 00.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	A0
Sku_impact	driver_permanent_wa

Release	Gen11-Display_ICLLP
Impact	hang
Lineage	1405638134
Title	VRR disables incorrectly when using MaxShift with HW Pipeline full
Bspec_wa_details	WA: When using VRR, TRANS_VRR_CTL Pipeline Full Override must be set to Programmed Pipeline Full Line Count and the FrameStart to Pipeline Full LineCount must be configured.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-Display_ICLLP
Impact	data_corruption
Lineage	1405642065
Title	Dev2 seq doesn't clear GT_RELOAD_FLUSH.BCLD_REQ which prevents 2nd MCHECK req
Bspec_wa_details	Issue: Device 2 sequencer does not clear GT_Reload_Flush.BCLD_Req bit which prevents supporting a 2nd MCHECK PRMRR flow. The result is microcode MCHECK flows will hang if attempted a 2nd time. WA: BIOS writes GTTMMADR offset x10_1014 bit 13 = 1 to disable DGR clock gating.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	data_corruption
Lineage	1405733216
Title	Coherency issue due to speculative fill & WBS2I
Bspec_wa_details	For speculative fills, L3 will leave line in S state without actually having ownership. If this line is Evicted while ownership flow is in progress, LLC CV bit may get cleared while GT L3 has ownership, which is an IDI protocol violation. WA : Disable Clean Evict by setting LSQCREG4[6] to 1.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-Display_ICLLP
Impact	data_corruption
Lineage	1405739292
Title	Display underrun with NV12 pixel format and VRR with hardware pipeline fill mode
Bspec_wa_details	Display underrun with NV12 pixel format and VRR with hardware pipeline fill mode. WA: When using VRR, TRANS_VRR_CTL Pipeline Full Override must be set to Programmed Pipeline Full Line Count and the FrameStart to Pipeline Full LineCount must be configured.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	data_corruption
Lineage	1405766107
Title	Insufficient storage in LNIunit for state requests results in loss of state request packets
Bspec_wa_details	CL2/SF state requests do not use credit based transfer and assume storage in LNI and SARB up to ROB depth. ROB depth changed midway without increasing this storage leading to loss of requests. WA : Program CL2, SF MAX allocation in the ROB to be max/2. 0xB43C[9] and 0xB43C[7] need to be set to '1
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-Display_ICLLP
Impact	
Lineage	1404523923
Title	Power optimization in display engine: Enable dynamic clock gating of PSF clock
Bspec_wa_details	Power optimization: HW default is for display engine to request the IOSF P clk even when display is idle. As a power optimization, trunk level clock gating can be enabled when display is idle. BIOS should opt in to dynamic clock gating/clock request via write to 0x101038h bit 1 = 1 .
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-Display_ICLLP
Impact	
Lineage	1405824203
Title	IR FSM can get stuck in cache lookup state forever
Bspec_wa_details	BIOS to write IOMMU_DEFEATURE_MISCDIS2 GTTMMADR offset x10_105C bit 23 == 1 This disables the interrupt entry cache in the IOMMU (MISC2DIS.IECDIS). IR FSM can get stuck in cache lookup state forever (hang).
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-Display_ICLLP
Impact	data_corruption
Lineage	1405871822
Title	Audio - GTC values not added to C-bits for pipe B or C if pipe A is not also used
Bspec_wa_details	Have pipeA always enabled when we want Audio GTC + DPMST. We cannot support Audio GTC + DPMST feature when pipeA is disabled.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	B0
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	
Lineage	1406206320
Title	PreemptToIdle being reported with ActiveToIdle bit set in CSB
Bspec_wa_details	SW can ignore ActiveToIdle bit when PreemptToIdle is indicated
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	hang
Lineage	1406306137
Title	Back-to-back send messages from threads on an EU where one of the requests is atomic cycle can result in cycles getting lost/corrupted
Bspec_wa_details	WaAtomicDisable Setting Atomic Control on SEND instruction does not guarantee back-to-back SEND messages. WA: Disable Pick 2nd EU optimization when using Atomic Control on SEND instruction (E48C[7]).
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-Display_ICLLP
Impact	
Lineage	1406434580
Title	Display trunk level clock gating: must program non-zero hysteresis when enabling
Bspec_wa_details	WaName: WABiosCLKReqHysterisis. WA: When BIOS enables aggressive clock gating via DG_CLKREQ_POLICY (x10_1038) MEM_UP_OVRD bit (bit 1) to 1, first set the hysteresis counter CLKREQ_HYST_CNTR (bits 23:16} to 8'b0000_0100.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-Display_ICLLP
Impact	Data_corruption
Lineage	1406463849
Title	Pipe CSC registers are getting disarmed on reads
Bspec_wa_details	Pipe CSC register updates not taking effect as expected. WA Sequence to arm/disarm Pipe CSC registers: Step A: Wait for start of Vblank or safe region before start of Vblank. Step B: Write the CSC registers, CSC_COEFF*, CSC_PREOFF*, and CSC_POSTOFF* with programming set A. Step C: Arm the CSC registers by writing to CSC_MODE register. Step D: Once the registers are armed, do not read the CSC registers, CSC_COEFF*, CSC_PREOFF*, CSC_POSTOFF* until after the next start of Vblank, since reads at this point will disarm the registers and set A programming would not take effect. Step E: Wait for next start of Vblank. Set A programming takes effect here if no reads or writes have occurred since arming. Step F: Reads of the CSC registers can occur here, even though the registers are disarmed, Set A programming is retained. Note: If the CSC registers are not read back, then no adjustment to programming is needed. If the CSC registers, CSC_COEFF*, CSC_PREOFF*, CSC_POSTOFF* are written to with new programming set B, between step C. and step E, then set B will take effect on step E Vblank.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	Data_corruption
Lineage	220818474
Title	Incorrect blue channel value when sampling from R32G32_FLOAT surface with border texture addressing mode
Bspec_wa_details	Issue: When sampling from an R32G32_FLOAT surface with border texture addressing mode, there is an issue where the blue channel value is missing. WA: Set the shader channel select to 1.0 (instead of 0) for the missing blue channel.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	
Lineage	2201039848
Title	Mid thread preemption hangs with sends instruction in case where src/dest overlap on the GRF registers touched/scoreboard
Bspec_wa_details	When src and dest overlap in non-pagefault cases for sends instruction, we must use NoPreempt. (New restriction needed in BSPEC).
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	
Lineage	1406614636
Title	Use {NoPreempt} when r2 is used as src0 of sends in regular kernel.
Bspec_wa_details	Use of {NoPremept} switch is required whenever r2 is used as src0 for sends instruction. This is to reserve use of r2 for SIP during context save and restore.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	
Lineage	1406680159
Title	Gateway clock gating Issue on EOT & Barrier Ram Valid
Bspec_wa_details	Disable GWL clock gating. Set bit16 for register 0x9524 to 1
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	
Lineage	1406689936
Title	POSH/PTBR workloads can hang if varying tile counts within a tile pass and preemption happens
Bspec_wa_details	WA Name: PoshPreemptionTilePassInfoCmd "Tile Count" value programmed must be same in the 3DSTATE_PTBR_TILE_PASS_INFO command programmed for "Start of Tile Pass" and "End of Tile Pass".
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	
Lineage	1406697149
Title	Default value of the control bit that controls the dropping out put to the client Data return from Bank is Incorrect.
Bspec_wa_details	WA Name: WADisableBankHangMode The L3 error detection can be programmed to hang the GPU on a non-recoverable error due to ECC. The default value of the register currently enables the hang mode which is not desirable. So, a register programming is necessary to disable the hang mode. Kernel driver • Program 0x7034[9] to 'b1 This can be done in the "golden context" image for OS's that use such a construct or programmed into the context image by the kernel driver on a per-context basis at context create time.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	
Lineage	1406756463
Title	Sampler chicken bit 0xe190[0] to disable DFR doesn't work properly
Bspec_wa_details	E190[0] must not be set to disable DFR. If DFR needs to be disabled for any reason, it should be done by programming bit 9 of the Subslice DFR_DFRENRATIO MMIO register (0x9550).
Sku	ALL
Stepping_impacted	A2
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	
Lineage	1406796446
Title	ICLLP FF DOP clock gating causes deref from TDL to be lost in SBE
Bspec_wa_details	WA Name: WAFFDOPPOSHderef Maintained rc_psmi_ctrl reg bit 15/12/7 values in memory per ctx and use per ctx WABB so that CS loads these values from memory every time is submitted(MI_LOAD_REGISTER_MEM). These bits will not impact other power entry point. For POSH enable ctx always set these bits at start. To set the bits an MMIO write to rc_psmi_ctrl(0x2050) of data 0x90809080 is required.
Sku	ALL
Stepping_impacted	C0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-Display_ICLLP
Impact	
Lineage	1406869607
Title	Display pipe_flipcnt_a/b/c showing wrong values
Bspec_wa_details	Issue: PIPE_FLIPCNT_B, PIPE_FLIPTMSTMP_B, PIPE_FLIPCNT_C, and PIPE_FLIPTMSTMP_C look at pipe A flips and not pipe B or pipe C. Workaround: Do not use the mentioned registers. If flip count or timestamp functionality is needed, it will have to be recreated in software by using flip done interrupts.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	hang
Lineage	1406950495
Title	EU Channel Enable register value not properly synchronized for access by EU hyperthread slot
Bspec_wa_details	WaName: WAChannelEnableRegister Channel enable register read is not pipelined correctly, and value obtained by accessing this register may not be the channel enable data for the currently executing EU thread, may be from another thread on that EU instead. Do not use this register.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	hang
Lineage	1406463099
Title	GAM TLBPend Internal Error seen - results in hang for workloads on GT
Bspec_wa_details	TLB miss allocation perf fix added in GEN11 is incorrectly detecting TLB hits as Hit on Miss for a corner case eventually leading to a HANG. Recommendation: Disable the TLB miss allocate stall Perf fix by setting this config bit 0x4AB8[31] to 1.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	
Lineage	1407240128
Title	Hang can occur when POSH is enabled if RCS/POCS concurrently send certain cycles
Bspec_wa_details	Below two workaround's to be Implemented by UMD and KMD respectively: 1. WorkAround UMD: WaExplictTdllNPStateAck: SW must program the following MI_LOAD_REGISTER_IMMEDIATE (LRI) sequence after every “STATE_BASE_ADDRESS” command programmed in POSH_START batch buffer. LRI :: MMIO ADD:E700h, DATA: 0x0 <<Address E700h is assumed to be non existing register and hence write to this must not cause any side affect. This to flush the Message Channel Path from POCS to TDL, ensures NP state to TDL>> LRI :: MMIO ADD: 180F0h, DATA: F000_0000 << Clears dirty flag in POCS (TDL0..3), hence POCS will not generate any more implied NP state ack on 3DPRIMTIVE or stalling flushes >> LRI :: MMIO ADD: 180F8h, DATA: F000_0000

	<< Clears dirty flag in POCS (TDL4..7), hence POCS will not generate any more implied NP state ack on 3DPRIMTIVE or stalling flushes >> Register 0x180F0 must be whitelisted by SW. 2. Work Around KMD Add the below sequence as part of the POSH Enabled Per Context WA BB. LRI :: MMIO ADD:E700h, DATA: 0x0 <<Address E700h is assumed to be non existing register and hence write to this must not cause any side affect. This to flush the Message Channel Path from POCS to TDL, ensures NP state to TDL>> LRI :: MMIO ADD: 180F0h, DATA: F000_0000 << Clears dirty flag in POCS (TDL0..3), hence POCS will not generate any more implied NP state ack on 3DPRIMTIVE or stalling flushes >> LRI :: MMIO ADD: 180F8h, DATA: F000_0000 << Clears dirty flag in POCS (TDL4..7), hence POCS will not generate any more implied NP state ack on 3DPRIMTIVE or stalling flushes >>
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	
Lineage	1407352427
Title	PSD clock gating causes WM flush done pulse to stay high
Bspec_wa_details	Disable PSD clock gating (0x94e4[5]=1)
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	Data_corruption
Lineage	1806068545
Title	Concurrent accesses to different portions of 128B "cacheline" of a 1D/linear mipmapped surface in RCC from multiple color pipes via different surface bpp descriptions can result in data corruption due to missing indication of shared state to CC in case of evict
Bspec_wa_details	For 1D/linear mip-mapped surfaces, each MIP must be accessed with the same pixel/texel format i.e. re-description of the sub-resource is not allowed.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	
Lineage	1305770284
Title	GT Hang can occur in Subslices PSD when using PTBR due to cycles getting lost due to missing back pressure when fifo full between hardware units
Bspec_wa_details	Disable color discard mechanism for PTBR by programming 0x5580[15]=0 before any tile pass.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	data_corruption, hang
Lineage	1806230709
Title	Page fault when access border color from SAMPLER_INDIRECT_STATE when POSH is enabled and dynamic base address or bindless sampler state are used.
Bspec_wa_details	if (a) the POSH VS uses sampler (flag from IGC) and (b) any sampler state bound to the VS stage has border color, then disable POSH for that Draw call.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	
Lineage	1407596294
Title	Hang can occur in OSB unit (hull shader related) due clock gating issue in certain corner cases
Bspec_wa_details	Disable the hsunit clock gating. Offset 9434 bit 8
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	
Lineage	1407685933
Title	PTBR: Hang can occur in OVR context sort flush if >128 tiles are used
Bspec_wa_details	In PTBR mode a max of 127 tiles can be used
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	
Lineage	1407925466
Title	POSH: Incorrect culling because 3DSTATE_SAMPLE_PATTERN is not restored as part of POCS CTXT Restore
Bspec_wa_details	DisableSmallTriangleCulling for MSRT in PositionCS: Chicken bit “Disable Small Triangle Culling for MSRT” (FF_SLICE_CHICKEN : 0x18088[3]) in POCS must be always set.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-Display_ICLLP
Impact	other
Lineage	1408136248
Title	Bogus ECC failures detected within the CUS after a cold-boot/low power reset
Bspec_wa_details	If checking for ECC errors from any of the CUS functions, then first clear out false ECC Single Error and ECC Double Error status bits of PLANE_CUS_CTL register after the first frame of a cold-boot/low power state. After the first frame, the ECC error reporting should be accurate.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	
Lineage	1306055483
Title	3D mid-object preemption with instancing can result in incorrect handling of InstanceId on resubmission, resulting in hang.
Bspec_wa_details	Put the Instance ID enabled element at the last of a vertex.
Sku	ALL
Stepping_impacted	C0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	
Lineage	1408615072
Title	clk gating bug in VS unit can cause UAV counters for HS, GS, TDS to result in hang
Bspec_wa_details	Disable the vsunit clock gating. Offset 9434 bit 3.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-Display_ICLLP
Impact	
Lineage	1408797083
Title	Bspec clarification for programming pixel pass through
Bspec_wa_details	Bit 23 of PIPE_MISC and bit 15 of 0x70038 (pipe A), 0x71038 (pipe B), 0x72038 (pipe C), or 0x73038 (pipe D) both need to be set for passthrough. Described in the display pipe section of bspec.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-Display_ICLLP
Impact	
Lineage	1408936778
Title	Pipe seam excess register missing double buffering
Bspec_wa_details	A full mode-set is required if the programming to PIPE_SEAM_EXCESS is changing
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	hang
Lineage	1408908852
Title	VF Bank Collision Bug with POSH + instancing - can result in hang in VF
Bspec_wa_details	So send 2 dummy 3DSTATE_VERTEX_ELEMENT in RCS whenever 3DSTATE_VF_INSTANCING[i].InstancingEnable = true for any element and the 3dprimitive is a posh enabled draw. - Also, we need to disable POSH for the draws which has more than 30 elements since we won't be able to add these 2 dummy elements in that case.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-Display_ICLLP
Impact	data_corruption
Lineage	1408961008
Title	Underrun seen with package C states when LP WM1-7 disabled
Bspec_wa_details	If PLANE_WM1 is not enabled, copy the contents of PLANE_WM0[30:0] into PLANE_WM1[30:0] when configuring watermarks. Needs to be done by GOP/VBIOS/EFI in driverless systems.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	
Lineage	1408413580
Title	Hardware hang on concurrent media compressed read + atomic fence
Bspec_wa_details	Work around is to disable MMCD. 0c4DDC[30] = 1'b1 (disable MMCD)
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-Display_ICLLP
Impact	data_corruption
Lineage	1409120013
Title	Underrun when FBC is compressing with odd plane size and first segment is only 3 lines
Bspec_wa_details	FBC causes screen corruption when plane size is odd for vertical and horizontal. Set 0x43224 bit 14 to 1 before enabling FBC. It is okay to leave it set when FBC is disabled.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-Display_ICLLP
Impact	power
Lineage	1409216368
Title	Package C2 increase when VRR is enabled with push mode
Bspec_wa_details	Package C2 increase when VRR is enabled with push mode. When enabling VRR, before setting TRANS_VRR_CTL VRR Enable, program GT-driver Pcode mailbox with command 0x11 and data low bit 0 = 1 to inform pcode that VRR is enabled. When disabling VRR, after clearing TRANS_VRR_CTL VRR Enable, program GT-driver Pcode mailbox with command 0x11 and data low bit 0 = 0 to inform pcode that VRR is disabled.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	
Lineage	1807004938
Title	Hang in EU due to instruction cache due to concurrent flush + in-flight miss.
Bspec_wa_details	Driver must ensure that a instruction cache invalidate cannot occur in parallel with EU execution. Below are the cases which this behavior could happen: 1) Mid-thread preemption and POSH context enabled in parallel for a workload 2) PIPE_CONTROL with Instruction Cache Invalidate Enable bit set without any prior PIPE_CONTROL with CS stall 3) STATE_BASE_ADDRESS or PIPE_CONTROL with Instruction Cache Invalidate Enable executed in render pipe while POSH shaders are active. 4) STATE_BASE_ADDRESS or PIPE_CONTROL with Instruction Cache Invalidate Enable executed in posh pipe while render shaders are active. Possible WA's: 1) Disable POSH and Flush prior to all PIPE_CONTROL with Instruction Cache Invalidation Enable 2) Disable MTP, Sync STATE_BASE_ADDRESS and PIPE_CONTROL with Instruction Cache Invalidation Enable between POSH and Render and Flush prior to all PIPE_CONTROL with Instruction Cache Invalidation Enable.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	
Lineage	1408767742
Title	Corruption seen for some tesselation workloads when TEDOP clk gating enabled
Bspec_wa_details	WA : mmio_write offset 20a0 value 00080000
Sku	ALL
Stepping_impacted	A2
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	hang
Lineage	1409178092
Title	3-strike Machine check when with full GT/IA coherency enabled and partial write merge enabled
Bspec_wa_details	To avoid hangs/crashes when using hardware-based fine grain coherency, 0xB140[19] - Coherent Partial Write Merge Enable must be set to 0. This applies to all ICL products which support coherency, so Lakefield is not affected.
Sku	ALL
Stepping_impacted	A2
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	
Lineage	1409273501
Title	Depth buffer corruption when state cache invalidate is triggered from POC
Bspec_wa_details	1) Insert PIPE_CONTROL with CS_stall prior to any PIPE_CONTROL with Read Only State Invalidate if engine is still active 2) Workaround Below. Note that the WA can be changed such that RCS can invalidate when POCS is active. enum ePipeSync { eBusy = 0, eIdle = 1, eNeedsSync = 2 }; ePipeSync poshStatus, rcsStatus; The POCS and RCS command buffers write to their semaphore location to indicate their status to the other pipeline. The Idle is updated after any PipeControl with CS Stall as a Post-Sync operation, the Busy is written before any following commands (state or rendering) – but must check whether the other pipeline needs a sync first. i.e. // Do not start state or rendering operations while the other pipeline is invalidating caches Mutex { SemaphoreWait(OtherPipeline < eNeedsSync); // Lock out the other pipeline from invalidating caches StoreDataImmediate(eBusy); } // State and rendering commands // When the pipeline goes idle PipeControl(CSStall, PostSync Write eIdle); // Pipeline is idle – allow the other pipeline to do any required cache invalidates When an SBA (or Cache Invalidate is needed), the following commands are inserted. // Flush this pipeline, in case both pipelines need to synchronize PipeControl(CSStall, PostSync Write eIdle); // (this might not be needed) // Request the other pipeline waits Mutex { PipeControl(CSStall, Post Sync Write eNeedsSync); } // Wait until the other pipeline acknowledges that it has halted. SemaphoreWait(OtherPipeline >= eIdle); SBA or PipeControl with Cache Invalidate // Remove the request for the other pipeline to wait StoreDataImmediate(eIdle); option use PipeControl(CSStall, PostSyncWrite eIdle); instead – but shouldn't be needed This approach allows both pipelines to invalidate the caches at the same time, so avoids the deadlock scenario. It assumes that we will eventually be doing a CSStall to inject the idle signal, but it can also be injected occasionally (using a predicate as follows) in the middle of rendering operations if we do not have sufficient naturally occurring pipeline flushes. Provided there are enough opportunities for the pipeline to complete the handshake without fully draining, we should avoid the cold restart costs. Potential performance enhancement (if needed) – however ending the Tile Pass requires a pipe flush as Tile Pass Info is NP state. Predicate (if OtherPipeline == eNeedsSync) // Use Predicated BBS to skip { // Flush and indicate that this pipeline is idle PipeControl(CSStall, PostSyncWrite eIdle); Mutex { // Wait for the other pipeline to complete its operation SemaphoreWait(OtherPipeline, < eNeedsSync); // Resume operations StoreDataImmediate(eBusy); } } Before starting any other semaphore, the pipeline must be flushed, and the state set to

	eIdle. Mutex Option 1 (using MI_PREDICATE) A initialized to the value 0 Start Mutex PREDICATE Never SEMA_WAIT (A == 0) ATOMIC Increment A, Read Return -> GPR4 REG2REG GPR4 -> Predicate result PREDICATE Clear (Pred Result[0] = 0) (values are 1 or 2) ATOMIC Decrement A BBS <Start Mutex> PREDICATE Never Got Mutex <BLOCK> End Mutex ATOMIC Decrement A Mutex Option 2 (using Predicated Batch Buffers) <= Preferred A initialized to the value 1 Start Mutex PREDICATE Never SEMA_WAIT (A == 1) ATOMIC Increment A, Read Return -> GPR4 REG2REG GPR4 -> PREDRESULT_1 BBS Predicate Enable (Got Mutex) ATOMIC Decrement A LRI PREDRESULT_1, 1 (for the benefit of GTX) BBS <Start Mutex> (Predicate Enable – for the benefit of GTX) Got Mutex <BLOCK> End Mutex ATOMIC Decrement A
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	
Lineage	1306463417
Title	Hang seen in hull shader unit enabled on some workloads in boundary case
Bspec_wa_details	Resubmit 3D State HS for every draw call containing Hull Shader.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-Display_ICLLP
Impact	data_corruption
Lineage	1409689360
Title	Corruption with FBC and plane enable/disable
Bspec_wa_details	Corruption with FBC around plane 1A enabling. In the Frame Buffer Compression programming sequence "Display Plane Enabling with FBC" add a wait for vblank between plane enabling step 1 and FBC enabling step 2.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	
Lineage	1805992985
Title	End of Thread (EOT) fifo overflow can happen if many DS threads are retiring at same time
Bspec_wa_details	The send cycle, which is a urb write with an eot must be 4 phases long and all 8 lanes must valid.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	data_corruption
Lineage	1506855762
Title	OVR causes a Page fault when running out of free pages in PTBR PAGE POOL
Bspec_wa_details	The driver has to map 1 page of dummy resource to address PTBR_PAGE_POOL_BASE_ADDRESS + (0xFFFF * 4KB).
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	performance
Lineage	1604223664
Title	HW default value for L3 bank hashing is not optimal for performance
Bspec_wa_details	WaL3BankAddressHashing Register B004 bit[6:0] is used for HASH Control for Address Bit Exclusion, the default value causes reduced performance. Software should program to to b'0000001. Register B404 bit[11:5] are Bank Hash Address Exclude Bits, the default value causes reduced performance. Software should program to to b'0000010.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	
Lineage	1604278689
Title	Issue with FBC Modify/Clear message generated on GEN11 with color cached in L3 (tile cache or data cache) in PTBR mode.
Bspec_wa_details	Work Around for Blitter Engine: "Blitter Tracking with Nuke" is the only FBC functional mode supported by blitter engine. SW must always program the "PPGTT Render Target Base Address Valid for FBC" to value ‘0’ in BCS_ECOSKPD register. This would disable blitter engine from generating modify messages to FBC unit in display. If using Front Buffer rendering via BLT and display FBC compression feature is enabled, software must follow the BLT command that target the front buffer with the following: • Flush • LRI to 0x50380 with data 0x0000_0004 (This causes FBC to recompress the entire buffer after BLT operation). Workaround for Render Engine: "Render Tracking with Nuke" is the only FBC functional mode supported by render engine. SW must always program the FBC_RT_BASE_ADDR_REGISTER_* register in Render Engine to a reserved value (0xFFFF_FFFF) such that the programmed value doesn’t match the render target surface address programmed. This would disable render engine from generating modify messages to FBC unit in display. Refer "Frame Buffer Compression" section for more details related to FBC functionality and programming.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	
Lineage	1604302699
Title	Coherent L3 & LLC cacheable full $Line writes with I2MWr mode enabled have poor performance
Bspec_wa_details	Enabling I2MWR for Gen11 causes a drop in coherent write performance due to a bug. WA is to disable I2MWR by setting bit 0xB114 bit 28 = 1.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-Display_ICLLP
Impact	other
Lineage	1604303684
Title	PAL_PREC_MULTI_SEG_INDEX and PRE_CSC_GAMC_INDEX register readback incorrect index value in auto increment mode
Bspec_wa_details	PAL_PREC_MULTI_SEG_INDEX Index Value and PRE_CSC_GAMC_INDEX Value does not readback the current index value when using auto increment mode. If index value is required, use the no increment mode or count the increments. Data register is not impacted.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-Display_ICLLP
Impact	
Lineage	1604331009
Title	Display underrun in HDR mode when cursor is enabled
Bspec_wa_details	Display underrun in HDR mode when cursor is enabled. Before any of the following are enabled (CUR_CTL[18], CUR_CTL[16] or CUR_COLOR_CTL[15]), disable the cursor clock gating. WA: Disable cursor clock gating in HDR mode. Program 0x46520 bit 28 = 1 (Pipe A), Program 0x46524 bit 28 = 1 (Pipe B), Program 0x46528 bit 28 = 1 (Pipe C)
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	data_corruption
Lineage	1604402567
Title	VFURB dropping data in some scenarios involving *_256 /*_64 format
Bspec_wa_details	WA Name: WaNo256BitVFCompPacking Component packing of vertex elements associated with 256-bit surface formats is not supported due to a HW bug. WA: All components of vertex elements associated with 256-bit surface formats MUST be enabled.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	hang
Lineage	1604578095
Title	HS Hang & TDG mismatches when dual_instance_enable is zero AND HS is handle limited.
Bspec_wa_details	WA Name: WAHSMaxthread Hang occurs when the number of max threads is less than 2 times the number of instance count. The number of max threads must be more than 2 times the number of instance count.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	hang
Lineage	1605330949
Title	Semaphore_wait with register poll command incorrectly returns value from NOPID on 2nd and later iterations of poll
Bspec_wa_details	When checking for register read access on Semaphore register poll command executed from non-privileged batch buffer, the command streamer correctly checks both the HW white list and the FORCE_TO_NONPRIV white list. However, if the poll is not satisfied on first iteration and has to execute a second time (or more), the access checking logic only looks at the FORCE_TO_NONPRIV list. Offsets which are in the HW white list but not in the FORCE_TO_NONPRIV list will incorrectly get shunted to the NOPID register in that case.. Workaround: For Semaphore Register Poll, SW must use the FORCE_PRIV_TO_NONPRIV to explicitly whitelist read access to the register, even for registers that are supposed to be readable from non-privileged batch.
Sku	ALL
Stepping_impacted	C0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	
Lineage	1606682166
Title	[ICL-LP]Incorrect TDL's SSP address shift in SARB for 16:6 & 18:8 modes
Bspec_wa_details	Disable the Sampler state prefetch functionality in the SARB by programming 0xB000[30] to '1'. This is to be done at boot time and the feature must remain disabled permanently.
Sku	ALL
Stepping_impacted	C0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	
Lineage	1607087056
Title	ICL-LP LNI completion clock gating issue
Bspec_wa_details	Disable L3 clock gating by setting bit 16 & 17 of register at offset 0x94d4
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	
Lineage	1805811773
Title	Draw with depth test disable/stencil test enabled and with pixel location outside of bound stencil buffer but within viewport leads to page faults or incorrect data
Bspec_wa_details	If stencil test is enabled and depth test is not enabled , ensure the clipping/draw rectangle dimensions are clamped to the size of the stencil buffer boundaries.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-Display_ICLLP
Impact	
Lineage	2006604312
Title	Plane/pipe scaler clock gating issue
Bspec_wa_details	If Plane or Pipe scaling is being performed then SW should disable the clock gating to the Scaler's register block. Set bit 8 of 0x46520 (pipe A), 0x46524 (pipe B), or 0x46258 (pipe C).
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-Display_ICLLP
Impact	data_corruption
Lineage	2006605046
Title	Transcoder WD tail pointer scan line count corrupted after fault
Bspec_wa_details	On receiving a fault, turn WD transcoder off and then back on again before starting another capture.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-Media_ICLLP
Impact	hang
Lineage	2006607890
Title	VCS hang after HuC Authentication fails
Bspec_wa_details	VCS hangs after HuC Authentication fails for Huc workload. Hucmx does not drop the Huc-Streamout command causing hang. SW workaround is to assert media reset for such case
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-Display_ICLLP
Impact	
Lineage	2006613073
Title	VRR port sync mode - Flips in Slave Pipe are not serviced in sync with master pipe
Bspec_wa_details	Program 0x4208C bit 17 = 1b when DisplayPort VRR port sync mode is used. Set the bit to 0b for VRR usage without port sync.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-Display_ICLLP
Impact	other
Lineage	2201998765
Title	PCH GMBUS i2c DDC clk first cycle fails HDMI compliance check >100khz
Bspec_wa_details	GMBUS DDC first cycle slightly exceeding HDMI spec limit of 100 KHz. WA: Adjust the clock divider to give more margin. Use the updated values found in RAWCLK_FREQ Microsecond Counter Divider.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	
Lineage	2202389218
Title	Invalid occlusion query results with "Pixel Shader Does not write to RT" bit
Bspec_wa_details	When Pixel Shader Kills Pixel is set, SW must perform a dummy render target write from the shader and not set this bit, so that Occlusion Query is correct.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-Media_ICLLP
Impact	hang
Lineage	2205427594
Title	ICL LP: Media compression issue: Issue during Macroblock processing during error concealment can result in page faults/engine soft hang
Bspec_wa_details	For all scenarios, use the first valid reference (or the closest reference if POC is available to detect) from reference list if available to fill all unused reference frame address regardless coding type (I, P or B) to prevent potential page fault. If valid reference is not available from reference list, use output surface for dummy reference as below: For ICL, Dx12: disable MMCD, use output for reference, no intermediate buffer allocation needed. Dx11/Dx9/VAAPI: check output, if MMCD is enabled, make an intermediate allocation as dummy reference, otherwise use output, no extra allocation.
Sku	ALL
Stepping_impacted	B1
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	data_corruption
Lineage	1807084924
Title	TRTT Aliased Buffers Data Mismatch - Possible race condition between Mem Wr and HDC Flush
Bspec_wa_details	A "HDC fence" message must be inserted before the EoT of a compute, 3D or a pixel shader thread, if there is any HDC memory write requests from the thread. [L3 cache flush from the fence message is NOT needed].
Sku	ALL
Stepping_impacted	B0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-Display_ICLLP
Impact	
Lineage	14010685332
Title	ICL-YN/ICL-UN - PCH display clock remains active when it shouldn't; impact to power and sleep state residency
Bspec_wa_details	Display driver should set and clear register offset 0xC2000 bit #7 as last step in preparation for entering S0ix state.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa

Release	Gen11-GT_ICLLP
Impact	data_corruption
Lineage	14010594013
Title	Display underrun when PM fill is issued while an interrupt is pending
Bspec_wa_details	Set the register offset 0x46430 bit 22 to 1. This prevents immediate NACK to the Fill PM request while there is a pending interrupt (some other cases where memory bring down is not allowed). Display responds with a NACK after the buffers are filled to top and pm_fill is de-asserted as expected.
Sku	ALL
Stepping_impacted	A0
Stepping_fixed	
Sku_impact	driver_permanent_wa