Intel® Iris® Plus Graphics and UHD Graphics Open Source

Programmer's Reference Manual

For the 2019 10th Generation Intel Core™ Processors based on the "Ice Lake" Platform

Volume 4: Configurations

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Configurations Overview

The Intel "Gen" Graphics Architecture was first introduced to the market in 2004. Since that time, the architecture and implementation have evolved to add many new features, increase performance, and improve power efficiency.

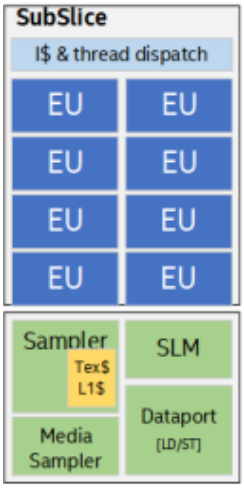
Each product generation has its own configurations chapter. Each chapter has a section for each project, and each project contains the following subsections:

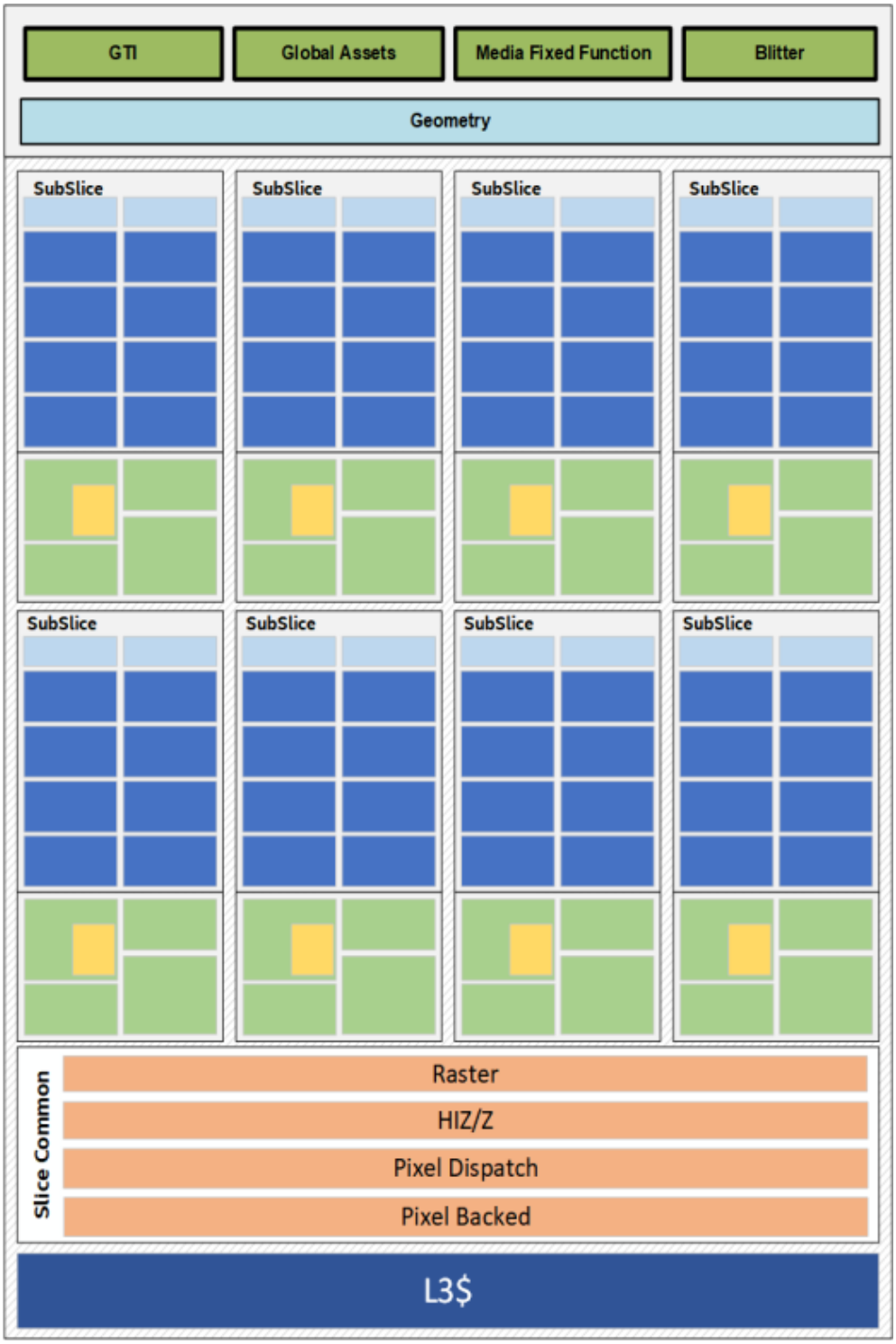
- Top Level Block Diagrams - Shows basic feature blocks of the project's graphics architecture for GT configurations.
- Device Attributes - Lists details of the graphics configuration options for each project.
- Steppings and Device IDs - Lists all the current unique GT Die / Packages for a specific project.

Top Level Block Diagrams

Gen11LP GT2 Configuration

This configuration has one slice with 8 subslices, with 8 EUs and a sampler in each subslice. The architecture is rebalanced to provide more computes and samplers.





The above diagrams consist of the following functional partitions: (a) Geometry Fixed Functions, (b) Media Fixed Functions, (c) Global Assets and GT Interface, (d) 8 Subslices, (e) one Slice-Common blocks, (f) L3 Cache blocks.

Global Assets presents a hardware and software interface from GPU to the rest of the SoC including Power Management. Graphics Technology Interface (GTI) is the gateway between GPU and the rest of the SoC. The rest of the SoC includes memory hierarchy elements such as the shared LLC memory and system Memory.

A single slice aggregates a total of 64 EU, grouped as Subslices with 8 EUs each. Aside from grouping Subslices, the Slice integrates additional logic for the geometry, L3 cache, and the Slice Common.

3D Geometry Fixed Function contains the front-end of the render pipeline. The SubSlice consists of 8 EUs supported by texture sampler, media sampler, SLM (Shared Local Memory) and a Load Store (Dataport) pipeline. The SliceCommon contains the Raster engine and the pixel pipeline (pixel dispatch and pixel backend).

Device Attributes

The following table lists detailed GT device attributes for proposed ICLLP SKUs.

NOTE: This information is preliminary, and subject to change.

Product Configuration Attribute Table				
Product Family		GEN11LP		
Architectural Name *	1x1x8	1x4x8	1x6x8	1x8x8
SKU Name	(Val)	(Fused)	(Fused)	GT2
Global Attributes				
Slice count	1	1	1	1
Subslice Count	4	4	6	8
EU/Subslice	8	8	8	8
EU count (total)	8	32	48	64
Thread Count	7	7	7	7
Thread Count (Total)	56	224	336	448
FLOPs/Clk - Half Precision, MAD (peak)	256	1024	1536	2048
FLOPs/Clk - Single Precision, MAD (peak)	128	512	768	1024
FLOPs/Clk - Double Precision, MAD (peak)	N/A	N/A	N/A	N/A
Unslice clocking (coupled/decoupled from Cr slice)	Coupled	Coupled	Coupled	Coupled
GTI / Ring Interfaces	1	1	1	1
GTI bandwidth (bytes/unslice-clk)	64R	64R	64R	64R
	64W	64W	64W	64W
eDRAM Support	N/A	N/A	N/A	N/A
Graphics Virtual Address Range	48 bit	48 bit	48 bit	48 bit
Graphics Physical Address Range	39 bit	39 bit	39 bit	39 bit
Caches & Dedicated Memories				
L3 Cache, total size (bytes)(1)	2304KB	2304KB	2304KB	3072KB
L3 Cache, bank count(1)	6	6	6	8
L3 Cache, bandwidth (bytes/clk)	12x64: R|W	12x64: R|W	12x64: R|W	16x64: R|W
L3 Cache, D$ Size (Kbytes)(1)	1152KB	1152KB	1152KB	1536KB
URB Size (kbytes)(1)	384KB-768KB	384KB-768KB	384KB-768KB	512KB-1024KB
L3 Cache, Tile Cache (Kbytes)	768KB	768KB	768KB	1024KB
SLM Size (kbytes)(1)	1x64KB	2x128KB	3x128KB	4x128KB
LLC/L4 size (bytes)	see SOC	see SOC	see SOC	see SOC
Instruction Cache (instances, bytes ea.)	1x48KB	4x48KB	6x48KB	8x48KB
Color Cache (RCC, bytes)	1x32k	2x32k	2x32k	2x32k

Product Configuration Attribute Table				
MSC Cache (MSC, bytes)	2x16k	2x16k	2x16k	2x16k
HiZ Cache (HZC, bytes)	2x12k 48 ways x 4 x 64	2x12k 48 ways x 4 x 64	2x12k	2x12k 48 ways x 4 x 64
Z Cache (RCZ, bytes)	2x32k 32 ways x16 x64	2x32k 32 ways x 16 x 64	2x32k	2x32k 32 ways x 16 x 64
Stencil Cache (STC, bytes)	2x8k 32 ways x 4 x 64	2x8k 32 ways x 4 x 64	2x8k	2x8k 32 ways x 4 x 64
Instruction Issue Rates				
FMAD, SP (ops/EU/clk)	8	8	8	8
FMUL, SP (ops/EU/clk)	8	8	8	8
FADD, SP (ops/EU/clk)	8	8	8	8
MIN,MAX, SP (ops/EU/clk)	8	8	8	8
CMP, SP (ops/EU/clk)	8	8	8	8
INV, SP (ops/EU/clk)	2	2	2	2
SQRT, SP (ops/EU/clk)	2	2	2	2
RSQRT, SP (ops/EU/clk)	2	2	2	2
LOG, SP (ops/EU/clk)	2	2	2	2
EXP, SP (ops/EU/clk)		2	2	2
POW, SP (ops/EU/clk)	1	1	1	1
IDIV, SP (ops/EU/clk)	1-6	1-6	1-6	1-6
TRIG, SP (ops/EU/clk)	2	2	2	2
FDIV, SP (ops/EU/clk)	1	1	1	1
Load/Store				
Data Ports (HDC)	1	2	3	4
L3 Load/Store - same addresses within msg (dwords/clk)	64 B/c (1*1*64)	128 B/c (1*2*64)	192 B/c	256 B/c (2*2*64)
L3 Load/Store - unique addresses within msg (dwords/clk)	64 B/c (1*1*64)	128 B/c (1*2*64)	192 B/c	256 B/c (2*2*64)
SLM Load//Store - same addresses within msg (dwords/clk)	64 B/c (1*1*64)	256 B/c (1*4*64)	384 B/c	512 B/c (4*2*64)
SLM Load//Store - unique addresses within msg (dwords/clk)	64 B/c (1*1*64)	256 B/c (1*4*64)	384 B/c	512 B/c (4*2*64)
Atomic, Local 32b - same addresses within msg (dwords/clk)	8 dw/c (1*1*8)	32 dw/c (2*2*8)	48 dw/c	64 dw/c (4*2*8)

Product Configuration Attribute Table				
Atomic, Global 32b - unique addresses within msg (dwords/clk)	8 dw/c (1*1*8)	32 dw/c (2*2*8)	48 dw/c	64 dw/c (2*2*16)
3D Attributes				
Geometry pipes	1	1	1	1
Samplers (3D)	1	4	6	8
2D Texel Rate, point, 32b (tex/clk)	4	16	24	32
2D Texel Rate, point, 64b (tex/clk)	4	16	24	32
2D Texel Rate, point, 128b (tex/clk)	4	16	24	32
2D Texel Rate, bilinear, 32b (tex/clk)	4	16	24	32
2D Texel Rate, bilinear, 64b (tex/clk)	4	16	24	32
2D Texel Rate, bilinear, 128b (tex/clk)	1	4	6	8
2D Texel Rate, trilinear, 32b (tex/clk)	2	8	12	16
2D Texel Rate, trilinear, 64b (tex/clk)	1	4	6	8
2D Texel Rate, trilinear, 128b (tex/clk)	1	4	6	8
2D Texel Sample Rate, aniso 2x (MIP nearest), 32b (tex/clk)	4	16	24	32
2D Texel Sample Rate, aniso 4x (MIP nearest), 32b (tex/clk)	2	8	12	16
2D Texel Sample Rate, aniso 8x (MIP nearest), 32b (tex/clk)	1	4	6	8
2D Texel Sample Rate, aniso 16x (MIP nearest), 32b (tex/clk)	0.5	2	3	4
3D Texel Sample Rate, point, 32b (tex/clk)	4	16	24	32
3D Texel Sample Rate, point, 64b (tex/clk)	4	16	24	32
3D Texel Sample Rate, point, 128b (tex/clk)	2	8	12	16
3D Texel Sample Rate, bilinear, 32b (tex/clk)	2	8	12	16
3D Texel Sample Rate, bilinear, 64b (tex/clk)	2	8	12	16
3D Texel Sample Rate, bilinear, 128b (tex/clk)	0.5	2	3	4
HiZ Rate, (ppc)	1x64	1x64	2x64	2x64
IZ Rate, (ppc)	1x16	1x16	2x16	2x16
Stencil Rate (ppc)	1x64	1x64	2x64	2x64
(500 MHz, DDR-2400 or eDRAM; Range depends on dynamic compression ratio)				
Pixel Rate, fill, 32bpp (pix/clk, RCC hit)	8	8	12	16

Product Configuration Attribute Table				
Pixel Rate, fill, 32bpp (pix/clk, LLC hit @ 1.0x unslice clk)	8	8	12	16
Pixel Rate, fill, 32bpp (pix/clk, memory, @ 1.0x unslice clk)	8	8	12	16
(500 MHz, DDR-2400 or eDRAM; Range depends on dynamic compression ratio)				
Pixel Rate, blend, 32bpp (p/clk, RCC hit)	8	8	12	16
Pixel Rate, blend, 32bpp (p/clk, RCC miss, @ 1.0x unslice clk)	8	8	12	16
Pixel Rate, blend, 32bpp (pix/clk, memory, @ 1.0x unslice clk)	8	8	12	16
Media Attributes				
Samplers (VME)	1	2	3	4
Samplers (AVS/IEF/VA)	1	4	6	8
VDBox Instances (See)	1	2	2	2
VEBox Instances	1	1	1	1
SFC Instances	1	1	1	1
WGBox Instances	0	0	0	0
Display Attributes				
Display Pipes	3	3	3	3
Display Planes per Pipe	7	7	7	7
DDI ports	3	3	3	3
MIPI ports	1	1	1	1

Notes:

* Architectural Name = Slice Count x Subslice Count x EUs per Subslice

(1) Programmable range; Data and URB portioning of L3 cache.

(2) Decoupled unslice clock sitll to be determined.

Steppings and Device IDs

Unique Devices

The following table details all currently planned SKUs for ICL. Prior to manufacturing, this information is subject to change at any time.

SKUs and Device IDs

Segment	SKU	GT	EU Config	Total EUs	VDBoxes	TDP	CPU Brand	Graphics Branding	Graphics Brand Number	SOC Stepping	Dev2 ID	RevID	POR	PRQd	OK to Upstream DevID?*	OK to add to Public Windows INF?**
Mobile	U42	GT2	1x8x8	64	2	15W	Core i7	Intel(R) Iris(R) Plus Graphics	N/A	D1	0x8A52	0x7	Yes	Yes	Yes	Yes
Mobile	U42	GT1.5F	1x6x8	48	2	15W	Core i3/i5/i7	Intel(R) Iris(R) Plus Graphics	N/A	D1	0x8A5A	0x7	Yes	Yes	Yes	Yes
Mobile	U42	GT1F	1x4x8	32	1	15W	Core i3	Intel(R) UHD Graphics	N/A	D1	0x8A56	0x7	Yes	Yes	Yes	Yes
Mobile	Y42	GT2	1x8x8	64	2	9W	Core i7	Intel(R) Iris(R) Plus Graphics	N/A	D1	0x8A51	0x7	Yes	Yes	Yes	Yes
Mobile	Y42	GT1.5F	1x6x8	48	2	9W	Core i3/i5/i7	Intel(R) Iris(R) Plus Graphics	N/A	D1	0x8A5C	0x7	Yes	Yes	Yes	Yes

Segment	SKU	GT	EU Config	Total EUs	VDBoxes	TDP	CPU Brand	Graphics Branding	Graphics Brand Number	SOC Stepping	Dev2 ID	RevID	POR	PRQd	OK to Upstream DevID?*	OK to add to Public Windows INF?**
Mobile	Y42	GT1F	1x4x8	32	1	9W	Core i3	Intel(R) UHD Graphics	N/A	D1	0x8A58	0x7	Yes	Yes	Yes	Yes
Mobile	U42	GT2	1x8x8	64	2	15W	Core i7	Intel(R) Iris(R) Plus Graphics	N/A	D2	0x8A52	0x7	Yes	Yes	Yes	Yes
Mobile	U42	GT1.5F	1x6x8	48	2	15W	Core i3/i5/i7	Intel(R) Iris(R) Plus Graphics	N/A	D2	0x8A5A	0x7	Yes	Yes	Yes	Yes
Mobile	U42	GT1F	1x4x8	32	1	15W	Core i3	Intel(R) UHD Graphics	N/A	D2	0x8A56	0x7	Yes	Yes	Yes	Yes
Mobile	Y42	GT2	1x8x8	64	2	9W	Core i7	Intel(R) Iris(R) Plus Graphics	N/A	D2	0x8A51	0x7	Yes	Yes	Yes	Yes
Mobile	Y42	GT1.5F	1x6x8	48	2	9W	Core i3/i5/i7	Intel(R) Iris(R) Plus Graphics	N/A	D2	0x8A5C	0x7	Yes	Yes	Yes	Yes
Mobile	Y42	GT1F	1x4x8	32	1	9W	Core i3	Intel(R) UHD Graphics	N/A	D2	0x8A58	0x7	Yes	Yes	Yes	Yes

Segment	SKU	GT	EU Config	Total EUs	VDBoxes	TDP	CPU Brand	Graphics Branding	Graphics Brand Number	SOC Stepping	Dev2 ID	RevID	POR	PRQd	OK to Upstream DevID?*	OK to add to Public Windows INF?**
Mobile	U42	GT2	1x8x8	64	2	15W	Core i7	Intel(R) Iris(R) Plus Graphics	N/A	D3	0x8A52	0x7	Yes	Yes	Yes	Yes
Mobile	U42	GT1.5F	1x6x8	48	2	15W	Core i3/i5/i7	Intel(R) Iris(R) Plus Graphics	N/A	D3	0x8A5A	0x7	Yes	Yes	Yes	Yes
Mobile	U42	GT1F	1x4x8	32	1	15W	Core i3	Intel(R) UHD Graphics	N/A	D3	0x8A56	0x7	Yes	Yes	Yes	Yes
Mobile	Y42	GT2	1x8x8	64	2	9W	Core i7	Intel(R) Iris(R) Plus Graphics	N/A	D3	0x8A51	0x7	Yes	Yes	Yes	Yes
Mobile	Y42	GT1.5F	1x6x8	48	2	9W	Core i3/i5/i7	Intel(R) Iris(R) Plus Graphics	N/A	D3	0x8A5C	0x7	Yes	Yes	Yes	Yes
Mobile	Y42	GT1F	1x4x8	32	1	9W	Core i3	Intel(R) UHD Graphics	N/A	D3	0x8A58	0x7	Yes	Yes	Yes	Yes