

Intel® Open Source HD Graphics Programmers' Reference Manual (PRM)

Volume 2c: Command Reference: Register Addresses

For the 2014-2015 Intel Atom™ Processors, Celeron™ Processors and Pentium™ Processors based on the "Cherry Trail/Braswell" Platform
(Cherryview/Braswell graphics)

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PWRMTR_WT3_EEVT33TO361014

PWRMTR_WT3_EEVT37TO401015

PWRMTR_WT3_EEVT41TO441016

PWRMTR_WT3_EEVT45TO481017

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Advanced Features Length and Capabilities

AFLC - Advanced Features Length and Capabilities			
Register Space:	PCI: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x03060013		
Size (in bits):	32		
Address:	000A4h		
FLR capability advertisement			
DWord	Bit	Description	
0	31:26	RESERVED	
		Default Value: 00h	
		Access: RO	
		Reserved	
		25	FLR_CAP
Access: RO			
Function Level Reset Capability (FLR_CAP): 0: Function Level Reset is not supported 1: Function Level Reset is supported			
24	TP_CAP	Default Value: 1b	
		Access: RO	
		Transactions Pending Capability (TP_CAP): 0: Transactions Pending bit is not supported 1: Transactions Pending bit is supported	
23:16	LENGTH	Default Value: 06h	
		Access: RO	
		Advanced Features Structure Length(LENGTH): The Advanced Features capability structure is 6bytes long.	
15:8	NXT_PTR	Default Value: 00h	
		Access: R/W Once	
		Next Pointer (NXT_PTR):	

AFLC - Advanced Features Length and Capabilities

		<p>Points to the next item in the list (B0=Vendor Capabilities ID). This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset. Write once so capabilities list can be changed if needed.</p>					
	7:0	<p>CAP_ID</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">13h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Capability Identifier (CAP_ID): A value of 13h identifies that this PCI Function is capable of Advanced Features.</p>		Default Value:	13h	Access:	RO
Default Value:	13h						
Access:	RO						

Advanced Scheduler Reset Request Messages

ASSRREQ - Advanced Scheduler Reset Request Messages				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0810Ch			
Hardware (CS, VCS) initiated Advanced Scheduler reset request messages.				
DWord	Bit	Description		
0	31:16	<p>Message Mask</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000</p>	Access:	RO
	Access:	RO		
	15:4	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved</p>	Access:	RO
	Access:	RO		
	3	<p>VINunit cmfxrst reset request message (2nd Vbox)</p> <table border="1"> <tr> <td>Access:</td> <td>R/W Set</td> </tr> </table> <p>CMFX Reset Request Message from the VINunit in 2nd Vbox: '1' : CMFX Reset Requested - This bit is cleared by the CP upon completion of the reset request '0' : CMFX Reset Not Requested</p>	Access:	R/W Set
Access:	R/W Set			
2	<p>VINunit cmfxrst Reset Request message</p> <table border="1"> <tr> <td>Access:</td> <td>R/W Set</td> </tr> </table> <p>CMFX Reset Request Message from the VINunit: '1' : CMFX Reset Requested - This bit is cleared by the CP upon completion of the reset request '0' : CMFX Reset Not Requested</p>	Access:	R/W Set	
Access:	R/W Set			
1	<p>Render AS Reset Request Message</p> <table border="1"> <tr> <td>Access:</td> <td>R/W Set</td> </tr> </table> <p>Render AS Reset Request Message from the CSunit: '1' : Render AS Reset Requested - This bit is cleared by the CP upon completion of the reset request '0' : Render AS Reset Not Requested</p>	Access:	R/W Set	
Access:	R/W Set			

ASSRREQ - Advanced Scheduler Reset Request Messages

	0			
		<p>Media AS Reset Request Message</p> <table border="1"> <tr> <td>Access:</td> <td>R/W Set</td> </tr> </table> <p>Media AS Reset Request Message from the VCSunit: '1' : Media AS Reset Requested - This bit is cleared by the CP upon completion of the reset request '0' : Media AS Reset Not Requested</p>	Access:	R/W Set
Access:	R/W Set			

Aggregate_Perf_Counter_A31

OAPERF_A31 - Aggregate_Perf_Counter_A31				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	BSpec			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	028F8h			
Valid Projects:	[CHV, BSW]			
This register reflects the count value of the OA Performance counter A31				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">U32</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32
Format:	U32			

Aggregate_Perf_Counter_A32

OAPERF_A32 - Aggregate_Perf_Counter_A32				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	BSpec			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	02900h			
Valid Projects:	[CHV, BSW]			
This register reflects the count value of the OA Performance counter A32				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U32</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32
Format:	U32			

Aggregate_Perf_Counter_A33

OAPERF_A33 - Aggregate_Perf_Counter_A33				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	BSpec			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	02904h			
Valid Projects:	[CHV, BSW]			
This register reflects the count value of the OA Performance counter A33				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U32</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32
Format:	U32			

Aggregate_Perf_Counter_A34

OAPERF_A34 - Aggregate_Perf_Counter_A34				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	BSpec			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	02908h			
Valid Projects:	[CHV, BSW]			
This register reflects the count value of the OA Performance counter A34				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U32</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32
Format:	U32			

Aggregate_Perf_Counter_A35

OAPERF_A35 - Aggregate_Perf_Counter_A35				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	BSpec			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	0290Ch			
Valid Projects:	[CHV, BSW]			
This register reflects the count value of the OA Performance counter A35				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U32</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32
Format:	U32			

Aggregate Perf Counter A1

OAPERF_A1 - Aggregate Perf Counter A1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02808h	
Valid Projects:	[CHV, BSW]	
This register reflects the count value of the OA Performance counter A1. DefaultValue="00000000h"		
DWord	Bit	Description
0	31:0	Considerations: This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A5

OAPERF_A5 - Aggregate Perf Counter A5		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02828h	
Valid Projects:	[CHV, BSW]	
This register reflects the count value of the OA Performance counter A5. DefaultValue="00000000h"		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>

Aggregate Perf Counter A7

OAPERF_A7 - Aggregate Perf Counter A7		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02838h	
Valid Projects:	[CHV, BSW]	
This register reflects the count value of the OA Performance counter A7. DefaultValue="00000000h"		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>

Aggregate Perf Counter A8

OAPERF_A8 - Aggregate Perf Counter A8		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02840h	
Valid Projects:	[CHV, BSW]	
This register reflects the count value of the OA Performance counter A8. DefaultValue="00000000h"		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>

Aggregate Perf Counter A9

OAPERF_A9 - Aggregate Perf Counter A9		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02848h	
Valid Projects:	[CHV, BSW]	
This register reflects the count value of the OA Performance counter A9. DefaultValue="00000000h"		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>

Aggregate Perf Counter A10

OAPERF_A10 - Aggregate Perf Counter A10		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02850h	
Valid Projects:	[CHV, BSW]	
This register reflects the count value of the OA Performance counter A10. DefaultValue="00000000h"		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>

Aggregate Perf Counter A11

OAPERF_A11 - Aggregate Perf Counter A11		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02858h	
Valid Projects:	[CHV, BSW]	
This register reflects the count value of the OA Performance counter A11. DefaultValue="00000000h"		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>

Aggregate Perf Counter A12

OAPERF_A12 - Aggregate Perf Counter A12		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02860h	
Valid Projects:	[CHV, BSW]	
This register reflects the count value of the OA Performance counter A12. DefaultValue="00000000h"		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>

Aggregate Perf Counter A13

OAPERF_A13 - Aggregate Perf Counter A13		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02868h	
Valid Projects:	[CHV, BSW]	
This register reflects the count value of the OA Performance counter A13. DefaultValue="00000000h"		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>

Aggregate Perf Counter A14

OAPERF_A14 - Aggregate Perf Counter A14		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02870h	
Valid Projects:	[CHV, BSW]	
This register reflects the count value of the OA Performance counter A14. DefaultValue="00000000h"		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>

Aggregate Perf Counter A15

OAPERF_A15 - Aggregate Perf Counter A15		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02878h	
Valid Projects:	[CHV, BSW]	
This register reflects the count value of the OA Performance counter A15. DefaultValue="00000000h"		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>

Aggregate Perf Counter A16

OAPERF_A16 - Aggregate Perf Counter A16		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02880h	
Valid Projects:	[CHV, BSW]	
This register reflects the count value of the OA Performance counter A16. DefaultValue="00000000h"		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>

Aggregate Perf Counter A17

OAPERF_A17 - Aggregate Perf Counter A17		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02888h	
Valid Projects:	[CHV, BSW]	
This register reflects the count value of the OA Performance counter A17. DefaultValue="00000000h"		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>

Aggregate Perf Counter A18

OAPERF_A18 - Aggregate Perf Counter A18		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02890h	
Valid Projects:	[CHV, BSW]	
This register reflects the count value of the OA Performance counter A9. DefaultValue="00000000h"		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>

Aggregate Perf Counter A21

OAPERF_A21 - Aggregate Perf Counter A21		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	028A8h	
Valid Projects:	[CHV, BSW]	
This register reflects the count value of the OA Performance counter A21. DefaultValue="00000000h"		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>

Aggregate Perf Counter A22

OAPERF_A22 - Aggregate Perf Counter A22		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	028B0h	
Valid Projects:	[CHV, BSW]	
This register reflects the count value of the OA Performance counter A22. DefaultValue="00000000h"		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>

Aggregate Perf Counter A23

OAPERF_A23 - Aggregate Perf Counter A23		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	028B8h	
Valid Projects:	[CHV, BSW]	
This register reflects the count value of the OA Performance counter A23. DefaultValue="00000000h"		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>

Aggregate Perf Counter A24

OAPERF_A24 - Aggregate Perf Counter A24		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	028C0h	
Valid Projects:	[CHV, BSW]	
This register reflects the count value of the OA Performance counter A24. DefaultValue="00000000h"		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>

Aggregate Perf Counter A25

OAPERF_A25 - Aggregate Perf Counter A25		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	028C8h	
Valid Projects:	[CHV, BSW]	
This register reflects the count value of the OA Performance counter A25. DefaultValue="00000000h"		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>

Aggregate Perf Counter A26

OAPERF_A26 - Aggregate Perf Counter A26		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	028D0h	
Valid Projects:	[CHV, BSW]	
This register reflects the count value of the OA Performance counter A26. DefaultValue="00000000h"		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>

Aggregate Perf Counter A27

OAPERF_A27 - Aggregate Perf Counter A27		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	028D8h	
Valid Projects:	[CHV, BSW]	
This register reflects the count value of the OA Performance counter A27. DefaultValue="00000000h"		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>

Aggregate Perf Counter A28

OAPERF_A28 - Aggregate Perf Counter A28		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	028E0h	
Valid Projects:	[CHV, BSW]	
This register reflects the count value of the OA Performance counter A28. DefaultValue="00000000h"		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>

Aggregate Perf Counter A29

OAPERF_A29 - Aggregate Perf Counter A29		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	028E8h	
Valid Projects:	[CHV, BSW]	
This register reflects the count value of the OA Performance counter A29. DefaultValue="00000000h"		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>

Aggregate Perf Counter A30

OAPERF_A30 - Aggregate Perf Counter A30		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	028F0h	
Valid Projects:	[CHV, BSW]	
This register reflects the count value of the OA Performance counter A30. DefaultValue="00000000h"		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>

AFCTLSTS

AFCTLSTS - AFCTLSTS		
Register Space:	PCI: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	16	
Address:	000A8h	
FLR control Advanced Feature Status		
DWord	Bit	Description
0	15:9	Reserved
		Default Value: 00h
		Access: RO
		Reserved (RSVD)
8	TP	Default Value: 0b
		Access: RO
		Transaction Pending (TP): 1: The Function has issued one or more non-posted transactions which have not been completed, including non-posted transactions that a target has terminated with Retry. 0: All non-posted transactions have been completed.
7:1	Reserved	Default Value: 00h
		Access: RO
		Reserved (RSVD)
0	INIT_FLR	Default Value: 0b
		Access: R/W Set
		Initiate Function Level Reset (INIT_FLR): A write of 1b initiates Function Level Reset (FLR). FLR requirements are defined in the PCI Express Base Specification. Registers and state information that do not apply to conventional PCI are exempt from the FLR requirements given there. Once written 1, FLR will be initiated. During FLR, a read will return 1's since device 2 reads abort. Once FLR completes, hardware will clear the bit to 0.

All Engine Fault Register

FAULT_REG - All Engine Fault Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	04094h			
DWord	Bit	Description		
0	31:1	All Engine Fault Register		
		<table border="1"> <tr> <td>Default Value:</td> <td>00000000000000000000000000000000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit[31:15]: Reserved. Bit[14:12]: Engine ID: 000b - GFX. 001b - MFX0. 010b - MFX1. 011b - VEBX. 100b - BLT. 110b - WIDI. Bit[11]: Reserved. Bit[10:3]: SRCID of Fault. This is the Source ID of the unit that requested the cycle that generated the First Page fault for this engine. This value is locked and not updated on subsequent faults, until the valid bit of this register is cleared by SW. Bit[2:1]: Fault Type (GFX_FT): Type of Fault recorded: 00b - Invalid PTE Fault. 01b - Invalid PDE Fault. 10b - Invalid PDPE Fault. 11b - Invalid PML4E Fault. This value is locked and not updated on subsequent faults, until the valid bit of this register is cleared by SW. All bits are only valid with bit[0]=1.</p>	Default Value:	00000000000000000000000000000000b
Default Value:	00000000000000000000000000000000b			
Access:	R/W			
0	0	Valid Bit		
		<table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This bit indicates that the first fault for this engine has been recorded. It can only be cleared by SW, which also clears the other fields.</p>	Default Value:	0b
Default Value:	0b			
Access:	R/W			

ARAT CUTRIG HI

ARAT_CUTRIG_HI - ARAT CUTRIG HI				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A1B4h			
DWord	Bit	Description		
0	31:0	<p>ARAT TRIG HI</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>[31:0]: 63:32 of (ARAT_TDELTA + TSC)[63:32] when A174[0] transitions to a one, or when A174[1:0]=11 and TSC crosses over ARAT_TRIG</p>	Access:	RO
Access:	RO			

ARAT CUTRIG LO

ARAT_CUTRIG_LO - ARAT CUTRIG LO		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A1B0h	
DWord	Bit	Description
0	31:3	ARAT TRIG LO Access: RO 31:3 of (ARAT_TDELTA + TSC)[31:3] when A174[0] transitions to a one, or when A174[1:0]=11 and TSC crosses over ARAT_TRIG
	2	Reserved Access: RO
	1:0	ARAT TRIG Mode Access: RO 0xA174[1:0] when A174[0] transitions to a one, or when A174[1:0]=11 and TSC crosses over ARAT_TRIG

ARAT Delta (LSB)

ARAT_TDELTA_LOW - ARAT Delta (LSB)				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A174h			
DWord	Bit	Description		
0	31:3	<p>Lower Bits of Delta Time for ARAT</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Low Bits [31:3] of Delta Time, in 80ns increments(LSB would be in 10ns increments, if it went down to zero)</p>	Access:	R/W
	Access:	R/W		
	2	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
1	<p>ARAT Mode</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>0b : One-Shot Mode (default) 1b : Periodic Mode</p>	Access:	R/W	
Access:	R/W			
0	<p>ARAT Enable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>0b : ARAT Disabled (default) 1b : ARAT Enabled</p>	Access:	R/W	
Access:	R/W			

ARAT Delta (MSB)

ARAT_TDELTA_HIGH - ARAT Delta (MSB)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A170h	
DWord	Bit	Description
0	31:24	Reserved Access: RO
	23:0	Upper Bits of Delta Time for ARAT Access: R/W High Bits [55:32] of Delta Time, in 80ns increments

ARAT POST CU BUSY

ARAT_POSTCUBUSY - ARAT POST CU BUSY				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A17Ch			
DWord	Bit	Description		
0	31:3	ARAT PostThreshold <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> PostThreshold, in 80ns increments to prevent short gfx_clockstartreq. If current_TSC - ARAT_CUTRIG > PostThreshold, show GFX as busy.	Access:	R/W
	Access:	R/W		
2:0	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			

ARAT PRE CU BUSY

ARAT_PRECUBUSY - ARAT PRE CU BUSY		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A178h	
DWord	Bit	Description
0	31:3	ARAT PreThreshold Access: R/W PreThreshold, in 80ns increments to prevent short gfx_clockstartreq. If ARAT_CUTRIG minus current_TSC < PreThreshold, show GFX as busy.
	2:0	Reserved Access: RO

Arbiter Control Register

GARBCNTLREG - Arbiter Control Register					
Register Space:	MMIO: 0/2/0				
Project:	CHV, BSW				
Source:	PRM				
Default Value:	0x29124100 CHV, BSW				
Size (in bits):	32				
Address:	0B004h				
DWord	Bit	Description			
0	31	Reserved			
	30	<p>Disables hashing function</p> <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Disables hashing function to generate bank_id[1:0] for L3\$ bank accessing, and forces the use of address[7:6] for bank_id[1:0].0: (default) Hash function enabled to generate L3\$ bank IDs. 1: L3\$ address[7:6] used as L3\$ bank IDs. Incf_csr_l3bankidhashdis. (This bit needs to set corresponding bit lpfcon_csr_l3bankidhashdis in LPFC.)</p>	Access:	R/W	
	Access:	R/W			
	29:28	<p>Arbitration priority order between RCC and MSC</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>10b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Arbitration priority order between RCC and MSC. 00b/11b: Invalid; default setting used. 10b: Default setting; RCC MSC (i.e., MSC has higher priority). 01b: RCC MSC (i.e., RCC has higher priority). Incf_csr_rcc_msc_pri[1:0].</p>	Default Value:	10b	Access:
Default Value:	10b				
Access:	R/W				
27:22	<p>Arbitration priority order between RCZ, STC, and HIZ</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>100100b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Arbitration priority order between RCZ, STC, and HIZ. 100100b: Default setting; RCZ STC HIZ. (i.e., RCZ has lowest priority; HIZ has highest priority). 100001b: RCZ ; HIZ ; STC. 011000b: STC ; RCZ ; HIZ. 010010b: STC ; HIZ ; RCZ. 001001b: HIZ ; RCZ ; STC. 000110b: HIZ ; STC ; RCZ. Note: Others settings are invalid, and result in use of default. Incf_csr_rcz_stc_hiz_pri[5:0].</p>	Default Value:	100100b	Access:	R/W
Default Value:	100100b				
Access:	R/W				

GARBCNTLREG - Arbiter Control Register

21:19	Write data port arbitration priority between Z client writes and L3\$ evictions		
	Default Value:	010b	
	Access:	R/W	
	<p>Z Max Write Request Limit Count (GFXC_MRLC). This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (both Slice 0 and 1). Minimum count value must be = 1. Incf_csr_wdpagapz[2:0].</p>		
18:16	Write data port arbitration priority between C client writes and Z/L3\$ writes/evictions		
	Default Value:	010b	
	Access:	R/W	
	<p>C Max Request Limit Count (GFXZ_MRLC). This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (both Slice 0 and 1). Minimum count value must be = 1. Incf_csr_wdpagapc[2:0].</p>		
15	Reserved		
	Access:	RO	
14:12	L3 Max Write Request Limit Count		
	Default Value:	100b	
	Access:	R/W	
	<p>L3 Max Write Request Limit Count (GFXL3_MRLC). This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1. Incf_csr_wdpagapl3[2:0].</p>		
11:9	Reserved		
	Access:	RO	
8	GAPs_fixarb_en		
	Default Value:	1b	
	Access:	R/W	
	Incf_csr_gaps_fixarb_en.		
6:0	Reserved		
	Project:	CHV, BSW	
	Access:	RO	

Arbiter Mode Control Register

ARB_MODE - Arbiter Mode Control Register			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	04030h		
DWord	Bit	Description	
0	31:16	Mask Bits	
		Default Value:	0000000000000000b
		Access:	RO
			Mask Bits act as Write Enables for the bits[15:0] of this register.
	15	Extra Register Bit 15	
		Default Value:	0b
		Access:	R/W
			Bit 15 toggles (XOR) the meaning of Per Client Write Drop Enables (Register 40b4); If 0, drop per client happens as stated in register 40b4 definition; If 1, the meaning changes, and a 1 on a bit in register 40b4 means dont drop while 0 means drop. In this case, the default (for clients not included in 40b4) will be drop enabled.
	14	Extra Register Bit 14	
		Default Value:	0b
		Project:	CHV, BSW
		Access:	R/W
		PD load disable - When this bit is set, the PD load is disabled for GFX/MFX0/MFX1. A-step: Default Value: 0 B-step: Default Value: 0 - Bug ID: 1905990 Future steppings can have value 1.	
13	DC GDR		
	Default Value:	0b	
		Access:	R/W
12	HIZ GDR		
	Default Value:	0b	
		Access:	R/W
11	STC GDR		
	Default Value:	0b	
		Access:	R/W

ARB_MODE - Arbiter Mode Control Register

10	BLB GDR <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table>	Default Value:	0b	Access:	R/W		
Default Value:	0b						
Access:	R/W						
9	GAM PD GDR <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table>	Default Value:	0b	Access:	R/W		
Default Value:	0b						
Access:	R/W						
8	Extra Register Bit 8 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #e6f2ff;"> <th style="text-align: center; padding: 5px;">Description</th> </tr> </thead> <tbody> <tr> <td style="padding: 5px;"> Snoop Override [CHV, BSW Only] 0 - No override (default) 1 - Snoop is set for all accesses to memory </td> </tr> </tbody> </table>	Default Value:	0b	Access:	R/W	Description	Snoop Override [CHV, BSW Only] 0 - No override (default) 1 - Snoop is set for all accesses to memory
Default Value:	0b						
Access:	R/W						
Description							
Snoop Override [CHV, BSW Only] 0 - No override (default) 1 - Snoop is set for all accesses to memory							
7:6	Cacheability Attribute Override <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">00b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>00b No override. 01b UC (LLC/eLLC) - Allocation age is don't care. 10b WT in LLC/eLLC - Aged is 3. 11b WB in LLC/eLLC - Aged is 3. The above conditions apply for the following conditions only: 1. Register overwrite except for GTT, CFG and L3 coherent wcil cycles 2. Read- GTTRD, CFGRD 3. Write- GTTWR, CFGWR, DMWR (with gam_ci_wcoherenttype[2:0]="001" WCIL* w/self snoop)</p>	Default Value:	00b	Access:	R/W		
Default Value:	00b						
Access:	R/W						
5	Extra Register Bit 5 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>Reserved.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b						
Access:	R/W						
4	VMC GDR Enable <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>When this bit is set, data requested from the VMC client is generated by the GDR Algorithm.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b						
Access:	R/W						
3	Texture Cache (MT) GDR Enable Bit <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>When this bit is set, data requested from the Texture Cache (MT) client is generated by the GDR algorithm.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b						
Access:	R/W						

ARB_MODE - Arbiter Mode Control Register					
2	<p>Depth (RCZ) Cache GDR Enable bit</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Depth Cache GDR enable bit. Project: All. Format: U1. When this bit is set, data requested from the Depth Cache client is generated by the GDR algorithm (See GDR algorithm in xxx section).</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
1	<p>Color Cache (RCC) GDR Enable Bit</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>When this bit is set, data requested from the Color Cache (RCC) client is generated by the GDR algorithm.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
0	<p>GTT Accesses GDR</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>When this bit is enabled along with the Client's GDR bit, PPGTT and GGTT requests for this memory access are also tagged as GDR to SQ.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				

ASLS

ASLS - ASLS						
Register Space:	PCI: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	000FCh					
<p>ASL Storage.</p> <p>This software scratch register only needs to be read/write accessible. The exact bit register usage must be worked out in common between System BIOS and driver software, but storage for switching/indicating up to 6 devices is possible with this amount.</p> <p>For each device, the ASL control method with require two bits for _DOD (BIOS detectable yes or no, VGA/NonVGA), one bit for _DGS (enable/disable requested), and two bits for _DCS (enabled now/disabled now, connected or not).</p>						
DWord	Bit	Description				
0	31:0	<p>SCRATCH</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This register provides a means for the BIOS to communicate with the driver. This definition of this scratch register is worked out in common between System BIOS and driver software. Storage for up to 6 devices is possible. For each device, the ASL control method requires two bits for _DOD (BIOS detectable yes or no, VGA/NonVGA), one bit for _DGS (enable/disable requested), and two bits for DCS (enabled now/disabled now, connected or not).</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

ASYNC_SLICE_COUNT

ASYNC_SLICE_COUNT - ASYNC_SLICE_COUNT			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000280		
Size (in bits):	32		
Address:	0A204h		
Async Slice Count Select Register			
DWord	Bit	Description	
0	31:11	Reserved	
		Default Value:	00000h
		Access:	RO
		Reserved	
	10:8	Async_SS	
		Default Value:	010b
		Access:	R/W
		Number of subslices to power (Async Mode): 001 : 1 subslice 010 : 2 subslices (GT1-based CHV, BSW only) Actual SSs used = Async_SS if SScountEn=0 Actual SSs used = SScount if SScountEn=1	
	7:4	Async_EU	
		Default Value:	1000b
		Access:	R/W
		Maximum number of EUs to power per subslice if multiple subslices enabled Async Mode Actual EUs used = Async_EU if EUmin < Async_EU < EUmax Actual EUs used = EUmax if Async_EU >= EUmax Actual EUs used = EUmin if EUmin >= Async_EU	
	3	Reserved	
		Default Value:	0b
		Access:	RO
		Reserved	
2:0	temp_slicecount		
	Default Value:	000b	
	Access:	R/W	
	Slice Count Request in Asynchronous Mode.		

Auto Draw End Offset

3DPRIM_END_OFFSET - Auto Draw End Offset				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	RenderCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	02420h-02423h			
Valid Projects:				
DWord	Bit	Description		
0	31:0	<p>End Offset</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>This register is used to store the end offset value used by the Vertex Fetch to determine when to stop processing the 3D_PRIMITIVE command. This register is valid when the End Offset Enable is set in the 3D_PRIMITIVE command.</p>	Format:	U32
Format:	U32			

Base of Data Stolen Memory

BDSM - Base of Data Stolen Memory						
Register Space:	PCI: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0005Ch					
<p>This register contains the base address of Graphics Data Stolen DRAM memory. Graphics Stolen Memory is within DRAM space. The base of stolen memory will always be below 4G.</p>						
DWord	Bit	Description				
0	31:20	<p>BDSM</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W Lock</td> </tr> </table> <p>BDSM: BASE_OF_Data_STOLEN_MEMORY. This register contains bits 31 to 20 of the base address of Data stolen DRAM memory. For certain GTLC generated accesses, this base register will be added to GTLC-provided offset address, forming the full physical address for the PFI fabric. This is also used as a base for VGA paged accesses.</p>	Default Value:	000h	Access:	R/W Lock
		Default Value:	000h			
		Access:	R/W Lock			
<p>RESERVED</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">00000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">RO</td> </tr> </table> <p>Reserved</p>	Default Value:	00000h	Access:	RO		
Default Value:	00000h					
Access:	RO					
<p>BDSM_LOCK</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W Lock</td> </tr> </table> <p>This bit will lock all writable settings in this register, including itself.</p>	Default Value:	0b	Access:	R/W Lock		
Default Value:	0b					
Access:	R/W Lock					

Base of GTT Stolen Memory

BGSM - Base of GTT Stolen Memory			
Register Space:	PCI: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	00070h		
<p>Base of GTT table in Gfx Stolen Memory The GTT table is located within Graphics Stolen Memory in DRAM space. The base of stolen memory will always be below 4G.</p>			
DWord	Bit	Description	
0	31:20	BGSM	
		Default Value:	000h
		Access:	R/W Lock
		BGSM: Gfx Base of GTT Stolen Memory. This register contains bits 31 to 20 of the base address of GTT Table in stolen DRAM memory. BIOS determines base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI offset 50 bits 9:8) from the Graphics Base of Data stolen(PCI offset 5C bits 31:20).	
	19:1	RESERVED	
		Default Value:	00000h
		Access:	RO
		Reserved	
	0	BGSM_LOCK	
		Default Value:	0b
Access:		R/W Lock	
This bit will lock all writeable settings in this register including itself			

Batch Address Difference Register

BB_ADDR_DIFF - Batch Address Difference Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	02154h-02157h			
Name:	Batch Address Difference Register			
ShortName:	BB_ADDR_DIFF_RCSUNIT			
Address:	12154h-12157h			
Name:	Batch Address Difference Register			
ShortName:	BB_ADDR_DIFF_VCSUNIT0			
Address:	1A154h-1A157h			
Name:	Batch Address Difference Register			
ShortName:	BB_ADDR_DIFF_VECSUNIT			
Address:	1C154h-1C157h			
Name:	Batch Address Difference Register			
ShortName:	BB_ADDR_DIFF_VCSUNIT1			
Address:	22154h-22157h			
Name:	Batch Address Difference Register			
ShortName:	BB_ADDR_DIFF_BCSUNIT			
<p>This register contains the difference between the start of the last batch and where the last initiated Batch Buffer is currently fetching commands.</p>				
Programming Notes				
<p>Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.</p>				
DWord	Bit	Description		
0	31:2	<p>Batch Buffer Address Difference</p> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>GraphicsAddress[31:2]</td> </tr> </table> <p>This field specifies the DWord-aligned difference between the starting address of the batch buffer and where the last initiated Batch Buffer is currently fetching commands.</p>	Format:	GraphicsAddress[31:2]
	Format:	GraphicsAddress[31:2]		
1:0	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ			

Batch Buffer Head Pointer Register

BB_ADDR - Batch Buffer Head Pointer Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Access:	RO			
Size (in bits):	32			
Address:	02140h-02143h			
Name:	Batch Buffer Head Pointer Register			
ShortName:	BB_ADDR_RCSUNIT			
Address:	12140h-12143h			
Name:	Batch Buffer Head Pointer Register			
ShortName:	BB_ADDR_VCSUNIT0			
Address:	1A140h-1A143h			
Name:	Batch Buffer Head Pointer Register			
ShortName:	BB_ADDR_VECSUNIT			
Address:	1C140h-1C143h			
Name:	Batch Buffer Head Pointer Register			
ShortName:	BB_ADDR_VCSUNIT1			
Address:	22140h-22143h			
Name:	Batch Buffer Head Pointer Register			
ShortName:	BB_ADDR_BCSUNIT			
This register contains the current DWord Graphics Memory Address of the last-initiated batch buffer.				
Programming Notes				
Programming Restriction: This register should NEVER be programmed by driver. This is for HW internal use only.				
DWord	Bit	Description		
0	31:2	Batch Buffer Head Pointer		
		<table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[31:2]</td> </tr> </table> <p>This field specifies the DWord-aligned Graphics Memory Address where the last initiated Batch Buffer is currently fetching commands. If no batch buffer is currently active, the Valid bit will be 0 and this field will be meaningless.</p>	Project:	CHV, BSW
Project:	CHV, BSW			
Format:	GraphicsAddress[31:2]			
1		Reserved		
		<table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			

BB_ADDR - Batch Buffer Head Pointer Register			
0	Valid		
	Format:	U1	
	Value	Name	Description
	0h	Invalid [Default]	Batch buffer Invalid
1h	Valid	Batch buffer Valid	

Batch Buffer Per Context Pointer

BB_PER_CTX_PTR - Batch Buffer Per Context Pointer	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	021C0h-021C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_RCSUNIT
Address:	121C0h-121C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VCSUNIT0
Address:	1A1C0h-1A1C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VECSUNIT
Address:	1C1C0h-1C1C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VCSUNIT1
Address:	221C0h-221C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_BCSUNIT
<p>This register is used to program the batch buffer address to be executed between context restore and execution of ring/execution list if enabled. This will only get executed due to regular context save/restore and not during power restore. This register is part of the execution list context and will be executed per context. Only supported if execution list is enabled. There is no preempting workloads within the Per Context Batch Buffer.</p>	
Source	
BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS	
RenderCS	
RenderCS	
RenderCS	

BB_PER_CTX_PTR - Batch Buffer Per Context Pointer

Workaround

Workaround: [Render CS Only][Execlist Mode of Scheduling]: SW must ensure arbitration is switched off while context restore is in progress for any given context. This is achieved by disabling arbitration by programming MI_ARB_ON_OFF to "Arbitration Disable" in RCS_INDIRECT_CTX buffer and by enabling back the arbitration by programming MI_ARB_ON_OFF to "Arbitration Enable" as the last command prior to MI_BATCH_END in the BB_PER_CTX_PTR buffer of every context submitted. Note that RCS_INDIRECT_CTX_OFFSET could be set to default value or any other legitimate value as per the programming notes of the register definition. Arbitration disabled by programming MI_ARB_ON_OFF (Arbitration Disabled) in RCS_INDIRECT_CTX buffer. Arbitration enabled by programming MI_ARB_ON_OFF (Arbitration Enabled) as the last command prior to MI_BATCH_BUFFER_END in BB_PER_CTX_PTR buffer. Additional Note: This WA need not be applied when it is guaranteed for no preemption to occur during execution of GPGPU workload. Preemption of GPGPU workload can be avoided by Bracketing the GPGPU workload with MI_ARB_ON_OFF (Arbitration Disable) and MI_ARB_ON_OFF (Arbitration Enable) command. MI_ARB_ON_OFF is a privileged command and can only be programmed in ring buffer or in privileged batch buffer (batch buffer in GGTT memory). Pending execlist submitted must not trigger preemption of the ongoing GPGPU workload due to following reasons First context of the pending execlist submitted is not the same as the ongoing GPGPU context. Force restore bit set for the submitted pending execlist.

Workaround:

To work around a known HW issue, SW must do the below Programming Sequence prior to programming MI_BATCH_BUFFER_END command in BB_PER_CTX_PTR. SW must ensure both MI_LOAD_REGISTER_REG and MI_BATCH_BUFFER_END commands mentioned in the below sequence are placed in the same cacheline of memory.

1. MI_LOAD_REGISTER_IMM: 0x00800000 à 0x20C0
2. MI_ATOMIC
 - a. Set "CS STALL" (Dword0[17])
 - b. "Return Data Control" enabled (Dword0[16])
 - c. "ATOMIC OPCODE" set to LOAD operation (Dword0[15:8]= 0x4)
 - d. "Memory Address" set to scratch space in GFX memory.
 - e. "Operand1 Data Dword 0" must be programmed to 0x0080_0080
3. MI_LOAD_REGISTER_MEM
 - a. Set "Async Mode Enable" (Dword0[21])
 - b. "Memory Address" set to same as in MI_ATOMIC command above.
 - c. "Register Address" set to 0x20C0
4. MI_LOAD_REGISTER_REG: 0x215C à 0x215C
5. MI_BATCH_BUFFER_END // Note that there shouldn't be any commands programmed between step4 & step5 and also these commands must be placed in the same cacheline of memory.

Additional Note:

BB_PER_CTX_PTR - Batch Buffer Per Context Pointer

This workaround need not be applied when Resource Streamer (RS) is not enabled or when a Resource Streamer enabled context is guaranteed not to be preempted.

- Preemption of RS enabled workload can be avoided by
- Bracketing the RS enabled workload with MI_ARB_ON_OFF (Arbitration Disable) and MI_ARB_ON_OFF (Arbitration Enable) command. MI_ARB_ON_OFF is a privileged command and can only be programmed in ring buffer or in privileged batch buffer (batch buffer in GGTT memory).
- Pending execlist submitted must not trigger preemption of the ongoing RS enabled workload due to following reasons
 - First context of the pending execlist submitted is not the same as the ongoing RS enabled context.
 - Force restore bit set for the submitted pending execlist.

DWord	Bit	Description		
0	31:12	<p>Batch Buffer Per Context Address</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Format:</td> <td style="width: 20%; text-align: center;">U20</td> </tr> </table> <p>Pointer to the Context in memory to be executed as a batch.</p>	Format:	U20
	Format:	U20		
	11:2	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Format:</td> <td style="width: 20%; text-align: center;">MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
1	<p>RS Enabled Batch Buffer Per Context</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Format:</td> <td style="width: 20%; text-align: center;">U1</td> </tr> </table> <p>If set, the command stream will enable the RS to parse commands.</p> <table border="1" style="width: 100%; background-color: #e6f2ff;"> <tr> <td style="text-align: center;">Programming Notes</td> </tr> </table> <p>This must be set when programming the resource streamer pool commands (3DSTATE_BINDING_TABLE_POOL_ALLOC, 3DSTATE_GATHER_POOL_ALLOC, and 3DSTATE_DX9_CONSTANT_BUFFER_POOL_ALLOC) in order for the pool alloc fields to be valid in both the render engine and resource streamer.</p>	Format:	U1	Programming Notes
Format:	U1			
Programming Notes				
0	<p>Batch Buffer Per Context Valid</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Format:</td> <td style="width: 20%; text-align: center;">U1</td> </tr> </table> <p>If set, the command stream will execute the context from the Batch Buffer Per Context Address prior to the execution of actual submitted workloads.</p>	Format:	U1	
Format:	U1			

Batch Buffer Start Head Pointer Register

BB_START_ADDR - Batch Buffer Start Head Pointer Register			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	RenderCS		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Address:	02150h		
Address:	12150h-12153h		
Name:	Batch Buffer Start Head Pointer Register		
ShortName:	BB_START_ADDR_VCSUNIT0		
Address:	1A150h-1A153h		
Name:	Batch Buffer Start Head Pointer Register		
ShortName:	BB_START_ADDR_VECSUNIT		
Address:	1C150h-1C153h		
Name:	Batch Buffer Start Head Pointer Register		
ShortName:	BB_START_ADDR_VCSUNIT1		
Address:	22150h-22153h		
Name:	Batch Buffer Start Head Pointer Register		
ShortName:	BB_START_ADDR_BCSUNIT		
This register contains the address specified in the last MI_START_BATCH_BUFFER command.			
Programming Notes			
Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.			
DWord	Bit	Description	
0	31:2	Batch Buffer Start Head Pointer Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>GraphicsAddress[31:2]</td></tr></table> This field specifies the DWord-aligned Graphics Memory Address where the last initiated Batch Buffer starting address.	GraphicsAddress[31:2]
	GraphicsAddress[31:2]		
1	Preempted Batch Buffer RS Control Stop Flag Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>Flag</td></tr></table> This field specifies RS Control Stop Flag when a batch buffer is preempted. This is for HW internal use and should not be written by SW. This bit gets reset when RS_PREEMPTED field of RS_PREEMPT_STATUS is written Zero.	Flag	
Flag			

BB_START_ADDR - Batch Buffer Start Head Pointer Register

		<p>This bit is set by:</p> <ul style="list-style-type: none"> • Ctx restore of this bit • MI_RS_CONTROL_STOP (except for the ctx restore command) <p>This bit is cleared by:</p> <ul style="list-style-type: none"> • MI_RS_CONTROL_START • Any Batch start except resubmitted RS batch • A batch end that doesn't include preemption • Ctx save <p>Writing 0 to bit[0] of the RS STATUS register</p>	
0	Reserved	Format:	MBZ

Batch Buffer Start Head Pointer Register for Upper DWord

BB_START_ADDR_UDW - Batch Buffer Start Head Pointer Register for Upper DWord			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	RenderCS		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Address:	02170h		
Address:	12170h-12173h		
Name:	Batch Buffer Start Upper Head Pointer Register		
ShortName:	BB_START_ADDR_UDW_VCSUNIT0		
Address:	1A170h-1A173h		
Name:	Batch Buffer Start Upper Head Pointer Register		
ShortName:	BB_START_ADDR_UDW_VECSUNIT		
Address:	1C170h-1C173h		
Name:	Batch Buffer Start Upper Head Pointer Register		
ShortName:	BB_START_ADDR_UDW_VCSUNIT1		
Address:	22170h-22173h		
Name:	Batch Buffer Start Upper Head Pointer Register		
ShortName:	BB_START_ADDR_UDW_BCSUNIT		
This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space specified in the last MI_START_BATCH_BUFFER command.			
Programming Notes			
Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.			
DWord	Bit	Description	
0	31:16	Reserved Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td> </td></tr></table> MBZ	
15:0	Batch Buffer Start Head Pointer Upper DWORD Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td> </td></tr></table> GraphicsAddress[47:32] This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space for the last initiated Batch Buffer starting address.		

Batch Buffer State Register

BB_STATE - Batch Buffer State Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000 CHV, BSW	
Access:	RO	
Size (in bits):	32	
Address:	02110h-02113h	
Name:	Batch Buffer State Register	
ShortName:	BB_STATE_RCSUNIT	
Address:	12110h-12113h	
Name:	Batch Buffer State Register	
ShortName:	BB_STATE_VCSUNIT0	
Address:	1A110h-1A113h	
Name:	Batch Buffer State Register	
ShortName:	BB_STATE_VECSUNIT	
Address:	1C110h-1C113h	
Name:	Batch Buffer State Register	
ShortName:	BB_STATE_VCSUNIT1	
Address:	22110h-22113h	
Name:	Batch Buffer State Register	
ShortName:	BB_STATE_BCSUNIT	
<p>This register contains the attributes of the current batch buffer initiated from the Ring Buffer.</p> <p>This register should not be written by software. These fields should only get written by a context restore. Software should always set these fields via the MI_BATCH_BUFFER_START command when initiating a batch buffer. This register is saved and restored with context.</p>		
DWord	Bit	Description
0	31:8	Reserved
		Project: All
	Format: MBZ	
	7	Reserved
Project: All		
Source: BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS		
Format: MBZ		

BB_STATE - Batch Buffer State Register

7	Resource Streamer Enable <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Source:</td> <td>RenderCS</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>When this bit is set, the Resource Streamer will execute the batch buffer. When this bit is clear the Resource Streamer will not execute the batch buffer.</p>		Project:	CHV, BSW	Source:	RenderCS	Format:	U1											
Project:	CHV, BSW																		
Source:	RenderCS																		
Format:	U1																		
6	Reserved																		
6	2nd Level Buffer Security Indicator <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Source:</td> <td>VideoCS, VideoCS2</td> </tr> <tr> <td>Exists If:</td> <td>//VCS, VCS2</td> </tr> </table> <p>If set, VCS is fetching 2nd level batch commands from a PPGTT address space. If clear, GGTT. If execlists are enabled and this is set, the batch buffer is non-secure and cannot execute privileged commands nor access privileged (GGTT) memory. It will be accessed via the PPGTT. If clear, this batch buffer is secure and will be accessed via the GGTT. Note: When execlists are enabled this field reflects the effective security level and may not be the same as the Buffer Security Indicator written using MI_BATCH_BUFFER_START.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 45%;">Name</th> <th style="width: 40%;">Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>MIBUFFER_SECURE [Default]</td> <td>Located in GGTT memory</td> </tr> <tr> <td>1h</td> <td>MIBUFFER_NONSECURE</td> <td>Located in PPGTT memory</td> </tr> </tbody> </table>		Project:	CHV, BSW	Source:	VideoCS, VideoCS2	Exists If:	//VCS, VCS2	Value	Name	Description	0h	MIBUFFER_SECURE [Default]	Located in GGTT memory	1h	MIBUFFER_NONSECURE	Located in PPGTT memory		
Project:	CHV, BSW																		
Source:	VideoCS, VideoCS2																		
Exists If:	//VCS, VCS2																		
Value	Name	Description																	
0h	MIBUFFER_SECURE [Default]	Located in GGTT memory																	
1h	MIBUFFER_NONSECURE	Located in PPGTT memory																	
6	2nd Level Buffer Security Indicator <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Source:</td> <td>BlitterCS, VideoEnhancementCS</td> </tr> <tr> <td>Exists If:</td> <td>//BCS, VECS</td> </tr> <tr> <td>Format:</td> <td>MI_2ndBufferSecurityType</td> </tr> </table> <p>If set, VECS is fetching 2nd level batch commands from a PPGTT address space. If clear, GGTT. If execlists are enabled and this is set, the batch buffer is non-secure and cannot execute privileged commands nor access privileged (GGTT) memory. It will be accessed via the PPGTT. If clear, this batch buffer is secure and will be accessed via the GGTT.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 45%;">Name</th> <th style="width: 40%;">Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>MIBUFFER_SECURE [Default]</td> <td>Located in GGTT memory</td> </tr> <tr> <td>1h</td> <td>MIBUFFER_NONSECURE</td> <td>Located in PPGTT memory</td> </tr> </tbody> </table> <div style="border: 1px solid black; padding: 5px; text-align: center; margin-top: 10px;"> Programming Notes </div> <p>When execlists are enabled, this field reflects the effective security level and may not be the same as the Buffer Security Indicator written using MI_BATCH_BUFFER_START.</p>		Project:	CHV, BSW	Source:	BlitterCS, VideoEnhancementCS	Exists If:	//BCS, VECS	Format:	MI_2ndBufferSecurityType	Value	Name	Description	0h	MIBUFFER_SECURE [Default]	Located in GGTT memory	1h	MIBUFFER_NONSECURE	Located in PPGTT memory
Project:	CHV, BSW																		
Source:	BlitterCS, VideoEnhancementCS																		
Exists If:	//BCS, VECS																		
Format:	MI_2ndBufferSecurityType																		
Value	Name	Description																	
0h	MIBUFFER_SECURE [Default]	Located in GGTT memory																	
1h	MIBUFFER_NONSECURE	Located in PPGTT memory																	

BB_STATE - Batch Buffer State Register		
5	Address Space Indicator	
	Project:	CHV, BSW
	Note: This field reflects the effective address space indicator security level and may not be the same as the Address Space Indicator written using MI_BATCH_BUFFER_START.	
	Value	Name
	Description	
0h	GGTT [Default]	This Batch buffer is located in GGTT memory and is privileged
1h	PPGTT	This Batch buffer is located in PPGTT memory and is non-privileged.
4	Reserved	
4	Reserved	
	Project:	All
	Source:	BlitterCS
	Exists If:	//BCS
	Format:	MBZ
3:0	Reserved	
	Project:	All
	Format:	MBZ

Batch Buffer Upper Head Pointer Preemption Register

BB_PREEMPT_ADDR_UDW - Batch Buffer Upper Head Pointer Preemption Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	0216Ch-0216Fh			
Name:	Batch Buffer Upper Head Pointer Preemption Register			
ShortName:	BB_PREEMPT_ADDR_UDW_RCSUNIT			
Address:	1216Ch-1216Fh			
Name:	Batch Buffer Upper Head Pointer Preemption Register			
ShortName:	BB_PREEMPT_ADDR_UDW_VCSUNIT0			
Address:	1A16Ch-1A16Fh			
Name:	Batch Buffer Upper Head Pointer Preemption Register			
ShortName:	BB_PREEMPT_ADDR_UDW_VECSUNIT			
Address:	1C16Ch-1C16Fh			
Name:	Batch Buffer Upper Head Pointer Preemption Register			
ShortName:	BB_PREEMPT_ADDR_UDW_VCSUNIT1			
Address:	2216Ch-2216Fh			
Name:	Batch Buffer Upper Head Pointer Preemption Register			
ShortName:	BB_PREEMPT_ADDR_UDW_BCSUNIT			
<p>This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the last preempted batch buffer. This register follows the same rules as the BB_PREEMPT_ADDR register.</p>				
Programming Notes				
Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.				
DWord	Bit	Description		
0	31:16	Reserved Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td> </td><td>MBZ</td></tr></table>		MBZ
		MBZ		
15:0	Batch Buffer Head Pointer Upper DWORD Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td> </td><td>GraphicsAddress[47:32]</td></tr></table> This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the last preempted batch buffer.		GraphicsAddress[47:32]	
	GraphicsAddress[47:32]			

Batch Buffer Upper Head Pointer Register

BB_ADDR_UDW - Batch Buffer Upper Head Pointer Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Access:	RO			
Size (in bits):	32			
Address:	02168h-0216Bh			
Name:	Batch Buffer Upper Head Pointer Register			
ShortName:	BB_ADDR_UDW_RCSUNIT			
Address:	12168h-1216Bh			
Name:	Batch Buffer Upper Head Pointer Register			
ShortName:	BB_ADDR_UDW_VCSUNIT0			
Address:	1A168h-1A16Bh			
Name:	Batch Buffer Upper Head Pointer Register			
ShortName:	BB_ADDR_UDW_VECSUNIT			
Address:	1C168h-1C16Bh			
Name:	Batch Buffer Upper Head Pointer Register			
ShortName:	BB_ADDR_UDW_VCSUNIT1			
Address:	22168h-2216Bh			
Name:	Batch Buffer Upper Head Pointer Register			
ShortName:	BB_ADDR_UDW_BCSUNIT			
<p>This register contains the current Upper DWord of Graphics Memory Address of the last-initiated batch buffer.</p> <p>Programming Restriction: This register should NEVER be programmed by driver. This is for HW internal use only.</p>				
DWord	Bit	Description		
0	31:16	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
15:0	<p>Batch Buffer Head Pointer Upper DWORD</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td style="width: 70%;">GraphicsAddress[47:32]</td> </tr> </table> <p>This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space where the last initiated Batch Buffer is currently fetching commands. If no batch buffer is currently active, the Valid bit in BB_ADDR will be 0 and this field is meaningless.</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			

BCS_PREEMPTION_HINT

BCS_PREEMPTION_HINT - BCS_PREEMPTION_HINT											
Register Space:	MMIO: 0/2/0										
Project:	CHV, BSW										
Source:	BlitterCS										
Default Value:	0x00000000										
Access:	R/W										
Size (in bits):	32										
Address:	224BCh										
<p>This register contains the Head pointer offset in to the Ring Buffer or the Dword aligned Graphics address in to the Batch Buffer corresponding to either MI_ARB_CHECK called Preemption Hint Address. When Preemption Hint Address is enabled, BCS will honor UHPTR only on parsing MI_ARB_CHK at Preemption Hint Address.</p> <p>This register contains the Head pointer offset into the Ring Buffer or the Dword aligned Graphics address into the Batch Buffer corresponding to the below listed commands in execlist mode of operation</p> <ul style="list-style-type: none"> MI_ARB_CHECK MI_WAIT_FOR_EVENT MI_SEMAPHORE_WAIT 											
Programming Notes											
<p>Programming Restriction: This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of UHPTR being sampled by a given MI_ARB_CHECK in command stream. Programmer has to ensure that BCS Preemption Hint register gets programmed before UHPTR is programmed and well before BCS crosses the corresponding execution point. Preemption hint for both RingBuffer and Batch Buffer can't be enabled simultaneously.</p>											
DWord	Bit	Description									
0	31:2	Preempted Hint Address									
		<table border="1"> <tr> <td>Format:</td> <td>U30</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[31:2]</td> </tr> </table> <p>This field contains the Head offset in to the Ring Buffer when Preemption Hint is set to Ring Buffer and Dword aligned Graphics Address in to the batch buffer when Preemption Hint is set to Batch Buffer.</p>	Format:	U30	Format:	GraphicsAddress[31:2]					
Format:	U30										
Format:	GraphicsAddress[31:2]										
1	1	Batch Buffer Preemption Hint									
		Format: Enable									
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disabled</td> <td>Preemption hint is disabled in batch buffer.</td> </tr> <tr> <td>1h</td> <td>Enabled</td> <td>Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Batch Buffer.</td> </tr> </tbody> </table>	Value	Name	Description	0h	Disabled	Preemption hint is disabled in batch buffer.	1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Batch Buffer.
		Value	Name	Description							
0h	Disabled	Preemption hint is disabled in batch buffer.									
1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Batch Buffer.									

BCS_PREEMPTION_HINT - BCS_PREEMPTION_HINT		
0	Ring Preemption Hint	
	Format:	Enable
	Value	Name
	Description	
0h	Disable	Preemption hint is disabled in ring buffer.
1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Ring Buffer.

BCS_PREEMPTION_HINT_UDW

BCS_PREEMPTION_HINT_UDW - BCS_PREEMPTION_HINT_UDW				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	BlitterCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	224C8h			
<p>This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the Batch Buffer corresponding to MI_ARB_CHECK command called Preemption Hint Address.</p>				
Programming Notes				
<p>Programming Restriction: This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of UHPTR being sampled by a given MI_ARB_CHK in command stream.</p>				
DWord	Bit	Description		
0	31:16	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
15:0	<p>Preempted Hint Address Upper DWORD</p> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>This field contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the batch buffer when Preemption Hint is set to Batch Buffer. This field is not valid when Preemption Hint is set to Ring Buffer.</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			

BCS Active Upper Head Pointer Register

BCS_ACTHD_UDW - BCS Active Upper Head Pointer Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BlitterCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	2205Ch	
This register contains the Head "Pointer" (4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space) of the currently-active batch buffer.		
DWord	Bit	Description
0	31:16	Reserved
		Format: MBZ
	15:0	Head Pointer Upper DWORD
		Default Value: 0h
Format: GraphicsAddress[47:32]		
4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space corresponding to the Head Pointer of the currently-active batch buffer.		

BCS Context ID Preemption Hint

BCS_CTXID_PREEMPTION_HINT - BCS Context ID Preemption Hint				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	BlitterCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	224CCh			
<p>This register contains the Context ID of a context in execlist mode of operation. In execlist mode of operation BCS_PREEMPTION_HINT registers are looked at by Blitter Command Streamer on executing a context having Context ID that matches with the contents of this register. This register contents are valid and looked at only in execlist mode of operation.</p>				
Programming Notes				
<p>This register should NEVER be programmed in functional mode, this must be used only in validation mode to achieve deterministic preemption behavior in execlist mode of operation.</p>				
DWord	Bit	Description		
0	31:0	<p>Context ID Preemption Hint</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="text-align: center;">U32</td> </tr> </table> <p>If 0 this field has no effect. If nonzero it indicates the only context ID that can be preempted when execlists are enabled. A preemption attempt when the context ID of the currently executing ring context does not match this field will be ignored.</p>	Format:	U32
Format:	U32			

BCS Context Sizes

BCS_CXT_SIZE - BCS Context Sizes								
Register Space:	MMIO: 0/2/0							
Project:	CHV, BSW							
Source:	BlitterCS							
Default Value:	0x00000A05 CHV, BSW							
Access:	Read/32 bit Write Only							
Size (in bits):	32							
Address:	221A8h							
DWord	Bit	Description						
0	31:13	Reserved						
		Project: All						
		Format: MBZ						
	12:8	BCS Context Size						
		Project: All						
		Format: U5						
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>Ah</td> <td>[Default]</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Value	Name	Project	Ah	[Default]	CHV, BSW
		Value	Name	Project				
	Ah	[Default]	CHV, BSW					
	Reserved							
	Project: All							
	Format: MBZ							
	7:5	Reserved						
		Project: All						
		Format: MBZ						
		Reserved						
Project: All								
4:0	Execlist Context Size							
	Project: CHV, BSW							
	Format: U5							
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>5h</td> <td>[Default]</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Value	Name	Project	5h	[Default]	CHV, BSW	
	Value	Name	Project					
5h	[Default]	CHV, BSW						
Reserved								
Project: All								
Format: MBZ								

BCS Context Timestamp Count

BCS_CTX_TIMESTAMP - BCS Context Timestamp Count				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	BlitterCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	223A8h			
<p>This register provides a mechanism to obtain cumulative run time of a GPU context on HW. This register gets context save/restored on a context switch. SW must reset this register on very first submission of a context to HW, then afterwards gets context save/restored maintaining the cumulative run time of the corresponding context. Note that the value of this register can be obtained in a 3D pipeline-synchronous fashion without a pipeline flush by using the PIPE_CONTROL command. See 3D Geometry Pipeline in the "3D and Media" volume. This register (effectively) counts at a constant frequency by adjusting the increment amount according to the actual reference clock frequency. SW therefore does not need to know the reference clock frequency. This register gets reset on an engine reset.</p> <p>This register is context save restore on a context switch.</p>				
DWord	Bit	Description		
0	31:0	<p>Timestamp Value</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>This register increments for every 80 ns of time.</p>	Format:	U32
Format:	U32			

BCS Counter for the Blitter Engine

BCS_CNTR - BCS Counter for the Blitter Engine				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	BlitterCS			
Default Value:	0xFFFFFFFF			
Access:	R/W			
Size (in bits):	32			
Address:	22178h			
DWord	Bit	Description		
0	31:0	<p>Count Value</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Default Value:</td> <td style="text-align: right;">fffffffh</td> </tr> </table> <p>Writing a Zero value to this register starts the counting. Writing a Value of FFFF FFFF to this counter stops the counter.</p>	Default Value:	fffffffh
Default Value:	fffffffh			

BCS Error Identity Register

BCS_EIR - BCS Error Identity Register													
Register Space:	MMIO: 0/2/0												
Project:	CHV, BSW												
Source:	BlitterCS												
Default Value:	0x00000000												
Access:	R/WC												
Size (in bits):	32												
Address:	220B0h												
<p>The EIR register contains the persistent values of Hardware-Detected Error Condition bits. Any bit set in this register will cause the Master Error bit in the ISR to be set. The EIR register is also used by software to clear detected errors (by writing a '1' to the appropriate bit(s) except for the unrecoverable bits described).</p>													
DWord	Bit	Description											
0	31:16	Reserved											
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ							
Project:	All												
Format:	MBZ												
	15:0	Error Identity Bits											
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Array of Error condition bits See Table 1 5. Hardware-Detected Error Bits</td> </tr> </table> <p>This register contains the persistent values of ESR error status bits that are unmasked via the EMR register. The logical OR of all (defined) bits in this register is reported in the Master Error bit of the Interrupt Status Register. To clear an error condition, software must first clear the error by writing a '1' to the appropriate bit(s) in this field. If required, software should then proceed to clear the Master Error bit of the IIR.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>[Default]</td> <td></td> </tr> <tr> <td>1h</td> <td>Error occurred</td> <td>Error occurred</td> </tr> </tbody> </table>	Project:	All	Format:	Array of Error condition bits See Table 1 5. Hardware-Detected Error Bits	Value	Name	Description	0h	[Default]		1h
Project:	All												
Format:	Array of Error condition bits See Table 1 5. Hardware-Detected Error Bits												
Value	Name	Description											
0h	[Default]												
1h	Error occurred	Error occurred											
Programming Notes													
<p>Writing a '1' to a set bit will cause that error condition to be cleared. However, the Instruction Error bit (Bit 0) cannot be cleared except by reset (i.e., it is a fatal error).</p>													

BCS Error Mask Register

BCS_EMR - BCS Error Mask Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	BlitterCS			
Default Value:	0xFFFFFFFF CHV, BSW			
Access:	R/W			
Size (in bits):	32			
Address:	220B4h			
<p>The EMR register is used by software to control which Error Status Register bits are "masked" or "unmasked". "Unmasked" bits will be reported in the EIR, thus setting the Master Error ISR bit and possibly triggering a CPU interrupt, and will persist in the EIR until cleared by software. "Masked" bits will not be reported in the EIR and therefore cannot generate Master Error conditions or CPU interrupts.</p> <p>Undefined or reserved bits in the Hardware Detected Error Bit Table will always return a read value of '1'</p>				
DWord	Bit	Description		
0	31:16	Reserved		
		Default Value:	FFFFh	
		Project:	CHV, BSW	
			Format:	Must Be One
	15:0	Error Mask Bits		
		Project:	All	
		Format:	Array of error condition mask bits See Table 1 5. Hardware-Detected Error Bits	
This register contains a bit mask that selects which error condition bits (from the ESR) are reported in the EIR.				
Value		Name	Description	
0000h	Not Masked	Will be reported in the EIR		
FFFFh	Masked [Default]	Will not be reported in the EIR		

BCS Error Status Register

BCS_ESR - BCS Error Status Register									
Register Space:	MMIO: 0/2/0								
Project:	CHV, BSW								
Source:	BlitterCS								
Default Value:	0x00000000								
Access:	RO								
Size (in bits):	32								
Address:	220B8h								
<p>The ESR register contains the current values of all Hardware-Detected Error condition bits (these are all by definition "persistent"). The EMR register selects which of these error conditions are reported in the persistent EIR (i.e., set bits must be cleared by software) and thereby causing a Master Error interrupt condition to be reported in the ISR.</p>									
DWord	Bit	Description							
0	31:16	Reserved							
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ			
Project:	All								
Format:	MBZ								
0	15:0	Error Status Bits							
		Project: All							
		Format: Array of error condition bits See Table 1 5. Hardware-Detected Error Bits							
		This register contains the non-persistent values of all hardware-detected error condition bits.							
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>[Default]</td> <td></td> </tr> <tr> <td>1h</td> <td>Error Condition Detected</td> <td>Error Condition detected</td> </tr> </tbody> </table>	Value	Name	Description	0h	[Default]		1h
Value	Name	Description							
0h	[Default]								
1h	Error Condition Detected	Error Condition detected							

BCS Execute Condition Code Register

BCS_EXCC - BCS Execute Condition Code Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	BlitterCS			
Default Value:	0x00000000			
Access:	R/W, RO			
Size (in bits):	32			
Trusted Type:	1			
Address:	22028h			
<p>This register contains user defined and hardware generated conditions that are used by MI_WAIT_FOR_EVENT commands. An MI_WAIT_FOR_EVENT instruction excludes the executing ring from arbitration if the selected event evaluates to a 1, while instruction is discarded if the condition evaluates to a 0. Once excluded, a ring is enabled into arbitration when the selected condition evaluates to a 0. This register also contains control for the invalidation of indirect state pointers on context restore.</p>				
DWord	Bit	Description		
0	31:16	Mask Bits <table border="1"> <tr> <td>Format:</td> <td>Mask[15:0]</td> </tr> </table> <p>These bits serves as a write enable for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.</p>	Format:	Mask[15:0]
		Format:	Mask[15:0]	
	15	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
	14	Context Wait for V-blank on Pipe-C <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This field when set indicates the corresponding context has executed MI_WAIT_FOR_EVENT with "Display Pipe C Vertical Blank Wait Enable" set. This is an internal HW flag and should not be accessed by SW.</p>	Project:	CHV, BSW
Project:	CHV, BSW			
13	Context Wait for V-blank on Pipe-B <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This field when set indicates the corresponding context has executed MI_WAIT_FOR_EVENT with "Display Pipe B Vertical Blank Wait Enable" set. This is an internal HW flag and should not be accessed by SW.</p>	Project:	CHV, BSW	
Project:	CHV, BSW			
12	Context Wait for V-blank on Pipe-A <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This field when set indicates the corresponding context has executed MI_WAIT_FOR_EVENT with "Display Pipe A Vertical Blank Wait Enable" set. This is an internal HW flag and should not be accessed by SW.</p>	Project:	CHV, BSW	
Project:	CHV, BSW			

BCS_EXCC - BCS Execute Condition Code Register		
	11:5	Reserved
		Format: MBZ
	4:0	Reserved
		Project: CHV, BSW
		Format: MBZ

BCS General Purpose Register

BCS_GPR - BCS General Purpose Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	BlitterCS			
Default Value:	0x00000000, 0x00000000			
Access:	R/W			
Size (in bits):	64			
Address:	22600h-2267Fh			
<p>This is a general purpose register bank of sixteen 64-bit registers, used as temporary storage by the MI_MATH command to do ALU operations.</p>				
Programming Notes				
<p>Any operation that initiates a read to register 0x2266C will return the value of 0x2260c register. This does not include context save or MI_MATH command operation.</p>				
DWord	Bit	Description		
0	63:0	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			

BCS Hardware Status Mask Register

BCS_HWSTAM - BCS Hardware Status Mask Register								
Register Space:	MMIO: 0/2/0							
Project:	CHV, BSW							
Source:	BlitterCS							
Default Value:	0xFFFFFFFF							
Access:	R/W							
Size (in bits):	32							
Trusted Type:	1							
Address:	22098h							
Access: RO for Reserved Control bits								
<p>The HWSTAM register has the same format as the Interrupt Control Registers. The bits in this register are "mask" bits that prevent the corresponding bits in the Interrupt Status Register from generating a "Hardware Status Write" (PCI write cycle). Any unmasked interrupt bit (HWSTAM bit set to 0) will allow the Interrupt Status Register to be written to the ISR location (within the memory page specified by the Hardware Status Page Address Register) when that Interrupt Status Register bit changes state.</p>								
Programming Notes								
To write the interrupt to the HWSP, the corresponding IMR bit must also be clear (enabled). At most 1 bit can be unmasked at any given time.								
DWord	Bit	Description						
0	31:0	<p>Hardware Status Mask Register</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>FFFFFFFFh</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Array of Masks</td> </tr> </table> <p>refer to Table 5-1 in Interrupt Control Register section for bit definitions</p>	Default Value:	FFFFFFFFh	Project:	All	Format:	Array of Masks
Default Value:	FFFFFFFFh							
Project:	All							
Format:	Array of Masks							

BCS IDLE Max Count

BCS_PWRCTX_MAXCNT - BCS IDLE Max Count		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BlitterCS	
Default Value:	0x00000040 CHV, BSW	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	22054h	
This register contains the time in 0.64us to wait before telling power management hardware the render pipe is IDLE		
DWord	Bit	Description
0	31:20	Reserved
		Project: All
	Format: MBZ	
	19:0	Reserved

BCS Idle Switch Delay

BCS_IDLEDLY - BCS Idle Switch Delay		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BlitterCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	2223Ch	
<p>The IDLEDLY register contains an Idle Delay field which specifies the minimum number of microseconds allowed for command streamer to wait before a context is switched out leading to IDLE state in Execlist mode, i.e following this context switch there is no active element available in HW to execute.</p> <p>A default value of 0, means that by default, there is no restriction to wait on a context switch leading to IDLE. This register has no significance when execlists are not enabled.</p>		
DWord	Bit	Description
0	31:21	Reserved
		Project: All
		Format: MBZ
	20:0	IDLE Delay
		Project: All
		Format: U21
		Minimum number of micro-seconds allowed

BCS Instruction Parser Mode Register

BCS_INSTPM - BCS Instruction Parser Mode Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BlitterCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	220C0h	
Desc		
DWord	Bit	Description
0	31:16	Mask Bits
		Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:11	Reserved
		Project: All Format: MBZ
	10	Reserved
	9	Reserved
		Project: CHV, BSW Format: MBZ
	8:7	Reserved
		Project: All Format: MBZ
	6:5	Reserved
		Project: CHV, BSW Format: MBZ
	4:0	Reserved
Project: All Format: MBZ		

BCS Interrupt Mask Register

BCS_IMR - BCS Interrupt Mask Register																		
Register Space:	MMIO: 0/2/0																	
Project:	CHV, BSW																	
Source:	BlitterCS																	
Default Value:	0xFFFFFFFF																	
Access:	R/W																	
Size (in bits):	32																	
Address:	220A8h																	
<p>The IMR register is used by software to control which Interrupt Status Register bits are "masked" or "unmasked". "Unmasked" bits will be reported in the IIR, possibly triggering a CPU interrupt, and will persist in the IIR until cleared by software. "Masked" bits will not be reported in the IIR and therefore cannot generate CPU interrupts.</p>																		
DWord	Bit	Description																
0	31:0	<p>Interrupt Mask Bits</p> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Array of interrupt mask bits Refer to Table 5-1 in Interrupt Control Register section for bit definitions</td> </tr> </table> <p>This field contains a bit mask which selects which interrupt bits (from the ISR) are reported in the IIR.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">FFFF FFFFh</td> <td style="text-align: center;">[Default]</td> <td></td> </tr> <tr> <td style="text-align: center;">0h</td> <td style="text-align: center;">Not Masked</td> <td>Will be reported in the IIR</td> </tr> <tr> <td style="text-align: center;">1h</td> <td style="text-align: center;">Masked</td> <td>Will not be reported in the IIR</td> </tr> </tbody> </table>	Project:	All	Format:	Array of interrupt mask bits Refer to Table 5-1 in Interrupt Control Register section for bit definitions	Value	Name	Description	FFFF FFFFh	[Default]		0h	Not Masked	Will be reported in the IIR	1h	Masked	Will not be reported in the IIR
Project:	All																	
Format:	Array of interrupt mask bits Refer to Table 5-1 in Interrupt Control Register section for bit definitions																	
Value	Name	Description																
FFFF FFFFh	[Default]																	
0h	Not Masked	Will be reported in the IIR																
1h	Masked	Will not be reported in the IIR																

BCS Mode Register for Software Interface

BCS_MI_MODE - BCS Mode Register for Software Interface										
Register Space:	MMIO: 0/2/0									
Project:	CHV, BSW									
Source:	BlitterCS									
Default Value:	0x00000200 CHV, BSW									
Access:	R/W									
Size (in bits):	32									
Address:	2209Ch-2209Fh									
The MI_MODE register contains information that controls software interface aspects of the command parser.										
DWord	Bit	Description								
0	31:16	Masks A 1 in a bit in this field allows the modification of the corresponding bit in Bits 15:0								
	15	Suspend Flush								
		Project:	All							
		Mask:	MMIO(0x209c)#31							
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>No Delay</td> <td>HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well</td> </tr> <tr> <td>1h</td> <td>Delay Flush</td> <td>Suspend flush is active</td> </tr> </tbody> </table>	Value	Name	Description	0h	No Delay	HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well	1h	Delay Flush
	Value	Name	Description							
	0h	No Delay	HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well							
	1h	Delay Flush	Suspend flush is active							
	14:12	Reserved Read/Write								
	11	Invalidate UHPTR enable If bit set H/W clears the valid bit of BCS_UHPTR (4134h, bit 0) when current active head pointer is equal to UHPTR.								
10	Atomic Read Return for MI_COPY_MEM_MEM									
	Project:	CHV, BSW								
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disable [Default]</td> <td>Hardware does a regular memory fence write to complete the write to the destination address before moving to the next instruction.</td> </tr> <tr> <td>1h</td> <td>Enable</td> <td>Hardware does Atomic Move with Read Return to complete the write to the destination address before moving to the next instruction.</td> </tr> </tbody> </table>	Value	Name	Description	0h	Disable [Default]	Hardware does a regular memory fence write to complete the write to the destination address before moving to the next instruction.	1h	Enable	Hardware does Atomic Move with Read Return to complete the write to the destination address before moving to the next instruction.
	Value	Name	Description							
0h	Disable [Default]	Hardware does a regular memory fence write to complete the write to the destination address before moving to the next instruction.								
1h	Enable	Hardware does Atomic Move with Read Return to complete the write to the destination address before moving to the next instruction.								

BCS_MI_MODE - BCS Mode Register for Software Interface

9	<p>Ring Idle (Read Only Status Bit) Writes to this bit are not allowed.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Parser not idle</td> </tr> <tr> <td>1</td> <td>Parser idle [Default]</td> </tr> </tbody> </table>	Value	Name	0	Parser not idle	1	Parser idle [Default]
Value	Name						
0	Parser not idle						
1	Parser idle [Default]						
8	<p>Stop Ring Software must set this bit to force the Ring and Command Parser to Idle. Software must read a 1 in Ring Idle bit after setting this bit to ensure that the hardware is idle. <i>Software must clear this bit for Ring to resume normal operation.</i></p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Normal Operation [Default]</td> </tr> <tr> <td>1</td> <td>Parser is turned off</td> </tr> </tbody> </table>	Value	Name	0	Normal Operation [Default]	1	Parser is turned off
Value	Name						
0	Normal Operation [Default]						
1	Parser is turned off						
7:2	<p>Reserved Read/Write</p>						
1	<p>Bypass Fence Write If set, this bit will bypass all writes during flushes, independent of programming. This includes post-sync op bits, the implicit TLB invalidate write (set in GFX_MODE[13]), and sync flush fences. <i>Note this is only intended for work-arounds</i></p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Normal Operation</td> </tr> <tr> <td>1</td> <td>Bypass</td> </tr> </tbody> </table>	Value	Name	0	Normal Operation	1	Bypass
Value	Name						
0	Normal Operation						
1	Bypass						
0	<p>Reserved Read/Write</p>						

BCS PPGTT Directory Cacheline Valid Register

BCS_PP_DCLV - BCS PPGTT Directory Cacheline Valid Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	BlitterCS			
Default Value:	0x00000000, 0x00000000			
Access:	R/W			
Size (in bits):	64			
Address:	22220h			
<p>Default Value = 0h</p> <p>This register controls update of the on-chip PPGTT Directory Cache during a context restore. Bits that are set will trigger the load of the corresponding 16 directory entry group. This register is restored with context (prior to restoring the on-chip directory cache itself). This register is also restored when switching to a context whose LRCA matches the current CCID if the Force PD Restore bit is set in the context descriptor.</p> <p>The context image of this register must be updated and maintained by SW; SW should not normally need to read this register.</p> <p>This register can also effectively be used to limit the size of a processes' virtual address space. Any access by a process that requires a PD entry in a set that is not enabled in this register will cause a fatal error, and no fetch of the PD entry will be attempted.</p>				
DWord	Bit	Description		
0	63:32	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
31:0	<p>PPGTT Directory Cache Restore</p> <table border="1"> <tr> <td>Format:</td> <td>Enable[32]</td> </tr> </table> <p>[1..32] 16 entries If set, the [1st..32nd] 16 entries of the directory cache are considered valid and will be brought in on context restore. If clear, these entries are considered invalid and fetch of these entries will not be attempted.</p>	Format:	Enable[32]	
Format:	Enable[32]			

BCS Primary DMA Engine Fetch Upper Address

BCS_DMA_FADD_P_UDW - BCS Primary DMA Engine Fetch Upper Address				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	BlitterCS			
Default Value:	0x00000000			
Access:	RO			
Size (in bits):	32			
Address:	22060h			
<p>This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the instruction being fetched by the Primary DMA engine. This register contents are valid only when Batch Buffer is active.</p>				
DWord	Bit	Description		
0	31:16	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
15:0	<p>Current DMA Address Upper DWORD</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Format:</td> <td style="width: 70%;">GraphicsAddress[47:32]</td> </tr> </table> <p>This field contains 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the batch buffer that the "Primary" instruction parser DMA engine is currently accessing (fetching). Note that this address will typically lead the Head offset (as instructions must be fetched before execution).</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			

BCS Reported Timestamp Count

BCS_TIMESTAMP - BCS Reported Timestamp Count		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BlitterCS	
Default Value:	0x00000000, 0x00000000	
Access:	RO. This register is not set by the context restore.	
Size (in bits):	64	
Address:	22358h	
<p>This register provides an elapsed real-time value that can be used as a timestamp. This register is not reset by a graphics reset. It will maintain its value unless a full chipset reset is performed. Note: This timestamp register reflects the value of the PCU TSC. The PCU TSC counts 10ns increments; this timestamp reflects bits 38:3 of the TSC (i.e. 80ns granularity, rolling over every 1.5 hours).</p>		
DWord	Bit	Description
0	63:36	Reserved
		Project: All
		Format: MBZ
	35:0	Timestamp Value
		Project: All
		Format: U36
This register toggles every 80 ns. The upper 28 bits are zero.		

BCS Reset Control Register

BCS_RESET_CTRL - BCS Reset Control Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BlitterCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	220D0h	
This register is to be used to control soft reset.		
DWord	Bit	Description
0	31:16	Mask Bits
		Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>Mask[15:0]</td></tr></table> Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	Mask[15:0]	
	15:2	Reserved
Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>MBZ</td></tr></table>		MBZ
MBZ		
1	Ready for Reset	
	Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>U1</td></tr></table> When set indicates blitter engine is ready for reset. This bit gets cleared on engine reset or when Soft Reset In progress is cleared.	U1
U1		
0	Request Reset	
	Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>U1</td></tr></table> When set, this bit indicates that SW wishes to reset the blitter engine. On seeing this bit set, Command Streamer will take appropriate action and set Ready For Reset status bit. This bit gets cleared on engine reset.	U1
U1		

BCS Ring Buffer Next Context ID Register

BCS_RNCID - BCS Ring Buffer Next Context ID Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BlitterCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Address:	22198h-2219Fh	
This register contains the <i>next</i> ring context ID associated with the ring buffer.		
Programming Notes		
The current context (RCCID) register can be updated indirectly from this register on a context switch event. Note that the only time a context switch can occur is when MI_ARB_CHECK enables preemption or the current context runs dry (head pointer becomes equal to tail pointer).		
DWord	Bit	Description
0	63:0	Unnamed See Context Descriptor for BCS

BCS Semaphore Polling Interval on Wait

BCS_SEMA_WAIT_POLL - BCS Semaphore Polling Interval on Wait		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BlitterCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	2224Ch	
<p>The SEMA_WAIT_POLL register contains Poll Interval field which specifies the minimum number of microseconds allowed for command streamer to wait before re-fetching the data from the address mentioned in the MI_SEMAPHORE_WAIT command on WAIT Mode set to POLL until the condition is satisfied while the context is not switched out.</p> <p>When value of 0 is written the poll interval will be equal to the memory latency of the read completion.</p>		
DWord	Bit	Description
0	31:21	Reserved
		Project: All
		Format: MBZ
	20:0	Poll Interval
		Project: All
		Format: U21
		Minimum number of micro-seconds allowed

BCS SW Control

BCS_SWCTRL - BCS SW Control			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	BlitterCS		
Default Value:	0x00000000		
Access:	r/w		
Size (in bits):	32		
Trusted Type:	1		
Address:	22200h		
DWord	Bit	Description	
0	31:16	Mask	
		Access:	WO
		Format:	Mask
	15:4	Reserved	
		Project:	CHV, BSW
		Format:	MBZ
	3:2	Reserved	
		Project:	CHV, BSW
		Format:	MBZ
	1	Tile Y Destination	
		Project:	CHV, BSW
		Format:	U1
Programming this bit makes the HW treat all destination surfaces as Tile Y. This bit over-rides the setting of the destination format in the packet provided to the blitter command streamer. SW is required to flush the HW before changing the polarity of this bit. This bit is part of the context save/restore.			
0	Tile Y Source		
	Project:	CHV, BSW	
	Format:	U1	
	Programming this bit makes the HW treat all source surfaces as Tile Y. This bit over-rides the setting of the source format in the packet provided to the blitter command streamer. SW is required to flush the HW before changing the polarity of this bit. This bit is part of the context save/restore.		

BCS Watchdog Counter Threshold

BCS_CTR_THRSH - BCS Watchdog Counter Threshold						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	BlitterCS					
Default Value:	0x00150000					
Access:	R/W					
Size (in bits):	32					
Address:	2217Ch					
DWord	Bit	Description				
0	31:0	<p>Counter logic Threshold</p> <table border="1"> <tr> <td>Default Value:</td> <td>00150000h</td> </tr> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>This field specifies the threshold that the hardware checks against for the value of the blitter clock counter before generating an interrupt. The counter in hardware generates an interrupt when the threshold is reached, rolls over and starts counting again. The interrupt generated is the "Media Hang Notify" interrupt since this watchdog timer is intended primarily to remedy VLD hangs on the main pipeline.</p>	Default Value:	00150000h	Format:	U32
Default Value:	00150000h					
Format:	U32					

Bitstream Output Bit Count for the last Syntax Element Report Register

MFC_BITSTREAM_SE_BITCOUNT_SLICE - Bitstream Output Bit Count for the last Syntax Element Report Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	128D4h	
Name:	VDBOX1	
Valid Projects:	CHV, BSW	
<p>This register stores the count of number of bits in the bitstream for the last syntax element before padding. The bit count is before the byte-aligned alignment padding insertion, but includes the stop-one-bit. This register is part of the context save and restore.</p>		
DWord	Bit	Description
0	31:0	<p>MFC Bitstream Syntax Element Bit Count Total number of bits in the bitstream output before padding. This count is updated each time the internal counter is incremented.</p>

Bitstream Output Byte Count Per Slice Report Register

MFC_BITSTREAM_BYTECOUNT_SLICE - Bitstream Output Byte Count Per Slice Report Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	128D0h	
Valid Projects:	CHV, BSW	
This register stores the count of bytes of the bitstream output. This register is part of the context save and restore.		
DWord	Bit	Description
0	31:0	MFC Bitstream Byte Count Total number of bytes in the bitstream output from the encoder. This count is updated for every time the internal bitstream counter is incremented.

Bitstream Output Minimal Size Padding Count Report Register

MFC_AVC_MINSIZE_PADDING_COUNT - Bitstream Output Minimal Size Padding Count Report Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	12814h	
Name:	VDBOX1	
Valid Projects:	CHV, BSW	
<p>This register stores the count in bytes of minimal size padding insertion. It is primarily provided for statistical data gathering. This register is part of the context save and restore.</p>		
DWord	Bit	Description
0	31:0	<p>MFC AVC MinSize Padding Count</p> <p>Total number of bytes in the bitstream output contributing to minimal size padding operation. This count is updated each time when the padding count is incremented.</p>

Blitter Mode Register

BLT_MODE - Blitter Mode Register			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	BlitterCS		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Trusted Type:	1		
Address:	2229Ch		
DWord	Bit	Description	
0	31:16	Mask Bits	
		Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)	
	15	Execlist Enable	
		Default Value: 0h	
		Project: CHV, BSW	
		Mask: MMIO#31	
			When set, software can utilize the execlist registers to load a context into hardware. When this bit is clear the Execlist mechanism cannot be used. The ring must be loaded via MMIO access.
			Programming Notes
			This bit is not intended to be changed dynamically. Changing the value of this bit while rendering is in progress will have UNDEFINED results. This bit should be changed only after a full reset and before submitting any commands to the device
	14	Interrupt Steering Bit	
		Project: CHV, BSW	
		Format: U1	
		When set, Command Streamer sends interrupt messages to the SHIM of the ON CHIP Micro Controller through message channel. When reset, Command Streamer sends the interrupt messages to Display Engine as config writes on GAM interface.	
13:10	Reserved		
	Project: All		
	Format: MBZ		

BLT_MODE - Blitter Mode Register

9	Per-Process GTT Enable	
Project:	All	
Format:	Enable Per-Process GTT BS Mode Enable	
	Value	Name
	Description	
0h	PPGTT Disable [Default]	When clear, the Global GTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.
1h	PPGTT Enable	When set, the PPGTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.
Programming Notes		
This bit is used for enabling PPGTT access in Ring Buffer mode of scheduling. Privilege field in context descriptor states the same in Execlist Mode of scheduling. This field should be set before programming PDP0/1/2/3 registers in order to set the PPGTT translation of memory access.		
8	Reserved	
Project:	All	
7	64Bit Virtual Addressing Enable	
Project:	CHV, BSW	
Format:	Enable	
Per-Process GTT Enable		
	Value	Name
	Description	
0h	64Bit Virtual Addressing Disable [Default]	When clear indicates GFX operating in 32bit Virtual Addressing for PPGTT based memory access.
Programming Notes		
This bit is only valid when PPGTT is enabled in ring buffer mode of scheduling. Context Descriptor has a similar bit to control 64bit virtual addressing in execlist mode of scheduling. Irrespective of this field set or clear virtual addresses translated through GGTT are always 32Bit. This field should be programmed before enabling PPGTT access. When this field is not set or for GGTT virtual addresses, Graphics Address [47:32] field of any commands or register exercised by SW should be programmed to 0x0.		
64 Bit Virtual Addressing is not supported on CHV, BSW and must not be set.		
6:5	Reserved	
Project:	CHV, BSW	
4	Reserved	
Project:	CHV, BSW	

BLT_MODE - Blitter Mode Register				
3:1	Reserved			
	<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:
Project:	All			
Format:	MBZ			
0	Privilege Check Disable			
	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field when set, disables Privilege Violation checks on non-privileged batch buffers. When set Privileged commands are allowed to be executed from non-privileged batch buffers.</p>	Project:	CHV, BSW	Format:
Project:	CHV, BSW			
Format:	Enable			

Blitter TLB Control Register

BTCR - Blitter TLB Control Register			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0426Ch		
DWord	Bit	Description	
0	31:1	Reserved	
		Default Value:	00000000000000000000000000000000b
		Access:	RO
	0	Invalidate TLBs on the corresponding Engine	
	Default Value:	0b	
	Access:	R/W	
<p>SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs.</p> <p>This bit is self clear.</p>			

BLT Context Element Descriptor (High Part)

BLT_CTX_EDR_H - BLT Context Element Descriptor (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04504h	
DWord	Bit	Description
0	31:0	BLT Context Element Descriptor (High Part)
		Default Value: 00000000h
		Access: R/W

BLT Context Element Descriptor (Low Part)

BLT_CTX_EDR_L - BLT Context Element Descriptor (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000009	
Size (in bits):	32	
Address:	04500h	
DWord	Bit	Description
0	31:0	BLT Context Element Descriptor (Low Part)
		Default Value: 00000009h
		Access: R/W

BLT Context Element Descriptor (Low Part)

BLT_CTX_EDR_L - BLT Context Element Descriptor (Low Part)						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000009					
Size (in bits):	32					
Address:	04500h					
DWord	Bit	Description				
0	31:0	BLT Context Element Descriptor <table border="1"> <tr> <td>Default Value:</td> <td>00000009h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Default Value:	00000009h	Access:	R/W
Default Value:	00000009h					
Access:	R/W					

BLT PDP0/PML4/PASID Descriptor (High Part)

BLT_CTX_PDP0_H - BLT PDP0/PML4/PASID Descriptor (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0450Ch	
DWord	Bit	Description
0	31:0	BLT PDP0/PML4/PASID Descriptor (High Part)
		Default Value: 00000000h
		Access: R/W

BLT PDP0/PML4/PASID Descriptor (Low Part)

BLT_CTX_PDP0_L - BLT PDP0/PML4/PASID Descriptor (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04508h	
DWord	Bit	Description
0	31:0	BLT PDP0/PML4/PASID Descriptor (Low Part)
		Default Value: 00000000h
		Access: R/W

BLT PDP1 Descriptor Register (High Part)

BLT_CTX_PDP1_H - BLT PDP1 Descriptor Register (High Part)						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04514h					
DWord	Bit	Description				
0	31:0	BLT PDP1 Descriptor Register (High Part) <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

BLT PDP1 Descriptor Register (Low Part)

BLT_CTX_PDP1_L - BLT PDP1 Descriptor Register (Low Part)			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	04510h		
DWord	Bit	Description	
0	31:0	BLT PDP1 Descriptor Register (Low Part)	
		Default Value:	00000000h
		Access:	R/W

BLT PDP2 Descriptor Register (High Part)

BLT_CTX_PDP2_H - BLT PDP2 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0451Ch	
DWord	Bit	Description
0	31:0	BLT PDP2 Descriptor Register (High Part)
		Default Value: 00000000h
		Access: R/W

BLT PDP2 Descriptor Register (Low Part)

BLT_CTX_PDP2_L - BLT PDP2 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04518h	
DWord	Bit	Description
0	31:0	BLT PDP2 Descriptor Register (Low Part)
		Default Value: 00000000h
		Access: R/W

BLT PDP3 Descriptor Register (High Part)

BLT_CTX_PDP3_H - BLT PDP3 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04524h	
DWord	Bit	Description
0	31:0	BLT PDP3 Descriptor Register (High Part)
		Default Value: 00000000h
		Access: R/W

BLT PDP3 Descriptor Register (Low Part)

BLT_CTX_PDP3_L - BLT PDP3 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04520h	
DWord	Bit	Description
0	31:0	BLT PDP3 Descriptor Register (Low Part)
		Default Value: 00000000h
		Access: R/W

Boolean_Counter_B0

OAPERF_B0 - Boolean_Counter_B0				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	BSpec			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	02920h			
Valid Projects:	[CHV, BSW]			
<p>This register enables the current live value of performance counter B0 to be read. Since what conditions cause B0 to increment are defined by the programming of CECO-0/CECO-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.</p>				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U32</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32
Format:	U32			

Boolean_Counter_B1

OAPERF_B1 - Boolean_Counter_B1				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	BSpec			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	02924h			
Valid Projects:	[CHV, BSW]			
<p>This register enables the current live value of performance counter B1 to be read. Since what conditions cause B1 to increment are defined by the programming of CEC1-0/CEC1-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.</p>				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">U32</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32
Format:	U32			

Boolean_Counter_B2

OAPERF_B2 - Boolean_Counter_B2				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	BSpec			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	02928h			
Valid Projects:	[CHV, BSW]			
<p>This register enables the current live value of performance counter B2 to be read. Since what conditions cause B2 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.</p>				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">U32</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32
Format:	U32			

Boolean_Counter_B3

OAPERF_B3 - Boolean_Counter_B3				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	BSpec			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	0292Ch			
Valid Projects:	[CHV, BSW]			
<p>This register enables the current live value of performance counter B3 to be read. Since what conditions cause B3 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.</p>				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="text-align: center;">U32</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32
Format:	U32			

Boolean_Counter_B4

OAPERF_B4 - Boolean_Counter_B4				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	BSpec			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	02930h			
Valid Projects:	[CHV, BSW]			
<p>This register enables the current live value of performance counter B4 to be read. Since what conditions cause B4 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.</p>				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">U32</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32
Format:	U32			

Boolean_Counter_B5

OAPERF_B5 - Boolean_Counter_B5				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	BSpec			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	02934h			
Valid Projects:	[CHV, BSW]			
<p>This register enables the current live value of performance counter B5 to be read. Since what conditions cause B5 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.</p>				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">U32</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32
Format:	U32			

Boolean_Counter_B6

OAPERF_B6 - Boolean_Counter_B6				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	BSpec			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	02938h			
Valid Projects:	[CHV, BSW]			
<p>This register enables the current live value of performance counter B6 to be read. Since what conditions cause B6 to increment are defined by the programming of CECO-0/CECO-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.</p>				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">U32</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32
Format:	U32			

Boolean_Counter_B7

OAPERF_B7 - Boolean_Counter_B7				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	BSpec			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	0293Ch			
Valid Projects:	[CHV, BSW]			
<p>This register enables the current live value of performance counter B7 to be read. Since what conditions cause B7 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.</p>				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U32</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32
Format:	U32			

BTB Not Consumed By RCS

BTP_PRODUCE_COUNT - BTB Not Consumed By RCS		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	02480h	
<p>This register keeps track of the outstanding BTP produced by RS which are not yet consumed by Render Command Streamer. This register is part of the render context save and restore.</p>		
Programming Notes		
<p>This register should not be programmed by SW.</p>		
DWord	Bit	Description
0	31:0	<p>BTP Produce Count This register keeps track of the outstanding BTP produced by RS which are not yet consumed by Render Command Streamer. This register is part of the render context save and restore.</p>

BTP Commands Parsed By RCS

BTP_PARSE_COUNT - BTP Commands Parsed By RCS		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	02490h	
<p>This register keeps track of the BTP commands parsed by RCS prior to encountering the Draw Call in an RS enabled Batch Buffer which has BTP Pool Alloc Valid. BTP parse count should be less then equal to the BTP produce count for Command Streamer to make progress on a 3D_PRIMITIVE command. BTP Parse count is subtracted from the BTP Produce Count upon parsing 3D_PRIMITIVE command. This register is part of the render context save and restore. This register should not be programmed by SW.</p>		
DWord	Bit	Description
0	31:0	<p>BTP Parse Count</p> <p>This register keeps track of the BTP commands parsed by RCS prior to encountering the Draw Call in an RS enabled Batch Buffer which has BTP Pool Alloc Valid. BTP parse count should be less then equal to the BTP produce count for Command Streamer to make progress on a 3D_PRIMITIVE command. BTP Parse count is subtracted from the BTP Produce Count upon parsing 3D_PRIMITIVE command.</p>

Cache Mode Register 0

CACHE_MODE_0 - Cache Mode Register 0												
Register Space:	MMIO: 0/2/0											
Project:	CHV, BSW											
Source:	RenderCS											
Default Value:	0x00000004 CHV, BSW											
Access:	R/W											
Size (in bits):	32											
Address:	07000h											
Valid Projects:	CHV, BSW											
Description												
<p>This register is used to control the operation of the Render and Sampler L2 Caches. All reserved bits are implemented as read/write.</p> <p>Before changing the value of this register, GFX pipeline must be idle i.e. full flush is required.</p> <p>This Register is saved and restored as part of Context.</p>												
RegisterType = MMIO_SVL												
DWord	Bit	Description										
0	31:16	Mask										
		Access:	WO									
		Format:	Mask[15:0]									
		A 1 in a bit in this field allows the modification of the corresponding bit in Bits 15:0.										
	15	Sampler L2 Disable										
		Project:	CHV, BSW									
		Access:	r/w									
		Format:	Disable									
			<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>[Default]</td> <td>Sampler L2 Cache Enabled.</td> </tr> <tr> <td>1h</td> <td></td> <td>Sampler L2 Cache Disabled. All accesses are treated as misses.</td> </tr> </tbody> </table>	Value	Name	Description	0h	[Default]	Sampler L2 Cache Enabled.	1h		Sampler L2 Cache Disabled. All accesses are treated as misses.
	Value	Name	Description									
	0h	[Default]	Sampler L2 Cache Enabled.									
	1h		Sampler L2 Cache Disabled. All accesses are treated as misses.									
14:12	MSSA Compression Plane Number Threshold for eLLC	Project:	CHV, BSW									
		Security:	IP.eLLC									
		Access:	r/w									
			<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>threshold0 [Default]</td> <td>Cache only planeID = 0 in eLLC.</td> </tr> <tr> <td>1h</td> <td>threshold1</td> <td>Cache only planeID = 0, 1 in eLLC.</td> </tr> </tbody> </table>	Value	Name	Description	0h	threshold0 [Default]	Cache only planeID = 0 in eLLC.	1h	threshold1	Cache only planeID = 0, 1 in eLLC.
	Value	Name	Description									
	0h	threshold0 [Default]	Cache only planeID = 0 in eLLC.									
	1h	threshold1	Cache only planeID = 0, 1 in eLLC.									

CACHE_MODE_0 - Cache Mode Register 0

	2h	threshold2	Cache only planeID = 0..2 in eLLC.
	3h	threshold3	Cache only planeID = 0..3 in eLLC.
	4h	threshold4	Cache only planeID = 0..4 in eLLC.
	5h	threshold5	Cache only planeID = 0..5 in eLLC.
	6h	threshold6	Cache only planeID = 0..6 in eLLC.
	7h	threshold7	Cache only planeID = 0..7 in eLLC.
Programming Notes			
This bit-field is programmed based on MSAA. When MSAA compression is enabled, these settings affect HW, else it is ignored. For 16X MSAA only lower 8 planes can be cached in eLLC.			
11	Sampler Set Remapping for 3D Disable		
	Project:	CHV, BSW	
	Access:	r/w	
	Value	Name	Description
	0h	Enable Set Remap [Default]	Set remapping for 3d enabled
	1h	Disable Set Remap	Set remapping for 3d disabled
10	Reserved		
	Project:	CHV, BSW	
	Format:	Disable	
This bit controls the bug-fix in the allocation pipe for expansions when the PMA-optimization mode is enabled.			
	Value	Name	Description
	0h	Enable [Default]	Allocation pipe is not stalled if there are pending expansions
	1h	Disable	Allocation pipe is stalled if there are pending expansions
9	Sampler L2 TLB Prefetch Enable		
	Access:	r/w	
	Value	Name	Description
	0h	[Default]	TLB Prefetch Disabled
	1h		TLB Prefetch Enabled
8	Reserved		

CACHE_MODE_0 - Cache Mode Register 0

7:6	Sampler L2 Request Arbitration		
	Project:	CHV, BSW	
	Access:	r/w	
	Format:	U2	
		Value	Name
		Description	
		00b	Round Robin
		01b	Fetch are Highest Priority
		10b	Constants are Highest Priority
		11b	Reserved
5	STC Eviction Policy		
	Project:	CHV, BSW	
	Access:	r/w	
	Format:	Disable	
	If this bit is set, STCunit will have LRA as replacement policy. The default value i.e. (when this bit is reset) indicates that non-LRA eviction policy. This bit must be reset. LRA replacement policy is not supported.		
	Programming Notes	Project	
	If this bit is set to "1", bit 4 of 0x7010h must also be set to "1".	CHV, BSW	
4	RCC Eviction Policy		
	Project:	CHV, BSW	
	Access:	r/w	
	Format:	Disable	
	If this bit is set, RCCunit will have LRA as replacement policy. The default value i.e. (when this bit is reset) indicates that non-LRA eviction policy. This bit must be reset. LRA replacement policy is not supported.		
	Programming Notes	Project	
	If this bit is set to "1", bit 7 of 0x7010h must also be set to "1".	CHV, BSW	
3	Reserved		

CACHE_MODE_0 - Cache Mode Register 0

2	Hierarchical Z RAW Stall Optimization Disable	
	Project:	CHV, BSW
	Access:	r/w
	Format:	U1
	The Hierarchical Z RAW Stall Optimization allows non-overlapping polygons in the same 8x4 pixel/sample area to be processed without stalling waiting for the earlier ones to write to Hierarchical Z buffer.	
	Value	Name
	0h	Enable
	1h	Disable [Default]
	Programming Notes	
	This bit must be set to 0 to enable the Hierarchical Z RAW stall optimization.	
1	Disable clock gating in the pixel backend	
	Access:	r/w
	Format:	Disable
	MCL related clock gating is disabled in the pixel backend. Before setting this bit to 1, the instruction/state caches must be invalidated. [DevGT:{WKA}]	
0	RW optimization (portal2) fix disable	
	Project:	CHV, BSW
	Access:	r/w
	Portal 2 fix :	
	a) In MSAA mode, RCC source clear cacheline will be allocated as RW, only if its a true read (ie blend enabled, etc) and will be allocated as WO otherwise.	
	b) In any mode, RCC should not allocate a cacheline as RW, if its not a true read, evenif MSC sends RW = 11 to RCC. MSC sends an additional "True read" indicator to help RCC override the RW bit.	
	Value	Name
	0	[Default]
	1	
	Description	
Portal 2 fix enabled.		
Portal 2 fix disabled. a) RCC will always allocate source clear as RW in MSAA mode. b) RCC will always allocate on the basic of MSC RW indicator to RCC, in non source clear mode.		

Cache Mode Register 1

CACHE_MODE_1 - Cache Mode Register 1			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	RenderCS		
Default Value:	0x00000180 CHV, BSW		
Access:	R/W		
Size (in bits):	32		
Address:	07004h		
Valid Projects:	CHV, BSW		
Description			
RegisterType: MMIO_SVL			
Before changing the value of this register, GFX pipeline must be idle; i.e., full flush is required. This Register is saved and restored as part of Context.			
DWord	Bit	Description	
0	31:16	Mask	
		Access:	WO
Mask:		MASK	
Format:		Mask[15:0]	
Must be set to modify corresponding data bit. Reads to this field returns zero.			
	15	MSC Smart Bank Arbitration Disable	
		Project:	CHV, BSW
		Access:	r/w
		Format:	Disable
	Setting this bit causes MSC Bank Arbitration to be disabled. Default value, i.e. resetting this bit, will Enable MSC Smart Bank Arbitration.		
	Value	Name	
	0h	Enable [Default]	
1h	Disable		

CACHE_MODE_1 - Cache Mode Register 1

14	MSC Resolve Optimization Disable	
	Project:	CHV, BSW
	Access:	r/w
	Format:	U1
	Setting this bit causes MSC to mark cachelines dirty and appropriately update MSC during the classic clear resolve pass. Default value, i.e. resetting this bit, suppresses MSC buffer modification during the classic clear resolve pass.	
	Value	Name
	1h	Disable
	0h	Enable [Default]
13	NP EARLY Z FAILS DISABLE	
	Project:	CHV, BSW
	Access:	r/w
	Value	Name
	0h	Disable [Default]
	1h	Enable
		Description
		When NP PMA FIX ENABLE = 1, clearing this bit disables IZ to conservatively fail pixels.
		When NP PMA FIX ENABLE = 1, IZ does conservatively fail any NP pixels.
	Programming Notes	
	This bit must be set when NP PMA FIX ENABLE = 1	
	This bit must not be set when NP PMA FIX ENABLE = 0	
12	HIZ Eviction Policy	
	Project:	CHV, BSW
	Access:	r/w
	Format:	U1
	If this bit is set, Hizunit will have LRA as replacement policy. The default value i.e. (when this bit is reset) indicates the non-LRA eviction policy. For performance reasons, this bit must be reset.	
	Value	Name
	0h	[Default]
	1h	
		Description
		Non-LRA eviction Policy
		LRA eviction Policy
	Programming Notes	
	If this bit is set to "1", bit 3 of 0x7010h must also be set to "1"	

CACHE_MODE_1 - Cache Mode Register 1

11	NP PMA FIX ENABLE		
	Project:	CHV, BSW	
	Access:	r/w	
	Value	Name	Description
	0h	Disable [Default]	Enables stalling PMA behavior for NP depth pixels in the early depth pipeline. (Legacy behavior)
	1h	Enable	Enables non-stalling PMA behavior for NP depth pixels in the early depth pipeline.
	Programming Notes		
	<p>SW must set this bit in order to enable this fix when following expression is TRUE. <code>3DSTATE_WM::ForceThreadDispatch != 1 && !(3DSTATE_RASTER::ForceSampleCount != NUMRASTSAMPLES_0) && (3DSTATE_DEPTH_BUFFER::SURFACE_TYPE != NULL) && (3DSTATE_DEPTH_BUFFER:: HIZ Enable) && !(3DSTATE_WM::EDSC_Mode == 2) && (3DSTATE_PS_EXTRA::PixelShaderValid) && !(3DSTATE_WM_HZ_OP::DepthBufferClear 3DSTATE_WM_HZ_OP::DepthBufferResolve 3DSTATE_WM_HZ_OP::Hierarchical Depth Buffer Resolve Enable 3DSTATE_WM_HZ_OP::StencilBufferClear) && (3DSTATE_WM_DEPTH_STENCIL::DepthTestEnable) && ((3DSTATE_PS_EXTRA::PixelShaderKillsPixels 3DSTATE_PS_EXTRA:: oMask Present to RenderTarget 3DSTATE_PS_BLEND::AlphaToCoverageEnable 3DSTATE_PS_BLEND::AlphaTestEnable 3DSTATE_WM_CHROMAKEY::ChromaKeyKillEnable) && (3DSTATE_WM::ForceKillPix != ForceOff && (3DSTATE_WM_DEPTH_STENCIL::DepthWriteEnable && 3DSTATE_DEPTH_BUFFER::DEPTH_WRITE_ENABLE) (3DSTATE_WM_DEPTH_STENCIL::Stencil Buffer Write Enable && 3DSTATE_DEPTH_BUFFER::STENCIL_WRITE_ENABLE && 3DSTATE_STENCIL_BUFFER::STENCIL_BUFFER_ENABLE))) (3DSTATE_PS_EXTRA:: Pixel Shader Computed Depth mode != PSCDEPTH_OFF))</code></p>		
10	Reserved		
	Project:	CHV, BSW	
9	Reserved		
	Project:	CHV, BSW	
	Access:	r/w	

CACHE_MODE_1 - Cache Mode Register 1

8:7

Sampler Cache Set XOR selection

Project:	CHV, BSW
Access:	r/w
Format:	U2

These bits have an impact only when the Sampler cache is configured in 16 way set associative mode. If the cache is being used for immediate data or for blitter data these bits have no effect.

Value	Name	Description
00b	None	No XOR.
01b	Scheme 1	$New_set_mask[3:0] = Tiled_address[16:13]$. $New_set[3:0] \text{ less than or } = New_set_mask[3:0] \wedge Old_set[3:0]$. Rationale: These bits can distinguish among 16 different equivalent classes of virtual pages. These bits also represent the lsb for tile rows ranging from a pitch of 1 tile to 16 tiles.
10b	Scheme 2	$New_set_mask[3] = Tiled_address[17] \wedge Tiled_address[16]$. $New_set_mask[2] = Tiled_address[16] \wedge Tiled_address[15]$. $New_set_mask[1] = Tiled_address[15] \wedge Tiled_address[14]$. $New_set_mask[0] = Tiled_address[14] \wedge Tiled_address[13]$. $New_set[3:0] \text{ less than or } = New_set_mask[3:0] \wedge Old_set[3:0]$. Rationale: More bits on each XOR can give better statistical uniformity on sets and since two lsbs are taken for each tile row size, it reduces the chance of aliasing on sets.
11b	Scheme 3 [Default]	$New_set_mask[3] = Tiled_address[22] \wedge Tiled_address[21] \wedge Tiled_address[20] \wedge Tiled_address[19]$. $New_set_mask[2] = Tiled_address[18] \wedge Tiled_address[17] \wedge Tiled_address[16]$. $New_set_mask[1] = Tiled_address[15] \wedge Tiled_address[14]$. $New_set_mask[0] = Tiled_address[13]$. $New_set[3:0] \text{ less than or } = New_set_mask[3:0] \wedge Old_set[3:0]$. Rationale: More bits on each XOR can give better statistical uniformity on sets and since each XOR has different bits, it reduces the chance of aliasing on sets even more.

Programming Notes

This field should be programmed as "00b" corresponding to NO XOR option when the 3D map performance fix in MT is enabled using the field "**Sampler Set Remapping for 3D Disable**" in **CACHE_MODE_0 - Cache Mode Register 0**.

CACHE_MODE_1 - Cache Mode Register 1

6	4X4 RCPFE-STC Optimization Disable	
Project:		CHV, BSW
Access:		r/w
Format:		Disable
Value	Name	Description
0h	[Default]	Enables two contiguous 4x2s to be collected as 4X4 access for STC interface. This allows for less bank collision and less RAM power on STC.
1h		Disables this optimization and therefore only one valid 4x2 is sent to STC on the 4X4 interface.
5	MCS Cache Disable	
Project:		CHV, BSW
Access:		r/w
Format:		Disable
For Programming restrictions please refer to the 3D Pipeline.		
Value	Name	Description
0h	[Default]	MCS cache enabled. It allows RTs with MCS buffer enabled to be rendered using either MSAA compression for MSRT OR with color clear feature for non MSRT.
1h		MCS cache is disabled. Hence no MSAA compression for MSRT and no color clear for non-MSRT.
4	Float Blend Optimization Enable	
Project:		CHV, BSW
Access:		r/w
Format:		Enable
Value	Name	Description
0h	[Default]	Disables blend optimization for floating point RTs.
1h		Enables blend optimization for floating point RTs.
3	Depth Read Hit Write-Only Optimization Disable	
Project:		CHV, BSW
Access:		r/w
Format:		Disable
Value	Name	Description
0h	[Default]	Read Hit Write-only optimization is enabled in the Depth cache (RCZ).
1h		Read Hit Write-only optimization is disabled in the Depth cache (RCZ).

CACHE_MODE_1 - Cache Mode Register 1							
2	RCZ Read after expansion control fix 2						
	Access: r/w						
	Format: Enable						
	Value Name Description						
	0h [Default] RCZ will suppress the read request to memory if it was allocated as a expansion Cacheline RCZ will always issue a read request to memory, even if it was previously allocated as expansion Cacheline						
	1h RCZ will always issue a read request to memory, even if it was previously allocated as expansion Cacheline RCZ will suppress the read request to memory if it was allocated as a expansion Cacheline						
	1 Blend Optimization Fix Disable						
	Project: CHV, BSW						
	Access: r/w						
	Description						
This bit when reset, enables blend optimization fix. If this bit is set, it disables the blend optimization fix and may exhibit corruption on alpha components in the render target under some conditions.							
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">[Default]</td> </tr> <tr> <td style="text-align: center;">1</td> <td></td> </tr> </tbody> </table>		Value	Name	0	[Default]	1	
Value	Name						
0	[Default]						
1							
0	Reserved						
	Project: CHV, BSW						

CAPPOINT

CAPPOINT - CAPPOINT						
Register Space:	PCI: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x000000D0					
Size (in bits):	32					
Address:	00034h					
This register points to a linked list of capabilities implemented by this device.						
DWord	Bit	Description				
0	31:8	RESERVED				
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	000000h	Access:	RO
	Default Value:	000000h				
	Access:	RO				
7:0	CAPABILITIES_POINTER	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">D0h</td> </tr> <tr> <td>Access:</td> <td>R/W Once</td> </tr> </table>	Default Value:	D0h	Access:	R/W Once
		Default Value:	D0h			
Access:	R/W Once					
		The first item in the capabilities list is at address D0h (PMCS). This register is programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.				

CCK_CTL1

CCK_CTL1 - CCK_CTL1			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00200000		
Size (in bits):	32		
Address:	101100h		
<p>BGF related programming. Note: This register should be the last one written between 10_1100, 10_1104, 10_1108. To be more specific, 10_1100[0] is the last one to be programmed between 10_1100h, 10_1104h and 10_1108h registers. The reason is that CZ clock does not stop on a frequency change and hence the fused values for the CZ clock domain must be the same and not intermittently transition to an invalid value, like all zeros. Changed for CHV, BSW.</p>			
DWord	Bit	Description	
0	31:28	czcount_30ns	
		Default Value:	0h
		Access:	R/W
		Description	
		This register contains the number of cz clock cycles that it takes to make up 30ns.	
		Frequency (MHz)	czcount_30ns
		400	4'b1011
		333.333	4'b1001
		320	4'b0001
		266.667	4'b0111
200	4'b0101		
Frequency (MHz)	czcount_30ns		
533.333	4'b1111		
466.667	4'b1101		
373.333	4'b1011		
360	4'b1010		
355.556	4'b1010		
350	4'b1010		
27		Reserved	
		Default Value:	0b
		Access:	RO
		Reserved	

CCK_CTL1 - CCK_CTL1

26:24	WellPUfreq		
		Default Value:	000b
		Access:	R/W
	<p>While Render or Media is being waking up from standby, clocks are allowed to be run for some time for x-contention removal. For CHV, BSW, there is a perceived di/dt risk by running this x-contention removal at full CU2X/CU frequency. This potential issue is amplified for CHV, BSW supports a 1:1 primary gear ratio and having a CU2X clock frequency of upto 2G.</p> <p>* 0xx: x-contention removal time will use: CU2X/1 for 2x clock, CU/1 for 1X clock. * 100: x-contention removal time will use a CU/4. * 101: x-contention removal time will use a CU/8. * 110: x-contention removal time will use a CU/16. * 111: x-contention removal time will use a CU/32.</p>		
	Programming Notes		
	Punit should never program this bitfield to 3'b000 and it should program this to 3'b110.		
23	CFG1Fuse0		
		Default Value:	0b
		Access:	R/W
	<p>bgfsource_config1fuse0. By default, there is no frequency change. The set of BGF and SS registers are provided by fuses. When frequency change is required, this bit must be set to '1' and Punit/driver must program the remainder of the clock crossing registers.</p> <p>This bit must be last bit written between register 10_1100, 10_1104 and 10_1108.</p> <p>The following registers are affected by this configuration bit: selecting between fuse values and configuration register:</p> <p>0x10_1100[26:24] 0x10_1100[22:16] 0x10_1104[31:0] 0x10_1108[31:0]</p>		
22:20	CZ2CU_PTRSEP		
		Default Value:	010b
		Access:	R/W
	<p>bgf_cz2cu_ptrsep. Pointer separation for cz2cu BGF</p> <p>000 = Pointer separation of 0 001 = Pointer separation of 1 010 = Pointer separation of 2 (Primary) 011 = Pointer separation of 3 (Secondary) 100 = Pointer separation of 4 101 = Pointer separation of 5 110 = Pointer separation of 6 111 = Pointer separation of 7</p>		

CCK_CTL1 - CCK_CTL1		
19	Reserved	
	Default Value:	0b
	Access:	RO
Reserved		
18:16	CU2CZ_PTRSEP	
	Default Value:	0h
	Access:	R/W
bgf_cu2cz_ptrsep. Pointer separation for cu2cz BGF 000 = Pointer separation of 0 001 = Pointer separation of 1 010 = Pointer separation of 2 (Primary) 011 = Pointer separation of 3 (Secondary) 100 = Pointer separation of 4 101 = Pointer separation of 5 110 = Pointer separation of 6 111 = Pointer separation of 7		
15:9	Reserved	
	Default Value:	00h
	Access:	RO
Reserved		
8	ClkSquashEn	
	Default Value:	0b
	Access:	R/W
Clock Squash Enable. 0 = disabled. 1 = enabled. When this bit is enabled the GFX clock squashing feature is enabled. Clock squashing is only allowed when VNN is set to Vmin.		
Programming Notes		
This field must be zero at all times when in HPLLmode.		
7:1	Reserved	
	Default Value:	0h
	Access:	RO
Reserved		
0	DbIBufPulse	
	Default Value:	0h
	Access:	WO
Reading from this register will always return a zero. Punit will write a one into this bit in order to push the BGF parameters into the double buffer during CPD/clock squah being enabled. A write to this register bit creates a one clock wide pulse (doublebufferpulse)to the CPunit.		

CCK_CTL2

CCK_CTL2 - CCK_CTL2						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	101104h					
CZ and CU ratios for BGFs and for common clock calculations.Changed for CHV, BSW.						
DWord	Bit	Description				
0	31:16	<p>CZ2CU_CUratio</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">0000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>These 16 bits shows the CU part of the BGF ratio between CZ and CU clock domain. CU_SquashAllow (=CZ2CU_CUratio) must always be less than or equal to CU_SquashWindow. When ClkSquashEn=0, CU_SquashAllow = CZ2CU_CUratio = CU_SquashWindow. 10_1108h will be dont care when ClkSquashEn=0. The effective/average squashed frequency will be determined by:(CU_SquashAllow/CU_SquashWindow)</p> <p>When ClkSquashEn=1 and in GPLLmode, $12 \leq CZ2CU_CUratio(10_1104[31:16]) \leq CU_Squashwindow(10_1108[31:16])$ and multiples of 4. Effective CUfrequency = CUratio/(CU Squash Window)</p> <p>Actual CUfrequency = UnsquashedFrequency*CUratio/(CU Squash Window)</p> <p>If in GPLLmode, CU2x frequency =</p> <ul style="list-style-type: none"> (400/10)*N, where N inside {2,50} (333/8)*N, where N inside {2,48} (320/8)*N, where N inside {2,50} (267/6)*N, where N inside {2,45} (200/5)*N, where N inside {2,50} <p>The value programmed into this bitfield will be N*4.</p> <p>In HPLLmode: CZ2CU_CUratio=720/(INTEGER*2). The HPLLvco (as determined by CCK_FUSE_REG0[1:0]) is divided by an INTEGER=(1,2,3,4,5,6,8,9,10) to create the CU2x frequency. CUclk=CU2xclk/2.</p>	Default Value:	0000h	Access:	R/W
Default Value:	0000h					
Access:	R/W					

CCK_CTL2 - CCK_CTL2

15:0	CZ2CU_CZratio		
	Default Value:	0000h	
	Access:	R/W	
<p>These 16 bits shows the CU part of the BGF ratio between CZ and CU clock domain. $CZ2CU_CZratio = UsyncPeriod/CZperiod$ In GPLLmode, UsyncPeriod is expected to be $(8 * GPLLref_in_ns)$. GPLLref_in_ns is expected to be $CZperiod * 5$ for CZ200 $CZperiod * 6$ for CZ266 $CZperiod * 8$ for CZ320 $CZperiod * 8$ for CZ333 $CZperiod * 10$ for CZ400. That makes $CZ2CU_CZratio = 8 * 5$ for CZ200 and GPLL mode. $CZ2CU_CZratio = 8 * 6$ for CZ266 and GPLL mode. $CZ2CU_CZratio = 8 * 8$ for CZ320 and GPLL mode. $CZ2CU_CZratio = 8 * 8$ for CZ333 and GPLL mode. $CZ2CU_CZratio = 8 * 10$ for CZ400 and GPLL mode. The above only applies for GPLL mode and when $UsyncPeriod = 8 * GPLLref$, CPunit will internally generate the following signal: $CZ_Com_limit = CZ2CU_CZratio - 1$ In HPLLmode: $CZ2CU_CZratio = 720 / (INTEGER * 1)$. The HPLLvco (as determined by $CCK_FUSE_REG0[1:0]$) is divided by an $INTEGER = (1, 2, 3, 4, 5, 6, 8, 9, 10)$ to create the CZ frequency.</p>			

CCK_CTL3

CCK_CTL3 - CCK_CTL3				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00008000			
Size (in bits):	32			
Address:	101108h			
Graphics clock squash control.Changed for CHV, BSW.				
DWord	Bit	Description		
0	31:16	CU SQUASH WINDOW		
		<table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>0000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This register will always show the number of unsquashed clock cycles in a usync window. $CU_SquashWindow = UsyncPeriod / Unsquashed_CUperiod$. In GPLLmode, UsyncPeriod is expected to be $(8 * GPLLref_in_ns)$. CUperiod will be $GPLLref_in_ns / Ratio$. That makes, $CU_SquashWindow = (8 * GPLLref_in_ns) / (GPLLref_in_ns / Ratio) = 8 * Ratio$. Ratio is the multiplier from GPLLref to provide the CU clock frequency. Note: $CU_SquashWindow = 8 * Ratio$ only applies for GPLL mode when the usync period is $8 * GPLL$. In HPLLmode, clock squashing is not supported and 10_1100[8] must be zero at all times in HPLLmode.</p>	Default Value:	0000h
Default Value:	0000h			
Access:	R/W			
	15:0	CU SQUASH INIT		
		<table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>8000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This register is used to move around the location of where the clocks are squashed. For initial design, this is always set to 8000h.</p>	Default Value:	8000h
Default Value:	8000h			
Access:	R/W			

CCK_CTL4

CCK_CTL4 - CCK_CTL4			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	10110Ch		
CZclk 30ns TSV Generation			
DCN requires support for more CZclk frequencies			
DWord	Bit	Description	
0	31:17	SPARE	
		Default Value:	00000000h
		Access:	R/W
		Reserved	
16		CZCLK 30ns Mechanism	
		Access:	R/W
This bit defines whether we use the old counter mechanism for generating the 30ns pulse or use this new TSV scheme 0 - Use the old counter mechanism to determine the 30ns pulse (default) 1 - Use the new TSV scheme with the Allow and Window values from this register			
15:8		CZclk HPLL VCOS IN 30ns	
		Access:	R/W
These bits determine the window in terms of the number of HPLL VCO clock cycles in 30ns			
7:0		CZclk HPLL DIV	
		Access:	R/W
These bits define the integer used to divide HPLLvco to get CZclk			

CLAIM_ER

CLAIM_ER - CLAIM_ER		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	182028h	
Claim Error Counter - counts the RM claim error (no RM claim) reported at CLAIM_ERROR field of EIR		
DWord	Bit	Description
0	31	CLAIM_ER_CLR
		Default Value: 0b
	Access: WO	
	writing a '1' to this bit clears the CLAIM_ER_CTR, CTR_OVERFLOW and CLAIM_ERROR bit (EIR[0]). A read of this bit always returns 0	
30:17	RESERVED	
	Default Value: 0000h	
	Access: RO	
Reserved		
16	CTR_OVERFLOW	
	Default Value: 0b	
	Access: RO	
When set, indicates that the CLAIM_ER_CTR field of this register has overflowed (i.e., claim-error count has reached the value of 65536) The overflow is supplied by the RMBus master.		
15:0	CLAIM_ER_CTR	
	Default Value: 0000h	
Access: RO		

Clipper Invocation Counter

CL_INVOCATION_COUNT - Clipper Invocation Counter		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	02338h	
Valid Projects:		
<p>This register stores the count of objects entering the Clipper stage. This register is part of the context save and restore.</p>		
DWord	Bit	Description
0	63:32	CL Invocation Count Report UDW Number of objects entering the clipper stage. Updated only when Statistics Enable is set in CLIP_STATE (see the Clipper Chapter in the 3D Volume.)
	31:0	CL Invocation Count Report LDW Number of objects entering the clipper stage. Updated only when Statistics Enable is set in CLIP_STATE (see the Clipper Chapter in the 3D Volume.)

Clipper Primitives Counter

CL_PRIMITIVES_COUNT - Clipper Primitives Counter		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	02340h	
Valid Projects:		
<p>This register reflects the total number of primitives that have been output by the clipper. This register is part of the context save and restore.</p>		
DWord	Bit	Description
0	63:32	<p>Clipped Primitives Output Count UDW</p> <p>Total number of primitives output by the clipper stage. This count is updated for every primitive output by the clipper stage, as long as Statistics Enable is set in SF_STATE (see the Clipper and SF Chapters in the 3D Volume.)</p>
	31:0	<p>Clipped Primitives Output Count LDW</p> <p>Total number of primitives output by the clipper stage. This count is updated for every primitive output by the clipper stage, as long as Statistics Enable is set in SF_STATE (see the Clipper and SF Chapters in the 3D Volume.)</p>

CLKGATE Messaging Register for Clocking Unit

MSG_CLKGATE_GCP - CLKGATE Messaging Register for Clocking Unit

Register Space: MMIO: 0/2/0

Project: CHV, BSW

Source: PRM

Default Value: 0x00000000

Size (in bits): 16

Address: 0802Ch

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	15:7	Reserved Access: RO
	6	Gate cmclk Acknowledgement (VCS1) Access: R/W Gate cmclk Acknowledgement (VCS1) 1'b0 : Clocks are ungated <default> 1'b1 : Clocks are gated
	5	Gate cwclk Acknowledgement (WIN) Access: R/W Gate cwclk Acknowledgement (WIN) 1'b0 : Clocks are ungated <default> 1'b1 : Clocks are gated
	4	Reserved
	3	Gate cfclk Acknowledgement (CS) Access: R/W Gate cfclk Acknowledgement (CS) 1'b0 : Clocks are ungated <default> 1'b1 : Clocks are gated
	2	Gate cvclk Acknowledgement (VECS) Access: R/W Gate cvclk Acknowledgement (VECS) 1'b0 : Clocks are ungated <default> 1'b1 : Clocks are gated

MSG_CLKGATE_GCP - CLKGATE Messaging Register for Clocking Unit

	1	Gate cmclk Acknowledgement (VCS0)	
		Access:	R/W
		Gate cmclk Acknowledgement (VCS0) 1'b0 : Clocks are ungated <default> 1'b1 : Clocks are gated	
	0	Gate crclk Acknowledgement (CS)	
		Access:	R/W
		Gate crclk Acknowledgement (CS) 1'b0 : Clocks are ungated <default> 1'b1 : Clocks are gated	

CLOCK_GATE_DIS1

CLOCK_GATE_DIS1 - CLOCK_GATE_DIS1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	182060h	
Gunit Clock Gating Disable		
DWord	Bit	Description
0	31	GIOSF_DIS
		Default Value: 0b
	Access: R/W	
	0 = Enable clock gating 1 = Disable clock gating	
	30	GPFI_DIS
		Default Value: 0b
	Access: R/W	
	0 = Enable clock gating 1 = Disable clock gating	
	29	GRMW_DIS
		Default Value: 0b
	Access: R/W	
	0 = Enable clock gating 1 = Disable clock gating	
	28	GSA_OUTBOUND_DIS
		Default Value: 0b
	Access: R/W	
	0 = Enable clock gating 1 = Disable clock gating	
	27	GSA_RTN_DIS
		Default Value: 0b
	Access: R/W	
	0 = Enable clock gating 1 = Disable clock gating	

CLOCK_GATE_DIS1 - CLOCK_GATE_DIS1	
26	GUP_DIS Default Value: 0b Access: R/W 0 = Enable clock gating 1 = Disable clock gating
	GWAKE_DIS Default Value: 0b Access: R/W 0 = Enable clock gating 1 = Disable clock gating
	GBC_DIS Default Value: 0b Access: R/W 0 = Enable clock gating 1 = Disable clock gating
	GRMBUS_DIS Default Value: 0b Access: R/W 0 = Enable clock gating 1 = Disable clock gating

CLOCK_GATE_DIS1 - CLOCK_GATE_DIS1				
19:16	SPARE1			
	<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>0h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Spare</p>	Default Value:	0h	Access:
Default Value:	0h			
Access:	R/W			
15	Reserved			
14	Reserved			
13	Reserved			
12	GSECDISP_DIS			
	<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>0 = Enable clock gating 1 = Disable clock gating</p>	Default Value:	0b	Access:
Default Value:	0b			
Access:	R/W			
11	GREGDISP_DIS			
	<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>0 = Enable clock gating 1 = Disable clock gating</p>	Default Value:	0b	Access:
Default Value:	0b			
Access:	R/W			
10	GCTLQ_DIS			
	<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>0 = Enable clock gating 1 = Disable clock gating</p>	Default Value:	0b	Access:
Default Value:	0b			
Access:	R/W			
9	GMMIO_DIS			
	<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>0 = Enable clock gating 1 = Disable clock gating</p>	Default Value:	0b	Access:
Default Value:	0b			
Access:	R/W			
8	GCFG_DIS			
	<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>0 = Enable clock gating 1 = Disable clock gating</p>	Default Value:	0b	Access:
Default Value:	0b			
Access:	R/W			
7:4	SPARE2			
	<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>0h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Spare</p>	Default Value:	0h	Access:
Default Value:	0h			
Access:	R/W			

CLOCK_GATE_DIS1 - CLOCK_GATE_DIS1

	3:0	CZ_IDLE_TIMER	
		Default Value:	0h
		Access:	R/W
		<p>Gunit CZ domain idle timer count value. Individual Gunit CZ fubs use this as a counter pre-load value. 0 = Idle timer disabled 1 - 15 = After a unit indicates idle, wait this many clocks before gating.</p>	

CLOCK_GATE_DIS2

CLOCK_GATE_DIS2 - CLOCK_GATE_DIS2			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	182064h		
Gunit Clock Gating Disable register2.			
DWord	Bit	Description	
0	31:9	CLKGATE_SPARE	
		Default Value:	000000h
		Access:	R/W
		Spare to be assigned to clock gate disables.	
		8	GPMH_DIS
Access:	R/W		
New for CHV, BSW 0 = Enable clock gating 1 = Disable clock gating			
7	ATOMICS_DIS	Default Value:	0b
		Access:	R/W
		New for CHV, BSW 0 = Enable clock gating 1 = Disable clock gating	
6	IOSFSB_P_DIS	Default Value:	0b
		Access:	R/W
		New for CHV, BSW 0 = Enable clock gating 1 = Disable clock gating	
5	IOSFSB_DIS	Default Value:	0b
		Access:	R/W
		New for CHV, BSW 0 = Enable clock gating 1 = Disable clock gating	

CLOCK_GATE_DIS2 - CLOCK_GATE_DIS2

	4	GARB_DIS	
		Default Value:	0b
		Access:	R/W
		0 = Enable clock gating 1 = Disable clock gating	
	3	GMAP_DIS	
		Default Value:	0b
		Access:	R/W
		0 = Enable clock gating 1 = Disable clock gating	
	2	Reserved	
	1	GRDDATBUF_DIS	
		Default Value:	0b
		Access:	R/W
		0 = Enable clock gating 1 = Disable clock gating	
	0	GWRDATQ_DIS	
		Default Value:	0b
		Access:	R/W
0 = Enable clock gating 1 = Disable clock gating			

Clock gate and clear EU metrics

EUMETRICSCLEAR - Clock gate and clear EU metrics																												
Register Space:	MMIO: 0/2/0																											
Project:	CHV, BSW																											
Source:	PRM																											
Default Value:	0x00000000																											
Size (in bits):	32																											
Address:	138198h																											
EU Metrics Clear																												
DWord	Bit	Description																										
0	31:1	Reserved																										
		Default Value:	00000000h																									
		Access:	RO																									
Reserved																												
0	0	Clear EU Metrics																										
		Default Value:	0b																									
		Access:	R/W																									
		For Cdyn optimization, when this bit is set to one, all of the 13 counters are clock gated. Then, after setting it to '0(zero), On the falling edge of EUMetricsClr, all of the 13 counters are reset to zero and counting resumes.																										
		<table border="1"> <thead> <tr> <th>Event Name</th> <th>Units</th> <th>Maximum per cycle (average)</th> <th>Metric</th> <th>Comments</th> </tr> </thead> <tbody> <tr> <td>event0: ss0_gpm_sampler_active_igpa</td> <td>1 = 1 sampler busy in this sub-slice.</td> <td>1 sampler busy in this sub-slice.</td> <td>Sampler busy per sub-slice</td> <td>Measures sampler utilization (i.e, sampler not idle)</td> </tr> <tr> <td>event1: ss1_gpm_sampler_active_igpa</td> <td>1 = 1 sampler busy in this sub-slice.</td> <td>1 sampler busy in this sub-slice.</td> <td>Sampler busy per sub-slice</td> <td>Measures sampler utilization (i.e, sampler not idle)</td> </tr> <tr> <td>event2: tdl0_gpm_eu_stall</td> <td>1 = 32 EUs stalled on this sub-slice.</td> <td>8 EUs stalled on this sub-slice.</td> <td>EU stall per sub-slice</td> <td>Measures EU stalls</td> </tr> <tr> <td>event3: tdl1_gpm_eu_stall</td> <td>1 = 32 EUs stalled on this sub-slice.</td> <td>8 EUs stalled on this sub-slice.</td> <td>EU stall per sub-slice</td> <td>Measures EU stalls</td> </tr> </tbody> </table>				Event Name	Units	Maximum per cycle (average)	Metric	Comments	event0: ss0_gpm_sampler_active_igpa	1 = 1 sampler busy in this sub-slice.	1 sampler busy in this sub-slice.	Sampler busy per sub-slice	Measures sampler utilization (i.e, sampler not idle)	event1: ss1_gpm_sampler_active_igpa	1 = 1 sampler busy in this sub-slice.	1 sampler busy in this sub-slice.	Sampler busy per sub-slice	Measures sampler utilization (i.e, sampler not idle)	event2: tdl0_gpm_eu_stall	1 = 32 EUs stalled on this sub-slice.	8 EUs stalled on this sub-slice.	EU stall per sub-slice	Measures EU stalls	event3: tdl1_gpm_eu_stall	1 = 32 EUs stalled on this sub-slice.	8 EUs stalled on this sub-slice.
Event Name	Units	Maximum per cycle (average)	Metric	Comments																								
event0: ss0_gpm_sampler_active_igpa	1 = 1 sampler busy in this sub-slice.	1 sampler busy in this sub-slice.	Sampler busy per sub-slice	Measures sampler utilization (i.e, sampler not idle)																								
event1: ss1_gpm_sampler_active_igpa	1 = 1 sampler busy in this sub-slice.	1 sampler busy in this sub-slice.	Sampler busy per sub-slice	Measures sampler utilization (i.e, sampler not idle)																								
event2: tdl0_gpm_eu_stall	1 = 32 EUs stalled on this sub-slice.	8 EUs stalled on this sub-slice.	EU stall per sub-slice	Measures EU stalls																								
event3: tdl1_gpm_eu_stall	1 = 32 EUs stalled on this sub-slice.	8 EUs stalled on this sub-slice.	EU stall per sub-slice	Measures EU stalls																								

EUMETRICSCLEAR - Clock gate and clear EU metrics

event4: tdl0_gpm_ipc_count	1 = 32 instructions executed on this sub-slice.	16 instructions executed on this sub-slice.	IPC per sub-slice	Measures EU utilization: 0, 1, or 2 counts per clock per EU
event5: tdl1_gpm_ipc_count	1 = 32 instructions executed on this sub-slice.	16 instructions executed on this sub-slice.	IPC per sub-slice	Measures EU utilization: 0, 1, or 2 counts per clock per EU
event6: tdl0_gpm_threads_allocated	1 = 64 threads allocated in this sub-slice.	56 threads allocated in this sub-slice.	Thread allocated per sub-slice	Measures the threads allocated
event7: tdl1_gpm_threads_allocated	1 = 64 threads allocated in this sub-slice.	56 threads allocated in this sub-slice.	Thread allocated per sub-slice	Measures the threads allocated
event8: tdl0_gpm_eu_stall_sampler	1 = 64 EUs stalled by sampler in this sub-slice.	56 threads stalled by sampler in this sub-slice.	Placeholder for EUstallTime by sampler per sub-slice	Measures how much of eu stalls are due to sampler
event9: tdl1_gpm_eu_stall_sampler	1 = 64 EUs stalled by sampler in this sub-slice.	56 threads stalled by sampler in this sub-slice.	Placeholder for EUstallTime by sampler per sub-slice	Measures how much of eu stalls are due to sampler
event10: tdl0_gpm_eu_not_idle	1 = 32 EUs not idle in this sub-slice.	8 EUs not idle in this sub-slice.	Clocks any EU is not idle per sub-slice	Measures EU utilization (i.e, EU not idle)
event11: tdl1_gpm_eu_not_idle	1 = 32 EUs not idle in this sub-slice.	8 EUs not idle in this sub-slice.	Clocks any EU is not idle per sub-slice	Measures EU utilization (i.e, EU not idle)
event12: constant_one	1			one clock cycle toggles.

Clock Gating Messages

CGMSG - Clock Gating Messages		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	08104h	
Clock Gating Messages Register		
DWord	Bit	Description
0	31:16	Message Mask
		Access: RO
	Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000	
	15:7	Reserved
		Access: RO
	Reserved	
	6	Media 1 Clock gating control message
		Access: R/W
Gate Media 1 (2nd Vbox) Clock Message : '0' : Media 1 Clock Un-gate Request (un-gates the cmclk clock in the 2n Media block) '1' : Media 1 Clock Gate Request (gates the cmclk clock in the 2nd Media block)		
5	WIDI Clock Gating control Message	
	Access: R/W	
Gate WIDI Clock Message : '0' : WIDI Clock Un-gate Request (un-gates the cwclk clock) '1' : WIDI Clock Gate Request (gates the cwclk clock)		
4	Reserved	
	Reserved	
3	Fix Function Clock gating Control Message	
	Access: R/W	
Gate Fix Clock Message : '0' : Fix Clock Un-gate Request (un-gates the cfclk/cf2xclk clock) '1' : Fix Clock Gate Request (gates the cfclk/cf2xclk clock)		
2	VEbox Clock gating Control message	
	Access: R/W	
Gate VE-box Clock Message : '0' : VEbox Clock Un-gate Request (un-gates the cvclk clock) '1' : VEbox Clock Gate Request (gates the cvclk clock)		

CGMSG - Clock Gating Messages			
1	<p>Media 0 Clock Gating Control Message</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>Gate Media Clock Message :</p> <p>'0' : Media 0 Clock Un-gate Request (un-gates the cmclk clock)</p> <p>'1' : Media 0 Clock Gate Request (gates the cmclk clock)</p>	Access:	R/W
Access:	R/W		
0	<p>Row Clock Gating Control Message</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>Gate Row Clocks Message :</p> <p>'0' : Row Clock Un-gate Request (un-gates the crclk and cr2xclk clocks)</p> <p>'1' : Row Clock Gate Request (gates the crclk and cr2xclk clocks)</p>	Access:	R/W
Access:	R/W		

Color/Depth Write FIFO Watermarks

CZWMRK - Color/Depth Write FIFO Watermarks			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	RenderCS		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Trusted Type:	1		
Address:	04060h		
This register is directly mapped to the current Virtual Addresses in the MTTLB (Texture and constant cache TLB).			
DWord	Bit	Description	
0	31:24	Reserved Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td> </td></tr></table> MBZ	
	23:18	Color Wr Burst Size This is the maximum size of the requests burst, from the last High Watermark trip, before reevaluating the High Watermark again.	
	17:16	Reserved Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td> </td></tr></table> MBZ	
	15:12	Color Wr FIFO High Watermark This is the number of accumulated Color writes that will trigger a Burst of Z Writes.	
	11:6	Z Wr Burst Size This is the maximum size of the requests burst, from the last High Watermark trip, before reevaluating the High Watermark again.	
	5:4	Reserved Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td> </td></tr></table> MBZ	
3:0	Z Wr FIFO High Watermark This is the number of accumulated Depth writes that will trigger a Burst of Z Writes.		

Configuration Register0 for RPMunit

CONFIG0 - Configuration Register0 for RPMunit					
Register Space:	MMIO: 0/2/0				
Project:	CHV, BSW				
Default Value:	0x00000000				
Size (in bits):	32				
Address:	00D00h				
Lock bit LOCK applies to all RW/L fields in this register. Lock is overridden during context restore.					
DWord	Bit	Description			
0	31	<p>Lock for RW/L Fields in this Register</p> <table border="1"> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>0 = Bits of CONFIG0 register are R/W. 1 = All bits of CONFIG0 register are RO (including this lock bit). Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). Lock is reset on a restore after context is captured.</p>	Access:	R/W Lock	
	Access:	R/W Lock			
30:0	<p>Placeholder Bits</p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>Placeholder bits for implementation or ECO loops.</p>	Project:	CHV, BSW	Access:	R/W Lock
Project:	CHV, BSW				
Access:	R/W Lock				

Configuration Register1 for RPMunit

CONFIG1 - Configuration Register1 for RPMunit					
Register Space:	MMIO: 0/2/0				
Project:	CHV, BSW				
Default Value:	0x00000000				
Size (in bits):	32				
Address:	00D04h				
Lock bit LOCK applies to all RW/L fields in this register. Lock is overridden during context restore.					
DWord	Bit	Description			
0	31	Lock for RW/L Fields in this Register <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Access:</td> <td style="width: 50%;">R/W Lock</td> </tr> </table> <p>0 = Bits of CONFIG0 register are R/W. 1 = All bits of CONFIG0 register are RO (including this lock bit). Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). Lock is reset on a restore after context is captured.</p>	Access:	R/W Lock	
	Access:	R/W Lock			
30:0	Placeholder Bits <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td style="width: 50%;">CHV, BSW</td> </tr> <tr> <td style="width: 50%;">Access:</td> <td style="width: 50%;">R/W Lock</td> </tr> </table> <p>Placeholder bits for implementation or ECO loops.</p>	Project:	CHV, BSW	Access:	R/W Lock
Project:	CHV, BSW				
Access:	R/W Lock				

Configuration Register for RCPunit

RCPCONFIG - Configuration Register for RCPunit		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Default Value:	0x0000000F	
Size (in bits):	32	
Address:	00D08h	
Unit Level Clock Gating Control Registers		
DWord	Bit	Description
0	31:5	Placeholder Bits
		Access: R/W Lock Placeholder bits for implementation or ECO loops.
	4	Reserved
	3	RPMunit Clock Gating Disable in Uncore Well
		Default Value: 1b
		Access: R/W
	Clock Gating Disable Control: '0': Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality). '1': Clock Gating Disabled. (i.e., clocks are toggling, always) (DEFAULT).	
	2	MGRunit Clock Gating Disable in Uncore Well
		Default Value: 1b
		Access: R/W
Clock Gating Disable Control: '0': Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality). '1': Clock Gating Disabled. (i.e., clocks are toggling, always) (DEFAULT).		
1	MDRBunit Clock Gating Disable in Uncore Well	
	Default Value: 1b	
	Access: R/W	
Clock Gating Disable Control: '0': Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality). '1': Clock Gating Disabled. (i.e., clocks are toggling, always) (DEFAULT).		

RCPCONFIG - Configuration Register for RCPunit					
0	<p>MCRunit Clock Gating Disable in Uncore Well</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Clock Gating Disable Control: '0': Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality). '1': Clock Gating Disabled. (i.e., clocks are toggling, always) (DEFAULT).</p>	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				

Context Load Protocol Register BLT

BLT_CTX_LD_PRTCL - Context Load Protocol Register BLT			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000 CHV, BSW		
Size (in bits):	32		
Address:	04014h		
DWord	Bit	Description	
0	31:16	Mask Bits	
		Default Value:	0000h
		Access:	RO
	15	Context Load Protocol Register - BCS 15	
		Default Value:	0b
		Access:	R/W
	For Future Use. This bit is self clear.		
	14	Context Load Protocol Register - BCS 14	
		Default Value:	0b
		Access:	R/W
	For Future Use. This bit is self clear.		
	13	Context Load Protocol Register - BCS 13	
		Default Value:	0b
		Access:	R/W
	For Future Use. This bit is self clear.		
	12	Context Load Protocol Register - BCS 12	
Default Value:		0b	
Access:		R/W	
For Future Use. This bit is self clear.			
11	Context Load Protocol Register - BCS 11		
	Default Value:	0b	
	Access:	R/W	
For Future Use. This bit is self clear.			

BLT_CTX_LD_PRTCL - Context Load Protocol Register BLT

10	Context Load Protocol Register - BCS 10		
	Default Value:	0b	
	Access:	R/W	
	For Future Use. This bit is self clear.		
	9	Context Load Protocol Register - BCS 9	
		Default Value:	0b
		Access:	R/W
	For Future Use. This bit is self clear.		
8	Context Load Protocol Register - BCS 8		
	Default Value:	0b	
	Access:	R/W	
For Future Use. This bit is self clear.			
7	Context Load Protocol Register - BCS 7		
	Default Value:	0b	
	Access:	R/W	
For Future Use. This bit is self clear.			
6	Context Load Protocol Register - BCS 6		
	Default Value:	0b	
	Access:	R/W	
For Future Use. This bit is self clear.			
5	Context Load Protocol Register - BCS 5		
	Default Value:	0b	
	Access:	R/W	
For Future Use. This bit is self clear.			
4	Context Load Protocol Register - BCS 4		
	Default Value:	0b	
	Access:	R/W	
For Future Use. This bit is self clear.			
3	Context Load Protocol Register - BCS 3		
	Default Value:	0b	
	Project:	CHV, BSW	
Access:		R/W	

BLT_CTX_LD_PRTCL - Context Load Protocol Register BLT					
	<p>Bit 3 = Context Complete. Only valid with Bit 2 asserted and indicates whether the context switching out as complete vs. incomplete. This bit is self clear.</p>				
2	<p>Context Load Protocol Register - BCS 2</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Context Load Protocol Register (Written by BCS) Bit 2 = Request from BCS to GAM for context save readiness. GAM will acknowledge appropriated steps taken. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
1	<p>Context Load Protocol Register - BCS 1</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Context Load Protocol Register (Written by BCS) Bit 1 = Context Launched. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
0	<p>Context Load Protocol Register - BCS 0</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Context Load Protocol Register (Written by BCS) Bit 0 = Context Available. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				

Context Load Protocol Register CS

GFX_CTX_LD_PRTCL - Context Load Protocol Register CS			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000 CHV, BSW		
Size (in bits):	32		
Address:	04004h		
DWord	Bit	Description	
0	31:16	Mask Bits	
		Default Value:	0000h
		Access:	RO
	15	Context Load Protocol Register - CS 15	
		Default Value:	0b
		Access:	R/W
			For Future Use. This bit is self clear.
	14	Context Load Protocol Register - CS 14	
		Default Value:	0b
		Access:	R/W
			For Future Use. This bit is self clear.
	13	Context Load Protocol Register - CS 13	
		Default Value:	0b
		Access:	R/W
			For Future Use. This bit is self clear.
	12	Context Load Protocol Register - CS 12	
Default Value:		0b	
Access:		R/W	
		For Future Use. This bit is self clear.	
11	Context Load Protocol Register - CS 11		
	Default Value:	0b	
	Access:	R/W	
		For Future Use. This bit is self clear.	

GFX_CTX_LD_PRTCL - Context Load Protocol Register CS

10	Context Load Protocol Register - CS 10	
	Default Value:	0b
	Access:	R/W
	For Future Use. This bit is self clear.	
9	Context Load Protocol Register - CS 9	
	Default Value:	0b
	Access:	R/W
	For Future Use. This bit is self clear.	
8	Context Load Protocol Register - CS 8	
	Default Value:	0b
	Access:	R/W
	For Future Use. This bit is self clear.	
7	Context Load Protocol Register - CS 7	
	Default Value:	0b
	Access:	R/W
	For Future Use. This bit is self clear.	
6	Context Load Protocol Register - CS 6	
	Default Value:	0b
	Access:	R/W
	For Future Use. This bit is self clear.	
5	Context Load Protocol Register - CS 5	
	Default Value:	0b
	Access:	R/W
	For Future Use. This bit is self clear.	
4	Context Load Protocol Register - CS 4	
	Default Value:	0b
	Access:	R/W
	For Future Use. This bit is self clear.	
3	Context Load Protocol Register - CS 3	
	Default Value:	0b
	Project:	CHV, BSW
	Access:	R/W

GFX_CTX_LD_PRTCL - Context Load Protocol Register CS

		<p>Bit 3 = Context Complete. Only valid with Bit 2 asserted and indicates whether the context switching out as complete vs. incomplete. This bit is self clear.</p>					
2	<p>Context Load Protocol Register - CS 2</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Context Load Protocol Register (Written by CS) Bit 2 = Request from CS to GAM for context save readiness. GAM will acknowledge appropriated steps taken. This bit is self clear.</p>			Default Value:	0b	Access:	R/W
Default Value:	0b						
Access:	R/W						
1	<p>Context Load Protocol Register - CS 1</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Context Load Protocol Register (Written by CS) Bit 1 = Context Launched. This bit is self clear.</p>			Default Value:	0b	Access:	R/W
Default Value:	0b						
Access:	R/W						
0	<p>Context Load Protocol Register - CS 0</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Context Load Protocol Register (Written by CS) Bit 0 = Context Available. This bit is self clear.</p>			Default Value:	0b	Access:	R/W
Default Value:	0b						
Access:	R/W						

Context Load Protocol Register VCS0

MFX0_CTX_LD_PRTCL - Context Load Protocol Register VCS0			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000 CHV, BSW		
Size (in bits):	32		
Address:	04008h		
DWord	Bit	Description	
0	31:16	Mask Bits	
		Default Value:	0000h
		Access:	RO
	15	Context Load Protocol Register - VCS0 15	
		Default Value:	0b
		Access:	R/W
			For Future Use. This bit is self clear.
	14	Context Load Protocol Register - VCS0 14	
		Default Value:	0b
		Access:	R/W
			For Future Use. This bit is self clear.
	13	Context Load Protocol Register - VCS0 13	
		Default Value:	0b
		Access:	R/W
			For Future Use. This bit is self clear.
	12	Context Load Protocol Register - VCS0 12	
		Default Value:	0b
		Access:	R/W
			For Future Use. This bit is self clear.
	11	Context Load Protocol Register - VCS0 11	
Default Value:		0b	
Access:		R/W	
		For Future Use. This bit is self clear.	

MFX0_CTX_LD_PRTCL - Context Load Protocol Register VCS0

10	Context Load Protocol Register - VCS0 10	
	Default Value:	0b
	Access:	R/W
	For Future Use. This bit is self clear.	
	Context Load Protocol Register - VCS0 9	
	Default Value:	0b
	Access:	R/W
For Future Use. This bit is self clear.		
8	Context Load Protocol Register - VCS0 8	
	Default Value:	0b
	Access:	R/W
For Future Use. This bit is self clear.		
7	Context Load Protocol Register - VCS0 7	
	Default Value:	0b
	Access:	R/W
For Future Use. This bit is self clear.		
6	Context Load Protocol Register - VCS0 6	
	Default Value:	0b
	Access:	R/W
For Future Use. This bit is self clear.		
5	Context Load Protocol Register - VCS0 5	
	Default Value:	0b
	Access:	R/W
For Future Use. This bit is self clear.		
4	Context Load Protocol Register - VCS0 4	
	Default Value:	0b
	Access:	R/W
For Future Use. This bit is self clear.		

MFX0_CTX_LD_PRTCL - Context Load Protocol Register VCS0

3	<p>Context Load Protocol Register - VCS0 3</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td>0b</td> </tr> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit 3 = Context Complete. Only valid with Bit 2 asserted and indicates whether the context switching out as complete vs. incomplete. This bit is self clear.</p>	Default Value:	0b	Project:	CHV, BSW	Access:	R/W
Default Value:	0b						
Project:	CHV, BSW						
Access:	R/W						
2	<p>Context Load Protocol Register - VCS0 2</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Context Load Protocol Register (Written by VCS0) Bit 2 = Request from VCS0 to GAM for context save readiness. GAM will acknowledge appropriated steps taken. This bit is self clear.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b						
Access:	R/W						
1	<p>Context Load Protocol Register - VCS0 1</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Context Load Protocol Register (Written by VCS0) Bit 1 = Context Launched. This bit is self clear.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b						
Access:	R/W						
0	<p>Context Load Protocol Register - VCS0 0</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Context Load Protocol Register (Written by VCS0) Bit 0 = Context Available. This bit is self clear.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b						
Access:	R/W						

Context Load Protocol Register VCS1

MFX1_CTX_LD_PRTCL - Context Load Protocol Register VCS1			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000 CHV, BSW		
Size (in bits):	32		
Address:	0400Ch		
DWord	Bit	Description	
0	31:16	Mask Bits	
		Default Value:	0000h
		Access:	RO
	15	Context Load Protocol Register - VCS1 15	
		Default Value:	0b
		Access:	R/W
			For Future Use. This bit is self clear.
	14	Context Load Protocol Register - VCS1 14	
		Default Value:	0b
		Access:	R/W
			For Future Use. This bit is self clear.
	13	Context Load Protocol Register - VCS1 13	
		Default Value:	0b
		Access:	R/W
			For Future Use. This bit is self clear.
12	Context Load Protocol Register - VCS1 12		
	Default Value:	0b	
	Access:	R/W	
		For Future Use. This bit is self clear.	
11	Context Load Protocol Register - VCS1 11		
	Default Value:	0b	
	Access:	R/W	
		For Future Use. This bit is self clear.	

MFX1_CTX_LD_PRTCL - Context Load Protocol Register VCS1

10	<p>Context Load Protocol Register - VCS1 10</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
9	<p>Context Load Protocol Register - VCS1 9</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
8	<p>Context Load Protocol Register - VCS1 8</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
7	<p>Context Load Protocol Register - VCS1 7</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
6	<p>Context Load Protocol Register - VCS1 6</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
5	<p>Context Load Protocol Register - VCS1 5</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
4	<p>Context Load Protocol Register - VCS1 4</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				

MFX1_CTX_LD_PRTCL - Context Load Protocol Register VCS1

3	Context Load Protocol Register - VCS1 3	
	Default Value:	0b
	Project:	CHV, BSW
	Access:	R/W
	<p>Bit 3 = Context Complete. Only valid with Bit 2 asserted and indicates whether the context switching out as complete vs. incomplete. This bit is self clear.</p>	
2	Context Load Protocol Register - VCS1 2	
	Default Value:	0b
	Access:	R/W
	<p>Context Load Protocol Register (Written by VCS1) Bit 2 = Request from VCS1 to GAM for context save readiness. GAM will acknowledge appropriated steps taken. This bit is self clear.</p>	
1	Context Load Protocol Register - VCS1 1	
	Default Value:	0b
	Access:	R/W
	<p>Context Load Protocol Register (Written by VCS1) Bit 1 = Context Launched This bit is self clear.</p>	
0	Context Load Protocol Register - VCS1 0	
	Default Value:	0b
	Access:	R/W
	<p>Context Load Protocol Register (Written by VCS1) Bit 0 = Context Available. This bit is self clear.</p>	

Context Load Protocol Register VEBX

VEBX_CTX_LD_PRTCL - Context Load Protocol Register VEBX			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000 CHV, BSW		
Size (in bits):	32		
Address:	04010h		
DWord	Bit	Description	
0	31:16	Mask Bits	
		Default Value:	0000h
		Access:	RO
	15	Context Load Protocol Register - VEBX 15	
		Default Value:	0b
		Access:	R/W
			For Future Use. This bit is self clear.
	14	Context Load Protocol Register - VEBX 14	
		Default Value:	0b
		Access:	R/W
			For Future Use. This bit is self clear.
	13	Context Load Protocol Register - VEBX 13	
		Default Value:	0b
		Access:	R/W
			For Future Use. This bit is self clear.
	12	Context Load Protocol Register - VEBX 12	
		Default Value:	0b
		Access:	R/W
			For Future Use. This bit is self clear.
	11	Context Load Protocol Register - VEBX 11	
Default Value:		0b	
Access:		R/W	
		For Future Use. This bit is self clear.	

VEBX_CTX_LD_PRTCL - Context Load Protocol Register VEBX

10	Context Load Protocol Register - VEBX 10		
	Default Value:	0b	
	Access:	R/W	
	For Future Use. This bit is self clear.		
	9	Context Load Protocol Register - VEBX 9	
		Default Value:	0b
		Access:	R/W
For Future Use. This bit is self clear.			
8	Context Load Protocol Register - VEBX 8		
	Default Value:	0b	
	Access:	R/W	
For Future Use. This bit is self clear.			
7	Context Load Protocol Register - VEBX 7		
	Default Value:	0b	
	Access:	R/W	
For Future Use. This bit is self clear.			
6	Context Load Protocol Register - VEBX 6		
	Default Value:	0b	
	Access:	R/W	
For Future Use. This bit is self clear.			
5	Context Load Protocol Register - VEBX 5		
	Default Value:	0b	
	Access:	R/W	
For Future Use. This bit is self clear.			
4	Context Load Protocol Register - VEBX 4		
	Default Value:	0b	
	Access:	R/W	
For Future Use. This bit is self clear.			

VEBX_CTX_LD_PRTCL - Context Load Protocol Register VEBX

3	<p>Context Load Protocol Register - VEBX 3</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td>0b</td> </tr> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit 3 = Context Complete. Only valid with Bit 2 asserted and indicates whether the context switching out as complete vs. incomplete. This bit is self clear.</p>	Default Value:	0b	Project:	CHV, BSW	Access:	R/W
Default Value:	0b						
Project:	CHV, BSW						
Access:	R/W						
2	<p>Context Load Protocol Register - VEBX 2</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Context Load Protocol Register (Written by VEBX) Bit 2 = Request from VEBX to GAM for context save readiness. GAM will acknowledge appropriated steps taken. This bit is self clear.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b						
Access:	R/W						
1	<p>Context Load Protocol Register - VEBX 1</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Context Load Protocol Register (Written by VEBX) Bit 1 = Context Launched. This bit is self clear.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b						
Access:	R/W						
0	<p>Context Load Protocol Register - VEBX 0</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Context Load Protocol Register (Written by VEBX) Bit 0 = Context Available. This bit is self clear.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b						
Access:	R/W						

Context Restore Request To TDL

TDL_CONTEXT_RESTORE - Context Restore Request To TDL								
Register Space:	MMIO: 0/2/0							
Project:	CHV, BSW							
Source:	PRM							
Default Value:	0x00000000							
Access:	WO							
Size (in bits):	32							
Address:	0E440h							
Valid Projects:	CHV, BSW							
DWord	Bit	Description						
0	31:17	Reserved Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td> </td><td>MBZ</td></tr></table>		MBZ				
		MBZ						
	16	Context Restore Mask <table border="1" style="display: inline-table; vertical-align: middle;"><thead><tr><th>Value</th><th>Name</th><th>Description</th></tr></thead><tbody><tr><td>1</td><td> </td><td>Bit 0 and bit 16 both need to be 1 for Context restore request</td></tr></tbody></table>	Value	Name	Description	1		Bit 0 and bit 16 both need to be 1 for Context restore request
	Value	Name	Description					
1		Bit 0 and bit 16 both need to be 1 for Context restore request						
15:1	Reserved Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td> </td><td>MBZ</td></tr></table>		MBZ					
	MBZ							
0	Context Restore <table border="1" style="display: inline-table; vertical-align: middle;"><thead><tr><th>Value</th><th>Name</th><th>Description</th></tr></thead><tbody><tr><td>1</td><td> </td><td>Bit 0 and bit 16 both need to be 1 for Context restore request</td></tr></tbody></table>	Value	Name	Description	1		Bit 0 and bit 16 both need to be 1 for Context restore request	
Value	Name	Description						
1		Bit 0 and bit 16 both need to be 1 for Context restore request						

Context Save Request To TDL

TDL_CONTEXT_SAVE - Context Save Request To TDL								
Register Space:	MMIO: 0/2/0							
Project:	CHV, BSW							
Source:	PRM							
Default Value:	0x00000000							
Access:	WO							
Size (in bits):	32							
Address:	0E4FCh							
Valid Projects:	CHV, BSW							
DWord	Bit	Description						
0	31:17	Reserved						
		Format: MBZ						
	16	Context Save Mask						
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td></td> <td>Bit 0 and Bit 16 both need to be '1' for Context Save Request</td> </tr> </tbody> </table>	Value	Name	Description	1		Bit 0 and Bit 16 both need to be '1' for Context Save Request
		Value	Name	Description				
	1		Bit 0 and Bit 16 both need to be '1' for Context Save Request					
	15:1	Reserved						
			Format: MBZ					
0	Context Save							
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td></td> <td>Bit 0 and Bit 16 both need to be '1' for Context Save Request</td> </tr> </tbody> </table>	Value	Name	Description	1		Bit 0 and Bit 16 both need to be '1' for Context Save Request	
	Value	Name	Description					
1		Bit 0 and Bit 16 both need to be '1' for Context Save Request						

Context Sizes

CXT_SIZE - Context Sizes				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	RenderCS			
Default Value:	0x05655582			
Access:	R/W			
Size (in bits):	32			
Trusted Type:	1			
Address:	021A8h			
<p>The actual size of a logical rendering context is the amount of data stored/restored during a context switch and is measured in 64B cache lines.</p> <p>This register will be power context save/restored. Note that this register will default to the correct value, so software should not have to modify it.</p>				
DWord	Bit	Description		
0	31:27	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
	26:24	<p>Ring Context Size</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">5h</td> </tr> </table> <p>This field indicates the Ring context data that needs to be save/restored.</p>	Default Value:	5h
	Default Value:	5h		
	23:16	<p>Render Context Size</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">65h</td> </tr> </table> <p>This field indicates the size of the render context data that needs to be save/restored when extended mode is not enabled for a context; this also excludes VF, VFE, and URB context size.</p>	Default Value:	65h
Default Value:	65h			
15:8	<p>SOL Context Offset</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">55h</td> </tr> </table> <p>This field indicates the cacheline aligned offset of the SOL context in the render context image starting from Ring Context. Note that in execlist of scheduling Ring context itself is at 4KB offset from LRCA.</p>	Default Value:	55h	
Default Value:	55h			
7:0	<p>VF and VFE State Context Size</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">82h</td> </tr> </table> <p>This field indicates the amount of VF and VFE unit data context save/restored in cachelines.</p>	Default Value:	82h	
Default Value:	82h			

Context Status Buffer Contents

CTXT_ST_BUF - Context Status Buffer Contents		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	384	
Trusted Type:	1	
Address:	02370h-0239Fh	
Name:	Context Status Buffer Contents	
ShortName:	CTXT_ST_BUF_RCSUNIT	
Address:	12370h-1239Fh	
Name:	Context Status Buffer Contents	
ShortName:	CTXT_ST_BUF_VCSUNIT0	
Address:	1A370h-1A39Fh	
Name:	Context Status Buffer Contents	
ShortName:	CTXT_ST_BUF_VECSUNIT	
Address:	1C370h-1C39Fh	
Name:	Context Status Buffer Contents	
ShortName:	CTXT_ST_BUF_VCSUNIT1	
Address:	22370h-2239Fh	
Name:	Context Status Buffer Contents	
ShortName:	CTXT_ST_BUF_BCSUNIT	
Contents of the Execlst 0 in HW.		
Programming Notes		
This structure contains the Context Switch status locations Context Status 0 to Context Status 5.		
DWord	Bit	Description
0	63:32	Context Status 0 UDW Format: Context Status CHV, BSW
	31:0	Context Status 0 LDW Format: Context Status CHV, BSW
1	63:32	Context Status 1 UDW Format: Context Status CHV, BSW

CTXT_ST_BUF - Context Status Buffer Contents		
	31:0	Context Status 1 LDW Format: Context Status CHV, BSW
2	63:32	Context Status 2 UDW Format: Context Status CHV, BSW
	31:0	Context Status 2 LDW Format: Context Status CHV, BSW
3	63:32	Context Status 3 UDW Format: Context Status CHV, BSW
	31:0	Context Status 3 LDW Format: Context Status CHV, BSW
4	63:32	Context Status 4 UDW Format: Context Status CHV, BSW
	31:0	Context Status 4 LDW Format: Context Status CHV, BSW
5	63:32	Context Status 5 UDW Format: Context Status CHV, BSW
	31:0	Context Status 5 LDW Format: Context Status CHV, BSW

Control Register for Power Management

WAIT_FOR_RC6_EXIT - Control Register for Power Management				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	RenderCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Trusted Type:	1			
Address:	020CCh			
Address:	120CCh-120CFh			
Name:	Control Register for Power Management			
ShortName:	WAIT_FOR_RC6_EXIT_VCSUNIT0			
Address:	1A0CCh-1A0CFh			
Name:	Control Register for Power Management			
ShortName:	WAIT_FOR_RC6_EXIT_VECSUNIT			
Address:	1C0CCh-1C0CFh			
Name:	Control Register for Power Management			
ShortName:	WAIT_FOR_RC6_EXIT_VCSUNIT1			
Address:	220CCh-220CFh			
Name:	Control Register for Power Management			
ShortName:	WAIT_FOR_RC6_EXIT_BCSUNIT			
DWord	Bit	Description		
	31:16	Mask Bits <table border="1"> <tr> <td>Format:</td> <td>Mask[15:0]</td> </tr> </table> Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)	Format:	Mask[15:0]
	Format:	Mask[15:0]		
15:14	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ			

WAIT_FOR_RC6_EXIT - Control Register for Power Management

0	This register gets power context save/restored. Bit[0] contents of this register doesn't get save/restored.	13	Selective Read Addressing Enable	
		Project:		CHV, BSW
		This field controls the outbound read request originating from Render Command Streamer. This field enables to read the MMIO register from selected unit in a given slice and sub-slice instead of multicasting the read cycle to all slices/sub-slices.		
		Value	Name	Description
		0h	[Default]	Lowest Slice and Lowest Sub-Slice Enabled. Ex: Slice-0, Sub-Slice-0 are the lowest in GT.
		1h	Selective Unit Enabled	Unit selected based on Selective Read Slice Select and Selective Read Sub-Slice Select .
		12:11	Selective Read Slice Select	
		Project:		CHV, BSW
		This field selects the slice from which the read return data value has to be considered when Selective Read Addressing Enable is set. Below value must be programmed with a legal value supported by the GT configuration, one must not program this to a slice that is disabled or not supported by GT.		
			Value	Name
	00b	Slice-0		
	01b	Slice-1		
	10b	Slice-2		
	11b	Reserved		
10:9	Selective Read Sub-Slice Select			
Project:		CHV, BSW		
This field selects the sub-slice from which the read return data value has to be considered when Selective Read Addressing Enable is set. Below value must be programmed with a legal value supported by the GT configuration, one must not program this to a sub-slice that is disabled or not supported by GT.				
	Value	Name		
	00b	Sub Slice-0		
	01b	Sub Slice-1		
	10b	Sub Slice-2		
	11b	Reserved		

WAIT_FOR_RC6_EXIT - Control Register for Power Management

	8	Render Inhibit	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">Disable</td> </tr> </table> <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 5px;"> <thead> <tr style="background-color: #e6f2ff;"> <th style="width: 15%;">Value</th> <th style="width: 20%;">Name</th> <th style="width: 65%;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0h</td> <td style="text-align: center;">Disabled [Default]</td> <td>When not Set CS doesn't take any special action.</td> </tr> <tr> <td style="text-align: center;">1h</td> <td style="text-align: center;">Enabled</td> <td>When Set CS will not save/restore render context as part of power context save/restore. Render context includes RS context as well if enabled.</td> </tr> </tbody> </table> <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 5px;"> <thead> <tr style="background-color: #e6f2ff;"> <th style="width: 100%;">Programming Notes</th> </tr> </thead> <tbody> <tr> <td>If this bit is set S/W should set Resource Streamer Context Enable (Bit[7] of this register)as well.</td> </tr> </tbody> </table>	Format:	Disable	Value	Name	Description	0h	Disabled [Default]	When not Set CS doesn't take any special action.	1h	Enabled	When Set CS will not save/restore render context as part of power context save/restore. Render context includes RS context as well if enabled.	Programming Notes	If this bit is set S/W should set Resource Streamer Context Enable (Bit[7] of this register)as well.
Format:	Disable															
Value	Name	Description														
0h	Disabled [Default]	When not Set CS doesn't take any special action.														
1h	Enabled	When Set CS will not save/restore render context as part of power context save/restore. Render context includes RS context as well if enabled.														
Programming Notes																
If this bit is set S/W should set Resource Streamer Context Enable (Bit[7] of this register)as well.																
	7	Resource Streamer Context Enable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">Enable</td> </tr> </table> <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 5px;"> <thead> <tr style="background-color: #e6f2ff;"> <th style="width: 15%;">Value</th> <th style="width: 20%;">Name</th> <th style="width: 65%;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">1h</td> <td style="text-align: center;">Disable</td> <td>The current context does not include the resource streamer context</td> </tr> <tr> <td style="text-align: center;">0h</td> <td style="text-align: center;">Enable [Default]</td> <td>The current context does include the resource streamer context.</td> </tr> </tbody> </table>	Format:	Enable	Value	Name	Description	1h	Disable	The current context does not include the resource streamer context	0h	Enable [Default]	The current context does include the resource streamer context.		
Format:	Enable															
Value	Name	Description														
1h	Disable	The current context does not include the resource streamer context														
0h	Enable [Default]	The current context does include the resource streamer context.														
	6	Selective Write Addressing Enable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Project:</td> <td style="width: 40%;">CHV, BSW</td> </tr> </table> <p>This field controls the outbound write request on message channel originating from Render Command Streamer on executing MI_LOAD_REGISTER_IMM, MI_LOAD_REGISTER_REG and MI_LOAD_REGISTER_MEM commands. Setting this field doesn't affect the execution of MI_LOAD_REGISTER_IMM command from context image during context restore. This field enables to direct the message channel write cycle to the unit in the selected slice and sub-slice instead of multicasting it to all the instances of the unit in all the slices and sub-slices.</p> <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 5px;"> <thead> <tr style="background-color: #e6f2ff;"> <th style="width: 15%;">Value</th> <th style="width: 20%;">Name</th> <th style="width: 65%;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0h</td> <td style="text-align: center;">Multi Cast [Default]</td> <td></td> </tr> <tr> <td style="text-align: center;">1h</td> <td style="text-align: center;">Selective Unit Enabled</td> <td>Unit selected based on Selective Write Slice Select and Selective Write Sub-Slice Select.</td> </tr> </tbody> </table>	Project:	CHV, BSW	Value	Name	Description	0h	Multi Cast [Default]		1h	Selective Unit Enabled	Unit selected based on Selective Write Slice Select and Selective Write Sub-Slice Select .		
Project:	CHV, BSW															
Value	Name	Description														
0h	Multi Cast [Default]															
1h	Selective Unit Enabled	Unit selected based on Selective Write Slice Select and Selective Write Sub-Slice Select .														

WAIT_FOR_RC6_EXIT - Control Register for Power Management

5:4	Selective Write Slice Select										
	Project:	CHV, BSW									
	This field selects the slice to which the write has to be done when Selective Write Addressing Enable is set. Below value must be programmed with a legal value supported by the GT configuration, one must not program this to a slice that is disabled or not supported by GT.										
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Slice-0</td> </tr> <tr> <td>01b</td> <td>Slice-1</td> </tr> <tr> <td>10b</td> <td>Slice-2</td> </tr> <tr> <td>11b</td> <td>Reserved</td> </tr> </tbody> </table>	Value	Name	00b	Slice-0	01b	Slice-1	10b	Slice-2	11b	Reserved
Value	Name										
00b	Slice-0										
01b	Slice-1										
10b	Slice-2										
11b	Reserved										
3:2	Selective Write Sub-Slice Select										
	Project:	CHV, BSW									
	This field selects the Sub-Slice to which the write has to be done when Selective Write Addressing Enable is set. Below value must be programmed with a legal value supported by the GT configuration, one must not program this to a sub-slice that is disabled or not supported by GT.										
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Sub Slice-0</td> </tr> <tr> <td>01b</td> <td>Sub Slice-1</td> </tr> <tr> <td>10b</td> <td>Sub Slice-2</td> </tr> <tr> <td>11b</td> <td>Reserved</td> </tr> </tbody> </table>	Value	Name	00b	Sub Slice-0	01b	Sub Slice-1	10b	Sub Slice-2	11b	Reserved
Value	Name										
00b	Sub Slice-0										
01b	Sub Slice-1										
10b	Sub Slice-2										
11b	Reserved										
1	Reserved										
	Format:	MBZ									
0	WAIT FOR RC6 EXIT										
	Format:	Disable									
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disabled [Default]</td> <td>When not Set CS doesn't take any action.</td> </tr> <tr> <td>1h</td> <td>Enabled</td> <td>When Set CS will stop on the next appropriate command boundary and will initiate IDLE sequence with PM.</td> </tr> </tbody> </table>	Value	Name	Description	0h	Disabled [Default]	When not Set CS doesn't take any action.	1h	Enabled	When Set CS will stop on the next appropriate command boundary and will initiate IDLE sequence with PM.	
	Value	Name	Description								
0h	Disabled [Default]	When not Set CS doesn't take any action.									
1h	Enabled	When Set CS will stop on the next appropriate command boundary and will initiate IDLE sequence with PM.									
Programming Notes											
WAIT_FOR_RC6_EXIT functionality is only supported in ring buffer mode of scheduling and not supported in exelist mode of scheduling.											

Count Active Channels Dispatched

TS_GPGPU_THREADS_DISPATCHED - Count Active Channels Dispatched				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	RenderCS			
Default Value:	0x00000000, 0x00000000			
Access:	R/W			
Size (in bits):	64			
Trusted Type:	1			
Address:	02290h			
<p>This register is used to count the number of active channels that TS sends for dispatch. For each dispatch the active bits in the execution mask are summed and added to this register. This register is reset when a write occurs to 2290h</p>				
DWord	Bit	Description		
0	63:32	<p>GPGPU_THREADS_DISPATCHED UDW</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U32</td> </tr> </table> <p>This count is increased by the number of active bits in the execution mask each time the TS sends a GPGPU dispatch.</p>	Format:	U32
	Format:	U32		
31:0	<p>GPGPU_THREADS_DISPATCHED LDW</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U32</td> </tr> </table> <p>This count is increased by the number of active bits in the execution mask each time the TS sends a GPGPU dispatch.</p>	Format:	U32	
Format:	U32			

CS Context Timestamp Count

CS_CTX_TIMESTAMP - CS Context Timestamp Count				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	RenderCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	023A8h			
<p>This register provides a mechanism to obtain cumulative run time of a GPU context on HW. This register gets context save/restored on a context switch. SW must reset this register on very first submission of a context to HW, then afterwards gets context save/restored maintaining the cumulative run time of the corresponding context. This register (effectively) counts at a constant frequency by adjusting the increment amount according to the actual reference clock frequency. SW therefore does not need to know the reference clock frequency. This register gets reset on an engine reset.</p> <p>This register is context save restore on a context switch. The time to execute the context switch is included in the CS_CTX_TIMESTAMP register.</p>				
DWord	Bit	Description		
0	31:0	<p>Timestamp Value</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>This register increments for every 80 ns of time.</p>	Format:	U32
Format:	U32			

CS General Purpose Register

CS_GPR - CS General Purpose Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	02600h
Name:	CS General Purpose Register 0
ShortName:	CS_GPR_R_0
Address:	02608h
Name:	CS General Purpose Register 1
ShortName:	CS_GPR_R_1
Address:	02610h
Name:	CS General Purpose Register 2
ShortName:	CS_GPR_R_2
Address:	02618h
Name:	CS General Purpose Register 3
ShortName:	CS_GPR_R_3
Address:	02620h
Name:	CS General Purpose Register 4
ShortName:	CS_GPR_R_4
Address:	02628h
Name:	CS General Purpose Register 5
ShortName:	CS_GPR_R_5
Address:	02630h
Name:	CS General Purpose Register 6
ShortName:	CS_GPR_R_6
Address:	02638h
Name:	CS General Purpose Register 7
ShortName:	CS_GPR_R_7
Address:	02640h
Name:	CS General Purpose Register 8
ShortName:	CS_GPR_R_8

CS_GPR - CS General Purpose Register	
Address:	02648h
Name:	CS General Purpose Register 9
ShortName:	CS_GPR_R_9
Address:	02650h
Name:	CS General Purpose Register 10
ShortName:	CS_GPR_R_10
Address:	02658h
Name:	CS General Purpose Register 11
ShortName:	CS_GPR_R_11
Address:	02660h
Name:	CS General Purpose Register 12
ShortName:	CS_GPR_R_12
Address:	02668h
Name:	CS General Purpose Register 13
ShortName:	CS_GPR_R_13
Address:	02670h
Name:	CS General Purpose Register 14
ShortName:	CS_GPR_R_14
Address:	02678h
Name:	CS General Purpose Register 15
ShortName:	CS_GPR_R_15
Address:	12600h-12607h
Name:	General Purpose Register
ShortName:	CS_GPR_VCSUNIT0
Address:	1A600h-1A607h
Name:	General Purpose Register
ShortName:	CS_GPR_VECSUNIT
Address:	1C600h-1C607h
Name:	General Purpose Register
ShortName:	CS_GPR_VCSUNIT1
Address:	22600h-22607h
Name:	General Purpose Register
ShortName:	CS_GPR_BCSUNIT
<p>This is a General Purpose Register bank of sixteen 64bit registers, which will be used as temporary storage by MI_MATH command to do ALU operations.</p>	

CS_GPR - CS General Purpose Register

GPR Index	MMIO Offset
R_0	0x2600
R_1	0x2608
R_2	0x2610
R_3	0x2618
R_4	0x2620
R_5	0x2628
R_6	0x2630
R_7	0x2638
R_8	0x2640
R_9	0x2648
R_10	0x2650
R_11	0x2658
R_12	0x2660
R_13	0x2668
R_14	0x2670
R_15	0x2678

DWord	Bit	Description		
0	63:0	<p>CS_GPR_DATA</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This register is a temporary register for ALU operations. See MI_MATH command for more details.</p>	Project:	CHV, BSW
Project:	CHV, BSW			

CS Power Management FSM

CSPWRFSM - CS Power Management FSM																														
Register Space:	MMIO: 0/2/0																													
Project:	CHV, BSW																													
Source:	RenderCS																													
Default Value:	0x00000000																													
Access:	RO																													
Size (in bits):	32																													
Address:	022ACh																													
<p>This register contains the state code of the Power Management FSM, FBC Forward FSM, CSSTDT FSM, CSARB FSM, CSBUPDATE FSM. Decoding the contents of this register will indicate what the state of the corresponding state machine.</p>																														
DWord	Bit	Description																												
0	31:30	Reserved Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td> </td><td>MBZ</td></tr></table>		MBZ																										
		MBZ																												
	29:28	CSFBCSLICE0 Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td> </td><td>U2</td></tr></table> FBC message forward FSM state <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr><td>0h</td><td>CSFBCIDLE_0</td></tr> <tr><td>1h</td><td>CSFBCMODIFY_0</td></tr> <tr><td>2h</td><td>CSFBCCLEAN_0</td></tr> <tr><td>3h</td><td>CSFBCDONE_0</td></tr> </tbody> </table>		U2	Value	Name	0h	CSFBCIDLE_0	1h	CSFBCMODIFY_0	2h	CSFBCCLEAN_0	3h	CSFBCDONE_0																
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	27:24	Reserved Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td> </td><td>MBZ</td></tr></table>		MBZ																										
	MBZ																													
23:21	CS ARB Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td> </td><td>U3</td></tr></table> Overall state of the command streamer. Describes what state CS is in <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> </thead> <tbody> <tr><td>0h</td><td>ARBIDLE_s</td><td></td></tr> <tr><td>1h</td><td>PORNG_s CS</td><td></td></tr> <tr><td>2h</td><td>POBATCH_s</td><td></td></tr> <tr><td>3h</td><td>ARBCHK</td><td></td></tr> <tr><td>4h</td><td>ARBCHK1</td><td></td></tr> <tr><td>5h</td><td>CTXOP_s</td><td></td></tr> <tr><td>6h</td><td>WABATCH_s</td><td>CHV, BSW</td></tr> <tr><td>7h</td><td>PSLBATCH</td><td>CHV, BSW</td></tr> </tbody> </table>		U3	Value	Name	Project	0h	ARBIDLE_s		1h	PORNG_s CS		2h	POBATCH_s		3h	ARBCHK		4h	ARBCHK1		5h	CTXOP_s		6h	WABATCH_s	CHV, BSW	7h	PSLBATCH	CHV, BSW
	U3																													
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7h	PSLBATCH	CHV, BSW																												

CSPWRFSM - CS Power Management FSM																															
20	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">MBZ</td> </tr> </table>	Format:	MBZ																												
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19:17	<p>CSSWITCH</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">U3</td> </tr> </table> <p>Arbiters CSSWITCH FSM state decoding.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 40%;">Value</th> <th style="width: 60%;">Name</th> </tr> </thead> <tbody> <tr><td>0h</td><td>SWIDLE_s</td></tr> <tr><td>1h</td><td>SWITCH_s</td></tr> <tr><td>2h</td><td>ASREQ_s</td></tr> <tr><td>3h</td><td>DMACHK_s</td></tr> <tr><td>4h</td><td>ARBWAIT_s</td></tr> <tr><td>5h</td><td>FIFORECFG_s</td></tr> <tr><td>6h-7h</td><td>Reserved</td></tr> </tbody> </table>	Format:	U3	Value	Name	0h	SWIDLE_s	1h	SWITCH_s	2h	ASREQ_s	3h	DMACHK_s	4h	ARBWAIT_s	5h	FIFORECFG_s	6h-7h	Reserved												
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16:13	<p>CSCSBUPDATE</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">U4</td> </tr> </table> <p>CS Power Management CSBLOCK FSM state</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 40%;">Value</th> <th style="width: 60%;">Name</th> </tr> </thead> <tbody> <tr><td>0h</td><td>CSBIDLE</td></tr> <tr><td>1h</td><td>CSQ</td></tr> <tr><td>2h</td><td>WRPTR</td></tr> <tr><td>3h</td><td>SEMA1</td></tr> <tr><td>4h</td><td>SEMA2</td></tr> <tr><td>5h</td><td>TS1</td></tr> <tr><td>6h</td><td>TS2</td></tr> <tr><td>7h</td><td>TS3</td></tr> <tr><td>8h</td><td>TS4</td></tr> <tr><td>9h</td><td>DUMMYREQ</td></tr> <tr><td>Ah</td><td>DUMMYWT</td></tr> <tr><td>Bh</td><td>INTWT</td></tr> <tr><td>Ch-Fh</td><td>Reserved</td></tr> </tbody> </table>	Format:	U4	Value	Name	0h	CSBIDLE	1h	CSQ	2h	WRPTR	3h	SEMA1	4h	SEMA2	5h	TS1	6h	TS2	7h	TS3	8h	TS4	9h	DUMMYREQ	Ah	DUMMYWT	Bh	INTWT	Ch-Fh	Reserved
Format:	U4																														
Value	Name																														
0h	CSBIDLE																														
1h	CSQ																														
2h	WRPTR																														
3h	SEMA1																														
4h	SEMA2																														
5h	TS1																														
6h	TS2																														
7h	TS3																														
8h	TS4																														
9h	DUMMYREQ																														
Ah	DUMMYWT																														
Bh	INTWT																														
Ch-Fh	Reserved																														

CSPWRFSM - CS Power Management FSM

12:11	R2MWRREQ		U2
		Format:	
CSSTDT memory request FSM state			
		Value	Name
		0h	WRIDLE
		1h	WRREQ_HW1
		2h	WRREQ_HW2
		3h	WRRD
10	Reserved		
		Format:	MBZ
9:7	LOADARB		U3
		Format:	
CSSTDT arbiter FSM state			
		Value	Name
		0h	LDIDLE
		1h	LDAUTO
		2h	LDPRSR
		3h	LDCTX
		4h	LDFLSH
		5h	LDREG
		6h	LDSHR1
Programming Notes			
LOADARB FSM states needs 4 bits for encoding, however only 3bits have been mapped on MMIO. 8h -> LDLRM is the state which is missed out, due to less bits mapped, LDLRM/LDIDLE cant be resolved with certain.			
6:4	CSBLOCK		U3
		Format:	
CS Power Management CSBLOCK FSM state			
		Value	Name
		0h	CSBLOCK
		1h	CSCTXARB
		2h	CSUNBLOCKRESTORE
		3h	CSUNBLOCK
		4h	CSPREP4BLOCK
		5h-7h	Reserved

CSPWRFSM - CS Power Management FSM

3:0	CSIDLE	
	Format:	U4
	CS Power Management CSBLOCK FSM state	
	Value	Name
	0h	CSBUSY
	1h	CNTWT
	2h	FLSHREQ
	3h	FLSHWT
	4h	CTXSAVE
	5h	CSREQBLOCK
	6h	PMTURNOFF
	7h	PMIDLEWT
	8h	IDLE
	9h	PMTURNON
	Ah	PMBUSYWT
Bh	DOPFFCGREQ	
Ch	DOPFFCGWAIT	
Dh	DOPFFCG	
Eh	DOPFFCUGREQ	
Fh	DOPFFCUGWAIT	

CSPREEMPT

CSPREEMPT - CSPREEMPT			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	RenderCS		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Trusted Type:	1		
Address:	024B0h		
Programming Notes			
This is for HW internal usage and must not be written by SW.			
DWord	Bit	Description	
0	31:16	Mask Bits	
		Project:	CHV, BSW
		Format:	Mask[15:0]
		Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)	
	15:1	Reserved	
		Project:	CHV, BSW
		Format:	MBZ
	0	Unnamed	
		Project:	CHV, BSW
Format:		Disable	
This is a message bit written by the cross CS in case of GT4-CBR/SFR mode of operation. To set this bit both bit[0] and bit[16] (mask) needs to be set. This bit set indicates CS in other GT has reached a preemption point. This bit gets reset by CS when preemption takes place.			

CS Reset Control Register

CS_RESET_CTRL - CS Reset Control Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	020D0h	
This register is to be used to control soft reset.		
DWord	Bit	Description
0	31:16	Mask Bits
		Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>Mask[15:0]</td></tr></table> Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	Mask[15:0]	
	15:2	Reserved
Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>MBZ</td></tr></table>		MBZ
MBZ		
1	Ready for Reset	
	Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>U1</td></tr></table> When set indicates render engine is ready for reset. This bit gets cleared on engine reset or when Soft Reset In progress is cleared.	U1
U1		
0	Request Reset	
	Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>U1</td></tr></table> When set indicates SW wishes to reset the render engine. On seeing this bit set Command Streamer will take appropriate action and set Ready For Reset status bit. This bit gets cleared on engine reset.	U1
U1		

Current Context Register

CCID - Current Context Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	RenderCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	02180h			
Address:	12180h-12183h			
Name:	Current Context Register			
ShortName:	CCID_VCSUNIT0			
Address:	1A180h-1A183h			
Name:	Current Context Register			
ShortName:	CCID_VECSUNIT			
Address:	1C180h-1C183h			
Name:	Current Context Register			
ShortName:	CCID_VCSUNIT1			
Address:	22180h-22183h			
Name:	Current Context Register			
ShortName:	CCID_BCSUNIT			
<p>This register contains the current logical rendering context address associated with the ring buffer in ring buffer mode of scheduling. This register contents are not valid in Exec-List mode of scheduling.</p>				
Programming Notes				
<p>The CCID register must not be written directly (via MMIO) unless the Command Streamer is completely idle (i.e., the Ring Buffer is empty and the pipeline is idle). Note that, under normal conditions, the CCID register should only be updated from the command stream using the MI_SET_CONTEXT command.</p>				
DWord	Bit	Description		
0	31:12	Logical Render Context Address (LRCA)		
		<table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[31:12]</td> </tr> </table> <p>This field contains the 4 KB-aligned Graphics Memory Address of the current Logical Rendering Context. Bit 11 MBZ.</p>	Default Value:	0h
Default Value:	0h			
Format:	GraphicsAddress[31:12]			
	11:10	Reserved		
		<table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			

CCID - Current Context Register		
9	HD DVD Context	
	Value	Name
	Description	
	0h	Regular Context
	1h	HD DVD Context Special considerations for TDP allow for higher voltage and frequency.
8	Reserved	
	Format:	Must Be One
7:4	Reserved	
	Format:	MBZ
3	Extended State Save Enable	
	Format:	Enable
	If set, the extended state identified in the Logical Context Data section of the Memory Data Formats chapter, is saved as part of switching away from this logical context.	
2	Extended State Restore Enable	
	Format:	Enable
	If set, the extended state identified in the Logical Context Data section of the Memory Data Formats chapter, was loaded (or restored) as part of switching to this logical context.	
1	Reserved	
	Format:	MBZ
0	Valid	
	Format:	U1
	Value	Name
	Description	
	0h	Invalid [Default]
	1h	Valid
	The other fields of this register are invalid. A switch away from the context will not invoke a context save operation.	
	The other fields of this register are valid, and a switch from the context will invoke the normal context save/restore operations.	

Current Idle/Busy/Avg Count for Freq Down Recommendation

RPCURDN - Current Idle/Busy/Avg Count for Freq Down Recommendation				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A060h-0A063h			
DWord	Bit	Description		
0	31:24	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
23:0	Current Busy in Down EI <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reports the current busyness in the down evaluation interval</p> <p>0 = 0 usec 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec</p> <p>pmcr_current_ei_down_busy[23:0]</p>	Access:	RO	
Access:	RO			

Current Idle/Busy/Avg Count for Freq Up Recommendation

RPCURUP - Current Idle/Busy/Avg Count for Freq Up Recommendation				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A054h-0A057h			
DWord	Bit	Description		
0	31:24	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
23:0	Current Busy in UP EI <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reports the current busyness in the UP evaluation interval</p> <p>0 = 0 usec 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec</p> <p>pmcr_current_ei_up_busy[23:0]</p>	Access:	RO	
Access:	RO			

Current Time in DOWN EI

RPCURDNEI - Current Time in DOWN EI				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A05Ch-0A05Fh			
DWord	Bit	Description		
0	31:24	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
23:0	Current Time in Down EI <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reports the current Time in the down evaluation interval</p> <p>0 = 0 usec 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec</p> <p>pmcr_current_ei_down_time[23:0]</p>	Access:	RO	
Access:	RO			

Current Time in UP EI

RPCURUPEI - Current Time in UP EI				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A050h-0A053h			
DWord	Bit	Description		
0	31:24	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
23:0	Current Time <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reports the current time in UP EI</p> <p>0 = 0 usec 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec</p> <p>pmcr_current_ei_up_time[23:0]</p>	Access:	RO	
Access:	RO			

Customizable Event Creation 0-0

CEC0-0 - Customizable Event Creation 0-0															
Register Space:	MMIO: 0/2/0														
Project:	CHV, BSW														
Source:	PRM														
Default Value:	0x00000000														
Access:	R/W														
Size (in bits):	32														
Address:	02770h														
Valid Projects:	CHV, BSW														
<p>This register is used to define custom counter event 0, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.</p>															
DWord	Bit	Description													
0	31:21	Negate <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U11</td> </tr> </table> <p>The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Pass-through</td> <td>Input bit is passed through to comparator as is</td> </tr> <tr> <td>1b</td> <td>Negated</td> <td>Input bit is negated before passing to comparator</td> </tr> </tbody> </table>	Project:	CHV, BSW	Format:	U11	Value	Name	Description	0b	Pass-through	Input bit is passed through to comparator as is	1b	Negated	Input bit is negated before passing to comparator
		Project:	CHV, BSW												
		Format:	U11												
Value	Name	Description													
0b	Pass-through	Input bit is passed through to comparator as is													
1b	Negated	Input bit is negated before passing to comparator													
20:19		Source Select <table border="1"> <tr> <td>Format:</td> <td>U2</td> </tr> </table> <p>Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>01b</td> <td>Prev Event</td> <td>Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block</td> </tr> <tr> <td>11b</td> <td>Reserved</td> <td></td> </tr> </tbody> </table>	Format:	U2	Value	Name	Description	01b	Prev Event	Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block	11b	Reserved			
		Format:	U2												
		Value	Name	Description											
01b	Prev Event	Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block													
11b	Reserved														
18:3		Compare Value <table border="1"> <tr> <td>Format:</td> <td>U16</td> </tr> </table> <p>The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.</p>	Format:	U16											
		Format:	U16												

CEC0-0 - Customizable Event Creation 0-0

2:0	Compare Function		
	Format:	U3	
	This field selects the function used by the CEC0 comparator when comparing the compare value to the value active on the CEC0 conditioned input bus (see block diagram in the Custom Event Counters section).		
	Value	Name	Description
	000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
	001b	Greater Than	Compare and assert output if greater than
	010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
	011b	Greater Than or Equal	Compare and assert output if greater than or equal
	100b	Less Than	Compare and assert output if less than
	101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal	
111b	Reserved		

Customizable Event Creation 1-0

CEC1-0 - Customizable Event Creation 1-0															
Register Space:	MMIO: 0/2/0														
Project:	CHV, BSW														
Source:	PRM														
Default Value:	0x00000000														
Access:	R/W														
Size (in bits):	32														
Address:	02778h														
Valid Projects:	CHV, BSW														
<p>This register is used to define custom counter event 1, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.</p>															
DWord	Bit	Description													
0	31:21	Negate <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U11</td> </tr> </table> <p>The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Pass-through</td> <td>Input bit is passed through to comparator as is</td> </tr> <tr> <td>1b</td> <td>Negated</td> <td>Input bit is negated before passing to comparator</td> </tr> </tbody> </table>	Project:	CHV, BSW	Format:	U11	Value	Name	Description	0b	Pass-through	Input bit is passed through to comparator as is	1b	Negated	Input bit is negated before passing to comparator
		Project:	CHV, BSW												
		Format:	U11												
Value	Name	Description													
0b	Pass-through	Input bit is passed through to comparator as is													
1b	Negated	Input bit is negated before passing to comparator													
20:19		Source Select <table border="1"> <tr> <td>Format:</td> <td>U2</td> </tr> </table> <p>Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>01b</td> <td>Prev Event</td> <td>Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block</td> </tr> <tr> <td>11b</td> <td>Reserved</td> <td></td> </tr> </tbody> </table>	Format:	U2	Value	Name	Description	01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block	11b	Reserved			
		Format:	U2												
		Value	Name	Description											
01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block													
11b	Reserved														
18:3		Compare Value <table border="1"> <tr> <td>Format:</td> <td>U16</td> </tr> </table> <p>The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.</p>	Format:	U16											
		Format:	U16												

CEC1-0 - Customizable Event Creation 1-0

2:0	Compare Function		
	Format:	U3	
	This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).		
	Value	Name	
	Description		
	000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
	001b	Greater Than	Compare and assert output if greater than
	010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
	011b	Greater Than or Equal	Compare and assert output if greater than or equal
	100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal	
110b	Less Than or Equal	Compare and assert output if less than or equal	
111b	Reserved		

Customizable Event Creation 2-0

CEC2-0 - Customizable Event Creation 2-0															
Register Space:	MMIO: 0/2/0														
Project:	CHV, BSW														
Source:	PRM														
Default Value:	0x00000000														
Access:	R/W														
Size (in bits):	32														
Address:	02780h														
Valid Projects:	CHV, BSW														
<p>This register is used to define custom counter event 2, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.</p>															
DWord	Bit	Description													
0	31:21	Negate <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U11</td> </tr> </table> <p>The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Pass-through</td> <td>Input bit is passed through to comparator as is</td> </tr> <tr> <td>1b</td> <td>Negated</td> <td>Input bit is negated before passing to comparator</td> </tr> </tbody> </table>	Project:	CHV, BSW	Format:	U11	Value	Name	Description	0b	Pass-through	Input bit is passed through to comparator as is	1b	Negated	Input bit is negated before passing to comparator
		Project:	CHV, BSW												
		Format:	U11												
Value	Name	Description													
0b	Pass-through	Input bit is passed through to comparator as is													
1b	Negated	Input bit is negated before passing to comparator													
20:19		Source Select <table border="1"> <tr> <td>Format:</td> <td>U2</td> </tr> </table> <p>Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>01b</td> <td>Prev Event</td> <td>Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block</td> </tr> <tr> <td>11b</td> <td>Reserved</td> <td></td> </tr> </tbody> </table>	Format:	U2	Value	Name	Description	01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block	11b	Reserved			
		Format:	U2												
		Value	Name	Description											
01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block													
11b	Reserved														
18:3		Compare Value <table border="1"> <tr> <td>Format:</td> <td>U16</td> </tr> </table> <p>The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.</p>	Format:	U16											
		Format:	U16												

CEC2-0 - Customizable Event Creation 2-0

2:0	Compare Function		
	Format:	U3	
	This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).		
	Value	Name	
	Description		
	000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
	001b	Greater Than	Compare and assert output if greater than
	010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
	011b	Greater Than or Equal	Compare and assert output if greater than or equal
	100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal	
110b	Less Than or Equal	Compare and assert output if less than or equal	
111b	Reserved		

Customizable Event Creation 3-0

CEC3-0 - Customizable Event Creation 3-0															
Register Space:	MMIO: 0/2/0														
Project:	CHV, BSW														
Source:	PRM														
Default Value:	0x00000000														
Access:	R/W														
Size (in bits):	32														
Address:	02788h														
Valid Projects:	CHV, BSW														
<p>This register is used to define custom counter event 3, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.</p>															
DWord	Bit	Description													
0	31:21	Negate <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U11</td> </tr> </table> <p>The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Pass-through</td> <td>Input bit is passed through to comparator as is</td> </tr> <tr> <td>1b</td> <td>Negated</td> <td>Input bit is negated before passing to comparator</td> </tr> </tbody> </table>	Project:	CHV, BSW	Format:	U11	Value	Name	Description	0b	Pass-through	Input bit is passed through to comparator as is	1b	Negated	Input bit is negated before passing to comparator
		Project:	CHV, BSW												
		Format:	U11												
Value	Name	Description													
0b	Pass-through	Input bit is passed through to comparator as is													
1b	Negated	Input bit is negated before passing to comparator													
20:19		Source Select <table border="1"> <tr> <td>Format:</td> <td>U2</td> </tr> </table> <p>Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>01b</td> <td>Prev Event</td> <td>Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block</td> </tr> <tr> <td>11b</td> <td>Reserved</td> <td></td> </tr> </tbody> </table>	Format:	U2	Value	Name	Description	01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block	11b	Reserved			
		Format:	U2												
		Value	Name	Description											
01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block													
11b	Reserved														
18:3		Compare Value <table border="1"> <tr> <td>Format:</td> <td>U16</td> </tr> </table> <p>The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.</p>	Format:	U16											
		Format:	U16												

CEC3-0 - Customizable Event Creation 3-0

2:0	Compare Function		
	Format:	U3	
	This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).		
	Value	Name	
	Description		
	000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
	001b	Greater Than	Compare and assert output if greater than
	010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
	011b	Greater Than or Equal	Compare and assert output if greater than or equal
	100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal	
110b	Less Than or Equal	Compare and assert output if less than or equal	
111b	Reserved		

Customizable Event Creation 4-0

CEC4-0 - Customizable Event Creation 4-0											
Register Space:	MMIO: 0/2/0										
Project:	CHV, BSW										
Source:	PRM										
Default Value:	0x00000000										
Access:	R/W										
Size (in bits):	32										
Address:	02790h										
This register is used to define custom counter event 4, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.											
DWord	Bit	Description									
0	31:21	Negate									
		Project: CHV, BSW									
		Format: U11 The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.									
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Pass-through</td> <td>Input bit is passed through to comparator as is</td> </tr> <tr> <td>1b</td> <td>Negated</td> <td>Input bit is negated before passing to comparator</td> </tr> </tbody> </table>	Value	Name	Description	0b	Pass-through	Input bit is passed through to comparator as is	1b	Negated	Input bit is negated before passing to comparator
Value	Name	Description									
0b	Pass-through	Input bit is passed through to comparator as is									
1b	Negated	Input bit is negated before passing to comparator									
	20:19	Source Select									
		Format: U2 Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).									
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>01b</td> <td>Prev Event</td> <td>Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block</td> </tr> <tr> <td>11b</td> <td>Reserved</td> <td></td> </tr> </tbody> </table>	Value	Name	Description	01b	Prev Event	Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block	11b	Reserved	
Value	Name	Description									
01b	Prev Event	Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block									
11b	Reserved										
	18:3	Compare Value									
		Format: U16 The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.									

CEC4-0 - Customizable Event Creation 4-0

2:0	Compare Function		
	Format:	U3	
	This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).		
	Value	Name	
	Description		
	000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
	001b	Greater Than	Compare and assert output if greater than
	010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
	011b	Greater Than or Equal	Compare and assert output if greater than or equal
	100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal	
110b	Less Than or Equal	Compare and assert output if less than or equal	
111b	Reserved		

Customizable Event Creation 5-0

CEC5-0 - Customizable Event Creation 5-0					
Register Space:	MMIO: 0/2/0				
Project:	CHV, BSW				
Source:	PRM				
Default Value:	0x00000000				
Access:	R/W				
Size (in bits):	32				
Address:	02798h				
This register is used to define custom counter event 5, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.					
DWord	Bit	Description			
0	31:21	Negate			
		Project:	CHV, BSW		
		Format:	U11		
		The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.			
		Value	Name	Description	Project
		0b	Pass-through	Input bit is passed through to comparator as is	All
		1b	Negated	Input bit is negated before passing to comparator	All
	20:19	Source Select			
		Format:	U2		
		Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).			
Value		Name	Description	Project	
	01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block	All	
	11b	Reserved			
18:3	Compare Value				
	Format:	U16			
	The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.				

CEC5-0 - Customizable Event Creation 5-0

2:0	Compare Function		
	Format:	U3	
	This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).		
	Value	Name	
	Description		
	000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
	001b	Greater Than	Compare and assert output if greater than
	010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
	011b	Greater Than or Equal	Compare and assert output if greater than or equal
	100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal	
110b	Less Than or Equal	Compare and assert output if less than or equal	
111b	Reserved		

Customizable Event Creation 6-0

CEC6-0 - Customizable Event Creation 6-0					
Register Space:	MMIO: 0/2/0				
Project:	CHV, BSW				
Source:	PRM				
Default Value:	0x00000000				
Access:	R/W				
Size (in bits):	32				
Address:	027A0h				
This register is used to define custom counter event 6, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.					
DWord	Bit	Description			
0	31:21	Negate			
		Project:	CHV, BSW		
		Format:	U11		
		The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.			
		Value	Name	Description	Project
		0b	Pass-through	Input bit is passed through to comparator as is	All
		1b	Negated	Input bit is negated before passing to comparator	All
	20:19	Source Select			
		Format:	U2		
		Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).			
		Value	Name	Description	Project
	01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block	All	
	11b	Reserved			
18:3	Compare Value				
	Format:	U16			
	The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.				

CEC6-0 - Customizable Event Creation 6-0

2:0	Compare Function		
	Format:	U3	
	This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).		
	Value	Name	
	Description		
	000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
	001b	Greater Than	Compare and assert output if greater than
	010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
	011b	Greater Than or Equal	Compare and assert output if greater than or equal
	100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal	
110b	Less Than or Equal	Compare and assert output if less than or equal	
111b	Reserved		

Customizable Event Creation 7-0

CEC7-0 - Customizable Event Creation 7-0												
Register Space:	MMIO: 0/2/0											
Project:	CHV, BSW											
Source:	PRM											
Default Value:	0x00000000											
Access:	R/W											
Size (in bits):	32											
Address:	027A8h											
This register is used to define custom counter event 7, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.												
DWord	Bit	Description										
0	31:21	Negate										
		Project:	CHV, BSW									
		Format:	U11									
		The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.										
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Pass-through</td> <td>Input bit is passed through to comparator as is</td> </tr> <tr> <td>1b</td> <td>Negated</td> <td>Input bit is negated before passing to comparator</td> </tr> </tbody> </table>			Value	Name	Description	0b	Pass-through	Input bit is passed through to comparator as is	1b	Negated	Input bit is negated before passing to comparator
	Value	Name	Description									
	0b	Pass-through	Input bit is passed through to comparator as is									
	1b	Negated	Input bit is negated before passing to comparator									
	20:19	Source Select										
		Format:	U2									
Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).												
<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>01b</td> <td>Prev Event</td> <td>Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block</td> </tr> <tr> <td>11b</td> <td>Reserved</td> <td></td> </tr> </tbody> </table>			Value	Name	Description	01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block	11b	Reserved		
Value	Name	Description										
01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block										
11b	Reserved											
18:3	Compare Value											
	Format:	U16										
	The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.											

CEC7-0 - Customizable Event Creation 7-0

2:0	Compare Function		
	Format:	U3	
	This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).		
	Value	Name	
	Description		
	000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
	001b	Greater Than	Compare and assert output if greater than
	010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
	011b	Greater Than or Equal	Compare and assert output if greater than or equal
	100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal	
110b	Less Than or Equal	Compare and assert output if less than or equal	
111b	Reserved		

CVS TLB LRA 0

CVS_TLB_LRA_0 - CVS TLB LRA 0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x5F201F00 CHV, BSW	
Size (in bits):	32	
Address:	04A20h	
DWord	Bit	Description
0	31	Reserved
		Default Value: 0b
		Access: RO
	30:24	CVS LRA1 Max
		Default Value: 1011111b
		Project: CHV, BSW, :GT2:B
		Access: R/W
	Maximum value of programmable LRA1.	
23	Reserved	
	Default Value: 0b	
	Access: RO	
22:16	CVS LRA1 Min	
	Default Value: 0100000b	
	Access: R/W	
Minimum value of programmable LRA1.		
15	Reserved	
	Default Value: 0b	
	Access: RO	
14:8	CVS LRA0 Max	
	Default Value: 0011111b	
	Access: R/W	
Maximum value of programmable LRA0.		
7	Reserved	
	Default Value: 0b	
	Access: RO	

CVS_TLB_LRA_0 - CVS TLB LRA 0										
	6:0	<table border="1" style="width: 100%;"> <tr> <td colspan="2">CVS LRA0 Min</td> </tr> <tr> <td style="width: 70%;">Default Value:</td> <td>0000000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="2">Minimum value of programmable LRA0.</td> </tr> </table>	CVS LRA0 Min		Default Value:	0000000b	Access:	R/W	Minimum value of programmable LRA0.	
CVS LRA0 Min										
Default Value:	0000000b									
Access:	R/W									
Minimum value of programmable LRA0.										

CVS TLB LRA 1

CVS_TLB_LRA_1 - CVS TLB LRA 1			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW, :GT2:B		
Source:	PRM		
Default Value:	0x7F007F60		
Size (in bits):	32		
Address:	04A24h		
DWord	Bit	Description	
0	31	Reserved	
		Default Value:	0b
		Access:	RO
	30:24	CVS LRA3 Max	
		Default Value:	1111111b
		Access:	R/W
			For Future Use.
	23	Reserved	
		Default Value:	0b
		Access:	RO
22:16	CVS LRA3 Min		
	Default Value:	0000000b	
	Access:	R/W	
		For Future Use.	
15	Reserved		
	Default Value:	0b	
	Access:	RO	
14:8	CVS LRA2 Max		
	Default Value:	1111111b	
	Access:	R/W	
		Maximum value of programmable LRA2.	
7	Reserved		
	Default Value:	0b	
	Access:	RO	

CVS_TLB_LRA_1 - CVS TLB LRA 1													
	<table border="1" style="width: 100%;"> <tr> <td style="width: 15%; text-align: center; vertical-align: top;">6:0</td> <td colspan="2">CVS LRA2 Min</td> </tr> <tr> <td></td> <td style="width: 55%;">Default Value:</td> <td style="width: 30%;">1100000b</td> </tr> <tr> <td></td> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="3">Minimum value of programmable LRA2.</td> </tr> </table>	6:0	CVS LRA2 Min			Default Value:	1100000b		Access:	R/W	Minimum value of programmable LRA2.		
6:0	CVS LRA2 Min												
	Default Value:	1100000b											
	Access:	R/W											
Minimum value of programmable LRA2.													

CVS TLB LRA 2

CVS_TLB_LRA_2 - CVS TLB LRA 2			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW, :GT2:B		
Source:	PRM		
Default Value:	0x0000001A		
Size (in bits):	32		
Address:	04A28h		
DWord	Bit	Description	
0	31:8	Reserved	
		Default Value:	000000h
		Access:	RO
	7:6	RS LRA	
		Default Value:	00b
		Access:	R/W
			Which LRA should RS use
	5:4	CS LRA	
		Default Value:	01b
		Access:	R/W
			Which LRA should CS use.
	3:2	SOL LRA	
		Default Value:	10b
		Access:	R/W
			Which LRA should SOL use.
	1:0	VF LRA	
		Default Value:	10b
		Access:	R/W
			Which LRA should VF use.

Depth/Early Depth TLB Partitioning Register

ZSHR - Depth/Early Depth TLB Partitioning Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	RenderCS			
Default Value:	0x00000020			
Access:	R/W			
Size (in bits):	32			
Trusted Type:	1			
Address:	04050h			
<p>This register is used to determine the number of TLB entries from the total of 64 available to be used by the Depth partition of the TLB. The rest of the entries are used for the Early Depth/Stencil TLB.</p>				
DWord	Bit	Description		
0	31:6	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
5:0	<p>Number of TLB Entries Out of 64 used for Depth TLB</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%; text-align: center;">32</td> </tr> </table> <p>The rest are be used for Early Depth/Stencil TLB. Default value is 32.</p>	Default Value:	32	
Default Value:	32			

DID

DID - DID								
Register Space:	PCI: 0/2/0							
Project:	CHV, BSW							
Source:	PRM							
Default Value:	0x22B08086 CHV, BSW							
Size (in bits):	32							
Address:	00000h							
D2: PCI Device ID and Vendor ID Register								
DWord	Bit	Description						
0	31:24	DEVICEID_UB <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">22h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>DID_MSB: Identifier assigned to the dev2 PCI. Punit will update this bitfield before handing control to BIOS.</p>	Default Value:	22h	Access:	R/W		
		Default Value:	22h					
		Access:	R/W					
23:16	23:16	DEVICEID_LB <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">B0h</td> </tr> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>DID_LSB: Identifier assigned to the dev2 PCI. This bitfield is updated from metal straps. CHV, BSW allocated values : 0xB0 0xB1 0xB2 0xB3.</p>	Default Value:	B0h	Project:	CHV, BSW	Access:	RO
		Default Value:	B0h					
		Project:	CHV, BSW					
Access:	RO							
23:16	23:16	DEVICEID_LB <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">B0h</td> </tr> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>DID_LSB: Identifier assigned to the dev2 PCI. Bits[7:2] is updated from metal straps. Bits[1:0] will be based on market segment SKU (ie via. fusing) CHV, BSW allocated values : 0xB0 0xB1 0xB2 0xB3.</p>	Default Value:	B0h	Project:	CHV, BSW	Access:	RO
		Default Value:	B0h					
		Project:	CHV, BSW					
Access:	RO							

DID - DID						
	15:0	<p>VENDORID</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>8086h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>VID: PCI standard identification for Intel</p>	Default Value:	8086h	Access:	RO
Default Value:	8086h					
Access:	RO					

DS Invocation Counter

DS_INVOCATION_COUNT - DS Invocation Counter		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	02308h	
<p>This register stores the number of domain points shaded by the DS threads. Domain points which hit in the DS cache will not cause this register to increment. Note that the spawning of a DS thread which shades two domain points will cause this counter to increment by two. This register is part of the context save and restore.</p>		
DWord	Bit	Description
0	63:32	DS Invocation Count UDW Number of domain points shaded by the DS threads. Updated only when DS Function Enable and Statistics Enable are set in 3DSTATE_DS
	31:0	DS Invocation Count LDW Number of domain points shaded by the DS threads. Updated only when DS Function Enable and Statistics Enable are set in 3DSTATE_DS

DX9 Constants Not Consumed By RCS

DX9CONST_PRODUCE_COUNT - DX9 Constants Not Consumed By RCS		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	02484h	
<p>This register keeps track of the outstanding DX9 Constants produced by RS which are not yet consumed by Render Command Streamer. This register is part of the render context save and restore. This register should not be programmed by SW.</p>		
DWord	Bit	Description
0	31:0	<p>DX9 Constants Produce Count</p> <p>This register keeps track of the outstanding DX9 Constants produced by RS which are not yet consumed by Render Command Streamer. This register is part of the render context save and restore.</p>

DX9 Constants Prsed By RCS

DX9CONST_PARSE_COUNT - DX9 Constants Prsed By RCS		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	02494h	
<p>This register keeps track of the DX9 Constant commands parsed by RCS prior to encountering the Draw Call in an RS enabled Batch Buffer which has DX9 Pool Alloc Valid. DX9 parse count should be less then equal to the DX9 produce count for Command Streamer to make progress on a 3D_PRIMITIVE command. DX9 Parse count is subtracted from the DX9 Produce Count upon parsing 3D_PRIMITIVE command. This register is part of the render context save and restore. This register should not be programmed by SW.</p>		
DWord	Bit	Description
0	31:0	<p>DX9 Constants Produce Count</p> <p>This register keeps track of the DX9 Constant commands parsed by RCS prior to encountering the Draw Call in an RS enabled Batch Buffer which has DX9 Pool Alloc Valid. DX9 parse count should be less then equal to the DX9 produce count for Command Streamer to make progress on a 3D_PRIMITIVE command. DX9 Parse count is subtracted from the DX9 Produce Count upon parsing 3D_PRIMITIVE command.</p>

ECO Bits - Bus Reset Domain with lock bit

ECOBUS - ECO Bits - Bus Reset Domain with lock bit		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A180h-0A183h	
DWord	Bit	Description
0	31	ECO Bits - Bus Reset Domain - LOCK BIT Access: R/W Lock
	30	Reserved Access: RO
	29	Flush and block gfx pipes during cpd enter Access: R/W Lock 0 = GFX Pipes will not be blocked during CPD enter 1 = GFX Pipes will be blocked and flushed during CPD enter. They will be unblocked again during CPD exit. This bit must not be set to 1
	28	Block gfx from accessing memory during cpd enter Access: R/W Lock 0 = GFX will not be blocked from accessing memory during CPD enter 1 = GFX will be blocked from accessing memory (go=0) during CPD enter. They will be unblocked again during CPD exit (go=1).
	27:26	ECO Bits - Bus Reset Domain1 Access: R/W Lock Register bits that have no connection to design. Used to enable/disable changes to the design that were put in during the ECO process. pmcr_eco_busrst[26:25]
	25	CPD GAM GO Messaging Enable Access: R/W Lock 0 = No GO Messages to GAM during during CPD enter/exit flows (including slice shutdown) (default) 1 = GO Messages to GAM will occur during CPD enter/exit flows (including slice shutdown)

ECOBUS - ECO Bits - Bus Reset Domain with lock bit

24:0	ECO Bits - Bus Reset Domain0			
		Access:	R/W Lock	
Description				
<p>Register bits that have no connection to design. Used to enable/disable changes to the design that were put in during the ECO process. pmcr_eco_busrst[24:0] ----</p> <p>[21] = 1 VCS/CS/BCS Idleness, as well as CP/MBC/DT Idleness required for RC6 entry [21] = 0 VCS/CS/BCS Idleness required for RC6 entry ----</p> <p>[20] - Reserved [19] - Reserved [18] - Reserved 1 - Disable compensation 0 - Enable compensation of respective counters ----</p> <p>[17] - Reserved 1 -- Disable WIDI Context Save/Restore 0 -- Enable WIDI Context Save/Restore (Default) ----</p> <p>[16:15] -- Bits to indicate how many EU's, in each SubSlice, to bring up as part of Render Standby exit 00 -- Bring up 8 EU's (Default) 01 -- Bring up only 6 EU's 10 -- Bring up only 4 EU's 11 -- Bring up just 2 EU's ----</p> <p>[14:0] are spare bits for ECO process. ----</p>				

ECO Bits - Device Reset Domain

ECODEV - ECO Bits - Device Reset Domain				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A184h-0A187h			
DWord	Bit	Description		
0	31:0	<p>ECODEV</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Register bits that have no connection to design. Used to enable/disable changes to the design that were put in during the ECO process. pmcr_eco_bits[31:0]</p>	Access:	R/W
Access:	R/W			

ECO Message Register

ECO_MSG - ECO Message Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	16			
Address:	08040h			
<p>Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.</p>				
DWord	Bit	Description		
0	15	<p>Placeholder for ECO Bit 15</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.</p>	Access:	R/W
	Access:	R/W		
	14	<p>Placeholder for ECO Bit 14</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.</p>	Access:	R/W
	Access:	R/W		
	13	<p>Placeholder for ECO Bit 13</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.</p>	Access:	R/W
	Access:	R/W		
12	<p>Placeholder for ECO Bit 12</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.</p>	Access:	R/W	
Access:	R/W			
11	<p>Placeholder for ECO Bit 11</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.</p>	Access:	R/W	
Access:	R/W			
10	<p>Placeholder for ECO Bit 10</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.</p>	Access:	R/W	
Access:	R/W			

ECO_MSG - ECO Message Register			
9	<p>Placeholder for ECO Bit 9</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.</p>	Access:	R/W
Access:	R/W		
8	<p>Placeholder for ECO Bit 8</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.</p>	Access:	R/W
Access:	R/W		
7	<p>Placeholder for ECO Bit 7</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.</p>	Access:	R/W
Access:	R/W		
6	<p>Placeholder for ECO Bit 6</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.</p>	Access:	R/W
Access:	R/W		
5	<p>Placeholder for ECO Bit 5</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.</p>	Access:	R/W
Access:	R/W		
4	<p>Placeholder for ECO Bit 4</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.</p>	Access:	R/W
Access:	R/W		
3	<p>Placeholder for ECO Bit 3</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.</p>	Access:	R/W
Access:	R/W		
2	<p>Placeholder for ECO Bit 2</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.</p>	Access:	R/W
Access:	R/W		
1	<p>Placeholder for ECO Bit 1</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.</p>	Access:	R/W
Access:	R/W		
0	<p>Placeholder for ECO Bit 0</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.</p>	Access:	R/W
Access:	R/W		

ECO Reserved

ECOResrv - ECO Reserved				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	09898h			
ECO Reserved bits				
DWord	Bit	Description		
0	31:0	ECO Reserved Bits <table border="1"> <tr> <td>Access:</td> <td>R/WC</td> </tr> </table>	Access:	R/WC
Access:	R/WC			

ECREQ

ECREQ - ECREQ						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	1300A0h					
This register contains the energy counter request bit.						
DWord	Bit	Description				
0	31:1	SPARE <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Spare bits for Duty cycle control feature.</p>	Default Value:	00000000h	Access:	R/W
		Default Value:	00000000h			
Access:	R/W					
0	Energy Count Request <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>WO</td> </tr> </table> <p>WO access type of this register means that it will always return a zero when read. A write will generate a one CZ clock wide pulse to indicate that Punit requests for Gunit to push the energy counters. This pulse will only be created when both the data attempted to be written is one and when the byte enables allow the write.</p>	Default Value:	0b	Access:	WO	
Default Value:	0b					
Access:	WO					

Element Descriptor Register

ELEM_DESCRIPTOR - Element Descriptor Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000, 0x00000000	
Access:	RO	
Size (in bits):	64	
Address:	04500h	
Name:	BCS Element Descriptor Register	
ShortName:	BCS_ELEM_DESCRIPTOR	
Address:	04400h	
Name:	RCS Element Descriptor Register	
ShortName:	RCS_ELEM_DESCRIPTOR	
Address:	04440h	
Name:	VCS Element Descriptor Register	
ShortName:	VCS_ELEM_DESCRIPTOR	
Address:	044C0h	
Name:	VECS Element Descriptor Register	
ShortName:	VECS_ELEM_DESCRIPTOR	
Element Information: The register is populated by command streamer and consumed by GAM		
DWord	Bit	Description
0	63:32	Context ID Context identification number assigned to separate this context from others. Context IDs needs to be recycled in such a way that there could not be two active context with the same ID. This is a unique identification number by which a context is identified and referenced
	31:12	LRCA Command Streamer Only
	11:9	Function Number GFX device is considered to be on Bus0 with device number of 2. Function number is normally assigned as "0" however for gfx virtualization; there would be different function numbers which needs to be attached to context. Not used in Gen8.

ELEM_DESCRIPTOR - Element Descriptor Register

8	Privileged Context / GGTT vs PPGTT mode In Legacy Context: Defines the page tables to be used. This is how page walker come to know PPGTT vs GGTT selection for the entire context. In Advanced Context: Defines the privilege level for the context		
	Value	Name	Description
	0h	[Default]	Use Global GTT (In Legacy Context) User Mode Context (In Advanced Context)
	1h		Use Per-Process GTT (In Legacy Context) Supervisor Mode Context (In Advanced Context)
7:6	Fault Model		
	Value	Name	Description
	00h	[Default]	Fault and Hang. Same mode as gen7.5
	01h		Fault and Halt/Wait. Same mode as gen7.5
	10h		Reserved
	11h		Fault and Continue (reserved for gen8) - does not generate a page request to IOMMU.
5	Deeper IA coherency Support In Advanced Context: Defines the level of IA coherency		
	Value	Name	Description
	0h	[Default]	IA coherency is provided at LLC level for all streams of GPU (i.e. gen7.5 like mode)
	1h		IA coherency is provided at L3 level for EU data accesses of GPU
4	A and D Support / 32 and 64b Address Support In Legacy Context: Defines 32b vs 64b (48b canonical) addressing format In Advanced Context: Defines A/D bit support		
	Value	Name	Description
	0h	[Default]	32b addressing format (In Legacy Context) A/D bit management in page tables is NOT supported (In Advanced Context)
	1h		64b (48b canonical) addressing format (In Legacy Context) A/D bit management in page tables is supported (In Advanced Context)
3	Context Type: Legacy vs Advanced Defines the context type. Note that: Bits [8:4] differs in functions when legacy vs advanced context modes are selected.		
	Value	Name	Description
	0h	[Default]	Advanced Context: Defines the rest of the advanced capabilities (i.e. OS page table support, fault models...). Note that advanced context is not bounded to GPGPU.
	1h		Legacy Context: Defines the context as legacy mode which is similar to prior generations of gen8.

ELEM_DESCRIPTOR - Element Descriptor Register														
2	FR	Command Streamer Specific												
1	Scheduling Mode	<table border="1" style="width: 100%;"> <tr> <td colspan="2">Project:</td> <td></td> </tr> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> <tr> <td style="text-align: center;">0h</td> <td style="text-align: center;">[Default]</td> <td>Indicates execlist mode of scheduling.</td> </tr> <tr> <td style="text-align: center;">1h</td> <td></td> <td>Indicates Ring Buffer mode of scheduling.</td> </tr> </table>	Project:			Value	Name	Description	0h	[Default]	Indicates execlist mode of scheduling.	1h		Indicates Ring Buffer mode of scheduling.
Project:														
Value	Name	Description												
0h	[Default]	Indicates execlist mode of scheduling.												
1h		Indicates Ring Buffer mode of scheduling.												
0	Valid	Indicates that element descriptor is valid. If GAM is programmed with an invalid descriptor, it will continue but flag an error.												

Error_Identity_Reg

EIR - Error_Identity_Reg			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	020B0h-020B3h		
Name:	Error Identity Register		
ShortName:	EIR_RCSUNIT		
Address:	120B0h-120B3h		
Name:	Error Identity Register		
ShortName:	EIR_VCSUNIT0		
Address:	1A0B0h-1A0B3h		
Name:	Error Identity Register		
ShortName:	EIR_VECSUNIT		
Address:	1C0B0h-1C0B3h		
Name:	Error Identity Register		
ShortName:	EIR_VCSUNIT1		
Address:	220B0h-220B3h		
Name:	Error Identity Register		
ShortName:	EIR_BCSUNIT		
Address:	1820B0h		
<p>Error Identity. This register contains the persistent values of ESR error status bits that are unmasked via the EMR register.</p> <p>The logical OR of all (defined) bits in this register is reported in the Master Error bit of the Interrupt Status Register (ISR).</p> <p>In order to clear an error condition, software must first clear the error by writing a 1 to the appropriate bit(s) in this field.</p> <p>If required, software should then proceed to clear the Master Error bit of the IIR</p>			
DWord	Bit	Description	
0	31:7	RESERVED	
		Default Value:	0000000h
		Access:	RO
Reserved			
6		Gunit_TLB_DataE	
		Default Value:	0b

EIR - Error_Identity_Reg		
	Access:	R/W One Clear
Set if Gunit TLB has a data valid error		
5	Gunit_TLB_PTE	
	Default Value:	0b
	Access:	R/W One Clear
Set if Gunit TLB has a PTE translation error.		
4	PAGE_TABLE_ERROR	
	Default Value:	0b
	Access:	R/W One Clear
<p>PTE: This bit is set when a Graphics Memory Mapping Error is detected and it's not EMR masked. The cause of the error is indicated (to some extent) in the PGTBL_ER register. This error condition cannot be cleared except by reset (i.e., it is a fatalerror)</p> <p>$mir_EIR[4] = (((dsp_gvd_invldgtpte_int_dczfwoh \text{ and } \sim mir_EMR[4]) mir_EIR[4]) \text{ and } \sim(sys_wdata[4] \text{ and } mir_write \text{ and } mirb0_decode \text{ and } \sim sys_data_mask[0]));$</p>		
3:1	RESERVED	
	Default Value:	0h
	Access:	RO
Reserved		
0	CLAIM_ERROR	
	Default Value:	0b
	Access:	R/W One Clear
<p>If EMR[0]=1, this bit is set when an address within Gunit address space is accessed, but no memory mapped register exists in this address. This error condition can be cleared by writing 1b to this bit.</p> <p>$Mir_EIR[0] = (((noRMclaim_err \text{ and } \sim mir_EMR[0]) mir_EIR[0]) \text{ and } \sim(sys_wdata[0] \text{ and } mir_write \text{ and } mirb0_decode \text{ and } \sim sys_data_mask[0]));$</p>		

Error_Mask_Reg

EMR - Error_Mask_Reg			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000071		
Size (in bits):	32		
Address:	020B4h-020B7h		
Name:	Error Mask Register		
ShortName:	EMR_RCSUNIT		
Address:	120B4h-120B7h		
Name:	Error Mask Register		
ShortName:	EMR_VCSUNIT0		
Address:	1A0B4h-1A0B7h		
Name:	Error Mask Register		
ShortName:	EMR_VECSUNIT		
Address:	1C0B4h-1C0B7h		
Name:	Error Mask Register		
ShortName:	EMR_VCSUNIT1		
Address:	220B4h-220B7h		
Name:	Error Mask Register		
ShortName:	EMR_BCSUNIT		
Address:	1820B4h		
Error Mask. This register contains a bit mask that selects which error condition bits (from the ESR) are reported in the EIR			
DWord	Bit	Description	
0	31:7	RESERVED	
		Default Value:	0000000h
		Access:	RO
Reserved			
6		Gunit_TLB_DataE	
		Default Value:	1b
		Access:	R/W
1 = Masked. This error will neither be reported in the EIR, nor set the master error condition in the IIR.			
0 = Unmasked. This interrupt will be reported in the EIR and will set the master error condition in the IIR.			

EMR - Error_Mask_Reg			
5	Gunit_TLB_PTE		
	Default Value:	1b	
	Access:	R/W	
	<p>1 = Masked. This error will neither be reported in the EIR, nor set the master error condition in the IIR.</p> <p>0 = Unmasked. This interrupt will be reported in the EIR and will set the master error condition in the IIR.</p>		
	4	PAGE_TABLE_ERROR	
		Default Value:	1b
		Access:	R/W
		<p>1 = Masked. This error will neither be reported in the EIR, nor set the master error condition in the IIR.</p> <p>0 = Unmasked. This interrupt will be reported in the EIR and will set the master error condition in the IIR.</p>	
	3:1	RESERVED	
		Default Value:	0h
		Access:	RO
		Reserved	
0	CLAIM_ERROR		
	Default Value:	1b	
	Access:	R/W	
	<p>1 = Masked. This error will neither be reported in the EIR, nor set the master error condition in the IIR.</p> <p>0 = Unmasked. This interrupt will be reported in the EIR and will set the master error condition in the IIR.</p>		

Error_Status_Reg

ESR - Error_Status_Reg				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	020B8h-020BBh			
Name:	Error Status Register			
ShortName:	ESR_RCSUNIT			
Address:	120B8h-120BBh			
Name:	Error Status Register			
ShortName:	ESR_VCSUNIT0			
Address:	1A0B8h-1A0BBh			
Name:	Error Status Register			
ShortName:	ESR_VECSUNIT			
Address:	1C0B8h-1C0BBh			
Name:	Error Status Register			
ShortName:	ESR_VCSUNIT1			
Address:	220B8h-220BBh			
Name:	Error Status Register			
ShortName:	ESR_BCSUNIT			
Address:	1820B8h			
Error Status. This register contains the non-persistent values of all hardware-detected error condition bits.				
DWord	Bit	Description		
0	31:7	RESERVED		
		<table border="1"> <tr> <td>Default Value:</td> <td>0000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Reserved	Default Value:	0000000h
Default Value:	0000000h			
Access:	RO			
6		Gunit_TLB_DataE		
		<table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> 1 = This error condition currently exists. 0 = This error condition currently does not exist	Default Value:	0b
Default Value:	0b			
Access:	RO			

ESR - Error_Status_Reg		
5	Gunit_TLB_PTE	
	Default Value: 0b	
	Access: RO	
	1 = This error condition currently exists. 0 = This error condition currently does not exist	
	4	PAGE_TABLE_ERROR
		Default Value: 0b
		Access: RO
		1 = This error condition currently exists. 0 = This error condition currently does not exist(Was reported based on 0x18_2024h "OR").
	3:1	RESERVED
		Default Value: 0h
		Access: RO
	Reserved	
0	CLAIM_ERROR	
	Default Value: 0b	
	Access: RO	
	No RMBus claim occurred. Logging the error. 1 = This error condition currently exists. 0 = This error condition currently does not exist. Internal Gunit 'noRMclaim_err' wire from RMBus master.	

Error Identity Register

EIR - Error Identity Register							
Register Space:	MMIO: 0/2/0						
Project:	CHV, BSW						
Source:	RenderCS						
Default Value:	0x00000000						
Access:	R/W, RO						
Size (in bits):	32						
Address:	020B0h						
<p>The EIR register contains the persistent values of Hardware-Detected Error Condition bits. Any bit set in this register will cause the Master Error bit in the ISR to be set. The EIR register is also used by software to clear detected errors (by writing a 1 to the appropriate bit(s)), except for the unrecoverable bits described.)</p>							
Restriction							
<p>Restriction EIR register contents are not power or render context save/restored. EIR register contents of an engine will get lost when the corresponding graphics engine (Render, Video, Video Enhancement, Blitter) is power down.</p>							
DWord	Bit	Description					
0	31:16	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ			
	Format:	MBZ					
15:0	<p>Error Identity Bits</p> <table border="1"> <tr> <td>Format:</td> <td>Array of Error condition bits See the table titled Hardware-Detected Error Bits.</td> </tr> </table> <p>This register contains the persistent values of ESR error status bits that are unmasked via the EMR register. (See Table Table 3-3. Hardware-Detected Error Bits). The logical OR of all (defined) bits in this register is reported in the Master Error bit of the Interrupt Status Register. In order to clear an error condition, software must first clear the error by writing a 1 to the appropriate bit(s) in this field. If required, software should then proceed to clear the Master Error bit of the IIR. Reserved bits are RO.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>1h</td> <td>Error occurred</td> </tr> </tbody> </table>	Format:	Array of Error condition bits See the table titled Hardware-Detected Error Bits.	Value	Name	1h	Error occurred
Format:	Array of Error condition bits See the table titled Hardware-Detected Error Bits.						
Value	Name						
1h	Error occurred						
Programming Notes							
<p>Writing a 1 to a set bit will cause that error condition to be cleared. However, neither the Page Table Error bit (Bit 4) nor the Instruction Error bit (Bit 0) can be cleared except by reset (i.e., it is a fatal error).</p>							

Error Mask Register

EMR - Error Mask Register														
Register Space:	MMIO: 0/2/0													
Project:	CHV, BSW													
Source:	RenderCS													
Default Value:	0xFFFFFFFF													
Access:	R/W, RO													
Size (in bits):	32													
Address:	020B4h													
<p>The EMR register is used by software to control which Error Status Register bits are masked or unmasked. Unmasked bits will be reported in the EIR, thus setting the Master Error ISR bit and possibly triggering a CPU interrupt, and will persist in the EIR until cleared by software. Masked bits will not be reported in the EIR and therefore cannot generate Master Error conditions or CPU interrupts. Reserved bits are RO.</p>														
DWord	Bit	Description												
0	31:8	Reserved												
		Default Value: FFFFFFh												
		Format: Must Be One												
		Programming Notes												
		These bits are not implemented in HW and must be set to '1'												
7:0	7:0	Error Mask Bits												
		Format: Array of error condition mask bits See the table titled Hardware-Detected Error Bits.												
		This register contains a bit mask that selects which error condition bits (from the ESR) are reported in the EIR.												
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>FFh</td> <td>[Default]</td> <td></td> </tr> <tr> <td>0h</td> <td>Not Masked</td> <td>Will be reported in the EIR</td> </tr> <tr> <td>1h</td> <td>Masked</td> <td>Will not be reported in the EIR</td> </tr> </tbody> </table>	Value	Name	Description	FFh	[Default]		0h	Not Masked	Will be reported in the EIR	1h	Masked	Will not be reported in the EIR
		Value	Name	Description										
FFh	[Default]													
0h	Not Masked	Will be reported in the EIR												
1h	Masked	Will not be reported in the EIR												

Error Reporting Register

ERR - Error Reporting Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B42Ch	
DWord	Bit	Description
0	31:5	Reserved
		Access: RO Reserved.
	4	First Content Buffer Ready 0
		Access: R/W
		First Content Buffer Ready 0 (FRSNTBFR0). First Content Buffer Ready: This bit gets set by the HW when the buffer is completely filled up and cleared by the driver when the contents of this buffer are copied out of memory. Is set by lpfc_lpconf_buffer0_ready (pulse). lpconf_lpfc_buffer0_ready (static signal to lpfc).
3	Second Buffer ready slice 0	
	Access: R/W	
2	Write Expire Error Slice 0	
	Access: R/W	
1	Buffer full Error Slice 0	
	Access: R/W	
Buffer full Error Slice 0 (BFFLERR0). Set by lpfc_lpconf_error_buffer_full. When all buffers are full lpfc sets this bit or if only 1 buffer is enabled then lpfc sets this bit when the buffer is full.		

ERR - Error Reporting Register						
	0	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%; text-align: center;">RO</td> </tr> <tr> <td colspan="2">Reserved.</td> </tr> </table>	Access:	RO	Reserved.	
Access:	RO					
Reserved.						

Error Status Register

ESR - Error Status Register					
Register Space:	MMIO: 0/2/0				
Project:	CHV, BSW				
Source:	RenderCS				
Default Value:	0x00000000				
Access:	RO				
Size (in bits):	32				
Address:	020B8h				
<p>The ESR register contains the current values of all Hardware-Detected Error condition bits (these are all by definition persistent). The EMR register selects which of these error conditions are reported in the persistent EIR (i.e., set bits must be cleared by software) and thereby causing a Master Error interrupt condition to be reported in the ISR.</p>					
DWord	Bit	Description			
0	31:16	Reserved Format: MBZ			
	15:0	Error Status Bits Format: Array of error condition bits See the table titled Hardware-Detected Error Bits. This register contains the non-persistent values of all hardware-detected error condition bits. <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th style="width: 20%;">Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>1h</td> <td>Error Condition Detected</td> </tr> </tbody> </table>	Value	Name	1h
Value	Name				
1h	Error Condition Detected				

EU Mask Programming

TD_PM_MODE_EUCOUNT - EU Mask Programming		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	WO	
Size (in bits):	32	
Address:	0E4F8h	
Name:	EU Mask Programming Slice 0	
ShortName:	TD_PM_MODE_EUCOUNT_S0	
Valid Projects:	CHV, BSW	
Address:	0E5F8h	
Name:	EU Mask Programming Slice 1	
ShortName:	TD_PM_MODE_EUCOUNT_S1	
Valid Projects:	CHV, BSW	
Address:	0E6F8h	
Name:	EU Mask Programming Slice 2	
ShortName:	TD_PM_MODE_EUCOUNT_S2	
Valid Projects:	CHV, BSW	
DWord	Bit	Description
0	31:24	Reserved
		Project: CHV, BSW
		Format: MBZ
	23	SubSlice 2 EU 7 Enable
	Format: Enable	
	22	SubSlice 2 EU 6 Enable
	Format: Enable	
	21	SubSlice 2 EU 5 Enable
Format: Enable		
20	SubSlice 2 EU 4 Enable	
Format: Enable		
19	SubSlice 2 EU 3 Enable	
Format: Enable		
18	SubSlice 2 EU 2 Enable	

TD_PM_MODE_EUCOUNT - EU Mask Programming		
		Format: Enable
17	SubSlice 2 EU 1 Enable	Format: Enable
16	SubSlice 2 EU 0 Enable	Format: Enable
15	SubSlice 1 EU 7 Enable	Format: Enable
14	SubSlice 1 EU 6 Enable	Format: Enable
13	SubSlice 1 EU 5 Enable	Format: Enable
12	SubSlice 1 EU 4 Enable	Format: Enable
11	SubSlice 1 EU 3 Enable	Format: Enable
10	SubSlice 1 EU 2 Enable	Format: Enable
9	SubSlice 1 EU 1 Enable	Format: Enable
8	SubSlice 1 EU 0 Enable	Format: Enable
7	SubSlice 0 EU 7 Enable	Format: Enable
6	SubSlice 0 EU 6 Enable	Format: Enable
5	SubSlice 0 EU 5 Enable	Format: Enable
4	SubSlice 0 EU 4 Enable	Format: Enable
3	SubSlice 0 EU 3 Enable	Format: Enable
2	SubSlice 0 EU 2 Enable	Format: Enable
1	SubSlice 0 EU 1 Enable	Format: Enable

TD_PM_MODE_EUCOUNT - EU Mask Programming			
	0	SubSlice 0 EU 0 Enable	
		Format:	Enable

EU Metrics for Event0 High

EUMETRICSEVENT0H - EU Metrics for Event0 High						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	138134h					
Upper 32 bits of the EU Metrics Event0						
DWord	Bit	Description				
0	31:0	EUMetrics, Event0 High <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Contains Upper 32 bits of EU Metrics, Event0	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

EU Metrics for Event0 Low

EUMETRICSEVENT0L - EU Metrics for Event0 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	138130h	
Lower 14 bits of the EU Metrics Event0		
DWord	Bit	Description
0	31:18	EUMetrics, Event0 Low
		Default Value: 0000h
		Access: RO
	Contains lower 14 bits of EU Metrics, Event0	
17:0	Reserved	
	Default Value: 00000h	
	Access: RO	
Reserved		

EU Metrics for Event1 High

EUMETRICSEVENT1H - EU Metrics for Event1 High						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	13813Ch					
Upper 32 bits of the EU Metrics Event1						
DWord	Bit	Description				
0	31:0	EUMetrics, Event1 High <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Contains Upper 32 bits of EU Metrics, Event1	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

EU Metrics for Event1 Low

EUMETRICSEVENT1L - EU Metrics for Event1 Low			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	138138h		
Lower 14 bits of the EU Metrics Event1			
DWord	Bit	Description	
0	31:18	EUMetrics, Event1 Low	
		Default Value:	0000h
		Access:	RO
	Contains lower 14 bits of EU Metrics, Event1		
17:0	Reserved	Reserved	
		Default Value:	00000h
		Access:	RO
Reserved			

EU Metrics for Event2 High

EUMETRICSEVENT2H - EU Metrics for Event2 High						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	138144h					
Upper 32 bits of the EU Metrics Event2						
DWord	Bit	Description				
0	31:0	EUMetrics, Event2 High <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Contains Upper 32 bits of EU Metrics, Event2	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

EU Metrics for Event2 Low

EUMETRICSEVENT2L - EU Metrics for Event2 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	138140h	
Lower 14 bits of the EU Metrics Event2		
DWord	Bit	Description
0	31:18	EUMetrics, Event2 Low
		Default Value: 0000h
		Access: RO
	Contains lower 14 bits of EU Metrics, Event2	
17:0	Reserved	
	Default Value: 00000h	
	Access: RO	
Reserved		

EU Metrics for Event3 High

EUMETRICSEVENT3H - EU Metrics for Event3 High						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	13814Ch					
Upper 32 bits of the EU Metrics Event3						
DWord	Bit	Description				
0	31:0	EUMetrics, Event3 High <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Contains Upper 32 bits of EU Metrics, Event3	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

EU Metrics for Event3 Low

EUMETRICSEVENT3L - EU Metrics for Event3 Low			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	138148h		
Lower 14 bits of the EU Metrics Event3			
DWord	Bit	Description	
0	31:18	EUMetrics, Event3 Low	
		Default Value:	0000h
		Access:	RO
	Contains lower 14 bits of EU Metrics, Event3		
17:0	Reserved	Default Value:	00000h
		Access:	RO
		Reserved	

EU Metrics for Event4 High

EUMETRICSEVENT4H - EU Metrics for Event4 High						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	138154h					
Upper 32 bits of the EU Metrics Event4						
DWord	Bit	Description				
0	31:0	EUMetrics, Event4 High <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Contains Upper 32 bits of EU Metrics, Event4	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

EU Metrics for Event4 Low

EUMETRICSEVENT4L - EU Metrics for Event4 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	138150h	
Lower 14 bits of the EU Metrics Event4		
DWord	Bit	Description
0	31:18	EUMetrics, Event4 Low
		Default Value: 0000h
		Access: RO
	Contains lower 14 bits of EU Metrics, Event4	
17:0	Reserved	
	Default Value: 00000h	
	Access: RO	
Reserved		

EU Metrics for Event5 High

EUMETRICSEVENT5H - EU Metrics for Event5 High						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	13815Ch					
Upper 32 bits of the EU Metrics Event5						
DWord	Bit	Description				
0	31:0	EUMetrics, Event5 High <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Contains Upper 32 bits of EU Metrics, Event5	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

EU Metrics for Event5 Low

EUMETRICSEVENT5L - EU Metrics for Event5 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	138158h	
Lower 14 bits of the EU Metrics Event5		
DWord	Bit	Description
0	31:18	EUMetrics, Event5 Low
		Default Value: 0000h
		Access: RO
		Contains lower 14 bits of EU Metrics, Event5
17:0	17:0	Reserved
		Default Value: 00000h
		Access: RO
		Reserved

EU Metrics for Event6 High

EUMETRICSEVENT6H - EU Metrics for Event6 High						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	138164h					
Upper 32 bits of the EU Metrics Event6						
DWord	Bit	Description				
0	31:0	EUMetrics, Event6 High <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Contains Upper 32 bits of EU Metrics, Event6	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

EU Metrics for Event6 Low

EUMETRICSEVENT6L - EU Metrics for Event6 Low			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	138160h		
Lower 14 bits of the EU Metrics Event6			
DWord	Bit	Description	
0	31:18	EUMetrics, Event6 Low	
		Default Value:	0000h
		Access:	RO
	Contains lower 14 bits of EU Metrics, Event6		
17:0	Reserved		
	Default Value:	00000h	
	Access:	RO	
Reserved			

EU Metrics for Event7 High

EUMETRICSEVENT7H - EU Metrics for Event7 High						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	13816Ch					
Upper 32 bits of the EU Metrics Event7						
DWord	Bit	Description				
0	31:0	EUMetrics, Event7 High <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Contains Upper 32 bits of EU Metrics, Event7	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

EU Metrics for Event7 Low

EUMETRICSEVENT7L - EU Metrics for Event7 Low			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	138168h		
Lower 14 bits of the EU Metrics Event7			
DWord	Bit	Description	
0	31:18	EUMetrics, Event7 Low	
		Default Value:	0000h
		Access:	RO
	Contains lower 14 bits of EU Metrics, Event7		
17:0	Reserved		
	Default Value:	00000h	
	Access:	RO	
Reserved			

EU Metrics for Event8 High

EUMETRICSEVENT8H - EU Metrics for Event8 High						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	138174h					
Upper 32 bits of the EU Metrics Event8						
DWord	Bit	Description				
0	31:0	EUMetrics, Event8 High <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Contains Upper 32 bits of EU Metrics, Event8	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

EU Metrics for Event8 Low

EUMETRICSEVENT8L - EU Metrics for Event8 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	138170h	
Lower 14 bits of the EU Metrics Event8		
DWord	Bit	Description
0	31:18	EUMetrics, Event8 Low
		Default Value: 0000h
		Access: RO
	Contains lower 14 bits of EU Metrics, Event8	
17:0	Reserved	
	Default Value: 00000h	
	Access: RO	
Reserved		

EU Metrics for Event9 High

EUMETRICSEVENT9H - EU Metrics for Event9 High						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	13817Ch					
Upper 32 bits of the EU Metrics Event9						
DWord	Bit	Description				
0	31:0	EUMetrics, Event9 High <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Contains Upper 32 bits of EU Metrics, Event9	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

EU Metrics for Event9 Low

EUMETRICSEVENT9L - EU Metrics for Event9 Low			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	138178h		
Lower 14 bits of the EU Metrics Event9			
DWord	Bit	Description	
0	31:18	EUMetrics, Event9 Low	
		Default Value:	0000h
		Access:	RO
	Contains lower 14 bits of EU Metrics, Event9		
17:0	Reserved	Default Value:	00000h
		Access:	RO
		Reserved	

EU Metrics for Event10 High

EUMETRICSEVENT10H - EU Metrics for Event10 High						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	138184h					
Upper 32 bits of the EU Metrics Event10						
DWord	Bit	Description				
0	31:0	EUMetrics, Event10 High <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Contains Upper 32 bits of EU Metrics, Event10	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

EU Metrics for Event10 Low

EUMETRICSEVENT10L - EU Metrics for Event10 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	138180h	
Lower 14 bits of the EU Metrics Event10		
DWord	Bit	Description
0	31:18	EUMetrics, Event10 Low
		Default Value: 0000h
	Access: RO	
	Contains lower 14 bits of EU Metrics, Event10	
17:0	Reserved	
	Default Value: 00000h	
	Access: RO	
		Reserved

EU Metrics for Event11 High

EUMETRICSEVENT11H - EU Metrics for Event11 High						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	13818Ch					
Upper 32 bits of the EU Metrics Event11						
DWord	Bit	Description				
0	31:0	EUMetrics, Event11 High <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Contains Upper 32 bits of EU Metrics, Event11	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

EU Metrics for Event11 Low

EUMETRICSEVENT11L - EU Metrics for Event11 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	138188h	
Lower 14 bits of the EU Metrics Event11		
DWord	Bit	Description
0	31:18	EUMetrics, Event11 Low
		Default Value: 0000h
		Access: RO
	Contains lower 14 bits of EU Metrics, Event11	
	17:0	Reserved
		Default Value: 00000h
		Access: RO
	Reserved	

EU Metrics for Event12 High

EUMETRICSEVENT12H - EU Metrics for Event12 High						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	138194h					
Upper 32 bits of the EU Metrics Event12						
DWord	Bit	Description				
0	31:0	EUMetrics, Event12 High <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Contains Upper 32 bits of EU Metrics, Event12	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

EU Metrics for Event12 Low

EUMETRICSEVENT12L - EU Metrics for Event12 Low						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	138190h					
Lower 14 bits of the EU Metrics Event12						
DWord	Bit	Description				
0	31:18	EUMetrics, Event12 Low <table border="1"> <tr> <td>Default Value:</td> <td>0000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Contains lower 14 bits of EU Metrics, Event12	Default Value:	0000h	Access:	RO
	Default Value:	0000h				
Access:	RO					
17:0	Reserved <table border="1"> <tr> <td>Default Value:</td> <td>00000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Reserved	Default Value:	00000h	Access:	RO	
Default Value:	00000h					
Access:	RO					

Event selection and base counters

LPFCREG2 - Event selection and base counters				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B00Ch			
DWord	Bit	Description		
0	31:24	<p>Counter 7 client</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Incf_lpf_c_cnt7_client[7:0].Client Encoding (hex):</p> <ul style="list-style-type: none"> GAFS Rd 00 GAFS Wr 01 HDC0 Data Rd 02 HDC0 Const Rd 03 HDC0 URB Rd 04 HDC0 Data Wr 05 HDC0 URB Wr 06 HDC1 Data Rd 07 HDC1 Const Rd 08 HDC1 URB Rd 09 HDC1 Data Wr 0A HDC1 URB Wr 0B TDL0 Rd 0C TDL1 Rd 0D Tex0 Rd 0E Tex1 Rd 0F Tex2 Rd (reserved) 10 Tex3 Rd (reserved) 11 SBE Rd 12 IC0 Rd 13 IC1 Rd 14 SARB Rd 15 Aggregated Tex 16 SLM0 Rd 17 SLM1 Rd 18 SLM0 Wr 19 SLM1 Wr 1A SLM0 Atomics 1B SLM1 Atomics 1C Reserved 1D Reserved 1E 	Access:	R/W
Access:	R/W			

LPFCREG2 - Event selection and base counters

	Reserved 1F
	FF Stalls 20
	HDC Stalls 21
	TDL Stalls 22
	Texture Stalls 23
	IC Stalls 24
	SBE Stalls 25
	SLM Stalls 26
	Bank0 Total Hits 40
	Bank0 Total Cycles 41
	Bank0 Total Rds 42
	Bank0 Total Wrs 43
	Bank0 FF Rds 44
	Bank0 FF Wrs 45
	Bank0 DC Rds 46
	Bank0 DC Wrs 47
	Bank0 DC Hits 48
	rsvd 49
	Bank0 Tex Rds 4A
	Bank0 Tex Hits 4B
	Bank0 IC Rds 4C
	Bank0 IC Hits 4D
	Reserved 4E
	Reserved 4F
	Bank1 Events 50-5F (except 59-reserved)
	Bank2 Events 60-6F(except 69-reserved)
	Bank3 Events 70-7F(except 79-reserved)
	MSC Rd 80
	MSC Wr 81
	STC Rd 82
	STC Wr 83
	Hiz Rd 84
	Hiz Wr 85
	RCZ Rd 86
	RCZ Wr 87
	RCC Rd 88
	RCC Wr 89
	LTCD0 Err Corr EE
	LTCD1 Err Corr EF
	LTCD2 Err Corr F0
	LTCD3 Err Corr F1
	LTCD0 Err UnCorr F2
	LTCD1 Err UnCorr F3
	LTCD2 Err UnCorr F4
	LTCD3 Err UnCorr F5

LPFCREG2 - Event selection and base counters		
	Counter#7 Client Selection: This field controls which client's request stream is observed in counter#7.	
23:16	Counter 6 client	
	<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>Incf_lpfc_cnt6_client[7:0].Counter#6 Client Selection: This field controls which client's request stream is observed in counter#6.</p>	Access:
Access:	R/W	
15:8	Counter 5 client	
	<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>Incf_lpfc_cnt5_client[7:0].Counter#5 Client Selection: This field controls which client's request stream is observed in counter#5.</p>	Access:
Access:	R/W	
7:0	Counter 4 client	
	<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>Incf_lpfc_cnt4_client[7:0].Counter#4 Client Selection: This field controls which client's request stream is observed in counter#4.</p>	Access:
Access:	R/W	

Event Selection and Base Counters1

LPFCREG1 - Event Selection and Base Counters1				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B010h			
DWord	Bit	Description		
0	31:24	<p>Counter 3 client</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Incf_lpf_cnt3_client[7:0].Counter#3 Client Selection: This field controls which client's request stream is observed in counter#3.</p>	Access:	R/W
	Access:	R/W		
	23:16	<p>Counter 2 client</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Incf_lpf_cnt2_client[7:0].Counter#2 Client Selection: This field controls which client's request stream is observed in counter#2.</p>	Access:	R/W
	Access:	R/W		
15:8	<p>Counter 1 Client</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Incf_lpf_cnt1_client[7:0].Counter#1 Client Selection: This field controls which client's request stream is observed in counter#1.</p>	Access:	R/W	
Access:	R/W			
7:0	<p>Counter0 Client</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Incf_lpf_cnt0_client[7:0].Counter#0 Client Selection: This field controls which client's request stream is observed in counter#0.</p>	Access:	R/W	
Access:	R/W			

Execlist Status

EXECLIST_STATUS - Execlist Status		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000001, 0x00000000	
Access:	RO	
Size (in bits):	64	
Address:	02234h-0223Bh	
Name:	RCS Execlist Status	
ShortName:	EXECLIST_STATUS_RCSUNIT	
Address:	12234h-1223Bh	
Name:	RCS Execlist Status	
ShortName:	EXECLIST_STATUS_VCSUNIT0	
Address:	1A234h-1A23Bh	
Name:	RCS Execlist Status	
ShortName:	EXECLIST_STATUS_VECSUNIT	
Address:	1C234h-1C23Bh	
Name:	RCS Execlist Status	
ShortName:	EXECLIST_STATUS_VCSUNIT1	
Address:	22234h-2223Bh	
Name:	RCS Execlist Status	
ShortName:	EXECLIST_STATUS_BCSUNIT	
This register contains the pointers and full indicator for the Execlist Queue and the context ID of the currently running context. DefaultValue = UUUU UUU1h (4:0 default to 00001b, others UNDEFINED).		
DWord	Bit	Description
0	63:32	Current Context ID Format: U32 Contains the context ID of the currently running context.
	31:30	Reserved Project: CHV, BSW Format: MBZ
	29:27	Reserved Format: MBZ

EXECLIST_STATUS - Execlist Status											
26:19	Reserved										
	<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ						
Project:	CHV, BSW										
Format:	MBZ										
18	Reserved										
17	Reserved										
16	Arbitration Enable										
	<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>This field reflects the Arbitration Flag set by the MI_ARB_ON_OFF command in Command Streamer.</p>	Project:	CHV, BSW	Format:	U1						
Project:	CHV, BSW										
Format:	U1										
15:14	Current Active Element Status										
	<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U2</td> </tr> </table> <p>Points at the element being executed in current Execlist (if there is one).</p>	Project:	CHV, BSW	Format:	U2						
	Project:	CHV, BSW									
	Format:	U2									
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>No Active Element being executed</td> </tr> <tr> <td>01b</td> <td>Element0 of current execlist being executed</td> </tr> <tr> <td>10b</td> <td>Element1 of current execlist being executed</td> </tr> <tr> <td>11b</td> <td>Reserved</td> </tr> </tbody> </table>	Value	Name	00b	No Active Element being executed	01b	Element0 of current execlist being executed	10b	Element1 of current execlist being executed	11b	Reserved
	Value	Name									
00b	No Active Element being executed										
01b	Element0 of current execlist being executed										
10b	Element1 of current execlist being executed										
11b	Reserved										
13:5	Last Context Switch Reason										
	<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>Format:</td> <td>U9</td> </tr> </table> <p>This field contains the switch reason for the last context to switch away, as captured in the Context Status Dword, bits 8:0.</p>	Project:	CHV, BSW	Access:	R/W	Format:	U9				
	Project:	CHV, BSW									
	Access:	R/W									
Format:	U9										
Programming Notes											
This field should not written by SW.											
4	Execlist 0 Valid										
	<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Flag</td> </tr> </table> <p>This bit is set when the first DW for this Execlist port 0 is written through the submission port, and will not be cleared till the CSB is updated and the command stream is switching to the next execution list. If no execution list is pending, the transition of this bit from one to zero guarentees there will be no preemption on the next submission.</p>	Project:	CHV, BSW	Format:	Flag						
	Project:	CHV, BSW									
	Format:	Flag									
<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Invalid [Default]</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Valid</td> </tr> </tbody> </table>	Value	Name	0	Invalid [Default]	1	Valid					
Value	Name										
0	Invalid [Default]										
1	Valid										
3	Execlist 1 Valid										

EXECLIST_STATUS - Execlist Status			
	Project:		CHV, BSW
	Format:		Flag
	<p>This bit is set when the first DW for this Execlist port 1 is written through the submission port, and will not be cleared till the CSB is updated and the command stream is switching to the next execution list. If no execution list is pending, the transition of this bit from one to zero guarantees there will be no preemption on the next submission.</p>		
	Value	Name	
	0	Invalid [Default]	
	1	Valid	
	2	Execlist Queue Full	
	Project:		CHV, BSW
	<p>When [Execlist Write Pointer] and [Current Execlist Pointer] are equal, this bit differentiates between Queue Full and Queue Empty.</p>		
	Value	Name	Description
0	Execlist Queue Empty [Default]		
1	Execlist Queue Full	There is a current and a pending execlist.	
1	Execlist Write Pointer		
Project:		CHV, BSW	
Format:		ExeclistContentsIndex	
<p>Determines which Execlist will be the next submitted to. When a new execlist is submitted, this pointer increments to point to the next execlist slot.</p>			
0	Current Execlist Pointer		
Default Value:		1h	
Project:		CHV, BSW	
Format:		ExeclistContentsIndex	
<p>Points at the currently executing Execlist (if there is one). This pointer advances when the first context of new execlist is restored.</p>			

Execlist Submit Port Register

EXECLIST_SUBMITPORT - Execlist Submit Port Register						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Access:	WO					
Size (in bits):	32					
Address:	02230h-02233h					
Name:	Execlist Submit Port Register					
ShortName:	EXECLIST_SUBMITPORT_RCSUNIT					
Address:	12230h-12233h					
Name:	Execlist Submit Port Register					
ShortName:	EXECLIST_SUBMITPORT_VCSUNIT0					
Address:	1A230h-1A233h					
Name:	Execlist Submit Port Register					
ShortName:	EXECLIST_SUBMITPORT_VECSUNIT					
Address:	1C230h-1C233h					
Name:	Execlist Submit Port Register					
ShortName:	EXECLIST_SUBMITPORT_VCSUNIT1					
Address:	22230h-22233h					
Name:	Execlist Submit Port Register					
ShortName:	EXECLIST_SUBMITPORT_BCSUNIT					
<p>SW should submit a new pending execlist to this register. The DWs of the context descriptors must be written in a specific order: Element 1 must be written first and then Element 0. For each Element, DW1 must be written first followed by DW0. Context descriptors for both the elements must be written even if only one context are being submitted. The valid bits of the unused context descriptors should be set to 0.</p> <table border="1"> <thead> <tr> <th style="text-align: left;">Order of DW Submission to the Execlist Port</th> </tr> </thead> <tbody> <tr> <td>Element 1, High Dword</td> </tr> <tr> <td>Element 1, Low Dword</td> </tr> <tr> <td>Element 0, High Dword</td> </tr> <tr> <td>Element 0, Low Dword</td> </tr> </tbody> </table> <p>If a execlist of only one element is being submitted, it must be submitted in Element 0. It is UNDEFINED to submit a execlist with the valid bit of Element 0 clear (an "empty" execlist). It is possible that one or all of the contexts submitted in a execlists are "empty"; that is, have head and tail pointers equal to each other indicating no commands to be run. All of the valid bits in the Execlist Element Status Registers for the "about to be submitted" execlist will be cleared when the first DW (DW1 of Element 1) is written to the submit port.</p>		Order of DW Submission to the Execlist Port	Element 1, High Dword	Element 1, Low Dword	Element 0, High Dword	Element 0, Low Dword
Order of DW Submission to the Execlist Port						
Element 1, High Dword						
Element 1, Low Dword						
Element 0, High Dword						
Element 0, Low Dword						

EXECLIST_SUBMITPORT - Execlist Submit Port Register

Submission of the Element 0 Context Descriptor low Dword with the valid bit set is interpreted as a request to switch (as soon as possible) to the new execlist, i.e., a pre-emption request.

If a submitted Execlist's Element 0 Context Descriptor LRCA matches the LRCA of the currently executing context, then the newly submitted execlist will become the currently executing execlist without any context switch and without any impact to the executing context except that it will re-sample the tail pointer from the context image. This is done in case more commands have been inserted into its ring buffer between the first execlist submission and the 2nd.

Programming Notes	Source
SW must ensure the contexts submitted to the both the context descriptors in the execlist are different, i.e SW must not submit the same context descriptor to both the elements of the execlist.	
SW must follow below programming sequence for ELSP submission in host mode of. SW must set Force Wakeup bit to prevent GT from entering C6 while ELSP writes are in progress. Ex: Set Force Wakeup Program ELSP writes Reset Force Wakeup	
<p>Render CS Only: Command Streamer triggers IDLE sequence flows for RDOP_CG on un-successful Semaphore Waits and Wait for Display Events when "Inhibit Synchronous Context Switch" is set in CTXT_SR_CTL register. As part of IDLE flows CS flushes the Write Caches (Z, Color, HDC). While IDLE flush in progress context switch can happen due to pending execlist submitted and when this condition occurs CS might not issue context switch flush resulting in RO caches not invalidated (State, Texture, Instruction, Constant).</p> <p>To WA above issue, SW must always program a valid BB_PER_CTX_PTR for every context submitted with a PIPE_CONTROL command to invalidate all RO caches.</p> <p>PIPE_CONTROL with below bits set in it:</p> <ul style="list-style-type: none"> Instruction Cache Invalidate Enable Texture Cache Invalidate Enable Constant Cache Invalidate Enable State Cache Invalidate Enable 	RenderCS
[All Command Streamers]: When SW intends to use semaphore signaling between Command streamers, SW must avoid lite restores in HW by programming Force Restore bit to '1' in context descriptor during context submission, this is required to avoid known HW issue.	
Workaround	Source
<p>Workaround:</p> <p>SW must always ensure there are valid commands to be executed by HW on a context submission, i.e ring buffer head pointer must not be equal to the ring buffer head pointer on context submission to HW for execution.</p>	RenderCS

EXECLIST_SUBMITPORT - Execlist Submit Port Register

Additional Note:

This WA need not be applied when the arbitration is not disabled prior to executing "Batch Buffer Per Context Pointer" as part of context restore. Arbitration can be disabled prior to executing "Batch Buffer Per Context Pointer" by programming MI_ARB_ON_OFF (arbitration disable) in indirect context pointer.

Workaround:

SW must always ensure a preempted context submitted to HW doesn't undergo lite restore due to the same context getting submitted on the next Execlist submission.

This can be achieved by setting "Force Restore Bit" in the context descriptor of the context getting submitted and if the same context is known to be submitted to HW for execution on the earlier Execlist submission Or

SW on submitting a **preempted** context must wait for the context to switch out before submitting the same context to the Execlist Submit Port.

Note:

This WA need not be applied when "Force Sync Command Ordering" bit of INSTPM register is not disabled (programmed to value '0') during execution of "Batch Buffer Per Context Pointer" during context restore. "Force Sync Command Ordering" can be disabled prior to or during execution of "Batch Buffer Per Context Pointer" by programming INSTPM register using MI_LOAD_REGISTER_IMM command in Indirect Context Pointer or in "Batch Buffer Per Context Pointer".

Disabling of "Force Sync Command Ordering" during "Batch Buffer Per Context Pointer" execution was required to address Resource Streamer related preemption issue on HSD 1912487, this WA is not applied when Resource Streamer (RS) is not enabled or when a Resource Streamer enabled context is not preemptable.

DWord	Bit	Description		
0	31:0	<p>Context Descriptor DW</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>Context Descriptor</td> </tr> </table> <p>See "Context Descriptor Format" for format. The element that this DW is submitted as and whether it is the high DW or the low DW is determined by order. This register must be written to 4 times in order to submit a execlist.</p>	Format:	Context Descriptor
Format:	Context Descriptor			

Execute Condition Code Register

EXCC - Execute Condition Code Register					
Register Space:	MMIO: 0/2/0				
Project:	CHV, BSW				
Source:	RenderCS				
Default Value:	0x00000000				
Access:	R/W, RO				
Size (in bits):	32				
Trusted Type:	1				
Address:	02028h				
Address:	12028h-1202Bh				
Name:	Execute Condition Code Register				
ShortName:	EXCC_VCSUNIT0				
Address:	1A028h-1A02Bh				
Name:	Execute Condition Code Register				
ShortName:	EXCC_VECSUNIT				
Address:	1C028h-1C02Bh				
Name:	Execute Condition Code Register				
ShortName:	EXCC_VCSUNIT1				
Address:	22028h-2202Bh				
Name:	Execute Condition Code Register				
ShortName:	EXCC_BCSUNIT				
<p>This register contains user defined and hardware generated conditions that are used by MI_WAIT_FOR_EVENT commands. An MI_WAIT_FOR_EVENT instruction excludes the executing ring from arbitration if the selected event evaluates to a 1, while instruction is discarded if the condition evaluates to a 0. Once excluded a ring is enabled into arbitration when the selected condition evaluates to a 0.</p> <p>This register also contains control for the invalidation of indirect state pointers on context restore.</p>					
DWord	Bit	Description			
0	31:16	<p>Mask Bits</p> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>Mask[15:0]</td> </tr> </table> <p>These bits serves as a write enable for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.</p>	Format:	Mask[15:0]	
	Format:	Mask[15:0]			
15	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ
Project:	CHV, BSW				
Format:	MBZ				

EXCC - Execute Condition Code Register					
14	<p>Context Wait for V-blank on Pipe-C</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This field when set indicates the corresponding context has executed MI_WAIT_FOR_EVENT with "Display Pipe C Vertical Blank Wait Enable" set. This is an internal HW flag and should not be accessed by SW.</p>	Project:	CHV, BSW		
Project:	CHV, BSW				
13	<p>Context Wait for V-blank on Pipe-B</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This field when set indicates the corresponding context has executed MI_WAIT_FOR_EVENT with "Display Pipe B Vertical Blank Wait Enable" set. This is an internal HW flag and should not be accessed by SW.</p>	Project:	CHV, BSW		
Project:	CHV, BSW				
12	<p>Context Wait for V-blank on Pipe-A</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This field when set indicates the corresponding context has executed MI_WAIT_FOR_EVENT with "Display Pipe A Vertical Blank Wait Enable" set. This is an internal HW flag and should not be accessed by SW.</p>	Project:	CHV, BSW		
Project:	CHV, BSW				
11	<p>Pending Indirect State Dirty Bit</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>This field keeps track of whether or not an indirect state pointer command has been parsed in the current context. Clears either on a context save or explicitly through a flush command. This bit is Read Only.</p>	Project:	CHV, BSW	Access:	RO
Project:	CHV, BSW				
Access:	RO				
10:7	<p>Pending Indirect State Counter</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table> <p>This field keeps track of the maximum number of indirect state pointers pending in the system. When the register is saved/restored, it saves either a value of 1 or 0. This field is Read-Only.</p>	Project:	CHV, BSW		
Project:	CHV, BSW				
6:5	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ				
4:0	<p>User Defined Condition Codes</p> <p>The software may signal a Stream Semaphore by setting the Mask bit and Signal Bit together to match the bit field specified in a WAIT_FOR_EVENT (Semaphore).</p>				

FAULT_TLB_RD_DATA0 Register

FAULT_TLB_RD_DATA0 - FAULT_TLB_RD_DATA0 Register						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B10h					
DWord	Bit	Description				
0	31:0	FAULT_TLB_READ_DATA0 Register <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Fault cycle Virtual address [43:12]	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

FAULT_TLB_RD_DATA1 Register

FAULT_TLB_RD_DATA1 - FAULT_TLB_RD_DATA1 Register			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	04B14h		
DWord	Bit	Description	
0	31:0	FAULT_TLB_READ_DATA1 Register	
		Default Value:	00000000h
		Access:	RO
		Bit[31:5] Reserved Bit[4] Cycle GTT SEL (1-GGTT Cycle, 0-PPGTT Cycle) Bit[3:0] Fault cycle Virtual address [47:44]	

Fault Switch Out

FAULT_SO - Fault Switch Out						
Register Space:	MMIO: 0/2/0					
Project:	CHV					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04590h					
DWord	Bit	Description				
0	31:0	Fault Switch Out <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

FBC_RT_BASE_ADDR_REGISTER

FBC_RT_BASE_ADDR_REGISTER - FBC_RT_BASE_ADDR_REGISTER											
Register Space:	MMIO: 0/2/0										
Project:	CHV, BSW										
Source:	RenderCS										
Default Value:	0x00000000										
Access:	R/W										
Size (in bits):	32										
Address:	07020h										
Valid Projects:	CHV, BSW										
This Register is saved and restored as part of Context.											
DWord	Bit	Description									
0	31:12	FBC RT Base Address									
		<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>Format:</td> <td>PPGraphicsAddress[31:12]</td> </tr> </table> <p>4KB aligned Base Address as mapped in the PPGTT or in the GGTT for the render target. This base address must be the one that is either front buffer or the back-buffer (a flip target). It must be programmed before any draw call binding that render target base address.</p>	Access:	R/W	Format:	PPGraphicsAddress[31:12]					
Access:	R/W										
Format:	PPGraphicsAddress[31:12]										
	11:2	Reserved									
		<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Access:	R/W	Format:	PBC					
Access:	R/W										
Format:	PBC										
1		FBC Front Buffer Target									
		Project:	CHV, BSW								
		Access:	R/W								
		Format:	Enable								
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>[Default]</td> <td>FBC is targeting the Back Buffer for compression. This buffer can be cached in the MLC/LLC, so a GFDT flush is required before FBC can begin compression.</td> </tr> <tr> <td>1h</td> <td></td> <td>FBC is targeting the Font Buffer for compression. This buffer cannot be cached in the MLC/LLC. FBC compression can begin after any RC flush.</td> </tr> </tbody> </table>	Value	Name	Description	0h	[Default]	FBC is targeting the Back Buffer for compression. This buffer can be cached in the MLC/LLC, so a GFDT flush is required before FBC can begin compression.	1h		FBC is targeting the Font Buffer for compression. This buffer cannot be cached in the MLC/LLC. FBC compression can begin after any RC flush.
Value	Name	Description									
0h	[Default]	FBC is targeting the Back Buffer for compression. This buffer can be cached in the MLC/LLC, so a GFDT flush is required before FBC can begin compression.									
1h		FBC is targeting the Font Buffer for compression. This buffer cannot be cached in the MLC/LLC. FBC compression can begin after any RC flush.									

FBC_RT_BASE_ADDR_REGISTER - FBC_RT_BASE_ADDR_REGISTER

	0	PPGTT Render Target Base Address Valid for FBC		
		Project:	CHV, BSW	
		Access:	R/W	
		Format:	Enable	
		Value	Name	Description
		0h	[Default]	Base address in this register [31:12] is not valid and therefore FBC will not get any modifications from rendering.
1h		Base address in this register [31:12] is valid and HW needs to compare the current render target base address with this base address to provide modifications to FBC.		

FBC_RT_BASE_ADDR_REGISTER_UPPER

FBC_RT_BASE_ADDR_REGISTER_UPPER - FBC_RT_BASE_ADDR_REGISTER_UPPER						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	RenderCS					
Default Value:	0x00000000					
Access:	R/W					
Size (in bits):	32					
Address:	07024h					
This Register is saved and restored as part of Context.						
DWord	Bit	Description				
0	31:16	Reserved				
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Access:	R/W	Format:	PBC
Access:	R/W					
Format:	PBC					
15:0	15:0	FBC RT Base Address High				
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> <tr> <td>Format:</td> <td>BaseAddress[47:32]</td> </tr> </table>	Access:	R/W	Format:	BaseAddress[47:32]
		Access:	R/W			
Format:	BaseAddress[47:32]					
<p>Must be set to modify corresponding data bit. Reads to this field returns zero. Upper 4KB aligned Base Address as mapped in the PPGTT or in the GGTT for the render target. This base address must be the one that is either front buffer or the back-buffer (a flip target). It can be only programmed once per context.</p>						
		Programming Notes				
		It must be programmed before any draw call binding that render target base address.				

FD

FD - FD						
Register Space:	PCI: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	000C4h					
Functional Disable. This register is used by SBIOS, not by driver.						
DWord	Bit	Description				
0	31:1	RESERVED				
		<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					
0	0	FUNCTION_DISABLE				
		<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Default Value:	0b	Access:	R/W
		Default Value:	0b			
Access:	R/W					
<table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td> FD: 0 : Default - normal operation. 1 : When set, the function is disabled (configuration space is disabled). All new requests on the IOSF Primary bus, including any new configuration cycle requests are not claimed on IOSF Primary. This bit as no effect register accessibility via IOSF SB. Once programmed to '1', the only way to re-enable device 2 is via an IOSF SB write of '0' to this register. </td> </tr> <tr> <td>CHV, BSW: Wire is sent to PSF for decode purposes gvd_psf_dev2disable_nczfwoh.</td> </tr> </tbody> </table>	Description	FD: 0 : Default - normal operation. 1 : When set, the function is disabled (configuration space is disabled). All new requests on the IOSF Primary bus, including any new configuration cycle requests are not claimed on IOSF Primary. This bit as no effect register accessibility via IOSF SB. Once programmed to '1', the only way to re-enable device 2 is via an IOSF SB write of '0' to this register.	CHV, BSW: Wire is sent to PSF for decode purposes gvd_psf_dev2disable_nczfwoh.			
Description						
FD: 0 : Default - normal operation. 1 : When set, the function is disabled (configuration space is disabled). All new requests on the IOSF Primary bus, including any new configuration cycle requests are not claimed on IOSF Primary. This bit as no effect register accessibility via IOSF SB. Once programmed to '1', the only way to re-enable device 2 is via an IOSF SB write of '0' to this register.						
CHV, BSW: Wire is sent to PSF for decode purposes gvd_psf_dev2disable_nczfwoh.						

FF Performance

FF_PERF - FF Performance				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	RenderCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Trusted Type:	1			
Address:	06B1Ch			
Valid Projects:	CHV, BSW			
DWord	Bit	Description		
0	31:16	Mask		
		Project:	All	
		Access:	WO	
		Format:	Mask[15:0]	
			Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)	
	15:11	Reserved		
		Project:	All	
		Access:	r/w	
	10:8	7:3	Throttle counter value	
			Project:	CHV, BSW
			Access:	r/w
		Format:	Disable	
				Counter value defining how many clocks the interface needs to be slowed down.
		Value	Name	Description
		0h	[Default]	Masked by default.
	7:3	Reserved		
Project:		CHV, BSW		
Access:		r/w		
Format:	PBC			

FF_PERF - FF Performance				
	2	Enable throttling for SF-WM interface		
		Access:	r/w	
		Format:	Disable	
		Value	Name	Description
		0h	Disable	No throttling
	1h	Enable	Enable throttling in all SF-WM interfaces	
	1	Enable throttling for SF-SBE interface		
		Access:	r/w	
		Format:	Disable	
		Value	Name	Description
		0h	Disable	No throttling
	1h	Enable	Enable throttling in all SF-SBE interfaces	
	0	Enable throttling for CL-SF interface		
		Access:	r/w	
		Format:	Disable	
Value		Name	Description	
0h		Disable	No throttling	
1h	Enable	Enable throttling in all CL-SF interfaces		

First Buffer Size and Start

FBSS - First Buffer Size and Start				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B420h			
LPFCREG02 - First Buffer Size and Start				
DWord	Bit	Description		
0	31:16	First Virtual Buffer Base		
		<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>First Virtual Buffer Base: Programmed by driver to allocate a memory space for performance data storage. The buffer size should be aligned to the size of the memory allocated so it naturally aligns to the base (i.e. for 128KB bit[16]=0, 256KB bit[17:16]=0, 512KB bit[18:16]=0). Signal - lpconf_lpfc_virtual_base0 [31:16].</p>	Access:	R/W
	Access:	R/W		
15:12	First Buffer Size			
		<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>First Buffer Size: Determines the allowed buffer size for performance data storage. 0000b: 64KB. 0001b: 128KB. 0010b: 256KB. 0011b: 512KB. ... 1111b: 2GB. Signal - lpconf_lpfc_buffer_size0 [3:0].</p>	Access:	R/W
Access:	R/W			
11:3		Reserved		
		<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> </table>	Project:	CHV, BSW
		Project:	CHV, BSW	
<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved.</p>	Access:	RO		
Access:	RO			

FBSS - First Buffer Size and Start													
2	<p>Frame count and Draw call enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>Enables the replacement of a specific L3 performance counter value in the reported data with a 16-bit tag created from the concatenation of the "Frame Count" and "Draw Call Number" programmable bitfields in the "Frame Count and Draw Call Number" register.</p> <p>The exact counter replaced is dependent on the programmed value of the "Counter Enabling Selection" bitfield. The replaced counter is always the last one, except in the case only a single performance counter is enabled for reporting (in which no replacement occurs):</p> <table border="1" style="width: 100%; margin-top: 10px;"> <thead> <tr> <th style="text-align: center;">CNTRENSEL Value</th> <th style="text-align: center;">Replaced Event Counter</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">00</td> <td style="text-align: center;">No Replacement</td> </tr> <tr> <td style="text-align: center;">01</td> <td style="text-align: center;">Counter 1</td> </tr> <tr> <td style="text-align: center;">10</td> <td style="text-align: center;">Counter 3</td> </tr> <tr> <td style="text-align: center;">11</td> <td style="text-align: center;">Counter 7</td> </tr> </tbody> </table>	Access:	R/W	CNTRENSEL Value	Replaced Event Counter	00	No Replacement	01	Counter 1	10	Counter 3	11	Counter 7
Access:	R/W												
CNTRENSEL Value	Replaced Event Counter												
00	No Replacement												
01	Counter 1												
10	Counter 3												
11	Counter 7												
1	Reserved												
0	<p>Master Counter Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>Master Counter Enable: This is the global enable for performance tracking. Once set, it kicks off all performance tracking mechanism.</p> <p>Signal - lpconf_lpfc_master_cnt_en.</p> <p>This bit is used by all slices.</p>	Access:	R/W										
Access:	R/W												

Flexible EU Event Control 0

EU_PERF_CNT_CTL0 - Flexible EU Event Control 0			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Address:	0E458h		
<p>This register configures flexible EU event 0/1. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.</p>			
DWord	Bit	Description	
0	31:24	Reserved	
		Project:	All
		Format:	MBZ
	23:20	Fine Event Filter Select EU event 1	
		Project:	CHV, BSW
		Format:	U4
	<p>This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 1. Note that the fine event filter is logically applied after the coarse event filter.</p>		
	19:16	Coarse Event Filter Select EU event 1	
		Project:	CHV, BSW
		Format:	U4
<p>This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 1. Note that the coarse event filter is logically applied before the fine event filter.</p>			
15:12	Increment Event for EU event 1		
	Project:	CHV, BSW	
	Format:	U4	
<p>This field controls which increment event provides the basis for flexible EU event 1.</p>			
11:8	Fine Event Filter Select EU event 0		
	Project:	CHV, BSW	
	Format:	U4	
<p>This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 0. Note that the fine event filter is logically applied after the coarse event filter.</p>			
7:4	Coarse Event Filter Select EU event 0		

EU_PERF_CNT_CTL0 - Flexible EU Event Control 0		
	Project:	CHV, BSW
	Format:	U4
	This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 0. Note that the coarse event filter is logically applied before the fine event filter.	
	3:0	Increment Event for EU event 0
	Project:	CHV, BSW
	Format:	U4
This field controls which increment event provides the basis for flexible EU event 0.		

Flexible EU Event Control 1

EU_PERF_CNT_CTL1 - Flexible EU Event Control 1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	0E558h	
<p>This register configures flexible EU event 2/3. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.</p>		
DWord	Bit	Description
0	31:24	Reserved
		Project: All
		Format: MBZ
	23:20	Fine Event Filter Select EU event 3
		Project: CHV, BSW
		Format: U4
	<p>This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 3. Note that the fine event filter is logically applied after the coarse event filter.</p>	
	19:16	Coarse Event Filter Select EU event 3
		Project: CHV, BSW
		Format: U4
	<p>This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 3. Note that the coarse event filter is logically applied before the fine event filter.</p>	
	15:12	Increment Event for EU event 3
Project: CHV, BSW		
Format: U4		
<p>This field controls which increment event provides the basis for flexible EU event 3.</p>		
11:8	Fine Event Filter Select EU event 2	
	Project: CHV, BSW	
	Format: U4	
<p>This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 2. Note that the fine event filter is logically applied after the coarse event filter.</p>		

EU_PERF_CNT_CTL1 - Flexible EU Event Control 1					
7:4	<p>Coarse Event Filter Select EU event 2</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U4</td> </tr> </table> <p>This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 2. Note that the coarse event filter is logically applied before the fine event filter.</p>	Project:	CHV, BSW	Format:	U4
Project:	CHV, BSW				
Format:	U4				
3:0	<p>Increment Event for EU event 2</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U4</td> </tr> </table> <p>This field controls which increment event provides the basis for flexible EU event 2.</p>	Project:	CHV, BSW	Format:	U4
Project:	CHV, BSW				
Format:	U4				

Flexible EU Event Control 2

EU_PERF_CNT_CTL2 - Flexible EU Event Control 2		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	0E658h	
<p>This register configures flexible EU event 4/5. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.</p>		
DWord	Bit	Description
0	31:24	Reserved
		Project: All
		Format: MBZ
	23:20	Fine Event Filter Select EU event 5
		Project: CHV, BSW
		Format: U4
	<p>This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 5. Note that the fine event filter is logically applied after the coarse event filter.</p>	
	19:16	Coarse Event Filter Select EU event 5
		Project: CHV, BSW
		Format: U4
	<p>This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 5. Note that the coarse event filter is logically applied before the fine event filter.</p>	
	15:12	Increment Event for EU event 5
Project: CHV, BSW		
Format: U4		
<p>This field controls which increment event provides the basis for flexible EU event 5.</p>		
11:8	Fine Event Filter Select EU event 4	
	Project: CHV, BSW	
	Format: U4	
<p>This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 4. Note that the fine event filter is logically applied after the coarse event filter.</p>		

EU_PERF_CNT_CTL2 - Flexible EU Event Control 2					
7:4	<p>Coarse Event Filter Select EU event 4</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U4</td> </tr> </table> <p>This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 4. Note that the coarse event filter is logically applied before the fine event filter.</p>	Project:	CHV, BSW	Format:	U4
Project:	CHV, BSW				
Format:	U4				
3:0	<p>Increment Event for EU event 4</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U4</td> </tr> </table> <p>This field controls which increment event provides the basis for flexible EU event 4.</p>	Project:	CHV, BSW	Format:	U4
Project:	CHV, BSW				
Format:	U4				

Flexible EU Event Control 3

EU_PERF_CNT_CTL3 - Flexible EU Event Control 3			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Address:	0E758h		
<p>This register configures flexible EU event 6/7. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.</p>			
DWord	Bit	Description	
0	31:24	Reserved	
		Project:	All
		Format:	MBZ
	23:20	Fine Event Filter Select EU event 7	
		Project:	CHV, BSW
		Format:	U4
	<p>This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 7. Note that the fine event filter is logically applied after the coarse event filter.</p>		
	19:16	Coarse Event Filter Select EU event 7	
		Project:	CHV, BSW
		Format:	U4
	<p>This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 7. Note that the coarse event filter is logically applied before the fine event filter.</p>		
	15:12	Increment Event for EU event 7	
Project:		CHV, BSW	
Format:		U4	
<p>This field controls which increment event provides the basis for flexible EU event 7.</p>			
11:8	Fine Event Filter Select EU event 6		
	Project:	CHV, BSW	
	Format:	U4	
<p>This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 6. Note that the fine event filter is logically applied after the coarse event filter.</p>			

EU_PERF_CNT_CTL3 - Flexible EU Event Control 3					
7:4	<p>Coarse Event Filter Select EU event 6</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U4</td> </tr> </table> <p>This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 6. Note that the coarse event filter is logically applied before the fine event filter.</p>	Project:	CHV, BSW	Format:	U4
Project:	CHV, BSW				
Format:	U4				
3:0	<p>Increment Event for EU event 6</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U4</td> </tr> </table> <p>This field controls which increment event provides the basis for flexible EU event 6.</p>	Project:	CHV, BSW	Format:	U4
Project:	CHV, BSW				
Format:	U4				

Flexible EU Event Control 4

EU_PERF_CNT_CTL4 - Flexible EU Event Control 4			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Address:	0E45Ch		
This register configures flexible EU event 8/9. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.			
DWord	Bit	Description	
0	31:24	Reserved	
		Project:	All
		Format:	MBZ
	23:20	Fine Event Filter Select EU event 9	
		Project:	CHV, BSW
		Format:	U4
	This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 9. Note that the fine event filter is logically applied after the coarse event filter.		
	19:16	Coarse Event Filter Select EU event 9	
		Project:	CHV, BSW
		Format:	U4
	This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 9. Note that the coarse event filter is logically applied before the fine event filter.		
	15:12	Increment Event for EU event 9	
Project:		CHV, BSW	
Format:		U4	
This field controls which increment event provides the basis for flexible EU event 9.			
11:8	Fine Event Filter Select EU event 8		
	Project:	CHV, BSW	
	Format:	U4	
This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 8. Note that the fine event filter is logically applied after the coarse event filter.			
7:4	Coarse Event Filter Select EU event 8		

EU_PERF_CNT_CTL4 - Flexible EU Event Control 4					
	<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U4</td> </tr> </table> <p>This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 8. Note that the coarse event filter is logically applied before the fine event filter.</p>	Project:	CHV, BSW	Format:	U4
Project:	CHV, BSW				
Format:	U4				
3:0	<p>Increment Event for EU event 8</p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U4</td> </tr> </table> <p>This field controls which increment event provides the basis for flexible EU event 8.</p>	Project:	CHV, BSW	Format:	U4
Project:	CHV, BSW				
Format:	U4				

Flexible EU Event Control 5

EU_PERF_CNT_CTL5 - Flexible EU Event Control 5		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	0E55Ch	
<p>This register configures flexible EU event 10/11. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.</p>		
DWord	Bit	Description
0	31:24	Reserved
		Project: All
		Format: MBZ
	23:20	Fine Event Filter Select EU event 11
		Project: CHV, BSW
		Format: U4
	<p>This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 11. Note that the fine event filter is logically applied after the coarse event filter.</p>	
	19:16	Coarse Event Filter Select EU event 11
		Project: CHV, BSW
		Format: U4
<p>This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 11. Note that the coarse event filter is logically applied before the fine event filter.</p>		
15:12	Increment Event for EU event 11	
	Project: CHV, BSW	
	Format: U4	
<p>This field controls which increment event provides the basis for flexible EU event 11.</p>		
11:8	Fine Event Filter Select EU event 10	
	Project: CHV, BSW	
	Format: U4	
<p>This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 10. Note that the fine event filter is logically applied after the coarse event filter.</p>		

EU_PERF_CNT_CTL5 - Flexible EU Event Control 5					
7:4	<p>Coarse Event Filter Select EU event 10</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U4</td> </tr> </table> <p>This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 10. Note that the coarse event filter is logically applied before the fine event filter.</p>	Project:	CHV, BSW	Format:	U4
Project:	CHV, BSW				
Format:	U4				
3:0	<p>Increment Event for EU event 10</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U4</td> </tr> </table> <p>This field controls which increment event provides the basis for flexible EU event 10.</p>	Project:	CHV, BSW	Format:	U4
Project:	CHV, BSW				
Format:	U4				

Flexible EU Event Control 6

EU_PERF_CNT_CTL6 - Flexible EU Event Control 6			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Address:	0E65Ch		
<p>This register configures flexible EU event 12/13. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.</p>			
DWord	Bit	Description	
0	31:24	Reserved	
		Project:	All
		Format:	MBZ
	23:20	Fine Event Filter Select EU event 13	
		Project:	CHV, BSW
		Format:	U4
	<p>This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 13. Note that the fine event filter is logically applied after the coarse event filter.</p>		
	19:16	Coarse Event Filter Select EU event 13	
		Project:	CHV, BSW
		Format:	U4
	<p>This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 13. Note that the coarse event filter is logically applied before the fine event filter.</p>		
	15:12	Increment Event for EU event 13	
		Project:	CHV, BSW
		Format:	U4
	<p>This field controls which increment event provides the basis for flexible EU event 13.</p>		
	11:8	Fine Event Filter Select EU event 12	
Project:		CHV, BSW	
Format:		U4	
<p>This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 12. Note that the fine event filter is logically applied after the coarse event filter.</p>			

EU_PERF_CNT_CTL6 - Flexible EU Event Control 6					
7:4	<p>Coarse Event Filter Select EU event 12</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U4</td> </tr> </table> <p>This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 12. Note that the coarse event filter is logically applied before the fine event filter.</p>	Project:	CHV, BSW	Format:	U4
Project:	CHV, BSW				
Format:	U4				
3:0	<p>Increment Event for EU event 12</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U4</td> </tr> </table> <p>This field controls which increment event provides the basis for flexible EU event 12.</p>	Project:	CHV, BSW	Format:	U4
Project:	CHV, BSW				
Format:	U4				

FORCE_TO_NONPRIV

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00002094
Access:	R/W
Size (in bits):	32
Address:	024D0h-024D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_RCSUNIT
Address:	024D4h-024D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_RCSUNIT
Address:	024D8h-024DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_RCSUNIT
Address:	024DCh-024DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_RCSUNIT
Address:	024E0h-024E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_RCSUNIT
Address:	024E4h-024E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_RCSUNIT
Address:	024E8h-024EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_RCSUNIT
Address:	024ECh-024EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_RCSUNIT
Address:	024F0h-024F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_RCSUNIT

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Address:	024F4h-024F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_RCSUNIT
Address:	024F8h-024FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_RCSUNIT
Address:	024FCh-024FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_RCSUNIT
Address:	124D0h-124D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VCSUNIT0
Address:	124D4h-124D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VCSUNIT0
Address:	124D8h-124DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VCSUNIT0
Address:	124DCh-124DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VCSUNIT0
Address:	124E0h-124E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VCSUNIT0
Address:	124E4h-124E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VCSUNIT0
Address:	124E8h-124EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VCSUNIT0
Address:	124ECh-124EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VCSUNIT0
Address:	124F0h-124F3h
Name:	FORCE_TO_NONPRIV

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
ShortName:	FORCE_TO_NONPRIV_8_VCSUNIT0
Address:	124F4h-124F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VCSUNIT0
Address:	124F8h-124FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VCSUNIT0
Address:	124FCh-124FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VCSUNIT0
Address:	1A4D0h-1A4D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VECSUNIT
Address:	1A4D4h-1A4D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VECSUNIT
Address:	1A4D8h-1A4DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VECSUNIT
Address:	1A4DCh-1A4DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VECSUNIT
Address:	1A4E0h-1A4E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VECSUNIT
Address:	1A4E4h-1A4E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VECSUNIT
Address:	1A4E8h-1A4EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VECSUNIT
Address:	1A4ECh-1A4EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VECSUNIT
Address:	1A4F0h-1A4F3h

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VECSUNIT
Address:	1A4F4h-1A4F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VECSUNIT
Address:	1A4F8h-1A4FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VECSUNIT
Address:	1A4FCh-1A4FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VECSUNIT
Address:	1C4D0h-1C4D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VCSUNIT1
Address:	1C4D4h-1C4D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VCSUNIT1
Address:	1C4D8h-1C4DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VCSUNIT1
Address:	1C4DCh-1C4DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VCSUNIT1
Address:	1C4E0h-1C4E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VCSUNIT1
Address:	1C4E4h-1C4E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VCSUNIT1
Address:	1C4E8h-1C4EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VCSUNIT1
Address:	1C4ECh-1C4EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VCSUNIT1

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Address:	1C4F0h-1C4F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VCSUNIT1
Address:	1C4F4h-1C4F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VCSUNIT1
Address:	1C4F8h-1C4FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VCSUNIT1
Address:	1C4FCh-1C4FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VCSUNIT1
Address:	224D0h-224D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_BCSUNIT
Address:	224D4h-224D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_BCSUNIT
Address:	224D8h-224DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_BCSUNIT
Address:	224DCh-224DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_BCSUNIT
Address:	224E0h-224E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_BCSUNIT
Address:	224E4h-224E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_BCSUNIT
Address:	224E8h-224EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_BCSUNIT
Address:	224ECh-224EFh
Name:	FORCE_TO_NONPRIV

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV							
ShortName:	FORCE_TO_NONPRIV_7_BCSUNIT						
Address:	224F0h-224F3h						
Name:	FORCE_TO_NONPRIV						
ShortName:	FORCE_TO_NONPRIV_8_BCSUNIT						
Address:	224F4h-224F7h						
Name:	FORCE_TO_NONPRIV						
ShortName:	FORCE_TO_NONPRIV_9_BCSUNIT						
Address:	224F8h-224FBh						
Name:	FORCE_TO_NONPRIV						
ShortName:	FORCE_TO_NONPRIV_10_BCSUNIT						
Address:	224FCh-224FFh						
Name:	FORCE_TO_NONPRIV						
ShortName:	FORCE_TO_NONPRIV_11_BCSUNIT						
<p>These registers are privilege registers and are not allowed to be written from non-privilege batch buffer. These are global registers and power context save/restored.</p>							
Programming Notes							
<p>RCS_FORCE_TO_NONPRIV registers in render CS must be used to force the below registers to be treated as non-privileged by HW:</p> <ul style="list-style-type: none"> • 0x7700 (GLOBAL_CLEAR_VALUE_0) • 0x7704 (GLOBAL_CLEAR_VALUE_1) • 0x7708 (GLOBAL_CLEAR_VALUE_2) • 0x770C (GLOBAL_CLEAR_VALUE_3) 							
DWord	Bit	Description					
0	31:26	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ			
	Format:	MBZ					
	25:2	<p>Non Privilege Register Address</p> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>MmioAddress[25:2]</td> </tr> </table> <p>This field contains the MMIO offset of a register. MMIO offset programmed in this field will be treated as a non-privilege register by render command streamer while processing register writes from a non-privilege batch buffer. This register provides programmability is to extend the non-privilege register table mentioned in MI_BATCH_BUFFER_START command in render command streamer.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>825h</td> <td>[Default]</td> </tr> </tbody> </table>	Format:	MmioAddress[25:2]	Value	Name	825h
Format:	MmioAddress[25:2]						
Value	Name						
825h	[Default]						
1:0	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ				
Format:	MBZ						

Frame count and Draw call number

FCDCN - Frame count and Draw call number				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B430h			
DWord	Bit	Description		
0	31:16	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	15:8	<p>Frame Number</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Frame number is the first of two reporting tags that software (i.e. driver) may populate in order to provide reference points during L3 performance reporting modes. Should the "Frame Count and Draw Call Enable" bit (FCDCE) in the "First Buffer Size and Start" register be set, LPFC will selectively replace one of the reporting events with this programmable tag (in addition to the "Draw Call Number" field below).</p> <p>Software may use this to provide reference points for L3 performance counts when parsing the resulting data stream to align reported counts to higher-level operations.</p> <p>The original incarnation called for software to increment this value with each frame, however, the field is generic and may be used for any tagging purpose.</p>	Access:	R/W
Access:	R/W			
7:0	<p>Draw call number</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>The draw call number is the second programmable reporting tag provided by LPFC. With this second programmable tag, a more granular sampling boundary may be created by software, or it may be used to provide an alternative reference point for tracking L3 performance. The original incarnation called for software to increment this value with every draw call, but the field is generic and may be used for any similar purpose.</p>	Access:	R/W	
Access:	R/W			

FUSEWORD0

FUSEWORD0 - FUSEWORD0						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	182130h					
Fuse readout information.						
DWord	Bit	Description				
0	31:0	FUSEDW0 <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Fuse Information DW0	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

FUSEWORD1

FUSEWORD1 - FUSEWORD1						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	182134h					
Fuse readout information.						
DWord	Bit	Description				
0	31:0	FUSEDW1 <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Fuse Information DW1	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

FUSEWORD2

FUSEWORD2 - FUSEWORD2						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	182138h					
Fuse readout information.						
DWord	Bit	Description				
0	31:0	FUSEDW2 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Fuse Information DW2	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

FUSEWORD3

FUSEWORD3 - FUSEWORD3						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	18213Ch					
Fuse readout information.						
DWord	Bit	Description				
0	31:0	FUSEDW3 <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Fuse Information DW3	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

FUSEWORD4

FUSEWORD4 - FUSEWORD4						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	182140h					
Fuse readout information.						
DWord	Bit	Description				
0	31:0	FUSEDW4 <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Fuse Information DW4	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

FUSEWORDS5

FUSEWORDS5 - FUSEWORDS5						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	182144h					
Fuse readout information.						
DWord	Bit	Description				
0	31:0	FUSEDW5 <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Fuse Information DW5	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

FUSEWORD6

FUSEWORD6 - FUSEWORD6						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	182148h					
Fuse readout information.						
DWord	Bit	Description				
0	31:0	FUSEDW6 <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Fuse Information DW6	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

FUSEWORD7

FUSEWORD7 - FUSEWORD7						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	18214Ch					
Fuse readout information.						
DWord	Bit	Description				
0	31:0	FUSEDW7 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Fuse Information DW7	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

FUSEWORD8

FUSEWORD8 - FUSEWORD8						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	182150h					
Fuse readout information.						
DWord	Bit	Description				
0	31:0	FUSEDW8 <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Fuse Information DW8	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

FUSEWORD9

FUSEWORD9 - FUSEWORD9						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	182154h					
Fuse readout information.						
DWord	Bit	Description				
0	31:0	FUSEDW9 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Fuse Information DW9	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

FUSEWORD10

FUSEWORD10 - FUSEWORD10						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	182158h					
Fuse readout information.						
DWord	Bit	Description				
0	31:0	FUSEDW10 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Fuse information DW10	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

FUSEWORD11

FUSEWORD11 - FUSEWORD11						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	18215Ch					
Fuse readout information.						
DWord	Bit	Description				
0	31:0	FUSEDW11 <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Fuse information DW11	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

FUSEWORD12

FUSEWORD12 - FUSEWORD12						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	182160h					
Fuse readout information. CHV, BSW: New for CHV, BSW.						
DWord	Bit	Description				
0	31:0	FUSEDW12 <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Fuse information DW12	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

FUSEWORD13

FUSEWORD13 - FUSEWORD13						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	182164h					
Fuse readout information. CHV, BSW: New for CHV, BSW.						
DWord	Bit	Description				
0	31:0	FUSEDW13 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Fuse information DW13	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

FUSEWORD14

FUSEWORD14 - FUSEWORD14						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	182168h					
Fuse readout information. CHV, BSW: New for CHV, BSW.						
DWord	Bit	Description				
0	31:0	<p>FUSEDW14</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Fuse information DW14 [31:28] - FUSE_GT_EU_DISABLE: SS1, ROW1 - EU[3:0] [27:24] - FUSE_GT_EU_DISABLE: SS1, ROW0 - EU[3:0] [23:20] - FUSE_GT_EU_DISABLE: SS0, ROW1 - EU[3:0] [19:16] - FUSE_GT_EU_DISABLE: SS0, ROW0 - EU[3:0] [11] - FUSE_GT_SUBSLICE_DISABLE - SS1 [10] - FUSE_GT_SUBSLICE_DISABLE - SS0</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

FUSEWORD15

FUSEWORD15 - FUSEWORD15						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	18216Ch					
Fuse readout information. CHV, BSW: New for CHV, BSW.						
DWord	Bit	Description				
0	31:0	FUSEDW15 <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Fuse information DW15	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

FUSEWORD16

FUSEWORD16 - FUSEWORD16						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	182170h					
Fuse readout information. CHV, BSW: New for CHV, BSW.						
DWord	Bit	Description				
0	31:0	FUSEDW16 <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Fuse information DW16	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

FUSEWORD17

FUSEWORD17 - FUSEWORD17								
Register Space:	MMIO: 0/2/0							
Project:	CHV, BSW							
Source:	PRM							
Default Value:	0x00000000							
Size (in bits):	32							
Address:	182174h							
Fuse readout information. CHV, BSW: New for CHV, BSW.								
DWord	Bit	Description						
0	31:0	FUSEDW17 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td colspan="2">Spare</td> </tr> </table>	Default Value:	00000000h	Access:	RO	Spare	
Default Value:	00000000h							
Access:	RO							
Spare								

FUSEWORD18

FUSEWORD18 - FUSEWORD18								
Register Space:	MMIO: 0/2/0							
Project:	CHV, BSW							
Source:	PRM							
Default Value:	0x00000000							
Size (in bits):	32							
Address:	182178h							
Fuse readout information. CHV, BSW: New for CHV, BSW.								
DWord	Bit	Description						
0	31:0	FUSEDW18 <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td colspan="2">Spare</td> </tr> </table>	Default Value:	00000000h	Access:	RO	Spare	
Default Value:	00000000h							
Access:	RO							
Spare								

FUSEWORD19

FUSEWORD19 - FUSEWORD19								
Register Space:	MMIO: 0/2/0							
Project:	CHV, BSW							
Source:	PRM							
Default Value:	0x00000000							
Size (in bits):	32							
Address:	18217Ch							
Fuse readout information. CHV, BSW: New for CHV, BSW.								
DWord	Bit	Description						
0	31:0	FUSEDW19 <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td colspan="2">Spare</td> </tr> </table>	Default Value:	00000000h	Access:	RO	Spare	
Default Value:	00000000h							
Access:	RO							
Spare								

G3D Control Register

G3DCTL - G3D Control Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	09024h			
G3D unit Control Register. Controls GUNIT's response to GAM Traffic.				
DWord	Bit	Description		
0	31:27	<p>G3D Spare</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%; text-align: center;">R/W</td> </tr> </table> <p>Spare config bits sent to G3D.</p>	Access:	R/W
	Access:	R/W		
	26	<p>RTN Mode</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%; text-align: center;">R/W</td> </tr> </table> <p>RTN mode. When set to one all GAM read returns are considered slow (no b2b to any source ID).</p>	Access:	R/W
	Access:	R/W		
	25	<p>Return Ordering Queue Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%; text-align: center;">R/W</td> </tr> </table> <p>ROQ Disable. When set to a '1', the G3D Return Ordering queue will be mostly disabled by forcing the Data queue to be considered full when it has one entry occupied.</p>	Access:	R/W
Access:	R/W			
24	<p>Command Bandwidth Arb Mode</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%; text-align: center;">R/W</td> </tr> </table> <p>Command Bandwidth Arbitration mode. When programmed to a '1', reads will be allowed to go 1 cycle after writes as long as writes are not in write grant mode.</p>	Access:	R/W	
Access:	R/W			
23:0	<p>RSVD</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%; text-align: center;">RO</td> </tr> </table> <p>Reserved.</p>	Access:	RO	
Access:	RO			

GAB Arbitration Programmable

GAB_AP - GAB Arbitration Programmable		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	040F0h	
DWord	Bit	Description
0	31:0	Reserved

GAB GAC GAM Idle

GABGACGAMIDLE - GAB GAC GAM Idle		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A540h-0A543h	
DWord	Bit	Description
0	31:26	Reserved Access: RO
	25:16	GAM Idle Timeout Access: R/W <hr/> <p style="text-align: center;">Programming Notes</p> This mode is not supported. It must be 0 at all times.
	15:10	Reserved Access: RO
	9:0	Min GAB GAC Idle Access: R/W <hr/> <p style="text-align: center;">Programming Notes</p> This mode is not supported. It must be 0 at all times.

GAB LRA 0

GAB_LRA_0 - GAB LRA 0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x1F100F00	
Size (in bits):	32	
Address:	04A70h	
DWord	Bit	Description
0	31:29	Reserved
		Default Value: 000b
		Access: RO
	28:24	GAB LRA1 Max
		Default Value: 11111b
		Access: R/W Maximum value of programmable LRA1.
	23:21	Reserved
		Default Value: 000b
Access: RO		
20:16	GAB LRA1 Min	
	Default Value: 10000b	
	Access: R/W Minimum value of programmable LRA1.	
15:13	Reserved	
	Default Value: 000b	
	Access: RO	
12:8	GAB LRA0 Max	
	Default Value: 01111b	
	Access: R/W Maximum value of programmable LRA0.	
7:5	Reserved	
	Default Value: 000b	
	Access: RO	

GAB_LRA_0 - GAB LRA 0						
	4:0	<p>GABLRA0 Min</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Minimum value of programmable LRA0.</p>	Default Value:	00000b	Access:	R/W
Default Value:	00000b					
Access:	R/W					

GAB LRA 1

GAB_LRA_1 - GAB LRA 1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000001	
Size (in bits):	32	
Address:	04A74h	
DWord	Bit	Description
0	31:4	Reserved
		Default Value: 0000000h
		Access: RO
	3:2	BLB
		Default Value: 00b
		Access: R/W Which LRA should BLB use.
	1:0	BCS
		Default Value: 01b
		Access: R/W Which LRA should BCS use.

GAB unit Control Register

GAB_CTL_REG - GAB unit Control Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	BlitterCS			
Default Value:	0x000000BF			
Access:	R/W			
Size (in bits):	32			
Address:	24000h			
DefaultValue=FF0000BFh Trusted Type = 1				
DWord	Bit	Description		
0	31:9	Reserved		
	8	Continue after Page Fault		
		Value	Name	Description
		1	GAB Set	Upon receiving a page fault when requesting an address translation, GAB will set address bit 39 to 1 and continue.
	0	GAB Hang	GAB will hang on a page fault. Default = b0.	
	7:6	PPGTT BCS TLB LRA MIN		
	Default Value:		10b	
	TLB Depth Partitioning Register In PP GTT Mode.			
	5:4	GAB write request priority signal value used in GAC arbitration		
	Default Value:		11b	
3:2	GAB read only request priority signal value used in GAC arbitration			
Default Value:		11b		
1:0	GAB read request priority signal value used in GAC arbitration			
Default Value:		11b		

GAC_GAM Arbitration Counters Register 0

ARB_GAC_GAM_REQCNTS0 - GAC_GAM Arbitration Counters Register 0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043A8h	
DWord	Bit	Description
0	31:22	Reserved
	21:16	Number of GAC WR requests to be accumulated before applying the arbitration
	15:14	Reserved
	13:8	Number of GAC R requests to be accumulated before applying the arbitration
	7:6	Reserved
	5:0	Number of GAC RO requests to be accumulated before applying the arbitration

GAC_GAM Arbitration Counters Register 1

ARB_GAC_GAM_REQCNTS1 - GAC_GAM Arbitration Counters Register 1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043ACh	
DWord	Bit	Description
0	31:22	Reserved
	21:16	Number of GAC WR requests to be accumulated before applying the arbitration
	15:14	Reserved
	13:8	Number of GAC R requests to be accumulated before applying the arbitration
	7:6	Reserved
	5:0	Number of GAC RO requests to be accumulated before applying the arbitration

GAC_GAM R Arbitration Register 0

ARB_R_GAC_GAM0 - GAC_GAM R Arbitration Register 0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043E0h	
DWord	Bit	Description
0	31:28	Reserved
	27	Priority for entry 1
	26:24	Goto field for entry 1 when request vector is 11b
	23:21	Goto field for entry 1 when request vector is 10b
	20:18	Goto field for entry 1 when request vector is 01b
	17:15	Goto field for entry 1 when request vector is 00b
	14:13	Reserved
	12	Priority for entry 0
	11:9	Goto field for entry 0 when request vector is 11b
	8:6	Goto field for entry 0 when request vector is 10b
	5:3	Goto field for entry 0 when request vector is 01b
	2:0	Goto field for entry 0 when request vector is 00b

GAC_GAM R Arbitration Register 1

ARB_R_GAC_GAM1 - GAC_GAM R Arbitration Register 1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043E4h	
DWord	Bit	Description
0	31:28	Reserved
	27	Priority for entry 3
	26:24	Goto field for entry 3 when request vector is 11b
	23:21	Goto field for entry 3 when request vector is 10b
	20:18	Goto field for entry 3 when request vector is 01b
	17:15	Goto field for entry 3 when request vector is 00b
	14:13	Reserved
	12	Priority for entry 2
	11:9	Goto field for entry 2 when request vector is 11b
	8:6	Goto field for entry 2 when request vector is 10b
	5:3	Goto field for entry 2 when request vector is 01b
	2:0	Goto field for entry 2 when request vector is 00b

GAC_GAM R Arbitration Register 2

ARB_R_GAC_GAM2 - GAC_GAM R Arbitration Register 2		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043E8h	
DWord	Bit	Description
0	31:28	Reserved
	27	Priority for entry 5
	26:24	Goto field for entry 5 when request vector is 11b
	23:21	Goto field for entry 5 when request vector is 10b
	20:18	Goto field for entry 5 when request vector is 01b
	17:15	Goto field for entry 5 when request vector is 00b
	14:13	Reserved
	12	Priority for entry 4
	11:9	Goto field for entry 4 when request vector is 11b
	8:6	Goto field for entry 4 when request vector is 10b
	5:3	Goto field for entry 4 when request vector is 01b
	2:0	Goto field for entry 4 when request vector is 00b

GAC_GAM R Arbitration Register 3

ARB_R_GAC_GAM3 - GAC_GAM R Arbitration Register 3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043ECh	
DWord	Bit	Description
0	31:28	Reserved
	27	Priority for entry 7
	26:24	Goto field for entry 7 when request vector is 11b
	23:21	Goto field for entry 7 when request vector is 10b
	20:18	Goto field for entry 7 when request vector is 01b
	17:15	Goto field for entry 7 when request vector is 00b
	14:13	Reserved
	12	Priority for entry 6
	11:9	Goto field for entry 6 when request vector is 11b
	8:6	Goto field for entry 6 when request vector is 10b
	5:3	Goto field for entry 6 when request vector is 01b
	2:0	Goto field for entry 6 when request vector is 00b

GAC_GAM RO Arbitration Register 0

ARB_RO_GAC_GAM0 - GAC_GAM RO Arbitration Register 0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043D0h	
DWord	Bit	Description
0	31:28	Reserved
	27	Priority for entry 1
	26:24	Goto field for entry 1 when request vector is 11b
	23:21	Goto field for entry 1 when request vector is 10b
	20:18	Goto field for entry 1 when request vector is 01b
	17:15	Goto field for entry 1 when request vector is 00b
	14:13	Reserved
	12	Priority for entry 01
	11:9	Goto field for entry 01 when request vector is 11b
	8:6	Goto field for entry 01 when request vector is 10b
	5:3	Goto field for entry 01 when request vector is 01b
	2:0	Goto field for entry 01 when request vector is 00b

GAC_GAM RO Arbitration Register 1

ARB_RO_GAC_GAM1 - GAC_GAM RO Arbitration Register 1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043D4h	
DWord	Bit	Description
0	31:28	Reserved
	27	Priority for entry 3
	26:24	Goto field for entry 3 when request vector is 11b
	23:21	Goto field for entry 3 when request vector is 10b
	20:18	Goto field for entry 3 when request vector is 01b
	17:15	Goto field for entry 3 when request vector is 00b
	14:13	Reserved
	12	Priority for entry 2
	11:9	Goto field for entry 2 when request vector is 11b
	8:6	Goto field for entry 2 when request vector is 10b
	5:3	Goto field for entry 2 when request vector is 01b
	2:0	Goto field for entry 2 when request vector is 00b

GAC_GAM RO Arbitration Register 2

ARB_RO_GAC_GAM2 - GAC_GAM RO Arbitration Register 2		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043D8h	
DWord	Bit	Description
0	31:28	Reserved
	27	Priority for entry 5
	26:24	Goto field for entry 5 when request vector is 11b
	23:21	Goto field for entry 5 when request vector is 10b
	20:18	Goto field for entry 5 when request vector is 01b
	17:15	Goto field for entry 5 when request vector is 00b
	14:13	Reserved
	12	Priority for entry 4
	11:9	Goto field for entry 4 when request vector is 11b
	8:6	Goto field for entry 4 when request vector is 10b
	5:3	Goto field for entry 4 when request vector is 01b
	2:0	Goto field for entry 4 when request vector is 00b

GAC_GAM RO Arbitration Register 3

ARB_RO_GAC_GAM3 - GAC_GAM RO Arbitration Register 3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043DCh	
DWord	Bit	Description
0	31:28	Reserved
	27	Priority for entry 7
	26:24	Goto field for entry 7 when request vector is 11b
	23:21	Goto field for entry 7 when request vector is 10b
	20:18	Goto field for entry 7 when request vector is 01b
	17:15	Goto field for entry 7 when request vector is 00b
	14:13	Reserved
	12	Priority for entry 6
	11:9	Goto field for entry 6 when request vector is 11b
	8:6	Goto field for entry 6 when request vector is 10b
	5:3	Goto field for entry 6 when request vector is 01b
	2:0	Goto field for entry 6 when request vector is 00b

GAC_GAM WR Arbitration Register 0

ARB_WR_GAC_GAM0 - GAC_GAM WR Arbitration Register 0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043F0h	
DWord	Bit	Description
0	31:28	Reserved
	27	Priority for entry 1
	26:24	Goto field for entry 1 when request vector is 11b
	23:21	Goto field for entry 1 when request vector is 10b
	20:18	Goto field for entry 1 when request vector is 01b
	17:15	Goto field for entry 1 when request vector is 00b
	14:13	Reserved
	12	Priority for entry 0
	11:9	Goto field for entry 0 when request vector is 11b
	8:6	Goto field for entry 0 when request vector is 10b
	5:3	Goto field for entry 0 when request vector is 01b
	2:0	Goto field for entry 0 when request vector is 00b

GAC_GAM WR Arbitration Register 1

ARB_WR_GAC_GAM1 - GAC_GAM WR Arbitration Register 1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043F4h	
DWord	Bit	Description
0	31:28	Reserved
	27	Priority for entry 3
	26:24	Goto field for entry 3 when request vector is 11b
	23:21	Goto field for entry 3 when request vector is 10b
	20:18	Goto field for entry 3 when request vector is 01b
	17:15	Goto field for entry 3 when request vector is 00b
	14:13	Reserved
	12	Priority for entry 2
	11:9	Goto field for entry 2 when request vector is 11b
	8:6	Goto field for entry 2 when request vector is 10b
	5:3	Goto field for entry 2 when request vector is 01b
	2:0	Goto field for entry 2 when request vector is 00b

GAC_GAM WR Arbitration Register 2

ARB_WR_GAC_GAM2 - GAC_GAM WR Arbitration Register 2		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043F8h	
DWord	Bit	Description
0	31:28	Reserved
	27	Priority for entry 5
	26:24	Goto field for entry 5 when request vector is 11b
	23:21	Goto field for entry 5 when request vector is 10b
	20:18	Goto field for entry 5 when request vector is 01b
	17:15	Goto field for entry 5 when request vector is 00b
	14:13	Reserved
	12	Priority for entry 4
	11:9	Goto field for entry 4 when request vector is 11b
	8:6	Goto field for entry 4 when request vector is 10b
	5:3	Goto field for entry 4 when request vector is 01b
	2:0	Goto field for entry 4 when request vector is 00b

GAC_GAM WR Arbitration Register 3

ARB_WR_GAC_GAM3 - GAC_GAM WR Arbitration Register 3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043FCh	
DWord	Bit	Description
0	31:28	Reserved
	27	Priority for entry 7
	26:24	Goto field for entry 7 when request vector is 11b
	23:21	Goto field for entry 7 when request vector is 10b
	20:18	Goto field for entry 7 when request vector is 01b
	17:15	Goto field for entry 7 when request vector is 00b
	14:13	Reserved
	12	Priority for entry 6
	11:9	Goto field for entry 6 when request vector is 11b
	8:6	Goto field for entry 6 when request vector is 10b
	5:3	Goto field for entry 6 when request vector is 01b
	2:0	Goto field for entry 6 when request vector is 00b

GAM and SA Communication Register

GAMSACOMREG - GAM and SA Communication Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	042A0h			
DWord	Bit	Description		
0	31:16	Mask Bits		
		Default Value:	0000h	
		Access:	RO	
		Mask Bits act as Write Enables for the bits[15:0] of this register.		
		GAM and SA Communication Register 15		
		Default Value:	0b	
Access:	R/W			
		For Future Use. This bit is self clear.		
14		GAM and SA Communication Register 14		
		Default Value:	0b	
		Access:	R/W	
		For Future Use. This bit is self clear.		
		13		GAM and SA Communication Register 13
				Default Value:
Access:	R/W			
For Future Use. This bit is self clear.				
12				GAM and SA Communication Register 12
				Default Value:
		Access:	R/W	
		For Future Use. This bit is self clear.		
		11		GAM and SA Communication Register 11
				Default Value:
Access:	R/W			
For Future Use.				

GAMSACOMREG - GAM and SA Communication Register

		This bit is self clear.	
10	GAM and SA Communication Register 10		
	Default Value:	0b	
	Access:	R/W	
For Future Use. This bit is self clear.			
9	GAM and SA Communication Register 9		
	Default Value:	0b	
	Access:	R/W	
For Future Use. This bit is self clear.			
8	GAM and SA Communication Register 8		
	Default Value:	0b	
	Access:	R/W	
For Future Use. This bit is self clear.			
7	GAM and SA Communication Register 7		
	Default Value:	0b	
	Access:	R/W	
For Future Use. This bit is self clear.			
6	GAM and SA Communication Register 6		
	Default Value:	0b	
	Access:	R/W	
For Future Use. This bit is self clear.			
5	GAM and SA Communication Register 5		
	Default Value:	0b	
	Access:	R/W	
For Future Use. This bit is self clear.			
4	GAM and SA Communication Register 4		
	Default Value:	0b	
	Access:	R/W	
For Future Use. This bit is self clear.			
3	GAM and SA Communication Register 3		
	Default Value:	0b	
	Access:	R/W	

GAMSACOMREG - GAM and SA Communication Register					
	<p>For Future Use. This bit is self clear.</p>				
2	<p>GAM and SA Communication Register 2</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>Bit2 - Root Table Address Update Request. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
1	<p>GAM and SA Communication Register 1</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>Bit1 - Queued Descriptor Request. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
0	<p>GAM and SA Communication Register 0</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>Bit0 - Context Cache Invalidator Request. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				

Gam Fub Done1 Lookup Register

DONE1_REG - Gam Fub Done1 Lookup Register						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0407Ch					
DWord	Bit	Description				
0	31:0	Gam Fub Done1 Lookup Reg <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> GAM Done1 signals.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Gam Fub Done Lookup Register

DONE_REG - Gam Fub Done Lookup Register						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	040B0h					
DWord	Bit	Description				
0	31:0	<p>Gam Fub Done Lookup Reg</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>31 CVS Credit Fifo is empty. 30 CVS TLB does not have any cycles. 29 Z Credit fifo is empty. 28 ZTLB does not have any cycles. 27 RCC Credit Fifo is empty. 26 RCC TLB does not have any cycles. 25 L3 Credit fifo is empty. 24 L3 TLB does not have any cycles. 23 VLF Credit fifo is empty. 22 VLF TLB does not have any cycles. 21 CASC Credit fifo empty. 20 CASC TLB does not have any cycles. 19 Miss Fub Done. 18 Read Stream Done. 17 Read Steam Fifo is empty. 16 Recycle Fifo in rstrm is empty. 15 TLB Pend Done. 14 TLB Pend PQ Array is done. 13 TLB pend PB Array is done. 12 Read route fub is done. 11 Gafm Data fifo is empty. 10 GAP data fifo is empty. 9 GAC data fifo is empty. 8 Wrdp is done with all the cycles. 7 Wrdp RID fifo is empty. 6 No hold from midarb to RTSTRM. 5 No hold from TLBPEND to MIDARB.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

DONE_REG - Gam Fub Done Lookup Register

		3 Tied to "1" - to be defined. 2 Fence FSM are IDLE. 1 Non PD Load Done. 0 Tied to "1" - to be defined.
--	--	--

GAM Put Delay

GAM_PUT_DLY - GAM Put Delay						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0401Ch					
Number of clocks to wait between puts						
DWord	Bit	Description				
0	31:0	GAM PUT DELAY <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GAMT_DONE Register

GAMT_DONE - GAMT_DONE Register						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04AC0h					
DWord	Bit	Description				
0	31:0	GAMT_DONE Register <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> 31: vebxtlb_all_done_f 30: cvstlb_all_done_f 29: ztlb_all_done_f 28: l3tlb_all_done_f 27: rcctlb_all_done_f 26: mfxtlb_all_done_f 25: vlftlb_all_done_f 24: bwgtlb_all_done_f 23: gamwrrb_all_done_f 22: mfxsl1tlb_all_done_f 21: vlfl1tlb_all_done_f 20: bwgtlb_fifo_empty 19: l3tlb_fifo_empty 18: ztlb_fifo_empty 17: rcctlb_fifo_empty 16: cvstlb_fifo_empty 15: vebxtlb_fifo_empty 14: mfxtlb_fifo_empty 13: mfxsl1tlb_fifo_empty 12: vlfl1tlb_fifo_empty 11: vlftlb_fifo_empty 10: wrdp_gafm_fifo_empty 9: wrdp_gap_fifo_empty 8: wrdp_gacfg_fifo_empty 7: wrdp_cs_fifo_empty 6: wrdp_vecs_fifo_empty 5: wrdp_oacs_fifo_empty 4: wrdp_gacv_fifo_empty	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

GAMT_DONE - GAMT_DONE Register

		3: Tied to 1
		2: Tied to 1
		1: Tied to 1
		0: Tied to 1

GAMT_ECO_REG_RO_IA

GAMT_ECO_REG_RO_IA - GAMT_ECO_REG_RO_IA						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04AB4h					
DWord	Bit	Description				
0	31:0	GAMTECO_REG_RO_IA <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> This register is for ECO usage. RO register with IA Access Type on DEV reset.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

GAMT_ECO_REG_RW_IA

GAMT_ECO_REG_RW_IA - GAMT_ECO_REG_RW_IA						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW, :GT2:B					
Source:	PRM					
Default Value:	0x0000AB1B					
Size (in bits):	32					
Address:	04AB0h					
Programmable Request Count - VEBX and BLT						
DWord	Bit	Description				
0	31:0	<p>GAMTECO_REG_RW_IA</p> <table border="1"> <tr> <td>Default Value:</td> <td>0000AB1Bh</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit[31:16] = Reserved. Bit[15:8] = Number of max outstanding cycles (Misses and Hits not present) that can be allowed to potentially fault = 171. Bit[7:6] = Reserved. Bit[5:0] = Number of max outstanding misses that can be allowed to potentially fault = 27.</p>	Default Value:	0000AB1Bh	Access:	R/W
Default Value:	0000AB1Bh					
Access:	R/W					

GAMT Arbiter Mode Control

GAMTARBMODE - GAMT Arbiter Mode Control			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000 CHV, BSW		
Size (in bits):	32		
Address:	04A08h		
DWord	Bit	Description	
0	31:16	Mask Bits	
		Default Value:	0000h
		Access:	RO
	15	GAMT Arbiter Mode Control 15	
		Default Value:	0b
		Access:	R/W
		For Future Use	
14	GAMT Arbiter Mode Control 14		
	Default Value:	0b	
	Project:	CHV, BSW	
	Access:	R/W	
		0 - Cache the TLB even if there is a FAULT in GAMW read return. 1 - Don't Cache the TLB if there is a fault in GAMW return.	
13	GAMT Arbiter Mode Control 13		
	Default Value:	0b	
	Access:	R/W	
		0 - VEBXTLB clock gate enabled. 1 - VEBXTLB clock gate disabled.	
12	GAMT Arbiter Mode Control 12		
	Default Value:	0b	
	Access:	R/W	
		0 - MFXSL1TLB clock gate enabled. 1 - MFXSL1TLB clock gate disabled.	
11	GAMT Arbiter Mode Control 11		
	Default Value:	0b	
	Access:	R/W	
		0 - VLFSL1TLB clock gate enabled. 1 - VLFSL1TLB clock gate disabled.	

GAMTARBMODE - GAMT Arbiter Mode Control			
10	GAMT Arbiter Mode Control 10		
	Default Value:	0b	
	Access:	R/W	
	0 - gamwrrb clock gate enabled. 1 - gamwrrb clock gate disabled.		
	9	GAMT Arbiter Mode Control 9	
		Default Value:	0b
		Access:	R/W
0 - BWGTLB clock gate enabled. 1 - BWGTLB clock gate disabled.			
8	GAMT Arbiter Mode Control 8		
	Default Value:	0b	
	Access:	R/W	
0 - VLFTLB clock gate enabled. 1 - VLFTLB clock gate disabled.			
7	GAMT Arbiter Mode Control 7		
	Default Value:	0b	
	Access:	R/W	
0 - MFXTLB clock gate enabled. 1 - MFXTLB clock gate disabled.			
6	GAMT Arbiter Mode Control 6		
	Default Value:	0b	
	Access:	R/W	
0 - RCCTLB clock gate enabled. 1 - RCCTLB clock gate disabled.			
5	GAMT Arbiter Mode Control 5		
	Default Value:	0b	
	Access:	R/W	
	0 - L3TLB clock gate enabled. 1 - L3TLB clock gate disabled. bit[5] needs to be set as a work-around due to recent gacb bug. To update bit 5, a value of 0x00200020 needs to be written.		
4	GAMT Arbiter Mode Control 4		
	Default Value:	0b	
	Access:	R/W	
0 - ZTLB clock gate enabled. 1 - ZTLB clock gate disabled.			

GAMTARBMODE - GAMT Arbiter Mode Control					
3	<p>GAMT Arbiter Mode Control 3</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>0 - CVS clock gate enabled. 1 - CVS clock gate disabled.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
2	<p>GAMT Arbiter Mode Control 2</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>0 - No reg_hdc_inval_ack_force - take the value from client. 1 - reg_hdc_inval_ack_force - force value to 1 - disregard client value.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
1	<p>GAMT Arbiter Mode Control 1</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit [1]: Address Swizzling for Tiled Surfaces. This register location is updated via GFX Driver prior to enabling DRAM accesses. Driver needs to obtain the need for memory address swizzling via DRAM configuration registers and set the following bits (in Display Engine and Render/Media access streams). 0: No address Swizzling. 1: Address bit[1] needs to be swizzled for tiled surfaces.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
0	<p>GAMT Arbiter Mode Control 0</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit[0]: GAM to Bypass GTT Translation. GAM to Bypass GTT Translation and pass logical addresses through with 0's padded on the MSBs to form the Physical Address.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				

GAMW_ECO_BUS_RO_IA

GAMW_ECO_BUS_RO_IA - GAMW_ECO_BUS_RO_IA						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0408Ch					
DWord	Bit	Description				
0	31:0	GAMWECO_BUS_RO_IA <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>This register is for ECO usage. RO register with IA Access Type on BUS reset.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

GAMW_ECO_BUS_RW_IA

GAMW_ECO_BUS_RW_IA - GAMW_ECO_BUS_RW_IA			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	04084h		
DWord	Bit	Description	
0	31:0	GAMWECO_BUS_RW_IA	
		Default Value:	00000000h
		Access:	R/W
		This register is for ECO usage. RW register with IA Access Type on BUS reset.	

GAMW_ECO_DEV_RO_IA

GAMW_ECO_DEV_RO_IA - GAMW_ECO_DEV_RO_IA						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04088h					
DWord	Bit	Description				
0	31:0	GAMWECO_DEV_RO_IA <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>This register is for ECO usage. RO register with IA Access Type on DEV reset.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

GAMW_ECO_DEV_RW_IA

GAMW_ECO_DEV_RW_IA - GAMW_ECO_DEV_RW_IA		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04080h	
DWord	Bit	Description
0	31:0	GAMWECO_DEV_RW_IA
		Default Value: 00000000h
		Access: R/W

GAMW Power Context Save

PWRCTXSAVE - GAMW Power Context Save			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	04000h		
DWord	Bit	Description	
0	31:16	Mask Bits	
		Default Value:	0000h
		Access:	RO
			Mask Bits act as Write Enables for the bits[15:0] of this register.
	15	Extra Bits15	
		Default Value:	0b
		Access:	R/W
		Extra Bits for future use.	
14	Extra Bits14		
	Default Value:	0b	
	Access:	R/W	
		Extra Bits for future use.	
13	Extra Bits13		
	Default Value:	0b	
	Access:	R/W	
		Extra Bits for future use.	
12	Extra Bits12		
	Default Value:	0b	
	Access:	R/W	
		Extra Bits for future use.	
11	Extra Bits11		
	Default Value:	0b	
	Access:	R/W	
		Extra Bits for future use.	
10	Extra Bits10		
	Default Value:	0b	
	Access:	R/W	
		Extra Bits for future use.	

PWRCTXSAVE - GAMW Power Context Save

9	Power Context Save Request		
		Default Value:	0b
		Access:	R/W
	Power Context Save Bit[9] Power Context Save Request 1'b0: Power context save is not being requested (default). 1'b1: Power context save is being requested. Unit needs to self-clear this bit upon sampling. This bit is self clear.		
8:0	Power Context Save Quad Word Credits		
		Default Value:	000000000b
		Access:	R/W
	Power Context Save Bits[8:0] QWord Credits for Power Context Save Request An initial length packet is required per power context save session, but that packet does not consume a credit. See protocol description for more details. Minimum Credits = 1: Unit may send 1 QWord pair. Maximum Credits = 511: Unit may send 511 QWord pairs. A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Only valid with PWRCTX_SAVE_REQ (Bit9).		

GARB Messaging Register for Boot Controller

MSG_GARB_MBC - GARB Messaging Register for Boot Controller				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	16			
Address:	0801Ch			
<p>Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.</p>				
DWord	Bit	Description		
0	15:7	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	6	<p>Fuse Download Done Indication</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Fuse Download Done Indication 1'b0 : Fuse download is not complete yet <default> 1'b1 : Fuse download is complete gpmunit self-clears this bit upon sampling.</p>	Access:	R/W
	Access:	R/W		
	5	<p>Boot Fetch Complete Indication</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Boot Fetch Complete Indication 1'b0 : Boot Fetch is not complete yet <default> 1'b1 : Boot Fetch is complete gpmunit self-clears this bit upon sampling.</p>	Access:	R/W
	Access:	R/W		
4	<p>IDI Block Status</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>IDI Block Status 1'b0 : IDI interface is not blocked <default> 1'b1 : IDI interface is blocked</p>	Access:	R/W	
Access:	R/W			
3	<p>IDI Awake Status</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>IDI Awake Status 1'b0 : IDI interface is not ready <default> 1'b1 : IDI interface is ready</p>	Access:	R/W	
Access:	R/W			
2	<p>Credit Active Status</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Credit Active Status 1'b0 : Send credit active deassert Event Bus Message on transition from 1'b1 => 1'b0 <default> 1'b1 : Send credit active assert Event Bus Message on transition from 1'b0 => 1'b1</p>	Access:	R/W	
Access:	R/W			

MSG_GARB_MBC - GARB Messaging Register for Boot Controller			
1	<p>Global Arbitration Request</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>Global Arbitration Request 1'b0 : No request <default> 1'b1 : Request for arbitration Full handshake requiring ack</p>	Access:	R/W
Access:	R/W		
0	<p>Busy Indication</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>Busy Indication 1'b0 : Idle <default> 1'b1 : Busy Full handshake requiring ack</p>	Access:	R/W
Access:	R/W		

GARB Messaging Register for Clocking Unit

MSG_GARB_GCP - GARB Messaging Register for Clocking Unit				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	16			
Address:	08024h			
<p>Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.</p>				
DWord	Bit	Description		
0	15:3	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	2	<p>GCP Request to send FLR Complete Message to SA via GAM</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>GCP Request to send FLR Complete Message to SA via GAM 1'b0 : No request <default> 1'b1 : Send cycle on GA* Interface to address < address > with data < data > gpm will self-clear the request once it completes it. MBC needs to self-clear the acknowledgement once it sees it. GPM indicates a write cycle is complete once it puts it on the interface. GPM indicates a read cycle is complete once the read-return data comes back. gpmunit self-clears this bit upon sampling.</p>	Access:	R/W
	Access:	R/W		
1	<p>Global Arbitration Request</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Global Arbitration Request 1'b0 : No request <default> 1'b1 : Request for arbitration Full handshake requiring ack</p>	Access:	R/W	
Access:	R/W			
0	<p>Busy Indication</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Busy Indication 1'b0 : Idle <default> 1'b1 : Busy Full handshake requiring ack</p>	Access:	R/W	
Access:	R/W			

Gather Constants Not Consumed By RCS

GATHER_CONST_PRODUCE_COUNT - Gather Constants Not Consumed By RCS		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	0248Ch	
<p>This register keeps track of the outstanding Gather Constants produced by RS which are not yet consumed by Render Command Streamer. This register is part of the render context save and restore. This register should not be programmed by SW.</p>		
DWord	Bit	Description
0	31:0	<p>Gather Constants Produce Count</p> <p>This register keeps track of the outstanding Gather Constants produced by RS which are not yet consumed by Render Command Streamer. This register is part of the render context save and restore.</p>

GDR Per Client Write Drop Enables

WR_DROP_MODE - GDR Per Client Write Drop Enables				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	040B4h			
DWord	Bit	Description		
0	31:0	GDR Per Client Write Drop Enables		
		<table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>31 RSVD: Future use. 30 MBC write drop disable (0) or enable (1). 29 CS write drop disable (0) or enable (1). 28 SOL write drop disable (0) or enable (1). 27 RS write drop disable (0) or enable (1). 26 RCC write drop disable (0) or enable (1). 25 MSC write drop disable (0) or enable (1). 24 All L3 clients write drop disable (0) or enable (1). 23 STC write drop disable (0) or enable (1). 22 HIZ write drop disable (0) or enable (1). 21 RCZ write drop disable (0) or enable (1). 20 GAFS write drop disable (0) or enable (1). 19 GPM write drop disable (0) or enable (1). 18 GCP write drop disable (0) or enable (1). 17 VCS write drop disable (0) or enable (1). 16 BSP write drop disable (0) or enable (1). 15 VCR write drop disable (0) or enable (1). 14 VMX_RS write drop disable (0) or enable (1). 13 VMX_BS write drop disable (0) or enable (1). 12 VMX_RA write drop disable (0) or enable (1). 11 VMX_VDS write drop disable (0) or enable (1). 10 VLF_RS write drop disable (0) or enable (1). 9 VLF_FW write drop disable (0) or enable (1). 8 VECS write drop disable (0) or enable (1). 7 VEO write drop disable (0) or enable (1).</p>	Default Value:	00000000h
Default Value:	00000000h			
Access:	R/W			

WR_DROP_MODE - GDR Per Client Write Drop Enables

- | | | |
|--|--|--|
| | | <ul style="list-style-type: none">5 uC (DMA) write drop disable (0) or enable (1).4 BCS write drop disable (0) or enable (1).3 BLB write drop disable (0) or enable (1).2 W_BSP write drop disable (0) or enable (1).1 W_VMX_RS write drop disable (0) or enable (1).0 W_VMX_BS write drop disable (0) or enable (1). |
|--|--|--|

GDR Write Drop

GDR_WR_DRP - GDR Write Drop						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04020h					
DWord	Bit	Description				
0	31:0	GDR_WRITE_DROP <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

General Purpose Power Management Performance Idle Hysteresis

GPMPIHYST - General Purpose Power Management Performance Idle Hysteresis				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A070h-0A073h			
DWord	Bit	Description		
0	31:24	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%; text-align: center;">RO</td> </tr> </table>	Access:	RO
	Access:	RO		
23:0	Performance Idle Hysteresis Direction <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%; text-align: center;">R/W</td> </tr> </table> <p>Idle intervals must be longer than this value to be considered idle.</p> <p>0 = 0 usec 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec pmcr_idle_hyst[23:0] FYI: 0 means disabled.</p>	Access:	R/W	
Access:	R/W			

GFX_FLSH_CNT

GFX_FLSH_CNT - GFX_FLSH_CNT		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	101008h	
Used to flush Gunit TLB		
DWord	Bit	Description
0	31:1	RESERVED
		Default Value: 00000000h
		Access: RO
		Reserved
0	0	GfxFlshCntl
		Default Value: 0b
		Access: WO
Access type of this register is WO. A write to this bit flushes the Gfx TLB in GUNIT. The data associated with the write is discarded and a read return all 0s.		

GFX Arbiter Client Priority Control

GFX_PRIO_CTRL - GFX Arbiter Client Priority Control			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x880A2D10		
Size (in bits):	32		
Address:	04A00h		
DWord	Bit	Description	
0	31:27	Read Rstrm Max Reject	
		Default Value:	10001b
		Access:	R/W
	26:21	Extra Bits	
		Default Value:	000000b
		Access:	R/W
	20:18	sol_gam_priority	
		Default Value:	010b
		Access:	R/W
	Client Priority Control Bits - Lowest Bit [18] is NOT Used.		
	17:15	veo_gam_priority	
		Default Value:	100b
Access:		R/W	
Client Priority Control Bits - Lowest Bit [15] is NOT Used.			
14:12	vfw_gam_priority		
	Default Value:	010b	
	Access:	R/W	
Client Priority Control Bits - Lowest Bit [12] is NOT Used.			
11:9	gapc_gam_c_priority		
	Default Value:	110b	
	Access:	R/W	
Client Priority Control Bits - Lowest Bit [9] is NOT Used.			
8:6	gapc_gam_z_priority		
	Default Value:	100b	
	Access:	R/W	
Client Priority Control Bits - Lowest Bit [6] is NOT Used.			

GFX_PRIO_CTRL - GFX Arbiter Client Priority Control		
	5:3	gapc_gam_l3_priority
		Default Value: 010b
	Access: R/W	
	Client Priority Control Bits - Lowest Bit [3] is NOT Used.	
	2:0	csrsvf_gam_priority
Default Value: 000b		
Access: R/W		
Client Priority Control Bits - Lowest Bit [0] is NOT Used.		

GFX Context Element Descriptor (High Part)

GFX_CTX_EDR_H - GFX Context Element Descriptor (High Part)						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04404h					
DWord	Bit	Description				
0	31:0	<p>GFX Context Element Descriptor (High Part)</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit[63:32] - Context ID: Context identification number assigned to separate this context from others. Context IDs need to be recycled in such a way that there cannot be two active contexts with the same ID. This is a unique identification number by which a context is identified and referenced.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GFX Context Element Descriptor (Low Part)

GFX_CTX_EDR_L - GFX Context Element Descriptor (Low Part)						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000009					
Size (in bits):	32					
Address:	04400h					
DWord	Bit	Description				
0	31:0	<p>GFX Context Element Descriptor (Low Part)</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000009h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit[31:12] - LRCA: Command Streamer Only.</p> <p>Bit[8] - Privileged Context / GGTT vs PPGTT mode: Differs in legacy vs advanced context modes: In Legacy Context: Defines the page tables to be used. This is how page walker comes to know PPGTT vs GGTT selection for the entire context. 0: Use Global GTT. 1: Use Per-Process GTT. In Advanced Context: Defines the privilege level for the context. 0: User mode context. 1: Supervisor mode context.</p> <p>Bit[5] - Deeper IA coherency Support: In Advanced Context: Defines the level of IA coherency. 0: IA coherency is provided at LLC level for all streams of GPU (i.e. Gen7.5 like mode). 1: IA coherency is provided at L3 level for EU data accesses of GPU.</p> <p>Bit[4] - A and D Support / 32 and 64b Address Support: Differs in legacy vs advanced context modes: In Legacy Context: Defines 32b vs 64b (48b canonical) addressing format: 0: 32b addressing format. 1: 64b (48b canonical) addressing format. In Advanced Context: Defines A and D bit support: 0: A and D bit management in page tables is NOT supported. 1: A and D bit management in page tables is supported.</p> <p>Bit[3] - Context Type: Legacy vs Advanced: Defines the context type 0: Advanced Context: Defines the rest of the advanced capabilities (i.e. OS page table support, fault models). Note that advanced context is not bounded to GPGPU. 1: Legacy Context: Defines the context as legacy mode which is similar to prior generations of Gen8.</p> <p>Note that: Bits [8:4] differs in functions when legacy vs advanced context modes are selected.</p>	Default Value:	00000009h	Access:	R/W
Default Value:	00000009h					
Access:	R/W					

GFX_CTX_EDR_L - GFX Context Element Descriptor (Low Part)

	<p>Bit[2] - FR: Command streamer specific.</p>
	<p>Bit[1] - Scheduling Mode: 1: Indicates execlist mode of scheduling. 0: Indicates Ring Buffer mode of scheduling.</p>
	<p>Bit[0] - Valid: Indicates that element descriptor is valid. If GAM is programmed with an invalid descriptor, it continues but flags an error.</p>

GFX Context Element Descriptor (Low Part)

GFX_CTX_EDR_L - GFX Context Element Descriptor (Low Part)						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000009					
Size (in bits):	32					
Address:	04400h					
DWord	Bit	Description				
0	31:0	<p>GFX Context Element Descriptor</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000009h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit[31:12] - LRCA: Command Streamer Only.</p> <p>Bit[8] - Privileged Context / GGTT vs PPGTT mode: Differs in legacy vs advanced context modes: In Legacy Context: Defines the page tables to be used. This is how page walker comes to know PPGTT vs GGTT selection for the entire context. 0: Use Global GTT. 1: Use Per-Process GTT. In Advanced Context: Defines the privilege level for the context. 0: User mode context. 1: Supervisor mode context.</p> <p>Bit[5] - Deeper IA coherency Support: In Advanced Context: Defines the level of IA coherency. 0: IA coherency is provided at LLC level for all streams of GPU (i.e. Gen7.5 like mode). 1: IA coherency is provided at L3 level for EU data accesses of GPU.</p> <p>Bit[4] - A and D Support / 32 and 64b Address Support: Differs in legacy vs advanced context modes: In Legacy Context: Defines 32b vs 64b (48b canonical) addressing format: 0: 32b addressing format. 1: 64b (48b canonical) addressing format. In Advanced Context: Defines A and D bit support: 0: A and D bit management in page tables is NOT supported. 1: A and D bit management in page tables is supported.</p> <p>Bit[3] - Context Type: Legacy vs Advanced: Defines the context type 0: Advanced Context: Defines the rest of the advanced capabilities (i.e. OS page table support, fault models). Note that advanced context is not bounded to GPGPU. 1: Legacy Context: Defines the context as legacy mode which is similar to prior generations of Gen8.</p> <p>Note that: Bits [8:4] differs in functions when legacy vs advanced context modes are selected.</p>	Default Value:	00000009h	Access:	R/W
Default Value:	00000009h					
Access:	R/W					

GFX_CTX_EDR_L - GFX Context Element Descriptor (Low Part)

	<p>Bit[2] - FR: Command streamer specific.</p>
	<p>Bit[1] - Scheduling Mode: 1: Indicates execlist mode of scheduling. 0: Indicates Ring Buffer mode of scheduling.</p>
	<p>Bit[0] - Valid: Indicates that element descriptor is valid. If GAM is programmed with an invalid descriptor, it continues but flags an error.</p>

GFX PDP0/PML4/PASID Descriptor (High Part)

GFX_CTX_PDP0_H - GFX PDP0/PML4/PASID Descriptor (High Part)						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0440Ch					
DWord	Bit	Description				
0	31:0	<p>GFX PDP0/PML4/PASID Descriptor (High Part)</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>PDP0/PML4/PASID: This register can contain three values which depend on the element descriptor definition. PASID[19:0]: Populated in the first 20bits of the register and selected when Advanced Context flag is set. PML4[38:12]: Pointer to base address of PML4 and selected when Legacy Context flag is set and 64b address support is selected. PDP0[38:12]: Pointer to one of the four page directory pointer (lowest) and defines the first 0-1GB of memory mapping. Note: This is a guest physical address.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GFX PDP0/PML4/PASID Descriptor (Low Part)

GFX_CTX_PDP0_L - GFX PDP0/PML4/PASID Descriptor (Low Part)						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04408h					
DWord	Bit	Description				
0	31:0	<p>GFX PDP0/PML4/PASID Descriptor (Low Part)</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>PDP0/PML4/PASID: This register can contain three values which depend on the element descriptor definition. PASID[19:0]: Populated in the first 20 bits of the register and selected when Advanced Context flag is set. PML4[38:12]: Pointer to base address of PML4 and selected when Legacy Context flag is set and 64b address support is selected. PDP0[38:12]: Pointer to one of the four page directory pointer (lowest) and defines the first 0-1GB of memory mapping. Note: This is a guest physical address.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GFX PDP1 Descriptor Register (High Part)

GFX_CTX_PDP1_H - GFX PDP1 Descriptor Register (High Part)						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04414h					
DWord	Bit	Description				
0	31:0	<p>GFX PDP1 Descriptor Register (High Part)</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Pointer to one of the four page directory pointer (lowest+1) and defines the first 1-2GB of memory mapping. Note: This is a guest physical address.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GFX PDP1 Descriptor Register (Low Part)

GFX_CTX_PDP1_L - GFX PDP1 Descriptor Register (Low Part)						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04410h					
DWord	Bit	Description				
0	31:0	<p>GFX PDP1 Descriptor Register (Low Part)</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Pointer to one of the four page directory pointer (lowest+1) and defines the first 1-2GB of memory mapping. Note: This is a guest physical address.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GFX PDP2 Descriptor Register (High Part)

GFX_CTX_PDP2_H - GFX PDP2 Descriptor Register (High Part)						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0441Ch					
DWord	Bit	Description				
0	31:0	<p>GFX PDP2 Descriptor Register (High Part)</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Pointer to one of the four page directory pointer (lowest+2) and defines the first 2-3GB of memory mapping. Note: This is a guest physical address.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GFX PDP2 Descriptor Register (Low Part)

GFX_CTX_PDP2_L - GFX PDP2 Descriptor Register (Low Part)						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04418h					
DWord	Bit	Description				
0	31:0	<p>GFX PDP2 Descriptor Register (Low Part)</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Pointer to one of the four page directory pointer (lowest+2) and defines the first 2-3GB of memory mapping. Note: This is a guest physical address.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GFX PDP3 Descriptor Register (High Part)

GFX_CTX_PDP3_H - GFX PDP3 Descriptor Register (High Part)						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04424h					
DWord	Bit	Description				
0	31:0	<p>GFX PDP3 Descriptor Register (High Part)</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Pointer to one of the four page directory pointer (lowest+3) and defines the first 3-4GB of memory mapping. Note: This is a guest physical address.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GFX PDP3 Descriptor Register (Low Part)

GFX_CTX_PDP3_L - GFX PDP3 Descriptor Register (Low Part)						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04420h					
DWord	Bit	Description				
0	31:0	<p>GFX PDP3 Descriptor Register (Low Part)</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Pointer to one of the four page directory pointer (lowest+3) and defines the first 3-4GB of memory mapping. Note: This is a guest physical address.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GGC

GGC - GGC			
Register Space:	PCI: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000028		
Size (in bits):	32		
Address:	00050h		
GMCH Graphics Control Register.			
DWord	Bit	Description	
0	31:15	RESERVED	
		Default Value:	00000h
		Access:	RO
		Reserved	
14	14	VAMEN	
		Default Value:	0b
		Access:	R/W Lock
Enables the use of the iGFX engines for Versatile Acceleration. 1 - iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 048000h. 0 - iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h.			
13:10	13:10	RESERVED	
		Default Value:	0h
		Access:	RO
Reserved			
9:8	9:8	GGMS	
		Default Value:	00b
		Access:	R/W Lock
GTT Graphics Memory Size (GGMS): This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware will derive the base of GSM from DSM only using the GSM size programmed in the register. Hardware functionality in case of programming this value to Reserved is not guaranteed. 0h:No Preallocated Memory 1h: 2MB of Preallocated Memory 2h: 4MB of Preallocated Memory 3h: 8MB of Preallocated Memory			

GGC - GGC

7:3	GMS	
	Default Value:	00101b
	Access:	R/W Lock
<p>Graphics Mode Select(GMS): This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled. BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0.</p>		
<p>0h = 0MB 1h = 32MB 2h = 64MB 3h = 96MB 4h = 128MB 5h = 160MB 6h = 192MB 7h = 224MB 8h = 256MB 9h = 288MB Ah = 320MB Bh = 352MB Ch = 384MB Dh = 416MB Eh = 448MB Fh = 480MB 10h = 512MB 11h = 8MB 12h = 12MB 13h = 16MB 14h = 20MB 15h = 24MB 16h = 28MB 17h = 36MB 18h = 40MB 19h = 44MB 1Ah = 48MB 1Bh = 52MB 1Ch = 56MB 1Dh = 60MB 1Eh = Reserved 1Fh = Reserved 20h:1024MB (Not supported for CHV, BSW)</p>		

GGC - GGC

		<p>..... 30h:1536MB (Not supported for CHV, BSW) 40h:2048MB (Not supported for CHV, BSW) 80h:4096MB (Not supported for CHV, BSW) 81h - FF:Reserved Other = Reserved When GMS != '0 (and VD=0): Address[31:0] is compared with VGA memory range. (The VGA memory range is A_0000h to B_FFFh.). If there is a match and MSE = 1 and MEMRD or MEMWR, the access will route as a Rmdwvgamemen_cr cycle on the RMBus. If the RMBus returns a hit the GVD will select the command. As well, when 0 the GVD will check if scldown3_address[15:0] is one of the VGA IO register range. (The VGA IO range is 03B0h - 03BBh and 03C0h - 03DFh.) If there is a match and IOSE = 1 and the SCL command is either an IORD or IOWR, the GVD will initiate a (VGA) register cycle on the RMBus. If the RMBus returns a hit the GVD will select the command When GMS == '0 : No address compare will occur against VGA memory range or the VGA IO register range. Also, CC[15:8] is changed to 8'h80 from 8'h00</p>	
	2	RESERVED	
		Default Value:	0b
		Access:	RO
		Reserved	
	1	VGA_DISABLE	
		Default Value:	0b
		Access:	R/W Lock
		<p>VGA Disable (VD): 0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub- Class Code field within Device 2 function 0 Class Code register is 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field pre-allocates no memory. This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override (CAPID0[38] = 1) or via a register (DEVEN[3] = 0).</p>	
	0	GGCLCK	
		Default Value:	0b
		Access:	R/W Lock
		When set to 1b, this will lock all the bits in this register.	

Global Clear Value Register 0

GLOBAL_CLEAR_VALUE_0 - Global Clear Value Register 0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	07700h	
<p>This register is to be used to program bits 31:0 of the Global clear value to be used for non MSRT render targets. This value will be used by pixel backend hardware in place of the 0/1 clear values, if the "Use Global Clear Value" bit is set.</p>		
DWord	Bit	Description
0	31:0	<p>Global Clear Value 0</p> <p>Contains bits 31:0 of the global clear value. Clear value will be in native RT format. Clear Value for 8/16/32 bpp RTs will be contained in this format. For the rest it will contain bits 31:0.</p>

Global Clear Value Register 1

GLOBAL_CLEAR_VALUE_1 - Global Clear Value Register 1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	07704h	
<p>This register is to be used to program bits 63:32 of the Global clear value to be used for non MSRT render targets. This value will be used by pixel backend hardware in place of the 0/1 clear values, if the "Use Global Clear Value" bit is set.</p>		
DWord	Bit	Description
0	31:0	<p>Global Clear Value 1 Contains bits 63:32 of the global clear value. Clear value will be in native RT format. This field will contain bits 63:32 of the clear value of 64 bpp and 128 bpp RTs.</p>

Global Clear Value Register 2

GLOBAL_CLEAR_VALUE_2 - Global Clear Value Register 2		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	07708h	
<p>This register is to be used to program bits 95:64 of the Global clear value to be used for non MSRT render targets. This value will be used by pixel backend hardware in place of the 0/1 clear values, if the "Use Global Clear Value" bit is set.</p>		
DWord	Bit	Description
0	31:0	<p>Global Clear Value 2 Contains bits 95:64 of the global clear value. Clear value will be in native RT format. Clear value will be in native RT format. This field will contain bits 95:64 of the clear value for 128 bpp RTs.</p>

Global Clear Value Register 3

GLOBAL_CLEAR_VALUE_3 - Global Clear Value Register 3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	0770Ch	
<p>This register is to be used to program bits 127:96 of the Global clear value to be used for non MSRT render targets. This value will be used by pixel backend hardware in place of the 0/1 clear values, if the "Use Global Clear Value" bit is set.</p>		
DWord	Bit	Description
0	31:0	<p>Global Clear Value 3 Contains bits 127:96 of the global clear value. Clear value will be in native RT format. This field will contain bits 127:96 of the clear value for 128 bpp RTs.</p>

Global Invalidation Register

GLBLINVL - Global Invalidation Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B404h	
DWord	Bit	Description
0	31:3	Reserved
		Access: RO Reserved.
	2	Cross sync read disable
		Access: R/W Ipconf_crs_sync_dis: Cross Sync Read Disable (CSRD). Cross Sync Read Disable (CSRD): Cross Sync Read Disable: upon a SYNC from HDC, follow with a write to cross SYNC Push and read to the same address. When set read is disabled.
1	Disables hashing function	
	Access: R/W Disables hashing function (DISHHF): Disables hashing function to generate bank_id[1:0] for L3\$ bank accessing, and forces the use of address[7:6] for bank_id[1:0].0: (default) Hash function enabled to generate L3\$ bank IDs. 1: L3\$ address[7:6] used as L3\$ bank IDs. Ipconf_csr_l3bankidhashdis. (This bit needs to set corresponding bit Incf_csr_l3bankidhashdis in LNCF.)	
0		Reserved

Global System Interrupt Routine

EU_GLOBAL_SIP - Global System Interrupt Routine							
Register Space:	MMIO: 0/2/0						
Project:	CHV, BSW						
Source:	PRM						
Default Value:	0x00000000						
Access:	R/W						
Size (in bits):	32						
Address:	0E42Ch						
DWord	Bit	Description					
0	31:3	Global SIP Format: GraphicsAddress[31:3] Specifies the base address for System Interrupt Routine that over-rides the SIP set by the state (STATE_SIP).					
	2:1	Reserved Format: MBZ					
	0	Global SIP Enable The bit specifies if the System Routine starts from the Global SIP provided by the DW OR the SIP provided by the state (STATE_SIP) <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>SIP used is from STATE_EIP</td> </tr> <tr> <td>1</td> <td>SIP used is from MMIO register</td> </tr> </tbody> </table>	Value	Name	0	SIP used is from STATE_EIP	1
Value	Name						
0	SIP used is from STATE_EIP						
1	SIP used is from MMIO register						

GMADR_LSB

GMADR_LSB - GMADR_LSB					
Register Space:	PCI: 0/2/0				
Project:	CHV, BSW				
Source:	PRM				
Default Value:	0x0000000C				
Size (in bits):	32				
Address:	00018h				
<p>Gfx Aperture location. GMADR is a Prefetchable range in order to apply USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining. Accesses to this range will be translated to DRAM Physical memory addresses. Fence registers may be used to sub-divide this range and allow tiled surfaces (determined by fence registers). The supported sizes are determined by the MSAC register.</p>					
DWord	Bit	Description			
0	31	ADMSK4096			
		<table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>4096MB Address Mask (ADMSK4096): Locked with MSAC.APSZ[4]. See MSAC (Dev2, Func 0, offset 62h) for details.</p>	Default Value:	0b	Access:
	Default Value:	0b			
	Access:	R/W Lock			
30	ADMSK2048				
	<table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>2048MB Address Mask (ADMSK2048): Locked with MSAC.APSZ[3]. See MSAC (Dev2, Func 0, offset 62h) for details.</p>	Default Value:	0b	Access:	R/W Lock
Default Value:	0b				
Access:	R/W Lock				
29	ADMSK1024				
	<table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>1024MB Address Mask (ADMSK1024): Locked with MSAC.APSZ[2]. See MSAC (Dev2, Func 0, offset 62h) for details.</p>	Default Value:	0b	Access:	R/W Lock
Default Value:	0b				
Access:	R/W Lock				
28	ADMSK512				
	<table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>512MB Address Mask (ADMSK512): Locked with MSAC.APSZ[1]. See MSAC (Dev2, Func 0, offset 62h) for details.</p>	Default Value:	0b	Access:	R/W Lock
Default Value:	0b				
Access:	R/W Lock				

GMADR_LSB - GMADR_LSB		
27	ADMSK256	
	Default Value: 0b	
	Access: R/W Lock	
	256MB Address Mask (ADMSK256): Locked with MSAC.APSZ[0]. See MSAC (Dev2, Func 0, offset 62h) for details.	
	Reserved	
26:4	Default Value: 000000h	
	Access: RO	
	Address Mask (ADM): Hardwired to 0s to indicate at least 128MB address range.	
3	PREFMEM	
	Default Value: 1b	
	Access: RO	
Prefetchable Memory (PREFMEM): Hardwired to 1 to enable prefetching.		
2:1	MEMTYP	
	Default Value: 10b	
	Access: RO	
Memory Type (MEMTYP): 00: To indicate 32 bit base address 01: Reserved 10: To indicate 64 bit base address 11: Reserved		
0	Reserved	
	Default Value: 0b	
	Access: RO	
Memory/IO Space (MIOS): Hardwired to 0 to indicate memory space.		

GMADR_MSB

GMADR_MSB - GMADR_MSB			
Register Space:	PCI: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0001Ch		
<p>Gfx Aperture location. GMADR is a Prefetchable range in order to apply USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining. Accesses to this range will be translated to DRAM Physical memory addresses. Fence registers may be used to sub-divide this range and allow tiled surfaces (determined by fence registers). The supported sizes are determined by the MSAC register.</p>			
DWord	Bit	Description	
0	31:4	MBA_MSB28	
		Default Value:	0000000h
		Access:	R/W
	Description		Project
	Set by the OS, these bits correspond to address signals [63:39]		
	Made them spare RW bits.		CHV, BSW
	3:0	MBA	
		Default Value:	0h
		Access:	R/W
Memory Base Address (MBA)Set by the OS, these bits correspond to address signals [35:32]			

GMBC Message Register

GMBCMSG - GMBC Message Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	08500h			
GMBC Message Register				
DWord	Bit	Description		
0	31:12	<p>RSVD</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved</p>	Access:	RO
	Access:	RO		
	11	<p>Context Restore Message</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Context Restore Message 1 = Context Restore Message From CS 0 = Not a Message, GMBC clears when sending ACK to CS.</p>	Access:	R/W
	Access:	R/W		
	10	<p>MBC BUSY ACK Message</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>1 = Busy Ack message from GPMG 0 = IDLE (non-busy) Ack message from GPMG</p>	Access:	R/W
	Access:	R/W		
	9:7	<p>RSVD</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved</p>	Access:	RO
	Access:	RO		
6	<p>Block Message</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Block Message from GPMG 1 = Block Outbound GAM Traffic and wait for outstanding GAM write requests to be GO'd and reads to return 0 = Unblock Outbound GAM traffic</p>	Access:	R/W	
Access:	R/W			
5	<p>RSVD</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved</p>	Access:	RO	
Access:	RO			
4	<p>Arbitration request/release ACK</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Access:	R/W	
Access:	R/W			

GMBCMSG - GMBC Message Register			
	Global Arb request ACK message: 1 = GPMG ACK of GMBC Global Arb Update Request. 0 = GPMG ACK of GMBC Global Arb Release Request.		
3	RSVD <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%;">RO</td> </tr> </table> Reserved	Access:	RO
Access:	RO		
2	Fuse Fetch Message <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%;">R/W</td> </tr> </table> Fuse Fetch message: written to 1 by GPMG to indicate GMBC should perform a fuse fetch. Cleared by GMBC when done with the fuse fetch.	Access:	R/W
Access:	R/W		
1:0	RSVD <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%;">RO</td> </tr> </table> Reserved	Access:	RO
Access:	RO		

GO Messaging Register for GAMunit

MSG_GO_GAM - GO Messaging Register for GAMunit		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	16	
Address:	08028h	
<p>Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.</p> <p>GA* Response to Allow Graphics Cycles to Read/Write from Memory</p> <p>1'b0 : No gfx cycles allowed to memory <default></p> <p>1'b1 : Allow gfx cycles to memory</p> <p>gpm currently only ever sends the same GO request for all agents; either all is go=0, or all is go=1.</p>		
DWord	Bit	Description
0	15:7	Reserved Access: RO
	6	GA* Response to Allow Wi-Di Graphics Cycles to Read/Write from Memory Access: R/W [6] Controls Wi-Di Cycles (winunit)
	5	Reserved
	4	GA* Response to Allow Blitter Graphics Cycles to Read/Write from Memory Access: R/W [4] Controls Blitter Cycles (bcsunit)
	3	GA* Response to Allow VEBox Graphics Cycles to Read/Write from Memory Access: R/W [3] Controls VEBox Cycles (vecsunit)
	2	GA* Response to Allow Media1 Graphics Cycles to Read/Write from Memory Access: R/W [2] Controls Media1 Cycles (vcs1unit)
	1	GA* Response to Allow Media0 Graphics Cycles to Read/Write from Memory Access: R/W [1] Controls Media0 Cycles (vcs0unit)

MSG_GO_GAM - GO Messaging Register for GAMunit

	0	GA* Response to Allow Render Graphics Cycles to Read/Write from Memory	
		Access:	R/W
		[0] Controls Render Cycles (csunit)	

Go Protocol GAM Request

GO_GAM_REQ - Go Protocol GAM Request			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000 CHV, BSW		
Size (in bits):	32		
Address:	040D0h		
DWord	Bit	Description	
0	31:16	Mask Bits	
		Default Value:	0000h
		Access:	RO
		Reserved.	
	15	GO_PROTOCOL_GAM_REQUEST15	
		Default Value:	0b
		Project:	CHV, BSW
		Access:	R/W
	Go Protocol Request Reasons: 1'b0: Engine will NOT be resetting. 1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset). Preparation for FLR (device) reset (cdevrst_b).		
	14	GO_PROTOCOL_GAM_REQUEST14	
		Default Value:	0b
		Project:	CHV, BSW
Access:		R/W	
Go Protocol Request Reasons: 1'b0: Engine will NOT be resetting. 1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset). Preparation for Media1 reset (vcs1unit).			
13	GO_PROTOCOL_GAM_REQUEST13		
	Default Value:	0b	
	Project:	CHV, BSW	
	Access:	R/W	
Go Protocol Request Reasons: 1'b0: Engine will NOT be resetting. 1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset). Preparation for Wi-Di reset (winunit).			

GO_GAM_REQ - Go Protocol GAM Request

12	GO_PROTOCOL_GAM_REQUEST12	Default Value:	0b
		Project:	CHV, BSW
		Access:	R/W
	Go Protocol Request Reasons: 1'b0: Engine will NOT be resetting. 1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset).		
11	GO_PROTOCOL_GAM_REQUEST11	Default Value:	0b
		Project:	CHV, BSW
		Access:	R/W
	Go Protocol Request Reasons: 1'b0: Engine will NOT be resetting. 1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset). Preparation for Blitter reset (bcsunit).		
10	GO_PROTOCOL_GAM_REQUEST10	Default Value:	0b
		Project:	CHV, BSW
		Access:	R/W
	Go Protocol Request Reasons: 1'b0: Engine will NOT be resetting. 1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset). Preparation for VEBox reset (vecsunit).		
9	GO_PROTOCOL_GAM_REQUEST9	Default Value:	0b
		Project:	CHV, BSW
		Access:	R/W
	Go Protocol Request Reasons: 1'b0: Engine will NOT be resetting. 1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset). Preparation for Media0 reset (vcs0unit).		
8	GO_PROTOCOL_GAM_REQUEST8	Default Value:	0b
		Project:	CHV, BSW
		Access:	R/W
	Go Protocol Request Reasons: 1'b0: Engine will NOT be resetting. 1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset). Preparation for Render reset (csunit).		

GO_GAM_REQ - Go Protocol GAM Request

7	Reserved	
6	GO_PROTOCOL_GAM_REQUEST6	
	Default Value:	0b
	Access:	R/W
	<p>GPM to GAM Go Protocol Request. 0: No graphic cycles allowed to memory (default). 1: Allow graphic cycles to memory. Controls Wi-Di Cycles (winunit). GPM currently only ever sends the same GO request for all agents; either all is go=0, or all is go=1.</p>	
5	Reserved	
4	GO_PROTOCOL_GAM_REQUEST4	
	Default Value:	0b
	Access:	R/W
	<p>GPM to GAM Go Protocol Request. 0: No graphic cycles allowed to memory (default). 1: Allow graphic cycles to memory. Controls Blitter Cycles (bcsunit). GPM currently only ever sends the same GO request for all agents; either all is go=0, or all is go=1.</p>	
3	GO_PROTOCOL_GAM_REQUEST3	
	Default Value:	0b
	Access:	R/W
	<p>GPM to GAM Go Protocol Request. 0: No graphic cycles allowed to memory (default). 1: Allow graphic cycles to memory. Controls VEBox Cycles (vecsunit). GPM currently only ever sends the same GO request for all agents; either all is go=0, or all is go=1.</p>	
2	GO_PROTOCOL_GAM_REQUEST2	
	Default Value:	0b
	Access:	R/W
	<p>GPM to GAM Go Protocol Request. 0: No graphic cycles allowed to memory (default). 1: Allow graphic cycles to memory. Controls Media1 Cycles (vcs1unit). GPM currently only ever sends the same GO request for all agents; either all is go=0, or all is go=1.</p>	
1	GO_PROTOCOL_GAM_REQUEST1	
	Default Value:	0b
	Access:	R/W

GO_GAM_REQ - Go Protocol GAM Request

	<p>GPM to GAM Go Protocol Request. 0: No graphic cycles allowed to memory (default). 1: Allow graphic cycles to memory. Controls Media0 Cycles (vcs0unit). GPM currently only ever sends the same GO request for all agents; either all is go=0, or all is go=1.</p>					
0	<p>GO_PROTOCOL_GAM_REQUEST0</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>GPM to GAM Go Protocol Request. 0: No graphic cycles allowed to memory (default). 1: Allow graphic cycles to memory. Controls Render Cycles (csunit). GPM currently only ever sends the same GO request for all agents; either all is go=0, or all is go=1.</p>		Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					

GPA to HPA Translation Request

GPA2HPAR - GPA to HPA Translation Request		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0420Ch	
DWord	Bit	Description
0	31:16	Mask Bits
		Default Value: 0000h
	Access: RO	
	Mask Bits act as Write Enables for the bits[15:0] of this register.	
	15	GPA to HPA Translation Request 15
		Default Value: 0b
Access: R/W		
For Future Use. This bit is self clear.		
14	GPA to HPA Translation Request 14	
	Default Value: 0b	
Access: R/W		
For Future Use. This bit is self clear.		
13	GPA to HPA Translation Request 13	
	Default Value: 0b	
Access: R/W		
For Future Use. This bit is self clear.		
12	GPA to HPA Translation Request 12	
	Default Value: 0b	
Access: R/W		
For Future Use. This bit is self clear.		
11	GPA to HPA Translation Request 11	
	Default Value: 0b	
Access: R/W		
For Future Use.		

GPA2HPAR - GPA to HPA Translation Request

	This bit is self clear.	
10	GPA to HPA Translation Request 10	
	Default Value:	0b
	Access:	R/W
For Future Use. This bit is self clear.		
9	GPA to HPA Translation Request 9	
	Default Value:	0b
	Access:	R/W
For Future Use. This bit is self clear.		
8	GPA to HPA Translation Request 8	
	Default Value:	0b
	Access:	R/W
For Future Use. This bit is self clear.		
7	GPA to HPA Translation Request 7	
	Default Value:	0b
	Access:	R/W
For Future Use. This bit is self clear.		
6	GPA to HPA Translation Request 6	
	Default Value:	0b
	Access:	R/W
For Future Use. This bit is self clear.		
5	GPA to HPA Translation Request 5	
	Default Value:	0b
	Access:	R/W
For Future Use. This bit is self clear.		
4	GPA to HPA Translation Request 4	
	Default Value:	0b
	Access:	R/W
For Future Use. This bit is self clear.		
3	GPA to HPA Translation Request 3	
	Default Value:	0b
	Access:	R/W

GPA2HPAR - GPA to HPA Translation Request

		For Future Use. This bit is self clear.	
	2	GPA to HPA Translation Request 2	
		Default Value:	0b
	Access:	R/W	
	Bit[2]: A request for GPA to HPA translation. Note that GPA register should have been written prior to sending the message for the translation. Mask bit[18] needs to be enabled to program the register. This bit is self clear.		
	1	GPA to HPA Translation Request 1	
		Default Value:	0b
		Access:	R/W
	For Future Use. This bit is self clear.		
	0	GPA to HPA Translation Request 0	
		Default Value:	0b
Access:		R/W	
For Future Use. This bit is self clear.			

GPA value for GPA to HPA Translation

GPA2HPAV - GPA value for GPA to HPA Translation						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04210h					
DWord	Bit	Description				
0	31:0	<p>GPA value for GPA to HPA Translation</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>The GPA value of the page that requires the GPA=>HPA translation bits[39:12] map to [28:1] of the register.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GPGPU Context Restore Request To TDL

GPGPU_CTX_RESTORE - GPGPU Context Restore Request To TDL	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	WO
Size (in bits):	32
Address:	0E4CCh
Name:	GPGPU Context Restore Request To TDL Slice 0 SubSlice 0
ShortName:	GPGPU_CTX_RESTORE_S0_SS0
Valid Projects:	CHV, BSW
Address:	0E5CCh
Name:	GPGPU Context Restore Request To TDL Slice 0 SubSlice 1
ShortName:	GPGPU_CTX_RESTORE_S0_SS1
Valid Projects:	CHV, BSW
Address:	0E6CCh
Name:	GPGPU Context Restore Request To TDL Slice 0 SubSlice 2
ShortName:	GPGPU_CTX_RESTORE_S0_SS2
Valid Projects:	CHV, BSW
Address:	0E4DCh
Name:	GPGPU Context Restore Request To TDL Slice 1 SubSlice 0
ShortName:	GPGPU_CTX_RESTORE_S1_SS0
Valid Projects:	CHV, BSW
Address:	0E5DCh
Name:	GPGPU Context Restore Request To TDL Slice 1 SubSlice 1
ShortName:	GPGPU_CTX_RESTORE_S1_SS1
Valid Projects:	CHV, BSW
Address:	0E6DCh
Name:	GPGPU Context Restore Request To TDL Slice 1 SubSlice 2
ShortName:	GPGPU_CTX_RESTORE_S1_SS2
Valid Projects:	CHV, BSW
Address:	0E4ECh
Name:	GPGPU Context Restore Request To TDL Slice 2 SubSlice 0
ShortName:	GPGPU_CTX_RESTORE_S2_SS0
Valid Projects:	CHV, BSW

GPGPU_CTX_RESTORE - GPGPU Context Restore Request To TDL

Address: 0E5ECh
 Name: GPGPU Context Restore Request To TDL Slice 2 SubSlice 1
 ShortName: GPGPU_CTX_RESTORE_S2_SS1
 Valid Projects: CHV, BSW

Address: 0E6ECh
 Name: GPGPU Context Restore Request To TDL Slice 2 SubSlice 2
 ShortName: GPGPU_CTX_RESTORE_S2_SS2
 Valid Projects: CHV, BSW

DWord	Bit	Description				
0	31:0	<table border="1" style="width: 100%;"> <tr> <td colspan="2">Reserved</td> </tr> <tr> <td style="width: 70%;">Format:</td> <td style="text-align: center;">MBZ</td> </tr> </table>	Reserved		Format:	MBZ
Reserved						
Format:	MBZ					

GPGPU Context Save Request To TDL

GPGPU_CTX_SAVE - GPGPU Context Save Request To TDL		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	WO	
Size (in bits):	32	
Address:	0E4D8h	
Valid Projects:	CHV, BSW	
DWord	Bit	Description
0	31:0	Reserved
		Format: MBZ

GPGPU Dispatch Dimension X

GPGPU_DISPATCHDIMX - GPGPU Dispatch Dimension X												
Register Space:	MMIO: 0/2/0											
Project:	CHV, BSW											
Source:	RenderCS											
Default Value:	0x00000000											
Access:	R/W											
Size (in bits):	32											
Address:	02500h											
DWord	Bit	Description										
0	31:0	<p>Dispatch Dimension X</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td colspan="2">The number of thread groups to be dispatched in the X dimension (max x + 1).</td> </tr> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> <tr> <td>0, FFFFFFFFh</td> <td></td> <td>CHV, BSW</td> </tr> </table>	Format:	U32	The number of thread groups to be dispatched in the X dimension (max x + 1).		Value	Name	Project	0, FFFFFFFFh		CHV, BSW
Format:	U32											
The number of thread groups to be dispatched in the X dimension (max x + 1).												
Value	Name	Project										
0, FFFFFFFFh		CHV, BSW										

GPGPU Dispatch Dimension Y

GPGPU_DISPATCHDIMY - GPGPU Dispatch Dimension Y												
Register Space:	MMIO: 0/2/0											
Project:	CHV, BSW											
Source:	RenderCS											
Default Value:	0x00000000											
Access:	R/W											
Size (in bits):	32											
Address:	02504h											
DWord	Bit	Description										
0	31:0	<p>Dispatch Dimension Y</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td colspan="2">The number of thread groups to be dispatched in the Y dimension (max y + 1)</td> </tr> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> <tr> <td>0, FFFFFFFFh</td> <td></td> <td>CHV, BSW</td> </tr> </table>	Format:	U32	The number of thread groups to be dispatched in the Y dimension (max y + 1)		Value	Name	Project	0, FFFFFFFFh		CHV, BSW
Format:	U32											
The number of thread groups to be dispatched in the Y dimension (max y + 1)												
Value	Name	Project										
0, FFFFFFFFh		CHV, BSW										

GPGPU Dispatch Dimension Z

GPGPU_DISPATCHDIMZ - GPGPU Dispatch Dimension Z												
Register Space:	MMIO: 0/2/0											
Project:	CHV, BSW											
Source:	RenderCS											
Default Value:	0x00000000											
Access:	R/W											
Size (in bits):	32											
Address:	02508h											
DWord	Bit	Description										
0	31:0	<p>Dispatch Dimension Z</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td colspan="2">The number of thread groups to be dispatched in the Zdimension (max Z + 1)</td> </tr> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> <tr> <td>0, FFFFFFFFh</td> <td></td> <td>CHV, BSW</td> </tr> </table>	Format:	U32	The number of thread groups to be dispatched in the Zdimension (max Z + 1)		Value	Name	Project	0, FFFFFFFFh		CHV, BSW
Format:	U32											
The number of thread groups to be dispatched in the Zdimension (max Z + 1)												
Value	Name	Project										
0, FFFFFFFFh		CHV, BSW										

GPU_Ticks_Counter

GPU_TICKS - GPU_Ticks_Counter				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	02910h			
Valid Projects:	CHV, BSW			
Reading this register returns the live value of the GPU ticks counter that is sampled and included in the performance counter report header.				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="text-align: center;">U32</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the GPU tick counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32
Format:	U32			

Graphics Device Reset Control

GDRST - Graphics Device Reset Control				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0941Ch			
Graphics Device Reset Control Registers				
DWord	Bit	Description		
0	31:7	Reserved		
		Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td style="width: 50px;">RO</td></tr></table> Reserved		RO
		RO		
	6	Reserved: MBZ		
	5	Reserved		
	4	4	Initiate Graphics Vebox Soft Reset	
			Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td style="width: 50px;">R/W Set</td></tr></table> Graphics VEbox Soft-Reset Control: '1' : Initiate a graphics Vebox domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.	
			R/W Set	
3	Initiate Graphics Blitter Soft Reset			
2	3	Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td style="width: 50px;">R/W Set</td></tr></table> Graphics Blitter Soft-Reset Control: '1' : Initiate a graphics blitter domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.		R/W Set
			R/W Set	
2	2	Initiate Graphics Media Soft Reset		
		Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td style="width: 50px;">R/W Set</td></tr></table> Graphics Media Soft-Reset Control: '1' : Initiate a graphics media 0 domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit.		R/W Set
	R/W Set			

GDRST - Graphics Device Reset Control			
	Note: This is a non-posted register.		
1	<p>Initiate Graphics Render Soft Reset</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Access:</td> <td style="width: 50%;">R/W Set</td> </tr> </table> <p>Graphics Render Soft-Reset Control: '1' : Initiate a graphics render domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.</p>	Access:	R/W Set
Access:	R/W Set		
0	<p>Initiate Graphics Full Soft Reset</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Access:</td> <td style="width: 50%;">R/W Set</td> </tr> </table> <p>Graphics Full Soft-Reset Control: '1' : Initiate a full graphics reset (i.e., graphics render, media, and blitter reset). - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.</p>	Access:	R/W Set
Access:	R/W Set		

Graphics Mode Register

GFX_MODE - Graphics Mode Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000 [CHV:B, CHV:C, CHV:K] 0x00000800 [CHV:A]	
Size (in bits):	32	
Trusted Type:	1	
Address:	0229Ch	
Valid Projects:	CHV, BSW	
Address:	1229Ch-1229Fh	
Name:	Graphics Mode Register	
ShortName:	GFX_MODE_VCSUNIT0	
Address:	1A29Ch-1A29Fh	
Name:	Graphics Mode Register	
ShortName:	GFX_MODE_VECSUNIT	
Address:	1C29Ch-1C29Fh	
Name:	Graphics Mode Register	
ShortName:	GFX_MODE_VCSUNIT1	
Address:	2229Ch-2229Fh	
Name:	Graphics Mode Register	
ShortName:	GFX_MODE_BCSUNIT	
Description		
This register contains a control bit for the new execlist and 2-level PPGTT functions.		
DefaultValue = 00002800h		
DWord	Bit	Description
0	31:16	Mask Bits
		<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>Mask[15:0]</td> </tr> </table> <p>Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)</p>
Format:	Mask[15:0]	
15		Execlist Enable
		<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Mask:</td> <td>MMIO#31</td> </tr> </table> <p>When set, software can utilize the execlist registers to load a context into hardware. MI_SET_CONTEXT and MI_ARB_CHECK commands will be converted to NOOP if parsed. When this bit is clear, the Execlist mechanism cannot be used. The context must be loaded via MI_SET_CONTEXT and the ring must be loaded via MMIO access.</p>
Mask:	MMIO#31	

GFX_MODE - Graphics Mode Register

Programming Notes														
<p>This bit is <i>not</i> intended to be changed dynamically. Changing the value of this bit while rendering is in progress will have UNDEFINED results. This bit should be changed only <u>after a full reset</u> and <u>before</u> submitting <i>any</i> commands to the device.</p>														
14	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table>	Project:	CHV, BSW											
Project:	CHV, BSW													
13	<p>Flush TLB invalidation Mode</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>This field controls the invalidation if the TLB cache inside the hardware. When enabled this bit limits the invalidation of the TLB only to batch buffer boundaries, to pipe_control commands which have the TLB invalidation bit set and sync flushes. If disabled, the TLB caches are flushed for every full flush of the pipeline.</p>	Project:	CHV, BSW	Format:	U1									
Project:	CHV, BSW													
Format:	U1													
12	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ									
Project:	All													
Format:	MBZ													
11	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ									
Project:	CHV, BSW													
Format:	MBZ													
11	<p>Replay Mode</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U1 Context Switch Granularity</td> </tr> </table> <p>This field controls the granularity of the replay mechanism when coming back into a previously preempted context.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 20%;">Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1h</td> <td>Object Level Preemption [Default]</td> <td>Object Level. Preemption is done on an Object Level Boundary in VF. Objects send down by VF are completely rendered. Pipeline is flushed before switching to the next context. On resubmission of the context VF starts parsing form the object where it got preempted last time.</td> </tr> <tr> <td>0h</td> <td>mid-cmdbuffer preemption</td> <td>Drawcall Level. Pipeline is flushed before switching to the next context. Commands parsed are committed to completing before a context switch.</td> </tr> </tbody> </table> <p style="text-align: center;">Programming Notes</p> <p>A fixed function pipe flush is required before modifying this field.</p> <p>The replay mode must be set to 0.</p>	Project:	CHV, BSW	Format:	U1 Context Switch Granularity	Value	Name	Description	1h	Object Level Preemption [Default]	Object Level. Preemption is done on an Object Level Boundary in VF. Objects send down by VF are completely rendered. Pipeline is flushed before switching to the next context. On resubmission of the context VF starts parsing form the object where it got preempted last time.	0h	mid-cmdbuffer preemption	Drawcall Level. Pipeline is flushed before switching to the next context. Commands parsed are committed to completing before a context switch.
Project:	CHV, BSW													
Format:	U1 Context Switch Granularity													
Value	Name	Description												
1h	Object Level Preemption [Default]	Object Level. Preemption is done on an Object Level Boundary in VF. Objects send down by VF are completely rendered. Pipeline is flushed before switching to the next context. On resubmission of the context VF starts parsing form the object where it got preempted last time.												
0h	mid-cmdbuffer preemption	Drawcall Level. Pipeline is flushed before switching to the next context. Commands parsed are committed to completing before a context switch.												
10	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> </table>	Project:	All											
Project:	All													

GFX_MODE - Graphics Mode Register

	Format:	MBZ
9	Per-Process GTT Enable	
	Project:	CHV, BSW
	Format:	Enabled
	Per-Process GTT Enable	
	Value	Name
	Description	
	0h	PPGTT Disable [Default]
		When clear, the Global GTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.
	1h	PPGTT Enable
		When set, the PPGTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.
	Programming Notes	
	<p>This bit is used for enabling PPGTT access in Ring Buffer mode of scheduling. Privilege field in context descriptor states the same in Execlist Mode of scheduling. This field should be set before programming PDP0/1/2/3 registers in order to set the PPGTT translation of memory access.</p> <p>Programming this bit doesn't enable or disable the PPGTT translation of memory access immediately; the change comes in to affect only when the Page Directory registers are programmed. Programming this bit must be followed by programming Page Directory Registers in order to enable or disable the PPGTT translation of memory access.</p>	
8	Reserved	
	Project:	CHV, BSW
7	64Bit Virtual Addressing Enable	
	Project:	CHV, BSW
	Format:	Enabled
	Per-Process GTT Enable	
	Value	Name
	Description	
	0h	64Bit Virtual Addressing Disable [Default]
		When clear indicates GFX operating in 32bit Virtual Addressing for PPGTT based memory access.
	Programming Notes	
	<p>This bit is only valid when PPGTT is enabled in ring buffer mode of scheduling. Context Descriptor has a similar bit to control 64bit virtual addressing in execlist mode of scheduling. Whether this field is set or clear virtual addresses translated through GGTT are always 32Bit. This field should be programmed before enabling PPGTT access. When this field is not set or for GGTT virtual addresses, Graphics Address [47:32] field of any commands or register exercised by SW should be programmed to 0x0.</p> <p>64 Bit Virtual Addressing is not supported on CHV, BSW and must not be set.</p>	

GFX_MODE - Graphics Mode Register		
6:5	Reserved	
	Project: CHV, BSW	
	Reserved	
	Project: CHV, BSW	
	Reserved	
	Project: CHV, BSW	
	Format: MBZ	
	Privilege Check Disable	
	Project: CHV, BSW	
	Format: Enable	
	<p>This field when set, disables Privilege Violation checks on non-privileged batch buffers. When set Privileged commands are allowed to be executed from non-privileged batch buffers.</p>	
	Workaround	
<p>Workaround: Irrespective of "Privilege Check Disable" bit set, HW enforces chained or second level batch buffer "Address Space Indicator" to be PPGTT if the parent batch buffer Address Space Indicator is PPGTT.</p>		

GS Domain Clock Gate Control Register

GSCKGCTL - GS Domain Clock Gate Control Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	09028h			
Gunit Graphics Slow Clock Domain Clock Gating Control Register				
DWord	Bit	Description		
0	31:29	<p>RSVD</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>RSVD</p>	Access:	RO
	Access:	RO		
	28:24	<p>GMBC Clock Gate IDLE Count</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>GMBC IDLE Timer Count Value - bits[27:24] 0 = GMBC Idle timer disabled 1-15 = After GMBC indicates idle, wait this many clocks before gating. Bit [28] is additional Reserved R/W</p>	Access:	R/W
	Access:	R/W		
	23:20	<p>GPMG Clock Gate IDLE Counter</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>GPMGi dle timer. GPMG uses this as a its idle counter pre-load value for clock gating 0 = Idle timer disabled 1 - 15 = After unit indicates its idle, wait this many clocks before gating</p>	Access:	R/W
	Access:	R/W		
19:16	<p>GSIDLECNT</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Generic GUNIT GSCLK domain idle timer. GUNIT GS fubs (other than GMBC) use this as a counter pre-load value 0 = Idle timer disabled 1 - 15 = After a unit indicates idle, wait this many clocks before gating.</p>	Access:	R/W	
Access:	R/W			
15:13	<p>RSVD</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved</p>	Access:	RO	
Access:	RO			
12	<p>GDTCKGEN</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Access:	R/W	
Access:	R/W			

GCKGCTL - GS Domain Clock Gate Control Register

	GDT Clock Gating Enable. 0 = Disable clock gating. 1 = Enable clock gating.		
11	<p>GMBCPCKDIS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>GMBC Performance Monitor Clock Gating Disable 0 = Enable clock gating 1 = Disable clock gating</p>	Access:	R/W
Access:	R/W		
10	<p>GMBCKGDIS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>GMBC Clock Gating Disable: controls non-performance monitoring related clocks in the GMBC 0 = Enable clock gating 1 = Disable clock gating</p>	Access:	R/W
Access:	R/W		
9	<p>GPMGCKDIS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>GPMG Clock Gating Disable 0 = Enable clock gating 1 = Disable clock gating</p>	Access:	R/W
Access:	R/W		
8	<p>G3DRDCKGDIS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>G3D Read Return Clock Gating Disable 0 = Enable clock gating 1 = Disable clock gating</p>	Access:	R/W
Access:	R/W		
7	<p>G3DOUTCKGDIS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>G3D Outbound Clock Gating Disable: controls clocks associated with outbound requests. 0 = Enable clock gating 1 = Disable clock gating</p>	Access:	R/W
Access:	R/W		
6	<p>GMCFGCKGDIS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>GMCFG Clock Gating Disable 0 = Enable clock gating 1 = Disable clock gating</p>	Access:	R/W
Access:	R/W		
5	<p>GKEYSCKGDIS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table>	Access:	R/W
Access:	R/W		

GCKGCTL - GS Domain Clock Gate Control Register	
	GKEYS Clock Gating Disable 0 = Enable clock gating 1 = Disable clock gating
4	GCCBGSGDIS Access: R/W GCCBGS Clock Gating Disable 0 = Enable clock gating 1 = Disable clock gating
3:0	RSVD Access: RO Reserved

GS Invocation Counter

GS_INVOCATION_COUNT - GS Invocation Counter		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	02328h	
<p>This register stores the number of objects that are part of geometry shader threads. This register is part of the context save and restore.</p>		
DWord	Bit	Description
0	63:32	<p>GS Invocation Count UDW</p> <p>Number of objects that are dispatched as a geometry shader threads invoked by the GS stage. Updated only when Statistics Enable is set in GS_STATE (see the Geometry Shader Chapter in the 3D Volume.)</p>
	31:0	<p>GS Invocation Count LDW</p> <p>Number of objects that are dispatched as a geometry shader threads invoked by the GS stage. Updated only when Statistics Enable is set in GS_STATE (see the Geometry Shader Chapter in the 3D Volume.)</p>

GS Primitives Counter

GS_PRIMITIVES_COUNT - GS Primitives Counter		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	02330h	
<p>This register reflects the total number of primitives that have been output by the Geometry Shader stage. This register is part of the context save and restore.</p>		
DWord	Bit	Description
0	63:32	<p>GS Primitives Count UDW</p> <p>Total number of primitives output by the geometry stage. Updated only when Statistics Enable is set in GS_STATE (see the Geometry Shader Chapter in the 3D Volume.)</p>
	31:0	<p>GS Primitives Count LDW</p> <p>Total number of primitives output by the geometry stage. Updated only when Statistics Enable is set in GS_STATE (see the Geometry Shader Chapter in the 3D Volume.)</p>

GT_CR_POWER_METER_CTRL

PWRMTRLK - GT_CR_POWER_METER_CTRL				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A248h-0A24Bh			
DWord	Bit	Description		
0	31	<p>Power Meter and Push Bus Control Lock</p> <table border="1"> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>Controls whether power meter weights and other push bus control registers are writeable. 0 : Power Meter weights and control registers are writeable. 1: Writes to Power Meter weights and control registers are blocked. Lock bit cannot be cleared without cold reset.</p>	Access:	R/W Lock
	Access:	R/W Lock		
	30:7	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	6	<p>GSclk Domain GTI Baseline Energy Count Enable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>Controls whether the energy counter for the GTI power well, counting in the GSclk domain, is running or not. 0: Accumulator in PM is disabled 1: Accumulator in PM is enabled</p>	Access:	R/W Lock
Access:	R/W Lock			
5	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
4	<p>Render Power Meter Counter Enable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>Render Power Meter Enable : Controls whether power meter is running or not. 0: All Power meter counters/accumulators in PM are disabled and held at zero. 1: All power meter counters/accumulators in PM are enabled. Note that this bit does not affect intermediate accumulation/overflow logic elsewhere in the Gfx engine.</p>	Access:	R/W Lock	
Access:	R/W Lock			
3	<p>Media Power Meter Counter Enable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>Media Power Meter Enable :</p>	Access:	R/W Lock	
Access:	R/W Lock			

PWRMTRLK - GT_CR_POWER_METER_CTRL			
	<p>Controls whether power meter is running or not.</p> <p>0: All Power meter counters/accumulators in PM are disabled and held at zero.</p> <p>1: All power meter counters/accumulators in PM are enabled.</p> <p>Note that this bit does not affect intermediate accumulation/overflow logic elsewhere in the Gfx engine.</p>		
2:0	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%; text-align: center;">RO</td> </tr> </table>	Access:	RO
Access:	RO		

GTFIFOCTL

GTFIFOCTL - GTFIFOCTL		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	120008h	
GT FIFO Control.		
DWord	Bit	Description
0	31	GT_IOSFSB_READ_POLICY
		Default Value: 0b
	Access: R/W	
	<p>The SEC must first write this register bit before attempting Gunit register context reads. This is identified usage model requiring IOSF SB reads. Note : For CHV, BSW, Punit has it's own IOSF SB P interface.</p> <p>0 (Default) : Abort IOSF SB reads. Only Kf1 and Kf1 status are allowed. 1 : Allow IOSF SB reads.</p>	
	30:16	SPARE15
Default Value: 0000h		
Access: RO		
Reserved		
15	GT_FIFO_SB_POLICY	
	Default Value: 0b	
	Access: R/W	
<p>GT_WakeFIFO IOSF SB Policy register</p> <p>0 (default) : If WakeFIFO threshold hit and dedicated IOSF SB buffering is full, stall IOSF SB accesses targeting WakeFIFO.</p> <p>1 : If WakeFIFO threshold is hit AND dedicated IOSF SB buffering is full : a. Drop IOSF SB write requests to WakeFIFO b. IOSF SB reads targeting WakeFIFO return 1s. Evaluated for the request at the head of the IA_WakeFIFO.</p>		
14	GT_FIFO_BLOB_POLICY	
	Default Value: 0b	
	Access: R/W	
13	GT_FIFO_PRI_POLICY	
	Default Value: 0b	
	Access: R/W	
<p>GT_WakeFIFO IOSF Primary Policy register.</p> <p>0 (Default) : If WakeFIFO threshold hit, stall IOSF Primary accesses targeting WakeFIFO.</p>		

GTFIFOCTL - GTFIFOCTL					
	<p>1 : If WakeFIFO threshold is hit :</p> <p>a. Drop IOSF Primary writes to WakeFIFO</p> <p>b. IOSF Primary reads targeting WakeFIFO return 1s.</p> <p>Don't hang the system, but device 2 may hang.</p>				
12	<p>Block all Policy</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>BlockALL policy register applies to both HW FIFO and IA GT FIFO. This bit only applies when the GPM BlockALL indication is asserted.</p> <p>GPM BlockALL indication can assert for : A) CPD and B) for a period of time during RC6 entry.</p> <p>0 (default) : Allow register collapsing and stall request at the head if it is not collapse-able.</p> <p>1 : Stall request at the head.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
11	<p>RC6_POLICY</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>RC6 policy register applies to both HW FIFO and IA GT FIFO. This bit only applies :</p> <ul style="list-style-type: none"> - when BlockALL is not asserted - within RC6, and - ONLY when AllowWake register (13_0090h[0]=1). <p>0 (default) : Allow register collapsing and drop request at the head if it is not collapsible.</p> <p>1 : Stall request at the head if within RC6.</p> <p>Note: All hardware initiated requests should be collapsible.</p> <p>Note: Starting with Gen8 Gfx, the driver is required to ensure the targeted power well is alive before initiating an access outside shadow register space.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
10:9	<p>SPARE2</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>spare bit</p>	Default Value:	00b	Access:	R/W
Default Value:	00b				
Access:	R/W				
8	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
7:0	<p>SPARE8</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved</p>	Default Value:	00h	Access:	RO
Default Value:	00h				
Access:	RO				

GT Function Level Reset Control Message

FLRCTLMSG - GT Function Level Reset Control Message				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	08100h			
GT FLR Control Register				
DWord	Bit	Description		
0	31:16	Message Mask		
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000</p>	Access:	RO
	Access:	RO		
15:1	Reserved			
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved</p>	Access:	RO
Access:	RO			
	0	Reserved		
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved R/W: FLR is not supported on CHV, BSW.</p>	Access:	RO
Access:	RO			

GT INTERRUPT 0 ENABLE REGISTER

GT_INTERRUPT0_IER - GT INTERRUPT 0 ENABLE REGISTER		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	4430Ch-4430Fh	
<p>This table indicates which events are mapped to each bit of the GT Interrupt 0 registers. Bits 15:0 are used for Render CS. Bits 31:16 are used for Blitter CS.</p> <p>The IER enabled Render Interrupt IIR (sticky) bits are ORed together to generate the Render Interrupts Pending bit in the Master Interrupt Control register.</p> <p>The IER enabled Blitter Interrupt IIR (sticky) bits are ORed together to generate the Blitter Interrupts Pending bit in the Master Interrupt Control register.</p>		
DWord	Bit	Description
0	31	UNUSED0 Access: <input type="text"/> R/W
	30	UNUSED1 Access: <input type="text"/> R/W
	29	UNUSED2 Access: <input type="text"/> R/W
	28	UNUSED3 Access: <input type="text"/> R/W
	27	BCS_WAIT_ON_SEMAPHORE Access: <input type="text"/> R/W BCS wait on semaphore
	26	UNUSED4 Access: <input type="text"/> R/W
	25	UNUSED5 Access: <input type="text"/> R/W
	24	BCS_CTX_SWITCH_INTERRUPT Access: <input type="text"/> R/W BCS context switch interrupt
	23	UNUSED6 Access: <input type="text"/> R/W

GT_INTERRUPT0_IER - GT INTERRUPT 0 ENABLE REGISTER

22	UNUSED7	Access:	R/W
21	UNUSED8	Access:	R/W
20	BCS_MI_FLUSH_DWNOTIFY	Access:	R/W
	BCS MI flush DW notify		
19	BCS_ERROR_INTERRUPT	Access:	R/W
	BCS error interrupt		
18	UNUSED9	Access:	R/W
17	UNUSED10	Access:	R/W
16	BCS_MI_USER_INTERRUPT	Access:	R/W
	BCS MI user interrupt		
15	UNUSED11	Access:	R/W
14	UNUSED12	Access:	R/W
13	UNUSED13	Access:	R/W
12	UNUSED14	Access:	R/W
11	CS_WAIT_ON_SEMAPHORE	Access:	R/W
	CS wait on semaphore		
10	CS_L3_COUNTER_SAVE	Access:	R/W
	CS L3 counter save		
9	UNUSED15	Access:	R/W

GT_INTERRUPT0_IER - GT INTERRUPT 0 ENABLE REGISTER

8	<p>CS_CTX_SWITCH_INTERRUPT</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%; text-align: center;">R/W</td> </tr> </table> <p>CS context switch interrupt</p>	Access:	R/W
Access:	R/W		
7	<p>PAGE_FAULT_ERROR</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%; text-align: center;">R/W</td> </tr> </table> <p>this interrupt is for handling legacy page fault interface for all command streamer (BCS, VCS, RCS, VECS). when fault repair mode is enabled, interrupt mask register value is not looked at to generate interrupt due to page fault. please refer to 'page fault support' section for more details.</p>	Access:	R/W
Access:	R/W		
6	<p>CS_WATCHDOG_COUNTER_EXPIRED</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%; text-align: center;">R/W</td> </tr> </table> <p>CS watchdog counter expired</p>	Access:	R/W
Access:	R/W		
5	<p>L3PARITYERROR</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%; text-align: center;">R/W</td> </tr> </table> <p>L3 parity error</p>	Access:	R/W
Access:	R/W		
4	<p>CS_PIPE_CONTROL_NOTIFY</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%; text-align: center;">R/W</td> </tr> </table> <p>CS pipe control notify</p>	Access:	R/W
Access:	R/W		
3	<p>CS_ERROR_INTERRUPT</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%; text-align: center;">R/W</td> </tr> </table> <p>CS error interrupt</p>	Access:	R/W
Access:	R/W		
2	<p>UNUSED17</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%; text-align: center;">R/W</td> </tr> </table>	Access:	R/W
Access:	R/W		
1	<p>Reserved</p>		
0	<p>CS_MI_USER_INTERRUPT</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%; text-align: center;">R/W</td> </tr> </table> <p>CS context switch interrupt</p>	Access:	R/W
Access:	R/W		

GT INTERRUPT 0 IDENTITY REGISTER

GT_INTERRUPT0_IIR - GT INTERRUPT 0 IDENTITY REGISTER		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	44308h-4430Bh	
<p>This table indicates which events are mapped to each bit of the GT Interrupt 0 registers. Bits 15:0 are used for Render CS. Bits 31:16 are used for Blitter CS.</p> <p>The IER enabled Render Interrupt IIR (sticky) bits are ORed together to generate the Render Interrupts Pending bit in the Master Interrupt Control register.</p> <p>The IER enabled Blitter Interrupt IIR (sticky) bits are ORed together to generate the Blitter Interrupts Pending bit in the Master Interrupt Control register.</p>		
DWord	Bit	Description
0	31	UNUSED0 Access: R/W One Clear
	30	UNUSED1 Access: R/W One Clear
	29	UNUSED2 Access: R/W One Clear
	28	UNUSED3 Access: R/W One Clear
	27	BCS_WAIT_ON_SEMAPHORE Access: R/W One Clear BCS wait on semaphore
	26	UNUSED4 Access: R/W One Clear
	25	UNUSED5 Access: R/W One Clear
	24	BCS_CTX_SWITCH_INTERRUPT Access: R/W One Clear BCS context switch interrupt
	23	UNUSED6 Access: R/W One Clear

GT_INTERRUPT0_IIR - GT INTERRUPT 0 IDENTITY REGISTER

22	UNUSED7	Access:	R/W One Clear
21	UNUSED8	Access:	R/W One Clear
20	BCS_MI_FLUSH_DWNOTIFY	Access:	R/W One Clear
	BCS MI flush DW notify		
19	BCS_ERROR_INTERRUPT	Access:	R/W One Clear
	BCS error interrupt		
18	UNUSED9	Access:	R/W One Clear
17	UNUSED10	Access:	R/W One Clear
16	BCS_MI_USER_INTERRUPT	Access:	R/W One Clear
	BCS MI user interrupt		
15	UNUSED11	Access:	R/W One Clear
14	UNUSED12	Access:	R/W One Clear
13	UNUSED13	Access:	R/W One Clear
12	UNUSED14	Access:	R/W One Clear
11	CS_WAIT_ON_SEMAPHORE	Access:	R/W One Clear
	CS wait on semaphore		
10	CS_L3_COUNTER_SAVE	Access:	R/W One Clear
	CS L3 counter save		
9	UNUSED15	Access:	R/W One Clear

GT_INTERRUPT0_IIR - GT INTERRUPT 0 IDENTITY REGISTER

8	CS_CTX_SWITCH_INTERRUPT	Access:	R/W One Clear
CS context switch interrupt			
7	PAGE_FAULT_ERROR	Access:	R/W One Clear
this interrupt is for handling legacy page fault interface for all command streamer (BCS, VCS, RCS, VECS). when fault repair mode is enabled, interrupt mask register value is not looked at to generate interrupt due to page fault. please refer to 'page fault support' section for more details.			
6	CS_WATCHDOG_COUNTER_EXPIRED	Access:	R/W One Clear
CS watchdog counter expired			
5	L3PARITYERROR	Access:	R/W One Clear
L3 parity error			
4	CS_PIPE_CONTROL_NOTIFY	Access:	R/W One Clear
CS pipe control notify			
3	CS_ERROR_INTERRUPT	Access:	R/W One Clear
CS error interrupt			
2	UNUSED17	Access:	R/W One Clear
1	Reserved		
0	CS_MI_USER_INTERRUPT	Access:	R/W One Clear
CS context switch interrupt			

GT INTERRUPT 0 MASK REGISTER

GT_INTERRUPT0_IMR - GT INTERRUPT 0 MASK REGISTER		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x09190DF9	
Size (in bits):	32	
Address:	44304h-44307h	
<p>This table indicates which events are mapped to each bit of the GT Interrupt 0 registers. Bits 15:0 are used for Render CS. Bits 31:16 are used for Blitter CS.</p> <p>The IER enabled Render Interrupt IIR (sticky) bits are ORed together to generate the Render Interrupts Pending bit in the Master Interrupt Control register.</p> <p>The IER enabled Blitter Interrupt IIR (sticky) bits are ORed together to generate the Blitter Interrupts Pending bit in the Master Interrupt Control register.</p>		
DWord	Bit	Description
0	31	UNUSED0 Access: R/W
	30	UNUSED1 Access: R/W
	29	UNUSED2 Access: R/W
	28	UNUSED3 Access: R/W
	27	BCS_WAIT_ON_SEMAPHORE Default Value: 1b Access: R/W BCS wait on semaphore
	26	UNUSED4 Access: R/W
	25	UNUSED5 Access: R/W
	24	BCS_CTX_SWITCH_INTERRUPT Default Value: 1b Access: R/W BCS context switch interrupt
	23	UNUSED6

GT_INTERRUPT0_IMR - GT INTERRUPT 0 MASK REGISTER

	Access:	R/W
22	UNUSED7	
	Access:	R/W
21	UNUSED8	
	Access:	R/W
20	BCS_MI_FLUSH_DWNOTIFY	
	Default Value:	1b
	Access:	R/W
	BCS MI flush DW notify	
19	BCS_ERROR_INTERRUPT	
	Default Value:	1b
	Access:	R/W
	BCS error interrupt	
18	UNUSED9	
	Access:	R/W
17	UNUSED10	
	Access:	R/W
16	BCS_MI_USER_INTERRUPT	
	Default Value:	1b
	Access:	R/W
	BCS MI user interrupt	
15	UNUSED11	
	Access:	R/W
14	UNUSED12	
	Access:	R/W
13	UNUSED13	
	Access:	R/W
12	UNUSED14	
	Access:	R/W
11	CS_WAIT_ON_SEMAPHORE	
	Default Value:	1b
	Access:	R/W
	CS wait on semaphore	

GT_INTERRUPT0_IMR - GT INTERRUPT 0 MASK REGISTER

10	<p>CS_L3_COUNTER_SAVE</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>CS L3 counter save</p>	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				
9	<p>UNUSED15</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table>	Access:	R/W		
Access:	R/W				
8	<p>CS_CTX_SWITCH_INTERRUPT</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>CS context switch interrupt</p>	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				
7	<p>PAGE_FAULT_ERROR</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>this interrupt is for handling legacy page fault interface for all command streamer (BCS, VCS, RCS, VECS). when fault repair mode is enabled, interrupt mask register value is not looked at to generate interrupt due to page fault. please refer to 'page fault support' section for more details.</p>	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				
6	<p>CS_WATCHDOG_COUNTER_EXPIRED</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>CS watchdog counter expired</p>	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				
5	<p>L3PARITYERROR</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>L3 parity error</p>	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				
4	<p>CS_PIPE_CONTROL_NOTIFY</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>CS pipe control notify</p>	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				
3	<p>CS_ERROR_INTERRUPT</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>CS error interrupt</p>	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				

GT_INTERRUPT0_IMR - GT INTERRUPT 0 MASK REGISTER

	2	UNUSED17	
		Access:	R/W
	1	Reserved	
	0	CS_MI_USER_INTERRUPT	
		Default Value:	1b
		Access:	R/W
		CS context switch interrupt	

GT INTERRUPT 0 STATUS REGISTER

GT_INTERRUPT0_ISR - GT INTERRUPT 0 STATUS REGISTER		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	44300h-44303h	
<p>This table indicates which events are mapped to each bit of the GT Interrupt 0 registers. Bits 15:0 are used for Render CS. Bits 31:16 are used for Blitter CS.</p> <p>The IER enabled Render Interrupt IIR (sticky) bits are ORed together to generate the Render Interrupts Pending bit in the Master Interrupt Control register.</p> <p>The IER enabled Blitter Interrupt IIR (sticky) bits are ORed together to generate the Blitter Interrupts Pending bit in the Master Interrupt Control register.</p>		
DWord	Bit	Description
0	31	UNUSED0 Access: RO
	30	UNUSED1 Access: RO
	29	UNUSED2 Access: RO
	28	UNUSED3 Access: RO
	27	BCS_WAIT_ON_SEMAPHORE Access: RO BCS wait on semaphore
	26	UNUSED4 Access: RO
	25	UNUSED5 Access: RO
	24	BCS_CTX_SWITCH_INTERRUPT Access: RO BCS context switch interrupt
	23	UNUSED6 Access: RO

GT_INTERRUPT0_ISR - GT INTERRUPT 0 STATUS REGISTER

22	UNUSED7	Access:	RO
21	UNUSED8	Access:	RO
20	BCS_MI_FLUSH_DWNOTIFY	Access:	RO
	BCS MI flush DW notify		
19	BCS_ERROR_INTERRUPT	Access:	RO
	BCS error interrupt		
18	UNUSED9	Access:	RO
17	UNUSED10	Access:	RO
16	BCS_MI_USER_INTERRUPT	Access:	RO
	BCS MI user interrupt		
15	UNUSED11	Access:	RO
14	UNUSED12	Access:	RO
13	UNUSED13	Access:	RO
12	UNUSED14	Access:	RO
11	CS_WAIT_ON_SEMAPHORE	Access:	RO
	CS wait on semaphore		
10	CS_L3_COUNTER_SAVE	Access:	RO
	CS L3 counter save		
9	UNUSED15	Access:	RO

GT_INTERRUPT0_ISR - GT INTERRUPT 0 STATUS REGISTER

8	<p>CS_CTX_SWITCH_INTERRUPT</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> </table> <p>CS context switch interrupt</p>	Access:	RO
Access:	RO		
7	<p>PAGE_FAULT_ERROR</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> </table> <p>this interrupt is for handling legacy page fault interface for all command streamer (BCS, VCS, RCS, VECS). when fault repair mode is enabled, interrupt mask register value is not looked at to generate interrupt due to page fault. please refer to 'page fault support' section for more details.</p>	Access:	RO
Access:	RO		
6	<p>CS_WATCHDOG_COUNTER_EXPIRED</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> </table> <p>CS watchdog counter expired</p>	Access:	RO
Access:	RO		
5	<p>L3PARITYERROR</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> </table> <p>L3 parity error</p>	Access:	RO
Access:	RO		
4	<p>CS_PIPE_CONTROL_NOTIFY</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> </table> <p>CS pipe control notify</p>	Access:	RO
Access:	RO		
3	<p>CS_ERROR_INTERRUPT</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> </table> <p>CS error interrupt</p>	Access:	RO
Access:	RO		
2	<p>UNUSED17</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> </table>	Access:	RO
Access:	RO		
1	<p>Reserved</p>		
0	<p>CS_MI_USER_INTERRUPT</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> </table> <p>CS context switch interrupt</p>	Access:	RO
Access:	RO		

GT INTERRUPT1 ENABLE REGISTER

GT_INTERRUPT1_IER - GT INTERRUPT1 ENABLE REGISTER		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	4431Ch-4431Fh	
<p>This table indicates which events are mapped to each bit of the GT Interrupt 0 registers. Bits 15:0 are used for VCS1. Bits 31:16 are used for VCS2.</p> <p>The IER enabled VCS1 Interrupt IIR (sticky) bits are ORed together to generate the VCS1 Interrupts Pending bit in the Master Interrupt Control register.</p> <p>The IER enabled VCS2 Interrupt IIR (sticky) bits are ORed together to generate the VCS2 Interrupt Pending bit in the Master Interrupt Control register.</p>		
DWord	Bit	Description
0	31	UNUSED0 Access: R/W
	30	UNUSED1 Access: R/W
	29	UNUSED2 Access: R/W
	28	UNUSED3 Access: R/W
	27	VCS2_WAIT_ON_SEMAPHORE Access: R/W VCS2 wait on semaphore
	26	UNUSED4 Access: R/W
	25	Reserved
	24	VCS2_CTX_SWITCH_INTERRUPT Access: R/W VCS2 context switch interrupt
	23	UNUSED5 Access: R/W
	22	VCS2_WATCHDOG_COUNTER_EXPIRED

GT_INTERRUPT1_IER - GT INTERRUPT1 ENABLE REGISTER

		Access:	R/W
		VCS2 watchdog counter expired	
21	Reserved		
20	VCS2_MI_FLUSH_DWNOTIFY		
		Access:	R/W
		VCS2 MI flush DW notify	
19	VCS2_ERROR_INTERRUPT		
		Access:	R/W
		VCS2 error interrupt	
18	UNUSED6		
		Access:	R/W
17	UNUSED7		
		Access:	R/W
16	VCS2_MI_USER_INTERRUPT		
		Access:	R/W
		VCS2 MI user interrupt	
15	UNUSED8		
		Access:	R/W
14	UNUSED9		
		Access:	R/W
13	UNUSED10		
		Access:	R/W
12	UNUSED11		
		Access:	R/W
11	VCS1_WAIT_ON_SEMAPHORE		
		Access:	R/W
		VCS1 wait on semaphore	
10	UNUSED12		
		Access:	R/W
9	Reserved		
8	VCS1_CTX_SWITCH_INTERRUPT		
		Access:	R/W
		VCS1 context switch interrupt	

GT_INTERRUPT1_IER - GT INTERRUPT1 ENABLE REGISTER

7	UNUSED13	
	Access:	R/W
6	VCS1_WATCHDOG_COUNTER_EXPIRED	
	Access:	R/W
	VCS1 watchdog counter expired	
5	Reserved	
4	VCS1_MI_FLUSH_DWNOTIFY	
	Access:	R/W
	VCS1 MI flush DW notify	
3	VCS1_ERROR_INTERRUPT	
	Access:	R/W
	VCS1 error interrupt	
2	UNUSED14	
	Access:	R/W
1	UNUSED15	
	Access:	R/W
0	VCS1_MI_USER_INTERRUPT	
	Access:	R/W
	VCS1 MI user interrupt	

GT INTERRUPT1 IDENTITY REGISTER

GT_INTERRUPT1_IIR - GT INTERRUPT1 IDENTITY REGISTER		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	44318h-4431Bh	
<p>This table indicates which events are mapped to each bit of the GT Interrupt 0 registers. Bits 15:0 are used for VCS1. Bits 31:16 are used for VCS2.</p> <p>The IER enabled VCS1 Interrupt IIR (sticky) bits are ORed together to generate the VCS1 Interrupts Pending bit in the Master Interrupt Control register.</p> <p>The IER enabled VCS2 Interrupt IIR (sticky) bits are ORed together to generate the VCS2 Interrupt Pending bit in the Master Interrupt Control register.</p>		
DWord	Bit	Description
0	31	UNUSED0 Access: R/W One Clear
	30	UNUSED1 Access: R/W One Clear
	29	UNUSED2 Access: R/W One Clear
	28	UNUSED3 Access: R/W One Clear
	27	VCS2_WAIT_ON_SEMAPHORE Access: R/W One Clear VCS2 wait on semaphore
	26	UNUSED4 Access: R/W One Clear
	25	Reserved
	24	VCS2_CTX_SWITCH_INTERRUPT Access: R/W One Clear VCS2 context switch interrupt
	23	UNUSED5 Access: R/W One Clear
	22	VCS2_WATCHDOG_COUNTER_EXPIRED

GT_INTERRUPT1_IIR - GT INTERRUPT1 IDENTITY REGISTER

		Access:	R/W One Clear
		VCS2 watchdog counter expired	
21	Reserved		
20	VCS2_MI_FLUSH_DWNOTIFY		
		Access:	R/W One Clear
		VCS2 MI flush DW notify	
19	VCS2_ERROR_INTERRUPT		
		Access:	R/W One Clear
		VCS2 error interrupt	
18	UNUSED6		
		Access:	R/W One Clear
17	UNUSED7		
		Access:	R/W One Clear
16	VCS2_MI_USER_INTERRUPT		
		Access:	R/W One Clear
		VCS2 MI user interrupt	
15	UNUSED8		
		Access:	R/W One Clear
14	UNUSED9		
		Access:	R/W One Clear
13	UNUSED10		
		Access:	R/W One Clear
12	UNUSED11		
		Access:	R/W One Clear
11	VCS1_WAIT_ON_SEMAPHORE		
		Access:	R/W One Clear
		VCS1 wait on semaphore	
10	UNUSED12		
		Access:	R/W One Clear
9	Reserved		
8	VCS1_CTX_SWITCH_INTERRUPT		
		Access:	R/W One Clear
		VCS1 context switch interrupt	

GT_INTERRUPT1_IIR - GT INTERRUPT1 IDENTITY REGISTER

7	UNUSED13	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Access:</td> <td style="width: 50%;">R/W One Clear</td> </tr> </table>	Access:	R/W One Clear
Access:	R/W One Clear			
6	VCS1_WATCHDOG_COUNTER_EXPIRED	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Access:</td> <td style="width: 50%;">R/W One Clear</td> </tr> </table> <p>VCS1 watchdog counter expired</p>	Access:	R/W One Clear
Access:	R/W One Clear			
5	Reserved			
4	VCS1_MI_FLUSH_DWNOTIFY	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Access:</td> <td style="width: 50%;">R/W One Clear</td> </tr> </table> <p>VCS1 MI flush DW notify</p>	Access:	R/W One Clear
Access:	R/W One Clear			
3	VCS1_ERROR_INTERRUPT	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Access:</td> <td style="width: 50%;">R/W One Clear</td> </tr> </table> <p>VCS1 error interrupt</p>	Access:	R/W One Clear
Access:	R/W One Clear			
2	UNUSED14	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Access:</td> <td style="width: 50%;">R/W One Clear</td> </tr> </table>	Access:	R/W One Clear
Access:	R/W One Clear			
1	UNUSED15	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Access:</td> <td style="width: 50%;">R/W One Clear</td> </tr> </table>	Access:	R/W One Clear
Access:	R/W One Clear			
0	VCS1_MI_USER_INTERRUPT	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Access:</td> <td style="width: 50%;">R/W One Clear</td> </tr> </table> <p>VCS1 MI user interrupt</p>	Access:	R/W One Clear
Access:	R/W One Clear			

GT INTERRUPT1 MASK REGISTER

GT_INTERRUPT1_IMR - GT INTERRUPT1 MASK REGISTER		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x09590959	
Size (in bits):	32	
Address:	44314h-44317h	
<p>This table indicates which events are mapped to each bit of the GT Interrupt 0 registers. Bits 15:0 are used for VCS1. Bits 31:16 are used for VCS2.</p> <p>The IER enabled VCS1 Interrupt IIR (sticky) bits are ORed together to generate the VCS1 Interrupts Pending bit in the Master Interrupt Control register.</p> <p>The IER enabled VCS2 Interrupt IIR (sticky) bits are ORed together to generate the VCS2 Interrupt Pending bit in the Master Interrupt Control register.</p>		
DWord	Bit	Description
0	31	UNUSED0 Access: <input type="text"/> R/W
	30	UNUSED1 Access: <input type="text"/> R/W
	29	UNUSED2 Access: <input type="text"/> R/W
	28	UNUSED3 Access: <input type="text"/> R/W
	27	VCS2_WAIT_ON_SEMAPHORE Default Value: <input type="text"/> 1b Access: <input type="text"/> R/W VCS2 wait on semaphore
	26	UNUSED4 Access: <input type="text"/> R/W
	25	Reserved
	24	VCS2_CTX_SWITCH_INTERRUPT Default Value: <input type="text"/> 1b Access: <input type="text"/> R/W VCS2 context switch interrupt
	23	UNUSED5 Access: <input type="text"/> R/W

GT_INTERRUPT1_IMR - GT INTERRUPT1 MASK REGISTER

22	VCS2_WATCHDOG_COUNTER_EXPIRED	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 65%;">Default Value:</td> <td style="width: 35%;">1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VCS2 watchdog counter expired</p>	Default Value:	1b	Access:	R/W
Default Value:	1b					
Access:	R/W					
21	Reserved					
20	VCS2_MI_FLUSH_DWNOTIFY	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 65%;">Default Value:</td> <td style="width: 35%;">1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VCS2 MI flush DW notify</p>	Default Value:	1b	Access:	R/W
Default Value:	1b					
Access:	R/W					
19	VCS2_ERROR_INTERRUPT	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 65%;">Default Value:</td> <td style="width: 35%;">1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VCS2 error interrupt</p>	Default Value:	1b	Access:	R/W
Default Value:	1b					
Access:	R/W					
18	UNUSED6	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 65%;">Access:</td> <td style="width: 35%;">R/W</td> </tr> </table>	Access:	R/W		
Access:	R/W					
17	UNUSED7	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 65%;">Access:</td> <td style="width: 35%;">R/W</td> </tr> </table>	Access:	R/W		
Access:	R/W					
16	VCS2_MI_USER_INTERRUPT	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 65%;">Default Value:</td> <td style="width: 35%;">1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VCS2 MI user interrupt</p>	Default Value:	1b	Access:	R/W
Default Value:	1b					
Access:	R/W					
15	UNUSED8	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 65%;">Access:</td> <td style="width: 35%;">R/W</td> </tr> </table>	Access:	R/W		
Access:	R/W					
14	UNUSED9	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 65%;">Access:</td> <td style="width: 35%;">R/W</td> </tr> </table>	Access:	R/W		
Access:	R/W					
13	UNUSED10	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 65%;">Access:</td> <td style="width: 35%;">R/W</td> </tr> </table>	Access:	R/W		
Access:	R/W					
12	UNUSED11	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 65%;">Access:</td> <td style="width: 35%;">R/W</td> </tr> </table>	Access:	R/W		
Access:	R/W					
11	VCS1_WAIT_ON_SEMAPHORE	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 65%;">Default Value:</td> <td style="width: 35%;">1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VCS1 wait on semaphore</p>	Default Value:	1b	Access:	R/W
Default Value:	1b					
Access:	R/W					

GT_INTERRUPT1_IMR - GT INTERRUPT1 MASK REGISTER

	10	UNUSED12	
		Access:	R/W
	9	Reserved	
	8	VCS1_CTX_SWITCH_INTERRUPT	
		Default Value:	1b
		Access:	R/W
		VCS1 context switch interrupt	
	7	UNUSED13	
		Access:	R/W
	6	VCS1_WATCHDOG_COUNTER_EXPIRED	
		Default Value:	1b
		Access:	R/W
		VCS1 watchdog counter expired	
	5	Reserved	
	4	VCS1_MI_FLUSH_DWNOTIFY	
		Default Value:	1b
	Access:	R/W	
	VCS1 MI flush DW notify		
3	VCS1_ERROR_INTERRUPT		
	Default Value:	1b	
	Access:	R/W	
	VCS1 error interrupt		
2	UNUSED14		
	Access:	R/W	
1	UNUSED15		
	Access:	R/W	
0	VCS1_MI_USER_INTERRUPT		
	Default Value:	1b	
	Access:	R/W	
	VCS1 MI user interrupt		

GT INTERRUPT1 STATUS REGISTER

GT_INTERRUPT1_ISR - GT INTERRUPT1 STATUS REGISTER		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	44310h-44313h	
<p>This table indicates which events are mapped to each bit of the GT Interrupt 0 registers. Bits 15:0 are used for VCS1. Bits 31:16 are used for VCS2.</p> <p>The IER enabled VCS1 Interrupt IIR (sticky) bits are ORed together to generate the VCS1 Interrupts Pending bit in the Master Interrupt Control register.</p> <p>The IER enabled VCS2 Interrupt IIR (sticky) bits are ORed together to generate the VCS2 Interrupt Pending bit in the Master Interrupt Control register.</p>		
DWord	Bit	Description
0	31	UNUSED0 Access: RO
	30	UNUSED1 Access: RO
	29	UNUSED2 Access: RO
	28	UNUSED3 Access: RO
	27	VCS2_WAIT_ON_SEMAPHORE Access: RO VCS2 wait on semaphore
	26	UNUSED4 Access: RO
	25	Reserved
	24	VCS2_CTX_SWITCH_INTERRUPT Access: RO VCS2 context switch interrupt
	23	UNUSED5 Access: RO
	22	VCS2_WATCHDOG_COUNTER_EXPIRED

GT_INTERRUPT1_ISR - GT INTERRUPT1 STATUS REGISTER

		Access: RO	VCS2 watchdog counter expired
21	Reserved		
20	VCS2_MI_FLUSH_DWNOTIFY	Access: RO	VCS2 MI flush DW notify
19	VCS2_ERROR_INTERRUPT	Access: RO	VCS2 error interrupt
18	UNUSED6	Access: RO	
17	UNUSED7	Access: RO	
16	VCS2_MI_USER_INTERRUPT	Access: RO	VCS2 MI user interrupt
15	UNUSED8	Access: RO	
14	UNUSED9	Access: RO	
13	UNUSED10	Access: RO	
12	UNUSED11	Access: RO	
11	VCS1_WAIT_ON_SEMAPHORE	Access: RO	VCS1 wait on semaphore
10	UNUSED12	Access: RO	
9	Reserved		
8	VCS1_CTX_SWITCH_INTERRUPT	Access: RO	VCS1 context switch interrupt

GT_INTERRUPT1_ISR - GT INTERRUPT1 STATUS REGISTER			
7	<p>UNUSED13</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> </table>	Access:	RO
Access:	RO		
6	<p>VCS1_WATCHDOG_COUNTER_EXPIRED</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> </table> <p>VCS1 watchdog counter expired</p>	Access:	RO
Access:	RO		
5	Reserved		
4	<p>VCS1_MI_FLUSH_DWNOTIFY</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> </table> <p>VCS1 MI flush DW notify</p>	Access:	RO
Access:	RO		
3	<p>VCS1_ERROR_INTERRUPT</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> </table> <p>VCS1 error interrupt</p>	Access:	RO
Access:	RO		
2	<p>UNUSED14</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> </table>	Access:	RO
Access:	RO		
1	<p>UNUSED15</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> </table>	Access:	RO
Access:	RO		
0	<p>VCS1_MI_USER_INTERRUPT</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> </table> <p>VCS1 MI user interrupt</p>	Access:	RO
Access:	RO		

GT INTERRUPT3 ENABLE REGISTER

GT_INTERRUPT3_IER - GT INTERRUPT3 ENABLE REGISTER		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	4433Ch-4433Fh	
This table indicates which events are mapped to each bit of the GT interrupt 3 register. The VEDBOX Interrupt IIR sticky bits are Or'ed together to generate VEDBOX interrupt pending bit in the master interrupt control register.		
DWord	Bit	Description
0	31:29	UNUSED0 Access: <input type="text"/> R/W
	28	Reserved
	27:17	Reserved
	16	Reserved
	15:12	UNUSED2 Access: <input type="text"/> R/W
	11	VECS_WAIT_SEMAPHORE Access: <input type="text"/> R/W VECS wait on semaphore
	10:9	UNUSED3 Access: <input type="text"/> R/W
	8	VECS_CTX_SWITCH_INT Access: <input type="text"/> R/W VECS context switch interrupt
	7:5	UNUSED4 Access: <input type="text"/> R/W
	4	VECS_MI_FLUSH_DWNOTIFY Access: <input type="text"/> R/W VECS MI Flush DW Notify
3	VECS_ERR_INT Access: <input type="text"/> R/W VECS error interrupt	

GT_INTERRUPT3_IER - GT INTERRUPT3 ENABLE REGISTER				
	2:1	UNUSED5 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Access:	R/W
	Access:	R/W		
0	VECS_MI_USER_INT <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> VECS MI user interrupt	Access:	R/W	
Access:	R/W			

GT INTERRUPT3 IDENTITY REGISTER

GT_INTERRUPT3_IIR - GT INTERRUPT3 IDENTITY REGISTER		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	44338h-4433Bh	
This table indicates which events are mapped to each bit of the GT interrupt 3 register. The VEDBOX Interrupt IIR sticky bits are Ored together to generate VEDBOX interrupt pending bit in the master interrupt control register.		
DWord	Bit	Description
0	31:29	UNUSED0 Access: <input type="text"/> R/W One Clear
	28	Reserved
	27:17	Reserved
	16	Reserved
	15:12	UNUSED2 Access: <input type="text"/> R/W One Clear
	11	VECS_WAIT_SEMAPHORE Access: <input type="text"/> R/W One Clear VECS wait on semaphore
	10:9	UNUSED3 Access: <input type="text"/> R/W One Clear
	8	VECS_CTX_SWITCH_INT Access: <input type="text"/> R/W One Clear VECS context switch interrupt
	7:5	UNUSED4 Access: <input type="text"/> R/W One Clear
	4	VECS_MI_FLUSH_DWNOTIFY Access: <input type="text"/> R/W One Clear VECS MI Flush DW Notify
	3	VECS_ERR_INT Access: <input type="text"/> R/W One Clear VECS error interrupt

GT_INTERRUPT3_IIR - GT INTERRUPT3 IDENTITY REGISTER				
	2:1	UNUSED5 <table border="1"> <tr> <td>Access:</td> <td>R/W One Clear</td> </tr> </table>	Access:	R/W One Clear
	Access:	R/W One Clear		
	0	VECS_MI_USER_INT <table border="1"> <tr> <td>Access:</td> <td>R/W One Clear</td> </tr> </table> VECS MI user interrupt	Access:	R/W One Clear
Access:	R/W One Clear			

GT INTERRUPT3 MASK REGISTER

GT_INTERRUPT3_IMR - GT INTERRUPT3 MASK REGISTER						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00010919					
Size (in bits):	32					
Address:	44334h-44337h					
This table indicates which events are mapped to each bit of the GT interrupt 3 register. The VEDBOX Interrupt IIR sticky bits are Ored together to generate VEDBOX interrupt pending bit in the master interrupt control register.						
DWord	Bit	Description				
0	31:29	UNUSED0 Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td></td><td>R/W</td></tr></table>		R/W		
		R/W				
	28	Reserved				
	27:17	Reserved				
	16	Reserved				
	15:12	UNUSED2 Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td></td><td>R/W</td></tr></table>		R/W		
		R/W				
	11	VECS_WAIT_SEMAPHORE Default Value: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td></td><td>1b</td></tr></table> Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td></td><td>R/W</td></tr></table> VECS wait on semaphore		1b		R/W
		1b				
		R/W				
	10:9	UNUSED3 Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td></td><td>R/W</td></tr></table>		R/W		
		R/W				
8	VECS_CTX_SWITCH_INT Default Value: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td></td><td>1b</td></tr></table> Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td></td><td>R/W</td></tr></table> VECS context switch interrupt		1b		R/W	
	1b					
	R/W					
7:5	UNUSED4 Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td></td><td>R/W</td></tr></table>		R/W			
	R/W					
4	VECS_MI_FLUSH_DWNOTIFY Default Value: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td></td><td>1b</td></tr></table> Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td></td><td>R/W</td></tr></table> VECS MI Flush DW Notify		1b		R/W	
	1b					
	R/W					

GT_INTERRUPT3_IMR - GT INTERRUPT3 MASK REGISTER		
	3	VECS_ERR_INT
		Default Value: 1b
		Access: R/W
		VECS error interrupt
	2:1	UNUSED5
		Access: R/W
	0	VECS_MI_USER_INT
		Default Value: 1b
		Access: R/W
		VECS MI user interrupt

GT INTERRUPT3 STATUS REGISTER

GT_INTERRUPT3_ISR - GT INTERRUPT3 STATUS REGISTER		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	44330h-44333h	
This table indicates which events are mapped to each bit of the GT interrupt 3 register. The VEDBOX Interrupt IIR sticky bits are Or'ed together to generate VEDBOX interrupt pending bit in the master interrupt control register.		
DWord	Bit	Description
0	31:29	UNUSED0 Access: <input type="text"/> RO
	28	Reserved
	27:17	Reserved
	16	Reserved
	15:12	UNUSED2 Access: <input type="text"/> RO
	11	VECS_WAIT_SEMAPHORE Access: <input type="text"/> RO VECS wait on semaphore
	10:9	UNUSED3 Access: <input type="text"/> RO
	8	VECS_CTX_SWITCH_INT Access: <input type="text"/> RO VECS context switch interrupt
	7:5	UNUSED4 Access: <input type="text"/> RO
	4	VECS_MI_FLUSH_DWNOTIFY Access: <input type="text"/> RO VECS MI Flush DW Notify
3	VECS_ERR_INT Access: <input type="text"/> RO VECS error interrupt	

GT_INTERRUPT3_ISR - GT INTERRUPT3 STATUS REGISTER		
	2:1	UNUSED5
		Access: RO
	0	VECS_MI_USER_INT
		Access: RO VECS MI user interrupt

GTLC_PW_STAT

GTLC_PW_STAT - GTLC_PW_STAT			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	130094h		
This register contains Ack and status information for power well requests.			
DWord	Bit	Description	
0	31:8	RESERVED	
		Default Value:	000000h
		Access:	RO
		Reserved	
	7	Reserved	
	6	Reserved	
		Default Value:	0b
		Access:	RO
	Reserved		
	5	Reserved	
4	Reserved		
	Default Value:	0b	
	Access:	RO	
Reserved			
3:2	Reserved		
	Default Value:	00b	
	Access:	RO	
Reserved			
1	ALLOWWAKEERR		
	Default Value:	0b	
	Access:	R/W One Clear	
HW set, SW cleared. When access to media or render is observed when ALLOWWAKE=0, the ALLOWWAKEERR bit will be set. It will be up to SW or a power cycle to clear the ALLOWWAKEERR bit.			
0	ALLOWWAKEACK		
	Default Value:	0b	

GTLC_PW_STAT - GTLC_PW_STAT	
Access:	RO
Indicates that the allow wake request has been completed.	

GTLC_SURVIVE

GTLC_SURVIVE - GTLC_SURVIVE			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	130098h		
This register contains configuration bits for modes that the PM unit should operate in.			
DWord	Bit	Description	
0	31:12	RESERVED	
		Default Value:	00000h
		Access:	RO
		Reserved	
		11	gvd_pmu_bonus1
			Default Value:
Access:	R/W		
gvd_pmu_bonus1_zczfwoh			
10	gvd_pmu_bonus0		
	Default Value:	0b	
	Access:	R/W	
gvd_pmu_bonus0_zczfwoh			
9	pmu_gvd_bonus1		
	Default Value:	0b	
	Access:	RO	
pmu_gvd_bonus1_zczfwoh			
8	pmu_gvd_bonus0		
	Default Value:	0b	
	Access:	RO	
pmu_gvd_bonus0_zczfwoh			
7:4		RESERVED	
		Default Value:	0h
		Access:	RO
		Reserved	

GTLC_SURVIVE - GTLC_SURVIVE			
3	GFXCLKSTATUS		
	Default Value:	0b	
	Access:	RO	
	This bit is used as a way to confirm that the GFX clocks have been turned on with bit 2. SW would normally write a one to bit2 and then poll on this bit until.		
	2	GFXCLKFORCEON	
		Default Value:	0b
		Access:	R/W
		When this bit is set to a '1, the gvd_pmu_gfxclockstartreq_zczfwoh signal to the Punit will be forced to a one.	
	1	SPAREBIT	
		Default Value:	0b
		Access:	R/W
		Description	Project
Spare bit for CHV, BSW.		CHV, BSW	
0	GangMediaRender		
	Default Value:	0b	
	Access:	R/W	
	0 : The media and render power wells are brought down and up independently. 1 : PM unit will treat both wells as a unit, taking well down together and up together.		

GTLC_WAKE

GTLC_WAKE - GTLC_WAKE			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	130090h		
<p>GT Wake Control. This register is used as a way for the Punit to control the GTLC Render and Media Power wells. Writing bit 0 during normal operation may result in a hang.</p>			
DWord	Bit	Description	
0	31:26	RESERVED	
		Default Value:	00h
		Access:	RO
		Reserved	
25		RenderContextExists	
		Default Value:	0b
		Access:	RO
		<p>The usage is for support of s0ix, where Punit/Driver would restore the value in this bit no later than the time a '1' is written to ALLOWWAKEREQ (bit 0 of this register) during s0ix exit. SW should not write '1' to this bit during a cold boot exit or warm reset exit. CZ reset is the only thing that can clear this bit.</p> <p>This bit is set by HW after the first Render context save after cold boot or warm reset. SW can only write a one to this bit. If SW tries to write a zero, the previous value will be maintained.</p>	
24		MediaContextExists	
		Default Value:	0b
		Access:	RO
		<p>The usage is for support of s0ix, where Punit/Driver would restore the value in this bit no later than the time a '1' is written to ALLOWWAKEREQ (bit 0 of this register) during s0ix exit. SW should not write '1' to this bit during a cold boot exit or warm reset exit. CZ reset is the only thing that can clear this bit.</p> <p>This bit is set by HW after the first Media context save after cold boot or warm reset. SW can only write a one to this bit. If SW tries to write a zero, the previous value will be maintained.</p>	
23:8		Common No-wake Hysteresis timer for gfxstartclkreq	
		Default Value:	0000h

GTLC_WAKE - GTLC_WAKE					
	<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>New for CHV, BSW. Hysteresis timer would be used to deassert gfxclockstartreq in case of both wells being in standby and common no-wake request occurs. Counter will be incremented on 60ns interval.</p>	Access:	R/W		
Access:	R/W				
7:1	<p>RESERVED</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">00h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved</p>	Default Value:	00h	Access:	RO
Default Value:	00h				
Access:	RO				
0	<p>ALLOWWAKEREQ</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This bit is used as a way for the driver to make sure GTLC Render AND MEDIA engines do not wake while powered down. The usage is specifically with s0ix, where the driver wants to access the message channel common well (GSclk domain) and does not want the render/media wells to wake up. To remove ambiguity, this bit should be set to '1 and the ALLOWWAKEACK should be observed to the '1 before the FWAKEMEDIAREQ/FWAKERENDERREQ are set. Care must be taken to ONLY use this register prior to Gunit being powered down for S0ix or after registers have been initialized.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				

GT Mode Register

GT_MODE - GT Mode Register												
Register Space:	MMIO: 0/2/0											
Project:	CHV, BSW											
Source:	RenderCS											
Default Value:	0x00000000 CHV, BSW											
Access:	R/W											
Size (in bits):	32											
Trusted Type:	1											
Address:	07008h											
Valid Projects:	CHV, BSW											
This Register is used to control the 6EU and 12EU configuration for GT. Writing 0x01FF01FF to this register enables the 6EU mode.												
DWord	Bit	Description										
0	31:16	Mask										
		Access:	WO									
		Format:	Mask[15:0]									
		Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)										
15		EU Local Thread Checking Enable										
		Project:	CHV, BSW									
		Access:	r/w									
		This field configures the EU local thread checking. If enable the stateless access will be checked against the local thread's scratch space size and start address.										
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disable [Default]</td> <td>EU local thread checking is disabled.</td> <td>CHV, BSW</td> </tr> <tr> <td>1h</td> <td>Enable</td> <td>EU local thread checking is enabled.</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Value	Name	Description	Project	0h	Disable [Default]	EU local thread checking is disabled.	CHV, BSW	1h	Enable
Value	Name	Description	Project									
0h	Disable [Default]	EU local thread checking is disabled.	CHV, BSW									
1h	Enable	EU local thread checking is enabled.	CHV, BSW									
14:13		SFR mode										
		Project:	CHV, BSW									
		Access:	r/w									
		Format:	U2									
		This field must be zero when not in GT4(SFR) configuration i.e GTB_rendermode fuse set to SFR.										
12		Reserved										
		Project:	CHV, BSW									
		Access:	r/w									
		Format:	PBC									
11		16X16 Cross Slice Hash Disable for SF										

GT_MODE - GT Mode Register

		Project:	CHV, BSW
		Access:	r/w
		Format:	U1
Description			
This field allows to control pixel block hashing across slices.			
Supports 16X16 pixel block hashing in the checker-board pattern irrespective of MSAA. Setting this bit disables hashing and therefore HW will send all the Pixels to both the slices.			
Value	Name	Description	
0h	Enable [Default]	16X16 Checkerboard hashing enabled across slices	
1h	Disable	16X16 Checkerboard hashing disabled across slices	
Programming Notes			
Normal mode of operation in GT3 mode will be to use either 16x16 Hashing or 32x32 Hashing.			
10	16X16 Cross Slice Hash Disable		
		Project:	CHV, BSW
		Access:	r/w
		Format:	U1
This field allows to control pixel block hashing across slices.			
Value	Name	Description	
0h	Enable [Default]	16X16 Checkerboard hashing enabled across slices	
1h	Disable	16X16 Checkerboard hashing disabled across slices	
9	WIZ Hashing Mode High Bit		
		Project:	CHV, BSW
		Access:	r/w
		Format:	U1
This field adds additional hashing modes in combination with the WIZ Hashing Mode field. The Value column in the table below refers to this field (high bit) and the WIZ Hashing Mode field (low bit). This field is don't care if the Hashing Disable bit is set.			
Value	Name	Description	
0h	[Default]	8x8 Checkerboard hashing	
1h		8x4 Checkerboard hashing	
2h		16x4 Checkerboard hashing	
3h		Reserved	
Programming Notes			
8x4 hashing preferred for when msaa enabled			

GT_MODE - GT Mode Register

8	Reserved		
	Project:	CHV, BSW	
	Access:	r/w	
	Format:	PBC	
	7	WIZ Hashing Mode	
		Project:	CHV, BSW
		Access:	r/w
		Format:	U1
		Description	
	This field configures the Hashing mode in Windower. This field is don't care if the Hashing Disable bit is set.		
	The WIZ Hashing Mode High Bit field is combined with this field to enable additional modes.		
	Project		
	CHV, BSW		
	6:3	Reserved	
		Access:	r/w
Format:		PBC	
2	Reserved		
	Access:	r/w	
	Format:	PBC	
1:0	Reserved		
	Access:	r/w	
	Format:	PBC	

GTSCRATCH1

GTSCRATCH1 - GTSCRATCH1						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F100h					
<p>These (8 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>GT_Scratchpad</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GTSCRATCH2

GTSCRATCH2 - GTSCRATCH2						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F104h					
<p>These (8 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>GT_Scratchpad</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GTSCRATCH3

GTSCRATCH3 - GTSCRATCH3						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F108h					
<p>These (8 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>GT_Scratchpad</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GTSCRATCH4

GTSCRATCH4 - GTSCRATCH4						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F10Ch					
<p>These (8 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>GT_Scratchpad</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GTSCRATCH5

GTSCRATCH5 - GTSCRATCH5						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F110h					
<p>These (8 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>GT_Scratchpad</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GTSCRATCH6

GTSCRATCH6 - GTSCRATCH6						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F114h					
<p>These (8 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>GT_Scratchpad</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GTSCRATCH7

GTSCRATCH7 - GTSCRATCH7						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F118h					
<p>These (8 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>GT_Scratchpad</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GTSCRATCH8

GTSCRATCH8 - GTSCRATCH8						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F11Ch					
<p>These (8 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>GT_Scratchpad</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GTSCRATCHPAD0

GTSCRATCHPAD0 - GTSCRATCHPAD0						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	130040h					
<p>GT scratchpad registers. Scratchpad register can be R/W by both driver and GT. One usage is that GT updates those registers before going to RC6 and reads them on RC6 exit. Write-able and read-able from GT. Reads do NOT rely on the register dispatch path, as dependencies could result. Read-able and write-able from IA. New for CHV, BSW.</p>						
DWord	Bit	Description				
0	31:0	<p>GT_Scratch0</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>GT scratchpad register.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GTSCRATCHPAD1

GTSCRATCHPAD1 - GTSCRATCHPAD1						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	130044h					
<p>GT scratchpad registers. Scratchpad register can be R/W by both driver and GT. One usage is that GT updates those registers before going to RC6 and reads them on RC6 exit. Write-able and read-able from GT. Reads do NOT rely on the register dispatch path, as dependencies could result. Read-able and write-able from IA. New for CHV, BSW.</p>						
DWord	Bit	Description				
0	31:0	<p>GT_Scratch1</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>GT scratchpad register.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GTSCRATCHPAD2

GTSCRATCHPAD2 - GTSCRATCHPAD2						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	130048h					
<p>GT scratchpad registers. Scratchpad register can be R/W by both driver and GT. One usage is that GT updates those registers before going to RC6 and reads them on RC6 exit. Write-able and read-able from GT. Reads do NOT rely on the register dispatch path, as dependencies could result. Read-able and write-able from IA. New for CHV, BSW.</p>						
DWord	Bit	Description				
0	31:0	<p>GT_Scratch2</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>GT scratchpad register.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GTSCRATCHPAD3

GTSCRATCHPAD3 - GTSCRATCHPAD3						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	13004Ch					
<p>GT scratchpad registers. Scratchpad register can be R/W by both driver and GT. One usage is that GT updates those registers before going to RC6 and reads them on RC6 exit. Write-able and read-able from GT. Reads do NOT rely on the register dispatch path, as dependencies could result. Read-able and write-able from IA. New for CHV, BSW.</p>						
DWord	Bit	Description				
0	31:0	<p>GT_Scratch3</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>GT scratchpad register.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GTSCRATCHPAD4

GTSCRATCHPAD4 - GTSCRATCHPAD4						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	130050h					
<p>GT scratchpad registers. Scratchpad register can be R/W by both driver and GT. One usage is that GT updates those registers before going to RC6 and reads them on RC6 exit. Write-able and read-able from GT. Reads do NOT rely on the register dispatch path, as dependencies could result. Read-able and write-able from IA. New for CHV, BSW.</p>						
DWord	Bit	Description				
0	31:0	<p>GT_Scratch4</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>GT scratchpad register.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GTSCRATCHPAD5

GTSCRATCHPAD5 - GTSCRATCHPAD5						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	130054h					
<p>GT scratchpad registers. Scratchpad register can be R/W by both driver and GT. One usage is that GT updates those registers before going to RC6 and reads them on RC6 exit. Write-able and read-able from GT. Reads do NOT rely on the register dispatch path, as dependencies could result. Read-able and write-able from IA. New for CHV, BSW.</p>						
DWord	Bit	Description				
0	31:0	<p>GT_Scratch5</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>GT scratchpad register.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GTSCRATCHPAD6

GTSCRATCHPAD6 - GTSCRATCHPAD6						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	130058h					
<p>GT scratchpad registers. Scratchpad register can be R/W by both driver and GT. One usage is that GT updates those registers before going to RC6 and reads them on RC6 exit. Write-able and read-able from GT. Reads do NOT rely on the register dispatch path, as dependencies could result. Read-able and write-able from IA. New for CHV, BSW.</p>						
DWord	Bit	Description				
0	31:0	<p>GT_Scratch6</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>GT scratchpad register.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GTSCRATCHPAD7

GTSCRATCHPAD7 - GTSCRATCHPAD7						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	13005Ch					
<p>GT scratchpad registers. Scratchpad register can be R/W by both driver and GT. One usage is that GT updates those registers before going to RC6 and reads them on RC6 exit. Write-able and read-able from GT. Reads do NOT rely on the register dispatch path, as dependencies could result. Read-able and write-able from IA. New for CHV, BSW.</p>						
DWord	Bit	Description				
0	31:0	<p>GT_Scratch7</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>GT scratchpad register.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GTT Cache Enable

GTT_CACHE_EN - GTT Cache Enable										
Register Space:	MMIO: 0/2/0									
Project:	CHV, BSW									
Source:	PRM									
Default Value:	0x00000000 CHV, BSW									
Size (in bits):	32									
Address:	04024h									
Enable GTT Cache for respective client(s), A0: Must program/observed this to all 0 due to Big Pages Bug 1898112										
DWord	Bit	Description								
0	31:0	<p>GTT Cache Enable for CS</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%; text-align: center;">R/W</td> </tr> </table> <p>Enable GTT Caching for all the client(s) below: 31: BLIT Engine (overrides individual enables of the units) 30: VEBX Engine (overrides individual enables of the units) 29: MFX Engine (overrides individual enables of the units) 28: GFX Engine (overrides individual enables of the units) 27-15: Reserved 14: VMCunit 13: VLFunit 12: BLBunit 11: VFWunit 10: VEOunit 9: HIZunit 8: RCZunit 7: RCCunit 6: ISCunit 5: DCunit 4: MTunit 3: SOLunit 2: VFunit 1: RSunit 0: CSunit</p> <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 10px;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Project</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">00000000h</td> <td style="text-align: center;">[Default]</td> <td style="text-align: center;">CHV, BSW</td> </tr> </tbody> </table>	Access:	R/W	Value	Name	Project	00000000h	[Default]	CHV, BSW
Access:	R/W									
Value	Name	Project								
00000000h	[Default]	CHV, BSW								

GTTMMADR_LSB

GTTMMADR_LSB - GTTMMADR_LSB					
Register Space:	PCI: 0/2/0				
Project:	CHV, BSW				
Source:	PRM				
Default Value:	0x00000004				
Size (in bits):	32				
Address:	00010h				
<p>Gfx Memory Mapped Address Range. This is the base address for all memory mapped registers and GTT table.</p> <p>This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. For the Global GTT, this range is defined as a memory BAR in graphics device config space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT memory area.</p> <p>GTTMMADR comprises of 2 regions, GTT and MMADR. Prior to this feature it had a max size of 4M with 2M MMADR + {0,1M, 2M} GTT. Now GTTMMADR will have a max size of 16M.GTTMMADR = 2M MMADR + 6M rsvd + {0, 2M, 4M, 8M} GTT.GTTMMADR will be 16M aligned.</p>					
DWord	Bit	Description			
0	31:24	MBA_LSB			
		<table border="1"> <tr> <td>Default Value:</td> <td>00h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Memory Base Address (MBA): Set by the OS, these bits correspond to address signals [35:24].16MB combined for MMIO and Global GTT table aperture (2MB for MMIO, 6MB reserved and 8 MB for GTT).</p>	Default Value:	00h	Access:
	Default Value:	00h			
	Access:	R/W			
23:4	Reserved				
	<table border="1"> <tr> <td>Default Value:</td> <td>00000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>RSVD:Hardwired to 0 to indicate at least 4MB address range.</p>	Default Value:	00000h	Access:	RO
Default Value:	00000h				
Access:	RO				
3	Reserved				
	<table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Prefetchable Memory (PREFMEM): Hardwired to 0to prevent prefetching.</p>	Default Value:	0b	Access:	RO
Default Value:	0b				
Access:	RO				
2:1	MEMTYP				
	<table border="1"> <tr> <td>Default Value:</td> <td>10b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Memory Type (MEMTYP):</p>	Default Value:	10b	Access:	RO
Default Value:	10b				
Access:	RO				

GTTMMADR_LSB - GTTMMADR_LSB	
	00: To indicate 32 bit base address 01: Reserved 10: To indicate 64 bit base address 11: Reserved
0	Reserved

GTTMMADR_MSB

GTTMMADR_MSB - GTTMMADR_MSB				
Register Space:	PCI: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	00014h			
<p>Gfx Memory Mapped Address Range. This is the base address for all memory mapped registers and GTT table.</p> <p>This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. For the Global GTT, this range is defined as a memory BAR in graphics device config space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT memory area.</p> <p>GTTMMADR comprises of 2 regions, GTT and MMADR. Prior to this feature it had a max size of 4M with 2M MMADR + {0,1M, 2M} GTT. Now GTTMMADR will have a max size of 16M. GTTMMADR = 2M MMADR + 6M rsvd + {0, 2M, 4M, 8M} GTT. GTTMMADR will be 16M aligned.</p>				
DWord	Bit	Description		
0	31:4	MBA_MSB28		
		Default Value:	0000000h	
		Access:	R/W	
		Description		Project
		This field must be set to 0 since addressing above 64GB is not supported.		
		Made them spare RW bits.		CHV, BSW
3:0		MBA_MSB		
		Default Value:	0h	
		Access:	R/W	
Memory Base Address (MBA): Set by the OS, these bits correspond to address signals [35:24]. 16MB combined for MMIO and Global GTT table aperture (2MB for MMIO, 6MB reserved and 8 MB for GTT).				

GU_CTL0

GU_CTL0 - GU_CTL0			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000070		
Size (in bits):	32		
Address:	182030h		
Gunit Configuration bits.			
DWord	Bit	Description	
0	31	GT_IOSFSB_P_READ_POLICY	
		Default Value:	0b
		Access:	R/W
		<p>During an SOIx flow, the Punit must read Gunit registers. 0 (Default) : Allow IOSF SB P reads. Note : Punit knows when appropriate times are to issue IOSF SB P reads. 1 : Abort IOSF SB P reads.</p> <p>Note : This default is the opposite of the IOSF SB polarity bit 12_0008h[31]. Note : For CHV, BSW, this policy register will applies to new PM endpoint (which includes the new PM endpoint).</p>	
30:16		SPARE15	
		Default Value:	0000h
		Access:	R/W
Spare register bits for future use			
15		SB_Doorbellprevention	
		Default Value:	0b
		Access:	R/W
<p>0 (default) : IOSF P to IOSF SB doorbell registers can be accesses by IOSF SB and IOSF SBp. Note : This should never occur during normal operation. 1 : IOSF SB and IOSF SBp accesses targeting the IOSF P to IOSF SB doorbell registers are aborted.</p>			
14		SPARE1	
		Default Value:	0b
		Access:	R/W
Spare register bits for future use			
13		Reserved	

GU_CTL0 - GU_CTL0		
12	CMDperCLK_ECO	
	Default Value:	0b
	Access:	R/W
0(default): GSA command per clock supported. 1: A GAM write followed by a read command cannot dispatch in consecutive clocked.		
11	Reserved	
10:9	SPARE2	
	Default Value:	00b
	Access:	R/W
Spare bits for future use		
8	RESERVED	
	Default Value:	0b
	Access:	RO
Reserved		
7	IOSFP_DCR_Policy	
	Default Value:	0b
	Access:	R/W
IOSF Primary Data Credit Policy. 0 (default) : IOSF Primary data credits reflect data buffer depth. 1: IOSF Primary infinite data credits for both posted and non-posted data is advertised. Credit accounting (and flow control) will rely on cmd credits only.		
6:4	IOSFP_PCRD	
	Default Value:	111b
	Access:	R/W
IOSF Primary Credit AdvertisementNumber of posted command (and data credits/4) will advertize.		
3	SPARE3	
	Default Value:	0b
	Access:	R/W
Spare bits for future use		
2	Reserved	
1	Reserved	
0	PFI_Snoop_Override	
	Default Value:	0b

GU_CTL0 - GU_CTL0

	Access:	R/W
	0 : Observe GAM snoop/non-snoop indications. 1 : Force all GAM requests to snoop.	

Hardware Status Mask Register

HWSTAM - Hardware Status Mask Register						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	RenderCS					
Default Value:	0xFFFFFFFF					
Access:	R/W, RO					
Size (in bits):	32					
Trusted Type:	1					
Address:	02098h					
Address:	12098h-1209Bh					
Name:	Hardware Status Mask Register					
ShortName:	HWSTAM_VCSUNIT0					
Address:	1A098h-1A09Bh					
Name:	Hardware Status Mask Register					
ShortName:	HWSTAM_VECSUNIT					
Address:	1C098h-1C09Bh					
Name:	Hardware Status Mask Register					
ShortName:	HWSTAM_VCSUNIT1					
Address:	22098h-2209Bh					
Name:	Hardware Status Mask Register					
ShortName:	HWSTAM_BCSUNIT					
<p>The HWSTAM register has the same format as the Interrupt Control Registers. The bits in this register are mask bits that prevent the corresponding bits in the Interrupt Status Register from generating a Hardware Status Write (PCI write cycle). Any unmasked interrupt bit (HWSTAM bit set to 0) will allow the Interrupt Status Register to be written to the ISR location (within the memory page specified by the Hardware Status Page Address Register) when that Interrupt Status Register bit changes state.</p>						
Programming Notes						
<ul style="list-style-type: none"> To write the interrupt to the HWSP, the corresponding IMR bit must also be clear (enabled). At most 1 bit can be unmasked at any given time. 						
DWord	Bit	Description				
0	31:0	<p>Hardware Status Mask Register Value</p> <table border="1"> <tr> <td>Default Value:</td> <td>FFFFFFFFh</td> </tr> <tr> <td>Format:</td> <td>Array of Masks</td> </tr> </table> <p>Refer to the Interrupt Control Register section for bit definitions. Reserved bits are RO.</p>	Default Value:	FFFFFFFFh	Format:	Array of Masks
Default Value:	FFFFFFFFh					
Format:	Array of Masks					

Hardware Status Page Address Register

HWS_PGA - Hardware Status Page Address Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Trusted Type:	1			
Address:	02080h-02083h			
Name:	Hardware Status Page Address Register			
ShortName:	HWS_PGA_RCSUNIT			
Address:	12080h-12083h			
Name:	Hardware Status Page Address Register			
ShortName:	HWS_PGA_VCSUNIT0			
Address:	1A080h-1A083h			
Name:	Hardware Status Page Address Register			
ShortName:	HWS_PGA_VECSUNIT			
Address:	1C080h-1C083h			
Name:	Hardware Status Page Address Register			
ShortName:	HWS_PGA_VCSUNIT1			
Address:	22080h-22083h			
Name:	Hardware Status Page Address Register			
ShortName:	HWS_PGA_BCSUNIT			
Description				
This register is used to program the 4 KB-aligned System Memory address of the Hardware Status Page used to report hardware status into (typically cacheable) System Memory.				
The address in this register is translated using the Global GTT in memory. The mapping type of the GTT entry determines the snoop nature of the transaction to memory.				
CHV, BSW				
DWord	Bit	Description		
0	31:12	<p>Address</p> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>GraphicsAddress[31:12]</td> </tr> </table> <p>This field is used by SW to specify Bits 31:12 of the 4 KB-aligned System Memory address of the 4 KB page known as the Hardware Status Page. The Global GTT is used to map this page from the graphics virtual address to physical address.</p>	Format:	GraphicsAddress[31:12]
Format:	GraphicsAddress[31:12]			

HWS_PGA - Hardware Status Page Address Register

		Programming Notes	
		If the Per-Process Virtual Address Space and Exec List Enable bit is set, HW requires that the status page is programmed to allow for the context switch status to be reported.	
	11:0	Reserved	
		Format:	MBZ

HCP CABAC Status

HCP_CABAC_STATUS - HCP CABAC Status			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	VideoCS		
Default Value:	0x00000000		
Size (in bits):	32		
Trusted Type:	1		
Address:	1E904h		
HCP CABAC status.			
DWord	Bit	Description	
0	31:12	Reserved	
		Format: MBZ	
	11	Temporal Direction Motion Vector Out-of-Bound Error	
		Default Value: 0	
		Access: RO	
		Format: U1	
			This flag indicates motion vectors calculated from the Temporal Direct Motion vector is larger than the allowed range.
	10:7	Reserved	
		Format: MBZ	
	6	Motion Vector Delta SE	
		Default Value: 0	
		Access: RO	
Format: U1			
		This flag indicates out-of-bound motion vector delta SEs coded in the bit-stream.	
5	Delta QP SE		
	Default Value: 0		
	Access: RO		
	Format: U1		
		This flag indicates leading-one overflow during CABAC decode of cu_qp_delta_abs.	
4	Residual Error		
	Default Value: 0		
	Access: RO		

HCP_CABAC_STATUS - HCP CABAC Status							
	<table border="1"> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>This flag indicates out-of-bound absolute coefficient level SEs coded in the bit-stream.</p>	Format:	U1				
Format:	U1						
3	<p>Slice and Error</p> <table border="1"> <tr> <td>Default Value:</td> <td>0</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>This flag indicates a pre-mature end to the slice or an inconsistent end of slice on the last Ctb of a slice.</p>	Default Value:	0	Access:	RO	Format:	U1
Default Value:	0						
Access:	RO						
Format:	U1						
2:1	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ				
Format:	MBZ						
0	<p>Ctb Concealment Flag</p> <table border="1"> <tr> <td>Default Value:</td> <td>0</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>Each pulse from this flag indicates one Ctb is concealed by the HCP.</p>	Default Value:	0	Access:	RO	Format:	U1
Default Value:	0						
Access:	RO						
Format:	U1						

HCP Decode Status

HCP_DEC_STATUS - HCP Decode Status			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	VideoCS		
Default Value:	0x00000000		
Access:	RO		
Size (in bits):	32		
Trusted Type:	1		
Address:	1E900h		
HCP Decode status.			
DWord	Bit	Description	
0	31:18	Number of Ctbs Concealed	
		Default Value:	0
		Format:	U14
		This 16-bit field indicates the number of Ctbs concealed during the decoding of the current frame. This field is cleared with the HCP_PIPE_MODE_SELECT command.	
17		Frame Dec Active	
		Default Value:	0
		Format:	U1
This flag indicates that the decoder hardware is actively decoding a picture.			
16		Indirect Bitstream ObjectAccess Upper Bound Error	
		Default Value:	0
		Format:	U1
This flag indicates that the upper bound bit-stream address was reached.			
15:0		Bit-stream Error Flags	
		Default Value:	0
		Format:	U16
This 16-bit field indicates the number of bit stream errors detected for each bit field indicated in the CABAC Status register.			

HCP Picture Checksum cldx0

HCP_PICTURE_CHECKSUM_CIDX0 - HCP Picture Checksum cldx0						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	VideoCS					
Default Value:	0x00000000					
Access:	RO					
Size (in bits):	32					
Trusted Type:	1					
Address:	1E91Ch					
	<ul style="list-style-type: none"> The HCP Picture Checksum cldx0 register reports the 32-bit unsigned picture checksum for cldx=0 calculated by the HCP hardware and whose algorithm is defined in Annex D of the HEVC standard specification. This calculated value is updated at the end of the frame. 					
DWord	Bit	Description				
0	31:0	Picture checksum cldx0 <table border="1"> <tr> <td>Default Value:</td> <td>0</td> </tr> <tr> <td>Format:</td> <td>U32</td> </tr> </table>	Default Value:	0	Format:	U32
Default Value:	0					
Format:	U32					

HCP Picture Checksum cldx1

HCP_PICTURE_CHECKSUM_CIDX1 - HCP Picture Checksum cldx1						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	VideoCS					
Default Value:	0x00000000					
Access:	RO					
Size (in bits):	32					
Trusted Type:	1					
Address:	1E920h					
	<ul style="list-style-type: none"> The HCP Picture Checksum cldx1 register reports the 32-bit unsigned picture checksum for cldx=1 calculated by the HCP hardware and whose algorithm is defined in Annex D of the HEVC standard specification. This calculated value is updated at the end of the frame. 					
DWord	Bit	Description				
0	31:0	Picture checksum cldx1 <table border="1"> <tr> <td>Default Value:</td> <td>0</td> </tr> <tr> <td>Format:</td> <td>U32</td> </tr> </table>	Default Value:	0	Format:	U32
Default Value:	0					
Format:	U32					

HCP Picture Checksum cldx2

HCP_PICTURE_CHECKSUM_CIDX2 - HCP Picture Checksum cldx2						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	VideoCS					
Default Value:	0x00000000					
Access:	RO					
Size (in bits):	32					
Trusted Type:	1					
Address:	1E924h					
	<ul style="list-style-type: none"> The HCP Picture Checksum cldx2 register reports the 32-bit unsigned picture checksum for cldx=2 calculated by the HCP hardware and whose algorithm is defined in Annex D of the HEVC standard specification. This calculated value is updated at the end of the frame. 					
DWord	Bit	Description				
0	31:0	Picture checksum cldx2 <table border="1"> <tr> <td>Default Value:</td> <td>0</td> </tr> <tr> <td>Format:</td> <td>U32</td> </tr> </table>	Default Value:	0	Format:	U32
Default Value:	0					
Format:	U32					

HDR

HDR - HDR		
Register Space:	PCI: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0000Ch	
Header Type		
DWord	Bit	Description
0	31:24	RESERVED
		Default Value: 00h
		Access: RO
		Reserved
	23	MULTI_FUNCTION_STATUS
		Default Value: 0b
		Access: RO
		MFUNC: Integrated graphics is a single function
	22:16	HEADER_CODE
		Default Value: 00h
		Access: RO
		HDR: Indicates a type 0 configuration space header format
	15:0	RESERVED
		Default Value: 0000h
		Access: RO
		Reserved

HEVC Local APIC Retry Vector

HEVC_LAPIC_RETRY_VECT - HEVC Local APIC Retry Vector				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoCS			
Default Value:	0x00000000			
Access:	RO			
Size (in bits):	32			
Address:	0D594h			
Valid Projects:	CHV, BSW			
<p>Holds the 4 last retry interrupt vectors. Retries are errors in hardware and are not expected. No interrupt is actually retried, and the interrupt stimulus will be lost if a retry occurs. The system will hang eventually. A 2-bit counter (starting at reset value of 0) is used to point to the slot/byte location from which to load the next retry vector (into the 4 available slots) in sequence. This means if a 5th retry vector shows up, it will be loaded into slot 0 again (as the counter wraps around), over-writing the retry vector which existed there in slot_0.</p>				
DWord	Bit	Description		
0	31:24	Vector Slot 3 Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td> </td><td>U8</td></tr></table>		U8
		U8		
	23:16	Vector Slot 2 Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td> </td><td>U8</td></tr></table>		U8
		U8		
15:8	Vector Slot 1 Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td> </td><td>U8</td></tr></table>		U8	
	U8			
7:0	Vector Slot 0 Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td> </td><td>U8</td></tr></table>		U8	
	U8			

HS Invocation Counter

HS_INVOCATION_COUNT - HS Invocation Counter		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	02300h	
<p>This register stores the number of patch objects processed by the HS unit. E.g., A PATCHLIST_2 topology with 6 vertices would cause this counter to increment by 3 (there are 3 2-vertex patch objects in that topology). This register is part of the context save and restore.</p>		
DWord	Bit	Description
0	63:32	HS Invocation Count UDW Number of patch objects processed by the HS stage. Updated only when HS Enable and HS Statistics Enable are set in 3DSTATE_HS
	31:0	HS Invocation Count LDW Number of patch objects processed by the HS stage. Updated only when HS Enable and HS Statistics Enable are set in 3DSTATE_HS

IA32 MTRR FIX4K_C0000 High

MTRR_FIX4K_C0000_H - IA32 MTRR FIX4K_C0000 High						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F13Ch					
Fixed MTRR to identify (C0000-C8000h).						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32 MTRR FIX4K_C0000 Low

MTRR_FIX4K_C0000_L - IA32 MTRR FIX4K_C0000 Low						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F138h					
Fixed MTRR to identify (C0000-C8000h).						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32 MTRR FIX4K_C8000 High

MTRR_FIX4K_C8000_H - IA32 MTRR FIX4K_C8000 High						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F144h					
Fixed MTRR to identify (C8000-D0000h).						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32 MTRR FIX4K_C8000 Low

MTRR_FIX4K_C8000_L - IA32 MTRR FIX4K_C8000 Low						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F140h					
Fixed MTRR to identify (C8000-D0000h).						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32 MTRR FIX4K_D0000 High

MTRR_FIX4K_D0000_H - IA32 MTRR FIX4K_D0000 High						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F14Ch					
Fixed MTRR to identify (D0000-D8000h)						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32 MTRR FIX4K_D0000 Low

MTRR_FIX4K_D0000_L - IA32 MTRR FIX4K_D0000 Low						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F148h					
Fixed MTRR to identify (D0000-D8000h)						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32 MTRR FIX4K_D8000 High

MTRR_FIX4K_D8000_H - IA32 MTRR FIX4K_D8000 High						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F154h					
Fixed MTRR to identify (D8000-E0000h)						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32 MTRR_FIX4K_D8000 Low

MTRR_FIX4K_D8000_L - IA32 MTRR_FIX4K_D8000 Low						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F150h					
Fixed MTRR to identify (D8000-E0000h)						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32 MTRR FIX4K_E0000 High

MTRR_FIX4K_E0000_H - IA32 MTRR FIX4K_E0000 High						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F15Ch					
Fixed MTRR to identify (E0000-E8000h).						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32 MTRR_FIX4K_E0000 Low

MTRR_FIX4K_E0000_L - IA32 MTRR_FIX4K_E0000 Low						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F158h					
Fixed MTRR to identify (E0000-E8000h).						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32 MTRR FIX4K_E8000 High

MTRR_FIX4K_E8000_H - IA32 MTRR FIX4K_E8000 High						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F164h					
Fixed MTRR to identify (E8000-F0000h).						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32 MTRR FIX4K_E8000 Low

MTRR_FIX4K_E8000_L - IA32 MTRR FIX4K_E8000 Low						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F160h					
Fixed MTRR to identify (E8000-F0000h).						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32 MTRR FIX4K_F0000 High

MTRR_FIX4K_F0000_H - IA32 MTRR FIX4K_F0000 High						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F16Ch					
Fixed MTRR to identify (F0000-F8000h).						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32 MTRR FIX4K_F0000 Low

MTRR_FIX4K_F0000_L - IA32 MTRR FIX4K_F0000 Low						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F168h					
Fixed MTRR to identify (F0000-F8000h).						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32 MTRR FIX4K_F8000 High

MTRR_FIX4K_F8000_H - IA32 MTRR FIX4K_F8000 High						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F174h					
Fixed MTRR to identify (F8000-100000h).						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32 MTRR FIX4K_F8000 Low

MTRR_FIX4K_F8000_L - IA32 MTRR FIX4K_F8000 Low						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F170h					
Fixed MTRR to identify (F8000-100000h).						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32 MTRR FIX16K_80000 High

MTRR_FIX16K_80000_H - IA32 MTRR FIX16K_80000 High						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F12Ch					
Fixed MTRR to identify 512K-768K of the main memory (80000-A0000h).						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32 MTRR_FIX16K_80000 Low

MTRR_FIX16K_80000_L - IA32 MTRR_FIX16K_80000 Low						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F128h					
Fixed MTRR to identify 512K-768K of the main memory (80000-A0000h).						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#.0</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32 MTRR FIX16K_A0000 High

MTRR_FIX16K_A0000_H - IA32 MTRR FIX16K_A0000 High						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F134h					
Fixed MTRR to identify 768K-1024K of the main memory (A0000-C0000h).						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32 MTRR_FIX16K_A0000 Low

MTRR_FIX16K_A0000_L - IA32 MTRR_FIX16K_A0000 Low						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F130h					
Fixed MTRR to identify 768K-1024K of the main memory (A0000-C0000h).						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32 MTRR FIX64K_00000 High

MTRR_FIX64K_00000_H - IA32 MTRR FIX64K_00000 High						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F124h					
Fixed MTRR to identify 0-512K of the main memory (0-80000h).						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32 MTRR FIX64K_00000 Low

MTRR_FIX64K_00000_L - IA32 MTRR FIX64K_00000 Low						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F120h					
Fixed MTRR to identify 0-512K of the main memory (0-80000h).						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32 MTRR PHYSBASE0 High

MTRR_PHYSBASE0_H - IA32 MTRR PHYSBASE0 High			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F184h		
Variable MTRR0			
DWord	Bit	Description	
0	31:7	Reserved	
		Default Value:	0000000000000000000000000000b
		Access:	RO
	6:0	PhysBase	
		Default Value:	0000000b
		Access:	R/W
		Physical Base address[38:32] of the variable MTRR.	

IA32 MTRR PHYSBASE0 Low

MTRR_PHYSBASE0_L - IA32 MTRR PHYSBASE0 Low			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F180h		
Variable MTRR0			
DWord	Bit	Description	
0	31:12	PhysBase	
		Default Value:	00000h
		Access:	R/W
			Physical Base address[31:0] of the variable MTRR.
	11:8	Reserved	
		Default Value:	0000b
		Access:	RO
	7:0	Memory Type	
		Default Value:	00h
Access:		R/W	
		Identifies the memory type 00h-FFh.	

IA32 MTRR PHYSBASE1 High

MTRR_PHYSBASE1_H - IA32 MTRR PHYSBASE1 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F194h	
Variable MTRR1		
DWord	Bit	Description
0	31:7	Reserved
		Default Value: 00000000000000000000000000000000b
	Access: RO	
	6:0	PhysBase
Default Value: 0000000b		
Access: R/W		
Physical Base address[38:32] of the variable MTRR.		

IA32 MTRR PHYSBASE1 Low

MTRR_PHYSBASE1_L - IA32 MTRR PHYSBASE1 Low			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F190h		
Variable MTRR1			
DWord	Bit	Description	
0	31:12	PhysBase	
		Default Value:	00000h
		Access:	R/W
			Physical Base address[31:0] of the variable MTRR.
	11:8	Reserved	
		Default Value:	0000b
		Access:	RO
	7:0	Memory Type	
		Default Value:	00h
Access:		R/W	
		Identifies the memory type 00h-FFh.	

IA32 MTRR PHYSBASE2 High

MTRR_PHYSBASE2_H - IA32 MTRR PHYSBASE2 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F1A4h	
Variable MTRR2		
DWord	Bit	Description
0	31:7	Reserved
		Default Value: 0000000000000000000000000000b
	Access: RO	
	6:0	PhysBase
Default Value: 0000000b		
Access: R/W		
Physical Base address[38:32] of the variable MTRR.		

IA32 MTRR PHYSBASE2 Low

MTRR_PHYSBASE2_L - IA32 MTRR PHYSBASE2 Low			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F1A0h		
Variable MTRR2			
DWord	Bit	Description	
0	31:12	PhysBase	
		Default Value:	00000h
		Access:	R/W
			Physical Base address[31:0] of the variable MTRR.
	11:8	Reserved	
		Default Value:	0000b
		Access:	RO
	7:0	Memory Type	
		Default Value:	00h
Access:		R/W	
		Identifies the memory type 00h-FFh.	

IA32 MTRR PHYSBASE3 High

MTRR_PHYSBASE3_H - IA32 MTRR PHYSBASE3 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F1B4h	
Variable MTRR3		
DWord	Bit	Description
0	31:7	Reserved
		Default Value: 0000000000000000000000000000b
	Access: RO	
	6:0	PhysBase
Default Value: 0000000b		
Access: R/W		
Physical Base address[38:32] of the variable MTRR.		

IA32 MTRR PHYSBASE3 Low

MTRR_PHYSBASE3_L - IA32 MTRR PHYSBASE3 Low			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F1B0h		
Variable MTRR3			
DWord	Bit	Description	
0	31:12	PhysBase	
		Default Value:	00000h
		Access:	R/W
			Physical Base address[31:0] of the variable MTRR.
	11:8	Reserved	
		Default Value:	0000b
		Access:	RO
	7:0	Memory Type	
		Default Value:	00h
Access:		R/W	
		Identifies the memory type 00h-FFh.	

IA32 MTRR PHYSBASE4 High

MTRR_PHYSBASE4_H - IA32 MTRR PHYSBASE4 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F1C4h	
Variable MTRR4		
DWord	Bit	Description
0	31:7	Reserved
		Default Value: 0000000000000000000000000000b
	Access: RO	
	6:0	PhysBase
Default Value: 0000000b		
Access: R/W		
Physical Base address[38:32] of the variable MTRR.		

IA32 MTRR PHYSBASE4 Low

MTRR_PHYSBASE4_L - IA32 MTRR PHYSBASE4 Low			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F1C0h		
Variable MTRR4			
DWord	Bit	Description	
0	31:12	PhysBase	
		Default Value:	00000h
		Access:	R/W
			Physical Base address[31:0] of the variable MTRR.
	11:8	Reserved	
		Default Value:	0000b
		Access:	RO
	7:0	Memory Type	
		Default Value:	00h
Access:		R/W	
		Identifies the memory type 00h-FFh	

IA32 MTRR PHYSBASE5 High

MTRR_PHYSBASE5_H - IA32 MTRR PHYSBASE5 High			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F1D4h		
Variable MTRR5			
DWord	Bit	Description	
0	31:7	Reserved	
		Default Value:	000000000000000000000000b
		Access:	RO
	6:0	PhysBase	
		Default Value:	0000000b
		Access:	R/W
		Physical Base address[38:32] of the variable MTRR.	

IA32 MTRR PHYSBASE5 Low

MTRR_PHYSBASE5_L - IA32 MTRR PHYSBASE5 Low			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F1D0h		
Variable MTRR5			
DWord	Bit	Description	
0	31:12	PhysBase	
		Default Value:	00000h
		Access:	R/W
			Physical Base address[31:0] of the variable MTRR.
	11:8	Reserved	
		Default Value:	0000b
		Access:	RO
	7:0	Memory Type	
		Default Value:	00h
Access:		R/W	
		Identifies the memory type 00h-FFh.	

IA32 MTRR PHYSBASE6 High

MTRR_PHYSBASE6_H - IA32 MTRR PHYSBASE6 High			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F1E4h		
Variable MTRR6			
DWord	Bit	Description	
0	31:7	Reserved	
		Default Value:	000000000000000000000000b
		Access:	RO
	6:0	PhysBase	
		Default Value:	0000000b
		Access:	R/W
		Physical Base address[38:32] of the variable MTRR.	

IA32 MTRR PHYSBASE6 Low

MTRR_PHYSBASE6_L - IA32 MTRR PHYSBASE6 Low			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F1E0h		
Variable MTRR6			
DWord	Bit	Description	
0	31:12	PhysBase	
		Default Value:	00000h
		Access:	R/W
			Physical Base address[31:0] of the variable MTRR.
	11:8	Reserved	
		Default Value:	0000b
		Access:	RO
	7:0	Memory Type	
		Default Value:	00h
Access:		R/W	
		Identifies the memory type 00h-FFh.	

IA32 MTRR PHYSBASE7 High

MTRR_PHYSBASE7_H - IA32 MTRR PHYSBASE7 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F1F4h	
Variable MTRR7		
DWord	Bit	Description
0	31:7	Reserved
		Default Value: 00000000000000000000000000000000b
	Access: RO	
	6:0	PhysBase
Default Value: 0000000b		
Access: R/W		
Physical Base address[38:32] of the variable MTRR.		

IA32 MTRR PHYSBASE7 Low

MTRR_PHYSBASE7_L - IA32 MTRR PHYSBASE7 Low			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F1F0h		
Variable MTRR7			
DWord	Bit	Description	
0	31:12	PhysBase	
		Default Value:	00000h
		Access:	R/W
			Physical Base address[31:0] of the variable MTRR.
	11:8	Reserved	
		Default Value:	0000b
		Access:	RO
	7:0	Memory Type	
		Default Value:	00h
Access:		R/W	
		Identifies the memory type 00h-FFh.	

IA32 MTRR PHYSBASE8 High

MTRR_PHYSBASE8_H - IA32 MTRR PHYSBASE8 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F204h	
Variable MTRR8		
DWord	Bit	Description
0	31:7	Reserved
		Default Value: 0000000000000000000000000000b
	Access: RO	
	6:0	PhysBase
Default Value: 0000000b		
Access: R/W		
Physical Base address[38:32] of the variable MTRR.		

IA32 MTRR PHYSBASE8 Low

MTRR_PHYSBASE8_L - IA32 MTRR PHYSBASE8 Low			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F200h		
Variable MTRR8			
DWord	Bit	Description	
0	31:12	PhysBase	
		Default Value:	00000h
		Access:	R/W
			Physical Base address[31:0] of the variable MTRR
	11:8	Reserved	
		Default Value:	0000b
		Access:	RO
	7:0	Memory Type	
		Default Value:	00h
Access:		R/W	
		Identifies the memory type 00h-FFh.	

IA32 MTRR PHYSBASE9 High

MTRR_PHYSBASE9_H - IA32 MTRR PHYSBASE9 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F214h	
Variable MTRR9		
DWord	Bit	Description
0	31:7	Reserved
		Default Value: 00000000000000000000000000000000b
	Access: RO	
	6:0	PhysBase
Default Value: 0000000b		
Access: R/W		
Physical Base address[38:32] of the variable MTRR.		

IA32 MTRR PHYSBASE9 Low

MTRR_PHYSBASE9_L - IA32 MTRR PHYSBASE9 Low			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F210h		
Variable MTRR9			
DWord	Bit	Description	
0	31:12	PhysBase	
		Default Value:	00000h
		Access:	R/W
			Physical Base address[31:0] of the variable MTRR.
	11:8	Reserved	
		Default Value:	0000b
		Access:	RO
	7:0	Memory Type	
		Default Value:	00h
Access:		R/W	
		Identifies the memory type 00h-FFh.	

IA32 MTRR PHYSMASK0 High

MTRR_PHYSMASK0_H - IA32 MTRR PHYSMASK0 High			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F18Ch		
Variable MTRR0			
DWord	Bit	Description	
0	31:7	Reserved	
		Default Value:	000000000000000000000000b
		Access:	RO
	6:0	PhysMask	
		Default Value:	0000000b
		Access:	R/W
		Physical MASK for the address[38:32] of the variable MTRR.	

IA32 MTRR PHYSMASK0 Low

MTRR_PHYSMASK0_L - IA32 MTRR PHYSMASK0 Low			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F188h		
Variable MTRR0			
DWord	Bit	Description	
0	31:12	PhysMask	
		Default Value:	00000h
		Access:	R/W
			Physical MASK for the address[31:0] of the variable MTRR.
	11	Valid	
		Default Value:	0b
		Access:	R/W
			Valid bit showing that MTRR decode is active.
	10:0	Reserved	
Default Value:		00000000000b	
Access:		RO	

IA32 MTRR PHYSMASK1 High

MTRR_PHYSMASK1_H - IA32 MTRR PHYSMASK1 High			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F19Ch		
Variable MTRR1			
DWord	Bit	Description	
0	31:7	Reserved	
		Default Value:	000000000000000000000000b
		Access:	RO
	6:0	PhysMask	
		Default Value:	0000000b
		Access:	R/W
		Physical MASK for the address[38:32] of the variable MTRR.	

IA32 MTRR PHYSMASK1 Low

MTRR_PHYSMASK1_L - IA32 MTRR PHYSMASK1 Low			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F198h		
Variable MTRR1			
DWord	Bit	Description	
0	31:12	PhysMask	
		Default Value:	00000h
		Access:	R/W
			Physical MASK for the address[31:0] of the variable MTRR.
	11	Valid	
		Default Value:	0b
		Access:	R/W
			Valid bit showing that MTRR decode is active.
	10:0	Reserved	
Default Value:		00000000000b	
Access:		RO	

IA32 MTRR PHYSMASK2 High

MTRR_PHYSMASK2_H - IA32 MTRR PHYSMASK2 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F1ACh	
Variable MTRR2		
DWord	Bit	Description
0	31:7	Reserved
		Default Value: 000000000000000000000000b
		Access: RO
	6:0	PhysMask
		Default Value: 0000000b
		Access: R/W
		Physical MASK for the address[38:32] of the variable MTRR.

IA32 MTRR PHYSMASK2 Low

MTRR_PHYSMASK2_L - IA32 MTRR PHYSMASK2 Low			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F1A8h		
Variable MTRR2			
DWord	Bit	Description	
0	31:12	PhysMask	
		Default Value:	00000h
		Access:	R/W
			Physical MASK for the address[31:0] of the variable MTRR.
	11	Valid	
		Default Value:	0b
		Access:	R/W
			Valid bit showing that MTRR decode is active.
	10:0	Reserved	
Default Value:		00000000000b	
Access:		RO	

IA32 MTRR PHYSMASK3 High

MTRR_PHYSMASK3_H - IA32 MTRR PHYSMASK3 High			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F1BCh		
Variable MTRR3			
DWord	Bit	Description	
0	31:7	Reserved	
		Default Value:	000000000000000000000000b
		Access:	RO
	6:0	PhysMask	
		Default Value:	0000000b
		Access:	R/W
		Physical MASK for the address[38:32] of the variable MTRR.	

IA32 MTRR PHYSMASK3 Low

MTRR_PHYSMASK3_L - IA32 MTRR PHYSMASK3 Low			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F1B8h		
Variable MTRR3			
DWord	Bit	Description	
0	31:12	PhysMask	
		Default Value:	00000h
		Access:	R/W
			Physical MASK for the address[31:0] of the variable MTRR.
	11	Valid	
		Default Value:	0b
		Access:	R/W
			Valid bit showing that MTRR decode is active.
	10:0	Reserved	
Default Value:		00000000000b	
Access:		RO	

IA32 MTRR PHYSMASK4 High

MTRR_PHYSMASK4_H - IA32 MTRR PHYSMASK4 High			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F1CCh		
Variable MTRR4			
DWord	Bit	Description	
0	31:7	Reserved	
		Default Value:	000000000000000000000000b
		Access:	RO
	6:0	PhysMask	
		Default Value:	0000000b
		Access:	R/W
		Physical MASK for the address[38:32] of the variable MTRR.	

IA32 MTRR PHYSMASK4 Low

MTRR_PHYSMASK4_L - IA32 MTRR PHYSMASK4 Low			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F1C8h		
Variable MTRR4			
DWord	Bit	Description	
0	31:12	PhysMask	
		Default Value:	00000h
		Access:	R/W
			Physical MASK for the address[31:0] of the variable MTRR.
	11	Valid	
		Default Value:	0b
		Access:	R/W
			Valid bit showing that MTRR decode is active.
	10:0	Reserved	
Default Value:		00000000000b	
Access:		RO	

IA32 MTRR PHYSMASK5 High

MTRR_PHYSMASK5_H - IA32 MTRR PHYSMASK5 High			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F1DCh		
Variable MTRR5			
DWord	Bit	Description	
0	31:7	Reserved	
		Default Value:	000000000000000000000000b
		Access:	RO
	6:0	PhysMask	
		Default Value:	0000000b
		Access:	R/W
		Physical MASK for the address[38:32] of the variable MTRR.	

IA32 MTRR PHYSMASK5 Low

MTRR_PHYSMASK5_L - IA32 MTRR PHYSMASK5 Low			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F1D8h		
Variable MTRR5			
DWord	Bit	Description	
0	31:12	PhysMask	
		Default Value:	00000h
		Access:	R/W
			Physical MASK for the address[31:0] of the variable MTRR.
	11	Valid	
		Default Value:	0b
		Access:	R/W
			Valid bit showing that MTRR decode is active.
	10:0	Reserved	
Default Value:		00000000000b	
Access:		RO	

IA32 MTRR PHYSMASK6 High

MTRR_PHYSMASK6_H - IA32 MTRR PHYSMASK6 High			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F1ECh		
Variable MTRR6			
DWord	Bit	Description	
0	31:7	Reserved	
		Default Value:	000000000000000000000000b
		Access:	RO
	6:0	PhysMask	
		Default Value:	0000000b
		Access:	R/W
		Physical MASK for the address[38:32] of the variable MTRR.	

IA32 MTRR PHYSMASK6 Low

MTRR_PHYSMASK6_L - IA32 MTRR PHYSMASK6 Low			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F1E8h		
Variable MTRR6			
DWord	Bit	Description	
0	31:12	PhysMask	
		Default Value:	00000h
		Access:	R/W
			Physical MASK for the address[31:0] of the variable MTRR.
	11	Valid	
		Default Value:	0b
		Access:	R/W
			Valid bit showing that MTRR decode is active.
	10:0	Reserved	
Default Value:		00000000000b	
Access:		RO	

IA32 MTRR PHYSMASK7 High

MTRR_PHYSMASK7_H - IA32 MTRR PHYSMASK7 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F1FCh	
Variable MTRR7		
DWord	Bit	Description
0	31:7	Reserved
		Default Value: 000000000000000000000000b
	Access: RO	
	6:0	PhysMask
Default Value: 0000000b		
Access: R/W		
Physical MASK for the address[38:32] of the variable MTRR.		

IA32 MTRR PHYSMASK7 Low

MTRR_PHYSMASK7_L - IA32 MTRR PHYSMASK7 Low			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F1F8h		
Variable MTRR7			
DWord	Bit	Description	
0	31:12	PhysMask	
		Default Value:	00000h
		Access:	R/W
			Physical MASK for the address[31:0] of the variable MTRR.
	11	Valid	
		Default Value:	0b
		Access:	R/W
			Valid bit showing that MTRR decode is active.
	10:0	Reserved	
Default Value:		00000000000b	
Access:		RO	

IA32 MTRR PHYSMASK8 High

MTRR_PHYSMASK8_H - IA32 MTRR PHYSMASK8 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F20Ch	
Variable MTRR8		
DWord	Bit	Description
0	31:7	Reserved
		Default Value: 000000000000000000000000b
		Access: RO
	6:0	PhysMask
		Default Value: 0000000b
		Access: R/W
		Physical MASK for the address[38:32] of the variable MTRR.

IA32 MTRR PHYSMASK8 Low

MTRR_PHYSMASK8_L - IA32 MTRR PHYSMASK8 Low			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F208h		
Variable MTRR8			
DWord	Bit	Description	
0	31:12	PhysMask	
		Default Value:	00000h
		Access:	R/W
			Physical MASK for the address[31:0] of the variable MTRR.
	11	Valid	
		Default Value:	0b
		Access:	R/W
			Valid bit showing that MTRR decode is active.
	10:0	Reserved	
Default Value:		00000000000b	
Access:		RO	

IA32 MTRR PHYSMASK9 High

MTRR_PHYSMASK9_H - IA32 MTRR PHYSMASK9 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F21Ch	
Variable MTRR9		
DWord	Bit	Description
0	31:7	Reserved
		Default Value: 000000000000000000000000b
		Access: RO
	6:0	PhysMask
		Default Value: 0000000b
		Access: R/W
		Physical MASK for the address[38:32] of the variable MTRR.

IA32 MTRR PHYSMASK9 Low

MTRR_PHYSMASK9_L - IA32 MTRR PHYSMASK9 Low			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F218h		
Variable MTRR9			
DWord	Bit	Description	
0	31:12	PhysMask	
		Default Value:	00000h
		Access:	R/W
			Physical MASK for the address[31:0] of the variable MTRR.
	11	Valid	
		Default Value:	0b
		Access:	R/W
			Valid bit showing that MTRR decode is active.
	10:0	Reserved	
Default Value:		00000000000b	
Access:		RO	

IA Vertices Count

IA_VERTICES_COUNT - IA Vertices Count		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	02310h	
Valid Projects:		
This register stores the count of vertices processed by VF. This register is part of the context save and restore.		
DWord	Bit	Description
0	63:32	IA Vertices Count Report UDW Total number of vertices fetched by the VF stage. This count is updated for every input vertex as long as Statistics Enable is set in VF_STATE (see the Vertex Fetch Chapter in the 3D Volume.)
	31:0	IA Vertices Count Report LDW Total number of vertices fetched by the VF stage. This count is updated for every input vertex as long as Statistics Enable is set in VF_STATE (see the Vertex Fetch Chapter in the 3D Volume.)

IDLE Messaging Register for Blitter Engine

MSG_IDLE_BCS - IDLE Messaging Register for Blitter Engine				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	16			
Address:	0800Ch			
<p>Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.</p>				
DWord	Bit	Description		
0	15:6	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	5	<p>Flush and Block Acknowledgement</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Flush and Block Acknowledgement 1'b0 : Not flushed and blocked <default> 1'b1 : Unit has flushed and blocked its pipeline</p>	Access:	R/W
	Access:	R/W		
4	<p>Preparation for Reset Acknowledgement</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Go Acknowledgement 1'b0 : Go=0 Ack <default> 1'b1 : Go=1 Ack Requirement is that when Go=0 request is sent, the agent has to indicate busy before sending the Go=0 acknowledgement. It can only go idle again once Go=1 is received.</p>	Access:	R/W	
Access:	R/W			
3:0	<p>Idle Messaging</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Idle Messaging Bit[3] Secondary Pipe Clock Gating 1'b0 : Secondary pipe clock must be on <default> 1'b1 : Secondary pipe clock may be gated Bit[2] Primary Pipe Clock Gating 1'b0 : Primary pipe clock must be on <default> 1'b1 : Primary pipe clock may be gated</p>	Access:	R/W	
Access:	R/W			

MSG_IDLE_BCS - IDLE Messaging Register for Blitter Engine

		Bit[1] C6 Allowed 1'b0 : Do not allow GT to enter C6 <default> 1'b1 : GT may enter C6 Bit[0] Idle Indication 1'b0 : Pipe is busy <default> 1'b1 : Pipe is idle ** See "Valid Combinations for Idle Messaging" Table
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IDLE Messaging Register for Media0 Engine

MSG_IDLE_VCS0 - IDLE Messaging Register for Media0 Engine				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	16			
Address:	08004h			
<p>Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.</p>				
DWord	Bit	Description		
0	15:6	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	5	<p>Flush and Block Acknowledgement</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Flush and Block Acknowledgement 1'b0 : Not flushed and blocked <default> 1'b1 : Unit has flushed and blocked its pipeline</p>	Access:	R/W
	Access:	R/W		
4	<p>Preparation for Reset Acknowledgement</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Go Acknowledgement 1'b0 : Go=0 Ack <default> 1'b1 : Go=1 Ack Requirement is that when Go=0 request is sent, the agent has to indicate busy before sending the Go=0 acknowledgement. It can only go idle again once Go=1 is received.</p>	Access:	R/W	
Access:	R/W			
3:0	<p>Idle Messaging</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Idle Messaging Bit[3] Secondary Pipe Clock Gating 1'b0 : Secondary pipe clock must be on <default> 1'b1 : Secondary pipe clock may be gated Bit[2] Primary Pipe Clock Gating 1'b0 : Primary pipe clock must be on <default> 1'b1 : Primary pipe clock may be gated Bit[1]</p>	Access:	R/W	
Access:	R/W			

MSG_IDLE_VCS0 - IDLE Messaging Register for Media0 Engine

	<p>C6 Allowed 1'b0 : Do not allow GT to enter C6 <default> 1'b1 : GT may enter C6</p> <p>Bit[0] IDLE Indication - Media done 1'b0 : Pipe is busy <default> 1'b1 : Pipe is idle</p> <p>Refer to bits A024[10:9] for different Media turbo scenarios. ** See "Valid Combinations for Idle Messaging" Table</p>
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IDLE Messaging Register for Media1 Engine

MSG_IDLE_VCS1 - IDLE Messaging Register for Media1 Engine				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	16			
Address:	08008h			
<p>Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.</p>				
DWord	Bit	Description		
0	15:6	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	5	<p>Flush and Block Acknowledgement</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Flush and Block Acknowledgement 1'b0 : Not flushed and blocked <default> 1'b1 : Unit has flushed and blocked its pipeline</p>	Access:	R/W
	Access:	R/W		
4	<p>Preparation for Reset Acknowledgement</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Go Acknowledgement 1'b0 : Go=0 Ack <default> 1'b1 : Go=1 Ack Requirement is that when Go=0 request is sent, the agent has to indicate busy before sending the Go=0 acknowledgement. It can only go idle again once Go=1 is received.</p>	Access:	R/W	
Access:	R/W			
3:0	<p>Idle Messaging</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Idle Messaging Bit[3] Secondary Pipe Clock Gating 1'b0 : Secondary pipe clock must be on <default> 1'b1 : Secondary pipe clock may be gated Bit[2] Primary Pipe Clock Gating 1'b0 : Primary pipe clock must be on <default> 1'b1 : Primary pipe clock may be gated Bit[1]</p>	Access:	R/W	
Access:	R/W			

MSG_IDLE_VCS1 - IDLE Messaging Register for Media1 Engine

		<p>C6 Allowed 1'b0 : Do not allow GT to enter C6 <default> 1'b1 : GT may enter C6</p> <p>Bit[0] Idle Indication 1'b0 : Pipe is busy <default> 1'b1 : Pipe is idle</p> <p>** See "Valid Combinations for Idle Messaging" Table</p>
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IDLE Messaging Register for Render Engine

MSG_IDLE_CS - IDLE Messaging Register for Render Engine				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	08000h			
<p>Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.</p> <p>NOTE - GPGPU_ACTIVE and MEDIA_ACTIVE are context saved and restored; the other bits are cleared out before saving context</p>				
DWord	Bit	Description		
0	31:16	Context Save Mask <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>When context save is in progress, mask is forced to particular value to save off messages that need to be retained across an RC6 event. Currently for this register, the following fields are context saved and restored for an RC6 event: [7] GPGPU_ACTIVE [6] MEDIA_ACTIVE</p>	Access:	R/W
		Access:	R/W	
	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
	Access:	RO		
7	GPGPU Active Load Indication <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Active Load Indication - bits[7:6] of this register 2'b00 : Render load is being executed <default> 2'b01 : Media load is being executed 2'b10 : GPGPU load is being executed 2'b11 : Undefined gpmunit self-clears this bit upon sampling.</p>	Access:	R/W	
	Access:	R/W		
Media Active Load Indication <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Active Load Indication - bits[7:6] of this register 2'b00 : Render load is being executed <default> 2'b01 : Media load is being executed 2'b10 : GPGPU load is being executed</p>	Access:	R/W		
Access:	R/W			

MSG_IDLE_CS - IDLE Messaging Register for Render Engine

		2'b11 : Undefined gpmunit self-clears this bit upon sampling.		
	5	<p>Flush and Block Acknowledgement</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>Flush and Block Acknowledgement 1'b0 : Not flushed and blocked <default> 1'b1 : Unit has flushed and blocked its pipeline</p>	Access:	R/W
Access:	R/W			
	4	<p>Preparation for Reset Acknowledgement</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>Go Acknowledgement 1'b0 : Go=0 Ack <default> 1'b1 : Go=1 Ack Requirement is that when Go=0 request is sent, the agent has to indicate busy before sending the Go=0 acknowledgement. It can only go idle again once Go=1 is received. Also, Refer to the table in the description for bits A024[10:9]</p>	Access:	R/W
Access:	R/W			
	3:0	<p>Idle Messaging</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>Idle Messaging Bit[3] Secondary Pipe Clock Gating 1'b0 : Secondary pipe clock must be on <default> 1'b1 : Secondary pipe clock may be gated Bit[2] Primary Pipe Clock Gating 1'b0 : Primary pipe clock must be on <default> 1'b1 : Primary pipe clock may be gated Bit[1] C6 Allowed 1'b0 : Do not allow GT to enter C6 <default> 1'b1 : GT may enter C6 Bit[0] Idle Indication 1'b0 : Pipe is busy <default> 1'b1 : Pipe is idle ** See "Valid Combinations for Idle Messaging" Table Also, Refer to the table in the description for bits A024[10:9]</p>	Access:	R/W
Access:	R/W			

IDLE Messaging Register for VEBox

MSG_IDLE_VECS - IDLE Messaging Register for VEBox				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	16			
Address:	08010h			
<p>Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.</p>				
DWord	Bit	Description		
0	15:6	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	5	<p>Flush and Block Acknowledgement</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Flush and Block Acknowledgement 1'b0 : Not flushed and blocked <default> 1'b1 : Unit has flushed and blocked its pipeline</p>	Access:	R/W
	Access:	R/W		
4	<p>Preparation for Reset Acknowledgement</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Go Acknowledgement 1'b0 : Go=0 Ack <default> 1'b1 : Go=1 Ack Requirement is that when Go=0 request is sent, the agent has to indicate busy before sending the Go=0 acknowledgement. It can only go idle again once Go=1 is received.</p>	Access:	R/W	
Access:	R/W			
3:0	<p>Idle Messaging</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Idle Messaging Bit[3] Secondary Pipe Clock Gating 1'b0 : Secondary pipe clock must be on <default> 1'b1 : Secondary pipe clock may be gated Bit[2] Primary Pipe Clock Gating 1'b0 : Primary pipe clock must be on <default> 1'b1 : Primary pipe clock may be gated Bit[1]</p>	Access:	R/W	
Access:	R/W			

MSG_IDLE_VECS - IDLE Messaging Register for VEBox

	<p>C6 Allowed 1'b0 : Do not allow GT to enter C6 <default> 1'b1 : GT may enter C6</p> <p>Bit[0] Idle Indication 1'b0 : Pipe is busy <default> 1'b1 : Pipe is idle</p> <p>** See "Valid Combinations for Idle Messaging" Table</p>
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IDLE Messaging Register for Wi-Di

MSG_IDLE_WIN - IDLE Messaging Register for Wi-Di				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	16			
Address:	08014h			
<p>Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.</p>				
DWord	Bit	Description		
0	15:5	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	4	<p>Preparation for Reset Acknowledgement</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Go Acknowledgement 1'b0 : Go=0 Ack <default> 1'b1 : Go=1 Ack Requirement is that when Go=0 request is sent, the agent has to indicate busy before sending the Go=0 acknowledgement. It can only go idle again once Go=1 is received.</p>	Access:	R/W
Access:	R/W			
3:0	<p>Idle Messaging</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Idle Messaging Bit[3] Secondary Pipe Clock Gating 1'b0 : Secondary pipe clock must be on <default> 1'b1 : Secondary pipe clock may be gated Bit[2] Primary Pipe Clock Gating 1'b0 : Primary pipe clock must be on <default> 1'b1 : Primary pipe clock may be gated Bit[1] C6 Allowed 1'b0 : Do not allow GT to enter C6 <default> 1'b1 : GT may enter C6 Bit[0] Idle Indication 1'b0 : Pipe is busy <default></p>	Access:	R/W	
Access:	R/W			

MSG_IDLE_WIN - IDLE Messaging Register for Wi-Di

		1'b1 : Pipe is idle ** See "Valid Combinations for Idle Messaging" Table
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Idle Switch Delay

IDLEDLY - Idle Switch Delay		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	0223Ch	
Address:	1223Ch-1223Fh	
Name:	Idle Switch Delay	
ShortName:	IDLEDLY_VCSUNIT0	
Address:	1A23Ch-1A23Fh	
Name:	Idle Switch Delay	
ShortName:	IDLEDLY_VECSUNIT	
Address:	1C23Ch-1C23Fh	
Name:	Idle Switch Delay	
ShortName:	IDLEDLY_VCSUNIT1	
Address:	2223Ch-2223Fh	
Name:	Idle Switch Delay	
ShortName:	IDLEDLY_BCSUNIT	
<p>The IDLEDLY register contains an Idle Delay field which specifies the minimum number of microseconds allowed for command streamer to wait before a context is switched out leading to IDLE state in Execlist mode, i.e following this context switch there is no active element available in HW to execute. A default value of 0, means that by default, there is no restriction to wait on a context switch leading to IDLE. This register has no significance when Execlists are not enabled.</p>		
DWord	Bit	Description
0	31:21	Reserved
		Format: MBZ
	20:0	IDLE Delay
		Project: All Format: U21 Minimum number of micro-seconds allowed

Indirect Context Pointer

INDIRECT_CTX - Indirect Context Pointer							
Register Space:	MMIO: 0/2/0						
Project:	CHV, BSW						
Source:	PRM						
Default Value:	0x00000000						
Access:	R/W						
Size (in bits):	32						
Trusted Type:	1						
Address:	021C4h-021C7h						
Name:	Indirect Context Pointer						
ShortName:	INDIRECT_CTX_RCSUNIT						
Address:	121C4h-121C7h						
Name:	Indirect Context Pointer						
ShortName:	INDIRECT_CTX_VCSUNIT0						
Address:	1A1C4h-1A1C7h						
Name:	Indirect Context Pointer						
ShortName:	INDIRECT_CTX_VECSUNIT						
Address:	1C1C4h-1C1C7h						
Name:	Indirect Context Pointer						
ShortName:	INDIRECT_CTX_VCSUNIT1						
Address:	221C4h-221C7h						
Name:	Indirect Context Pointer						
ShortName:	INDIRECT_CTX_BCSUNIT						
<p>This register is used to program the indirect address to be executed between CS and SVG engine context if enabled. This will only get executed due to regular context save/restore and not during power restore. This register is part of the execution list context and will be executed per context. Only supported if execution list is enabled. There is no preempting workloads within this context.</p>							
Programming Notes							
<p>The following commands are not supported within Render CS indirect context:</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left;">Command Name</th> </tr> </thead> <tbody> <tr> <td>MI_WAIT_FOR_EVENT</td> </tr> <tr> <td>MI_SEMAPHORE_SIGNAL</td> </tr> <tr> <td>MI_ARB_CHECK</td> </tr> <tr> <td>MI_RS_CONTROL</td> </tr> <tr> <td>MI_REPORT_HEAD</td> </tr> </tbody> </table>		Command Name	MI_WAIT_FOR_EVENT	MI_SEMAPHORE_SIGNAL	MI_ARB_CHECK	MI_RS_CONTROL	MI_REPORT_HEAD
Command Name							
MI_WAIT_FOR_EVENT							
MI_SEMAPHORE_SIGNAL							
MI_ARB_CHECK							
MI_RS_CONTROL							
MI_REPORT_HEAD							
Source							
RenderCS							

INDIRECT_CTX - Indirect Context Pointer

MI_URB_ATOMIC_ALLOC		
MI_SUSPEND_FLUSH		
MI_TOPOLOGY_FILTER		
MI_RS_CONTEXT		
MI_SET_CONTEXT		
MI_URB_CLEAR		
MI_SEMAPHORE_WAIT in Memory Poll Mode is not supported.		
MI_BATCH_BUFFER_START		
MI_CONDITIONAL_BATCH_BUFFER_END		
MEDIA_OBJECT_WALKER		
GPGPU_WALKER		
3DPRIMITIVE		
3DSTATE_BINDING_TABLE_POINTERS_VS		
3DSTATE_BINDING_TABLE_POINTERS_HS		
3DSTATE_BINDING_TABLE_POINTERS_DS		
3DSTATE_BINDING_TABLE_POINTERS_GS		
3DSTATE_BINDING_TABLE_POINTERS_PS		
3DSTATE_GATHER_CONSTANT_VS		
3DSTATE_GATHER_CONSTANT_GS		
3DSTATE_GATHER_CONSTANT_HS		
3DSTATE_GATHER_CONSTANT_DS		
3DSTATE_GATHER_CONSTANT_PS		
3DSTATE_DX9_CONSTANTF_VS		
3DSTATE_DX9_CONSTANTF_HS		
3DSTATE_DX9_CONSTANTF_DS		
3DSTATE_DX9_CONSTANTF_GS		
3DSTATE_DX9_CONSTANTF_PS		
3DSTATE_DX9_CONSTANTI_VS		
3DSTATE_DX9_CONSTANTI_HS		
3DSTATE_DX9_CONSTANTI_DS		
3DSTATE_DX9_CONSTANTI_GS		
3DSTATE_DX9_CONSTANTI_PS		
3DSTATE_DX9_CONSTANTB_VS		
3DSTATE_DX9_CONSTANTB_HS		
3DSTATE_DX9_CONSTANTB_DS		

INDIRECT_CTX - Indirect Context Pointer

3DSTATE_DX9_CONSTANTB_GS		
3DSTATE_DX9_CONSTANTB_PS		
3DSTATE_DX9_LOCAL_VALID_VS		
3DSTATE_DX9_LOCAL_VALID_DS		
3DSTATE_DX9_LOCAL_VALID_HS		
3DSTATE_DX9_LOCAL_VALID_GS		
3DSTATE_DX9_LOCAL_VALID_PS		
3DSTATE_DX9_GENERATE_ACTIVE_VS		
3DSTATE_DX9_GENERATE_ACTIVE_HS		
3DSTATE_DX9_GENERATE_ACTIVE_DS		
3DSTATE_DX9_GENERATE_ACTIVE_GS		
3DSTATE_DX9_GENERATE_ACTIVE_PS		
3DSTATE_BINDING_TABLE_EDIT_VS		
3DSTATE_BINDING_TABLE_EDIT_GS		
3DSTATE_BINDING_TABLE_EDIT_HS		
3DSTATE_BINDING_TABLE_EDIT_DS		
3DSTATE_BINDING_TABLE_EDIT_PS		
3DSTATE_CONSTANT_VS		
3DSTATE_CONSTANT_GS		
3DSTATE_CONSTANT_PS		
3DSTATE_CONSTANT_HS		
3DSTATE_CONSTANT_DS		
MI_BATCH_BUFFER_END		

INDIRECT_CTX - Indirect Context Pointer

Workaround

Workaround: [Render CS Only][Execlist Mode of Scheduling]: SW must ensure arbitration is switched off while context restore is in progress for any given context. This is achieved by disabling arbitration by programming MI_ARB_ON_OFF to "Arbitration Disable" in RCS_INDIRECT_CTX buffer and by enabling back the arbitration by programming MI_ARB_ON_OFF to "Arbitration Enable" as the last command prior to MI_BATCH_END in the BB_PER_CTX_PTR buffer of every context submitted. Note that RCS_INDIRECT_CTX_OFFSET could be set to default value or any other legitimate value as per the programming notes of the register definition. Arbitration disabled by programming MI_ARB_ON_OFF (Arbitration Disabled) in RCS_INDIRECT_CTX buffer. Arbitration enabled by programming MI_ARB_ON_OFF (Arbitration Enabled) as the last command prior to MI_BATCH_BUFFER_END in BB_PER_CTX_PTR buffer. Additional Note: This WA need not be applied when it is guaranteed for no preemption to occur during execution of GPGPU workload. Preemption of GPGPU workload can be avoided by Bracketing the GPGPU workload with MI_ARB_ON_OFF (Arbitration Disable) and MI_ARB_ON_OFF (Arbitration Enable) command. MI_ARB_ON_OFF is a privileged command and can only be programmed in ring buffer or in privileged batch buffer (batch buffer in GGTT memory). Pending execlist submitted must not trigger preemption of the ongoing GPGPU workload due to following reasons First context of the pending execlist submitted is not the same as the ongoing GPGPU context. Force restore bit set for the submitted pending execlist.

DWord	Bit	Description					
0	31:6	<p>Indirect CS Context Address</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[31:6]</td> </tr> </table> <p>Pointer to the Context in memory to be executed as a batch.</p>	Format:	GraphicsAddress[31:6]			
	Format:	GraphicsAddress[31:6]					
5:0	<p>Size of Indirect CS Context</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>U6</td> </tr> </table> <p>This is the size of the Indirect Context for CS. This size supports up to 63 cache lines worth of commands where a cache line is 64B. If programmed to zero then the indirect fetch of the CS context is disabled.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>[0,63]</td> <td></td> </tr> </tbody> </table>	Format:	U6	Value	Name	[0,63]	
Format:	U6						
Value	Name						
[0,63]							

Instruction Parser Mode Register

INSTPM - Instruction Parser Mode Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00004080 [CHV:B, CHV:C, CHV:K] 0x00006080 [CHV:A]
Access:	R/W, RO
Size (in bits):	32
Trusted Type:	1
Address:	020C0h
Address:	120C0h-120C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VCSUNIT0
Address:	1A0C0h-1A0C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VECSUNIT
Address:	1C0C0h-1C0C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VCSUNIT1
Address:	220C0h-220C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_BCSUNIT
<p>The INSTPM register is used to control the operation of the Instruction Parser. Certain classes of instructions can be disabled (ignored) - often useful for detecting performance bottlenecks. Also, Synchronizing Flush operations can be initiated - useful for ensuring the completion (vs. only parsing) of rendering instructions.</p>	
Programming Notes	
<ul style="list-style-type: none"> • If an instruction type is disabled, the parser will read those instructions but not process them. • Error checking will be performed even if the instruction is ignored. • All Reserved bits are implemented. • This Register is saved and restored as part of Context. 	

DWord	Bit	Description									
0	31:16	Mask Bits									
		Format: Mask[15:0] Masks: These bits serve as write enables for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.									
	15	Reserved									
		Project: CHV, BSW									
		Access: RO Format: MBZ									
	14	14	Replay Mode								
			Project: CHV, BSW Format: U1 This field controls the granularity of the replay mechanism when coming back into a previously preempted context.								
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1h</td> <td>Object Level Preemption [Default]</td> <td>Object Level. Preemption is done on an Object Level Boundary in VF. Objects send down by VF are completely rendered. Pipeline is flushed before switching to the next context. On resubmission of the context VF starts parsing from the object where it got preempted last time.</td> </tr> <tr> <td>0h</td> <td></td> <td>Drawcall Level. Pipeline is flushed before switching to the next context. Commands parsed are committed to completing before a context switch.</td> </tr> </tbody> </table>	Value	Name	Description	1h	Object Level Preemption [Default]	Object Level. Preemption is done on an Object Level Boundary in VF. Objects send down by VF are completely rendered. Pipeline is flushed before switching to the next context. On resubmission of the context VF starts parsing from the object where it got preempted last time.	0h		Drawcall Level. Pipeline is flushed before switching to the next context. Commands parsed are committed to completing before a context switch.
		Value	Name	Description							
		1h	Object Level Preemption [Default]	Object Level. Preemption is done on an Object Level Boundary in VF. Objects send down by VF are completely rendered. Pipeline is flushed before switching to the next context. On resubmission of the context VF starts parsing from the object where it got preempted last time.							
0h			Drawcall Level. Pipeline is flushed before switching to the next context. Commands parsed are committed to completing before a context switch.								
Programming Notes											
This bit must be set to 0 prior to any 3DPRIMITIVE using trifan, polygon, lineloop or quadstrip topology. This bit must be set to 0 prior to any 3DPRIMITIVE using linestrip_adjacency and 3dstate_GS.enable is set to 1.											
14:13		Reserved									
		Default Value: 11b									
	Project: CHV, BSW Format: Must Be One										
13	Reserved										
	Project: CHV, BSW Format: Must Be One										
12	Reserved										
	Project: CHV, BSW										
11	CLFLUSH Toggle										

DWord	Bit	Description	
		Project: CHV, BSW	
		Access: RO	
		Format: U1	
			This bit changes polarity each time the MI_CLFLUSH command completes. This bit is Read Only.
	10	Reserved	
	9:8	Reserved	
		Project: CHV, BSW	
		Format: MBZ	
	7	Force Sync Command Ordering	
		Default Value: 1b	
		Project: CHV, BSW	
		Format: Enable	
			By default, driver/OS synchronization commands (MI_STORE_DATA_IMM, for instance) can execute out of order with respect to 3D state and 3D primitive commands. When set, this bit forces ordering of these commands. See section 3.2.2 for a list of these commands.
	6	CONSTANT_BUFFER Address Offset Disable	
		Project: CHV, BSW	
		Format: Disable	
		When this bit is clear, the 3DSTATE_CONSTANT_* Buffers' Starting Address is used as a DynamicStateOffset. That is, it serves as an offset from the Dynamic State Base Address. Accesses will be subject to Dynamic State bounds checking. When this bit is set, the 3DSTATE_CONSTANT_* Buffers' Starting Address is used as a true GraphicsAddress (not an offset). No bounds checking will be performed during access.	
5	Reserved		
	Project: CHV, BSW		
	Format: MBZ		
4	Reserved		
	Project: CHV, BSW		
3	Media Instruction Disable		
	Project: CHV, BSW		
	Format: U1		
		This bit instructs the Renderer instruction parser to parse and error-check Media instructions, but not execute them. Format = Disable	

DWord	Bit	Description	
	2	3D Rendering Instruction Disable	
		Project:	CHV, BSW
		Format:	U1
			This bit instructs the Renderer instruction parser to parse and error-check 3D Rendering instructions, but not execute them. This bit must always be set by software if 3D State Instruction Disable is set. Setting this bit without setting 3D State Instruction Disable is allowed. Format = Disable
	1	3D State Instruction Disable	
		Project:	CHV, BSW
		Format:	Disable
	0	Texture Palette Load Instruction Disable	
Project:		CHV, BSW	
Format:		U1	
		This bit instructs the Renderer instruction parser to parse and error-check Texture Palette Load instructions, but not execute them. Format = Disable	

Internal GAM State

INTSTATE - Internal GAM State		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	040C0h	
DWord	Bit	Description
0	31:0	Reserved

INTERRUPT LINE

INTRLINE - INTERRUPT LINE			
Register Space:	PCI: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000100		
Size (in bits):	16		
Address:	0003Ch		
<p>3C - Interrupt. This register is programmed by SBIOS. It is not used by the graphics/display driver. This 8-bit register is used to communicate interrupt line routing information. It is read/write and must be implemented by the device. POST software will write the routing information into this register as it initializes and configures the system.</p> <p>The value in this register tells which input of the system interrupt controller(s) the device's interrupt pin is connected to. The device itself does not use this value, rather it is used by device drivers and operating systems to determine priority and vector information.</p> <p>3D - Interrupt. This register is programmed by SBIOS. It is not used by the graphics/display driver</p>			
DWord	Bit	Description	
0	15:8	INTERRUPT_PIN	
		Default Value:	01h
		Access:	RO
		IPIN: Value indicates which interrupt pin this device uses. 01h: INTA	
	7:0	INTRLINE	
		Default Value:	00h
		Access:	R/W
		ILIN: BIOS written value to communicate interrupt line routing information to the device driver. Used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates to which input of the system interrupt controller the device's interrupt pin is connected.	

Interrupt Mask Register

IMR - Interrupt Mask Register														
Register Space:	MMIO: 0/2/0													
Project:	CHV, BSW													
Source:	RenderCS													
Default Value:	0xFFFFFFFF													
Access:	R/W, RO													
Size (in bits):	32													
Address:	020A8h													
Address:	120A8h-120ABh													
Name:	Interrupt Mask Register													
ShortName:	IMR_VCSUNIT0													
Address:	1A0A8h-1A0ABh													
Name:	Interrupt Mask Register													
ShortName:	IMR_VECSUNIT													
Address:	1C0A8h-1C0ABh													
Name:	Interrupt Mask Register													
ShortName:	IMR_VCSUNIT1													
Address:	220A8h-220ABh													
Name:	Interrupt Mask Register													
ShortName:	IMR_BCSUNIT													
<p>The IMR register is used by software to control which Interrupt Status Register bits are masked or unmasked. Unmasked bits will be reported in the IIR, possibly triggering a CPU interrupt, and will persist in the IIR until cleared by software. Masked bits will not be reported in the IIR and therefore cannot generate CPU interrupts.</p>														
DWord	Bit	Description												
0	31:0	<p>Interrupt Mask Bits</p> <p>Format: InterruptMask[32] Refer to the Interrupt Control Register section for bit definitions.</p> <p>This field contains a bit mask which selects which interrupt bits (from the ISR) are reported in the IIR. Reserved bits in the Interrupt Control Register are RO.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>FFFF FFFFh</td> <td>[Default]</td> <td></td> </tr> <tr> <td>0h</td> <td>Not Masked</td> <td>Will be reported in the IIR</td> </tr> <tr> <td>1h</td> <td>Masked</td> <td>Will not be reported in the IIR</td> </tr> </tbody> </table>	Value	Name	Description	FFFF FFFFh	[Default]		0h	Not Masked	Will be reported in the IIR	1h	Masked	Will not be reported in the IIR
Value	Name	Description												
FFFF FFFFh	[Default]													
0h	Not Masked	Will be reported in the IIR												
1h	Masked	Will not be reported in the IIR												

IOBAR

IOBAR - IOBAR		
Register Space:	PCI: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000001	
Size (in bits):	32	
Address:	00020h	
<p>I/O Base Address. This is used only by SBIOS. This register is the base address for the MMIO_INDEX and MMIO_DATA registers.</p> <p>This register provides the Base offset of the I/O registers within Device #2. Access to the 8Bs of IO space is allowed in PM state D0 when IO Enable (PCICMD bit 0) set. Access is disallowed :</p> <ul style="list-style-type: none"> * in PM states D1-D3 or * if IO Enable is clear or * if Device #2 is turned off or * if Internal graphics is disabled thru the fuse or fuse override mechanisms. <p>Note that access to this IO BAR is independent of VGA functionality within Device #2. If accesses to this IO bar is allowed then the GMCH claims all 8, 16 or 32 bit IO cycles from the CPU that falls within the 8B claimed.</p>		
DWord	Bit	Description
0	31:16	RESERVED
		Default Value: 0000h
	Access: RO	
	Reserved	
15:6	BASE_ADDRESS	
	Default Value: 0000h	
	Access: R/W	
BA: Set by the OS, these bits correspond to address signals [15:6]. IOBAR is to be used for both GTLC register programming and GTT table programming. This is an indirect access method.		
5:1	RESERVED	
	Default Value: 0h	
Access: RO		
0	RESOURCE_TYPE RTE	
	Default Value: 1b	
	Access: RO	
Indicates a request for I/O space		

L3 Bank Status

L3STAT - L3 Bank Status					
Register Space:	MMIO: 0/2/0				
Project:	CHV, BSW				
Source:	PRM				
Default Value:	0x00000000				
Size (in bits):	32				
Address:	0B128h				
L3 Status register					
DWord	Bit	Description			
0	31	L3 Fill Access Status bit <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%;">RO</td> </tr> </table> <p>This register is Hardware Set and Clear. Set condition: set when the first command is seen on LTCC-LTCD interface. Reset condition: reset when the first Pipeline Flush command is seen on the LTCC-LTCD interface. Reset condition: This Flag will be reset only if we have atleast 1 modified line in the cache written by DC client.</p>	Access:	RO	
	Access:	RO			
30:0	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td style="width: 50%;">CHV, BSW</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Project:	CHV, BSW	Access:	RO
Project:	CHV, BSW				
Access:	RO				

L3CD Error Status register 1

L3CDERRST - L3CD Error Status register 1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000080	
Size (in bits):	32	
Address:	0B1F0h	
DWord	Bit	Description
0	31:25	Reserved Access: RO
	24	Double bit ECC error detected Default Value: 0b Access: R/W One Clear Indicates if bank detected a double bit ECC error. When Itcd_lbcf_ecc_2bit_err_valid is set.
	23:14	Parity row address error Default Value: 0000000000b Access: R/W One Clear Data array address which has parity B1. Report the data array address which has the Error. Itcd_lbcf_parity_err_rownum[9:0].Once set by HW, it can be cleared only by MMIO Write of 1 to this register bit 13. Driver needs to write 1 to clear this bit.
	13	Parity Error Valid Access: R/W One Clear Parity Error valid. Report the Parity Error. Itcd_lbcf_parity_err_valid. Once set by HW, it can be cleared only by MMIO Write of 1 to this register bit 13. Driver needs to write 1 to clear this bit. when Itcd_lbcf_parity_err_valid is asserted, lbcf generates interrupt to Itiseqsl lbcf_litiseqsl_parity_intr.
	12:11	Parity error bank number Access: R/W One Clear bank number which has parity error. Report the bank no. which has the Error. Itcd_lbcf_parity_err_banknum[1:0].Once set by HW, it can be cleared only by MMIO Write of 1 to this register bit 13. Driver needs to write 1 to clear this bit.

L3CDERRST - L3CD Error Status register 1					
10:8	<p>Parity Error sub-bank no</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Access:</td> <td>R/W One Clear</td> </tr> </table> <p>Parity Error in sub bank: ltcd0_lbcf_parity_err_subbanknum[2:0].Once set by HW, it can be cleared only by MMIO Write of 1 to this register bit 13. Driver needs to write 1 to clear this bit.</p>	Access:	R/W One Clear		
Access:	R/W One Clear				
7	<p>Parity report enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Default Value:</td> <td>1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Parity report enable (LCPRTYRPTEN): lbcf_csr_lc_parity_report_en. This is the parity reporting enable, by default it is enabled. When enabled parity is reported by ltcd to sarb. When disabled by driver, ltcd should not send out any parity error to SARB. Driver needs to write 1 to clear this bit.</p>	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				
6:0	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Access:</td> <td>RO</td> </tr> </table>	Access:	RO		
Access:	RO				

L3 Control Register

L3CNTLREG - L3 Control Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000 CHV, BSW			
Access:	R/W			
Size (in bits):	32			
Address:	07034h			
Programming Notes		Project		
The L3 allocation programming should assign all ways of the cache with no left over ways. Refer to L3 section for the recommended settings.				
Any L3 configuration change that reduces the data cache allocation when strong IA coherency is used requires the full flush of L3 prior to the programming update. An explicit or implicit flush of L3 (DC Flush) through the command streamer doesn't result in flushing/invalidating the IA Coherent lines from L3. However this can be achieved by setting the "Pipe line flush Coherent lines" control bit in the "L3SQCREG4" register.				
SLM comes up in an in-consistent state post reconfiguration and must be initialized by the driver for proper parity generation		CHV, BSW		
DWord	Bit	Description		
0	31:25	All L3 Client Pool		
		Project: All		
		Access: R/W		
		Number of ways allocated for the all client pool. This is a combined pool for all clients.		
		Value	Name	Project
		30h	[Default]	CHV, BSW
		Programming Notes		
		When this field is non-zero, DC Way Assignment and Read Only Client Pool should be 0KB. Odd number values are not allowed. Please refer to L3 Section with Allocation and Programming for recommended settings.		
		24:18		DC Way Assignment
				Project: All
Access: R/W				
Number of ways allocated for DC. Note this allocation is only for DC data types.				
Programming Notes				
Note: This field must be 0KB if All L3 Client Pool is non-zero. Odd number values are not allowed. Please refer to L3 HAS for valid programming values				

L3CNTLREG - L3 Control Register

17:11	Read Only Client Pool			
	Project:	All		
	Access:	R/W		
	Number of ways allocated for Read Only L3 clients. This is a combined pool for all Read Only clients.			
	Programming Notes			
	Note: This field must be 0KB if All L3 Client Pool is non-zero. Odd number values are not allowed. Please refer to L3 HAS for valid programming values			
10	Reserved			
	Access:	R/W		
	Format:	PBC		
9	Error Detection Behavior Control			
	Project:	CHV, BSW		
	Access:	R/W		
	Format:	Enable		
	The L3 error detection can be enabled to hang the GPU on a non-recoverable error due to SER type events. Such option will be used when corresponding context has data consistency requirements. Once error detection is enabled, s/w has to initialize URB or SLM to all 0's (based on usage model) prior to execution of the workload. Initialization is required to clean up the error detection logic and syndrome tracking.			
	Value	Name	Description	Project
	0h	[Default]	RTL does not hang on parity errors or double bit error	CHV, BSW
	1h		RTL enforces a hang on parity errors or double bit error	CHV, BSW
8	GPGPU L3 Credit Mode Enable			
	Project:	All		
	Access:	R/W		
	Format:	Enable		
	This bit is required to be enabled under GPGPU workloads to provide the MAX latency coverage from L3 cache. It will override the registers 0xB100[18:14] and 0xB100[23:19], to 0 and the maximum value respectively.			
7:1	URB Allocation			
	Project:	All		
	Access:	R/W		
	Number of ways allocated for URB usage			
	Value	Name	Project	
	30h	[Default]	CHV, BSW	
	Programming Notes			
	Odd number values are not allowed. Please refer to L3 HAS for valid programming values			

L3CNTLREG - L3 Control Register							
0	<p>SLM Mode Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>When enabled, a 64KB (per bank) region of L3 is reserved for SLM.</p>	Project:	All	Access:	R/W	Format:	Enable
Project:	All						
Access:	R/W						
Format:	Enable						

L3 Control Register1

L3CNTLREG1 - L3 Control Register1						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x8C47FF80 CHV, BSW					
Size (in bits):	32					
Address:	0B10Ch					
DWord	Bit	Description				
0	31:28	Data Fifo Depth Control				
		Access: R/W				
		Data Fifo Depth Control (TS mode). Value cannot be zero for normal operation. lbcf_csr_lc_datafifo_depth[3:0].				
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>1000b</td> <td>[Default]</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Value	Name	Project	1000b
Value	Name	Project				
1000b	[Default]	CHV, BSW				
27:24		Data Clock off time				
		Default Value: 1100b				
		Access: R/W				
		Data Clock off time (DATACLKOFF): Data Clock off time - Data block is shut off after these many number of clocks programmed in this register bits. lbcf_csr_lc_dataclkoff_time[3:0].Min value to be 4'h0100. It should be between 4'h4 : 4'hf.				
23:20		TAG CLK OFF TIME				
		Default Value: 0100b				
		Access: R/W				
19		L3 Aging Disable Bit				
		Default Value: 0b				
		Access: R/W				
		L3 Aging Disable Bit (L3AGDIS): Aging Disable. lbcf_csr_lc_agingdis.				
18:15		Fill aging				
		Default Value: 1111b				

L3CNTLREG1 - L3 Control Register1

	<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>Fill aging (L3AGF): Aging Counter for Fill. lbcf_csr_lc_fill_aging_cnt[3:0].If bit B103.19 is 0 then this register value has to be nonzero.</p>	Access:	R/W				
Access:	R/W						
14:11	<p>Aging Counter for Read 1 Port</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1111b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Aging Counter for Read 1 Port (L3AGR1): Aging Counter for Read 1 Port. lbcf_csr_lc_r1_aging_cnt[3:0].If bit B103.19 is 0 then this register value has to be nonzero.</p>	Default Value:	1111b	Access:	R/W		
Default Value:	1111b						
Access:	R/W						
10:7	<p>L3 Aging Counter for R0</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1111b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>L3 Aging Counter for R0 (L3AGR0): Aging Counter for R0 Port. lbcf_csr_lc_r0_aging_cnt[3:0].If bit B103.19 is 0 then this register value has to be nonzero.</p>	Default Value:	1111b	Access:	R/W		
Default Value:	1111b						
Access:	R/W						
6:0	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">000000b</td> </tr> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved.</p>	Default Value:	000000b	Project:	CHV, BSW	Access:	RO
Default Value:	000000b						
Project:	CHV, BSW						
Access:	RO						

L3 LRA 0

L3_LRA_0 - L3 LRA 0			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x0E037C00		
Size (in bits):	32		
Exists If:	Device[Platform] == 'Client'		
Address:	04A10h		
DWord	Bit	Description	
0	31:30	L3	
		Default Value:	00b
		Access:	R/W
		Which LRA should L3 use.	
	29:20	L3 LRA1 Min	
		Default Value:	0011100000b
		Access:	R/W
		Minimum value of programmable LRA1.	
	19:10	L3 LRA0 Max	
		Default Value:	0011011111b
		Access:	R/W
		Maximum value of programmable LRA0.	
9:0	L3 LRA0 Min		
	Default Value:	0000000000b	
	Access:	R/W	
	Minimum value of programmable LRA0.		

L3 LRA 0 GPGPU

L3_LRA_0_GPGPU - L3 LRA 0 GPGPU			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x0400FC00		
Size (in bits):	32		
Address:	04DD0h		
DWord	Bit	Description	
0	31:30	L3 GPGPU	
		Default Value: 00b	
		Access: R/W	
		Which LRA should L3 use.	
	29:20	L3 LRA1 Min GPGPU	
		Default Value: 0001000000b	
		Access: R/W	
		Minimum value of programmable LRA1.	
	19:10	L3 LRA0 Max GPGPU	
		Default Value: 0000111111b	
		Access: R/W	
		Maximum value of programmable LRA0.	
	9:0	L3 LRA0 Min GPGPU	
		Default Value: 0000000000b	
		Access: R/W	
		Minimum value of programmable LRA0.	

L3 LRA 1

L3_LRA_1 - L3 LRA 1			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x67F701BF		
Size (in bits):	32		
Exists If:	Device[Platform] == 'Client'		
Address:	04A14h		
DWord	Bit	Description	
0	31:30	DC	
		Default Value:	01b
		Access:	R/W
		Which LRA should DC use.	
	29:20	L3 LRA2 Max	
		Default Value:	1001111111b
		Access:	R/W
		Maximum value of programmable LRA2.	
	19:10	L3 LRA2 Min	
		Default Value:	0111000000b
		Access:	R/W
		Minimum value of programmable LRA2.	
9:0	L3 LRA1 Max		
	Default Value:	0110111111b	
	Access:	R/W	
	Maximum value of programmable LRA1.		

L3 LRA 1 GPGPU

L3_LRA_1_GPGPU - L3 LRA 1 GPGPU			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x5FF6C1AF		
Size (in bits):	32		
Address:	04DD4h		
DWord	Bit	Description	
0	31:30	DC GPGPU	
		Default Value:	01b
		Access:	R/W
		Which LRA should DC use.	
	29:20	L3 LRA2 Max GPGPU	
		Default Value:	0111111111b
		Access:	R/W
		Maximum value of programmable LRA2.	
	19:10	L3 LRA2 Min GPGPU	
		Default Value:	0110110000b
		Access:	R/W
		Minimum value of programmable LRA2.	
9:0	L3 LRA1 Max GPGPU		
	Default Value:	0110101111b	
	Access:	R/W	
	Maximum value of programmable LRA1.		

L3 LRA 2

L3_LRA_2 - L3 LRA 2					
Register Space:	MMIO: 0/2/0				
Project:	CHV, BSW				
Source:	PRM				
Default Value:	0x00000002				
Size (in bits):	32				
Exists If:	Device[Platform] == 'Client'				
Address:	04A18h				
DWord	Bit	Description			
0	31:2	Reserved			
		<table border="1" style="width: 100%;"> <tr> <td style="width: 40%;">Default Value:</td> <td>00000000000000000000000000000000b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	00000000000000000000000000000000b	Access:
	Default Value:	00000000000000000000000000000000b			
	Access:	RO			
1:0	Texture				
	<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>10b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Which LRA should Texture use.</p>	Default Value:	10b	Access:	R/W
Default Value:	10b				
Access:	R/W				

L3 LRA 2 GPGPU

L3_LRA_2_GPGPU - L3 LRA 2 GPGPU		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000002	
Size (in bits):	32	
Address:	04DD8h	
DWord	Bit	Description
0	31:2	Reserved
		Default Value: 0000000000000000000000000000000b
		Access: RO
	1:0	Texture GPGPU
		Default Value: 10b
		Access: R/W
		Which LRA should Texture use.

L3 LRA 0 3D

L3_LRA_0_3D - L3 LRA 0 3D			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x0400FC00		
Size (in bits):	32		
Address:	04A10h		
DWord	Bit	Description	
0	31:30	L3 3D	
		Default Value:	00b
		Access:	R/W
		Which LRA should L3 use.	
	29:20	L3 LRA1 Min 3D	
		Default Value:	0001000000b
		Access:	R/W
		Minimum value of programmable LRA1.	
	19:10	L3 LRA0 Max 3D	
		Default Value:	0000111111b
		Access:	R/W
		Maximum value of programmable LRA0.	
	9:0	L3 LRA0 Min 3D	
		Default Value:	0000000000b
		Access:	R/W
		Minimum value of programmable LRA0.	

L3 LRA 1 3D

L3_LRA_1_3D - L3 LRA 1 3D							
Register Space:	MMIO: 0/2/0						
Project:	CHV, BSW						
Source:	PRM						
Default Value:	0x5FF2408F CHV, BSW						
Size (in bits):	32						
Address:	04A14h						
DWord	Bit	Description					
0	31:30	DC 3D					
		Default Value:	01b				
		Access:	R/W				
		Which LRA should DC use.					
	29:20	L3 LRA2 Max 3D					
		Access:	R/W				
		Maximum value of programmable LRA2.					
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>011111111b</td> <td>[Default]</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Value	Name	Project	011111111b	[Default]
	Value	Name	Project				
	011111111b	[Default]	CHV, BSW				
	19:10	L3 LRA2 Min 3D					
		Default Value:	0010010000b				
		Access:	R/W				
		Minimum value of programmable LRA2.					
	9:0	L3 LRA1 Max 3D					
		Default Value:	0010001111b				
Access:		R/W					
Maximum value of programmable LRA1.							

L3 LRA 2 3D

L3_LRA_2_3D - L3 LRA 2 3D			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW, :GT2:B		
Source:	PRM		
Default Value:	0x00000002		
Size (in bits):	32		
Address:	04A18h		
DWord	Bit	Description	
0	31:2	Reserved	
		Default Value:	0000000000000000000000000000000b
		Access:	RO
	1:0	Texture 3D	
		Default Value:	10b
		Access:	R/W
		Which LRA should Texture use.	

L3 Messaging Register

MSG_L3_LPFC - L3 Messaging Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	16			
Address:	08038h			
<p>Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.</p>				
DWord	Bit	Description		
0	15:2	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%;">RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	1	<p>Acknowledge that L3 Unblock Completed</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%;">R/W</td> </tr> </table> <p>Acknowledge that L3 Unblock Completed 1'b0 : L3 unblock not complete yet (default) 1'b1 : L3 unblock has completed gpmunit self-clears this bit upon sampling.</p>	Access:	R/W
Access:	R/W			
0	<p>Acknowledge that L3 Flush and Block Completed</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%;">R/W</td> </tr> </table> <p>Acknowledge that L3 Flush and Block Completed 1'b0 : L3 flush and block not complete yet (default) 1'b1 : L3 flush and block has completed gpmunit self-clears this bit upon sampling.</p>	Access:	R/W	
Access:	R/W			

L3 SLM Register

L3SLMREG - L3 SLM Register					
Register Space:	MMIO: 0/2/0				
Project:	CHV, BSW				
Source:	PRM				
Default Value:	0x40000000				
Size (in bits):	32				
Address:	0B110h				
DWord	Bit	Description			
0	31	Disable Periodic SLM/SQ slot allocation			
		<table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Disable Periodic SLM/SQ slot allocation: When <code>cfg_lslm_livelock_fairarb_dis=1</code> lslm unit always has the higher priority and <code>lslm_lsqc_block</code> to <code>lsqcunit</code> is asserted as long as there are requests in SLM FIFO. <code>lbcf_csr_lslm_livelock_fairarb_dis</code>.</p>	Default Value:	0b	Access:
	Default Value:	0b			
	Access:	R/W			
30:26	LSLM_SQ_PENDING_MAX				
	<table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>10000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>If lslmunit has read data to be sent to lcbunit this <code>cfg</code> register specifies the maximum number of clocks for which LSLMunit can block SQ request from being sent o lcbunit. Default value = 8. Value cannot be zero. <code>lbcf_csr_lslm_sqpend_max[4:0]</code>.</p>	Default Value:	10000b	Access:	R/W
Default Value:	10000b				
Access:	R/W				
25		LSLM address disable			
		<table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Default Value:	0b	Access:
	Default Value:	0b			
	Access:	R/W			
Description					
<p>0 - Enable b2b addr matching fix. lslmunit should not block the cycle in fifo if there is a match in the pipeline. 1 - Disable b2b addr matching fix. lslmunit should block the cycle in fifo if there is a match in the pipeline. <code>lbcf_csr_lslm_same_addr_dis</code>. Default = 0.</p> <p>Set this bit to 1'b1 to workaround Atomic b2b bug on SLM for CHV, BSW A-step only.</p>					
24:0	Reserved				
	<table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO		
Access:	RO				

L3 SQC register 4

L3SQCREG4 - L3 SQC register 4						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x40400000 CHV, BSW					
Size (in bits):	32					
Address:	0B118h					
DWord	Bit	Description				
0	31	Reserved				
	30	L3SQ URB Read CAM Match Disable				
		<table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">1b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>L3SQ URB Read CAM Match Disable (SQURBRDCAMDIS): Disables the L3SQ Cam Match ability for URB Reads. By disabling, this allows a performance mode where URB reads are not dependent upon one another but only on any previous URB writes to the same address. This allows many URB reads to the same cacheline at any given time instead of serializing the requests. 1 = URB Read CAM matching is disabled; multiple URB reads to the same cacheline are allowed to be concurrent (default). 0 = URB Read CAM matching is enabled; multiple URB reads to the same cacheline are serialized. lbcf_csr_lsqc_urbrdcam_dis.</p>	Default Value:	1b	Access:	R/W
Default Value:	1b					
Access:	R/W					
29:28	Traffic regulation in LSQC for URB lookup traffic					
		<table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">00b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>Traffic regulation in LSQC for URB lookup traffic (URB lookups are issued to ltcc these many clocks apart). 00b - Continuous. 01b - 4 clocks apart. 10b - 8 clocks apart. 11b - 16 clocks apart. lbcf_lsqc_urb_traffic.</p>	Default Value:	00b	Access:	R/W
		Default Value:	00b			
	Access:	R/W				
27	LQSC RO PERF DIS					
		<table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>Default: 0. when set, RO performance mode is disabled and all Reads proceed only after Parent recycles. lbcf_csr_lsqc_roperf_dis.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					

L3SQCREG4 - L3 SQC register 4

26	<p>Order Cam Snp Reject</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Default: 0. when set, all slots resulting in matches to snp addr result in snprsp as REJECT instead of MISS. lbcf_csr_lsqc_ordercam_snpreject.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
25	<p>LQSC RW PERF DIS</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Default: 0. 0: Performance mode is enabled. when set, Rd to RW performance mode is disabled and all cycles proceed only after Parent recycles. lbcf_csr_lsqc_rwperf_dis.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
24	<p>LSQC read rtn local crdt pre-consume disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>0 - Default, LSQD consumes the LNE local slice credit when read return pending. 1 - LSQD consumes read rtn credit in the clock it is ready to send read return data. lbcf_csr_lsqc_rdtrn_precredit_dis.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
23	<p>LSQC Mem Write sqcam HITM response disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>0 - Default. 1 - This disables any Memory Write from cache with HitM tag response to respond for SQCAMs. lbcf_csr_lsqc_sqcam_l3tagrsphitm_dis.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
22	<p>Non-IA coherent atomics enable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>0: Atomics in GTI. 1: Atomics in L3 (non-IA atomic) (default). lbcf_csr_lsqc_glblatmcs_l3. Value of this bit should be same as LNCF register bit 0xb008[0]. Value of this bit should be same as LBCF register bit 0xb11c[8].</p>	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				

L3SQCREG4 - L3 SQC register 4

21	Pipe line flush Coherent lines	
	Default Value:	0b
	Project:	CHV, BSW
	Access:	R/W
<p>1: Treat pipeline flush as invalidating even coherent lines along with non coherent lines . 0: Flush invalidates non coherent lines only. lbcf_csr_lsqc_pipeflush_coh.</p>		
20:0	Reserved	
	Project:	CHV, BSW
	Access:	RO

L3 SQC registers 1

L3SQCREG1 - L3 SQC registers 1							
Register Space:	MMIO: 0/2/0						
Project:	CHV, BSW						
Source:	PRM						
Default Value:	0x00810000 CHV, BSW						
Size (in bits):	32						
Address:	0B100h						
DWord	Bit	Description					
0	31:24	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Access:</td> <td style="text-align: center;">RO</td> </tr> </table> <p>Reserved.</p>	Access:	RO			
	Access:	RO					
23:19	<p>L3SQ General Priority Credit Initialization</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td> <p>L3SQ General Priority Credit Initialization (SQGPCI): Number of general and high priority credits that SQ presents to L3 Arbiter blocks This inherently also determines the depth of the SQ; reduce the number of credits and SQ uses fewer slots. Any value not listed here is considered Reserved. Gen priority credits is always greater than high priority credits. When this register is programmed through KMD, the crclk DOP clk gating should be disabled before the programming and be enabled ~100 clocks after the programming is done. Value # General Credits 00000b 0 00001b 2 00010b 4 00011b 6 00100b 8 00101b 10 00110b 12 00111b</p> </td> </tr> </tbody> </table>	Project:	CHV, BSW	Access:	R/W	Description	<p>L3SQ General Priority Credit Initialization (SQGPCI): Number of general and high priority credits that SQ presents to L3 Arbiter blocks This inherently also determines the depth of the SQ; reduce the number of credits and SQ uses fewer slots. Any value not listed here is considered Reserved. Gen priority credits is always greater than high priority credits. When this register is programmed through KMD, the crclk DOP clk gating should be disabled before the programming and be enabled ~100 clocks after the programming is done. Value # General Credits 00000b 0 00001b 2 00010b 4 00011b 6 00100b 8 00101b 10 00110b 12 00111b</p>
Project:	CHV, BSW						
Access:	R/W						
Description							
<p>L3SQ General Priority Credit Initialization (SQGPCI): Number of general and high priority credits that SQ presents to L3 Arbiter blocks This inherently also determines the depth of the SQ; reduce the number of credits and SQ uses fewer slots. Any value not listed here is considered Reserved. Gen priority credits is always greater than high priority credits. When this register is programmed through KMD, the crclk DOP clk gating should be disabled before the programming and be enabled ~100 clocks after the programming is done. Value # General Credits 00000b 0 00001b 2 00010b 4 00011b 6 00100b 8 00101b 10 00110b 12 00111b</p>							

L3SQCREG1 - L3 SQC registers 1

	<p>14 01000b 16 01001b 18 01010b 20 01011b 22 01100b 24 (default) 01101b 26 01110b 28 01111b 30 10000b 32 Other values are not possible. Need to go up to 32 credits. lbcf_csr_lsqc_gen_credit_init[4:0].</p>						
	<p>34 10010 36 10011 38 10100 40 Other values are not possible. ^M need to go upto 40 credits</p>						
	<table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th style="width: 33%;">Value</th> <th style="width: 33%;">Name</th> <th style="width: 33%;">Project</th> </tr> </thead> <tbody> <tr> <td>10000b</td> <td>[Default]</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Value	Name	Project	10000b	[Default]	CHV, BSW
Value	Name	Project					
10000b	[Default]	CHV, BSW					
18:14	<p>L3SQ High Priority Credit Initialization</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td>00100b</td> </tr> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>L3SQ High Priority Credit Initialization (SQHPCI): Number of general and high priority credits that SQ presents to L3 Arbiter blocks. This inherently also determines the depth of the SQ; reduce the number of credits and SQ uses fewer slots. Any value not listed here is considered Reserved. gen priority credits is always greater than high priority credits.</p>	Default Value:	00100b	Project:	CHV, BSW	Access:	R/W
Default Value:	00100b						
Project:	CHV, BSW						
Access:	R/W						

L3SQCREG1 - L3 SQC registers 1

		<p>When this register is programmed through KMD, the crclk DOP clk gating should be disabled before the programming and be enabled ~100 clocks after the programming is done.</p> <p>Value</p> <p># High Pri Credits</p> <p>00000b 0</p> <p>00001b 2</p> <p>00010b 4</p> <p>00011b 6</p> <p>00100b 8 (default)</p> <p>00101b 10</p> <p>00110b 12</p> <p>00111b 14</p> <p>01000b 16</p> <p>01001b 18</p> <p>01010b 20</p> <p>01011b 22</p> <p>01100b 24</p> <p>01101b 26</p> <p>01110b 28</p> <p>01111b 30</p> <p>10000b 32</p> <p>Other values are not possible.</p> <p>lbcf_csr_lsqc_hp_credit_init[4:0].lbcf_csr_lsqc_hp_credit_init[4:0] ++ lbcf_csr_lsqc_gen_credit_init[4:0] should always be less than or equal to 32.</p>		
	13:10	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%; text-align: center;">RO</td> </tr> </table> <p>Reserved.</p>	Access:	RO
Access:	RO			

L3SQCREG1 - L3 SQC registers 1			
9	<p>L3SQ Read Once Enable for Sampler Client</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>L3SQ Read Once Enable for Sampler Client (SQROE): Enables Read Once indications to L3 Cache from SQ. Once enabled, any reads from Sampler client (MT) are sent as Read Once. 0 = (default) Reads from Sampler clients issue Read to L3 Cache. 1 = Reads from Sampler clients issue Read Once to L3 Cache. lbcf_csr_sampler_readonce_en.</p>	Access:	R/W
Access:	R/W		
8:6	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">RO</td> </tr> </table> <p>Reserved.</p>	Access:	RO
Access:	RO		
5:3	<p>L3SQ Outstanding L3 Fills</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>L3SQ Outstanding L3 Fills (SQOUTSL3F): Identifies the number of L3 Fills that can be outstanding before SQ throttles the fill requests to L3 Cache. This is not an exact limit, but instead it is used as a threshold to throttling. Once the fill count is greater than or equal to the threshold, then no fills are issued until the fill responses are received to bring the outstanding count back below the threshold. 000b = (default) No limit. 001b = 1 fill. 010b = 2 fills. 011b = 4 fills. 100b = 8 fills. 101b = 16 fills. 11Xb = Reserved. lbcf_csr_lsqc_outs_fill[2:0].</p>	Access:	R/W
Access:	R/W		
2:0	<p>L3SQ Outstanding L3 Lookups</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>L3SQ Outstanding L3 Lookups (SQOUTSL3L): Identifies the number of L3 lookups that can be outstanding before SQ throttles the lookup requests to L3 Cache. This is not an exact limit, but instead it is used as a threshold to throttling. once the lookup count is greater than or equal to the threshold, then no lookups are issued until the lookup responses are received to bring the outstanding count back below the threshold. 000b = (default) No limit. 001b = 1 lookup. 010b = 2 lookups. 011b = 4 lookups. 100b = 8 lookups. 101b = 16 lookups. 11Xb = Reserved. lbcf_csr_lsqc_outs_lookup[2:0].</p>	Access:	R/W
Access:	R/W		

L3 SQC registers 2

L3SQCREG2 - L3 SQC registers 2		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00004567	
Size (in bits):	32	
Address:	0B104h	
DWord	Bit	Description
0	31:17	Reserved
		Access: RO Reserved.
	16	L3SQ Priority Selection Disable
		Access: R/W
		Description
		L3SQ Priority Selection Disable (SQPRIDIS): Enables the use of priority selection based on client ID decodes. If disabled, all cycles in SQ are treated as same priority. 0 = (default) Priority selection is enabled. 1 = Priority selection is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). lbcf_csr_priority_cnt_disable.
		Workaround: If this bit is set to 1 then the following bits in register B108-B10B should have identical values 29:28, 27:26, 25:24, 23:22, 21:20, 19:18, 17:16, 15:14, 13:12, 11:10, 9:8, 7:6, 5:4, 3:2, 1:0.
15		L3SQ Priority 3 Pool Count Disable
		Access: R/W
		Description
		L3SQ Priority 3 Pool Count Disable (SQPRI3CNTDIS): When set, priority3 pool becomes unlimited. And priority3 pool count value should not be used in reset of the remaining counters. 0 = (default) Priority 3 pool count is enabled. 1 = Priority 3 pool count is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). lbcf_csr_priority3_cnt_disable.

L3SQCREG2 - L3 SQC registers 2

	<p>Workaround: If this bit is set to 1 then the following bits in register B108-B10B should have identical values 29:28, 27:26, 25:24, 23:22, 21:20, 19:18, 17:16, 15:14, 13:12, 11:10, 9:8, 7:6, 5:4, 3:2, 1:0.</p>						
14:12	<p>L3SQ Priority 3 Pool Counter</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>100b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>L3SQ Priority 3 Pool Counter (SQPRI3CNT): The count of cycles is selected from priority3 pool before switching to other priority pools. Count is used as the power of 2. 000b = 1 request. 001b = 2 requests. 010b = 4 requests. 011b = 8 requests. ... 111b = 128 requests. lbcf_csr_priority3_cnt[2:0].</p>		Default Value:	100b	Access:	R/W	
Default Value:	100b						
Access:	R/W						
11	<p>L3SQ Priority 2 Pool Count Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td>R/W</td> </tr> </table> <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 5px;"> <thead> <tr style="background-color: #e6f2ff;"> <th style="text-align: center; padding: 5px;">Description</th> </tr> </thead> <tbody> <tr> <td style="padding: 5px;"> <p>L3SQ Priority 2 Pool Count Disable (SQPRI2CNTDIS): When set, priority2 pool becomes unlimited. And priority2 pool count value should not be used in reset of the remaining counters. 0 = (default) Priority 2 pool count is enabled. 1 = Priority 2 pool count is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). lbcf_csr_priority2_cnt_disable.</p> </td> </tr> <tr> <td style="padding: 5px;"> <p>Workaround: If this bit is set to 1 then the following bits in register B108-B10B should have identical values 29:28, 27:26, 25:24, 23:22, 21:20, 19:18, 17:16, 15:14, 13:12, 11:10, 9:8, 7:6, 5:4, 3:2, 1:0.</p> </td> </tr> </tbody> </table>		Access:	R/W	Description	<p>L3SQ Priority 2 Pool Count Disable (SQPRI2CNTDIS): When set, priority2 pool becomes unlimited. And priority2 pool count value should not be used in reset of the remaining counters. 0 = (default) Priority 2 pool count is enabled. 1 = Priority 2 pool count is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). lbcf_csr_priority2_cnt_disable.</p>	<p>Workaround: If this bit is set to 1 then the following bits in register B108-B10B should have identical values 29:28, 27:26, 25:24, 23:22, 21:20, 19:18, 17:16, 15:14, 13:12, 11:10, 9:8, 7:6, 5:4, 3:2, 1:0.</p>
Access:	R/W						
Description							
<p>L3SQ Priority 2 Pool Count Disable (SQPRI2CNTDIS): When set, priority2 pool becomes unlimited. And priority2 pool count value should not be used in reset of the remaining counters. 0 = (default) Priority 2 pool count is enabled. 1 = Priority 2 pool count is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). lbcf_csr_priority2_cnt_disable.</p>							
<p>Workaround: If this bit is set to 1 then the following bits in register B108-B10B should have identical values 29:28, 27:26, 25:24, 23:22, 21:20, 19:18, 17:16, 15:14, 13:12, 11:10, 9:8, 7:6, 5:4, 3:2, 1:0.</p>							
10:8	<p>L3SQ Priority 2 Pool Counter</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>101b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>L3SQ Priority 2 Pool Counter (SQPRI2CNT): The count of cycles is selected from priority2 pool before switching to other priority pools. Count is used as the power of 2. 000b = 1 request. 001b = 2 requests. 010b = 4 requests. 011b = 8 requests. ... 111b = 128 requests.</p>		Default Value:	101b	Access:	R/W	
Default Value:	101b						
Access:	R/W						

L3SQCREG2 - L3 SQC registers 2					
	lbcf_csr_priority2_cnt[2:0].				
7	<p>L3SQ Priority 1 Pool Count Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p style="text-align: center;">Description</p> <p>L3SQ Priority 1 Pool Count Disable (SQPRI1CNTDIS): When set, priority1 pool becomes unlimited. And priority1 pool count value should not be used in reset of the remaining counters. 0 = (default) Priority 1 pool count is enabled. 1 = Priority 1 pool count is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). lbcf_csr_priority1_cnt_disable.</p> <p>Workaround: If this bit is set to 1 then the following bits in register B108-B10B should have identical values 29:28, 27:26, 25:24, 23:22, 21:20, 19:18, 17:16, 15:14, 13:12, 11:10, 9:8, 7:6, 5:4, 3:2, 1:0.</p>	Access:	R/W		
Access:	R/W				
6:4	<p>L3SQ Priority 1 Pool Counter</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Default Value:</td> <td style="width: 40%;">110b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>L3SQ Priority 1 Pool Counter (SQPRI1CNT): The count of cycles is selected from priority1 pool before switching to other priority pools. Count is used as the power of 2. 000b = 1 request. 001b = 2 requests. 010b = 4 requests. 011b = 8 requests. ... 111b = 128 requests. lbcf_csr_priority1_cnt[2:0].</p>	Default Value:	110b	Access:	R/W
Default Value:	110b				
Access:	R/W				
3	<p>L3SQ Priority 0 Pool Count Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p style="text-align: center;">Description</p> <p>L3SQ Priority 0 Pool Count Disable (SQPRI0CNTDIS): When set, priority0 pool becomes unlimited. And priority0 pool count value should not be used in reset of the remaining counters. 0 = (default) Priority 0 pool count is enabled. 1 = Priority 0 pool count is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). lbcf_csr_priority0_cnt_disable.</p>	Access:	R/W		
Access:	R/W				

L3SQCREG2 - L3 SQC registers 2					
	<p>Workaround: If this bit is set to 1 then the following bits in register B108-B10B should have identical values 29:28, 27:26, 25:24, 23:22, 21:20, 19:18, 17:16, 15:14, 13:12, 11:10, 9:8, 7:6, 5:4, 3:2, 1:0.</p>				
2:0	<p>L3SQ Priority 0 Pool Counter</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>111b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>L3SQ Priority 0 Pool Counter (SQPRIOCNT): The count of cycles is selected from priority0 pool before switching to other priority pools. Count is used as the power of 2. 000b = 1 request. 001b = 2 requests. 010b = 4 requests. 011b = 8 requests. ... 111b = (default) 128 requests. lbcf_csr_priority0_cnt[2:0].</p>	Default Value:	111b	Access:	R/W
Default Value:	111b				
Access:	R/W				

L3 SQC registers 3

L3SQCREG3 - L3 SQC registers 3				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00001ABF			
Size (in bits):	32			
Address:	0B108h			
DWord	Bit	Description		
0	31:30	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved.</p>	Access:	RO
	Access:	RO		
	29:28	<p>SOLunit Priority Value</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>SOLunit Priority Value (SQSOLPRIVAL): Identifies the priority value for all cycles that are initiated by SOLunit. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0 (default). 01b = Priority 1. 10b = Priority 2. 11b = Priority 3. lbcf_csr_sol_priority[1:0].</p>	Access:	R/W
	Access:	R/W		
27:26	<p>GSunit Priority Value</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>GSunit Priority Value (SQGSPRIVAL): Identifies the priority value for all cycles that are initiated by GSunit. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0 (default). 01b = Priority 1. 10b = Priority 2. 11b = Priority 3. lbcf_csr_gs_priority[1:0].</p>	Access:	R/W	
Access:	R/W			
25:24	<p>TEunit Priority Value</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>TEunit Priority Value (SQTEPRIVAL): Identifies the priority value for all cycles that are initiated by TEunit. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0 (default). 01b = Priority 1. 10b = Priority 2. 11b = Priority 3.</p>	Access:	R/W	
Access:	R/W			

L3SQCREG3 - L3 SQC registers 3			
	lbcf_csr_te_priority[1:0].		
23:22	<p>CLunit Priority Value</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>CLunit Priority Value (SQCLPRIVAL): Identifies the priority value for all cycles that are initiated by CLunit. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0 (default). 01b = Priority 1. 10b = Priority 2. 11b = Priority 3. lbcf_csr_cl_priority[1:0].</p>	Access:	R/W
Access:	R/W		
21:20	<p>TSunit Priority Value</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>TSunit Priority Value (SQTSPRIVAL): Identifies the priority value for all cycles that are initiated by TSunit. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0 (default). 01b = Priority 1. 10b = Priority 2. 11b = Priority 3. lbcf_csr_ts_priority[1:0].</p>	Access:	R/W
Access:	R/W		
19:18	<p>SFunit Priority Value</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>SFunit Priority Value (SQSFPRIVAL): Identifies the priority value for all cycles that are initiated by SFunit. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0 (default). 01b = Priority 1. 10b = Priority 2. 11b = Priority 3. lbcf_csr_sf_priority[1:0].</p>	Access:	R/W
Access:	R/W		
17:16	<p>SVSM Priority Value</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>SVSM Priority Value (SQSVMPRIVAL): Identifies the priority value for all cycles that are initiated by SVSM. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0 (default). 01b = Priority 1. 10b = Priority 2. 11b = Priority 3. lbcf_csr_svsm_priority[1:0].</p>	Access:	R/W
Access:	R/W		
15:14	<p>SARB Priority Value</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table>	Access:	R/W
Access:	R/W		

L3SQCREG3 - L3 SQC registers 3

		<p>SARB Priority Value (SQSARBPRIVAL): Identifies the priority value for all cycles that are initiated by State Arbiter (SARB). Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0 (default). 01b = Priority 1. 10b = Priority 2. 11b = Priority 3. lbcf_csr_sarb_priority[1:0].</p>					
	13:12	<p>SBE Priority Value</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">01b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>SBE Priority Value (SQSBEPRIVAL): Identifies the priority value for all cycles that are initiated by SBE. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0. 01b = Priority 1 (default). 10b = Priority 2. 11b = Priority 3. lbcf_csr_sbe_priority[1:0].</p>		Default Value:	01b	Access:	R/W
Default Value:	01b						
Access:	R/W						
	11:10	<p>IC\$ Priority Value</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">10b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>IC\$ Priority Value (SQICPRIVAL): Identifies the priority value for all cycles that are initiated by Instruction Cache (IC\$). Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0. 01b = Priority 1. 10b = Priority 2 (default). 11b = Priority 3. lbcf_csr_ic_priority[1:0].</p>		Default Value:	10b	Access:	R/W
Default Value:	10b						
Access:	R/W						
	9:8	<p>TDL Priority Value</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">10b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>TDL Priority Value (SQTDLPRIVAL): Identifies the priority value for all cycles that are initiated by TDL. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0. 01b = Priority 1. 10b = Priority 2 (default). 11b = Priority 3. lbcf_csr_tdl_priority[1:0].</p>		Default Value:	10b	Access:	R/W
Default Value:	10b						
Access:	R/W						
	7:6	<p>DCunit Priority Value</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">10b</td> </tr> </table>		Default Value:	10b		
Default Value:	10b						

L3SQCREG3 - L3 SQC registers 3					
	<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>DCunit Priority Value (SQDCPRIVAL): Identifies the priority value for all cycles that are initiated by DC. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0. 01b = Priority 1. 10b = Priority 2 (default). 11b = Priority 3. lbcf_csr_dc_priority[1:0].</p>	Access:	R/W		
Access:	R/W				
5:4	<p>DAPR Priority Value</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">11b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>DAPR Priority Value (SQDAPRPRIVAL): Identifies the priority value for all cycles that are initiated by DAPR. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0. 01b = Priority 1. 10b = Priority 2. 11b = Priority 3 (default). lbcf_csr_dapr_priority[1:0].</p>	Default Value:	11b	Access:	R/W
Default Value:	11b				
Access:	R/W				
3:2	<p>MTunit Priority Value</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">11b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>MTunit Priority Value (SQMTPRIVAL): Identifies the priority value for all cycles that are initiated by Sampler (MT). Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0. 01b = Priority 1. 10b = Priority 2. 11b = Priority 3 (default). lbcf_csr_mt_priority[1:0].</p>	Default Value:	11b	Access:	R/W
Default Value:	11b				
Access:	R/W				
1:0	<p>LSQCunit Priority Value</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">11b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>LSQCunit Priority Value (SQPRIVAL): Identifies the priority value for all cycles that are initiated by Super Queue (L3 Evictions). Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0. 01b = Priority 1. 10b = Priority 2. 11b = Priority 3 (default). lbcf_csr_lsqc_priority[1:0].</p>	Default Value:	11b	Access:	R/W
Default Value:	11b				
Access:	R/W				

LBCF config save msg

LBCFCSR - LBCF config save msg				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B2FCh			
This register is not context saved and is written by PM unit.				
DWord	Bit	Description		
0	31:10	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%; text-align: center;">RO</td> </tr> </table>	Access:	RO
	Access:	RO		
9:0	Context save bit <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 40%;">Access:</td> <td style="width: 60%;">R/W Hardware Clear</td> </tr> </table> <p>Bit[9]: Power Context Save Request. 0: Power context save is not being requested (default). 1: Power context save is being requested. Unit needs to self-clear this bit upon sampling.</p> <p>Bits[8:0]: QWord Credits for Power Context Save Request. Minimum Credits = 1: Unit may send 1 QWord pair (enough for first LRI at least). Maximum Credits = 511: Unit may send 511 QWord pairs. A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and consumes one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).</p>	Access:	R/W Hardware Clear	
Access:	R/W Hardware Clear			

LBCF DPF Error log register 0

LBCFPM00 - LBCF DPF Error log register 0				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B130h			
Slice0 Bank 0 subbank0 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. lbcf_sb0_error_addr1[9:0].</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The Address located in field 31:21 is valid. lbcf_sb0_valid_error1.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. lbcf_sb0_error_addr0[9:0].</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The address located in field 15:5 is valid. lbcf_sb0_valid_error0.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 1

LBCFPM01 - LBCF DPF Error log register 1				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B134h			
Slice0 Bank 0 subbank1 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. lbcf_sb1_error_addr1[9:0].</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The Address located in field 31:21 is valid. lbcf_sb1_error_addr0[9:0].</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. lbcf_sb1_error_addr0[9:0].</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The address located in field 15:5 is valid. lbcf_sb1_valid_error0.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 2

LBCFPM02 - LBCF DPF Error log register 2				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B138h			
Slice0 Bank0 Subbank 2 Error log register				
DWord	Bit	Description		
0	31:21	Row Number for Error 1 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. lbcf_sb2_error_addr1[9:0].	Access:	R/W
	Access:	R/W		
	20:17	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	Valid Error 1 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Valid Error: The Address located in field 31:21 is valid. lbcf_sb2_valid_error1.	Access:	R/W
	Access:	R/W		
15:5	Row Number for Error0 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. lbcf_sb2_error_addr0[9:0].	Access:	R/W	
Access:	R/W			
4:1	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	Valid Error 0 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Valid Error: The address located in field 15:5 is valid. lbcf_sb2_valid_error0.	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 3

LBCFPM03 - LBCF DPF Error log register 3				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B13Ch			
Slice0 Bank0 subbank3 Error log register				
DWord	Bit	Description		
0	31:21	Row Number for Error 1 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. lbcf_sb3_error_addr1[9:0].	Access:	R/W
	Access:	R/W		
	20:17	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	Valid Error 1 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Valid Error: The Address located in field 31:21 is valid. lbcf_sb3_valid_error1.	Access:	R/W
	Access:	R/W		
15:5	Row Number for Error0 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. lbcf_sb3_error_addr0[9:0].	Access:	R/W	
Access:	R/W			
4:1	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	Valid Error 0 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Valid Error: The address located in field 15:5 is valid. lbcf_sb3_valid_error0.	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 4

LBCFERRLOG01 - LBCF DPF Error log register 4				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B140h			
Slice 0 Bank 1 Subbank0 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 1 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 0 Bank 1 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 0 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 5

LBCFERRLOG02 - LBCF DPF Error log register 5				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B144h			
Slice 0 Bank 1 Subbank1 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 1 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The Address located in field 31:21 is valid. Slice 0 Bank 1 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The address located in field 15:5 is valid</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 6

LBCFERRLOG03 - LBCF DPF Error log register 6				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B148h			
Slice 0 Bank 1 subbank2 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 1 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 1 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The address located in field 15:5 is valid. Slice 0 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 7

LBCFERRLOG04 - LBCF DPF Error log register 7				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B14Ch			
Slice0 Bank1 subbank3 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 1 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The Address located in field 31:21 is valid. Slice 0 Bank 1 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The address located in field 15:5 is valid. Slice 0 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 8

LBCFERRLOG05 - LBCF DPF Error log register 8				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B150h			
Slice 0 Bank 2 Subbank0 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. The number of rows varies between 4K vs. 8K/16K subbanks which requires 10 bits vs 11 bits respectively. This field contains the row# with the error. Slice 0 Bank 2 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 16:5 is valid and Slice 0 Bank 2 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
16:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 16:5 is valid and Slice 0 Bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 16:5 is valid. Slice 0 Bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 9

LBCFERRLOG06 - LBCF DPF Error log register 9				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B154h			
Slice 0 Bank 2 subbank1 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. The number of rows varies between 4K vs. 8K/16K subbanks which requires 10 bits vs 11 bits respectively. This field contains the row# with the error. Slice 0 Bank 2 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 0 Bank 2 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 10

LBCFERRLOG07 - LBCF DPF Error log register 10				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B158h			
Slice 0 Bank 2 subbank2 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. The number of rows varies between 4K vs. 8K/16K subbanks which requires 10 bits vs. 11 bits respectively. This field contains the row# with the error. Slice 0 Bank 2 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 0 Bank 2 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 0 Bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 11

LBCFERRLOG08 - LBCF DPF Error log register 11				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B15Ch			
slice0 Bank 2 subbank3 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. The number of rows varies between 4K vs. 8K/16K subbanks which requires 10 bits vs. 11 bits respectively. This field contains the row# with the error. Slice 0 Bank 2 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 0 Bank 2 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 0 Bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 12

LBCFERRLOG09 - LBCF DPF Error log register 12				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B160h			
Slice 0 Bank 3 subbank0 Error log register				
DWord	Bit	Description		
0	31:21	Row Number for Error 1 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 3 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	Valid Error 1 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 0 Bank 3 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	Row Number for Error0 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	Valid Error 0 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 0 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 13

LBCFERRLOG10 - LBCF DPF Error log register 13				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B164h			
Slice 0 Bank 3 subbank1 Error log register 00				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 3 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 0 Bank 3 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 14

LBCFERRLOG11 - LBCF DPF Error log register 14				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B168h			
Slice 0 Bank 3 subbank2 Error log register 00				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 3 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 0 Bank 3 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 0 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 15

LBCFERRLOG12 - LBCF DPF Error log register 15				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B16Ch			
Slice0 Bank 3 subbank3 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 3 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 0 Bank 3 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 0 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 16

LBCFERRLOG13 - LBCF DPF Error log register 16				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B170h			
Slice 1 bank 0 Subbank0 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 1 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 bank 1 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 1 bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 17

LBCFERRLOG14 - LBCF DPF Error log register 17				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B174h			
Slice 1 bank 0 subbank1 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 1 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 bank 1 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 18

LBCFERRLOG15 - LBCF DPF Error log register 18				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B178h			
Slice 1 bank 0 subbank2 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 1 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 bank 1 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 1 bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 19

LBCFERRLOG16 - LBCF DPF Error log register 19				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B17Ch			
Slice1 bank 0 subbank3 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 1 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 bank 1 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 1 bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 20

LBCFERRLOG17 - LBCF DPF Error log register 20				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B180h			
Slice 1 bank 1 subbank0 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 0 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 bank 0 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 1 bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 21

LBCFERRLOG18 - LBCF DPF Error log register 21				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B184h			
Slice 1 bank 1 subbank1 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 0 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 bank 0 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 22

LBCFERRLOG19 - LBCF DPF Error log register 22				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B188h			
Slice 1 bank 1 subbank2 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 0 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 bank 0 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 1 bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 23

LBCFERRLOG20 - LBCF DPF Error log register 23				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B18Ch			
slice1 bank1 subbbank 3 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 0 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 bank 0 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 1 bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 24

LBCFERRLOG21 - LBCF DPF Error log register 24				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B190h			
Slice 1 bank 2 subbank0 Error log register 00				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 2 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 bank 2 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 1 bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 25

LBCFERRLOG22 - LBCF DPF Error log register 25				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B194h			
Slice 1 bank 2 subbank 1 Error log register 00				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 2 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 bank 2 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 26

LBCFERRLOG23 - LBCF DPF Error log register 26				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B198h			
Slice 1 bank 2 subbank 2 Error log register				
DWord	Bit	Description		
0	31:21	Row Number for Error 1 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 2 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	Valid Error 1 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 bank 2 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	Row Number for Error0 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	Valid Error 0 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 1 bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 27

LBCFERRLOG24 - LBCF DPF Error log register 27				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B19Ch			
Slice 1 bank 2 subbank 3 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 2 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 bank 2 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 1 bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 28

LBCFERRLOG25 - LBCF DPF Error log register 28				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B1A0h			
Slice 1 Bank 3 subbank 0 Error log register				
DWord	Bit	Description		
0	31:21	Row Number for Error 1 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 Bank 3 Error log register 00.	Access:	R/W
	Access:	R/W		
	20:17	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	Valid Error 1 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Valid Error: The error located in field 31:21 is valid. Slice 1 Bank 3 Error log register 00.	Access:	R/W
	Access:	R/W		
15:5	Row Number for Error0 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 Bank 3 Error log register 00.	Access:	R/W	
Access:	R/W			
4:1	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	Valid Error 0 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Valid Error: The error located in field 15:5 is valid. Slice 1 Bank 3 Error log register 00.	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 29

LBCFERRLOG26 - LBCF DPF Error log register 29				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B1A4h			
Slice 1 Bank 3 subbank 1 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 Bank 3 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 Bank 3 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 30

LBCFERRLOG27 - LBCF DPF Error log register 30				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B1A8h			
Slice 1 Bank 3 subbank 2 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 Bank 3 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 Bank 3 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 1 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 31

LBCFERRLOG28 - LBCF DPF Error log register 31				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B1ACh			
slice1 Bank 3 subbank 3 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 Bank 3 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 Bank 3 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 1 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 32

LBCFERRLOG29 - LBCF DPF Error log register 32				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B1B0h			
Slice 2 Bank 0 subbank0 Error log register				
DWord	Bit	Description		
0	31:21	Row Number for Error 1 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 0 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	Valid Error 1 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 0 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	Row Number for Error0 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	Valid Error 0 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 33

LBCFERRLOG30 - LBCF DPF Error log register 33				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B1B4h			
Slice 2 Bank 0 subbank 1 Error log register				
DWord	Bit	Description		
0	31:21	Row Number for Error 1 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 0 Error log register 00.	Access:	R/W
	Access:	R/W		
	20:17	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	Valid Error 1 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 0 Error log register 00.	Access:	R/W
	Access:	R/W		
15:5	Row Number for Error0 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 0 Error log register 00.	Access:	R/W	
Access:	R/W			
4:1	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	Valid Error 0 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Valid Error: The error located in field 15:5 is valid.	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 34

LBCFERRLOG31 - LBCF DPF Error log register 34				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B1B8h			
Slice 2 Bank 0 Subbank 2 Error log register 00				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 0 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 0 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 35

LBCFERRLOG32 - LBCF DPF Error log register 35				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B1BCh			
Slice2 Bank 0 Subbank 3 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 0 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 0 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 36

LBCFERRLOG33 - LBCF DPF Error log register 36				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B1C0h			
Slice 2 Bank 1 Subbank 0 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 1 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 1 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 37

LBCFERRLOG34 - LBCF DPF Error log register 37				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B1C4h			
Slice 2 Bank 1 Subbank 1 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 1 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 1 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 38

LBCFERRLOG35 - LBCF DPF Error log register 38				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B1C8h			
Slice 2 Bank 1 Subbank 2 Error log register 00				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 1 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 1 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 39

LBCFERRLOG36 - LBCF DPF Error log register 39				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B1CCh			
Slice 2 Bank 1 subbank 3 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 1 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 1 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 40

LBCFERRLOG37 - LBCF DPF Error log register 40				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B1D0h			
Slice 2 Bank 2 subbank 0 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 2 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 2 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 41

LBCFERRLOG38 - LBCF DPF Error log register 41				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B1D4h			
Slice 2 Bank 2 subbank 1 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 2 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 2 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 42

LBCFERRLOG39 - LBCF DPF Error log register 42				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B1D8h			
Slice 2 Bank 2 subbank 2 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 2 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 2 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 43

LBCFERRLOG40 - LBCF DPF Error log register 43				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B1DCh			
Slice 2 Bank 2 subbank 3 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 2 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 2 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 44

LBCFERRLOG41 - LBCF DPF Error log register 44				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B1E0h			
Slice 2 Bank 3 subbank 0 Error log register				
DWord	Bit	Description		
0	31:21	Row Number for Error 1 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 3 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	Valid Error 1 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 3 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	Row Number for Error0 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. and Slice 2 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	Valid Error 0 <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is validcorresponding logical 16KB group should bypass this row. Slice 2 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 45

LBCFERRLOG42 - LBCF DPF Error log register 45				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B1E4h			
Slice 2 Bank 3 subbank 1 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 3 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 3 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 46

LBCFERRLOG43 - LBCF DPF Error log register 46				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B1E8h			
Slice 2 Bank 3 subbank 2 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 3 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 3 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 47

LBCFERRLOG44 - LBCF DPF Error log register 47				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B1ECh			
slice 2 Bank 3 subbank 3 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 3 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 3 Error log register 00.</p>	Access:	R/W
	Access:	R/W		
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBS config bits

LBSREG - LBS config bits			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x46000000 CHV, BSW		
Size (in bits):	32		
Address:	0B124h		
Config Bits for LBS unit			
DWord	Bit	Description	
0	31:27	Retry timer for lookup into LSQC	
		Default Value:	01000b
		Access:	R/W
		Time between receiving Reject Response from LSQC and doing a snoop lookup request again onto LSQCunit. 00000b: 0 clocks. 00001b: 1 clocks. 00010b: 2 clocks. ... 01000b: 8 clocks (default value). ... 11111b: 32 clocks. lbcf_retry_timer[4:0].	
26		Recycle parent faster in R/W perf mode	
		Default Value:	1b
		Access:	R/W
Arc into recycle as soon as parent becomes eligible to be recycled. 0: Disabled (recycle possible only when parent is recycled). 1: Enabled (default). lbcf_csr_lsqc_rwperf_quickrec.			
25		Perf mode for Writes to same address	
		Default Value:	1b
		Project:	CHV, BSW
		Access:	R/W
Performance improvement for writes to same address in L3: 0 - Performance mode is not enabled. 1 - Performance mode is enabled (default). lbcf_csr_lsqc_erlyrec.			
24:0		Reserved	
		Access:	RO

LEAKAGECOUNTER

LEAKAGECOUNTER - LEAKAGECOUNTER						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	1300D4h					
Leakage counter readout						
DWord	Bit	Description				
0	31:0	<p>Leakage_Counter</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>This is a live read of the 32-bit leakage counter. Reading this register does not cause the counter to clear. Only the write-write protocol from Punit to Gunit will casue the leakage counter to clear.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

LEAKAGECOUNTERCTL

LEAKAGECOUNTERCTL - LEAKAGECOUNTERCTL			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	1300D0h		
Leakage counter control.			
DWord	Bit	Description	
0	31	leakage_lock	
		Default Value:	0b
		Access:	R/W Lock
This is the lock bit for the leakage counter registers. 13_00D0-13_00DC.			
30:1		Reserved	
		Default Value:	00000000h
		Access:	RO
Reserved			
0		leakage_count_en	
		Default Value:	0b
		Access:	R/W Lock
Enable the leakage counters. When zero, the counters will be held to zero. As this transitions to 0-1, counting is enabled. Like the EMON Energy Counters, the leakage counter will perform a "sum of weights" for the 16 events(/subwells) described in 13_00D8 and 13_00DC.			

LEAKAGEWEIGHT1

LEAKAGEWEIGHT1 - LEAKAGEWEIGHT1			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	1300D8h		
Leakage weights for wells types 1 to 4.			
DWord	Bit	Description	
0	31:24	leakage_vdve	
		Default Value:	00h
		Access:	R/W Lock
		Leakage weight for 'vdve' well type. One of these wells are expected on CHV, BSW.	
	23:16	Reserved	
		Default Value:	00h
		Access:	R/W Lock
	15:8	Reserved	
		Default Value:	00h
		Access:	R/W Lock
	7:0	leakage_aon	
		Default Value:	00h
		Access:	R/W Lock
		Leakage weight for 'aon' well type. One of these wells are expected on CHV, BSW.	

LEAKAGEWEIGHT2

LEAKAGEWEIGHT2 - LEAKAGEWEIGHT2			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	1300DCh		
Leakage weights for wells types 5 to 8.			
DWord	Bit	Description	
0	31:24	leakage_eupair	
		Default Value:	00h
		Access:	R/W Lock
		Leakage weight for 'eupair' well type. Eight of these wells are expected on CHV, BSW.	
	23:16	leakage_ss	
		Default Value:	00h
		Access:	R/W Lock
		Leakage weight for 'ss' well type. Two of these wells are expected on CHV, BSW.	
	15:8	leakage_l3	
		Default Value:	00h
		Access:	R/W Lock
		Leakage weight for 'l3' well type. One of these wells are expected on CHV, BSW.	
	7:0	leakage_ffsc	
		Default Value:	00h
		Access:	R/W Lock
		Leakage weight for 'ffsc' well type. One of these wells are expected on CHV, BSW.	

LNCF config save msg

LNCFCSR - LNCF config save msg				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B0FCh			
This register is not context saved and is written by pm unit.				
DWord	Bit	Description		
0	31:10	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> </table>	Access:	RO
	Access:	RO		
9:0	<p>Context save bit</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 40%;">Access:</td> <td style="width: 60%;">R/W Hardware Clear</td> </tr> </table> <p>Bit[9].Power Context Save Request 0: Power context save is not being requested (default). 1: Power context save is being requested. Unit needs to self-clear this bit upon sampling.</p> <p>Bits[8:0].QWord Credits for Power Context Save Request. Minimum Credits = 1: Unit may send 1 QWord pair (enough for first LRI at least). Maximum Credits = 511: Unit may send 511 QWord pairs.</p> <p>A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and consume one QWord credit.</p> <p>Only valid with PWRCTX_SAVE_REQ (Bit9).</p>	Access:	R/W Hardware Clear	
Access:	R/W Hardware Clear			

Load Indirect Base Vertex

3DPRIM_BASE_VERTEX - Load Indirect Base Vertex				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	RenderCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	02440h-02443h			
Valid Projects:				
DWord	Bit	Description		
0	31:0	<p>Base Vertex</p> <table border="1"> <tr> <td>Format:</td> <td>S31</td> </tr> </table> <p>This register is used to store the Base Vertex of the 3D_PRIMITIVE command when Load Indirect Enable is set.</p>	Format:	S31
Format:	S31			

Load Indirect Instance Count

3DPRIM_INSTANCE_COUNT - Load Indirect Instance Count		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02438h-0243Bh	
Valid Projects:		
DWord	Bit	Description
0	31:0	Instance Count This register is used to store the Instance Count of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Start Instance

3DPRIM_START_INSTANCE - Load Indirect Start Instance				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	RenderCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	0243Ch-0243Fh			
Valid Projects:				
DWord	Bit	Description		
0	31:0	<p>Start Vertex</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>This register is used to store the Start Instance of the 3D_PRIMITIVE command when Load Indirect Enable is set.</p>	Format:	U32
Format:	U32			

Load Indirect Start Vertex

3DPRIM_START_VERTEX - Load Indirect Start Vertex				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	RenderCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	02430h-02433h			
Valid Projects:				
DWord	Bit	Description		
0	31:0	<p>Start Vertex</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>This register is used to store the Start Vertex of the 3D_PRIMITIVE command when Load Indirect Enable is set.</p>	Format:	U32
Format:	U32			

Load Indirect Vertex Count

3DPRIM_VERTEX_COUNT - Load Indirect Vertex Count				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	RenderCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	02434h-02437h			
Valid Projects:				
DWord	Bit	Description		
0	31:0	<p>Vertex Count</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>This register is used to store the Vertex Count of the 3D_PRIMITIVE command when Load Indirect Enable is set.</p>	Format:	U32
Format:	U32			

LOW 2X FREQUENCY THRESHOLD

LOW2XFREQTHRESH - LOW 2X FREQUENCY THRESHOLD						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x000000A0					
Size (in bits):	32					
Address:	101128h					
New for CHV, BSW.						
BIOS/Driver programs the Low2x frequency threshold.						
DWord	Bit	Description				
0	31:16	<p>RESERVED</p> <table border="1"> <tr> <td>Default Value:</td> <td>0000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved</p>	Default Value:	0000h	Access:	RO
	Default Value:	0000h				
Access:	RO					
15:0	<p>L3FREQREG</p> <table border="1"> <tr> <td>Default Value:</td> <td>00A0h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This is control signal needed from clock unit that can be set at 1 when 2X clock frequency is less than or equal to 1GHz. It needs to be at 0 when 2X clock frequency is > 1GHz. Value when in HPLL mode: low2xthresh=0x00B4. This sets low2xfreq high whenever cu2x frequency is less than or equal to 800, 800, 1000, 800, and 800 for CZ400, CZ320, CZ333, CZ266, and CZ200 respectively. Value when in GPLL mode: low2xthresh=0x00A0. This sets low2xfreq high whenever cu2x frequency is less than or equal to 1000, 800, 834, 889, and 800 for CZ400, CZ320, CZ333, CZ266, and CZ200 respectively.</p>	Default Value:	00A0h	Access:	R/W	
Default Value:	00A0h					
Access:	R/W					

LPFC control register

LPFCNTL - LPFC control register					
Register Space:	MMIO: 0/2/0				
Project:	CHV, BSW				
Source:	PRM				
Default Value:	0x00000000				
Size (in bits):	32				
Address:	0B01Ch				
LPFC control register.					
DWord	Bit	Description			
0	31	LPFC enable signal <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> LPFC event collection enable signal. Incf_lpfc_cnt_en.	Access:	R/W	
	Access:	R/W			
30:0	Reserved <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Reserved.	Project:	CHV, BSW	Access:	RO
Project:	CHV, BSW				
Access:	RO				

LTCD Error Injection Register

LBCFERR - LTCD Error Injection Register			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000 CHV, BSW		
Size (in bits):	32		
Address:	0B12Ch		
LTCD Error Inject control bits in LBCF			
DWord	Bit	Description	
0	31:25	Reserved	
		Project:	CHV, BSW
		Access:	RO
	24	LTISEQSL parity error interrupt	
		Default Value:	0b
		Project:	CHV, BSW
		Access:	R/W
	Parity error interrupt to LTISEQ Slice.		
	23	Bank hang on parity disable	
		Default Value:	0b
		Project:	CHV, BSW
	22	Parity Error Injection Enable	
		Project:	CHV, BSW
		Access:	R/W
	0: Disable parity error injection. 1: Enable parity error injection. lbcf_parity_err_inject_en. Do not Enable this when ECC Error injection is enabled.		
	21	Double Bit Error injection	
Project:		CHV, BSW	
Access:		R/W	
0: Default No error injected. 1: Double bit error is injected. lbcf_ecc_2bit_err_inject. Single bit Error Injection and double bit error injection are mutually exclusive.			

LBCFERR - LTCD Error Injection Register

		Do not Enable this when Parity Error injection is enabled.	
20	Single Bit Error injection	Project:	CHV, BSW
		Access:	R/W
	<p>0: Default No error injected. 1: Single bit error is injected. lbcf_ecc_1bit_err_inject. Single bit Error Injection and double bit error injection are mutually exclusive. Do not Enable this when Parity Error injection is enabled.</p>		
19	ECC Error Injection Enable	Project:	CHV, BSW
		Access:	R/W
	<p>0: Disable ECC error injection. 1: Enable ECC error injection. lbcf_ecc_err_inject_en. Do not Enable this when Parity Error injection is enabled.</p>		
18:4	Row address for error injection	Project:	CHV, BSW
		Access:	R/W
	<p>Row address for which error is injected. For ECC error injection, the same row address is overloaded to inject ECC error for that particular row address. SLM configuration. For Address: Rowaddress [16:7] is applicable for SLM banks and Parity injection is enabled and Rowaddress[18:7] is applicable for ECC (for both NonSLM/SLM banks). Sub bank is applicable only for Parity injection. Only Subbank 0, 1, 2, 3 are supported and are only related to SLM Banks (4KB). Total 12 bits address. Bits 18:7: Row address. Bits 6:4: Sub-Bank number. lbcf_parity_err_inject_rowaddr[9:0].lbcf_parity_err_inject_subbank[2:0].16:7 - For SLM parity only. lbcf_parity_err_inject_rowaddr[9:0].lbcf_ecc_err_inject_rowaddr[11:0].For ECC error injection, the same row address is overloaded to inject ECC error for that particular row address.</p>		
3:2	Bank ID for error injection	Project:	CHV, BSW
		Access:	R/W
	<p>00b: Inject in Bank 0. 01b: Inject in Bank 1. 10b: Inject in Bank 2. 11b: Inject in Bank 3 (error injection not supported for SLM bank3).</p>		

LBCFERR - LTCD Error Injection Register	
	lbcf_err_inject_bankid[1:0].
1:0	Slice ID for Error injection
	Project: CHV, BSW
	Access: R/W
	00b: Inject error in Slice 0. 01b: Inject error in Slice 1. 10b: Inject error in Slice 2. lbcf_err_inject_sliceid.

MA

MA - MA		
Register Space:	PCI: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00094h	
Message Address		
DWord	Bit	Description
0	31:2	ADDRESS
		Default Value: 00000000h
	Access: R/W	
	MA: Lower 32-bits of the system specified message address, always DW aligned. When GVD issues an MSI interrupt as a MEMWR on the SCL, the memory address corresponds to the value of this field.	
1:0	RESERVED	
	Default Value: 00b	
	Access: RO	
Reserved		

Main Graphic Arbiter Error Report

ERROR - Main Graphic Arbiter Error Report		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	040A0h	
This register is used to report different error conditions. Error bits are writable.		
DWord	Bit	Description
0	31	Reserved Error Bits 31
		Default Value: 0b
		Access: R/W
		Future Use.
	30	Reserved Error Bits 30
		Default Value: 0b
		Access: R/W
		Future Use.
	29	Reserved Error Bits 29
		Default Value: 0b
		Access: R/W
		Future Use.
	28	Reserved Error Bits 28
		Default Value: 0b
		Access: R/W
		Future Use.
	27	Reserved Error Bits 27
		Default Value: 0b
		Access: R/W
		Future Use.
26	Reserved Error Bits 26	
	Default Value: 0b	
	Access: R/W	

ERROR - Main Graphic Arbiter Error Report

	Future Use.	
25	Reserved Error Bits 25	
	Default Value:	0b
	Access:	R/W
	Future Use.	
24	Reserved Error Bits 24	
	Default Value:	0b
	Access:	R/W
	Future Use.	
23	Reserved Error Bits 23	
	Default Value:	0b
	Access:	R/W
	Future Use.	
22	Reserved Error Bits 22	
	Default Value:	0b
	Access:	R/W
	Future Use.	
21	Reserved Error Bits 21	
	Default Value:	0b
	Access:	R/W
	Future Use.	
20	Reserved Error Bits 20	
	Default Value:	0b
	Access:	R/W
	Future Use.	
19	Reserved Error Bits 19	
	Default Value:	0b
	Access:	R/W
	Future Use.	
18	Reserved Error Bits 18	
	Default Value:	0b

ERROR - Main Graphic Arbiter Error Report

		Access:	R/W
		Future Use.	
17	Reserved Error Bits 17		
		Default Value:	0b
		Access:	R/W
		Future Use.	
16	Reserved Error Bits 16		
		Default Value:	0b
		Access:	R/W
		Future Use.	
15	Reserved Error Bits 15		
		Default Value:	0b
		Access:	R/W
		ctx_fault_ctxt_not_prsmt_err - The Present (P) field in the context-entry used to process the DMA request is Clear.	
14	Reserved Error Bits 14		
		Default Value:	0b
		Access:	R/W
		ctx_fault_root_not_prsmt_err - The present (UP/LP) field in the root-entry used to process the untranslated request with PASID is 0.	
13	Reserved Error Bits 13		
		Default Value:	0b
		Access:	R/W
		ctx_fault_pasid_not_prsnt_err - PASID Table entry to be used does not have the PRESENT flag set. This means the PASID entry is not valid.	
12	Reserved Error Bits 12		
		Default Value:	0b
		Access:	R/W
		ctx_fault_pasid_ovflw_err - PASID Table size in extended context entry defines the number of PASIDs that will be supported. If hardware receives a PASID number outside the supported boundary, report as an error.	
11	Reserved Error Bits 11		
		Default Value:	0b

ERROR - Main Graphic Arbiter Error Report

		Access:	R/W
		ctx_fault_pasid_dis_err - Submission of advanced context where the PASID field is not enabled in the extended context entry.	
10	Reserved Error Bits 10		
		Default Value:	0b
		Access:	R/W
		rstrm_fault_nowb_atomic_err - All page table accesses in advanced context with A/D bits are considered as atomic operations in WB space. However if the memory type for the page table accesses come out as anything but WB, that is an error.	
9	Reserved		
8	Unloaded PD Error		
		Default Value:	0b
		Access:	R/W
		The Cache Line containing a PD entry being accessed, was marked as invalid in the last PD load cycle.	
7	Reserved Error Bits 7		
		Default Value:	0b
		Access:	R/W
		Future Use.	
6	Reserved		
5	Reserved		
4	Reserved		
3	Reserved		
2	Invalid Page Directory Entry Error		
		Default Value:	0b
		Access:	R/W
		PD entry's valid bit is 0.	
1	Reserved		
0	TLB Page Fault Error		
		Default Value:	0b
		Access:	R/W
		A TLB Page's GTT translation generated a page fault (GTT entry not valid).	

Main Graphic Arbiter Error Report 2

ERROR_2 - Main Graphic Arbiter Error Report 2						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	040A4h					
DWord	Bit	Description				
0	31:0	Main Graphic Arbiter Error Report 2 <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Bit [31:6] - Reserved. Bit [5:0] - tlbpend_reg_faultcnt[5:0].	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Main Graphic Arbiter Error Report 3

ERROR_3 - Main Graphic Arbiter Error Report 3			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000 CHV, BSW		
Size (in bits):	32		
Address:	040A8h		
This register is used to report different error conditions. Error bits are writable.			
DWord	Bit	Description	
0	31:16	Reserved	
		Default Value:	0000h
		Access:	RO
	15	Error3 Bits 15	
		Default Value:	0b
		Access:	R/W
	Future Use.		
	14	Error3 Error Bits 14	
		Default Value:	0b
		Access:	R/W
	Future Use.		
	13	Error3 Error Bits 13	
Default Value:		0b	
Access:		R/W	
Future Use.			
12	Error3 Error Bits 12		
	Default Value:	0b	
	Access:	R/W	
Future Use.			
11	Error3 Error Bits 11		
	Default Value:	0b	
	Project:	CHV, BSW	
	Access:	R/W	
invalid_varmtrr_overlap_memtype_rd.			

ERROR_3 - Main Graphic Arbiter Error Report 3

	10	Error3 Error Bits 10	
		Default Value:	0b
		Project:	CHV, BSW
		Access:	R/W
	invalid_varmtrr_overlap_memtype_wr.		
	9	Error3 Error Bits 9	
		Default Value:	0b
	Project:	CHV, BSW	
	Access:	R/W	
invalid_default_memtype_value_rd.			
8	Error3 Error Bits 8		
	Default Value:	0b	
	Project:	CHV, BSW	
	Access:	R/W	
invalid_default_memtype_value_wr.			
7	Error3 Error Bits 7		
	Default Value:	0b	
	Project:	CHV, BSW	
	Access:	R/W	
invalid_varmtrr_memtype_value_rd.			
6	Error3 Error Bits 6		
	Default Value:	0b	
	Project:	CHV, BSW	
	Access:	R/W	
invalid_varmtrr_memtype_value_wr.			
5	Error3 Error Bits 5		
	Default Value:	0b	
	Project:	CHV, BSW	
	Access:	R/W	
invalid_fixedmtrr_memtype_value_rd.			
4	Error3 Error Bits 4		

ERROR_3 - Main Graphic Arbiter Error Report 3

		Default Value:		0b	
		Project:		CHV, BSW	
		Access:		R/W	
		invalid_fixedmtrr_memtype_value_wr.			
	3	Error3 Error Bits 3			
		Default Value:		0b	
		Project:		CHV, BSW	
		Access:		R/W	
					gttc_internal_error.
	2	Reserved			
	1	Error3 Error Bits 1			
		Default Value:		0b	
		Access:		R/W	
		tlbpend_internal_error.			
	0	Error3 Error Bits 0			
		Default Value:		0b	
Access:		R/W			
reg_wrid_internal_error.					

Main Graphic Arbiter Error Report Register

GFX_ARB_ERROR_RPT - Main Graphic Arbiter Error Report Register			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	RenderCS		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Trusted Type:	1		
Address:	040A0h		
This register is used to report error conditions. Error bits are writable.			
DWord	Bit	Description	
0	31:16	Reserved Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td> </td></tr></table> MBZ	
	15:9	Reserved	
	8	Unloaded PD Error The Cache Line containing a PD entry being accessed was marked as invalid in the last PD load cycle.	
	7	Reserved	
	6	Reserved	
	5	Reserved	
	4	Reserved	
	3	Hardware Status Page Fault Error HWSP's GTT translation generated a page fault (GTT entry not valid).	
	2	Invalid Page Directory entry error PD entry's valid bit is 0.	
1	Context Page Fault Error A Context Page's GTT translation generated a page fault (GTT entry not valid).		
0	TLB Page Fault Error A TLB Page's GTT translation generated a page fault (GTT entry not valid).		

MASTER_INT_CTL

MASTER_INT_CTL - MASTER_INT_CTL		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	44200h	
<p>This register has the master enable for graphics interrupts and gives an overview of what interrupts are pending. An interrupt pending bit will read 1b while one or more interrupts of that category are set (IIR) and enabled (IER). All Pending Interrupts are ORed together to generate the combined interrupt. The combined interrupt is ANDed with the Master Interrupt enable to create the master enabled interrupt. The master enabled interrupt goes to PCI device 2 interrupt processing. The master interrupt enable must be set before any of these interrupts will propagate to PCI device 2 interrupt processing.</p>		
DWord	Bit	Description
0	31	MASTER_INTERRUPT_ENABLE
		Default Value: 0b
	Access: R/W	
	<p>THIS IS THE MASTER CONTROL FOR GRAPHICS INTERRUPT. this must be enabled for any of these interrupts to propagate to PCI dev2 interrupt processing. 0b - master interrupt disable, 1b - master interrupt enable</p>	
	30	PCU_INTERRUPT_PENDING
Default Value: 0b		
29:8	Reserved	
	Default Value: 00000b	
7	WDBOX_OACS_INTERRUPT_PENDING	
	Default Value: 0b	
6	VEBOX_INTERRUPT_PENDING	
	Default Value: 0b	

MASTER_INT_CTL - MASTER_INT_CTL									
	<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td colspan="2">This field indicates if iterrups of this category is pending.</td> </tr> </table>	Access:	RO	This field indicates if iterrups of this category is pending.					
Access:	RO								
This field indicates if iterrups of this category is pending.									
5	Reserved								
4	<table border="1"> <tr> <td colspan="2">GTPM_INTERRUPT_PENDING</td> </tr> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td colspan="2">This field indicates if iterrups of this category is pending.</td> </tr> </table>	GTPM_INTERRUPT_PENDING		Default Value:	0b	Access:	RO	This field indicates if iterrups of this category is pending.	
GTPM_INTERRUPT_PENDING									
Default Value:	0b								
Access:	RO								
This field indicates if iterrups of this category is pending.									
3	<table border="1"> <tr> <td colspan="2">VCS2_INTERRUPT_PENDING</td> </tr> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td colspan="2">This field indicates if iterrups of this category is pending.</td> </tr> </table>	VCS2_INTERRUPT_PENDING		Default Value:	0b	Access:	RO	This field indicates if iterrups of this category is pending.	
VCS2_INTERRUPT_PENDING									
Default Value:	0b								
Access:	RO								
This field indicates if iterrups of this category is pending.									
2	<table border="1"> <tr> <td colspan="2">VCS1_INTERRUPT_PENDING</td> </tr> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td colspan="2">This field indicates if iterrups of this category is pending.</td> </tr> </table>	VCS1_INTERRUPT_PENDING		Default Value:	0b	Access:	RO	This field indicates if iterrups of this category is pending.	
VCS1_INTERRUPT_PENDING									
Default Value:	0b								
Access:	RO								
This field indicates if iterrups of this category is pending.									
1	<table border="1"> <tr> <td colspan="2">BLITTER_INTERRUPT_PENDING</td> </tr> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td colspan="2">This field indicates if iterrups of this category is pending.</td> </tr> </table>	BLITTER_INTERRUPT_PENDING		Default Value:	0b	Access:	RO	This field indicates if iterrups of this category is pending.	
BLITTER_INTERRUPT_PENDING									
Default Value:	0b								
Access:	RO								
This field indicates if iterrups of this category is pending.									
0	<table border="1"> <tr> <td colspan="2">RENDER_INTERRUPT_PENDING</td> </tr> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td colspan="2">This field indicates if iterrups of this category is pending.</td> </tr> </table>	RENDER_INTERRUPT_PENDING		Default Value:	0b	Access:	RO	This field indicates if iterrups of this category is pending.	
RENDER_INTERRUPT_PENDING									
Default Value:	0b								
Access:	RO								
This field indicates if iterrups of this category is pending.									

Master start timer

MASTIMER - Master start timer						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000001					
Size (in bits):	32					
Address:	0B438h					
DWord	Bit	Description				
0	31:0	<p>Master start timer value</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>00000000000000000000000000000001b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Master Start Timer (MSTSTTMR). Ipconf_lpfcr_master_start_timer [31:0]. So many clocks are expired before starting the rest of the counters. Time to wait is 256 * value clocks. Value for this register cannot be 0.</p>	Default Value:	00000000000000000000000000000001b	Access:	R/W
Default Value:	00000000000000000000000000000001b					
Access:	R/W					

Max Outstanding Pending TLB Requests 0

GFX_PEND_TLB_0 - Max Outstanding Pending TLB Requests 0			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	04034h		
DWord	Bit	Description	
0	31	TEX Limit Enable Bit	
		Default Value:	0b
		Access:	R/W
	This bit is used to enable the pending TLB requests limitation function for the Texture Cache. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.		
	30	Reserved	
		Default Value:	0b
		Access:	RO
	29:24	TEX TLB Limit Count	
		Default Value:	000000b
		Access:	R/W
	This is the MAX number of Allowed internal pending read requests which require a TLB read.		
	23	DC Limit Enable Bit	
Default Value:		0b	
Access:		R/W	
This bit is used to enable the pending TLB requests limitation function for the Instruction Cache. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.			
22	Reserved		
	Default Value:	0b	
	Access:	RO	
21:16	DC TLB Limit Count		
	Default Value:	000000b	
	Access:	R/W	
This is the MAX number of Allowed internal pending read requests which require a TLB read.			

GFX_PEND_TLB_0 - Max Outstanding Pending TLB Requests 0

15	VF Limit Enable Bit <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>This bit is used to enable the pending TLB requests limitation function for the Vertex Fetch. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
14	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">RO</td> </tr> </table>	Default Value:	0b	Access:	RO
Default Value:	0b				
Access:	RO				
13:8	VF TLB Limit Count <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td style="text-align: center;">000000b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>This is the MAX number of Allowed internal pending read requests which require a TLB read.</p>	Default Value:	000000b	Access:	R/W
Default Value:	000000b				
Access:	R/W				
7	VMC Limit Enable bit <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>This bit is used to enable the pending TLB requests limitation function for the Video Motion Compensation. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
6	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">RO</td> </tr> </table>	Default Value:	0b	Access:	RO
Default Value:	0b				
Access:	RO				
5:0	VMC TLB Limit Count <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td style="text-align: center;">000000b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>This is the MAX number of Allowed internal pending read requests which require a TLB read.</p>	Default Value:	000000b	Access:	R/W
Default Value:	000000b				
Access:	R/W				

Max Outstanding Pending TLB Requests 1

GFX_PEND_TLB_1 - Max Outstanding Pending TLB Requests 1				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	04038h			
DWord	Bit	Description		
0	31	SOL Limit Enable Bit		
		<table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This bit is used to enable the pending TLB requests limitation function for the SOL. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.</p>	Default Value:	0b
Default Value:	0b			
Access:	R/W			
	30	Reserved		
		<table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	0b
Default Value:	0b			
Access:	RO			
29:24		SOL TLB Limit Count		
		<table border="1"> <tr> <td>Default Value:</td> <td>000000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This is the MAX number of Allowed internal pending read requests which require a TLB read.</p>	Default Value:	000000b
Default Value:	000000b			
Access:	R/W			
23		L3 Limit Enable Bit		
		<table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This bit is used to enable the pending TLB requests limitation function for the L3. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.</p>	Default Value:	0b
Default Value:	0b			
Access:	R/W			
22		Reserved		
		<table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	0b
Default Value:	0b			
Access:	RO			
21:16		L3 TLB Limit Count		
		<table border="1"> <tr> <td>Default Value:</td> <td>000000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This is the MAX number of Allowed internal pending read requests which require a TLB read.</p>	Default Value:	000000b
Default Value:	000000b			
Access:	R/W			

GFX_PEND_TLB_1 - Max Outstanding Pending TLB Requests 1

15	RCZ Limit Enable Bit	Default Value:	0b
		Access:	R/W
This bit is used to enable the pending TLB requests limitation function for the Render Depth Cache. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.			
14	Reserved	Default Value:	0b
		Access:	RO
13:8	RCZ TLB Limit Count	Default Value:	000000b
		Access:	R/W
RCZ TLB Limit Count Project: All Format: U6 This is the MAX number of Allowed internal pending read requests which require a TLB read.			
7	RCC Limit Enable bit	Default Value:	0b
		Access:	R/W
This bit is used to enable the pending TLB requests limitation function for the Render Color Cache. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.			
6	Reserved	Default Value:	0b
		Access:	RO
5:0	RCC TLB Limit Count	Default Value:	000000b
		Access:	R/W
This is the MAX number of Allowed internal pending read requests which require a TLB read.			

MAX Requests Allowed - GAM

GFX_MAX_REQ_COUNT - MAX Requests Allowed - GAM		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x43F20101	
Size (in bits):	32	
Address:	04AA4h	
Programmable Request Count - GAM		
DWord	Bit	Description
0	31:26	GAP Writes Max Request Limit Count
		Default Value: 010000b
	Access: R/W	
	This is the MAX number of Allowed Write Requests Count - These counters keep track of the accepted write requests from all GAP clients (RCZ, HiZ, Stc, RCC, L3). Minimum count value must be = 1.	
	25:20	CVS Max Request Limit Count
Default Value: 111111b		
Access: R/W		
This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each client. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.		
19	Reserved	
	Default Value: 0b	
Access: RO		
18:13	L3 Max Request Limit Count	
	Default Value: 010000b	
Access: R/W		
This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each client. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.		
12	Reserved	
	Default Value: 0b	
Access: RO		

GFX_MAX_REQ_COUNT - MAX Requests Allowed - GAM

11:6	Z Request Limit Count		
	Default Value:	000100b	
	Access:	R/W	
<p>This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each client. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.</p>			
5:0	RCC Request Limit Count		
	Default Value:	000001b	
	Access:	R/W	
<p>This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each client. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.</p>			

MAX Requests Allowed - MFX

MEDIA_MAX_REQ_COUNT - MAX Requests Allowed - MFX			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x10201020		
Size (in bits):	32		
Address:	04AA0h		
Programmable Request Count - MFX			
DWord	Bit	Description	
0	31:24	GFX Max Request Limit Count	
		Default Value:	00010000b
		Access:	R/W
		This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.	
		MFX Max Request Limit Count	
23:16		Default Value:	00100000b
		Access:	R/W
		This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.	
15:14		Reserved	
		Default Value:	00b
		Access:	RO
13:8		VLF Max Request Limit Count	
		Default Value:	010000b
		Access:	R/W
		This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each client. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.	
7:6		Reserved	
		Default Value:	00b
		Access:	RO

MEDIA_MAX_REQ_COUNT - MAX Requests Allowed - MFX

	5:0	MFX Max Request Limit Count	
		Default Value:	100000b
		Access:	R/W
<p>This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each client. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.</p>			

MAX Requests Allowed - VEBX and BLT

VEBX_BLIT_MAX_REQ_COUNT - MAX Requests Allowed - VEBX and BLT			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x08081020		
Size (in bits):	32		
Address:	04AA8h		
Programmable Request Count - VEBX and BLT			
DWord	Bit	Description	
0	31:24	BLT Max Request Limit Count	
		Default Value:	00001000b
		Access:	R/W
		This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (Miss/Hit/Present).	
23:16		VEBX Max Request Limit Count	
		Default Value:	00001000b
		Access:	R/W
		This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (Miss/Hit/Present).	
15:8		VLF1 Max Request Limit Count	
		Default Value:	00010000b
		Access:	R/W
		This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (Miss/Hit/Present).	
7:0		MFX1 Max Request Limit Count	
		Default Value:	00100000b
		Access:	R/W
		This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (Miss/Hit/Present).	

MBC Control Register

MBCTL - MBC Control Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0907Ch			
MBC Control Register				
DWord	Bit	Description		
0	31:17	<p>ECORSVD</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>ECO purposes Reserved</p>	Access:	R/W
	Access:	R/W		
	16	<p>Fuse Write to VCR as Nonposted</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>0 - Default - MBCunit will send the VCR (Fuse) writes as Posted Write cycles 1 - MBCunit will send the VCR (Fuse) writes as Non Posted Write cycles</p>	Access:	R/W
	Access:	R/W		
	15:8	<p>RSVD</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>RSVD</p>	Access:	RO
	Access:	RO		
	7	<p>Disable Wait for G3d Outbound empty in MAE</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>0 - Wait for SQempty for MAE update Flow 1 - MBC MAE update FSM will not wait for the SQempty to complete the FSM</p>	Access:	R/W
	Access:	R/W		
6:5	<p>RSVD</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>RSVD</p>	Access:	RO	
Access:	RO			
4	<p>RSVD</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>RSVD</p>	Access:	RO	
Access:	RO			
3	<p>RSVD</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>RSVD</p>	Access:	RO	
Access:	RO			

MBCTL - MBC Control Register			
2	<p>BME Update Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>BME update Enable - 0 - Default Mae Update is not Enable. MBC will ignore all theBME updates from SA. 1- BME update is Enabled.</p>	Access:	R/W
Access:	R/W		
1	<p>MAE Update Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>MAE update Enable - 0 - Default Mae Update is not Enable. MBC will ignore all the MAE updates from SA. 1- MAE update is Enabled. MBC will respond to the MAE updates.</p>	Access:	R/W
Access:	R/W		
0	<p>RSVD</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> </table> <p>0 = Use MBC to GAM path with 8B reads (default) 1 = Use MBC to Config Agent register interface with 4B reads</p>	Access:	RO
Access:	RO		

MBDSM

MBDSM - MBDSM			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	1080C0h		
<p>Mirror of base of data stolen memory. Simply a read-only alias to the configuration registers. Used by the MBC for boot context fetches.</p> <p>This register contains the base address of Graphics Data Stolen DRAM memory. Note: This register is in device 0, 0xB0. Mirrored into device2, 0x5C. Graphics Stolen Memory is within DRAM space. The base of stolen memory will always be below 4G</p>			
DWord	Bit	Description	
0	31:20	BDSM	
		Default Value:	000h
		Access:	RO
			<p>BDSM: BASE_OF_Data_STOLEN_MEMORY.</p> <p>This register contains bits 31 to 20 of the base address of Data stolen DRAM memory. For certain GTLC generated accesses, this base register will be added to GTLC provided offset address, forming the full physical address for the PFI fabric. This is also used as a base for VGA paged accesses.</p>
	19:1	RESERVED	
		Default Value:	00000h
		Access:	RO
			Reserved
	0	BDSM_LOCK	
Default Value:		0b	
Access:		RO	
		When set to 1b, this bit will lock all the bits in this register, including itself	

MBGSM

MBGSM - MBGSM						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	108100h					
<p>Mirror of base of graphics stolen memory. Simply a read-only alias to the configuration registers. Used by the MBC for boot context fetches.</p> <p>Base of GTT table in Gfx Stolen Memory Note : This register is located in device 0, 0xB4. Mirrored into Device 2. The GTT table is located within Graphics Stolen Memory in DRAM space.</p> <p>The base of stolen memory will always be below 4G.</p>						
DWord	Bit	Description				
0	31:20	<p>BGSM</p> <table border="1"> <tr> <td>Default Value:</td> <td>000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>BGSM: Gfx Base of GTT Stolen Memory. This register contains bits 31 to 20 of the base address of GTT Table in stolen DRAM memory. BIOS determines base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI offset 50 bits 9:8) from the Graphics Base of Data stolen(PCI offset 5C bits 31:20).</p>	Default Value:	000h	Access:	RO
		Default Value:	000h			
		Access:	RO			
<p>RESERVED</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved</p>	Default Value:	00000h	Access:	RO		
Default Value:	00000h					
Access:	RO					
0	0	<p>BGSM_LOCK</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>This bit will lock all writeable settings in this register including itself</p>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					

MD

MD - MD			
Register Space:	PCI: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	00098h		
Message Data			
DWord	Bit	Description	
0	31:16	RESERVED	
		Default Value:	0000h
		Access:	RO
	Reserved		
	15:0	DATA	
		Default Value:	0000h
Access:		R/W	
MD: This 16-bit field is programmed by system software. This forms the lower word of data for the MSI write transaction.			

MEDFW_ACK

MEDFW_ACK - MEDFW_ACK						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	1300BCh					
This register contains the per thread force wake acknowledge bits for the Media power well.						
DWord	Bit	Description				
0	31:16	<p>RESERVED</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved.</p>	Default Value:	0000h	Access:	RO
	Default Value:	0000h				
Access:	RO					
15:0	<p>FWAKEMEDIAACK</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Force Wake Media request bits. Driver must poll on the corresponding bit to confirm that the well has woken. For example, if 13_00B8[0] is written to a 1 (along with 13_00B8[16]='1'), then bit0 of this register indicates when the force wake request has been completed.</p>	Default Value:	0000h	Access:	RO	
Default Value:	0000h					
Access:	RO					

Media 1 TLB Control Register

M1TCR - Media 1 TLB Control Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	04264h			
DWord	Bit	Description		
0	31:1	Reserved		
		<table border="1"> <tr> <td>Default Value:</td> <td>00000000000000000000000000000000b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	00000000000000000000000000000000b
Default Value:	00000000000000000000000000000000b			
Access:	RO			
0	0	Invalidate TLBs on the corresponding Engine		
		<table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. This bit is self clear.</p>	Default Value:	0b
Default Value:	0b			
Access:	R/W			

Media 2 TLB Control Register

M2TCR - Media 2 TLB Control Register			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	04268h		
DWord	Bit	Description	
0	31:1	Reserved	
		Default Value:	00000000000000000000000000000000b
		Access:	RO
	0	Invalidate TLBs on the corresponding Engine	
	Default Value:	0b	
	Access:	R/W	
SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. This bit is self clear.			

Media forcewake request

MEDFW_REQ - Media forcewake request			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	1300B8h		
<p>This register contains per thread force wake request bits for the Render power Well. The upper 16 bits act as masks for the lower 16 bits. Bit 31 masks bit 15 and bit 16 masks bit 0.</p> <ol style="list-style-type: none"> 1. Driver writes to GPM force wake request bit. (VV will have a Render(13_00B0(15:0)) and a Media (13_00B8(15:0)) bits.) 2. The GPM responds by writing (via PLINK) to 1300B4[15:0] or 1300BC[15:0] register. 3. Driver polls (1300B4[15:0] and/or 1300BC[15:0])status until 1... indicating that that well has completed wake sequence. <p>Since the registers are per thread, only the specific bit that was forced should be checked for status.</p>			
DWord	Bit	Description	
0	31:16	FWAKEMEDIAREQMSK	
		Default Value:	0000h
		Access:	RO
		Mask bits for lower 16 bits to avoid a read modify/write. If '0', the corresponding bit in [15:0] is not changed. If '1', the corresponding bit in [15:0] is changed to the value in [15:0]	
15	15	FWAKEMEDIAREQ15	
		Default Value:	0b
		Access:	R/W
		Force Wake Media request 15.	
14	14	FWAKEMEDIAREQ14	
		Default Value:	0b
		Access:	R/W
		Force Wake Render request 14.	
13	13	FWAKEMEDIAREQ13	
		Default Value:	0b
		Access:	R/W

MEDFW_REQ - Media forcewake request		
		Force Wake Render request 13.
12	FWAKEMEDIAREQ12	
	Default Value:	0b
	Access:	R/W
		Force Wake Render request 12.
11	FWAKEMEDIAREQ11	
	Default Value:	0b
	Access:	R/W
		Force Wake Render request 11.
10	FWAKEMEDIAREQ10	
	Default Value:	0b
	Access:	R/W
		Force Wake Render request 10.
9	FWAKEMEDIAREQ9	
	Default Value:	0b
	Access:	R/W
		Force Wake Render request 9.
8	FWAKEMEDIAREQ8	
	Default Value:	0b
	Access:	R/W
		Force Wake Render request 8.
7	FWAKEMEDIAREQ7	
	Default Value:	0b
	Access:	R/W
		Force Wake Render request 7.
6	FWAKEMEDIAREQ6	
	Default Value:	0b
	Access:	R/W
		Force Wake Render request 6.
5	FWAKEMEDIAREQ5	
	Default Value:	0b

MEDFW_REQ - Media forcewake request						
		<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>Force Wake Render request 5.</p>	Access:	R/W		
Access:	R/W					
	4	<p>FWAKEMEDIAREQ4</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Force Wake Render request 4.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	3	<p>FWAKEMEDIAREQ3</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Force Wake Render request 3.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	2	<p>FWAKEMEDIAREQ2</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Force Wake Render request 2.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	1	<p>FWAKEMEDIAREQ1</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Force Wake Render request 1.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	0	<p>FWAKEMEDIAREQ0</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Force Wake Render request 0.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					

Media Power Meter Counter

MPMCNT - Media Power Meter Counter		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A270h-0A273h	
DWord	Bit	Description
0	31	Media Power Meter Counter Overflow Access: RO
	30:0	Media PWRMTR Counter Access: RO

Media Power Meter Counter No Clear

MPMCNTCLR - Media Power Meter Counter No Clear				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A288h-0A28Bh			
Formerly cleared the count and the overflow bit, but now it is just a read-only value.				
DWord	Bit	Description		
0	31	<p>Media Power Meter Counter Overflow No Clear</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Formerly cleared the overflow bit, but now it is just a read-only value.</p>	Access:	RO
	Access:	RO		
30:0	<p>Media PWRMTR Counter No Clear</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Formerly cleared the count, but now is just a read-only value.</p>	Access:	RO	
Access:	RO			

MEDIARCOCOUNTER

MEDIARCOCOUNTER - MEDIARCOCOUNTER						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	13811Ch					
Description		Project				
<p>This register contains the total RC0 residency (Media powered on and clocks running) time that Media was in since boot.</p> <p>SOXi Context Save/Restore : No</p> <p>The 40-bit HW counter will wrap around. The only clear condition is CZ reset.</p> <p>When 0x13_8104[15] is set to zero, bits 31:0 of the 40-bit counter are reported. When 0x13_8104[15] is set to one, bits 39:8 of the 40-bit counter are reported.</p> <p>The units are CZ clock cycles.</p> <p>It is up to SW to periodically read this register and do a difference from the last time it was read. The primary usage for this register is for power characterization.</p> <p>0x13_8104[5] controls if this register should count or if it should be gated: 0= clear, 1=count</p> <p>This register will be cleared when A024[8] is set to 1</p>		CHV, BSW				
<p>This register contains the total RC0 residency (Media powered on and clocks running) time that Media was in since boot.</p> <p>SOXi Context Save/Restore : No</p> <p>The 40-bit HW counter will wrap around. The only clear condition is CZ reset.</p> <p>When 0x13_8104[15] is set to zero, bits 31:0 of the 40-bit counter are reported. When 0x13_8104[15] is set to one, bits 39:8 of the 40-bit counter are reported.</p> <p>The units are CZ clock cycles.</p> <p>It is up to SW to periodically read this register and do a difference from the last time it was read. The primary usage for this register is for power characterization.</p> <p>0x13_8104[5] controls if this register should count or if it should be gated: 0= clear, 1=count</p>		CHV, BSW				
DWord	Bit	Description				
0	31:0	<p>MEDIARCOTIME</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Media RC0 Residency Counter.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

MEDIARC1COUNTER

MEDIARC1COUNTER - MEDIARC1COUNTER						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	138114h					
<p>This register contains the total RC1 residency (Media powered on and clock gated) time that Media was in since boot.</p> <p>SOXi Context Save/Restore : No</p> <p>The 40-bit HW counter will wrap around. The only clear condition is CZ reset.</p> <p>When 0x13_8104[15] is set to zero, bits 31:0 of the 40-bit counter are reported. When 0x13_8104[15] is set to one, bits 39:8 of the 40-bit counter are reported.</p> <p>The units are CZ clock cycles.</p> <p>It is up to SW to periodically read this register and do a difference from the last time it was read. The primary usage for this register is for power characterization.</p> <p>0x13_8104[3] controls if this register should count or if it should be gated: 0= clear, 1=count</p>						
DWord	Bit	Description				
0	31:0	<p>MEDIARC1TIME</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Media RC1 Residency Counter.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

MEDIARC6COUNTER

MEDIARC6COUNTER - MEDIARC6COUNTER						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	13810Ch					
<p>This register contains the total RC6 residency (Media power gated and clock gated) time that Media was in since boot. The counter will wrap around.</p> <p>SOXi Context Save/Restore : No</p> <p>The time is given in units of CZ clock cycles. The counter will reset on CZ reset going high.</p> <p>This means that a warm reset will also reset this counter and it will also wrap around when it reaches max with no indication that an overflow occurred.</p> <p>This register will freeze the count value (stop counting, but not reset) when pmu_gvd_renwakeack_nczfwoh=1.</p> <p>This register will count whenever pmu_gvd_renwakeack_nczfwoh=0.</p> <p>When 0x13_8104[15] is set to zero, bits 31:0 of the 40-bit counter are reported. When 0x13_8104[15] is set to one, bits 39:8 of the 40-bit counter are reported.</p> <p>The units are CZ clock cycles.</p> <p>It is up to SW to periodically read this register and do a difference from the last time it was read. The primary usage for this register is for power characterization.</p> <p>0x13_8104[1] controls if this register should count or if it should be gated: 0= clear, 1=count</p>						
DWord	Bit	Description				
0	31:0	<p>MEDIARC6TIME</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Media Residency Counter.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

MEMBOUNDCOUNTER

MEMBOUNDCOUNTER - MEMBOUNDCOUNTER						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	138120h					
<p>SOXi Context Save/Restore : No</p> <p>The 40-bit HW counter will wrap around. The only clear condition is CZ reset.</p> <p>When 0x13_8104[15] is set to zero, bits 31:0 of the 40-bit counter are reported. When 0x13_8104[15] is set to one, bits 39:8 of the 40-bit counter are reported.</p> <p>The units are CZ clock cycles.</p> <p>It is up to SW to periodically read this register and do a difference from the last time it was read. The primary usage for this register is for power characterization.</p> <p>0x13_8104[6] controls if this register should count or if it should be gated: 0= clear, 1=count</p>						
DWord	Bit	Description				
0	31:0	<p>MEMBOUNDTIME</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Render RC0 Residency Counter.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Message Register

MSGREG - Message Register			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000001		
Size (in bits):	32		
Address:	040D4h		
DWord	Bit	Description	
0	31:16	Mask Bits	
		Default Value:	0000h
		Access:	RO
		Reserved.	
	15	GO_PROTOCOL_GAM_REQUEST15	
		Default Value:	0b
		Access:	R/W
		Reserved.	
	14	GO_PROTOCOL_GAM_REQUEST14	
		Default Value:	0b
		Access:	R/W
		Reserved.	
	13	GO_PROTOCOL_GAM_REQUEST13	
		Default Value:	0b
Access:		R/W	
Reserved.			
12	GO_PROTOCOL_GAM_REQUEST12		
	Default Value:	0b	
	Access:	R/W	
	Reserved.		
11	GO_PROTOCOL_GAM_REQUEST11		
	Default Value:	0b	
	Access:	R/W	
	Reserved.		
10	GO_PROTOCOL_GAM_REQUEST10		
	Default Value:	0b	
	Access:	R/W	
	Reserved.		

MSGREG - Message Register						
	9	GO_PROTOCOL_GAM_REQUEST9 <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Reserved.	Default Value:	0b	Access:	R/W
	Default Value:	0b				
	Access:	R/W				
	8	GO_PROTOCOL_GAM_REQUEST8 <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Reserved.	Default Value:	0b	Access:	R/W
	Default Value:	0b				
	Access:	R/W				
	7	GO_PROTOCOL_GAM_REQUEST7 <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Reserved.	Default Value:	0b	Access:	R/W
	Default Value:	0b				
	Access:	R/W				
	6	GO_PROTOCOL_GAM_REQUEST6 <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Reserved.	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
5	GO_PROTOCOL_GAM_REQUEST5 <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Reserved.	Default Value:	0b	Access:	R/W	
Default Value:	0b					
Access:	R/W					
4	GO_PROTOCOL_GAM_REQUEST4 <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Reserved.	Default Value:	0b	Access:	R/W	
Default Value:	0b					
Access:	R/W					
3	GO_PROTOCOL_GAM_REQUEST3 <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Reserved.	Default Value:	0b	Access:	R/W	
Default Value:	0b					
Access:	R/W					
2	GO_PROTOCOL_GAM_REQUEST2 <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Reserved.	Default Value:	0b	Access:	R/W	
Default Value:	0b					
Access:	R/W					
1	GO_PROTOCOL_GAM_REQUEST1 <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Reserved.	Default Value:	0b	Access:	R/W	
Default Value:	0b					
Access:	R/W					
0	GO_PROTOCOL_GAM_REQUEST0 <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>1b</td> </tr> </table>	Default Value:	1b			
Default Value:	1b					

MSGREG - Message Register							
	<table border="1"><tr><td>Access:</td><td>R/W</td></tr><tr><td colspan="2">0 - GPM to GAM Busy Ack Indication.</td></tr><tr><td colspan="2">1 - GPM to GAM Idle Ack Indication.</td></tr></table>	Access:	R/W	0 - GPM to GAM Busy Ack Indication.		1 - GPM to GAM Idle Ack Indication.	
Access:	R/W						
0 - GPM to GAM Busy Ack Indication.							
1 - GPM to GAM Idle Ack Indication.							

Messaging Register for GPMunit

MSG_GPM - Messaging Register for GPMunit		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00C00h	
<p>Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. To set bit0, for example, the data would be 0x0001_0001. To clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.</p>		
DWord	Bit	Description
0	31:16	Reserved Access: RO
	15	GPM Messages Bit 15 Access: R/W Placeholder for GPM Messages. RPMunit could self-clear these bits upon sampling.
	14	GPM Messages Bit 14 Access: R/W Placeholder for GPM Messages. RPMunit could self-clear these bits upon sampling.
	13	GPM Messages Bit 13 Access: R/W Placeholder for GPM Messages. RPMunit could self-clear these bits upon sampling.
	12	GPM Messages Bit 12 Access: R/W Placeholder for GPM Messages. RPMunit could self-clear these bits upon sampling.
	11	GPM Messages Bit 11 Access: R/W Placeholder for GPM Messages. RPMunit could self-clear these bits upon sampling.

MSG_GPM - Messaging Register for GPMunit

10	GPM Messages Bit 10	
	Access:	R/W
	Placeholder for GPM Messages. RPMunit could self-clear these bits upon sampling.	
	GPM Messages Bit 9	
	Access:	R/W
	Placeholder for GPM Messages. RPMunit could self-clear these bits upon sampling.	
	GPM Messages Bit 8	
	Access:	R/W
7	GPM Messages Bit 7	
	Project:	CHV, BSW
	Access:	R/W
Placeholder for GPM Messages RPMunit could self-clear these bits upon sampling.		
6	GPM Messages Bit 6	
	Project:	CHV, BSW
	Access:	R/W
Placeholder for GPM Messages. RPMunit could self-clear these bits upon sampling.		
5	GPM Messages Bit 5	
	Project:	CHV, BSW
	Access:	R/W
Placeholder for GPM Messages. RPMunit could self-clear these bits upon sampling.		
4	Request to send CPD Exit Ack Message on EventBus (U2C)	
	Access:	R/W
Request from GPMunit for RPMunit to send CPD_EXIT_ACK message on the Eventbus. RPMunit self-clears this bit upon sampling.		
3	Request to send CPD Enter Ack Message on EventBus (U2C)	
	Access:	R/W
Request from GPMunit for RPMunit to send CPD_ENTER_ACK message on the Eventbus. RPMunit self-clears this bit upon sampling.		

MSG_GPM - Messaging Register for GPMunit

	2	Request to send Credit Active Deassert Message on EventBus (U2C)		
		<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Request from GPMunit for RPMunit to send CREDIT_ACTIVE_DEASSERT message on the Eventbus. RPMunit self-clears this bit upon sampling.</p>	Access:	R/W
	Access:	R/W		
1	Request to send Credit Active Assert Message on EventBus (U2C)			
		<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Request from GPMunit for RPMunit to send CREDIT_ACTIVE_ASSERT message on the Eventbus. RPMunit self-clears this bit upon sampling.</p>	Access:	R/W
Access:	R/W			
	0	Request to send IDI Shutdown Ack Message on EventBus (U2C)		
		<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Request from GPMunit for RPMunit to send IDI_SHUTDOWN_ACK message on the Eventbus. RPMunit self-clears this bit upon sampling.</p>	Access:	R/W
Access:	R/W			

Messaging Register for MDRBunit

MSG_MDRB - Messaging Register for MDRBunit		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Default Value:	0x00000001	
Size (in bits):	32	
Address:	00C08h	
<p>Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. To set bit0, for example, the data would be 0x0001_0001. To clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.</p>		
DWord	Bit	Description
0	31:16	Reserved Access: RO
	15:2	MDRB Messages Access: R/W Placeholder for MDRB Messages. MDRBunit could self-clear these bits upon sampling.
	1	RFO Enable/Disable Ack for RPM (internal) RFO Request Access: R/W RFO Enable/Disable Ack for Internal RFO Request. Enable Ack = 1'b1 Disable Ack = 1'b0
	0	RFO Enable/Disable Ack for U2C (Evtentbus) RFO Request Default Value: 1b Access: R/W RFO Enable/Disable Ack for U2C RFO Request. Enable Ack = 1'b1 Disable Ack = 1'b0

Messaging Register for MGSRunit

MSG_MGSR - Messaging Register for MGSRunit				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	00C04h			
<p>Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. To set bit0, for example, the data would be 0x0001_0001. To clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.</p>				
DWord	Bit	Description		
0	31:16	Reserved Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td>RO</td></tr></table>		RO
		RO		
15:0	MGSR Messages Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td>R/W</td></tr></table> Placeholder for MGSR Messages. MGSRunit could self-clear these bits upon sampling.		R/W	
	R/W			

MFC_AVC_CABAC_INSERTION_COUNT

AVC_CABAC_INSERTION_COUNT - MFC_AVC_CABAC_INSERTION_COUNT		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	128ACh	
Valid Projects:	CHV, BSW	
<p>This register stores the count in bytes of CABAC ZERO_WORD insertion. It is primarily provided for statistical data gathering.</p>		
DWord	Bit	Description
0	31:0	<p>MFC AVC Cabac Insertion Count</p> <p>Total number of bytes in the bitstream output before for the CABAC zero word insertion. This count is updated each time when the insertion count is incremented.</p>

MFC_AVC Bitstream Decoding Front-End Parsing Logic Error Counter

MFC_VIN_AVD_ERROR_CNTR - MFC_AVC Bitstream Decoding Front-End Parsing Logic Error Counter				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Trusted Type:	1			
Address:	12804h			
Valid Projects:	CHV, BSW			
DWord	Bit	Description		
0	31:0	Reserved		
avd_error_flagsR[31:0]		Format: <table border="1"> <tr> <td></td> <td>MBZ</td> </tr> </table>		MBZ
	MBZ			

MFC Image Status Control

MFC_IMAGE_STATUS_CONTROL - MFC Image Status Control						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	VideoCS					
Default Value:	0x00000000					
Access:	RO					
Size (in bits):	32					
Trusted Type:	1					
Address:	128B8h					
Valid Projects:	CHV, BSW					
This register stores the suggested data for next frame in multi-pass.						
DWord	Bit	Description				
0	31:24	Cumulative slice delta QP				
	23:16	QP Value suggested slice QP delta value for frame level Rate control. This value can be +ve or -ve				
	15	QP-Polarity Change Cumulative slice delta QP polarity change.				
	14:13	Num-Pass Polarity Change Number of passes after cumulative slice delta QP polarity changes.				
	12	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ
	Project:	CHV, BSW				
	Format:	MBZ				
	11:8	Total Num-Pass				
	7:4	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
	Format:	MBZ				
3	Missing Huffman Code <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table> <p>Jpeg HW encoder reports if Huffman table entry is missing.</p>	Project:	CHV, BSW			
Project:	CHV, BSW					
2	Panic Panic triggered to avoid too big packed file.					
1	Frame Bit Count Frame Bit count over-run/under-run flag					
0	Max Conformance Flag Max Macroblock conformance flag or Frame Bit count over-run/under-run					

MFC Image Status Mask

MFC_IMAGE_STATUS_MASK - MFC Image Status Mask		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	128B4h	
Valid Projects:	CHV, BSW	
This register stores the image status(flags).		
DWord	Bit	Description
0	31:0	Control Mask Control Mask for dynamic frame repeat.

MFC QP Status Count

MFC_QUP_CT - MFC QP Status Count				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoCS			
Default Value:	0x00000000			
Access:	RO			
Size (in bits):	32			
Trusted Type:	1			
Address:	128BCh			
Valid Projects:	CHV, BSW			
This register stores the suggested QP COUNTS in multi-pass.				
DWord	Bit	Description		
0	31:24	<p>Cumulative QP Adjust</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%; text-align: center;">U8</td> </tr> </table> <p>Cumulative QP adjustment after multiple passes. If there is no need to multi-pass, this value would be zero. (This is in sign magnitude form).</p>	Format:	U8
	Format:	U8		
23:0	<p>Cumulative QP</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%; text-align: center;">U24</td> </tr> </table> <p>Cumulative QP for all MB of a Frame (Can be used for computing average QP).</p>	Format:	U24	
Format:	U24			

MFD Error Status

MFD_ERROR_STATUS - MFD Error Status				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoCS			
Default Value:	0x00000000			
Access:	RO			
Size (in bits):	32			
Trusted Type:	1			
Address:	12800h			
Valid Projects:	CHV, BSW			
<p>This register stores the error status flags and count reports by the bit-stream decoder. This register is not part of hardware context save and restore. Driver should read the content prior to starting a new batch/frame.</p>				
DWord	Bit	Description		
0	31:20	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>This field is currently reserved</p>	Format:	MBZ
	Format:	MBZ		
	19:16	<p>AVC Short Format Error Flags</p> <table border="1" style="width: 100%;"> <tr> <td>Exists If:</td> <td>// AVC Short Format == Ture</td> </tr> </table> <p>Bit-stream error detected by VLD short format bit-stream decoder. These flags are reset at the beginning of a frame and updated until starting of another frame.</p> <p>[19] – Slice Type SE Error Flag – Invalid Slice Type SE</p> <p>[18] – MMCO SE Error Flag – Invalid memory management control operation SE. MMCO Loop does not end (mmco control != 0) even after all MMCO SEs are decoded OR MMCO SEs are still being decoded and MMCO SE loop end (mmco control == 0) is hit</p> <p>[17] – Reordering IDC Error Flag – Syntax Element modification_of_pic_nums_idc >= 6 OR modification_of_pic_nums_idc != 3 (end of reordering loop) but reordering count has already hit maximum value</p> <p>[16] – Premature bitstream end is hit before finishing slice header decode</p>	Exists If:	// AVC Short Format == Ture
Exists If:	// AVC Short Format == Ture			
15:0	<p>Bit-stream Error flags</p> <table border="1" style="width: 100%;"> <tr> <td>Exists If:</td> <td>// AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True</td> </tr> </table> <p>Bitstream error detected by the VLD bit-steram decoder. These flags are reset at the beginning of a frame and updated until starting of another frame.</p> <p>AVC CAVLC: Please refer to AVC CAVLC table for each bit field</p> <p>AVC CABAC: Please refer to AVC CABAC table for each bit field</p> <p>VC1: Please refer to VC1 table for each bit field</p> <p>MPEG2: Please refer to MPEG2 table for each bit field</p>	Exists If:	// AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True	
Exists If:	// AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True			

MFD Picture Parameter

MFD_PICTURE_PARAM - MFD Picture Parameter				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Trusted Type:	1			
Address:	12820h			
Valid Projects:	CHV, BSW			
DWord	Bit	Description		
0	31:0	Reserved <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			

MFX_Memory_Latency_Count1

MFX_LAT_CT1 - MFX_Memory_Latency_Count1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	12870h	
Valid Projects:	CHV, BSW	
<p>This register stores the max and min memory latency counts reported on reference read requests. This register is not part of hardware context save and restore.</p>		
DWord	Bit	Description
0	31:24	<p>Max Request Count This field indicates the maximum number of requests allowed by the memory sub-system channel.</p>
	23:16	<p>Current Request Count This field indicates the number of requests currently outstanding in the memory sub-system. This field should report with a value of zero at the end of frame; otherwise the motion compensation engine is most likely hung waiting for read data to be returned from sub-system.</p>
	15:8	<p>MFX Reference picture read request - Max Latency Count in 8xMedia clock cycles This field reports the maximum memory latency count on all reference reads requested by the motion compensation engine.</p>
	7:0	<p>MFX Reference picture read request - Min Latency Count in 8xMedia clock cycles This field reports the minimum memory latency count on all reference reads requested by the motion compensation engine.</p>

MFX0 Context Element Descriptor (High Part)

MFX0_CTX_EDR_H - MFX0 Context Element Descriptor (High Part)						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04444h					
DWord	Bit	Description				
0	31:0	MFX0 Context Element Descriptor (High Part) <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

MFX0 Context Element Descriptor (Low Part)

MFX0_CTX_EDR_L - MFX0 Context Element Descriptor (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000009	
Size (in bits):	32	
Address:	04440h	
DWord	Bit	Description
0	31:0	MFX0 Context Element Descriptor (Low Part)
		Default Value: 00000009h
		Access: R/W

MFX0 Context Element Descriptor (Low Part)

MFX0_CTX_EDR_L - MFX0 Context Element Descriptor (Low Part)						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000009					
Size (in bits):	32					
Address:	04440h					
DWord	Bit	Description				
0	31:0	MFX0 Context Element Descriptor <table border="1"> <tr> <td>Default Value:</td> <td>00000009h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Default Value:	00000009h	Access:	R/W
Default Value:	00000009h					
Access:	R/W					

MFX0 PDP0/PML4/PASID Descriptor (High Part)

MFX0_CTX_PDP0_H - MFX0 PDP0/PML4/PASID Descriptor (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0444Ch	
DWord	Bit	Description
0	31:0	MFX0 PDP0/PML4/PASID Descriptor (High Part)
		Default Value: 00000000h
		Access: R/W

MFX0 PDP0/PML4/PASID Descriptor (Low Part)

MFX0_CTX_PDP0_L - MFX0 PDP0/PML4/PASID Descriptor (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04448h	
DWord	Bit	Description
0	31:0	MFX0 PDP0/PML4/PASID Descriptor (Low Part) Default Value: 00000000h Access: R/W

MFX0 PDP1 Descriptor Register (High Part)

MFX0_CTX_PDP1_H - MFX0 PDP1 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04454h	
DWord	Bit	Description
0	31:0	MFX0 PDP1 Descriptor Register (High Part)
		Default Value: 00000000h
		Access: R/W

MFX0 PDP1 Descriptor Register (Low Part)

MFX0_CTX_PDP1_L - MFX0 PDP1 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04450h	
DWord	Bit	Description
0	31:0	MFX0 PDP1 Descriptor Register (Low Part)
		Default Value: 00000000h
		Access: R/W

MFX0 PDP2 Descriptor Register (High Part)

MFX0_CTX_PDP2_H - MFX0 PDP2 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0445Ch	
DWord	Bit	Description
0	31:0	MFX0 PDP2 Descriptor Register (High Part)
		Default Value: 00000000h
		Access: R/W

MFX0 PDP2 Descriptor Register (Low Part)

MFX0_CTX_PDP2_L - MFX0 PDP2 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04458h	
DWord	Bit	Description
0	31:0	MFX0 PDP2 Descriptor Register (Low Part)
		Default Value: 00000000h
		Access: R/W

MFX0 PDP3 Descriptor Register (High Part)

MFX0_CTX_PDP3_H - MFX0 PDP3 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04464h	
DWord	Bit	Description
0	31:0	MFX0 PDP3 Descriptor Register (High Part)
		Default Value: 00000000h
		Access: R/W

MFX0 PDP3 Descriptor Register (Low Part)

MFX0_CTX_PDP3_L - MFX0 PDP3 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04460h	
DWord	Bit	Description
0	31:0	MFX0 PDP3 Descriptor Register (Low Part)
		Default Value: 00000000h
		Access: R/W

MFX1 Context Element Descriptor (High Part)

MFX1_CTX_EDR_H - MFX1 Context Element Descriptor (High Part)						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04484h					
DWord	Bit	Description				
0	31:0	MFX1 Context Element Descriptor (High Part) <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

MFx1 Context Element Descriptor (Low Part)

MFx1_CTX_EDR_L - MFx1 Context Element Descriptor (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000009	
Size (in bits):	32	
Address:	04480h	
DWord	Bit	Description
0	31:0	MFx1 Context Element Descriptor (Low Part)
		Default Value: 00000009h
		Access: R/W

MFX1 Context Element Descriptor (Low Part)

MFX1_CTX_EDR_L - MFX1 Context Element Descriptor (Low Part)						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000009					
Size (in bits):	32					
Address:	04480h					
DWord	Bit	Description				
0	31:0	MFX1 Context Element Descriptor <table border="1"> <tr> <td>Default Value:</td> <td>00000009h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Default Value:	00000009h	Access:	R/W
Default Value:	00000009h					
Access:	R/W					

MFX1 PDP0/PML4/PASID Descriptor (High Part)

MFX1_CTX_PDP0_H - MFX1 PDP0/PML4/PASID Descriptor (High Part)						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0448Ch					
DWord	Bit	Description				
0	31:0	MFX1 PDP0/PML4/PASID Descriptor (High Part) <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

MFx1 PDP0/PML4/PASID Descriptor (Low Part)

MFx1_CTX_PDP0_L - MFx1 PDP0/PML4/PASID Descriptor (Low Part)						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04488h					
DWord	Bit	Description				
0	31:0	MFx1 PDP0/PML4/PASID Descriptor (Low Part) <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

MFX1 PDP1 Descriptor Register (High Part)

MFX1_CTX_PDP1_H - MFX1 PDP1 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04494h	
DWord	Bit	Description
0	31:0	MFX1 PDP1 Descriptor Register (High Part)
		Default Value: 00000000h
		Access: R/W

MFx1 PDP1 Descriptor Register (Low Part)

MFx1_CTX_PDP1_L - MFx1 PDP1 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04490h	
DWord	Bit	Description
0	31:0	MFx1 PDP1 Descriptor Register (Low Part)
		Default Value: 00000000h
		Access: R/W

MFX1 PDP2 Descriptor Register (High Part)

MFX1_CTX_PDP2_H - MFX1 PDP2 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0449Ch	
DWord	Bit	Description
0	31:0	MFX1 PDP2 Descriptor Register (High Part)
		Default Value: 00000000h
		Access: R/W

MFX1 PDP2 Descriptor Register (Low Part)

MFX1_CTX_PDP2_L - MFX1 PDP2 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04498h	
DWord	Bit	Description
0	31:0	MFX1 PDP2 Descriptor Register (Low Part)
		Default Value: 00000000h
		Access: R/W

MFX1 PDP3 Descriptor Register (High Part)

MFX1_CTX_PDP3_H - MFX1 PDP3 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044A4h	
DWord	Bit	Description
0	31:0	MFX1 PDP3 Descriptor Register (High Part)
		Default Value: 00000000h
		Access: R/W

MFX1 PDP3 Descriptor Register (Low Part)

MFX1_CTX_PDP3_L - MFX1 PDP3 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044A0h	
DWord	Bit	Description
0	31:0	MFX1 PDP3 Descriptor Register (Low Part)
		Default Value: 00000000h
		Access: R/W

MFX Frame BitStream SE/BIN Count

MFX_SE-BIN_CT - MFX Frame BitStream SE/BIN Count		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	1286Ch	
Valid Projects:	CHV, BSW	
<p>This register stores the number of BINs (AVC CABAC) and SEs (CAVLD, VLD) decoded in a frame. This register is not part of hardware context save and restore.</p>		
DWord	Bit	Description
0	31:0	<p>MFX Frame Bit-stream SE/BIN Count</p> <p>Total number of BINs/SEs decoded in current frame. This number is used with frame performance count to derive Bin/clock or SE/clock.</p>

MFX Frame Macroblock Count

MFX_MB_COUNT - MFX Frame Macroblock Count		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	12868h	
Valid Projects:	CHV, BSW	
<p>This register stores the number of Macro-blocks decoded/encoded in current frame. This register is not part of hardware context save and restore.</p>		
DWord	Bit	Description
0	31:20	MBZ
		Exists If: // JPEG == True
		Format: MBZ
		This field is currently reserved
31:16	31:16	Intra MB Count
		Exists If: // AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True
		Format: U16
19:0	19:0	JPEG Block Count
		Exists If: // JPEG == True
		Format: U20
		This 20-bit field indicates the number of 8x8 blocks within the JPEG frame. This field is clear at the start of decoding a new frame.
15:0	15:0	Number of MB Concealment
		Exists If: // AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True
<p>This 16-bit field indicates the number of MB is concealed by hardware. This field is clear at the start of decoding a new frame.</p>		

MFX Frame Motion Comp Miss Count

MFX_MISSION_CT - MFX Frame Motion Comp Miss Count				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoCS			
Default Value:	0x00000000			
Access:	RO			
Size (in bits):	32			
Trusted Type:	1			
Address:	12888h			
Valid Projects:	CHV, BSW			
<p>This register stores the total number of cacheline hits occurred in the motion compensation cache per frame. This register is not part of hardware context save and restore.</p>				
DWord	Bit	Description		
0	31:16	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
15:0	<p>MFX Frame Motion Comp cache miss Count Total number of CL misses occurred in the 12KB cache of the motion compensation engine per frame. This number is used along with MFX Frame Motion Comp Read Count to derive motion comp cache miss/hit ratio.</p>			

MFX Frame Motion Comp Read Count

MFX_READ_CT - MFX Frame Motion Comp Read Count				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoCS			
Default Value:	0x00000000			
Access:	RO			
Size (in bits):	32			
Trusted Type:	1			
Address:	12484h			
<p>This register stores the total number of reference picture read requests made by the Motion Compensation engine per frame. This register is not part of hardware context save and restore.</p>				
DWord	Bit	Description		
0	31:20	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
19:0	<p>MFX Frame Motion Comp CL read request Count</p> <p>Total number of reference picture read requests by the motion compensation engine per frame.</p>			

MFX Frame Row-Stored/BitStream Read Count

MFX_ROW-PER-BS_COUNT - MFX Frame Row-Stored/BitStream Read Count				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoCS			
Default Value:	0x00000000			
Access:	RO			
Size (in bits):	32			
Trusted Type:	1			
Address:	12880h			
Valid Projects:	CHV, BSW			
<p>This register stores the total number of row-stored/bit-stream read requests made by the pre-fetch engine per frame. This register is not part of hardware context save and restore.</p>				
DWord	Bit	Description		
0	31:16	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
15:0	<p>MFX row-stored/bit-stream read request Count</p> <p>Total number of row-stored/bit-stream read requests sent by the memory pre-fetch engine per frame.</p>			

MFX LRA 0

MFX_LRA_0 - MFX LRA 0			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x7F403F00		
Size (in bits):	32		
Address:	04A50h		
DWord	Bit	Description	
0	31:24	MFX LRA1 Max	
		Default Value:	01111111b
		Access:	R/W
		Maximum value of programmable LRA1.	
	23:16	MFX LRA1 Min	
		Default Value:	01000000b
		Access:	R/W
		Minimum value of programmable LRA1.	
	15:8	MFX LRA0 Max	
		Default Value:	00111111b
		Access:	R/W
		Maximum value of programmable LRA0.	
	7:0	MFX LRA0 Min	
		Default Value:	00000000b
		Access:	R/W
		Minimum value of programmable LRA0.	

MFX LRA 1

MFX_LRA_1 - MFX LRA 1			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0xFFC0BF80		
Size (in bits):	32		
Address:	04A54h		
DWord	Bit	Description	
0	31:24	MFX LRA3 Max	
		Default Value:	11111111b
		Access:	R/W
		Maximum value of programmable LRA3.	
	23:16	MFX LRA3 Min	
		Default Value:	11000000b
		Access:	R/W
		Minimum value of programmable LRA3.	
	15:8	MFX LRA2 Max	
		Default Value:	10111111b
		Access:	R/W
		Maximum value of programmable LRA2.	
	7:0	MFX LRA2 Min	
		Default Value:	10000000b
		Access:	R/W
		Minimum value of programmable LRA2.	

MFX LRA 2

MFX_LRA_2 - MFX LRA 2			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x0000001B		
Size (in bits):	32		
Address:	04A58h		
DWord	Bit	Description	
0	31:8	Reserved	
		Default Value:	000000h
		Access:	RO
	7:6	VCS LRA	
		Default Value:	00b
		Access:	R/W
			Which LRA should VCS use.
	5:4	VMX LRA	
		Default Value:	01b
		Access:	R/W
			Which LRA should VMX use.
	3:2	VMC LRA	
		Default Value:	10b
		Access:	R/W
			Which LRA should VMC use.
	1:0	VCR LRA	
		Default Value:	11b
		Access:	R/W
			Which LRA should VCRSL1 use.

MFX LRA SL1 0

MFX_LRA_SL1_0 - MFX LRA SL1 0			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x7F403F00		
Size (in bits):	32		
Address:	04A60h		
DWord	Bit	Description	
0	31:24	MFX SL1 LRA1 Max	
		Default Value:	01111111b
		Access:	R/W
		Maximum value of programmable LRA1.	
	23:16	MFX SL1 LRA1 Min	
		Default Value:	01000000b
		Access:	R/W
		Minimum value of programmable LRA1.	
	15:8	MFX SL1 LRA0 Max	
		Default Value:	00111111b
		Access:	R/W
		Maximum value of programmable LRA0.	
	7:0	MFX SL1 LRA0 Min	
		Default Value:	00000000b
		Access:	R/W
		Minimum value of programmable LRA0.	

MFX LRA SL1 1

MFX_LRA_SL1_1 - MFX LRA SL1 1			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0xFFC0BF80		
Size (in bits):	32		
Address:	04A64h		
DWord	Bit	Description	
0	31:24	MFX SL1 LRA3 Max	
		Default Value:	11111111b
		Access:	R/W
		Maximum value of programmable LRA3.	
	23:16	MFX SL1 LRA3 Min	
		Default Value:	11000000b
		Access:	R/W
		Minimum value of programmable LRA3.	
	15:8	MFX SL1 LRA2 Max	
		Default Value:	10111111b
		Access:	R/W
		Maximum value of programmable LRA2.	
	7:0	MFX SL1 LRA2 Min	
		Default Value:	10000000b
		Access:	R/W
		Minimum value of programmable LRA2.	

MFx LRA SL1 2

MFx_LRA_SL1_2 - MFx LRA SL1 2			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x0000001B		
Size (in bits):	32		
Address:	04A68h		
DWord	Bit	Description	
0	31:8	Reserved	
		Default Value:	000000h
		Access:	RO
	7:6	VCSSL1 LRA	
		Default Value:	00b
		Access:	R/W
			Which LRA should VCSSL1 use.
	5:4	VMXSL1 LRA	
		Default Value:	01b
		Access:	R/W
			Which LRA should VMXSL1 use.
	3:2	VMCSL1 LRA	
		Default Value:	10b
		Access:	R/W
			Which LRA should VMCSL1 use.
	1:0	VCRSL1 LRA	
		Default Value:	11b
		Access:	R/W
			Which LRA should VCRSL1 use.

MFX Memory Latency Count2

MFX_LAT_CT2 - MFX Memory Latency Count2				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoCS			
Default Value:	0x00000000			
Access:	RO			
Size (in bits):	32			
Trusted Type:	1			
Address:	12874h			
Valid Projects:	CHV, BSW			
<p>This register stores the accumulative memory latency count on reference picture read requests. This register is not part of hardware context save and restore.</p>				
DWord	Bit	Description		
0	31:26	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
25:0	MFX Reference picture read request - Accumulative Memory Latency Count for the entire frame in 8xMedia clock cycles The accumulative memory latency count of all reference reads requested by motion compensative engine per frame. This number is used with MFX Frame Motion Comp Read Count to derive average memory latency.			

MFX Memory Latency Count3

MFX_LAT_CT3 - MFX Memory Latency Count3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	12878h	
Valid Projects:	CHV, BSW	
<p>This register stores the max and min memory latency counts reported on row-stored/bit-stream read requests. Max and current requests into memory sub-system engine. This register is not part of hardware context save and restore.</p>		
DWord	Bit	Description
0	31:24	<p>Max Request Count This field indicates the maximum number of requests allowed by the memory sub-system channel.</p>
	23:16	<p>Current Request Count This field indicates the number of requests currently outstanding in the memory sub-system. This field should report with a value of zero at the end of frame; otherwise the pre-fetch engine most likely hung waiting for read data to be returned from sub-system.</p>
	15:8	<p>MFX row-stored/bit-stream read request - Max Latency Count in 8xMedia clock cycles This field reports the maximum memory latency count on all row-stored/bit-stream reads requested by the memory pre-fetch engine.</p>
	7:0	<p>MFX row-stored/bit-stream read request - Min Latency Count in 8xMedia clock cycles This field reports the minimum memory latency count on all row-stored/bit-stream reads requested by the memory pre-fetch engine.</p>

MFX Memory Latency Count4

MFX_LAT_CT4 - MFX Memory Latency Count4				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoCS			
Default Value:	0x00000000			
Access:	RO			
Size (in bits):	32			
Trusted Type:	1			
Address:	1287Ch			
Valid Projects:	CHV, BSW			
<p>This register stores the accumulative memory latency count on row-stored/bit-stream read requests. This register is not part of hardware context save and restore.</p>				
DWord	Bit	Description		
0	31:26	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
25:0	MFX row-stored/bit-stream read request - Accumulative Memory Latency Count for the entire frame in 8xMedia clock cycles The accumulative memory latency count of all row-stored/bit-stream reads requested by pre-fetch engine per frame. This number is used with Frame row-stored/bit-stream memory read count to derive average memory latency.			

MFX Pipeline Status Flags

MFX_STATUS_FLAGS - MFX Pipeline Status Flags											
Register Space:	MMIO: 0/2/0										
Project:	CHV, BSW										
Source:	VideoCS										
Default Value:	0x00000000										
Access:	RO										
Size (in bits):	32										
Trusted Type:	1										
Address:	12838h										
Valid Projects:	CHV, BSW										
This register stores the various pipeline status flags. This register is not part of hardware context save and restore.											
DWord	Bit	Description									
0	31:17	Reserved									
	16	MFX Active Frame decoding/encoding is in progress. Set on frame_start; clear on frame_end.									
	15:10	Reserved									
	9	Streamout Enable									
	8	Reserved									
	7	Post Deblocking Mode Enable									
	6	Pre Deblocking Mode Enable									
	5	Decoder Mode Select									
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Configure the MFD Engine for VLD Mode</td> </tr> <tr> <td>1</td> <td>Configure the MFD Engine for IT Mode</td> </tr> </tbody> </table>	Value	Name	0	Configure the MFD Engine for VLD Mode	1	Configure the MFD Engine for IT Mode			
	Value	Name									
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	1	Configure the MFD Engine for IT Mode									
	4	Codec Select									
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Decode</td> </tr> <tr> <td>1</td> <td>Encode</td> </tr> </tbody> </table>	Value	Name	0	Decode	1	Encode				
Value	Name										
0	Decode										
1	Encode										
3:2	Video Mode										
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>MPEG2</td> </tr> <tr> <td>01b</td> <td>VC1</td> </tr> <tr> <td>10b</td> <td>AVC</td> </tr> <tr> <td>11b</td> <td>JPEG</td> </tr> </tbody> </table>	Value	Name	00b	MPEG2	01b	VC1	10b	AVC	11b	JPEG
Value	Name										
00b	MPEG2										
01b	VC1										
10b	AVC										
11b	JPEG										

MFX_STATUS_FLAGS - MFX Pipeline Status Flags											
	1	Decoder Short Format Mode									
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td></td> <td>AVC/VC1 Short Format Mode is in use</td> </tr> <tr> <td>1</td> <td></td> <td>AVC/VC1 Long Format Mode is in use</td> </tr> </tbody> </table>	Value	Name	Description	0		AVC/VC1 Short Format Mode is in use	1		AVC/VC1 Long Format Mode is in use
		Value	Name	Description							
	0		AVC/VC1 Short Format Mode is in use								
	1		AVC/VC1 Long Format Mode is in use								
0	Stitch Mode										
<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td></td> <td>Not in Stitch Mode</td> </tr> <tr> <td>1b</td> <td></td> <td>In the Special Stitch Mode</td> </tr> </tbody> </table>	Value	Name	Description	0b		Not in Stitch Mode	1b		In the Special Stitch Mode		
Value	Name	Description									
0b		Not in Stitch Mode									
1b		In the Special Stitch Mode									

MFX Slice Performance Count

MFX_SLICE_PERFORM_CT - MFX Slice Performance Count		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	12864h	
Valid Projects:	CHV, BSW	
This register stores the number of clock cycles spent decoding/encoding the current slice. This register is not part of hardware context save and restore.		
DWord	Bit	Description
0	31:0	MFX Frame Performance Count Total number of clocks between slice start and slice end. This count is incremented on crm_clk

MGGC

MGGC - MGGC			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000028		
Size (in bits):	32		
Address:	108040h		
Mirror of GMCH Graphics Control Register. Simply a read-only alias to the configuration registers. Used by the MBC for boot context fetches.			
DWord	Bit	Description	
0	31:15	RESERVED	
		Default Value:	00000h
		Access:	RO
Reserved			
14		VAMEN	
		Default Value:	0b
		Access:	RO
Enables the use of the iGFX engines for Versatile Acceleration. 1 - iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 048000h. 0 - iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h.			
13:10		RESERVED	
		Default Value:	0h
		Access:	RO
Reserved			
9:8		GGMS	
		Default Value:	00b
		Access:	RO
GTT Graphics Memory Size (GGMS): This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware will derive the base of GSM from DSM only using the GSM size programmed in the register. Hardware functionality in case of programming this value to Reserved is not guaranteed. 0h: No Preallocated Memory 1h: 2MB of Preallocated Memory 2h: 4MB of Preallocated Memory 3h: 8MB of Preallocated Memory			

MGGC - MGGC

7:3	GMS																																				
	Default Value:	00101b																																			
	Access:	RO																																			
<p>Graphics Mode Select(GMS): This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled. BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0.</p>																																					
<table style="width: 100%; border-collapse: collapse;"> <tr><td style="padding: 2px;">0h = 0MB</td></tr> <tr><td style="padding: 2px;">1h = 32MB</td></tr> <tr><td style="padding: 2px;">2h = 64MB</td></tr> <tr><td style="padding: 2px;">3h = 96MB</td></tr> <tr><td style="padding: 2px;">4h = 128MB</td></tr> <tr><td style="padding: 2px;">5h = 160MB</td></tr> <tr><td style="padding: 2px;">6h = 192MB</td></tr> <tr><td style="padding: 2px;">7h = 224MB</td></tr> <tr><td style="padding: 2px;">8h = 256MB</td></tr> <tr><td style="padding: 2px;">9h = 288MB</td></tr> <tr><td style="padding: 2px;">Ah = 320MB</td></tr> <tr><td style="padding: 2px;">Bh = 352MB</td></tr> <tr><td style="padding: 2px;">Ch = 384MB</td></tr> <tr><td style="padding: 2px;">Dh = 416MB</td></tr> <tr><td style="padding: 2px;">Eh = 448MB</td></tr> <tr><td style="padding: 2px;">Fh = 480MB</td></tr> <tr><td style="padding: 2px;">10h = 512MB</td></tr> <tr><td style="padding: 2px;">11h = 8MB</td></tr> <tr><td style="padding: 2px;">12h = 12MB</td></tr> <tr><td style="padding: 2px;">13h = 16MB</td></tr> <tr><td style="padding: 2px;">14h = 20MB</td></tr> <tr><td style="padding: 2px;">15h = 24MB</td></tr> <tr><td style="padding: 2px;">16h = 28MB</td></tr> <tr><td style="padding: 2px;">17h = 36MB</td></tr> <tr><td style="padding: 2px;">18h = 40MB</td></tr> <tr><td style="padding: 2px;">19h = 44MB</td></tr> <tr><td style="padding: 2px;">1Ah = 48MB</td></tr> <tr><td style="padding: 2px;">1Bh = 52MB</td></tr> <tr><td style="padding: 2px;">1Ch = 56MB</td></tr> <tr><td style="padding: 2px;">1Dh = 60MB</td></tr> <tr><td style="padding: 2px;">1Eh = Reserved</td></tr> <tr><td style="padding: 2px;">1Fh = Reserved</td></tr> <tr><td style="padding: 2px;">.....</td></tr> <tr><td style="padding: 2px;">20h:1024MB (Not supported for CHV, BSW)</td></tr> </table>				0h = 0MB	1h = 32MB	2h = 64MB	3h = 96MB	4h = 128MB	5h = 160MB	6h = 192MB	7h = 224MB	8h = 256MB	9h = 288MB	Ah = 320MB	Bh = 352MB	Ch = 384MB	Dh = 416MB	Eh = 448MB	Fh = 480MB	10h = 512MB	11h = 8MB	12h = 12MB	13h = 16MB	14h = 20MB	15h = 24MB	16h = 28MB	17h = 36MB	18h = 40MB	19h = 44MB	1Ah = 48MB	1Bh = 52MB	1Ch = 56MB	1Dh = 60MB	1Eh = Reserved	1Fh = Reserved	20h:1024MB (Not supported for CHV, BSW)
0h = 0MB																																					
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MGGC - MGGC

		<p>..... 30h:1536MB (Not supported for CHV, BSW) 40h:2048MB (Not supported for CHV, BSW) 80h:4096MB (Not supported for CHV, BSW) 81h - FF:Reserved Other = Reserved When GMS != '0 (and VD=0): Address[31:0] is compared with VGA memory range. (The VGA memory range is A_0000h to B_FFFh.). If there is a match and MSE = 1 and MEMRD or MEMWR, the access will route as a Rmdwvgamemen_cr cycle on the RMBus. If the RMBus returns a hit the GVD will select the command. As well, when 0 the GVD will check if scldown3_address[15:0] is one of the VGA IO register range. (The VGA IO range is 03B0h - 03BBh and 03C0h - 03DFh.) If there is a match and IOSE = 1 and the SCL command is either an IORD or IOWR, the GVD will initiate a (VGA) register cycle on the RMBus. If the RMBus returns a hit the GVD will select the command When GMS == '0 : No address compare will occur against VGA memory range or the VGA IO register range. Also, CC[15:8] is changed to 8'h80 from 8'h00</p>					
	2	<p>RESERVED</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved</p>		Default Value:	0b	Access:	RO
Default Value:	0b						
Access:	RO						
	1	<p>VGA_DISABLE</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>VGA Disable (VD): 0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub- Class Code field within Device 2 function 0 Class Code register is 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field pre-allocates no memory. This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override (CAPID0[38] = 1) or via a register (DEVEN[3] = 0).</p>		Default Value:	0b	Access:	RO
Default Value:	0b						
Access:	RO						
	0	<p>GGCLCK</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>When set to 1b, this will lock all the bits in this register, including itself</p>		Default Value:	0b	Access:	RO
Default Value:	0b						
Access:	RO						

MGSR2GAM Message Register

MGSR2GAM_MSGREG - MGSR2GAM Message Register			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	040D8h		
DWord	Bit	Description	
0	31:16	Mask Bits	
		Default Value:	0000h
		Access:	RO
		Mask Bits act as Write Enables for the bits[15:0] of this register.	
		MGSR2GAM Message Register 15	
		Default Value:	0b
Access:	R/W		
		For Future Use. This bit is self clear.	
14		MGSR2GAM Message Register 14	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
		MGSR2GAM Message Register 13	
		Default Value:	0b
Access:	R/W		
		For Future Use. This bit is self clear.	
12		MGSR2GAM Message Register 12	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
		MGSR2GAM Message Register 11	
		Default Value:	0b
Access:	R/W		
		For Future Use.	

MGSR2GAM_MSGREG - MGSR2GAM Message Register

		This bit is self clear.	
10	MGSR2GAM Message Register 10		
	Default Value:	0b	
	Access:	R/W	
	For Future Use. This bit is self clear.		
9	MGSR2GAM Message Register 9		
	Default Value:	0b	
	Access:	R/W	
	For Future Use. This bit is self clear.		
8	MGSR2GAM Message Register 8		
	Default Value:	0b	
	Access:	R/W	
	For Future Use. This bit is self clear.		
7	MGSR2GAM Message Register 7		
	Default Value:	0b	
	Access:	R/W	
	For Future Use. This bit is self clear.		
6	MGSR2GAM Message Register 6		
	Default Value:	0b	
	Access:	R/W	
	For Future Use. This bit is self clear.		
5	MGSR2GAM Message Register 5		
	Default Value:	0b	
	Access:	R/W	
	For Future Use. This bit is self clear.		
4	MGSR2GAM Message Register 4		
	Default Value:	0b	
	Access:	R/W	
	For Future Use. This bit is self clear.		
3	MGSR2GAM Message Register 3		
	Default Value:	0b	
	Access:	R/W	
	For Future Use. This bit is self clear.		

MGSR2GAM_MSGREG - MGSR2GAM Message Register		
	2	MGSR2GAM Message Register 2
		Default Value: 0b
		Access: R/W
	For Future Use. This bit is self clear.	
	1	MGSR2GAM Message Register 1
		Default Value: 0b
		Access: R/W
	For Future Use. This bit is self clear.	
	0	MGSR2GAM Message Register 0
Default Value: 0b		
Access: R/W		
Bit0 - Tail Update Ack Message. This bit is self clear.		

Misc. Clocking / Reset Control Registers

MISCCPCTL - Misc. Clocking / Reset Control Registers			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000002		
Size (in bits):	32		
Address:	09424h		
Miscellaneous Clocking / Reset Control Registers.			
DWord	Bit	Description	
0	31:8	Bonus ECO bits	
		Access: <table border="1" style="width: 100%;"><tr><td style="width: 80%;"></td><td style="width: 20%; text-align: center;">R/W</td></tr></table> Bonus ECO bits	
		R/W	
	7	DOP clock gating enable for VEbox clks	
		Access: <table border="1" style="width: 100%;"><tr><td style="width: 80%;"></td><td style="width: 20%; text-align: center;">R/W</td></tr></table> Controls the Enabling of the DOP-level Vebox (cvclk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled	
		R/W	
6	DOP clock gating enable for Media clocks		
	Access: <table border="1" style="width: 100%;"><tr><td style="width: 80%;"></td><td style="width: 20%; text-align: center;">R/W</td></tr></table> Controls the Enabling of the DOP-level Media (cmclk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled		R/W
	R/W		
5	Reserved		
	Access: <table border="1" style="width: 100%;"><tr><td style="width: 80%;"></td><td style="width: 20%; text-align: center;">RO</td></tr></table> Made Reserved field as we dont have Media 1 in CHV, BSW Controls the Enabling of the DOP-level Render (cmclk for 2nd media block) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled		RO
	RO		
4	Reserved		
3	DOP Clock gating Enable for Widi clocks		
	Access: <table border="1" style="width: 100%;"><tr><td style="width: 80%;"></td><td style="width: 20%; text-align: center;">R/W</td></tr></table> Controls the Enabling of the DOP-level Render (cwclk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled		R/W
	R/W		

MISCCPCTL - Misc. Clocking / Reset Control Registers

2	DOP clock gating Enable for Fix clocks (cfclk)	
	Access:	R/W
	Controls the Enabling of the DOP-level Render (cfclk/cf2xclk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled	
1	L1 Clock Ungate Enabling Control During Reset	
	Default Value:	1b
	Access:	R/W
Control to enable/disable L1 clock gating during soft resets and FLR reset processing 1 - disable L1 clock gating during soft resets and FLR 0 - enable L1 clock gating during soft resets and FLR (default op)		
0	DOP Clock Gating Enable for Render Clocks	
	Access:	R/W
Controls the Enabling of the DOP-level Render (crclk/cr2xclk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled		

MISC. CTX control register

MISCCTXCTL - MISC. CTX control register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0942Ch	
DWord	Bit	Description
0	31:1	Reserved
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Reserved.
Access:	RO	
0	0	Context Restore ACk indication from Csunit
		<table border="1"> <tr> <td>Access:</td> <td>R/W Set</td> </tr> </table> Context Restore ACk indication from Csunit 1'b1 : Csunit has completed restoring CPunits address space Once set, CPunit hardware clears this bit after sending the ctx save ack done message to CS 1'b0 : Csunit has NOT completed restoring CPunits address space
Access:	R/W Set	

Misc. Reset Control Register

RSTCTL - Misc. Reset Control Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	09420h			
Miscellaneous reset control registers.				
DWord	Bit	Description		
0	31:4	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%; text-align: center;">RO</td> </tr> </table> <p>Reserved</p>	Access:	RO
	Access:	RO		
	3:2	<p>Reset Staggering Period Control</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%; text-align: center;">R/W</td> </tr> </table> <p>Reset assertion staggering period between reset domains during FLR and soft-resets: 00: 24 cs clocks 01: 48 cs clocks 10: 72 cs clocks 11: 96 cs clocks</p>	Access:	R/W
Access:	R/W			
1:0	<p>Reset Residency Control</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%; text-align: center;">R/W</td> </tr> </table> <p>Reset assertion residency period for FLR and soft-resets. 00: 24 cs clocks 01: 48 cs clocks 10: 96 cs clocks 11: 192 cs clocks</p>	Access:	R/W	
Access:	R/W			

Miscellaneous Message Register for Power Management Unit

MSG_MISC - Miscellaneous Message Register for Power Management Unit

Register Space: MMIO: 0/2/0

Project: CHV, BSW

Source: PRM

Default Value: 0x00000000

Size (in bits): 16

Address: 08048h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].

In order to set bit0, for example, the data would be 0x0001_0001.;In order to clear bit0, for example, the data would be 0x0001_0000.

Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	15:3	Reserved Access: RO
	2	Reserved
	1	Internal RFO Enable Ack (forwarded from MDRB to RPM to gpm) Access: R/W From RPM on behalf of MGSR: Internal RFO Enable Acknowledgement b0 : RFO Disable Ack (default) b1 : RFO Enable Ack
	0	GO Acknowledgement from OAunit Access: R/W Go Acknowledgement b0 : Go=0 Ack <default> b1 : Go=1 Ack Normally the requirement is that when Go=0 request is sent, the agent has to indicate busy before sending the Go=0 acknowledgement. It can only go idle again once Go=1 is received. For OA, however, it does not have an idle indication to PM and thus do not have to do this.

MISRO

MISRO - MISRO						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	182040h					
Spare0 registers. Note: Changed for CHV, BSW.						
DWord	Bit	Description				
0	31:17	Spare0				
		Default Value:	0000h			
		Access:	R/W			
Spare bits in case an ECO is needed.						
16		Standby Threshold Periodic Enable				
		Default Value:	0000h			
		Access:	R/W			
Standby Threshold Periodic Enable						
15:0		Standby Threshold				
		Default Value:	0000h			
		Access:	R/W			
		<table border="1"> <thead> <tr> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>Standby Threshold For 33MHz cz freq (200MHz, 267MHz, 320MHz, 333MHz, 400MHz, 467MHz, 533MHz) 0 = 0 us 1 = 15.36 us 2 = 30.72 us 3 = 46.08 us FFFF ~= 1s For non-33MHz cz freq (350MHz, 356MHz, 360MHz, 373MHz), standby threshold will be in increments of (15.36us + (1-7)%)</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Description	Project	Standby Threshold For 33MHz cz freq (200MHz, 267MHz, 320MHz, 333MHz, 400MHz, 467MHz, 533MHz) 0 = 0 us 1 = 15.36 us 2 = 30.72 us 3 = 46.08 us FFFF ~= 1s For non-33MHz cz freq (350MHz, 356MHz, 360MHz, 373MHz), standby threshold will be in increments of (15.36us + (1-7)%)	CHV, BSW
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MISR1

MISR1 - MISR1						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	182044h					
Spare1 registers. Note: Changed for CHV, BSW.						
DWord	Bit	Description				
0	31:0	Spare1 <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Spare bits in case an ECO is needed.	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

MISR2

MISR2 - MISR2						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	182048h					
Spare2 registers. Note: Changed for CHV, BSW.						
DWord	Bit	Description				
0	31:0	Spare2 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Spare bits in case an ECO is needed.	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

MISR3

MISR3 - MISR3						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	18204Ch					
Spare3 registers. Note: Changed for CHV, BSW.						
DWord	Bit	Description				
0	31:0	Spare3 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Spare bits in case an ECO is needed.	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

MISR4

MISR4 - MISR4						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	182050h					
Spare4 registers. Note: Changed for CHV, BSW.						
DWord	Bit	Description				
0	31:0	<p>Spare4</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Spare bits in case an ECO is needed.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

MMIO_INDEX

MMIO_INDEX - MMIO_INDEX						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	00000h					
<p>Contains address and target. Punit cannot access IO space from message channel. A 32 bit IO write to this port loads the offset of the MMIO register or offset into the GTT that needs to be accessed. An IO Read returns the current value of this register. An 8/16 bit IO write to this register is completed but does not update this register. This mechanism to access internal graphics MMIO registers must not be used to access VGA IO registers which are mapped through the MMIO space. VGA registers must be accessed directly through the dedicated VGA IO ports. This is used by SBIOS. It is not used by graphics driver. This register is only accessible through the IOSF Primary bus. The base register is defined by IOBAR.</p>						
DWord	Bit	Description				
0	31:2	Register_offset <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This field selects GTT entry or any one of the Dword registers within the MMIO register space of this device.</p>	Default Value:	00000000h	Access:	R/W
		Default Value:	00000000h			
Access:	R/W					
1:0	Target	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>00 = MMIO Registers, 01 = GTT, 1X =Reserved</p>	Default Value:	00b	Access:	R/W
		Default Value:	00b			
		Access:	R/W			

Mode Register for GAB

GAB_MODE - Mode Register for GAB						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	BlitterCS					
Default Value:	0x00000000					
Access:	r/w					
Size (in bits):	32					
Address:	220A0h-220A3h					
The GAB_MODE register contains information that controls configurations in the GAB.						
DWord	Bit	Description				
0	31:16	Mask <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">WO</td> </tr> <tr> <td>Format:</td> <td>Mask</td> </tr> </table>	Access:	WO	Format:	Mask
	Access:	WO				
	Format:	Mask				
	15:6	Reserved Read/Write				
5:3	BLB Arbitration Priority <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U3</td> </tr> </table>	Format:	U3			
Format:	U3					
2:0	BCS Arbitration Priority <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U3</td> </tr> </table>	Format:	U3			
Format:	U3					

Mode Register for GAC

GAC_MODE - Mode Register for GAC		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000 CHV, BSW	
Access:	r/w	
Size (in bits):	32	
Address:	120A0h-120A3h	
ShortName:	GAC_MODE	
Valid Projects:	CHV, BSW	
The GAC_MODE register contains information that controls configurations in the GAC.		
DWord	Bit	Description
0	31:16	Mask
		Access: WO
		Format: Mask
	15:1	Reserved
		Access: r/w
	0	Reserved
Project: CHV, BSW		
Access: r/w		

Mode Register for GAFS

GAFS_MODE - Mode Register for GAFS			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	RenderCS		
Default Value:	0x00000000		
Access:	r/w		
Size (in bits):	32		
Trusted Type:	1		
Address:	0212Ch		
DWord	Bit	Description	
0	31:16	Mask Bits	
		Access: WO	
		Format: Mask	
			Masks: These bits serve as write enables for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.
	15:11	Reserved	
		Format: MBZ	
	10	Reserved	
Project: CHV, BSW			
Format: MBZ			
9	Reserved		
8:2	Reserved		
	Format: MBZ		
1:0	Reserved		
	Project: CHV, BSW		
	Format: MBZ		

MSAC

MSAC - MSAC			
Register Space:	PCI: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00010000		
Size (in bits):	32		
Address:	00060h		
<p>This register determines the size of the graphics memory aperture. Only the system BIOS will write this register based on pre-boot address allocation efforts. Graphics may read this register to determine the correct aperture size. System BIOS needs to save this value on boot so that it can reset it correctly during S3 resume. The size of the aperture must not be modified by software after its location is written into GMADR (offset 18h).</p>			
DWord	Bit	Description	
0	31:21	RESERVED	
		Default Value:	000h
		Access:	RO
		Reserved	
	20	APSZ_4	
		Default Value:	0b
		Access:	R/W
		<p>This field is used to determine the size of Aperture (GMADR) and controls affects certain bits of GMADR register.</p> <p>00000 = 128MB =>GMADR.B [26:4] is hardwired to 0 00001 = 256MB =>GMADR.B[27] = 0, RO 00010 = illegal (hardware will treat this as 00011) 00011 = 512MB =>GMADR.B[28:27] = 0, RO 00100-00110 = illegal (hardware will treat this as 00111) 00111 = 1024MB =>GMADR.B[29:27] = 0, RO 01000-01110= illegal (hardware will treat this as 01111) 01111= 2048MB=> GMADR.B[30:27] = 0, RO 10000-11110 = illegal (hardware will treat this as 11111) 11111= 4096MB => GMADR.B[31:27] = 0, RO</p>	
	19	APSZ_3	
		Default Value:	0b
		Access:	R/W
		<p>This field is used to determine the size of Aperture (GMADR) and controls affects certain bits of GMADR register.</p> <p>00000 = 128MB =>GMADR.B [26:4] is hardwired to 0 00001 = 256MB =>GMADR.B[27] = 0, RO 00010 = illegal (hardware will treat this as 00011)</p>	

MSAC - MSAC

		<p>00011 = 512MB =>GMADR.B[28:27] = 0, RO 00100-00110 = illegal (hardware will treat this as 00111) 00111 = 1024MB =>GMADR.B[29:27] = 0, RO 01000-01110= illegal (hardware will treat this as 01111) 01111= 2048MB=> GMADR.B[30:27] = 0, RO 10000-11110 = illegal (hardware will treat this as 11111) 11111= 4096MB => GMADR.B[31:27] = 0, RO</p>					
	18	<p>APSZ_2</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This field is used to determine the size of Aperture (GMADR) and controls affects certain bits of GMADR register. 00000 = 128MB =>GMADR.B [26:4] is hardwired to 0 00001 = 256MB =>GMADR.B[27] = 0, RO 00010 = illegal (hardware will treat this as 00011) 00011 = 512MB =>GMADR.B[28:27] = 0, RO 00100-00110 = illegal (hardware will treat this as 00111) 00111 = 1024MB =>GMADR.B[29:27] = 0, RO 01000-01110= illegal (hardware will treat this as 01111) 01111= 2048MB=> GMADR.B[30:27] = 0, RO 10000-11110 = illegal (hardware will treat this as 11111) 11111= 4096MB => GMADR.B[31:27] = 0, RO</p>		Default Value:	0b	Access:	R/W
Default Value:	0b						
Access:	R/W						
	17	<p>APSZ_1</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This field is used to determine the size of Aperture (GMADR) and controls affects certain bits of GMADR register. 00000 = 128MB =>GMADR.B [26:4] is hardwired to 0 00001 = 256MB =>GMADR.B[27] = 0, RO 00010 = illegal (hardware will treat this as 00011) 00011 = 512MB =>GMADR.B[28:27] = 0, RO 00100-00110 = illegal (hardware will treat this as 00111) 00111 = 1024MB =>GMADR.B[29:27] = 0, RO 01000-01110= illegal (hardware will treat this as 01111) 01111= 2048MB=> GMADR.B[30:27] = 0, RO 10000-11110 = illegal (hardware will treat this as 11111) 11111= 4096MB => GMADR.B[31:27] = 0, RO</p>		Default Value:	0b	Access:	R/W
Default Value:	0b						
Access:	R/W						
	16	<p>APSZ_0</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>		Default Value:	1b	Access:	R/W
Default Value:	1b						
Access:	R/W						

MSAC - MSAC					
	<p>This field is used to determine the size of Aperture (GMADR) and controls affects certain bits of GMADR register.</p> <p>00000 = 128MB =>GMADR.B [26:4] is hardwired to 0</p> <p>00001 = 256MB =>GMADR.B[27] = 0, RO</p> <p>00010 = illegal (hardware will treat this as 00011)</p> <p>00011 = 512MB =>GMADR.B[28:27] = 0, RO</p> <p>00100-00110 = illegal (hardware will treat this as 00111)</p> <p>00111 = 1024MB =>GMADR.B[29:27] = 0, RO</p> <p>01000-01110= illegal (hardware will treat this as 01111)</p> <p>01111= 2048MB=> GMADR.B[30:27] = 0, RO</p> <p>10000-11110 = illegal (hardware will treat this as 11111)</p> <p>11111= 4096MB => GMADR.B[31:27] = 0, RO</p>				
15:0	<p>RESERVED</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">0000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">RO</td> </tr> </table> <p>Reserved</p>	Default Value:	0000h	Access:	RO
Default Value:	0000h				
Access:	RO				

MSI_CAPID_MC

MSI_CAPID_MC - MSI_CAPID_MC			
Register Space:	PCI: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x0000B005		
Size (in bits):	32		
Address:	00090h		
90-91h: Message Signaled Interrupts Capability ID			
92-93h: Message Signaled Control Register			
DWord	Bit	Description	
0	31:24	RESERVED	
		Default Value:	00h
		Access:	RO
		Reserved	
23		MODE_64B_ADDRCAP	
		Default Value:	0b
		Access:	RO
		C64: 32-bit capable only	
22:20		MULTIPLE_MESSAGE_ENABLE	
		Default Value:	000b
		Access:	R/W
		MME: This field is RW for software compatibility, but only a single message is ever generated. System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested. The encoding is the same as for the MMC field below.	
19:17		MULTIPLE_MESSAGE_CAPABLE	
		Default Value:	000b
		Access:	RO
		MMC: This device is only single message capable. System Software reads this field to determine the number of messages being requested by this device. Value: Number of requests 000: 1 001-111: Reserved	

MSI_CAPID_MC - MSI_CAPID_MC					
16	<p>MSI_ENABLE</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>MSIE: If set, MSI is enabled and traditional interrupts are not used to generate interrupts. PCICMDSTS.BME must be set for an MSI to be generated. 0 : MSI interrupts are disabled. 1 : MSI interrupts are enabled. Permits sending an MSI interrupt.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
15:8	<p>POINTER_TO_NEXT_CAPABILITY</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Default Value:</td> <td>B0h</td> </tr> <tr> <td>Access:</td> <td>R/W Once</td> </tr> </table> <p>Points to the next item in the list(B0=VCID support). This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.</p>	Default Value:	B0h	Access:	R/W Once
Default Value:	B0h				
Access:	R/W Once				
7:0	<p>CAPABILITY_ID</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>05h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>CAPID: Indicates an MSI capability</p>	Default Value:	05h	Access:	RO
Default Value:	05h				
Access:	RO				

MTRR Capability Register 0

MTRR_CR_0 - MTRR Capability Register 0			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x0000050A		
Size (in bits):	32		
Address:	0F100h		
Register to define MTRR - range register capabilities.			
DWord	Bit	Description	
0	31:11	Reserved	
		Default Value:	00000000000000000000b
		Access:	RO
	10	Write Combining Support	
		Default Value:	1b
		Access:	RO
	0: Write Combining (WC) memory type is not supported. 1: Write Combining (WC) memory type is supported. GFX Implementation: More details on memory type section however WC support in GFX looks like streamlining non-cacheable accesses. This is the existing UC concept used in GFX architecture.		
	9	Reserved	
		Default Value:	0b
		Access:	RO
	8	Fixed Range MTRRs Support	
		Default Value:	1b
		Access:	RO
	0: No Fixed range MTRRs are supported. 1: Fixed Range MTRRs (IA32_MTRR_FIX64K_00000 through IA32_MTRR_FIX4K_0F8000) are supported.		
	7:0	Variable Range MTRR Count	
		Default Value:	0Ah
Access:		RO	
Indicates the number of variable ranges implemented.			

MTRR Capability Register 1

MTRR_CR_1 - MTRR Capability Register 1						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F104h					
Register to define MTRR - range register capabilities						
DWord	Bit	Description				
0	31:0	MTRR Capability Register 1 Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">RO</td> </tr> </table> Bit[63:32]: Reserved.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

MTRR Default Type Register 0

MTRR_DT_0 - MTRR Default Type Register 0			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F108h		
Register to define MTRR - range register capabilities.			
DWord	Bit	Description	
0	31:12	Reserved	
		Default Value:	00000000000000000000b
		Access:	RO
	11	Reserved	
		10	Fixed Range MTRR Enable/Disable
			Default Value:
	Access:		R/W
			0: Disable fixed-range MTRRs. 1: Enable fixed-range MTRRs. When the fixed-range MTRRs are enabled, they take priority over the variable-range MTRRs when overlaps in ranges occur. If the fixed-range MTRRs are disabled, the variable range MTRRs can still be used and can map the range ordinarily covered by the fixed-range MTRRs. GFX Implementation: GFX uses this field as a specific enable/disable for fixed range MTRRs.
	9:8	Reserved	
		Default Value:	00b
		Access:	RO
	7:0	Default Memory Type	
Default Value:		00h	
Access:		R/W	
		Indicates default memory type used for physical memory address ranges that do not have a memory type specified for them by an MTRR. Legal values for this field are 0, 1, 4, 5, and 6. GFX Implementation: GFX uses this field to assign memory regions that are not assigned as part of the fixed and variable range registers.	

MTRR Default Type Register 1

MTRR_DT_1 - MTRR Default Type Register 1						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F10Ch					
Register to define MTRR - range register capabilities.						
DWord	Bit	Description				
0	31:0	<p>MTRR Default Type Register 1 Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Bit[63:32]: Reserved.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

MT Virtual Page Address Registers

MTTLB_VA - MT Virtual Page Address Registers		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	04800h-04803h	
DWord	Bit	Description
0	31:12	Address
		Format: GraphicsAddress[31:12] Page virtual address.
	11:0	Reserved
		Project: CHV, BSW Format: MBZ

NOP Identification Register

NOPID - NOP Identification Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	RenderCS			
Default Value:	0x00000000			
Size (in bits):	32			
Trusted Type:	1			
Address:	02094h			
Address:	12094h-12097h			
Name:	NOP Identification Register			
ShortName:	NOPID_VCSUNIT0			
Address:	1A094h-1A097h			
Name:	NOP Identification Register			
ShortName:	NOPID_VECSUNIT			
Address:	1C094h-1C097h			
Name:	NOP Identification Register			
ShortName:	NOPID_VCSUNIT1			
Address:	22094h-22097h			
Name:	NOP Identification Register			
ShortName:	NOPID_BCSUNIT			
Description		Project		
Access: RW		CHV, BSW		
The NOPID register contains the Noop Identification value specified by the last MI_NOOP instruction that enabled this register to be updated.				
DWord	Bit	Description		
0	31:22	Reserved		
		Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;"></td><td style="width: 100px;">MBZ</td></tr></table>		MBZ
	MBZ			
	21:0	Reserved		

P2GCONTROL

P2GCONTROL - P2GCONTROL		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	1300F0h	
Punit to Gunit Control. Punit will context save/restore this register.		
DWord	Bit	Description
0	31:1	Reserved Access: RO
	0	P2GCONTROL_POLICY Access: R/W 0: Let Gunit do the context save. (Power-On default) 1: Context save will be handled by Punit and driver.

PAGE_FAULT_MODE

PAGE_FAULT_MODE - PAGE_FAULT_MODE							
Register Space:	MMIO: 0/2/0						
Project:	CHV, BSW						
Source:	PRM						
Default Value:	0x00000000						
Size (in bits):	32						
Address:	0E454h						
Name:	PAGE_FAULT_MODE						
ShortName:	PAGE_FAULT_MODE						
Valid Projects:	CHV, BSW						
This is a basic register template							
DWord	Bit	Description					
0	31:8	Reserved					
		Default Value:	0000000000000000b				
		Access:	RO				
	7:6	FAULT_MODE					
		Project:	CHV, BSW				
		Access:	R/W				
		Fault Model: Applicable only in advanced context					
		"00": Fault & Hang. Same mode as gen7.5					
		"01": Fault & Halt					
	"10": Fault & Continue & Switch						
"11": Reserved							
<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>[Default]</td> </tr> <tr> <td>01b</td> <td></td> </tr> </tbody> </table>		Value	Name	00b	[Default]	01b	
Value	Name						
00b	[Default]						
01b							
5:0	Reserved						
	Project:	CHV, BSW					

Page Directory Pointer Descriptor - PDP0/PML4/PASID

PDP0 - Page Directory Pointer Descriptor - PDP0/PML4/PASID	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	02270h-02277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_RCSUNIT
Address:	12270h-12277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VCSUNIT0
Address:	1A270h-1A277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VECSUNIT
Address:	1C270h-1C277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VCSUNIT1
Address:	22270h-22277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_BCSUNIT
<p>PDP0/PML4/PASID: This register can contain three values which depend on the element descriptor definition. PASID[19:0]: Populated in the first 20bits of the register and selected when Advanced Context flag is set in the element descriptor in execlist mode of submission. This is not valid in ring buffer mode of scheduling. PML4[38:12]: Pointer to base address of PML4 and selected when Legacy Context flag is set and 64b address support is selected. PDP0[38:12]: Pointer to one of the four page directory pointer (lowest) and defines the first 0-1GB of memory mapping. This is valid when Legacy Context Flag is set and 64bit virtual addressing is not supported. <i>Note: This is a guest physical address.</i></p>	
Programming Notes	Project
<p><i>Execlist Based Scheduling:</i> SW should update PDP0/12/3 registers in context image with proper values before submitting the context to HW in execlist mode of scheduling. HW restores these registers as part of context restore to set the PPGTT access accordingly. PPGTT is always enabled in advanced context mode of execlist based scheduling and can be disabled only in legacy context mode. Privilege Access Bit in Element Descriptor controls the PPGTT enabling in legacy context mode.</p>	

PDP0 - Page Directory Pointer Descriptor - PDP0/PML4/PASID

Ring Buffer Based Scheduling: A write via MMIO to PDP0_DESCRIPTOR (lower Dword) triggers the Page Directory Restore in HW when PPGTT is enabled. SW should ensure PDP1/2/3 registers are programmed appropriately prior to programming PDP0. PDP0_DESCRIPTOR lower dword should be programmed at the end. Per-Process GTT Enable Bit in GFX_MODE register controls the PPGTT enabling and disabling. Programming Per-Process GTT Enable Bit in GFX_MODE register doesn't enable/disable the PPGTT translation of memory access immediately; the change comes in to affect only when the Page Directory registers are programmed. Programming Per-Process GTT Enable Bit in GFX_MODE register bit must be followed by programming Page Directory Registers in order to enable or disable the PPGTT translation of memory access. PDP*_DESCRIPTOR registers must always be programmed through MI_LOAD_REGISTER_IMMEDIATE command in ring buffer with PDP0_DESCRIPTOR lower dword written at the end. PDP0/12/3 registers are context save restored. PDP descriptors are power context save restored in VCS, BCS and VECS engines. PDP descriptors are context save restored per render context in RCS and must be programmed following MI_SET_CONTEXT command, in case of PDP descriptors programmed without context set (MI_SET_CONTEXT) will get lost on C6 entry/exit. PDP descriptor registers should be programmed after ensuring the pipe is completely flushed and TLB's invalidated.

CHV,
BSW

DWord	Bit	Description						
0	63	<p>PD Load Busy</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>Valid</td> </tr> </table> <p>This read-only field gets set when PDP0 is written to indicating Page Directory Restore activity is in progress and will get reset once the activity is completed.</p>	Project:	CHV, BSW	Access:	RO	Format:	Valid
Project:	CHV, BSW							
Access:	RO							
Format:	Valid							
	62:0	<p>PDP0 Descriptor</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> </table>	Project:	CHV, BSW				
Project:	CHV, BSW							

Page Directory Pointer Descriptor - PDP1

PDP1 - Page Directory Pointer Descriptor - PDP1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Address:	02278h-0227Fh	
Name:	Page Directory Pointer Descriptor - PDP1	
ShortName:	PDP1_RCSUNIT	
Address:	12278h-1227Fh	
Name:	Page Directory Pointer Descriptor - PDP1	
ShortName:	PDP1_VCSUNIT0	
Address:	1A278h-1A27Fh	
Name:	Page Directory Pointer Descriptor - PDP1	
ShortName:	PDP1_VECSUNIT	
Address:	1C278h-1C27Fh	
Name:	Page Directory Pointer Descriptor - PDP1	
ShortName:	PDP1_VCSUNIT1	
Address:	22278h-2227Fh	
Name:	Page Directory Pointer Descriptor - PDP1	
ShortName:	PDP1_BCSUNIT	
<p>PDP1[38:12]: Pointer to one of the four page directory pointer (lowest+1) and defines the first 1-2GB of memory mapping. This is valid when Legacy Context Flag is set and 64bit virtual addressing is not supported. <i>Note: This is a guest physical address.</i></p>		
DWord	Bit	Description
0	63:0	PDP1 Descriptor

Page Directory Pointer Descriptor - PDP2

PDP2 - Page Directory Pointer Descriptor - PDP2		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Address:	02280h-02287h	
Name:	Page Directory Pointer Descriptor - PDP2	
ShortName:	PDP2_RCSUNIT	
Address:	12280h-12287h	
Name:	Page Directory Pointer Descriptor - PDP2	
ShortName:	PDP2_VCSUNIT0	
Address:	1A280h-1A287h	
Name:	Page Directory Pointer Descriptor - PDP2	
ShortName:	PDP2_VECSUNIT	
Address:	1C280h-1C287h	
Name:	Page Directory Pointer Descriptor - PDP2	
ShortName:	PDP2_VCSUNIT1	
Address:	22280h-22287h	
Name:	Page Directory Pointer Descriptor - PDP2	
ShortName:	PDP2_BCSUNIT	
<p>PDP2[38:12]: Pointer to one of the four page directory pointer (lowest+2) and defines the first 2-3GB of memory mapping. This is valid when Legacy Context Flag is set and 64bit virtual addressing is not supported. <i>Note: This is a guest physical address.</i></p>		
DWord	Bit	Description
0	63:0	PDP2 Descriptor

Page Directory Pointer Descriptor - PDP3

PDP3 - Page Directory Pointer Descriptor - PDP3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Address:	02288h-0228Fh	
Name:	Page Directory Pointer Descriptor - PDP3	
ShortName:	PDP3_RCSUNIT	
Address:	12288h-1228Fh	
Name:	Page Directory Pointer Descriptor - PDP3	
ShortName:	PDP3_VCSUNIT0	
Address:	1A288h-1A28Fh	
Name:	Page Directory Pointer Descriptor - PDP3	
ShortName:	PDP3_VECSUNIT	
Address:	1C288h-1C28Fh	
Name:	Page Directory Pointer Descriptor - PDP3	
ShortName:	PDP3_VCSUNIT1	
Address:	22288h-2228Fh	
Name:	Page Directory Pointer Descriptor - PDP3	
ShortName:	PDP3_BCSUNIT	
<p>PDP3[38:12]: Pointer to one of the four page directory pointer (lowest+3) and defines the first 3-4GB of memory mapping. This is valid when Legacy Context Flag is set and 64bit virtual addressing is not supported. <i>Note: This is a guest physical address.</i></p>		
DWord	Bit	Description
0	63:0	PDP3 Descriptor

Page Request Queue Address Register 0

PAGEREQ_QADDR_0 - Page Request Queue Address Register 0			
Register Space:	MMIO: 0/2/0		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F0D0h		
Register to configure the base address and size of the page request queue.			
DWord	Bit	Description	
0	31:12	Page Request Queue Base Register	
		Default Value:	00000h
		Access:	R/W
This field points to the base of 4KB aligned invalidation request queue. Hardware may ignore and not implement bits 63:HAW, where HAW is the host address width. Reads of this field return the value that was last programmed to it.			
11:3	Reserved	Default Value:	000000000b
		Access:	RO
		This field is reserved.	
2:0	Queue Size	Default Value:	000b
		Access:	R/W
		This field specifies the size of the page request queue. A value of X in this field indicates a page request queue of (2X) 4KB pages. The number of entries in the invalidation queue is 2(X+8).	

Page Request Queue Address Register 1

PAGEREQ_QADDR_1 - Page Request Queue Address Register 1						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F0D4h					
Register to configure the base address and size of the page request queue.						
DWord	Bit	Description				
0	31:0	<p>Page Request Queue Base Register</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This field points to the base of 4KB aligned invalidation request queue. Hardware may ignore and not implement bits 63:HAW, where HAW is the host address width. Reads of this field return the value that was last programmed to it.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

Page Request Queue Head Register 0

PAGEREQ_QHEAD_0 - Page Request Queue Head Register 0			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F0C0h		
Register indicating the page request queue head.			
DWord	Bit	Description	
0	31:19	Reserved	
		Default Value:	0000000000000b
		Access:	RO
	18:4	Queue Head	
		Default Value:	000000000000000b
		Access:	R/W
		Specifies the offset (128-bit aligned) to the page request queue for the command that is processed next by software. GFX implementation: GFX has to read the content of the Head pointer as tail pointer gets close to it to prevent overflows in page request queue.	
3:0	Reserved		
	Default Value:	0h	
	Access:	RO	

Page Request Queue Head Register 1

PAGEREQ_QHEAD_1 - Page Request Queue Head Register 1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F0C4h	
Register indicating the page request queue head.		
DWord	Bit	Description
0	31:0	Page Request Queue Head Register 1 Reserved Default Value: 00000000h Access: RO Bit[63:32]: Reserved.

Page Request Queue Tail Register 0

PAGEREQ_QTAIL_0 - Page Request Queue Tail Register 0				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0F0C8h			
Register indicating the page request queue tail.				
DWord	Bit	Description		
0	31:1	Queue Tail		
		<table border="1"> <tr> <td>Default Value:</td> <td>00000000000000000000000000000000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit[31:19]: Reserved. Bit[18:4]: Specifies the offset (128-bit aligned) to the page request queue for the request that is written next by hardware. GFX Implementation: GT manages the tail pointer value as part of page requests. The value can be acquired as part of the RC6 exit. Bit[3:1]: Reserved.</p>	Default Value:	00000000000000000000000000000000b
Default Value:	00000000000000000000000000000000b			
Access:	R/W			
0	0	Valid Bit		
		<table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This bit can only be cleared by SW, which also clears the other fields.</p>	Default Value:	0b
Default Value:	0b			
Access:	R/W			

Page Request Queue Tail Register 1

PAGEREQ_QTAIL_1 - Page Request Queue Tail Register 1						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F0CCh					
Register indicating the page request queue tail.						
DWord	Bit	Description				
0	31:0	Page Request Queue Tail Register 1 Reserved <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Bit[63:32]: Reserved.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

PAK_Stream-Out Report (Errors)

PAK_ERR - PAK_Stream-Out Report (Errors)				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoCS			
Default Value:	0x00000000			
Access:	RO			
Size (in bits):	32			
Trusted Type:	1			
Address:	128E8h			
Valid Projects:	CHV, BSW			
DWord	Bit	Description		
0	31:22	Reserved <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
	21	Incorrect IntraMBFlag in I-slice(AVCf)		
	20	Out of Range Symbol Code(AVC/mpeg2)		
	19	Incorrect MBType(AVC/mpeg2)		
	18	Motion Vectors are not inside the frame boundary(mpeg2)		
	17	Scale code is zero(mpeg2)		
	16	Incorrect DCTtype for given motionType(mpeg2)		
	15:8	MB Y-position This field indicates Macro Block(MB) Y- position where an error occured while encoding.		
7:0	MB X-position This field indicates Macro Block(MB) X- position where an error occured while encoding.			

PAK_Stream-Out Report (Warnings)

PAK_WARN - PAK_Stream-Out Report (Warnings)			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	VideoCS		
Default Value:	0x00000000		
Access:	RO		
Size (in bits):	32		
Trusted Type:	1		
Address:	128E4h		
Valid Projects:	CHV, BSW		
DWord	Bit	Description	
0	31:22	Reserved	
		Project:	All
		Format:	MBZ
	21	Skip Run > 8192 (AVC)	
	20	Incorrect SkipMB (AVC and mpeg2)	
	19	Incorrect MV difference for dual-prime MB (mpeg2)	
	18	End of Slice signal missing on last MB of a Row(mpeg2)	
	17	Incorrect DCT type for field picture	
	16	MVs are not within defined range by fcode	
	15:8	MB Y-position	
7:0	MB X-position		

PAK Report Running Status

PAK_REPORT_STAT - PAK Report Running Status			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	VideoCS		
Default Value:	0x00000000		
Access:	RO		
Size (in bits):	32		
Trusted Type:	1		
Address:	128ECh		
Valid Projects:	CHV, BSW		
DWord	Bit	Description	
0	31:1	Reserved	
	0	PAK Status	
		Value	Name
0		PAK engine is IDLE	
1		PAK engine is currently generating bit stream.	

PAT Index

PAT_INDEX - PAT Index		
Register Space:	MMIO: 0/2/0	
Source:	PRM	
Default Value:	0x00000003	
Access:	R/W	
Size (in bits):	32	
DWord	Bit	Description
0	31:10	Reserved Default Value: 000000000000000000000000b
	9:8	Class of Service Default Value: 00b This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the PRM 00: Class0 01: Class1 10: Class2 11: Class3
	7:6	Reserved Default Value: 00b
	5:4	LRU AGE Default Value: 00b 00: Take the age value from Uncore CRs 01: Assign the age of "0" 10: Do not change the age on a hit 11: Assign the age of "3"
	3:2	Target Cache Default Value: 00b 00: eLLC only 01: LLC only 10: LLC/eLLC allowed 11: LLC/eLLC allowed
	1:0	Mem Type Default Value: 11b 00: Uncacheable(UC) 01: Write Combining(WC) 10: Write through(WT) 11: Write back(WB)

PAT Index High

PAT_INDEX_H - PAT Index High						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x03030303					
Size (in bits):	32					
Address:	040E4h					
DWord	Bit	Description				
0	31:0	<p>PAT Index High</p> <table border="1"> <tr> <td>Default Value:</td> <td>03030303h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Description</p> <p>Bit[31:24]: PAT Index#7: Index#7 definition for page tables. (See bit[7:0] for definition.)</p> <p>Bit[23:16]: PAT Index#6: Index#6 definition for page tables. (See bit[7:0] for definition.)</p> <p>Bit[15:8]: PAT Index#5: Index#5 definition for page tables. (See bit[7:0] for definition.)</p> <p>Bit[7:0]: PAT Index#4: Index#4 definition for page tables.</p> <p>Bit[7]: Reserved.</p> <p>Bit[6]: Snoop Required [CHV, BSW Only] 1: System agent will snoop the IA cores 0: System agent will not snoop the IA cores</p> <p>Bit[5:4]: (See below.) 00b: Age is 0. 01b: Age is 1. 10b: Age is 2. 11b: Age is 3.</p> <p>Bit[3:2]: (See below.) 00b: eLLC only. 01b: LLC only. 10b: LLC and eLLC allowed. 11b: L3, LLC, and eLLC are allowed.</p> <p>Bit[1:0]: (see below): 00b: Uncacheable (UC). 01b: Write Combining (WC). 10b: Write Through (WT). 11b: Write Back (WB).</p>	Default Value:	03030303h	Access:	R/W
Default Value:	03030303h					
Access:	R/W					

PAT Index Low

PAT_INDEX_L - PAT Index Low						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x03030303					
Size (in bits):	32					
Address:	040E0h					
DWord	Bit	Description				
0	31:0	<p>PAT Index Low</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: right;">03030303h</td> </tr> <tr> <td>Access:</td> <td style="text-align: right;">R/W</td> </tr> </table> <p style="text-align: center;">Description</p> <p>Bit[31:24]: PAT Index#3: Index#3 definition for page tables. (See bit[7:0] for definition.)</p> <p>Bit[23:16]: PAT Index#2: Index#2 definition for page tables. (See bit[7:0] for definition.)</p> <p>Bit[15:8]: PAT Index#1: Index#1 definition for page tables. (See bit[7:0] for definition.)</p> <p>Bit[7:0]: PAT Index#0: Index#0 definition for page tables.</p> <p>Bit[7]: Reserved.</p> <p>Bit[6]: Snoop Required [CHV, BSW Only] 1: System agent will snoop the IA cores 0: System agent will not snoop the IA cores</p> <p>Bit[5:4]: (See below.) 00b: Age is 0. 01b: Age is 1. 10b: Age is 2. 11b: Age is 3.</p> <p>Bit[3:2]: (See below.) 00b: eLLC only. 01b: LLC only. 10b: LLC and eLLC allowed. 11b: L3, LLC, and eLLC are allowed.</p> <p>Bit[1:0]: (see below): 00b: Uncacheable (UC). 01b: Write Combining (WC). 10b: Write Through (WT). 11b: Write Back (WB).</p>	Default Value:	03030303h	Access:	R/W
Default Value:	03030303h					
Access:	R/W					

PCBR

PCBR - PCBR			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	182120h		
<p>This provides a base address for context save/restore of GT and Media power context to DRAM. Gunit adds the GAM provided offsets to this base register for power context reads and writes. GTLC stores Power Context in DRAM. The BIOS is expected to program this register and ensure proper allocation within Gfx stolen memory.</p>			
<p>Removing bits 63:32 since this will always be below 4GB.</p>			
DWord	Bit	Description	
0	31:12	Power_Context_Address	
		Default Value:	0000000h
		Access:	R/W Lock
4KB aligned address. Locked with bit 0.			
	11:1	Reserved	
		Default Value:	000h
		Access:	RO
Reserved			
0	0	Power_Context_Register_Lock	
		Default Value:	0b
		Access:	R/W Lock
Writing a '1' to this register locks this bit - preventing further updates. The Power Context Address bits are also locked.			

PCICMD_STS

PCICMD_STS - PCICMD_STS			
Register Space:	PCI: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00100000		
Size (in bits):	32		
Address:	00004h		
04h: PCI Command Register. 06h: PCI Status Register			
DWord	Bit	Description	
0	31:21	RESERVED	
		Default Value:	000h
		Access:	RO
	20	CAPABILITY_LIST	
		Default Value:	1b
		Access:	RO
CAP: Indicates that the CAPPOINT register at 34h provides an offset into PCI Configuration Space containing a pointer to the location of the first item in the list			
19	INTERRUPT_STATUS		
	Default Value:	0b	
	Access:	RO	
18:16	RESERVED		
	Default Value:	000b	
	Access:	RO	
15:11	RESERVED		
	Default Value:	00h	
10	INTERRUPT_DISABLE	Default Value:	0b
		Access:	R/W
		ID: 0 : Legacy interrupt message is enabled. ID: 1 : Disables legacy interrupt message generation on IOSF Sideband. Note : The interrupt status is not blocked from being reflected in PCISTS.IS. Note: MSI interrupt generation : (PCISTS.IS and PCICMD.BME and MSI_CAPID.MSIE) changes from 0 to 1. Note: Message bus interrupt assert is sent : (PCISTS.IS and ~PCICMD.ID and ~MSI_CAPID.MSIE) changes from 0 to 1. Note: Message bus interrupt de-assert is sent : (PCISTS.IS and ~PCICMD.ID and ~MSI_CAPID.MSIE) changes from 1 to 0.	

PCICMD_STS - PCICMD_STS					
9:3	<p>RESERVED</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">00h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved</p>	Default Value:	00h	Access:	RO
Default Value:	00h				
Access:	RO				
2	<p>BUS_MASTER_ENABLE</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>BME: (BME and MAE are observed. But context save/restore can occur.) 0 : Blocks the sending of MSI interrupts. 1 : Permits the sending of MSI interrupts</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
1	<p>Reserved</p>				
0	<p>IO_SPACE_ENABLE</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>IOSE: 0 : I/O space is disabled. IORD and IOWr cycles will not be claimed. 1 : I/O space is enabled. VGA_IO and Gfx_IOBAR are checked. If an IORD/IOWR matches (VGA IO address range or GFX_IOBAR), the cycle will be claimed. Care should be taken in setting up GFX_IOBAR that more than 1 match is not made as this will result in unpredictable behavior. VGA_IO : Address[15:0] is checked to determine if it falls in the VGA IO range. (The VGA IO range is 03B0h - 03BBh and 03C0h - 03DFh.) Gfx_IOBAR : Address[15:3] is compared to GFX_IOBAR[15:3].</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				

PCU INTERRUPT ENABLE REGISTER

PCU_INTERRUPT_IER - PCU INTERRUPT ENABLE REGISTER		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	444ECh-444EFh	
<p>This table indicates which events are mapped to each bit of the GT interrupt 1 register. The IER enabled PCU interrupt IIR sticky bits are ORed together to generate PCU interrupt pending bit in the master interrupt control register.</p>		
DWord	Bit	Description
0	31:26	UNUSED0 Access: <input type="text"/> R/W
	25	PCU_MAILBOX_EVT Access: <input type="text"/> R/W PCU Pcode 2 driver mailbox event
	24	PCU_THERMAL_EVT Access: <input type="text"/> R/W PCU thermal event
	23:0	UNUSED1 Access: <input type="text"/> R/W

PCU INTERRUPT IDENTITY REGISTER

PCU_INTERRUPT_IIR - PCU INTERRUPT IDENTITY REGISTER		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	444E8h-444EBh	
<p>This table indicates which events are mapped to each bit of the GT interrupt 1 register. The IER enabled PCU interrupt IIR sticky bits are ORed together to generate PCU interrupt pending bit in the master interrupt control register.</p>		
DWord	Bit	Description
0	31:26	UNUSED0 Access: <input type="text"/> R/W One Clear
	25	PCU_MAILBOX_EVT Access: <input type="text"/> R/W One Clear PCU Pcode 2 driver mailbox event
	24	PCU_THERMAL_EVT Access: <input type="text"/> R/W One Clear PCU thermal event
	23:0	UNUSED1 Access: <input type="text"/> R/W One Clear

PCU INTERRUPT MASK REGISTER

PCU_INTERRUPT_IMR - PCU INTERRUPT MASK REGISTER						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x03000000					
Size (in bits):	32					
Address:	444E4h-444E7h					
<p>This table indicates which events are mapped to each bit of the GT interrupt 1 register. The IER enabled PCU interrupt IIR sticky bits are ORed together to generate PCU interrupt pending bit in the master interrupt control register.</p>						
DWord	Bit	Description				
0	31:26	UNUSED0 Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td>R/W</td></tr></table>		R/W		
		R/W				
	25	PCU_MAILBOX_EVT Default Value: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td>1b</td></tr></table> Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td>R/W</td></tr></table> PCU Pcode 2 driver mailbox event		1b		R/W
			1b			
	R/W					
PCU_THERMAL_EVT Default Value: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td>1b</td></tr></table> Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td>R/W</td></tr></table> PCU thermal event		1b		R/W		
	1b					
	R/W					
23:0	UNUSED1 Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td>R/W</td></tr></table>		R/W			
	R/W					

PCU INTERRUPT STATUS REGISTER

PCU_INTERRUPT_ISR - PCU INTERRUPT STATUS REGISTER				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	444E0h-444E3h			
<p>This table indicates which events are mapped to each bit of the GT interrupt 1 register. The IER enabled PCU interrupt IIR sticky bits are ORed together to generate PCU interrupt pending bit in the master interrupt control register.</p>				
DWord	Bit	Description		
0	31:26	UNUSED0 Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td>RO</td></tr></table>		RO
		RO		
	25	PCU_MAILBOX_EVT Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td>RO</td></tr></table> PCU Pcode 2 driver mailbox event		RO
		RO		
24	PCU_THERMAL_EVT Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td>RO</td></tr></table> PCU thermal event		RO	
	RO			
23:0	UNUSED1 Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td>RO</td></tr></table>		RO	
	RO			

Pending Head Pointer Register

UHPTR - Pending Head Pointer Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02134h-02137h	
Name:	Pending Head Pointer Register	
ShortName:	UHPTR_RCSUNIT	
Address:	12134h-12137h	
Name:	Pending Head Pointer Register	
ShortName:	UHPTR_VCSUNIT0	
Address:	1A134h-1A137h	
Name:	Pending Head Pointer Register	
ShortName:	UHPTR_VECSUNIT	
Address:	1C134h-1C137h	
Name:	Pending Head Pointer Register	
ShortName:	UHPTR_VCSUNIT1	
Address:	22134h-22137h	
Name:	Pending Head Pointer Register	
ShortName:	UHPTR_BCSUNIT	
Programming Notes		
Once SW uses UHPTR to preempt the existing workload, should explicitly program MI_SET_CONTEXT to save the preempted context status before submitting the new workload. In case SW doesn't want to save the state of the preempted context, it should at the minimum program RS_PREEMPT_STATUS to 0x0 so that the register status doesn't interfere with the new workloads.		
Source		
RenderCS		
DWord	Bit	Description
0	31:3	Head Pointer Address
		Format: GraphicsAddress[31:3]
		Description
		This register represents the GFX address offset where execution should continue in the ring buffer following execution of a Preemptable Command. Refer to the Preemption section for the list of preemptable commands supported in ring buffer mode of scheduling.

UHPTR - Pending Head Pointer Register		
2:1	Reserved	
	Format:	MBZ
0	Head Pointer Valid	
	Description	
	This bit is set by the software to request a pre-emption.	
	It is reset by hardware when a Preemptable command is parsed by the command streamer. The hardware uses the head pointer programmed in this register at the time the reset is generated. Refer to the Preemption section for the list of preemptable commands supported in ring buffer mode of scheduling.	
	This bit is treated as set by command streamer only when arbitration is not disabled using MI_ARB_ON_OFF command. Preemption will not occur on MI_ARB_CHEK command when UHPTR is valid if the arbitration is disabled using MI_ARB_ON_OFF command.	
	Value	Name
	Description	
0	InValid	No valid updated head pointer register, resume execution at the current location in the ring buffer
1	Valid	Indicates that there is an updated head pointer programmed in this register

Plink G2H Spare

SPAREG2H - Plink G2H Spare				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A194h-0A197h			
DWord	Bit	Description		
0	31:9	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
8:0	Plink_G2H_Spare <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These are spares for ECO use.</p>	Access:	R/W	
Access:	R/W			

PM_PWR_CLK_STATE

PM_PWR_CLK_STATE - PM_PWR_CLK_STATE									
Register Space:	MMIO: 0/2/0								
Project:	CHV, BSW								
Source:	PRM								
Default Value:	0x00008288								
Size (in bits):	32								
Address:	0A200h								
PM Power Clock State Request									
DWord	Bit	Description							
0	31	Enable <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Power Clock State Enable: 0 : No specific power state set, no message/wait with PMunit 1 : CSunit sends the contents of this register to PMunit each time it is written, Send contents of this register to PMunit, wait for Ack. When CS writes to A200, requesting new set of resources: Actual EUs used = Async_EU if EUmin < Async_EU < EUMax Actual EUs used = EUMax if Async_EU > equal to EUMax Actual EUs used = EUmin if EUmin > equal to Async_EU Actual SSs used = Async_SS if SScountEn=0 Actual SSs used = SScount if SScountEn=1 After new resources are set by GPMunit, GPM replies to CS by writing 0001_0001 to 0x00_300c</p>	Access:	R/W					
		Access:	R/W						
		30:19	RSVD <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved (CSunit implements full 32b storage)</p>	Access:	RO				
		Access:	RO						
18	SCountEn <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <table border="1"> <thead> <tr> <th>Programming Notes</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>Not supported in CHV, BSW. Must be zero (MBZ).</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Access:	R/W	Programming Notes	Project	Not supported in CHV, BSW. Must be zero (MBZ).	CHV, BSW		
	Access:	R/W							
	Programming Notes	Project							
Not supported in CHV, BSW. Must be zero (MBZ).	CHV, BSW								
17:15	SliceCount <table border="1"> <tr> <td>Default Value:</td> <td>001b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <table border="1"> <thead> <tr> <th>Programming Notes</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>Not supported in CHV, BSW. Must be zero (MBZ).</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Default Value:	001b	Access:	R/W	Programming Notes	Project	Not supported in CHV, BSW. Must be zero (MBZ).	CHV, BSW
Default Value:	001b								
Access:	R/W								
Programming Notes	Project								
Not supported in CHV, BSW. Must be zero (MBZ).	CHV, BSW								

PM_PWR_CLK_STATE - PM_PWR_CLK_STATE							
14:13	<p>RSVD</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> </table> <p>Reserved (CSunit implements full 32b storage)</p>	Access:	RO				
Access:	RO						
12	<p>Spare</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>Spare bit for CHV, BSW</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 70%; text-align: center;">Programming Notes</th> <th style="width: 30%; text-align: center;">Project</th> </tr> </thead> <tbody> <tr> <td>Must be zero (MBZ).</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Access:	R/W	Programming Notes	Project	Must be zero (MBZ).	CHV, BSW
Access:	R/W						
Programming Notes	Project						
Must be zero (MBZ).	CHV, BSW						
11	<p>SSCountEn</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>Enable Subslice Count Request 0 = Use async PMunit subslice count request 1 = Use SliceCount from this register</p>	Access:	R/W				
Access:	R/W						
10:8	<p>SScount</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">010b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Number of subslices to power: 001 : 1 subslice 010 : 2 subslices (GT1-based CHV, BSW only)</p>	Default Value:	010b	Access:	R/W		
Default Value:	010b						
Access:	R/W						
7:4	<p>EUmax</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Maximum number of EUs to power (per subslice if multiple subslices enabled). To specify an exact number of subslices, set EUmax equal to EUmin MinEU and MaxEU need to be even and that odd numbers are illegal</p>	Default Value:	1000b	Access:	R/W		
Default Value:	1000b						
Access:	R/W						
3:0	<p>EUmin</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Minimum number of EUs to power (per subslice if multiple subslices enabled): 0010 : 2 EUs 0100 : 4 EUs 0110 : 6 EUs 1000 : 8 EUs MinEU and MaxEU need to be even and that odd numbers are illegal When both subslices are enabled (ie 0x18_2168[11:10] = 2'b00)</p>	Default Value:	1000b	Access:	R/W		
Default Value:	1000b						
Access:	R/W						

PM_PWR_CLK_STATE - PM_PWR_CLK_STATE

Config	Disabled Column	FUSE_GT_EU_DISABLE - 0x18_2168[31:16]	Desired Config	Actual/Driver Config
2x8	none	0x0000	2x8	2x8
2x8	none	0x0000	2x6	2x6
2x8	none	0x0000	2x4	2x4
2x8	none	0x0000	2x2	2x2
2x6	1	0x1111	2x8	NA
2x6	1	0x1111	2x6	2x8
2x6	1	0x1111	2x4	2x6
2x6	1	0x1111	2x2	2x4
2x6	2	0x2222	2x8	NA
2x6	2	0x2222	2x6	2x8
2x6	2	0x2222	2x4	2x6
2x6	2	0x2222	2x2	2x2
2x6	3	0x4444	2x8	NA
2x6	3	0x4444	2x6	2x8
2x6	3	0x4444	2x4	2x4
2x6	3	0x4444	2x2	2x2
2x6	4	0x8888	2x8	NA
2x6	4	0x8888	2x6	2x6
2x6	4	0x8888	2x4	2x4
2x6	4	0x8888	2x2	2x2
2x5	1+EU3	0x1919	2x8	NA
2x5	1+EU3	0x1919	2x5	2x8
2x5	1+EU3	0x1919	2x4	2x6
2x5	1+EU3	0x1919	2x2	2x4
2x5	2+EU3	0x2A2A	2x8	NA
2x5	2+EU3	0x2A2A	2x5	2x8
2x5	2+EU3	0x2A2A	2x4	2x6
2x5	2+EU3	0x2A2A	2x2	2x2

PM_PWR_CLK_STATE - PM_PWR_CLK_STATE

	2x5	3+EU3	0x4C4C	2x8	NA
	2x5	3+EU3	0x4C4C	2x5	2x8
	2x5	3+EU3	0x4C4C	2x4	2x4
	2x5	3+EU3	0x4C4C	2x2	2x2
	2x5	4+EU2	0x8C8C	2x8	NA
	2x5	4+EU2	0x8C8C	2x5	2x6
	2x5	4+EU2	0x8C8C	2x4	2x4
	2x5	4+EU2	0x8C8C	2x2	2x2

PMCAPID

PMCAPID - PMCAPID		
Register Space:	PCI: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00229001	
Size (in bits):	32	
Address:	000D0h	
PCI Address: D0-D1h Description : Power Management Capabilities ID		
PCI Address: D2-D3h Description : Power Management Capabilities		
DWord	Bit	Description
0	31:27	PME_SUPPORT
		Default Value: 00h
	Access: RO	
	PMES The graphics controller does not generate PME.	
	26	D2_SUPPORT
Default Value: 0b		
25	D1_SUPPORT	
	Default Value: 0b	
24:22	RESERVED	
	Default Value: 000b	
21	DEVICE_SPECIFIC_INITIALIZATION	
	Default Value: 1b	
20:19	RESERVED	
	Default Value: 00b	

PMCAPID - PMCAPID					
	<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td colspan="2">Reserved</td> </tr> </table>	Access:	RO	Reserved	
Access:	RO				
Reserved					
18:16	<p>VERSION</p> <table border="1"> <tr> <td>Default Value:</td> <td>010b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Version compliance with revision 1.1 of PCI Power management spec.</p>	Default Value:	010b	Access:	RO
Default Value:	010b				
Access:	RO				
15:8	<p>NEXT_POINTER</p> <table border="1"> <tr> <td>Default Value:</td> <td>90h</td> </tr> <tr> <td>Access:</td> <td>R/W Once</td> </tr> </table> <p>Indicates the next item in the capabilities list(90=MSI) This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset. Write once allowing changing of the capabilities list.</p>	Default Value:	90h	Access:	R/W Once
Default Value:	90h				
Access:	R/W Once				
7:0	<p>CAPABILITIES_ID</p> <table border="1"> <tr> <td>Default Value:</td> <td>01h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>CAPID: SIG defines this ID is 01h for power management.</p>	Default Value:	01h	Access:	RO
Default Value:	01h				
Access:	RO				

PMCS

PMCS - PMCS				
Register Space:	PCI: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	000D4h			
Power Management Control/Status. Driver does not use this register. SBIOS does not use this register				
DWord	Bit	Description		
0	31:2	RESERVED		
		<table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved</p>	Default Value:	00000000h
Default Value:	00000000h			
Access:	RO			
	1:0	POWER_STATE_PS		
		<table border="1"> <tr> <td>Default Value:</td> <td>00b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. On a transition from D3 to D0 the graphics controller is optionally reset to initial values. Behavior of the graphics controller in supported states is detailed in the power management section of the PRM. Bits[1:0] Power state 00: D0 Default 01: D1 Not Supported 10: D2 Not Supported 11: D3</p>	Default Value:	00b
Default Value:	00b			
Access:	R/W			

POWER_WELL_SS0_SIG1

POWER_WELL_SS0_SIG1 - POWER_WELL_SS0_SIG1			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x02020242		
Size (in bits):	32		
Address:	0A720h		
<p>Subwell signals to be driven out to subslice0 wells: Subwells 1-4. This register is modified by HW based on sub-power domain configuration and SW should not be writing to this register.</p>			
DWord	Bit	Description	
0	31:30	Reserved	
		Default Value:	00b
		Access:	RO
		Reserved	
	29	ss0_eu210_rst_b	
		Default Value:	0b
		Access:	R/W
		Subwell control signal 'rst_b' for subwell 'ss0_eu210'	
	28	ss0_eu210_fwenb	
		Default Value:	0b
		Access:	R/W
		Subwell control signal 'fwenb' for subwell 'ss0_eu210'	
27	ss0_eu210_pwrok		
	Default Value:	0b	
	Access:	R/W	
	Subwell control signal 'pwrok' for subwell 'ss0_eu210'		
26	ss0_eu210_asyncrst_b		
	Default Value:	0b	
	Access:	R/W	
	Subwell control signal 'asyncrst_b' for subwell 'ss0_eu210'		
25	ss0_eu210_pgenb		

POWER_WELL_SS0_SIG1 - POWER_WELL_SS0_SIG1						
		<table border="1"> <tr> <td>Default Value:</td> <td>1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Subwell control signal 'pgenb' for subwell 'ss0_eu210' 0 = sub-well is powered on. 1 = sub-well is powered off.</p>	Default Value:	1b	Access:	R/W
Default Value:	1b					
Access:	R/W					
24	ss0_eu210_clocken	<table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Subwell control signal 'clocken' for subwell 'ss0_eu210'</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
23:22	Reserved	<table border="1"> <tr> <td>Default Value:</td> <td>00b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved</p>	Default Value:	00b	Access:	RO
Default Value:	00b					
Access:	RO					
21	ss0_eu19_rst_b	<table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Subwell control signal 'rst_b' for subwell 'ss0_eu19'</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
20	ss0_eu19_fwenb	<table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Subwell control signal 'fwenb' for subwell 'ss0_eu19'</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
19	ss0_eu19_pwrok	<table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Subwell control signal 'pwrok' for subwell 'ss0_eu19'</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
18	ss0_eu19_asyncrst_b	<table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Subwell control signal 'asyncrst_b' for subwell 'ss0_eu19'</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
17	ss0_eu19_pgenb	<table border="1"> <tr> <td>Default Value:</td> <td>1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Default Value:	1b	Access:	R/W
Default Value:	1b					
Access:	R/W					

POWER_WELL_SS0_SIG1 - POWER_WELL_SS0_SIG1

		Subwell control signal 'pgenb' for subwell 'ss0_eu19' 0 = sub-well is powered on. 1 = sub-well is powered off.	
16	ss0_eu19_clocken	Subwell control signal 'clocken' for subwell 'ss0_eu19'	
	Default Value:	0b	
	Access:	R/W	
15:14	Reserved	Reserved	
	Default Value:	00b	
	Access:	RO	
13	ss0_eu08_rst_b	Subwell control signal 'rst_b' for subwell 'ss0_eu08'	
	Default Value:	0b	
	Access:	R/W	
12	ss0_eu08_fwenb	Subwell control signal 'fwenb' for subwell 'ss0_eu08'	
	Default Value:	0b	
	Access:	R/W	
11	ss0_eu08_pwrok	Subwell control signal 'pwrok' for subwell 'ss0_eu08'	
	Default Value:	0b	
	Access:	R/W	
10	ss0_eu08_asyncrst_b	Subwell control signal 'asyncrst_b' for subwell 'ss0_eu08'	
	Default Value:	0b	
	Access:	R/W	
9	ss0_eu08_pgenb	Subwell control signal 'pgenb' for subwell 'ss0_eu08' 0 = sub-well is powered on. 1 = sub-well is powered off.	
	Default Value:	1b	
	Access:	R/W	

POWER_WELL_SS0_SIG1 - POWER_WELL_SS0_SIG1						
	8	<p>ss0_eu08_clocken</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Subwell control signal 'clocken' for subwell 'ss0_eu08'</p>	Default Value:	0b	Access:	R/W
	Default Value:	0b				
	Access:	R/W				
	7	<p>Reserved</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved</p>	Default Value:	0b	Access:	RO
	Default Value:	0b				
	Access:	RO				
	6	<p>ss0_pgenb_sig1</p> <table border="1"> <tr> <td>Default Value:</td> <td>1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Subwell control signal 'pgenb' for subwell 'ss0_ss0'</p>	Default Value:	1b	Access:	R/W
	Default Value:	1b				
	Access:	R/W				
	5	<p>ss0_rst_b</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Subwell control signal 'rst_b' for subwell 'ss0_ss0'</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
4	<p>ss0_fwenb</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Subwell control signal 'fwenb' for subwell 'ss0_ss0'</p>	Default Value:	0b	Access:	R/W	
Default Value:	0b					
Access:	R/W					
3	<p>ss0_pwrok</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Subwell control signal 'pwrok' for subwell 'ss0_ss0'</p>	Default Value:	0b	Access:	R/W	
Default Value:	0b					
Access:	R/W					
2	<p>ss0_asyncrst_b</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Subwell control signal 'asyncrst_b' for subwell 'ss0_ss0'</p>	Default Value:	0b	Access:	R/W	
Default Value:	0b					
Access:	R/W					
1	<p>ss0_pgenb_sig0</p> <table border="1"> <tr> <td>Default Value:</td> <td>1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Default Value:	1b	Access:	R/W	
Default Value:	1b					
Access:	R/W					

POWER_WELL_SS0_SIG1 - POWER_WELL_SS0_SIG1					
	<p>Subwell control signal 'pgenb' for subwell 'ss0_ss0'</p> <p>0 = sub-well is powered on. 1 = sub-well is powered off.</p>				
0	<p>ss0_clocken</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>Subwell control signal 'clocken' for subwell 'ss0_ss0'</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				

POWER_WELL_SS0_SIG2

POWER_WELL_SS0_SIG2 - POWER_WELL_SS0_SIG2			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000002		
Size (in bits):	32		
Address:	0A724h		
<p>Subwell signals to be driven out to subslice0 wells: subwell 5. This register is modified by HW based on sub-power domain configuration and SW should not be writing to this register.</p>			
DWord	Bit	Description	
0	31:6	Reserved	
		Default Value:	0000000h
		Access:	RO
		Reserved	
	5	ss0_eu311_rst_b	
		Default Value:	0b
		Access:	R/W
	Subwell control signal 'rst_b' for subwell 'ss0_eu311'		
	4	ss0_eu311_fwenb	
		Default Value:	0b
		Access:	R/W
	Subwell control signal 'fwenb' for subwell 'ss0_eu311'		
	3	ss0_eu311_pwrok	
		Default Value:	0b
		Access:	R/W
	Subwell control signal 'pwrok' for subwell 'ss0_eu311'		
2	ss0_eu311_asyncrst_b		
	Default Value:	0b	
	Access:	R/W	
Subwell control signal 'asyncrst_b' for subwell 'ss0_eu311'			
1	ss0_eu311_pgenb		

POWER_WELL_SS0_SIG2 - POWER_WELL_SS0_SIG2					
	<table border="1"> <tr> <td>Default Value:</td> <td>1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Subwell control signal 'pgenb' for subwell 'ss0_eu311' 0 = sub-well is powered on. 1 = sub-well is powered off.</p>	Default Value:	1b	Access:	R/W
	Default Value:	1b			
Access:	R/W				
0	<p>ss0_eu311_clocken</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Subwell control signal 'clocken' for subwell 'ss0_eu311'</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				

POWER_WELL_SS1_SIG1

POWER_WELL_SS1_SIG1 - POWER_WELL_SS1_SIG1			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x02020242		
Size (in bits):	32		
Address:	0A728h		
<p>Subwell signals to be driven out to subslice1 wells: Subwells 1-4. This register is modified by HW based on sub-power domain configuration and SW should not be writing to this register.</p>			
DWord	Bit	Description	
0	31:30	Reserved	
		Default Value:	00b
		Access:	RO
			Reserved
	29	ss1_eu210_rst_b	
		Default Value:	0b
		Access:	R/W
			Subwell control signal 'rst_b' for subwell 'ss1_eu210'
	28	ss1_eu210_fwenb	
		Default Value:	0b
Access:		R/W	
		Subwell control signal 'fwenb' for subwell 'ss1_eu210'	
27	ss1_eu210_pwrok		
	Default Value:	0b	
	Access:	R/W	
		Subwell control signal 'pwrok' for subwell 'ss1_eu210'	
26	ss1_eu210_asyncrst_b		
	Default Value:	0b	
	Access:	R/W	
		Subwell control signal 'asyncrst_b' for subwell 'ss1_eu210'	
25	ss1_eu210_pgenb		

POWER_WELL_SS1_SIG1 - POWER_WELL_SS1_SIG1

		Default Value:	1b
		Access:	R/W
		Subwell control signal 'pgenb' for subwell 'ss1_eu210' 0 = sub-well is powered on. 1 = sub-well is powered off.	
24	ss1_eu210_clocken	Default Value:	0b
		Access:	R/W
		Subwell control signal 'clocken' for subwell 'ss1_eu210'	
23:22	Reserved	Default Value:	00b
		Access:	RO
		Reserved	
21	ss1_eu19_rst_b	Default Value:	0b
		Access:	R/W
		Subwell control signal 'rst_b' for subwell 'ss1_eu19'	
20	ss1_eu19_fwenb	Default Value:	0b
		Access:	R/W
		Subwell control signal 'fwenb' for subwell 'ss1_eu19'	
19	ss1_eu19_pwrok	Default Value:	0b
		Access:	R/W
		Subwell control signal 'pwrok' for subwell 'ss1_eu19'	
18	ss1_eu19_asyncrst_b	Default Value:	0b
		Access:	R/W
		Subwell control signal 'asyncrst_b' for subwell 'ss1_eu19'	
17	ss1_eu19_pgenb	Default Value:	1b
		Access:	R/W

POWER_WELL_SS1_SIG1 - POWER_WELL_SS1_SIG1					
	Subwell control signal 'pgenb' for subwell 'ss1_eu19' 0 = sub-well is powered on. 1 = sub-well is powered off.				
16	<p>ss1_eu19_clocken</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Subwell control signal 'clocken' for subwell 'ss1_eu19'</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
15:14	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>00b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved</p>	Default Value:	00b	Access:	RO
Default Value:	00b				
Access:	RO				
13	<p>ss1_eu08_rst_b</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Subwell control signal 'rst_b' for subwell 'ss1_eu08'</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
12	<p>ss1_eu08_fwenb</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Subwell control signal 'fwenb' for subwell 'ss1_eu08'</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
11	<p>ss1_eu08_pwrok</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Subwell control signal 'pwrok' for subwell 'ss1_eu08'</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
10	<p>ss1_eu08_asyncrst_b</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Subwell control signal 'asyncrst_b' for subwell 'ss1_eu08'</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
9	<p>ss1_eu08_pgenb</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Subwell control signal 'pgenb' for subwell 'ss1_eu08' 0 = sub-well is powered on. 1 = sub-well is powered off.</p>	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				

POWER_WELL_SS1_SIG1 - POWER_WELL_SS1_SIG1						
8	<p>ss1_eu08_clocken</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Subwell control signal 'clocken' for subwell 'ss1_eu08'</p>	Default Value:	0b	Access:	R/W	
	Default Value:	0b				
	Access:	R/W				
	7	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved</p>	Default Value:	0b	Access:	RO
		Default Value:	0b			
		Access:	RO			
	6	<p>ss1_pgenb_sig1</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Subwell control signal 'pgenb' for subwell 'ss1_ss1'</p>	Default Value:	1b	Access:	R/W
		Default Value:	1b			
Access:		R/W				
5	<p>ss1_rst_b</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Subwell control signal 'rst_b' for subwell 'ss1_ss1'</p>	Default Value:	0b	Access:	R/W	
	Default Value:	0b				
	Access:	R/W				
4	<p>ss1_fwenb</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Subwell control signal 'fwenb' for subwell 'ss1_ss1'</p>	Default Value:	0b	Access:	R/W	
	Default Value:	0b				
	Access:	R/W				
3	<p>ss1_pwrok</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Subwell control signal 'pwrok' for subwell 'ss1_ss1'</p>	Default Value:	0b	Access:	R/W	
	Default Value:	0b				
	Access:	R/W				
2	<p>ss1_asyncrst_b</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Subwell control signal 'asyncrst_b' for subwell 'ss1_ss1'</p>	Default Value:	0b	Access:	R/W	
	Default Value:	0b				
	Access:	R/W				
1	<p>ss1_pgenb_sig0</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Default Value:	1b	Access:	R/W	
	Default Value:	1b				
	Access:	R/W				

POWER_WELL_SS1_SIG1 - POWER_WELL_SS1_SIG1					
	<p>Subwell control signal 'pgenb' for subwell 'ss1_ss1'</p> <p>0 = sub-well is powered on. 1 = sub-well is powered off.</p>				
0	<p>ss1_clocken</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>Subwell control signal 'clocken' for subwell 'ss1_ss1'</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				

POWER_WELL_SS1_SIG2

POWER_WELL_SS1_SIG2 - POWER_WELL_SS1_SIG2			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000002		
Size (in bits):	32		
Address:	0A72Ch		
<p>Subwell signals to be driven out to subslice1 wells: subwell 5. This register is modified by HW based on sub-power domain configuration and SW should not be writing to this register.</p>			
DWord	Bit	Description	
0	31:6	Reserved	
		Default Value:	0000000h
		Access:	RO
		Reserved	
	5	ss1_eu311_rst_b	
		Default Value:	0b
		Access:	R/W
	Subwell control signal 'rst_b' for subwell 'ss1_eu311'		
	4	ss1_eu311_fwenb	
		Default Value:	0b
		Access:	R/W
	Subwell control signal 'fwenb' for subwell 'ss1_eu311'		
	3	ss1_eu311_pwrok	
		Default Value:	0b
		Access:	R/W
	Subwell control signal 'pwrok' for subwell 'ss1_eu311'		
	2	ss1_eu311_asyncrst_b	
		Default Value:	0b
		Access:	R/W
Subwell control signal 'asyncrst_b' for subwell 'ss1_eu311'			

POWER_WELL_SS1_SIG2 - POWER_WELL_SS1_SIG2					
1	ss1_eu311_pgenb <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">1b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>Subwell control signal 'pgenb' for subwell 'ss1_eu311' 0 = sub-well is powered on. 1 = sub-well is powered off.</p>	Default Value:	1b	Access:	R/W
	Default Value:	1b			
Access:	R/W				
0	ss1_eu311_cloken <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>Subwell control signal 'cloken' for subwell 'ss1_eu311'</p>	Default Value:	0b	Access:	R/W
	Default Value:	0b			
Access:	R/W				

Power Context Save

PWRCTXSAVE - Power Context Save			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	04A04h		
DWord	Bit	Description	
0	31:16	Mask Bits	
		Default Value:	0000h
		Access:	RO
	15	Extra Bits15	
		Default Value:	0b
		Access:	R/W
	Extra Bits for future use.		
14	Extra Bits14		
	Default Value:	0b	
	Access:	R/W	
Extra Bits for future use.			
13	Extra Bits13		
	Default Value:	0b	
	Access:	R/W	
Extra Bits for future use.			
12	Extra Bits12		
	Default Value:	0b	
	Access:	R/W	
Extra Bits for future use.			
11	Extra Bits11		
	Default Value:	0b	
	Access:	R/W	
Extra Bits for future use.			
10	Extra Bits10		
	Default Value:	0b	
	Access:	R/W	
Extra Bits for future use.			

PWRCTXSAVE - Power Context Save					
9	<p>Power Context Save Request</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Power Context Save. Bit[9].Power Context Save Request. 1'b0: Power context save is not being requested (default). 1'b1: Power context save is being requested. Unit needs to self-clear this bit upon sampling. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
8:0	<p>Power Context Save Quad Word Credits</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Default Value:</td> <td>000000000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Power Context Save. Bits[8:0].QWord Credits for Power Context Save Request. An initial length packet is required per power context save session, but that packet does not consume a credit. See protocol description for more details. Minimum Credits = 1: Unit may send 1 QWord pair. Maximum Credits = 511: Unit may send 511 QWord pairs. A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Only valid with PWRCTX_SAVE_REQ (Bit9).</p>	Default Value:	000000000b	Access:	R/W
Default Value:	000000000b				
Access:	R/W				

Power context Save Register for LPFC

LPCSR - Power context Save Register for LPFC		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B408h	
DWord	Bit	Description
0	31:10	Reserved
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Reserved.
Access:	RO	
	9:0	Power context save register command
		<table border="1"> <tr> <td>Access:</td> <td>R/W Hardware Clear</td> </tr> </table> Bit[9].Power Context Save Request. 1'b0: Power context save is not being requested (default). 1'b1: Power context save is being requested. Unit needs to self-clear this bit upon sampling. Bits[8:0].QWord Credits for Power Context Save Request. Minimum Credits = 1: Unit may send 1 QWord pair (enough for first LRI at least). Maximum Credits = 511: Unit may send 511 QWord pairs. A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).
Access:	R/W Hardware Clear	

Power Context Save request

PCTXSAVEREQ - Power Context Save request				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	08110h			
DWord	Bit	Description		
0	31:16	<p>Message Mask</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Message Mask bits for lower 16 bits</p>	Access:	RO
	Access:	RO		
	15:10	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved</p>	Access:	RO
	Access:	RO		
9	<p>Power context save req</p> <table border="1"> <tr> <td>Access:</td> <td>R/W Set</td> </tr> </table> <p>Power Context Save Request 1'b0 : Power context save is not being requested (default) 1'b1 : Power context save is being requested CUnit self-clears this bit upon sampling.</p>	Access:	R/W Set	
Access:	R/W Set			
8:0	<p>Power Context Save request credit count</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).</p>	Access:	R/W	
Access:	R/W			

POWERDOWN_STATE

POWERDOWN_STATE - POWERDOWN_STATE			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x66654321		
Size (in bits):	32		
Address:	0A710h		
Subwell Power down state description.			
DWord	Bit	Description	
0	31:28	pmcr_powerdown_state8	
		Default Value:	0110b
		Access:	R/W
			The 8th state/signal that needs to be driven
	27:24	pmcr_powerdown_state7	
		Default Value:	0110b
		Access:	R/W
			The 7th state/signal that needs to be driven
	23:20	pmcr_powerdown_state6	
		Default Value:	0110b
		Access:	R/W
			The 6th state/signal that needs to be driven
	19:16	pmcr_powerdown_state5	
		Default Value:	0101b
		Access:	R/W
			The 5th state/signal that needs to be driven
	15:12	pmcr_powerdown_state4	
		Default Value:	0100b
		Access:	R/W
			The 4th state/signal that needs to be driven
	11:8	pmcr_powerdown_state3	
		Default Value:	0011b
		Access:	R/W

POWERDOWN_STATE - POWERDOWN_STATE	
	The 3rd state/signal that needs to be driven
7:4	pmcr_powerdown_state2
	Default Value: 0010b
	Access: R/W
	The 2nd state/signal that needs to be driven
3:0	pmcr_powerdown_state1
	Default Value: 0001b
	Access: R/W
	<p>This is the very first state and the signal that needs to be driven appropriately</p> <p>Encodings:</p> <ul style="list-style-type: none"> 001 = Reset Sync Reset 010 = Reset Firewall 011 = Set Power EnB 100 = Reset Clock En 101 = Reset Async Reset 110 = Done 111 = Reserved. <p>Open: Do we want to have an extra bit for future support</p>

POWERDOWN_WAIT1

POWERDOWN_WAIT1 - POWERDOWN_WAIT1			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x01010101		
Size (in bits):	32		
Address:	0A714h		
Subwell power down state wait time 1.			
DWord	Bit	Description	
0	31:24	pmcr_powerdown_wait_state4_5	
		Default Value:	01h
		Access:	R/W
		This is the programmed value as to how long there is a wait from the time signal 4 is driven before signal 5 can be driven	
	23:16	pmcr_powerdown_wait_state3_4	
		Default Value:	01h
		Access:	R/W
		This is the programmed value as to how long there is a wait from the time signal 3 is driven before signal 4 can be driven	
	15:8	pmcr_powerdown_wait_state2_3	
		Default Value:	01h
		Access:	R/W
		This is the programmed value as to how long there is a wait from the time signal 2 is driven before signal 3 can be driven	
	7:0	pmcr_powerdown_wait_state1_2	
		Default Value:	01h
		Access:	R/W
		This is the programmed value as to how long there is a wait from the time signal 1 is driven before signal 2 can be driven. Note: The granularity of these are in 30ns intervals meaning the counters will increment/decrement every 30ns pulse	

POWERDOWN_WAIT2

POWERDOWN_WAIT2 - POWERDOWN_WAIT2			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x01010101		
Size (in bits):	32		
Address:	0A718h		
Subwell power down state wait time 2.			
DWord	Bit	Description	
0	31:24	pmcr_powerdown_interval	
		Default Value:	01h
		Access:	R/W
		Stagger between different power gate enables for power down.	
	23:16	pmcr_powerdown_wait_state7_8	
		Default Value:	01h
		Access:	R/W
		This is the programmed value as to how long there is a wait from the time signal 7 is driven before signal 8 can be driven	
	15:8	pmcr_powerdown_wait_state6_7	
		Default Value:	01h
		Access:	R/W
		This is the programmed value as to how long there is a wait from the time signal 6 is driven before signal 7 can be driven	
	7:0	pmcr_powerdown_wait_state5_6	
		Default Value:	01h
		Access:	R/W
		This is the programmed value as to how long there is a wait from the time signal 5 is driven before signal 6 can be driven	

Power Down/Up Control

PWRDWNUPCTL - Power Down/Up Control				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A294h-0A297h			
DWord	Bit	Description		
0	31:4	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	3	<p>Block Signaling Policy</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>BlockAll signaling policy register. Applies to signaling sent to Wake FIFO (ie. IA GT FIFO and HW FIFO). 0 (default) : BlockALL signal only asserts for CPD. 1 : BlockALL signal can assert for CPD and for a timeperiod during RC6 entry. Note : This affects MMIO requests crossing from CZ clock domain to message channel in Gfx clock domain.</p>	Access:	R/W
	Access:	R/W		
	2	<p>Serialize Power Requests</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Determines whether simultaneous requests to REMOVE power are presented to the Punit at the same time or whether the handshake for one must complete before the handshake for the other may start. 0=simultaneous 1=serial</p>	Access:	R/W
Access:	R/W			
1	<p>Powerdown Request Order</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Determines which well is disabled first if both wells are requesting to enter standby simultaneously, if serialized. 0=render well power is removed first 1=media well power is removed first.</p>	Access:	R/W	
Access:	R/W			
0	<p>Wake Media First</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>When waking both wells, it determines which well wakes first. 0=wake render first 1=wake media first. (It is NOT possible to wake both simultaneously for di/dt reasons)</p>	Access:	R/W	
Access:	R/W			

Power Enable stagger control

PWRENSTAGCNTRL - Power Enable stagger control		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000001	
Size (in bits):	32	
Address:	0A70Ch	
Power Enable Stagger Control		
DWord	Bit	Description
0	31:8	Reserved
		Access: RO
	7:0	pgen_phase_interval
		Default Value: 01h
Access: R/W		
<p>It is the separation between pgen0 and pgen1 on SSx. (units = 30ns) Default value 0x01. (Real silicon settings will be determined by circuit simulation, but expect it to be no higher than 0x21. Nominally, expect it to be 0x0A)</p>		

Power Meter Weight for gti_idle_cz

PMWGICZ - Power Meter Weight for gti_idle_cz				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	1300A4h			
This register contains the power meter weight for the idleness in CZ clock domain.				
DWord	Bit	Description		
0	31:16	RESERVED		
		<table border="1"> <tr> <td>Default Value:</td> <td>0000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved</p>	Default Value:	0000h
Default Value:	0000h			
Access:	RO			
	15:0	PMWGICZ		
		<table border="1"> <tr> <td>Default Value:</td> <td>0000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This 16-bit value is used to indicate how often to accumulate power within the CZ clock domain. When this field is set to zero, CZ clock domain will not contribute to the overall energy count. Otherwise, the value in this register will dictate how often to add CZ power contribution.</p>	Default Value:	0000h
Default Value:	0000h			
Access:	R/W			

Power Meter Weight for gti_idle_gs

PWRMTR_WT_GTI - Power Meter Weight for gti_idle_gs		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0AABCh	
DWord	Bit	Description
0	31:16	Reserved
		Access: RO
	15:0	Power Meter Weight GTI
		Access: R/W Power meter weight for gti_idle_gs.

Power Meter Weight for media/render

PWRMTR_WT_MEDREN - Power Meter Weight for media/render				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0AAB8h			
DWord	Bit	Description		
0	31:16	Power Meter Weight Render <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Power meter weight for render_idle.	Access:	R/W
	Access:	R/W		
15:0	Power Meter Weight Media <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Power meter event weight media_idle.	Access:	R/W	
Access:	R/W			

POWERUP_STATE

POWERUP_STATE - POWERUP_STATE			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x76543210		
Size (in bits):	32		
Address:	0A700h		
Subwell Power up state description.			
DWord	Bit	Description	
0	31:28	pmcr_powerup_state8	
		Default Value:	0111b
		Access:	R/W
			The 8th state/signal that needs to be driven
	27:24	pmcr_powerup_state7	
		Default Value:	0110b
		Access:	R/W
			The 7th state/signal that needs to be driven
	23:20	pmcr_powerup_state6	
		Default Value:	0101b
		Access:	R/W
			The 6th state/signal that needs to be driven
	19:16	pmcr_powerup_state5	
		Default Value:	0100b
		Access:	R/W
			The 5th state/signal that needs to be driven
	15:12	pmcr_powerup_state4	
		Default Value:	0011b
		Access:	R/W
			The 4th state/signal that needs to be driven
	11:8	pmcr_powerup_state3	
		Default Value:	0010b
		Access:	R/W

POWERUP_STATE - POWERUP_STATE		
		The 3rd state/signal that needs to be driven
7:4	pmcr_powerup_state2	
	Default Value:	0001b
	Access:	R/W
		The 2nd state/signal that needs to be driven
3:0	pmcr_powerup_state1	
	Default Value:	0000b
	Access:	R/W
		This is the very first state and the signal that needs to be driven appropriately Encodings: 0000 = First Set Clock En 0001 = Reset Power EnB 0010 = Reset Clock En 0011 = Set Firewall 0100 = Set Async Reset/ Set Pwrok 0101 = Final Set clock en 0110 = Set Sync Reset. 0111 = Done 1xxx = Reserved for future

POWERUP_WAIT1

POWERUP_WAIT1 - POWERUP_WAIT1			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x01010101		
Size (in bits):	32		
Address:	0A704h		
Subwell power up state wait time 1			
DWord	Bit	Description	
0	31:24	pmcr_powerup_wait_state4_5	
		Default Value:	01h
		Access:	R/W
		This is the programmed value as to how long there is a wait from the time signal 4 is driven before signal 5 can be driven	
	23:16	pmcr_powerup_wait_state3_4	
		Default Value:	01h
		Access:	R/W
		This is the programmed value as to how long there is a wait from the time signal 3 is driven before signal 4 can be driven	
	15:8	pmcr_powerup_wait_state2_3	
		Default Value:	01h
		Access:	R/W
		This is the programmed value as to how long there is a wait from the time signal 2 is driven before signal 3 can be driven	
	7:0	pmcr_powerup_wait_state1_2	
		Default Value:	01h
		Access:	R/W
		This is the programmed value as to how long there is a wait from the time signal 1 is driven before signal 2 can be driven. Note: The granularity of these are in 30ns intervals meaning the counters will increment or decrement every 30ns pulse unless we are asserting clocken in which case it is on a usync boundary	

POWERUP_WAIT2

POWERUP_WAIT2 - POWERUP_WAIT2			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x01010101		
Size (in bits):	32		
Address:	0A708h		
Subwell power up state wait time 2.			
DWord	Bit	Description	
0	31:24	pmcr_powerup_interval	
		Default Value:	01h
		Access:	R/W
		Stagger between different power gate enables on power up	
	23:16	pmcr_powerup_wait_state7_8	
		Default Value:	01h
		Access:	R/W
		This is the programmed value as to how long there is a wait from the time signal 7 is driven before signal 8 can be driven	
	15:8	pmcr_powerup_wait_state6_7	
		Default Value:	01h
		Access:	R/W
		This is the programmed value as to how long there is a wait from the time signal 6 is driven before signal 7 can be driven	
7:0	pmcr_powerup_wait_state5_6		
	Default Value:	01h	
	Access:	R/W	
	This is the programmed value as to how long there is a wait from the time signal 5 is driven before signal 6 can be driven		

PPGTT Page Fault Data Registers

PP_PFD[0:31] - PPGTT Page Fault Data Registers		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	04580h	
<p>The GTT Page Fault Log entries can be read from these registers. 4580h-4583h: Fault Entry 0 ... 45FCh-45FFh: Fault Entry 31</p>		
DWord	Bit	Description
0	31:12	Fault Entry Page Address Format: <input type="text" value="GraphicsAddress[31:12]"/> This RO field contains the faulting page address for this Fault Log entry. This field will contain a valid fault address only if the bit in the GTT Page Fault Indication Register corresponding with the address offset of this entry is set.
	11:0	Reserved Format: <input type="text" value="MBZ"/>

Predicate Rendering Data Result

MI_PREDICATE_RESULT - Predicate Rendering Data Result		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02418h	
Valid Projects:		
DWord	Bit	Description
0	31:1	Reserved
		Format: MBZ
	0	MI_PREDICATE_RESULT This bit is the result of the last MI_PREDICATE.

Predicate Rendering Data Result 1

MI_PREDICATE_RESULT_1 - Predicate Rendering Data Result 1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	0241Ch-0241Fh	
Name:	Predicate Rendering Data Result 1	
ShortName:	MI_PREDICATE_RESULT_1_RCSUNIT	
Address:	1241Ch-1241Fh	
Name:	Predicate Rendering Data Result 1	
ShortName:	MI_PREDICATE_RESULT_1_VCSUNIT0	
Address:	1A41Ch-1A41Fh	
Name:	Predicate Rendering Data Result 1	
ShortName:	MI_PREDICATE_RESULT_1_VECSUNIT	
Address:	1C41Ch-1C41Fh	
Name:	Predicate Rendering Data Result 1	
ShortName:	MI_PREDICATE_RESULT_1_VCSUNIT1	
Address:	2241Ch-2241Fh	
Name:	Predicate Rendering Data Result 1	
ShortName:	MI_PREDICATE_RESULT_1_BCSUNIT	
DWord	Bit	Description
0	31:1	Reserved
		Format: MBZ
0		MI_PREDICATE_RESULT_1 This bit is used to predicate MI_BATCH_BUFFER_START commands in the RCS command stream. Usage Model: MI_MATH command will be used to do some ALU operations over GPR followed by a MI_LOAD_REGISTER_REGISTER to move the result from GPR to MI_PREDICATE_RESULT_1.

Predicate Rendering Data Result 2

MI_PREDICATE_RESULT_2 - Predicate Rendering Data Result 2										
Register Space:	MMIO: 0/2/0									
Project:	CHV, BSW									
Source:	PRM									
Default Value:	0x00000000									
Access:	R/W									
Size (in bits):	32									
Address:	023BCh-023BFh									
Name:	Predicate Rendering Data Result 2									
ShortName:	MI_PREDICATE_RESULT_2_RCSUNIT									
Valid Projects:	CHV, BSW									
Address:	123BCh-123BFh									
Name:	Predicate Rendering Data Result 2									
ShortName:	MI_PREDICATE_RESULT_2_VCSUNIT0									
Valid Projects:	CHV, BSW									
Address:	1A3BCh-1A3BFh									
Name:	Predicate Rendering Data Result 2									
ShortName:	MI_PREDICATE_RESULT_2_VECSUNIT									
Valid Projects:	CHV, BSW									
Address:	1C3BCh-1C3BFh									
Name:	Predicate Rendering Data Result 2									
ShortName:	MI_PREDICATE_RESULT_2_VCSUNIT1									
Valid Projects:	CHV, BSW									
Address:	223BCh-223BFh									
Name:	Predicate Rendering Data Result 2									
ShortName:	MI_PREDICATE_RESULT_2_BCSUNIT									
DWord	Bit	Description								
0	31:1	Reserved Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td>MBZ</td></tr></table>		MBZ						
		MBZ								
0	<p>MI_PREDICATE_RESULT_2 This bit must be loaded with by SW based on GT mode of operation. This register must be loaded appropriately before using MI_SET_PREDICATE command.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 70%;">Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>[Default]</td> <td>Indicates GT2 mode and lower slice is disabled.</td> </tr> <tr> <td>1h</td> <td></td> <td>Indicates GT3 mode and lower slice is enabled.</td> </tr> </tbody> </table>	Value	Name	Description	0h	[Default]	Indicates GT2 mode and lower slice is disabled.	1h		Indicates GT3 mode and lower slice is enabled.
Value	Name	Description								
0h	[Default]	Indicates GT2 mode and lower slice is disabled.								
1h		Indicates GT3 mode and lower slice is enabled.								

Predicate Rendering Data Storage

MI_PREDICATE_DATA - Predicate Rendering Data Storage		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Address:	02410h-02417h	
Valid Projects:		
DWord	Bit	Description
0	63:32	MI_PREDICATE_DATA_UDW This register is used either as computed value based off the MI_PREDICATE_SRC0 and MI_PREDICATE_SRC1 or a temporary register. See Predicate Rendering section for more details.
	31:0	MI_PREDICATE_DATA_LDW This register is used either as computed value based off the MI_PREDICATE_SRC0 and MI_PREDICATE_SRC1 or a temporary register. See Predicate Rendering section for more details.

Predicate Rendering Temporary Register0

MI_PREDICATE_SRC0 - Predicate Rendering Temporary Register0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Address:	02400h-02407h	
Valid Projects:		
DWord	Bit	Description
0	63:0	MI_PREDICATE_SRC0 This register is a temporary register for Predicate Rendering. See Predicate Rendering section for more details.

Predicate Rendering Temporary Register1

MI_PREDICATE_SRC1 - Predicate Rendering Temporary Register1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Address:	02408h-0240Fh	
Valid Projects:	CHV, BSW	
DWord	Bit	Description
0	63:0	MI_PREDICATE_SRC1 This register is a temporary register for Predicate Rendering. See Predicate Rendering section for more details.

Previous Idle/Busy/Avg Count for Freq Down Recommendation

RPPREVDN - Previous Idle/Busy/Avg Count for Freq Down Recommendation				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A064h-0A067h			
DWord	Bit	Description		
0	31:24	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%; text-align: center;">RO</td> </tr> </table> Reserved	Access:	RO
	Access:	RO		
23:0	Previous Busy in Down EI <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%; text-align: center;">RO</td> </tr> </table> Previous Busy in Down EI (PRVBSYTAVG): Reports the busyness at the end of the previous down evaluation interval 0 = 0 usec 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec pmcr_previous_ei_down_busy[23:0]	Access:	RO	
Access:	RO			

Previous Idle/Busy/Avg Count for Freq Up Recommendation

RPPREVUP - Previous Idle/Busy/Avg Count for Freq Up Recommendation				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A058h-0A05Bh			
DWord	Bit	Description		
0	31:24	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%;">RO</td> </tr> </table> <p>Reserved</p>	Access:	RO
	Access:	RO		
23:0	<p>Previous Busy in UP EI</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%;">RO</td> </tr> </table> <p>Reports the busyness at the end of the previous Up evaluation interval</p> <p>0 = 0 usec 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec</p> <p>pmcr_previous_ei_up_busy[23:0]</p>	Access:	RO	
Access:	RO			

Primitives Generated By VF

IA_PRIMITIVES_COUNT - Primitives Generated By VF		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	02318h	
Valid Projects:		
This register stores the count of primitives generated by VF. This register is part of the context save and restore.		
DWord	Bit	Description
0	63:32	IA Primitives Count Report UDW Total number of primitives output by the Vertex Fetch (IA) stage. This count is updated for every primitive output by the VF stage, as long as Statistics Enable is set in VF_STATE (see the Vertex Fetch Chapter in the 3D Volume.)
	31:0	IA Primitives Count Report LDW Total number of primitives output by the Vertex Fetch (IA) stage. This count is updated for every primitive output by the VF stage, as long as Statistics Enable is set in VF_STATE (see the Vertex Fetch Chapter in the 3D Volume.)

Private PAT

PRIV_PAT - Private PAT												
Register Space:	MMIO: 0/2/0											
Project:	CHV, BSW											
Source:	PRM											
Default Value:	0x00000003											
Size (in bits):	32											
Address:	040E8h											
DWord	Bit	Description										
0	31:0	Private PAT										
		Default Value:	00000003h									
		Access:	R/W									
		<table border="1"> <thead> <tr> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>Bit[31:8]: Reserved.</td> <td></td> </tr> <tr> <td>Bit[7]: Reserved.</td> <td rowspan="11">CHV, BSW</td> </tr> <tr> <td>Bit[6]: Snoop Required [CHV, BSW Only] 1: System agent will snoop the IA cores 0: System agent will not snoop the IA cores</td> </tr> <tr> <td>Bit[5:4]: (See below.) 00b: Age is 0. 01b: Age is 1. 10b: Age is 2. 11b: Age is 3.</td> </tr> <tr> <td>Bit[3:2]: (See below.) 00b: eLLC only. 01b: LLC only. 10b: LLC and eLLC allowed. 11b: L3, LLC, and eLLC are allowed.</td> </tr> <tr> <td>Bit[1:0]: (see below): 00b: Uncacheable (UC). 01b: Write Combining (WC). 10b: Write Through (WT). 11b: Write Back (WB).</td> </tr> </tbody> </table>	Description	Project	Bit[31:8]: Reserved.		Bit[7]: Reserved.	CHV, BSW	Bit[6]: Snoop Required [CHV, BSW Only] 1: System agent will snoop the IA cores 0: System agent will not snoop the IA cores	Bit[5:4]: (See below.) 00b: Age is 0. 01b: Age is 1. 10b: Age is 2. 11b: Age is 3.	Bit[3:2]: (See below.) 00b: eLLC only. 01b: LLC only. 10b: LLC and eLLC allowed. 11b: L3, LLC, and eLLC are allowed.	Bit[1:0]: (see below): 00b: Uncacheable (UC). 01b: Write Combining (WC). 10b: Write Through (WT). 11b: Write Back (WB).
Description	Project											
Bit[31:8]: Reserved.												
Bit[7]: Reserved.	CHV, BSW											
Bit[6]: Snoop Required [CHV, BSW Only] 1: System agent will snoop the IA cores 0: System agent will not snoop the IA cores												
Bit[5:4]: (See below.) 00b: Age is 0. 01b: Age is 1. 10b: Age is 2. 11b: Age is 3.												
Bit[3:2]: (See below.) 00b: eLLC only. 01b: LLC only. 10b: LLC and eLLC allowed. 11b: L3, LLC, and eLLC are allowed.												
Bit[1:0]: (see below): 00b: Uncacheable (UC). 01b: Write Combining (WC). 10b: Write Through (WT). 11b: Write Back (WB).												

Private PAT

PRIV_PAT - Private PAT						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	040E8h					
DWord	Bit	Description				
0	31:0	<p>Private PAT</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit[31:16]: Reserved. Bit[15:8]: PPGTT Private PAT. (See bit[7:0] for definition.)</p> <p>Bit[7:6]: Reserved. Bit[5:4]: (See below.) 00b: Age is 0. 01b: Age is 1. 10b: Age is 2. 11b: Age is 3. Bit[3:2]: (See below.) 00b: Override to eLLC Only. (This setting overrides the memory_object_control_state via surface state to be eLLC target only.) 01b: eLLC only. 10b: LLC only. 11b: eLLC/LLC. Bit[1:0]: (see below): 00b: Uncached with fence. 01b: Write Combining (traditional UC). 10b: Write Through. 11b: Write Back.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

PS Depth Count

PS_DEPTH_COUNT - PS Depth Count		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	02350h	
<p>This register stores the value of the count of samples that have passed the depth test. This register is part of the context save and restore. Note that the value of this register can be obtained in a pipeline-synchronous fashion without a pipeline flush by using the 3DCONTROL command. See 3D Overview in the 3D volume.</p>		
DWord	Bit	Description
0..1	63:32	<p>Depth Count UDW</p> <p>This register reflects the total number of samples that have passed the depth test (i.e., will be visible). All samples are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Samples that pass the depth test but fail the stencil test will not be counted.</p>
	31:0	<p>Depth Count LDW</p> <p>This register reflects the total number of samples that have passed the depth test (i.e., will be visible). All samples are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Samples that pass the depth test but fail the stencil test will not be counted.</p>

PS Depth Count for Slice0

PS_DEPTH_COUNT_SLICE0 - PS Depth Count for Slice0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	022D8h	
<p>This register stores the value of the count of pixels that have passed the depth test in Slice0. This register is part of the context save and restore. This register should not be programmed by SW. Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).</p>		
DWord	Bit	Description
0..1	63:32	<p>Depth Count UDW</p> <p>This register reflects the total number of pixels that have passed the depth test in Slice0(i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.</p>
	31:0	<p>Depth Count LDW</p> <p>This register reflects the total number of pixels that have passed the depth test in Slice0(i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.</p>

PS Depth Count for Slice1

PS_DEPTH_COUNT_SLICE1 - PS Depth Count for Slice1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	022F8h	
<p>This register stores the value of the count of pixels that have passed the depth test in Slice1. This register is part of the context save and restore. This register should not be programmed by SW. Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).</p>		
DWord	Bit	Description
0..1	63:32	<p>Depth Count UDW</p> <p>This register reflects the total number of pixels that have passed the depth test in Slice1 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.</p>
	31:0	<p>Depth Count LDW</p> <p>This register reflects the total number of pixels that have passed the depth test in Slice1 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.</p>

PS Depth Count for Slice2

PS_DEPTH_COUNT_SLICE2 - PS Depth Count for Slice2		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	02450h	
<p>This register stores the value of the count of pixels that have passed the depth test in Slice2. This register is part of the render context save and restore. This register should not be programmed by SW.</p>		
DWord	Bit	Description
0..1	63:32	<p>Depth Count UDW</p> <p>This register reflects the depth test in slice2 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.</p>
	31:0	<p>Depth Count LDW</p> <p>This register reflects the depth test in slice2 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.</p>

PS Depth Count for Slice3

PS_DEPTH_COUNT_SLICE3 - PS Depth Count for Slice3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	02460h	
<p>This register stores the value of the count of pixels that have passed the depth test in Slice3. This register is part of the render context save and restore. This register should not be programmed by SW.</p>		
DWord	Bit	Description
0..1	63:32	<p>Depth Count UDW</p> <p>This register reflects the depth test in slice3 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.</p>
	31:0	<p>Depth Count LDW</p> <p>This register reflects the depth test in slice3 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.</p>

PS Invocation Count

PS_INVOCATION_COUNT - PS Invocation Count		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	02348h	
DWord	Bit	Description
0..1	63:32	PS Invocation Count UDW Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	PS Invocation Count LDW Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice0

PS_INVOCATION_COUNT_SLICE0 - PS Invocation Count for Slice0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	022C8h	
<p>This register stores the value of the count of pixels that get shaded in Slice0. This register is part of the context save and restore. This register should not be programmed by SW. Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).</p>		
Workaround		
HW reports this count 4X the actual value and therefore SW must divide the count by 4 for correct reporting.		
DWord	Bit	Description
0..1	63:32	PS Invocation Count UDW Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice0. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	PS Invocation Count LDW Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice0. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice1

PS_INVOCATION_COUNT_SLICE1 - PS Invocation Count for Slice1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	022F0h	
<p>This register stores the value of the count of pixels that get shaded in Slice0. This register is part of the context save and restore. This register should not be programmed by SW. Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).</p>		
Workaround		
<p>Workaround: HW reports this count 4X the actual value and therefore SW must divide the count by 4 for correct reporting.</p>		
DWord	Bit	Description
0..1	63:32	<p>PS Invocation Count UDW</p> <p>Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice1. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.</p>
	31:0	<p>PS Invocation Count LDW</p> <p>Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice1. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.</p>

PS Invocation Count for Slice2

PS_INVOCATION_COUNT_SLICE2 - PS Invocation Count for Slice2		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	02448h	
<p>This register stores the value of the count of pixels that get shaded in Slice2. This register is part of the render context save and restore. This register should not be programmed by SW.</p>		
DWord	Bit	Description
0..1	63:32	<p>PS Invocation Count UDW</p> <p>Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice2. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.</p>
	31:0	<p>PS Invocation Count LDW</p> <p>Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice2. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.</p>

PS Invocation Count for Slice3

PS_INVOCATION_COUNT_SLICE3 - PS Invocation Count for Slice3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	02458h	
<p>This register stores the value of the count of pixels that get shaded in Slice3. This register is part of the render context save and restore. This register should not be programmed by SW.</p>		
DWord	Bit	Description
0..1	63:32	<p>PS Invocation Count UDW</p> <p>Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice3. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.</p>
	31:0	<p>PS Invocation Count LDW</p> <p>Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice3. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.</p>

PTBR_PAGE_POOL_OOM_EVENT_REGISTER

PTBR_PAGE_POOL_OOM_EVENT_REGISTER		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PositionCS	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	1A5A4h	
Name:	Register Template Address	
ShortName:	ADDR_SHORT_NAME	
Indicates the number of times the POSH pipe has encountered Out of Memory at any given point of time.. This register is engine context save/restored.		
DWord	Bit	Description
0	31:17	Reserved
		Default Value: 000000000000000b
		Access: RO

PTBR Page Pool Size on Out Of Memory

PTBR_PAGE_POOL_SIZE_ON_OOM_REGISTER		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PositionCS	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	18594h	
Name:	Register Template Address	
ShortName:	PTBR_PAGE_POOL_SIZE_ON_OOM_REGISTER	
Indicates the PTBR_PAGE_POOL_SIZE when POSH pipe has encountered out of memory. This register is engine context save/restored.		
DWord	Bit	Description
0	31:17	Reserved
		Default Value: 000000000000000b
		Access: RO

PTE SW Fault Repair High

PTESWC_H - PTE SW Fault Repair High						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04104h					
DWord	Bit	Description				
0	31:0	<p>PTE SW Fault Repair High</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Fixed PTE entry is written by SW here.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

PTE SW Fault Repair Low

PTESWC_L - PTE SW Fault Repair Low						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04100h					
DWord	Bit	Description				
0	31:0	<p>PTE SW Fault Repair Low</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Fixed PTE entry is written by SW here.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

Punit to Gunit Message

P2GMESSAGE - Punit to Gunit Message			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	1300A8h		
This register is used for messaging communication between Punit and Gunit.			
DWord	Bit	Description	
0	31:16	P2GMSGMSK	
		Default Value:	0000h
		Access:	RO
Mask bits for lower 16 bits to avoid a read/modify write if '0' the corresponding bit in [15:0] is not changed if '1' the corresponding bit in [15:0] is changed to the value in [15:0]			
15		Punit to Gunit Ack for (EU/SS) resource profile change	
		Default Value:	0b
		Access:	WO
<p>New for CHV, BSW.</p> <p>Punit sends an ack to proceed with changing the EU/SS requested by CS.</p> <p>This is self clearing bit. Both this bit and bit 31 should be '1' and byte enables should be set for writing into this bit.</p> <p>Once written, ack will stay high for one czclk wide and self clears. Reads will always return '0'. Other bits that are involved in the flow are A11C[28] and A11C[27].Sequencing.</p> <ol style="list-style-type: none"> 1) CS sends (EU/SS) resource request to GPM. 2) GPM writes to offset 0xDA in Punit config space showing what the intended new configuration will be, when config bit allows. 3) Punit has opportunity to do whatever is needed, but can not wait for CPDack as it will result in a hang. 4) Based on a config unit setting, GPM will wait for an acknowledge from Punit. By default, GPM does not wait for ack due to large latency. 5) GPM continues to change the (EU/SS) resource profile. 6) GPM replies to CS with the new resource profile. 7) Execute the workload or arbitrate CPD. 			
14:1		P2G_MSG_RSVD	
		Default Value:	0000h
		Access:	R/W
P2GMSGReserved			

P2GMESSAGE - Punit to Gunit Message

0	P2GMSG0 Default Value: 0b Access: R/W	
	<p>Context restore. this bit is used as part of the hardware context restore process.</p> <p>Step1: Punit writes '1(with mask bit 16 set) to initiate the HW context restore(for registers driver would normally restore)</p> <p>Step2: Gunit goes through context restore.</p> <p>Step3: Gunit writes a 1 to Punit register DB[0] indicating context restore has completed.</p> <p>This bit is cleared automatically when Gunit is powered down. Punit must do the same.</p> <p>The specific usage of this bit limits it to only be set once, for initial context restore request after an s0ix exit. Any subsequent write is undefined.</p>	

PWRCTXSAVE Message Register for Power Management Unit

MSG_PWRCTXSAVE_GPM - PWRCTXSAVE Message Register for Power Management Unit

Register Space: MMIO: 0/2/0

Project: CHV, BSW

Source: PRM

Default Value: 0x00000000

Size (in bits): 16

Address: 08044h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	15:10	Reserved
		Access: RO
	9	Power Context Save Request Access: R/W Power Context Save Request 1'b0 : Power context save is not being requested <default> 1'b1 : Power context save is being requested Unit needs to self-clear this bit upon sampling.
8:0	QWord Credits for Power Context Save Request	
	Access: R/W QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTXSAVE_REQ (Bit9).	

PWRMTR_WT1_EEVT1TO4

PWRMTR_WT1_EEVT1TO4 - PWRMTR_WT1_EEVT1TO4			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A850h		
PWRMTR_WT1_EEVT1to4			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_EU_TH_EVT4	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_EU_TH_EVT4 This event measured by this field can be overwritten by AACC[3].	
	23:16	PWRMTR_WT1_EU_GA_EVT3	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_EU_GA_EVT3 This event measured by this field can be overwritten by AACC[2].	
	15:8	PWRMTR_WT1_EU_GA_EVT2	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_EU_GA_EVT2 This event measured by this field can be overwritten by AACC[1].	
	7:0	PWRMTR_WT1_EU_GA_EVT1	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_EU_GA_EVT1 This event measured by this field can be overwritten by AACC[0].	

PWRMTR_WT1_EEVT5TO8

PWRMTR_WT1_EEVT5TO8 - PWRMTR_WT1_EEVT5TO8			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A854h		
PWRMTR_WT1_EEVT5to8			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_E0_HP_EVT8	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E0_HP_EVT8 This event measured by this field can be overwritten by AACC[7].	
	23:16	PWRMTR_WT1_E0_HP_EVT7	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E0_HP_EVT7 This event measured by this field can be overwritten by AACC[6].	
	15:8	PWRMTR_WT1_E0_HP_EVT6	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E0_HP_EVT6 This event measured by this field can be overwritten by AACC[5].	
	7:0	PWRMTR_WT1_EU_IO_EVT5	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_EU_IO_EVT5 This event measured by this field can be overwritten by AACC[4].	

PWRMTR_WT1_EEVT9TO12

PWRMTR_WT1_EEVT9TO12 - PWRMTR_WT1_EEVT9TO12			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A858h		
PWRMTR_WT1_EEVT9to12			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_E0_SP_EVT12	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E0_SP_EVT12 This event measured by this field can be overwritten by AACC[11].	
	23:16	PWRMTR_WT1_E0_SP_EVT11	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E0_SP_EVT11 This event measured by this field can be overwritten by AACC[10].	
	15:8	PWRMTR_WT1_E0_SP_EVT10	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E0_SP_EVT10 This event measured by this field can be overwritten by AACC[9].	
	7:0	PWRMTR_WT1_E0_HP_EVT9	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E0_HP_EVT9 This event measured by this field can be overwritten by AACC[8].	

PWRMTR_WT1_EEVT13TO16

PWRMTR_WT1_EEVT13TO16 - PWRMTR_WT1_EEVT13TO16		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A85Ch	
PWRMTR_WT1_EEVT13to16		
DWord	Bit	Description
0	31:24	PWRMTR_WT1_E0_DP_EVT16
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E0_DP_EVT16 This event measured by this field can be overwritten by AACC[15].
Programming Notes		
Must be 0 at all times.		
	23:16	PWRMTR_WT1_E0_DP_EVT15
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E0_DP_EVT15 This event measured by this field can be overwritten by AACC[14].
Programming Notes		
Must be 0 at all times.		
	15:8	PWRMTR_WT1_E0_DP_EVT14
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E0_DP_EVT14 This event measured by this field can be overwritten by AACC[13].
Programming Notes		
Must be 0 at all times.		
	7:0	PWRMTR_WT1_E0_SP_EVT13
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E0_SP_EVT13 This event measured by this field can be overwritten by AACC[12].

PWRMTR_WT1_EEVT17TO20

PWRMTR_WT1_EEVT17TO20 - PWRMTR_WT1_EEVT17TO20			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A860h		
PWRMTR_WT1_EEVT17to20			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_E0INT_EVT20	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E0INT_EVT20 This event measured by this field can be overwritten by AACC[19].	
	23:16	PWRMTR_WT1_E0INT_EVT19	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E0INT_EVT19 This event measured by this field can be overwritten by AACC[18].	
		Programming Notes	
	Must be 0 at all times.		
	15:8	PWRMTR_WT1_E0INT_EVT18	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E0INT_EVT18 This event measured by this field can be overwritten by AACC[17].	
	7:0	PWRMTR_WT1_E0_DP_EVT17	
		Default Value:	00h
Access:		R/W Lock	
PWRMTR_WT1_E0_DP_EVT17 This event measured by this field can be overwritten by AACC[16].			
Programming Notes			
Must be 0 at all times.			

PWRMTR_WT1_EEVT21TO24

PWRMTR_WT1_EEVT21TO24 - PWRMTR_WT1_EEVT21TO24		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A864h	
PWRMTR_WT1_EEVT21to24		
DWord	Bit	Description
0	31:24	PWRMTR_WT1_E0_QP_EVT24
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E0_QP_EVT24 This event measured by this field can be overwritten by AACCC[23].
Programming Notes		
Must be 0 at all times.		
	23:16	PWRMTR_WT1_E0_QP_EVT23
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E0_QP_EVT23 This event measured by this field can be overwritten by AACCC[22].
Programming Notes		
Must be 0 at all times.		
	15:8	PWRMTR_WT1_E0_QP_EVT22
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E0_QP_EVT22 This event measured by this field can be overwritten by AACCC[21].
	7:0	PWRMTR_WT1_E0INT_EVT21
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E0INT_EVT21 This event measured by this field can be overwritten by AACCC[20].

PWRMTR_WT1_EEVT25TO28

PWRMTR_WT1_EEVT25TO28 - PWRMTR_WT1_EEVT25TO28		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A868h	
PWRMTR_WT1_EEVT25to28		
DWord	Bit	Description
0	31:24	PWRMTR_WT1_EFPU0_EVT28
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_EFPU0_EVT28 This event measured by this field can be overwritten by AACC[27].
23:16		PWRMTR_WT1_EFPU0_EVT27
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_EFPU0_EVT27 This event measured by this field can be overwritten by AACC[26].
15:8		PWRMTR_WT1_EFPU0_EVT26
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_EFPU0_EVT26 This event measured by this field can be overwritten by AACC[25].
7:0		PWRMTR_WT1_E0_QP_EVT25
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E0_QP_EVT25 This event measured by this field can be overwritten by AACC[24].
Programming Notes		
Must be 0 at all times.		

PWRMTR_WT1_EEVT29TO32

PWRMTR_WT1_EEVT29TO32 - PWRMTR_WT1_EEVT29TO32			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A86Ch		
PWRMTR_WT1_EEVT29to32			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_E1_HP_EVT32	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E1_HP_EVT32 This event measured by this field can be overwritten by AACC[31].	
	23:16	PWRMTR_WT1_E1_HP_EVT31	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E1_HP_EVT31 This event measured by this field can be overwritten by AACC[30].	
	15:8	PWRMTR_WT1_E1_HP_EVT30	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E1_HP_EVT30 This event measured by this field can be overwritten by AACC[29].	
	7:0	PWRMTR_WT1_EFPU0_EVT29	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_EFPU0_EVT29 This event measured by this field can be overwritten by AACC[28].	

PWRMTR_WT1_EEVT33TO36

PWRMTR_WT1_EEVT33TO36 - PWRMTR_WT1_EEVT33TO36			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A870h		
PWRMTR_WT1_EEVT33to36			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_E1_SP_EVT36	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E1_SP_EVT36 This event measured by this field can be overwritten by AAD0[3].	
	23:16	PWRMTR_WT1_E1_SP_EVT35	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E1_SP_EVT35 This event measured by this field can be overwritten by AAD0[2].	
	15:8	PWRMTR_WT1_E1_SP_EVT34	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E1_SP_EVT34 This event measured by this field can be overwritten by AAD0[1].	
	7:0	PWRMTR_WT1_E1_HP_EVT33	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E1_HP_EVT33 This event measured by this field can be overwritten by AAD0[0].	

PWRMTR_WT1_EEVT37TO40

PWRMTR_WT1_EEVT37TO40 - PWRMTR_WT1_EEVT37TO40			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A874h		
PWRMTR_WT1_EEVT37to40			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_E1_DP_EVT40	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E1_DP_EVT40 This event measured by this field can be overwritten by AAD0[7].	
	23:16	PWRMTR_WT1_E1_DP_EVT39	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E1_DP_EVT39 This event measured by this field can be overwritten by AAD0[6].	
	15:8	PWRMTR_WT1_E1_DP_EVT38	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E1_DP_EVT38 This event measured by this field can be overwritten by AAD0[5].	
	7:0	PWRMTR_WT1_E1_SP_EVT37	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E1_SP_EVT37 This event measured by this field can be overwritten by AAD0[4].	

PWRMTR_WT1_EEVT41TO44

PWRMTR_WT1_EEVT41TO44 - PWRMTR_WT1_EEVT41TO44		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A878h	
PWRMTR_WT1_EEVT41to44		
DWord	Bit	Description
0	31:24	PWRMTR_WT1_E1INT_EVT44
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E1INT_EVT44 This event measured by this field can be overwritten by AAD0[11].
23:16		PWRMTR_WT1_E1INT_EVT43
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E1INT_EVT43 This event measured by this field can be overwritten by AAD0[10].
		Programming Notes
		Must be 0 at all times.
15:8		PWRMTR_WT1_E1INT_EVT42
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E1INT_EVT42 This event measured by this field can be overwritten by AAD0[9].
7:0		PWRMTR_WT1_E1_DP_EVT41
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E1_DP_EVT41 This event measured by this field can be overwritten by AAD0[8].

PWRMTR_WT1_EEVT45TO48

PWRMTR_WT1_EEVT45TO48 - PWRMTR_WT1_EEVT45TO48			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A87Ch		
PWRMTR_WT1_EEVT45to48			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_E1_QP_EVT48	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E1_QP_EVT48 This event measured by this field can be overwritten by AAD0[15].	
23:16	23:16	PWRMTR_WT1_E1_QP_EVT47	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E1_QP_EVT47 This event measured by this field can be overwritten by AAD0[14].	
		Programming Notes	
		Must be 0 at all times.	
15:8	15:8	PWRMTR_WT1_E1_QP_EVT46	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E1_QP_EVT46 This event measured by this field can be overwritten by AAD0[13].	
7:0	7:0	PWRMTR_WT1_E1INT_EVT45	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E1INT_EVT45 This event measured by this field can be overwritten by AAD0[12].	

PWRMTR_WT1_EEVT49TO52

PWRMTR_WT1_EEVT49TO52 - PWRMTR_WT1_EEVT49TO52			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A880h		
PWRMTR_WT1_EEVT49to52			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_EFPU1_EVT52	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_EFPU1_EVT52 This event measured by this field can be overwritten by AAD0[19].	
	23:16	PWRMTR_WT1_EFPU1_EVT51	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_EFPU1_EVT51 This event measured by this field can be overwritten by AAD0[18].	
	15:8	PWRMTR_WT1_EFPU1_EVT50	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_EFPU1_EVT50 This event measured by this field can be overwritten by AAD0[17].	
	7:0	PWRMTR_WT1_E1_QP_EVT49	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E1_QP_EVT49 This event measured by this field can be overwritten by AAD0[16].	

PWRMTR_WT1_EEVT53TO56

PWRMTR_WT1_EEVT53TO56 - PWRMTR_WT1_EEVT53TO56			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A884h		
PWRMTR_WT1_EEVT53to56			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_EEMEM_EVT56	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_EEMEM_EVT56 This event measured by this field can be overwritten by AAD0[23].	
	23:16	PWRMTR_WT1_EEMEM_EVT55	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_EEMEM_EVT55 This event measured by this field can be overwritten by AAD0[22].	
	15:8	PWRMTR_WT1_EEMEM_EVT54	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_EEMEM_EVT54 This event measured by this field can be overwritten by AAD0[21].	
	7:0	PWRMTR_WT1_EFPU1_EVT53	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_EFPU1_EVT53 This event measured by this field can be overwritten by AAD0[20].	

PWRMTR_WT1_EEVT57TO58

PWRMTR_WT1_EEVT57TO58 - PWRMTR_WT1_EEVT57TO58			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A888h		
PWRMTR_WT1_EEVT57to58			
DWord	Bit	Description	
0	31:16	Reserved	
		Default Value:	0000h
		Access:	RO
		Reserved	
	15:8	PWRMTR_WT1_EBUSS_EVT58	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_EBUSS_EVT58 This event measured by this field can be overwritten by AAD0[25].	
	7:0	PWRMTR_WT1_EEMEM_EVT57	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_EEMEM_EVT57 This event measured by this field can be overwritten by AAD0[24].	

PWRMTR_WT1_MEVT1TO4

PWRMTR_WT1_MEVT1TO4 - PWRMTR_WT1_MEVT1TO4			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A890h		
PWRMTR_WT1_MEVT1to4			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_MMDOI_EVT4	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDOI_EVT4 This event measured by this field can be overwritten by AAD4[3].	
	23:16	PWRMTR_WT1_MMSOI_EVT3	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMSOI_EVT3 This event measured by this field can be overwritten by AAD4[2].	
	15:8	PWRMTR_WT1_MMSOI_EVT2	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMSOI_EVT2 This event measured by this field can be overwritten by AAD4[1].	
	7:0	PWRMTR_WT1_MMSOI_EVT1	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMSOI_EVT1 This event measured by this field can be overwritten by AAD4[0].	

PWRMTR_WT1_MEVT5TO8

PWRMTR_WT1_MEVT5TO8 - PWRMTR_WT1_MEVT5TO8			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A894h		
PWRMTR_WT1_MEVT5to8			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_MMDOI_EVT8	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDOI_EVT8 This event measured by this field can be overwritten by AAD4[7].	
	23:16	PWRMTR_WT1_MMDOI_EVT7	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDOI_EVT7 This event measured by this field can be overwritten by AAD4[6].	
	15:8	PWRMTR_WT1_MMDOI_EVT6	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDOI_EVT6 This event measured by this field can be overwritten by AAD4[5].	
	7:0	PWRMTR_WT1_MMDOI_EVT5	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDOI_EVT5 This event measured by this field can be overwritten by AAD4[4].	

PWRMTR_WT1_MEVT9TO12

PWRMTR_WT1_MEVT9TO12 - PWRMTR_WT1_MEVT9TO12			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A898h		
PWRMTR_WT1_MEVT9to12			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_MMDCN_EVT12	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDCN_EVT12 This event measured by this field can be overwritten by AAD4[11].	
	23:16	PWRMTR_WT1_MMDCN_EVT11	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDCN_EVT11 This event measured by this field can be overwritten by AAD4[10].	
	15:8	PWRMTR_WT1_MMDCN_EVT10	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDCN_EVT10 This event measured by this field can be overwritten by AAD4[9].	
	7:0	PWRMTR_WT1_MMDCN_EVT9	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDCN_EVT9 This event measured by this field can be overwritten by AAD4[8].	

PWRMTR_WT1_MEVT13TO16

PWRMTR_WT1_MEVT13TO16 - PWRMTR_WT1_MEVT13TO16			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A89Ch		
PWRMTR_WT1_MEVT13to16			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_MMDCN_EVT16	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDCN_EVT16 This event measured by this field can be overwritten by AAD4[15].	
	23:16	PWRMTR_WT1_MMDCN_EVT15	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDCN_EVT15 This event measured by this field can be overwritten by AAD4[14].	
	15:8	PWRMTR_WT1_MMDCN_EVT14	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDCN_EVT14 This event measured by this field can be overwritten by AAD4[13].	
	7:0	PWRMTR_WT1_MMDCN_EVT13	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDCN_EVT13 This event measured by this field can be overwritten by AAD4[12].	

PWRMTR_WT1_MEVT17TO20

PWRMTR_WT1_MEVT17TO20 - PWRMTR_WT1_MEVT17TO20			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A8A0h		
PWRMTR_WT1_MEVT17to20			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_MMDMH_EVT20	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDMH_EVT20 This event measured by this field can be overwritten by AAD4[19].	
23:16		PWRMTR_WT1_MMDCN_EVT19	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDCN_EVT19 This event measured by this field can be overwritten by AAD4[18].	
15:8		PWRMTR_WT1_MMDCN_EVT18	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDCN_EVT18 This event measured by this field can be overwritten by AAD4[17].	
7:0		PWRMTR_WT1_MMDCN_EVT17	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDCN_EVT17 This event measured by this field can be overwritten by AAD4[16].	

PWRMTR_WT1_MEVT21TO24

PWRMTR_WT1_MEVT21TO24 - PWRMTR_WT1_MEVT21TO24			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A8A4h		
PWRMTR_WT1_MEVT21to24			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_MMDOH_EVT24	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDOH_EVT24 This event measured by this field can be overwritten by AAD4[23].	
	23:16	PWRMTR_WT1_MMDMH_EVT23	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDMH_EVT23 This event measured by this field can be overwritten by AAD4[22].	
	15:8	PWRMTR_WT1_MMDMH_EVT22	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDMH_EVT22 This event measured by this field can be overwritten by AAD4[21].	
	7:0	PWRMTR_WT1_MMDMH_EVT21	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDMH_EVT21 This event measured by this field can be overwritten by AAD4[20].	

PWRMTR_WT1_MEVT25TO28

PWRMTR_WT1_MEVT25TO28 - PWRMTR_WT1_MEVT25TO28			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A8A8h		
PWRMTR_WT1_MEVT25to28			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_MMDCN_EVT28	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDCN_EVT28 This event measured by this field can be overwritten by AAD4[27].	
23:16		PWRMTR_WT1_MMDCN_EVT27	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDCN_EVT27 This event measured by this field can be overwritten by AAD4[26].	
15:8		PWRMTR_WT1_MMDCN_EVT26	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDCN_EVT26 This event measured by this field can be overwritten by AAD4[25].	
		Programming Notes	
		Must be 0 at all times.	
Project			
CHV, BSW			
7:0		PWRMTR_WT1_MMDOH_EVT25	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDOH_EVT25 This event measured by this field can be overwritten by AAD4[24].	

PWRMTR_WT1_MEVT29TO32

PWRMTR_WT1_MEVT29TO32 - PWRMTR_WT1_MEVT29TO32			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A8ACh		
PWRMTR_WT1_MEVT29to32			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_MHECN_EVT32	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MHECN_EVT32 This event measured by this field can be overwritten by AAD4[31].	
	23:16	PWRMTR_WT1_MHECN_EVT31	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MHECN_EVT31 This event measured by this field can be overwritten by AAD4[30].	
	15:8	PWRMTR_WT1_MHECN_EVT30	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MHECN_EVT30 This event measured by this field can be overwritten by AAD4[29].	
	7:0	PWRMTR_WT1_MMDCN_EVT29	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDCN_EVT29 This event measured by this field can be overwritten by AAD4[28].	

PWRMTR_WT1_MEVT33TO36

PWRMTR_WT1_MEVT33TO36 - PWRMTR_WT1_MEVT33TO36			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A8B0h		
PWRMTR_WT1_MEVT33to36			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_MHECN_EVT36	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MHECN_EVT36 This event measured by this field can be overwritten by AAD8[3].	
	23:16	PWRMTR_WT1_MHECN_EVT35	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MHECN_EVT35 This event measured by this field can be overwritten by AAD8[2].	
	15:8	PWRMTR_WT1_MHECN_EVT34	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MHECN_EVT34 This event measured by this field can be overwritten by AAD8[1].	
	7:0	PWRMTR_WT1_MHECN_EVT33	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MHECN_EVT33 This event measured by this field can be overwritten by AAD8[0].	

PWRMTR_WT1_REVT1TO4

PWRMTR_WT1_REVT1TO4 - PWRMTR_WT1_REVT1TO4			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A800h		
PWRMTR_WT1_REVT1to4			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_RFFOI_EVT4	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RFFOI_EVT4. This event measured by this field can be overwritten by AAC0[3].	
	23:16	PWRMTR_WT1_RFFOI_EVT3	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RFFOI_EVT3. This event measured by this field can be overwritten by AAC0[2].	
	15:8	PWRMTR_WT1_RFFOI_EVT2	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RFFOI_EVT2. This event measured by this field can be overwritten by AAC0[1].	
	7:0	PWRMTR_WT1_RFFOI_EVT1	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RFFOI_EVT1. This event measured by this field can be overwritten by AAC0[0].	

PWRMTR_WT1_REVT5TO8

PWRMTR_WT1_REVT5TO8 - PWRMTR_WT1_REVT5TO8			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A804h		
PWRMTR_WT1_REVT5to8			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_RFFOI_EVT8	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RFFOI_EVT8. This event measured by this field can be overwritten by AAC0[7].	
	23:16	PWRMTR_WT1_RFFOI_EVT7	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RFFOI_EVT7. This event measured by this field can be overwritten by AAC0[6].	
	15:8	PWRMTR_WT1_RFFOI_EVT6	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RFFOI_EVT6. This event measured by this field can be overwritten by AAC0[5].	
	7:0	PWRMTR_WT1_RFFOI_EVT5	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RFFOI_EVT5. This event measured by this field can be overwritten by AAC0[4].	

PWRMTR_WT1_REVT9TO12

PWRMTR_WT1_REVT9TO12 - PWRMTR_WT1_REVT9TO12			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A808h		
PWRMTR_WT1_REVT9to12			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_RFFOI_EVT12	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RFFOI_EVT12.This event measured by this field can be overwritten by AAC0[11].	
	23:16	PWRMTR_WT1_RFFOI_EVT11	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RFFOI_EVT11.This event measured by this field can be overwritten by AAC0[10].	
	15:8	PWRMTR_WT1_RFFOI_EVT10	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RFFOI_EVT10. This event measured by this field can be overwritten by AAC0[9].	
	7:0	PWRMTR_WT1_RFFOI_EVT9	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RFFOI_EVT9.This event measured by this field can be overwritten by AAC0[8].	

PWRMTR_WT1_REVT13TO16

PWRMTR_WT1_REVT13TO16 - PWRMTR_WT1_REVT13TO16						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0A80Ch					
PWRMTR_WT1_REVT13to16						
DWord	Bit	Description				
0	31:24	PWRMTR_WT1_RFFCN_EVT16				
		Default Value: 00h				
		Access: R/W Lock				
		PWRMTR_WT1_RFFCN_EVT16.This event measured by this field can be overwritten by AAC0[15].				
		<table border="1"> <thead> <tr> <th>Programming Notes</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>Must be 0 at all times.</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Programming Notes	Project	Must be 0 at all times.	CHV, BSW
Programming Notes	Project					
Must be 0 at all times.	CHV, BSW					
	23:16	PWRMTR_WT1_RFFCN_EVT15				
		Default Value: 00h				
		Access: R/W Lock				
		PWRMTR_WT1_RFFCN_EVT15. This event measured by this field can be overwritten by AAC0[14].				
	15:8	PWRMTR_WT1_RFFOI_EVT14				
		Default Value: 00h				
		Access: R/W Lock				
		PWRMTR_WT1_RFFOI_EVT14.This event measured by this field can be overwritten by AAC0[13].				
	7:0	PWRMTR_WT1_RFFOI_EVT13				
		Default Value: 00h				
		Access: R/W Lock				
		PWRMTR_WT1_RFFOI_EVT13.This event measured by this field can be overwritten by AAC0[12].				

PWRMTR_WT1_REVT17TO20

PWRMTR_WT1_REVT17TO20 - PWRMTR_WT1_REVT17TO20				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A810h			
PWRMTR_WT1_REVT17to20				
DWord	Bit	Description		
0	31:24	PWRMTR_WT1_RFFCN_EVT20		
		Default Value:	00h	
		Access:	R/W Lock	
		PWRMTR_WT1_RFFCN_EVT20. This event measured by this field can be overwritten by AAC0[19].		
	23:16	PWRMTR_WT1_RFFCN_EVT19		
		Default Value:	00h	
		Access:	R/W Lock	
		PWRMTR_WT1_RFFCN_EVT19 This event measured by this field can be overwritten by AAC0[18].		
	15:8	PWRMTR_WT1_RFFCN_EVT18		
		Default Value:	00h	
		Access:	R/W Lock	
		PWRMTR_WT1_RFFCN_EVT18 This event measured by this field can be overwritten by AAC0[17].		
	7:0	PWRMTR_WT1_RFFCN_EVT17	Default Value:	00h
			Access:	R/W Lock
			PWRMTR_WT1_RFFCN_EVT17 This event measured by this field can be overwritten by AAC0[16].	
			Programming Notes	
Must be 0 at all times.				
Project				
CHV, BSW				

PWRMTR_WT1_REVT21TO24

PWRMTR_WT1_REVT21TO24 - PWRMTR_WT1_REVT21TO24			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A814h		
PWRMTR_WT1_REVT21to24			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_RSCOI_EVT24	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RSCOI_EVT24 This event measured by this field can be overwritten by AAC0[23].	
	23:16	PWRMTR_WT1_RSCOI_EVT23	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RSCOI_EVT23 This event measured by this field can be overwritten by AAC0[22].	
	15:8	PWRMTR_WT1_RSCOI_EVT22	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RSCOI_EVT22 This event measured by this field can be overwritten by AAC0[21].	
	7:0	PWRMTR_WT1_RSCOI_EVT21	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RSCOI_EVT21 This event measured by this field can be overwritten by AAC0[20].	

PWRMTR_WT1_REVT25TO28

PWRMTR_WT1_REVT25TO28 - PWRMTR_WT1_REVT25TO28			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A818h		
PWRMTR_WT1_REVT25to28			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_RSCOI_EVT28	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RSCOI_EVT28 This event measured by this field can be overwritten by AAC0[27].	
	23:16	PWRMTR_WT1_RSCOI_EVT27	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RSCOI_EVT27 This event measured by this field can be overwritten by AAC0[26].	
	15:8	PWRMTR_WT1_RSCOI_EVT26	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RSCOI_EVT26 This event measured by this field can be overwritten by AAC0[25].	
	7:0	PWRMTR_WT1_RSCOI_EVT25	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RSCOI_EVT25 This event measured by this field can be overwritten by AAC0[24].	

PWRMTR_WT1_REVT29TO32

PWRMTR_WT1_REVT29TO32 - PWRMTR_WT1_REVT29TO32			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A81Ch		
PWRMTR_WT1_REVT29to32			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_RSCOI_EVT32	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RSCOI_EVT32 This event measured by this field can be overwritten by AAC0[31].	
	23:16	PWRMTR_WT1_RSCOI_EVT31	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RSCOI_EVT31 This event measured by this field can be overwritten by AAC0[30].	
	15:8	PWRMTR_WT1_RSCOI_EVT30	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RSCOI_EVT30 This event measured by this field can be overwritten by AAC0[29].	
	7:0	PWRMTR_WT1_RSCOI_EVT29	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RSCOI_EVT29 This event measured by this field can be overwritten by AAC0[28].	

PWRMTR_WT1_REVT33TO36

PWRMTR_WT1_REVT33TO36 - PWRMTR_WT1_REVT33TO36			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A820h		
PWRMTR_WT1_REVT33to36			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_RL3MI_EVT36	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RL3MI_EVT36 This event measured by this field can be overwritten by AAC4[3].	
	23:16	PWRMTR_WT1_RL3CN_EVT35	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RL3CN_EVT35 This event measured by this field can be overwritten by AAC4[2].	
	15:8	PWRMTR_WT1_RSCCN_EVT34	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RSCCN_EVT34 This event measured by this field can be overwritten by AAC4[1].	
	7:0	PWRMTR_WT1_RSCOI_EVT33	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RSCOI_EVT33 This event measured by this field can be overwritten by AAC4[0].	

PWRMTR_WT1_REVT37TO40

PWRMTR_WT1_REVT37TO40 - PWRMTR_WT1_REVT37TO40			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A824h		
PWRMTR_WT1_REVT37to40			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_RTAOI_EVT40	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTAOI_EVT40 This event measured by this field can be overwritten by AAC4[7].	
	23:16	PWRMTR_WT1_RL3MI_EVT39	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RL3MI_EVT39 This event measured by this field can be overwritten by AAC4[6].	
	15:8	PWRMTR_WT1_RL3MI_EVT38	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RL3MI_EVT38 This event measured by this field can be overwritten by AAC4[5].	
7:0	PWRMTR_WT1_RL3MI_EVT37		
	Default Value:	00h	
	Access:	R/W Lock	
	PWRMTR_WT1_RL3MI_EVT37 This event measured by this field can be overwritten by AAC4[4].		

PWRMTR_WT1_REVT41TO44

PWRMTR_WT1_REVT41TO44 - PWRMTR_WT1_REVT41TO44			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A828h		
PWRMTR_WT1_REVT41to44			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_RTAOI_EVT44	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTAOI_EVT44 This event measured by this field can be overwritten by AAC4[11].	
	23:16	PWRMTR_WT1_RTAOI_EVT43	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTAOI_EVT43 This event measured by this field can be overwritten by AAC4[10].	
	15:8	PWRMTR_WT1_RTAOI_EVT42	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTAOI_EVT42 This event measured by this field can be overwritten by AAC4[9].	
	7:0	PWRMTR_WT1_RTAOI_EVT41	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTAOI_EVT41 This event measured by this field can be overwritten by AAC4[8].	

PWRMTR_WT1_REVT45TO48

PWRMTR_WT1_REVT45TO48 - PWRMTR_WT1_REVT45TO48			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A82Ch		
PWRMTR_WT1_REVT45to48			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_RTAOI_EVT48	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTAOI_EVT48 This event measured by this field can be overwritten by AAC4[15].	
	23:16	PWRMTR_WT1_RTAOI_EVT47	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTAOI_EVT47 This event measured by this field can be overwritten by AAC4[14].	
	15:8	PWRMTR_WT1_RTAOI_EVT46	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTAOI_EVT46 This event measured by this field can be overwritten by AAC4[13].	
	7:0	PWRMTR_WT1_RTAOI_EVT45	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTAOI_EVT45 This event measured by this field can be overwritten by AAC4[12].	

PWRMTR_WT1_REVT49TO52

PWRMTR_WT1_REVT49TO52 - PWRMTR_WT1_REVT49TO52			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A830h		
PWRMTR_WT1_REVT49to52			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_RTAOH_EVT52	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTAOH_EVT52 This event measured by this field can be overwritten by AAC4[19].	
	23:16	PWRMTR_WT1_RTAOH_EVT51	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTAOH_EVT51 This event measured by this field can be overwritten by AAC4[18].	
	15:8	PWRMTR_WT1_RTAOI_EVT50	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTAOI_EVT50 This event measured by this field can be overwritten by AAC4[17].	
	7:0	PWRMTR_WT1_RTAOI_EVT49	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTAOI_EVT49 This event measured by this field can be overwritten by AAC4[16].	

PWRMTR_WT1_REVT53TO56

PWRMTR_WT1_REVT53TO56 - PWRMTR_WT1_REVT53TO56			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A834h		
PWRMTR_WT1_REVT53to56			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_RTSOI_EVT56	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTSOI_EVT56 This event measured by this field can be overwritten by AAC4[23].	
	23:16	PWRMTR_WT1_RTACN_EVT55	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTACN_EVT55 This event measured by this field can be overwritten by AAC4[22].	
	15:8	PWRMTR_WT1_RTACN_EVT54	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTACN_EVT54 This event measured by this field can be overwritten by AAC4[21].	
	7:0	PWRMTR_WT1_RTACN_EVT53	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTACN_EVT53 This event measured by this field can be overwritten by AAC4[20].	

PWRMTR_WT1_REVT57TO60

PWRMTR_WT1_REVT57TO60 - PWRMTR_WT1_REVT57TO60			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A838h		
PWRMTR_WT1_REVT57to60			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_RTSOI_EVT60	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTS OI_EVT60 This event measured by this field can be overwritten by AAC4[27].	
	23:16	PWRMTR_WT1_RTSOI_EVT59	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTS OI_EVT59 This event measured by this field can be overwritten by AAC4[26].	
	15:8	PWRMTR_WT1_RTSOI_EVT58	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTS OI_EVT58 This event measured by this field can be overwritten by AAC4[25].	
Programming Notes			
Must be set to zero at all times.			
7:0	PWRMTR_WT1_RTSOI_EVT57		
	Default Value:	00h	
	Access:	R/W Lock	
	PWRMTR_WT1_RTS OI_EVT57 This event measured by this field can be overwritten by AAC4[24].		
	Programming Notes		
	Must be set to zero at all times.		

PWRMTR_WT1_REVT61TO64

PWRMTR_WT1_REVT61TO64 - PWRMTR_WT1_REVT61TO64			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A83Ch		
PWRMTR_WT1_REVT61to64			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_RTOOI_EVT64	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTOOI_EVT64 This event measured by this field can be overwritten by AAC4[31].	
	23:16	PWRMTR_WT1_RTOOI_EVT63	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTOOI_EVT63 This event measured by this field can be overwritten by AAC4[30].	
	15:8	PWRMTR_WT1_RTOOI_EVT62	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTOOI_EVT62 This event measured by this field can be overwritten by AAC4[29].	
	7:0	PWRMTR_WT1_RTOOI_EVT61	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTOOI_EVT61 This event measured by this field can be overwritten by AAC4[28].	

PWRMTR_WT1_REVT65TO68

PWRMTR_WT1_REVT65TO68 - PWRMTR_WT1_REVT65TO68			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A840h		
PWRMTR_WT1_REVT65to68			
DWord	Bit	Description	
0	31:24	PWRMTR_WT1_RGTCN_EVT68	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RGTCN_EVT68 This event measured by this field can be overwritten by AAC8[3].	
	23:16	PWRMTR_WT1_RGTCN_EVT67	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RGTCN_EVT67 This event measured by this field can be overwritten by AAC8[2].	
	15:8	PWRMTR_WT1_RGTCN_EVT66	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RGTCN_EVT66 This event measured by this field can be overwritten by AAC8[1].	
	7:0	PWRMTR_WT1_RGTOI_EVT65	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RGTOI_EVT65 This event measured by this field can be overwritten by AAC8[0].	

PWRMTR_WT1_REVT69TO70

PWRMTR_WT1_REVT69TO70 - PWRMTR_WT1_REVT69TO70			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A844h		
PWRMTR_WT1_REVT69to70			
DWord	Bit	Description	
0	31:16	Reserved	
		Default Value:	0000h
		Access:	RO
		Reserved	
		15:8	PWRMTR_WT1_RGTCN_EVT70
			Default Value:
	Access:		R/W Lock
	PWRMTR_WT1_RGTCN_EVT70 This event measured by this field can be overwritten by AAC8[5].		
	7:0		PWRMTR_WT1_RGTCN_EVT69
			Default Value:
		Access:	R/W Lock
		PWRMTR_WT1_RGTCN_EVT69 This event measured by this field can be overwritten by AAC8[4].	

PWRMTR_WT2_EEVT1TO4

PWRMTR_WT2_EEVT1TO4 - PWRMTR_WT2_EEVT1TO4			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A950h		
PWRMTR_WT2_EEVT1to4			
DWord	Bit	Description	
0	31:24	PWRMTR_WT2_EU_TH_EVT4	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_EU_TH_EVT4 This event measured by this field can be overwritten by AACC[3].	
	23:16	PWRMTR_WT2_EU_GA_EVT3	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_EU_GA_EVT3 This event measured by this field can be overwritten by AACC[2].	
	15:8	PWRMTR_WT2_EU_GA_EVT2	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_EU_GA_EVT2 This event measured by this field can be overwritten by AACC[1].	
	7:0	PWRMTR_WT2_EU_GA_EVT1	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_EU_GA_EVT1 This event measured by this field can be overwritten by AACC[0].	

PWRMTR_WT2_EEVT5TO8

PWRMTR_WT2_EEVT5TO8 - PWRMTR_WT2_EEVT5TO8			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A954h		
PWRMTR_WT2_EEVT5to8			
DWord	Bit	Description	
0	31:24	PWRMTR_WT2_E0_HP_EVT8	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E0_HP_EVT8 This event measured by this field can be overwritten by AACC[7].	
	23:16	PWRMTR_WT2_E0_HP_EVT7	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E0_HP_EVT7 This event measured by this field can be overwritten by AACC[6].	
	15:8	PWRMTR_WT2_E0_HP_EVT6	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E0_HP_EVT6 This event measured by this field can be overwritten by AACC[5].	
	7:0	PWRMTR_WT2_EU_IO_EVT5	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_EU_IO_EVT5 This event measured by this field can be overwritten by AACC[4].	

PWRMTR_WT2_EEVT9TO12

PWRMTR_WT2_EEVT9TO12 - PWRMTR_WT2_EEVT9TO12			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A958h		
PWRMTR_WT2_EEVT9to12			
DWord	Bit	Description	
0	31:24	PWRMTR_WT2_E0_SP_EVT12	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E0_SP_EVT12 This event measured by this field can be overwritten by AACC[11].	
	23:16	PWRMTR_WT2_E0_SP_EVT11	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E0_SP_EVT11 This event measured by this field can be overwritten by AACC[10].	
	15:8	PWRMTR_WT2_E0_SP_EVT10	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E0_SP_EVT10 This event measured by this field can be overwritten by AACC[9].	
	7:0	PWRMTR_WT2_E0_HP_EVT9	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E0_HP_EVT9 This event measured by this field can be overwritten by AACC[8].	

PWRMTR_WT2_EEVT13TO16

PWRMTR_WT2_EEVT13TO16 - PWRMTR_WT2_EEVT13TO16		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A95Ch	
PWRMTR_WT2_EEVT13to16		
DWord	Bit	Description
0	31:24	PWRMTR_WT2_E0_DP_EVT16
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_E0_DP_EVT16 This event measured by this field can be overwritten by AACC[15].
Programming Notes		
Must be 0 at all times.		
	23:16	PWRMTR_WT2_E0_DP_EVT15
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_E0_DP_EVT15 This event measured by this field can be overwritten by AACC[14].
Programming Notes		
Must be 0 at all times.		
	15:8	PWRMTR_WT2_E0_DP_EVT14
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_E0_DP_EVT14 This event measured by this field can be overwritten by AACC[13].
Programming Notes		
Must be 0 at all times.		
	7:0	PWRMTR_WT2_E0_SP_EVT13
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_E0_SP_EVT13 This event measured by this field can be overwritten by AACC[12].

PWRMTR_WT2_EEVT17TO20

PWRMTR_WT2_EEVT17TO20 - PWRMTR_WT2_EEVT17TO20			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A960h		
PWRMTR_WT2_EEVT17to20			
DWord	Bit	Description	
0	31:24	PWRMTR_WT2_E0INT_EVT20	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E0INT_EVT20 This event measured by this field can be overwritten by AACC[19].	
	23:16	PWRMTR_WT2_E0INT_EVT19	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E0INT_EVT19 This event measured by this field can be overwritten by AACC[18].	
		Programming Notes	
	Must be 0 at all times.		
	15:8	PWRMTR_WT2_E0INT_EVT18	
		Default Value:	00h
Access:		R/W Lock	
PWRMTR_WT2_E0INT_EVT18 This event measured by this field can be overwritten by AACC[17].			
7:0	PWRMTR_WT2_E0_DP_EVT17		
	Default Value:	00h	
	Access:	R/W Lock	
	PWRMTR_WT2_E0_DP_EVT17 This event measured by this field can be overwritten by AACC[16].		
	Programming Notes		
Must be 0 at all times.			

PWRMTR_WT2_EEVT21TO24

PWRMTR_WT2_EEVT21TO24 - PWRMTR_WT2_EEVT21TO24			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A964h		
PWRMTR_WT2_EEVT21to24			
DWord	Bit	Description	
0	31:24	PWRMTR_WT2_E0_QP_EVT24	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E0_QP_EVT24 This event measured by this field can be overwritten by AACC[23].	
		Programming Notes	
		Must be 0 at all times.	
	23:16	PWRMTR_WT2_E0_QP_EVT23	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E0_QP_EVT23 This event measured by this field can be overwritten by AACC[22].	
		Programming Notes	
		Must be 0 at all times.	
	15:8	PWRMTR_WT2_E0_QP_EVT22	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E0_QP_EVT22 This event measured by this field can be overwritten by AACC[21].	
	7:0	PWRMTR_WT2_E0INT_EVT21	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E0INT_EVT21 This event measured by this field can be overwritten by AACC[20].	

PWRMTR_WT2_EEVT25TO28

PWRMTR_WT2_EEVT25TO28 - PWRMTR_WT2_EEVT25TO28		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A968h	
PWRMTR_WT2_EEVT25to28		
DWord	Bit	Description
0	31:24	PWRMTR_WT2_EFPU0_EVT28
		Default Value: 00h
	Access: R/W Lock	
	PWRMTR_WT2_EFPU0_EVT28 This event measured by this field can be overwritten by AACC[27].	
23:16	PWRMTR_WT2_EFPU0_EVT27	
	Default Value: 00h	
Access: R/W Lock		
PWRMTR_WT2_EFPU0_EVT27 This event measured by this field can be overwritten by AACC[26].		
15:8	PWRMTR_WT2_EFPU0_EVT26	
	Default Value: 00h	
Access: R/W Lock		
PWRMTR_WT2_EFPU0_EVT26 This event measured by this field can be overwritten by AACC[25].		
7:0	PWRMTR_WT2_E0_QP_EVT25	
	Default Value: 00h	
Access: R/W Lock		
PWRMTR_WT2_E0_QP_EVT25 This event measured by this field can be overwritten by AACC[24].		
Programming Notes		
Must be 0 at all times.		

PWRMTR_WT2_EEVT29TO32

PWRMTR_WT2_EEVT29TO32 - PWRMTR_WT2_EEVT29TO32			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A96Ch		
PWRMTR_WT2_EEVT29to32			
DWord	Bit	Description	
0	31:24	PWRMTR_WT2_E1_HP_EVT32	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E1_HP_EVT32 This event measured by this field can be overwritten by AACC[31].	
	23:16	PWRMTR_WT2_E1_HP_EVT31	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E1_HP_EVT31 This event measured by this field can be overwritten by AACC[30].	
	15:8	PWRMTR_WT2_E1_HP_EVT30	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E1_HP_EVT30 This event measured by this field can be overwritten by AACC[29].	
	7:0	PWRMTR_WT2_EFPU0_EVT29	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_EFPU0_EVT29 This event measured by this field can be overwritten by AACC[28].	

PWRMTR_WT2_EEVT33TO36

PWRMTR_WT2_EEVT33TO36 - PWRMTR_WT2_EEVT33TO36			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A970h		
PWRMTR_WT2_EEVT33to36			
DWord	Bit	Description	
0	31:24	PWRMTR_WT2_E1_SP_EVT36	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E1_SP_EVT36 This event measured by this field can be overwritten by AAD0[3].	
	23:16	PWRMTR_WT2_E1_SP_EVT35	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E1_SP_EVT35 This event measured by this field can be overwritten by AAD0[2].	
	15:8	PWRMTR_WT2_E1_SP_EVT34	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E1_SP_EVT34 This event measured by this field can be overwritten by AAD0[1].	
	7:0	PWRMTR_WT2_E1_HP_EVT33	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E1_HP_EVT33 This event measured by this field can be overwritten by AAD0[0].	

PWRMTR_WT2_EEVT37TO40

PWRMTR_WT2_EEVT37TO40 - PWRMTR_WT2_EEVT37TO40			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A974h		
PWRMTR_WT2_EEVT37to40			
DWord	Bit	Description	
0	31:24	PWRMTR_WT2_E1_DP_EVT40	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E1_DP_EVT40 This event measured by this field can be overwritten by AAD0[7].	
	23:16	PWRMTR_WT2_E1_DP_EVT39	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E1_DP_EVT39 This event measured by this field can be overwritten by AAD0[6].	
	15:8	PWRMTR_WT2_E1_DP_EVT38	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E1_DP_EVT38 This event measured by this field can be overwritten by AAD0[5].	
	7:0	PWRMTR_WT2_E1_SP_EVT37	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E1_SP_EVT37 This event measured by this field can be overwritten by AAD0[4].	

PWRMTR_WT2_EEVT41TO44

PWRMTR_WT2_EEVT41TO44 - PWRMTR_WT2_EEVT41TO44				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A978h			
PWRMTR_WT2_EEVT41to44				
DWord	Bit	Description		
0	31:24	PWRMTR_WT2_E1INT_EVT44		
		Default Value:	00h	
		Access:	R/W Lock	
		PWRMTR_WT2_E1INT_EVT44 This event measured by this field can be overwritten by AAD0[11].		
	23:16	PWRMTR_WT2_E1INT_EVT43	Default Value:	00h
			Access:	R/W Lock
			PWRMTR_WT2_E1INT_EVT43 This event measured by this field can be overwritten by AAD0[10].	
			Programming Notes	
		Must be 0 at all times.		
	15:8	PWRMTR_WT2_E1INT_EVT42	Default Value:	00h
			Access:	R/W Lock
			PWRMTR_WT2_E1INT_EVT42 This event measured by this field can be overwritten by AAD0[9].	
	7:0	PWRMTR_WT2_E1_DP_EVT41	Default Value:	00h
			Access:	R/W Lock
			PWRMTR_WT2_E1_DP_EVT41 This event measured by this field can be overwritten by AAD0[8].	

PWRMTR_WT2_EEVT45TO48

PWRMTR_WT2_EEVT45TO48 - PWRMTR_WT2_EEVT45TO48		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A97Ch	
PWRMTR_WT2_EEVT45to48		
DWord	Bit	Description
0	31:24	PWRMTR_WT2_E1_QP_EVT48
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_E1_QP_EVT48 This event measured by this field can be overwritten by AAD0[15].
23:16		PWRMTR_WT2_E1_QP_EVT47
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_E1_QP_EVT47 This event measured by this field can be overwritten by AAD0[14].
Programming Notes		
Must be 0 at all times.		
15:8		PWRMTR_WT2_E1_QP_EVT46
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_E1_QP_EVT46 This event measured by this field can be overwritten by AAD0[13].
7:0		PWRMTR_WT2_E1INT_EVT45
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_E1INT_EVT45 This event measured by this field can be overwritten by AAD0[12].

PWRMTR_WT2_EEVT49TO52

PWRMTR_WT2_EEVT49TO52 - PWRMTR_WT2_EEVT49TO52			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A980h		
PWRMTR_WT2_EEVT49to52			
DWord	Bit	Description	
0	31:24	PWRMTR_WT2_EFPU1_EVT52	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_EFPU1_EVT52 This event measured by this field can be overwritten by AAD0[19].	
	23:16	PWRMTR_WT2_EFPU1_EVT51	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_EFPU1_EVT51 This event measured by this field can be overwritten by AAD0[18].	
	15:8	PWRMTR_WT2_EFPU1_EVT50	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_EFPU1_EVT50 This event measured by this field can be overwritten by AAD0[17].	
	7:0	PWRMTR_WT2_E1_QP_EVT49	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E1_QP_EVT49 This event measured by this field can be overwritten by AAD0[16].	

PWRMTR_WT2_EEVT53TO56

PWRMTR_WT2_EEVT53TO56 - PWRMTR_WT2_EEVT53TO56			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A984h		
PWRMTR_WT2_EEVT53to56			
DWord	Bit	Description	
0	31:24	PWRMTR_WT2_EEMEM_EVT56	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_EEMEM_EVT56 This event measured by this field can be overwritten by AAD0[23].	
	23:16	PWRMTR_WT2_EEMEM_EVT55	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_EEMEM_EVT55 This event measured by this field can be overwritten by AAD0[22].	
	15:8	PWRMTR_WT2_EEMEM_EVT54	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_EEMEM_EVT54 This event measured by this field can be overwritten by AAD0[21].	
	7:0	PWRMTR_WT2_EFPU1_EVT53	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_EFPU1_EVT53 This event measured by this field can be overwritten by AAD0[20].	

PWRMTR_WT2_EEVT57TO58

PWRMTR_WT2_EEVT57TO58 - PWRMTR_WT2_EEVT57TO58			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A988h		
PWRMTR_WT2_EEVT57to58			
DWord	Bit	Description	
0	31:16	Reserved	
		Default Value:	0000h
		Access:	RO
		Reserved	
	15:8	PWRMTR_WT2_EBUSS_EVT58	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_EBUSS_EVT58 This event measured by this field can be overwritten by AAD0[25].	
	7:0	PWRMTR_WT2_EEMEM_EVT57	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_EEMEM_EVT57 This event measured by this field can be overwritten by AAD0[24].	

PWRMTR_WT2_REVT5TO8

PWRMTR_WT2_REVT5TO8 - PWRMTR_WT2_REVT5TO8		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A904h	
PWRMTR_WT2_REVT5to8		
DWord	Bit	Description
0	31:24	Reserved
		Default Value: 00h
	Access: RO	
	Reserved	
23:16	Reserved	
	Default Value: 00h	
15:8	Reserved	
	Default Value: 00h	
7:0	7:0	PWRMTR_WT2_RFFOI_EVT5
		Default Value: 00h
	Access: R/W Lock	
	PWRMTR_WT2_RFFOI_EVT5 This event measured by this field can be overwritten by AAC0[4].	

PWRMTR_WT2_REVT33TO36

PWRMTR_WT2_REVT33TO36 - PWRMTR_WT2_REVT33TO36			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A920h		
PWRMTR_WT2_REVT33to36			
DWord	Bit	Description	
0	31:24	PWRMTR_WT2_RL3MI_EVT36	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_RL3MI_EVT36 This event measured by this field can be overwritten by AAC4[3].	
	23:16	Reserved	
		Default Value:	00h
		Access:	RO
		Reserved	
	15:8	Reserved	
		Default Value:	00h
		Access:	RO
		Reserved	
7:0	Reserved		
	Default Value:	00h	
	Access:	RO	
	Reserved		

PWRMTR_WT2_REVT37TO40

PWRMTR_WT2_REVT37TO40 - PWRMTR_WT2_REVT37TO40			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A924h		
PWRMTR_WT2_REVT37to40			
DWord	Bit	Description	
0	31:24	PWRMTR_WT2_RTAOI_EVT40	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_RTAOI_EVT40 This event measured by this field can be overwritten by AAC4[7].	
	23:16	Reserved	
		Default Value:	00h
		Access:	RO
		Reserved	
	15:8	Reserved	
		Default Value:	00h
		Access:	RO
		Reserved	
7:0	PWRMTR_WT2_RL3MI_EVT37		
	Default Value:	00h	
	Access:	R/W Lock	
	PWRMTR_WT2_RL3MI_EVT37 This event measured by this field can be overwritten by AAC4[4].		

PWRMTR_WT2_REVT41TO44

PWRMTR_WT2_REVT41TO44 - PWRMTR_WT2_REVT41TO44			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A928h		
PWRMTR_WT2_REVT41to44			
DWord	Bit	Description	
0	31:24	Reserved	
		Default Value:	00h
		Access:	RO
		Reserved	
	23:16	Reserved	
		Default Value:	00h
		Access:	RO
		Reserved	
	15:8	Reserved	
		Default Value:	00h
		Access:	RO
		Reserved	
7:0	PWRMTR_WT2_RTAOI_EVT41		
	Default Value:	00h	
	Access:	R/W Lock	
	PWRMTR_WT2_RTAOI_EVT41 This event measured by this field can be overwritten by AAC4[8].		

PWRMTR_WT2_REVT49TO52

PWRMTR_WT2_REVT49TO52 - PWRMTR_WT2_REVT49TO52			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A930h		
PWRMTR_WT2_REVT49to52			
DWord	Bit	Description	
0	31:24	PWRMTR_WT2_RTAOH_EVT52	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_RTAOH_EVT52 This event measured by this field can be overwritten by AAC4[19].	
	23:16	PWRMTR_WT2_RTAOH_EVT51	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_RTAOH_EVT51 This event measured by this field can be overwritten by AAC4[18].	
	15:8	Reserved	
		Default Value:	00h
		Access:	RO
		Reserved	
	7:0	PWRMTR_WT2_RTAOI_EVT49	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_RTAOI_EVT49 This event measured by this field can be overwritten by AAC4[16].	

PWRMTR_WT2_REVT53TO56

PWRMTR_WT2_REVT53TO56 - PWRMTR_WT2_REVT53TO56			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A934h		
PWRMTR_WT2_REVT53to56			
DWord	Bit	Description	
0	31:24	PWRMTR_WT2_RTSOI_EVT56	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_RTSOI_EVT56 This event measured by this field can be overwritten by AAC4[23].	
	23:16	PWRMTR_WT2_RTACN_EVT55	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_RTACN_EVT55 This event measured by this field can be overwritten by AAC4[22].	
	15:8	PWRMTR_WT2_RTACN_EVT54	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_RTACN_EVT54 This event measured by this field can be overwritten by AAC4[21].	
	7:0	Reserved	
		Default Value:	00h
		Access:	RO
		Reserved	

PWRMTR_WT2_REVT65TO68

PWRMTR_WT2_REVT65TO68 - PWRMTR_WT2_REVT65TO68			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A940h		
PWRMTR_WT2_REVT65to68			
DWord	Bit	Description	
0	31:24	Reserved	
		Default Value:	00h
		Access:	RO
		Reserved	
	23:16	Reserved	
		Default Value:	00h
		Access:	RO
		Reserved	
	15:8	PWRMTR_WT2_RGTCN_EVT66	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_RGTCN_EVT66 This event measured by this field can be overwritten by AAC8[1].	
7:0	PWRMTR_WT2_RGTOI_EVT65		
	Default Value:	00h	
	Access:	R/W Lock	
	PWRMTR_WT2_RGTOI_EVT65 This event measured by this field can be overwritten by AAC8[0].		

PWRMTR_WT2_REVT69TO70

PWRMTR_WT2_REVT69TO70 - PWRMTR_WT2_REVT69TO70			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A944h		
PWRMTR_WT2_REVT69to70			
DWord	Bit	Description	
0	31:16	Reserved	
		Default Value:	0000h
		Access:	RO
		Reserved	
		15:8	PWRMTR_WT2_RGTCN_EVT70
			Default Value:
	Access:		R/W Lock
	PWRMTR_WT2_RGTCN_EVT70 This event measured by this field can be overwritten by AAC8[5].		
	7:0	PWRMTR_WT2_RGTCN_EVT69	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_RGTCN_EVT69 This event measured by this field can be overwritten by AAC8[4].	

PWRMTR_WT3_EEVT1TO4

PWRMTR_WT3_EEVT1TO4 - PWRMTR_WT3_EEVT1TO4			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0AA50h		
PWRMTR_WT3_EEVT1to4			
DWord	Bit	Description	
0	31:24	PWRMTR_WT3_EU_TH_EVT4	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_EU_TH_EVT4 This event measured by this field can be overwritten by AACC[3].	
	23:16	PWRMTR_WT3_EU_GA_EVT3	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_EU_GA_EVT3 This event measured by this field can be overwritten by AACC[2].	
	15:8	PWRMTR_WT3_EU_GA_EVT2	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_EU_GA_EVT2 This event measured by this field can be overwritten by AACC[1].	
	7:0	PWRMTR_WT3_EU_GA_EVT1	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_EU_GA_EVT1 This event measured by this field can be overwritten by AACC[0].	

PWRMTR_WT3_EEVT5TO8

PWRMTR_WT3_EEVT5TO8 - PWRMTR_WT3_EEVT5TO8			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0AA54h		
PWRMTR_WT3_EEVT5to8			
DWord	Bit	Description	
0	31:24	PWRMTR_WT3_E0_HP_EVT8	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_E0_HP_EVT8 This event measured by this field can be overwritten by AACC[7].	
	23:16	PWRMTR_WT3_E0_HP_EVT7	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_E0_HP_EVT7 This event measured by this field can be overwritten by AACC[6].	
	15:8	PWRMTR_WT3_E0_HP_EVT6	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_E0_HP_EVT6 This event measured by this field can be overwritten by AACC[5].	
	7:0	PWRMTR_WT3_EU_IO_EVT5	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_EU_IO_EVT5 This event measured by this field can be overwritten by AACC[4].	

PWRMTR_WT3_EEVT9TO12

PWRMTR_WT3_EEVT9TO12 - PWRMTR_WT3_EEVT9TO12		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0AA58h	
PWRMTR_WT3_EEVT9to12		
DWord	Bit	Description
0	31:24	PWRMTR_WT3_E0_SP_EVT12
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E0_SP_EVT12 This event measured by this field can be overwritten by AACC[11].
23:16		PWRMTR_WT3_E0_SP_EVT11
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E0_SP_EVT11 This event measured by this field can be overwritten by AACC[10].
15:8		PWRMTR_WT3_E0_SP_EVT10
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E0_SP_EVT10 This event measured by this field can be overwritten by AACC[9].
7:0		PWRMTR_WT3_E0_HP_EVT9
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E0_HP_EVT9 This event measured by this field can be overwritten by AACC[8].

PWRMTR_WT3_EEVT13TO16

PWRMTR_WT3_EEVT13TO16 - PWRMTR_WT3_EEVT13TO16		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0AA5Ch	
PWRMTR_WT3_EEVT13to16		
DWord	Bit	Description
0	31:24	PWRMTR_WT3_E0_DP_EVT16
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E0_DP_EVT16 This event measured by this field can be overwritten by AACC[15].
Programming Notes		
Must be 0 at all times.		
	23:16	PWRMTR_WT3_E0_DP_EVT15
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E0_DP_EVT15 This event measured by this field can be overwritten by AACC[14].
Programming Notes		
Must be 0 at all times.		
	15:8	PWRMTR_WT3_E0_DP_EVT14
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E0_DP_EVT14 This event measured by this field can be overwritten by AACC[13].
Programming Notes		
Must be 0 at all times.		
	7:0	PWRMTR_WT3_E0_SP_EVT13
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E0_SP_EVT13 This event measured by this field can be overwritten by AACC[12].

PWRMTR_WT3_EEVT17TO20

PWRMTR_WT3_EEVT17TO20 - PWRMTR_WT3_EEVT17TO20			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0AA60h		
PWRMTR_WT3_EEVT17to20			
DWord	Bit	Description	
0	31:24	PWRMTR_WT3_E0INT_EVT20	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_E0INT_EVT20 This event measured by this field can be overwritten by AACC[19].	
	23:16	PWRMTR_WT3_E0INT_EVT19	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_E0INT_EVT19 This event measured by this field can be overwritten by AACC[18].	
		Programming Notes	
	Must be 0 at all times.		
	15:8	PWRMTR_WT3_E0INT_EVT18	
		Default Value:	00h
Access:		R/W Lock	
PWRMTR_WT3_E0INT_EVT18 This event measured by this field can be overwritten by AACC[17].			
7:0	PWRMTR_WT3_E0_DP_EVT17		
	Default Value:	00h	
	Access:	R/W Lock	
	PWRMTR_WT3_E0_DP_EVT17 This event measured by this field can be overwritten by AACC[16].		
	Programming Notes		
Must be 0 at all times.			

PWRMTR_WT3_EEVT21TO24

PWRMTR_WT3_EEVT21TO24 - PWRMTR_WT3_EEVT21TO24		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0AA64h	
PWRMTR_WT3_EEVT21to24		
DWord	Bit	Description
0	31:24	PWRMTR_WT3_E0_QP_EVT24
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E0_QP_EVT24 This event measured by this field can be overwritten by AACC[23].
		Programming Notes
		Must be 0 at all times.
	23:16	PWRMTR_WT3_E0_QP_EVT23
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E0_QP_EVT23 This event measured by this field can be overwritten by AACC[22].
		Programming Notes
		Must be 0 at all times.
	15:8	PWRMTR_WT3_E0_QP_EVT22
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E0_QP_EVT22 This event measured by this field can be overwritten by AACC[21].
	7:0	PWRMTR_WT3_E0INT_EVT21
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E0INT_EVT21 This event measured by this field can be overwritten by AACC[20].

PWRMTR_WT3_EEVT25TO28

PWRMTR_WT3_EEVT25TO28 - PWRMTR_WT3_EEVT25TO28		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0AA68h	
PWRMTR_WT3_EEVT25to28		
DWord	Bit	Description
0	31:24	PWRMTR_WT3_EFPU0_EVT28
		Default Value: 00h
	Access: R/W Lock	
	PWRMTR_WT3_EFPU0_EVT28 This event measured by this field can be overwritten by AACC[27].	
23:16	PWRMTR_WT3_EFPU0_EVT27	
	Default Value: 00h	
Access: R/W Lock		
PWRMTR_WT3_EFPU0_EVT27 This event measured by this field can be overwritten by AACC[26].		
15:8	PWRMTR_WT3_EFPU0_EVT26	
	Default Value: 00h	
Access: R/W Lock		
PWRMTR_WT3_EFPU0_EVT26 This event measured by this field can be overwritten by AACC[25].		
7:0	PWRMTR_WT3_E0_QP_EVT25	
	Default Value: 00h	
Access: R/W Lock		
PWRMTR_WT3_E0_QP_EVT25 This event measured by this field can be overwritten by AACC[24].		
Programming Notes		
Must be 0 at all times.		

PWRMTR_WT3_EEVT29TO32

PWRMTR_WT3_EEVT29TO32 - PWRMTR_WT3_EEVT29TO32			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0AA6Ch		
PWRMTR_WT3_EEVT29to32			
DWord	Bit	Description	
0	31:24	PWRMTR_WT3_E1_HP_EVT32	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_E1_HP_EVT32 This event measured by this field can be overwritten by AACC[31].	
	23:16	PWRMTR_WT3_E1_HP_EVT31	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_E1_HP_EVT31 This event measured by this field can be overwritten by AACC[30].	
	15:8	PWRMTR_WT3_E1_HP_EVT30	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_E1_HP_EVT30 This event measured by this field can be overwritten by AACC[29].	
	7:0	PWRMTR_WT3_EFPU0_EVT29	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_EFPU0_EVT29 This event measured by this field can be overwritten by AACC[28].	

PWRMTR_WT3_EEVT33TO36

PWRMTR_WT3_EEVT33TO36 - PWRMTR_WT3_EEVT33TO36			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0AA70h		
PWRMTR_WT3_EEVT33to36			
DWord	Bit	Description	
0	31:24	PWRMTR_WT3_E1_SP_EVT36	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_E1_SP_EVT36 This event measured by this field can be overwritten by AAD0[3].	
	23:16	PWRMTR_WT3_E1_SP_EVT35	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_E1_SP_EVT35 This event measured by this field can be overwritten by AAD0[2].	
	15:8	PWRMTR_WT3_E1_SP_EVT34	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_E1_SP_EVT34 This event measured by this field can be overwritten by AAD0[1].	
	7:0	PWRMTR_WT3_E1_HP_EVT33	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_E1_HP_EVT33 This event measured by this field can be overwritten by AAD0[0].	

PWRMTR_WT3_EEVT37TO40

PWRMTR_WT3_EEVT37TO40 - PWRMTR_WT3_EEVT37TO40			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0AA74h		
PWRMTR_WT3_EEVT37to40			
DWord	Bit	Description	
0	31:24	PWRMTR_WT3_E1_DP_EVT40	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_E1_DP_EVT40 This event measured by this field can be overwritten by AAD0[7].	
	23:16	PWRMTR_WT3_E1_DP_EVT39	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_E1_DP_EVT39 This event measured by this field can be overwritten by AAD0[6].	
	15:8	PWRMTR_WT3_E1_DP_EVT38	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_E1_DP_EVT38 This event measured by this field can be overwritten by AAD0[5].	
	7:0	PWRMTR_WT3_E1_SP_EVT37	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_E1_SP_EVT37 This event measured by this field can be overwritten by AAD0[4].	

PWRMTR_WT3_EEVT41TO44

PWRMTR_WT3_EEVT41TO44 - PWRMTR_WT3_EEVT41TO44		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0AA78h	
PWRMTR_WT3_EEVT41to44		
DWord	Bit	Description
0	31:24	PWRMTR_WT3_E1INT_EVT44
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E1INT_EVT44 This event measured by this field can be overwritten by AAD0[11].
23:16		PWRMTR_WT3_E1INT_EVT43
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E1INT_EVT43 This event measured by this field can be overwritten by AAD0[10].
Programming Notes		
Must be 0 at all times.		
15:8		PWRMTR_WT3_E1INT_EVT42
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E1INT_EVT42 This event measured by this field can be overwritten by AAD0[9].
7:0		PWRMTR_WT3_E1_DP_EVT41
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E1_DP_EVT41 This event measured by this field can be overwritten by AAD0[8].

PWRMTR_WT3_EEVT45TO48

PWRMTR_WT3_EEVT45TO48 - PWRMTR_WT3_EEVT45TO48		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0AA7Ch	
PWRMTR_WT3_EEVT45to48		
DWord	Bit	Description
0	31:24	PWRMTR_WT3_E1_QP_EVT48
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E1_QP_EVT48 This event measured by this field can be overwritten by AAD0[15].
23:16		PWRMTR_WT3_E1_QP_EVT47
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E1_QP_EVT47 This event measured by this field can be overwritten by AAD0[14].
		Programming Notes
		Must be 0 at all times.
15:8		PWRMTR_WT3_E1_QP_EVT46
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E1_QP_EVT46 This event measured by this field can be overwritten by AAD0[13].
7:0		PWRMTR_WT3_E1INT_EVT45
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E1INT_EVT45 This event measured by this field can be overwritten by AAD0[12].

PWRMTR_WT3_EEVT49TO52

PWRMTR_WT3_EEVT49TO52 - PWRMTR_WT3_EEVT49TO52			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0AA80h		
PWRMTR_WT3_EEVT49to52			
DWord	Bit	Description	
0	31:24	PWRMTR_WT3_EFPU1_EVT52	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_EFPU1_EVT52 This event measured by this field can be overwritten by AAD0[19].	
	23:16	PWRMTR_WT3_EFPU1_EVT51	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_EFPU1_EVT51 This event measured by this field can be overwritten by AAD0[18].	
	15:8	PWRMTR_WT3_EFPU1_EVT50	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_EFPU1_EVT50 This event measured by this field can be overwritten by AAD0[17].	
	7:0	PWRMTR_WT3_E1_QP_EVT49	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_E1_QP_EVT49 This event measured by this field can be overwritten by AAD0[16].	

PWRMTR_WT3_EEVT53TO56

PWRMTR_WT3_EEVT53TO56 - PWRMTR_WT3_EEVT53TO56			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0AA84h		
PWRMTR_WT3_EEVT53to56			
DWord	Bit	Description	
0	31:24	PWRMTR_WT3_EEMEM_EVT56	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_EEMEM_EVT56 This event measured by this field can be overwritten by AAD0[23].	
	23:16	PWRMTR_WT3_EEMEM_EVT55	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_EEMEM_EVT55 This event measured by this field can be overwritten by AAD0[22].	
	15:8	PWRMTR_WT3_EEMEM_EVT54	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_EEMEM_EVT54 This event measured by this field can be overwritten by AAD0[21].	
	7:0	PWRMTR_WT3_EFPU1_EVT53	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_EFPU1_EVT53 This event measured by this field can be overwritten by AAD0[20].	

PWRMTR_WT3_EEVT57TO58

PWRMTR_WT3_EEVT57TO58 - PWRMTR_WT3_EEVT57TO58			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0AA88h		
PWRMTR_WT3_EEVT57to58			
DWord	Bit	Description	
0	31:16	Reserved	
		Default Value:	0000h
		Access:	RO
		Reserved	
	15:8	PWRMTR_WT3_EBUSS_EVT58	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_EBUSS_EVT58 This event measured by this field can be overwritten by AAD0[25].	
	7:0	PWRMTR_WT3_EEMEM_EVT57	
		Default Value:	00h
Access:		R/W Lock	
PWRMTR_WT3_EEMEM_EVT57 This event measured by this field can be overwritten by AAD0[24].			

PWRMTR_WT3_REVT5TO8

PWRMTR_WT3_REVT5TO8 - PWRMTR_WT3_REVT5TO8		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0AA04h	
PWRMTR_WT3_REVT5to8		
DWord	Bit	Description
0	31:24	Reserved
		Default Value: 00h
	Access: RO	
	Reserved	
23:16	Reserved	
	Default Value: 00h	
15:8	Reserved	
	Default Value: 00h	
7:0	PWRMTR_WT3_RFFOI_EVT5	
	Default Value: 00h	
	Access: R/W Lock	
PWRMTR_WT3_RFFOI_EVT5 This event measured by this field can be overwritten by AAC0[4].		

PWRMTR_WT3_REVT33TO36

PWRMTR_WT3_REVT33TO36 - PWRMTR_WT3_REVT33TO36			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0AA20h		
PWRMTR_WT3_REVT33to36			
DWord	Bit	Description	
0	31:24	PWRMTR_WT3_RL3MI_EVT36	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_RL3MI_EVT36 This event measured by this field can be overwritten by AAC4[3].	
	23:16	Reserved	
		Default Value:	00h
		Access:	RO
		Reserved	
	15:8	Reserved	
		Default Value:	00h
		Access:	RO
		Reserved	
7:0	Reserved		
	Default Value:	00h	
	Access:	RO	
	Reserved		

PWRMTR_WT3_REVT37TO40

PWRMTR_WT3_REVT37TO40 - PWRMTR_WT3_REVT37TO40			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0AA24h		
PWRMTR_WT3_REVT37to40			
DWord	Bit	Description	
0	31:24	PWRMTR_WT3_RTAOI_EVT40	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_RTAOI_EVT40 This event measured by this field can be overwritten by AAC4[7].	
	23:16	Reserved	
		Default Value:	00h
		Access:	RO
		Reserved	
	15:8	Reserved	
		Default Value:	00h
		Access:	RO
		Reserved	
7:0	PWRMTR_WT3_RL3MI_EVT37		
	Default Value:	00h	
	Access:	R/W Lock	
	PWRMTR_WT3_RL3MI_EVT37 This event measured by this field can be overwritten by AAC4[4].		

PWRMTR_WT3_REVT41TO44

PWRMTR_WT3_REVT41TO44 - PWRMTR_WT3_REVT41TO44			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0AA28h		
PWRMTR_WT3_REVT41to44			
DWord	Bit	Description	
0	31:24	Reserved	
		Default Value:	00h
		Access:	RO
		Reserved	
	23:16	Reserved	
		Default Value:	00h
		Access:	RO
		Reserved	
	15:8	Reserved	
		Default Value:	00h
		Access:	RO
		Reserved	
	7:0	PWRMTR_WT3_RTAOI_EVT41	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_RTAOI_EVT41 This event measured by this field can be overwritten by AAC4[8].	

PWRMTR_WT3_REVT49TO52

PWRMTR_WT3_REVT49TO52 - PWRMTR_WT3_REVT49TO52			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0AA30h		
PWRMTR_WT3_REVT49to52			
DWord	Bit	Description	
0	31:24	PWRMTR_WT3_RTAOH_EVT52	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_RTAOH_EVT52 This event measured by this field can be overwritten by AAC4[19].	
	23:16	PWRMTR_WT3_RTAOH_EVT51	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_RTAOH_EVT51 This event measured by this field can be overwritten by AAC4[18].	
	15:8	Reserved	
		Default Value:	00h
		Access:	RO
		Reserved	
	7:0	PWRMTR_WT3_RTAOI_EVT49	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_RTAOI_EVT49 This event measured by this field can be overwritten by AAC4[16].	

PWRMTR_WT3_REVT53TO56

PWRMTR_WT3_REVT53TO56 - PWRMTR_WT3_REVT53TO56			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0AA34h		
PWRMTR_WT3_REVT53to56			
DWord	Bit	Description	
0	31:24	PWRMTR_WT3_RTSOI_EVT56	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_RTSOI_EVT56 This event measured by this field can be overwritten by AAC4[23].	
	23:16	PWRMTR_WT3_RTACN_EVT55	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_RTACN_EVT55 This event measured by this field can be overwritten by AAC4[22].	
	15:8	PWRMTR_WT3_RTACN_EVT54	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_RTACN_EVT54 This event measured by this field can be overwritten by AAC4[21].	
	7:0	Reserved	
		Default Value:	00h
		Access:	RO
		Reserved	

PWRMTR_WT3_REVT65TO68

PWRMTR_WT3_REVT65TO68 - PWRMTR_WT3_REVT65TO68			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0AA40h		
PWRMTR_WT3_REVT65to68			
DWord	Bit	Description	
0	31:24	Reserved	
		Default Value:	00h
		Access:	RO
		Reserved	
	23:16	Reserved	
		Default Value:	00h
		Access:	RO
		Reserved	
	15:8	PWRMTR_WT3_RGTCN_EVT66	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_RGTCN_EVT66 This event measured by this field can be overwritten by AAC8[1].	
7:0	PWRMTR_WT3_RGTOI_EVT65		
	Default Value:	00h	
	Access:	R/W Lock	
	PWRMTR_WT3_RGTOI_EVT65 This event measured by this field can be overwritten by AAC8[0].		

PWRMTR_WT3_REVT69TO70

PWRMTR_WT3_REVT69TO70 - PWRMTR_WT3_REVT69TO70			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0AA44h		
PWRMTR_WT3_REVT69to70			
DWord	Bit	Description	
0	31:16	Reserved	
		Default Value:	0000h
		Access:	RO
		Reserved	
	15:8	PWRMTR_WT3_RGTCN_EVT70	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_RGTCN_EVT70 This event measured by this field can be overwritten by AAC8[5].	
	7:0	PWRMTR_WT3_RGTCN_EVT69	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_RGTCN_EVT69 This event measured by this field can be overwritten by AAC8[4].	

PWRMTREVTORE0

PWRMTREVTORE0 - PWRMTREVTORE0						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0AACCh					
GT_CR_POWER_METER_EVENT_OVERRIDE_EU1_32						
DWord	Bit	Description				
0	31:0	<p>PMEVORE0</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>Power Meter Event Override for Render Events. Allows user to override signal coming in from Gfx engine and count event every cycle on a per event basis. For each event: 0: Power Meter works normally with event input taken from Gfx engine. 1: Force event input to weighting logic high every cuclk, overriding event data coming in from Gfx engine. This register is the override for events 1 through 32, where bit 0 corresponds to event 1, and bit 31 corresponds to event 32. "</p>	Default Value:	00000000h	Access:	R/W Lock
Default Value:	00000000h					
Access:	R/W Lock					

PWRMTREVTOR1

PWRMTREVTOR1 - PWRMTREVTOR1				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0AAD0h			
GT_CR_POWER_METER_EVENT_OVERRIDE_EU33_58				
DWord	Bit	Description		
0	31:26	Reserved		
		<table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved</p>	Default Value:	00000000h
Default Value:	00000000h			
Access:	RO			
	25:0	PMEVORE1		
		<table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>Power Meter Event Override for Render Events. Allows user to override signal coming in from Gfx engine and count event every cycle on a per event basis. For each event: 0: Power Meter works normally with event input taken from Gfx engine. 1: Force event input to weighting logic high every cuclk, overriding event data coming in from Gfx engine. This register is the override for events 33 through 64, where bit 0 corresponds to event 33, and bit 25 corresponds to event 58. "</p>	Default Value:	00000000h
Default Value:	00000000h			
Access:	R/W Lock			

PWRMTREVTORM0

PWRMTREVTORM0 - PWRMTREVTORM0						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0AAD4h					
GT_CR_POWER_METER_EVENT_OVERRIDE_MEDIA1_32						
DWord	Bit	Description				
0	31:0	<p>PMEVORM0</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>Power Meter Event Override for Media Events. Allows user to override signal coming in from Gfx engine and count event every cycle on a per event basis. For each event: 0: Power Meter works normally with event input taken from Gfx engine. 1: Force event input to weighting logic high every cuclk, overriding event data coming in from Gfx engine. This register is the override for events 1 through 32, where bit 0 corresponds to event 1, and bit 31 corresponds to event 32. "</p>	Default Value:	00000000h	Access:	R/W Lock
Default Value:	00000000h					
Access:	R/W Lock					

PWRMTREVTORM1

PWRMTREVTORM1 - PWRMTREVTORM1				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0AAD8h			
GT_CR_POWER_METER_EVENT_OVERRIDE_MEDIA33_36				
DWord	Bit	Description		
0	31:4	Reserved		
		<table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved</p>	Default Value:	00000000h
Default Value:	00000000h			
Access:	RO			
	3:0	PMEVORM1		
		<table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>Power Meter Event Override for Media Events. Allows user to override signal coming in from Gfx engine and count event every cycle on a per event basis. For each event: 0: Power Meter works normally with event input taken from Gfx engine. 1: Force event input to weighting logic high every cuclk, overriding event data coming in from Gfx engine. This register is the override for events 33 through 36, where bit 0 corresponds to event 33, and bit 3 corresponds to event 36. "</p>	Default Value:	0h
Default Value:	0h			
Access:	R/W Lock			

PWRMTREVTORR0

PWRMTREVTORR0 - PWRMTREVTORR0						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0AAC0h					
GT_CR_POWER_METER_EVENT_OVERRIDE_RENDER1_32						
DWord	Bit	Description				
0	31:0	<p>PMEVORR0</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>Power Meter Event Override for Render Events. Allows user to override signal coming in from Gfx engine and count event every cycle on a per event basis. For each event: 0: Power Meter works normally with event input taken from Gfx engine. 1: Force event input to weighting logic high every cuclk, overriding event data coming in from Gfx engine. This register is the override for events 1 through 32, where bit 0 corresponds to event 1, and bit 31 corresponds to event 32.</p>	Default Value:	00000000h	Access:	R/W Lock
Default Value:	00000000h					
Access:	R/W Lock					

PWRMTREVTORR1

PWRMTREVTORR1 - PWRMTREVTORR1						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0AAC4h					
GT_CR_POWER_METER_EVENT_OVERRIDE_RENDER33_64						
DWord	Bit	Description				
0	31:0	<p>PMEVORR1</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>Power Meter Event Override for Render Events. Allows user to override signal coming in from Gfx engine and count event every cycle on a per event basis. For each event: 0: Power Meter works normally with event input taken from Gfx engine. 1: Force event input to weighting logic high every cuclk, overriding event data coming in from Gfx engine. This register is the override for events 33 through 64, where bit 0 corresponds to event 33, and bit 31 corresponds to event 64.</p>	Default Value:	00000000h	Access:	R/W Lock
Default Value:	00000000h					
Access:	R/W Lock					

PWRMTREVTORR2

PWRMTREVTORR2 - PWRMTREVTORR2				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0AAC8h			
GT_CR_POWER_METER_EVENT_OVERRIDE_RENDER65_70				
DWord	Bit	Description		
0	31:6	Reserved		
		<table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved</p>	Default Value:	00000000h
Default Value:	00000000h			
Access:	RO			
	5:0	PMEVORR2		
		<table border="1"> <tr> <td>Default Value:</td> <td>00h</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>Power Meter Event Override for Render Events. Allows user to override signal coming in from Gfx engine and count event every cycle on a per event basis. For each event: 0: Power Meter works normally with event input taken from Gfx engine. 1: Force event input to weighting logic high every cuclk, overriding event data coming in from Gfx engine. This register is the override for events 65 through 70, where bit 0 corresponds to event 65, and bit 5 corresponds to event 70. "</p>	Default Value:	00h
Default Value:	00h			
Access:	R/W Lock			

RAM Clock Gating Control 1

RCGCTL1 - RAM Clock Gating Control 1				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	09410h			
RAM Clock Gating Control Registers.				
DWord	Bit	Description		
0	31	<p>USBunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>USBunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
	Access:	R/W		
	30	<p>VLFunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VLFunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
	Access:	R/W		
29	<p>VISunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VISunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			
28	<p>STCunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>STCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			

RCGCTL1 - RAM Clock Gating Control 1

27	<p>TDSunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>TDSunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
26	<p>VMCunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VMCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
25	<p>QRCunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>QRCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
24	<p>SCunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>SCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
23	<p>SVLunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>SVLunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
22	<p>VFunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VFunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

RCGCTL1 - RAM Clock Gating Control 1

21	<p>URBunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>URBunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
20	<p>GAMWunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>GAMWunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
19	<p>SVGunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>SVGunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
18	<p>RCZunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>RCZunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
17	<p>RCPBEunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>RCPBEunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
16	<p>RCCunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>RCCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

RCGCTL1 - RAM Clock Gating Control 1

15	<p>PSDunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>PSDunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
14	<p>MTunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>MTunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
13	<p>SBEunit RAM Clock gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>SBEunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
12	<p>IZunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>IZunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
11	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table>	Access:	R/W
Access:	R/W		
10	<p>ICunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>ICunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
9	<p>HIZunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>HIZunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

RCGCTL1 - RAM Clock Gating Control 1

8	<p>GAMunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>GAMunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
7	<p>BCunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td>R/W</td> </tr> </table> <p>BCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
6	<p>HDCunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td>R/W</td> </tr> </table> <p>GAFSunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
5	<p>DMunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td>R/W</td> </tr> </table> <p>DMunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
4	<p>WMFEunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td>R/W</td> </tr> </table> <p>WMFEunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
3	<p>CSunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td>R/W</td> </tr> </table> <p>CSunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				

RCGCTL1 - RAM Clock Gating Control 1			
2	<p>BLBunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>BLBunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
1	<p>MPCunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>MPCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
0	<p>BFunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>BFunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

RAM Clock Gating Control 1

RCGCTL1 - RAM Clock Gating Control 1				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000100			
Size (in bits):	32			
Address:	09410h			
RAM Clock Gating Control Registers.				
DWord	Bit	Description		
0	31	USBunit RAM Clock Gating Disable <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> USBunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	Access:	R/W
	Access:	R/W		
	30	VLFunite RAM Clock Gating Disable <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> VLFunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	Access:	R/W
	Access:	R/W		
29	VISunit RAM Clock Gating Disable <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> VISunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	Access:	R/W	
Access:	R/W			
28	STCunit RAM Clock Gating Disable <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> STCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	Access:	R/W	
Access:	R/W			

RCGCTL1 - RAM Clock Gating Control 1

27	<p>TDSunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>TDSunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
26	<p>VMCunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VMCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
25	<p>QRCunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>QRCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
24	<p>SCunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>SCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
23	<p>SVLunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>SVLunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
22	<p>VFunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VFunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

RCGCTL1 - RAM Clock Gating Control 1

21	<p>URBunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>URBunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
20	<p>GAMWunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>GAMWunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
19	<p>SVGunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>SVGunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
18	<p>RCZunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>RCZunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
17	<p>RCPBEunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>RCPBEunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
16	<p>RCCunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>RCCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

RCGCTL1 - RAM Clock Gating Control 1

15	<p>PSDunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>PSDunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
14	<p>MTunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>MTunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
13	<p>SBEunit RAM Clock gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>SBEunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
12	<p>IZunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>IZunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
11	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table>	Access:	R/W
Access:	R/W		
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Access:	R/W		
9	<p>HIZunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>HIZunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

RCGCTL1 - RAM Clock Gating Control 1

8	<p>GAMunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>GAMunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				
7	<p>BCunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>BCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
6	<p>HDCunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>GAFSunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
5	<p>DMunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>DMunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
4	<p>WMFEunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>WMFEunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
3	<p>CSunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>CSunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				

RCGCTL1 - RAM Clock Gating Control 1			
2	<p>BLBunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>BLBunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
1	<p>MPCunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>MPCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
0	<p>BFunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>BFunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

RAM Clock Gating Control 2

RCGCTL2 - RAM Clock Gating Control 2		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x7FC00000	
Size (in bits):	32	
Address:	09414h	
RAM Clock Gating Control Registers.		
DWord	Bit	Description
0	31	SPARE 2 clock gate disable
		Access: R/W
	SPARE 2 unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	30:28	VMCRunit clock gate disable
Default Value: 111b Access: R/W		
VMCR unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
27:25	SMCRunit clock gate disable	
	Default Value: 111b Access: R/W	
SMCR unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
24:22	MCRunit clock gate disable	
	Default Value: 111b Access: R/W	
MCR unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		

RCGCTL2 - RAM Clock Gating Control 2

21	Reserved		
20	<p>WVISunit clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>WVIS unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
19	<p>WAVM unit RAM clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>WAVM unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
18	<p>WHME unit RAM clock gate disable bit</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>WHME unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
17	<p>WIME unit RAM clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>WIME unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
16	<p>WMPC unit RAM clock gating disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>WMPC unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
15	<p>SDEunit RAM clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>SDE unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

RCGCTL2 - RAM Clock Gating Control 2

14	<p>VSHM unit clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VSHM unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
13	<p>DAPRTS unit RAM clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>DAPRTS unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.</p>	Access:	R/W
Access:	R/W		
12	<p>GS unit RAM clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>GS unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
11	Reserved		
10	<p>GAMTunit RAM clock gate disable bit</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>GAMT unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
9	<p>VCW unit RAM clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VCW unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
8	<p>VEO unit RAM clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VEO unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

RCGCTL2 - RAM Clock Gating Control 2

7	<p>IMEunit RAM clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>IMEunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
6	<p>CREunit RAM clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>CREunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
5	<p>RSunit RAM clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>RSunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
4	<p>MSCunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>MSCunit RAM Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
3	<p>VMXunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VMXunit RAM Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
2	<p>GAunit RAM Clock Gating Disable for all EUs</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>GAunit RAM Clock Gating Disable Control For all EUs in each Row: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

RCGCTL2 - RAM Clock Gating Control 2			
1	<p>VSunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VSunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
0	<p>HSunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>HSunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

RAM Clock Gating Control 2

RCGCTL2 - RAM Clock Gating Control 2			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0xFFC00000		
Size (in bits):	32		
Address:	09414h		
RAM Clock Gating Control Registers.			
DWord	Bit	Description	
0	31	1x2X Assign fub XOR clock gate disable	
		Default Value:	1b
		Access:	R/W
		XOR based unit level clock gating disable in 1x2x_asgn fub: '0' : XOR Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : XOR Clock Gating Disabled. (i.e., clocks are toggling, always)	
	30:28	VMCRunit clock gate disable	
		Default Value:	111b
		Access:	R/W
		VMCR unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	27:25	SMCRunit clock gate disable	
		Default Value:	111b
		Access:	R/W
		SMCR unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	24:22	MCRunit clock gate disable	
		Default Value:	111b
		Access:	R/W
		MCR unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

RCGCTL2 - RAM Clock Gating Control 2

21	<p>MUCunit RAM clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>MUC unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
20	<p>WVISunit clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>WVIS unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
19	<p>WAVM unit RAM clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>WAVM unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
18	<p>WHME unit RAM clock gate disable bit</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>WHME unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
17	<p>WIME unit RAM clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>WIME unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
16	<p>WMPC unit RAM clock gating disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>WMPC unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

RCGCTL2 - RAM Clock Gating Control 2

15	<p>SDEunit RAM clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>SDE unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
14	<p>VSHM unit clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VSHM unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
13	<p>DAPRTS unit RAM clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>DAPRTS unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.</p>	Access:	R/W
Access:	R/W		
12	<p>GS unit RAM clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>GS unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
11	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table>	Access:	R/W
Access:	R/W		
10	<p>GAMTunit RAM clock gate disable bit</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>GAMT unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
9	<p>VCW unit RAM clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VCW unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

RCGCTL2 - RAM Clock Gating Control 2

8	<p>VEO unit RAM clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VEO unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
7	<p>IMEunit RAM clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>IMEunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
6	<p>CREunit RAM clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>CREunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
5	<p>RSunit RAM clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>RSunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
4	<p>MSCunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>MSCunit RAM Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
3	<p>VMXunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VMXunit RAM Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

RCGCTL2 - RAM Clock Gating Control 2			
2	<p>GAunit RAM Clock Gating Disable for all EUs</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>GAunit RAM Clock Gating Disable Control For all EUs in each Row: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
1	<p>VSunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VSunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
0	<p>HSunit RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>HSunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

RAM Clock Gating Control 3

RCGCTL3 - RAM Clock Gating Control 3				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	09434h			
DWord	Bit	Description		
0	31:13	<p>RSVD</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved</p>	Access:	RO
	Access:	RO		
	12	Reserved		
	11	<p>cp_ramcgdis_hwm</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>HWM unit Clock Gating Disable (cp_ramcgdis_hwm) HWM unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
	Access:	R/W		
10	<p>cp_ramcgdis_hed</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>HED unit Clock Gating Disable (cp_ramcgdis_hed) HED unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			
9	<p>cp_ramcgdis_hpp</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>HPP unit Clock Gating Disable (cp_ramcgdis_hpp) HPP unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			
8	<p>cp_ramcgdis_hpr</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>HPR unit Clock Gating Disable (cp_ramcgdis_hpr) HPR unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p>	Access:	R/W	
Access:	R/W			

RCGCTL3 - RAM Clock Gating Control 3

		'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
7	cp_ramcgdis_hmc	Access:	R/W
	HMC unit Clock Gating Disable (cp_ramcgdis_hmc) HMC unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
6	cp_ramcgdis_hlf	Access:	R/W
	HLF unit Clock Gating Disable (cp_ramcgdis_hlf) HLF unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
5	cp_ramcgdis_hmx	Access:	R/W
	HMX unit Clock Gating Disable (cp_ramcgdis_hmx) HMX unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
4	cp_ramcgdis_vmm	Access:	R/W
	VMM unit Clock Gating Disable (cp_ramcgdis_vmm) VMM unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
3	cp_ramcgdis_mpd	Access:	R/W
	MPD unit Clock Gating Disable (cp_ramcgdis_mpd) MPD unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)		

RCGCTL3 - RAM Clock Gating Control 3

		'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
2	cp_ramcgdis_mbd	
	Access:	R/W
	MBD unit Clock Gating Disable (cp_ramcgdis_mbd) MBD unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
1	cp_ramcgdis_mmx	
	Access:	R/W
	MMX unit Clock Gating Disable (cp_ramcgdis_mmx) MMX unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
0	cp_ramcgdis_vmvc	
	Access:	R/W
	VMVC unit Clock Gating Disable (cp_ramcgdis_vmvc) VMVC unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

RC6 Wake Rate Limit

RCXWRL - RC6 Wake Rate Limit				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A09Ch-0A09Fh			
DWord	Bit	Description		
0	31:16	<p>RC6WRL</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>RC Promotion Time Modulated by wake rate limits when using EI method: Even though the RC6 promotion time is met, if the wake limit is exceeded, no promotion pmcr_rc6_wake_rate_limit[15:0]</p>	Access:	R/W
	Access:	R/W		
15:0	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			

RCC LRA 0

RCC_LRA_0 - RCC LRA 0			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x7F403F00		
Size (in bits):	32		
Address:	04A40h		
DWord	Bit	Description	
0	31:24	RCC LRA1 Max	
		Default Value:	01111111b
		Access:	R/W
		Maximum value of programmable LRA1.	
	23:16	RCC LRA1 Min	
		Default Value:	01000000b
		Access:	R/W
		Minimum value of programmable LRA1.	
	15:8	RCC LRA0 Max	
		Default Value:	00111111b
		Access:	R/W
		Maximum value of programmable LRA0.	
	7:0	RCC LRA0 Min	
		Default Value:	00000000b
		Access:	R/W
		Minimum value of programmable LRA0.	

RCC LRA 1

RCC_LRA_1 - RCC LRA 1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000001	
Size (in bits):	32	
Address:	04A44h	
DWord	Bit	Description
0	31:2	Reserved
		Default Value: 0000000000000000000000000000000b
		Access: RO
	1	MSC LRA
		Default Value: 0b
		Access: R/W Which LRA should MSC use.
	0	RCC LRA
		Default Value: 1b
		Access: R/W Which LRA should RCC use.

RCC Virtual page Address Registers

RCCTLB_VA - RCC Virtual page Address Registers						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	RenderCS					
Default Value:	0x00000000					
Access:	RO					
Size (in bits):	32					
Trusted Type:	1					
Address:	04A00h-04A03h					
These registers are directly mapped to the current Virtual Addresses in the RCCTLB (Render Cache for Color TLB).						
DWord	Bit	Description				
0	31:12	Address <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[31:12]</td> </tr> </table> Page virtual address.	Project:	All	Format:	GraphicsAddress[31:12]
	Project:	All				
Format:	GraphicsAddress[31:12]					
11:0	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ	
Project:	CHV, BSW					
Format:	MBZ					

RC Evaluation Interval

RCI - RC Evaluation Interval			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A0A8h-0A0ABh		
DWord	Bit	Description	
0	31:24	Reserved Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>RO</td></tr></table>	RO
	RO		
23:0	Render Standby Evaluation Interval Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>R/W</td></tr></table> 0 = 0 usec 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec pmcr_rc_ei[23:0]	R/W	
R/W			

RC Idle Hysteresis

RCIHYST - RC Idle Hysteresis				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A0ACh-0A0AFh			
DWord	Bit	Description		
0	31:24	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%; text-align: center;">RO</td> </tr> </table>	Access:	RO
	Access:	RO		
23:0	RC Idle Hysteresis Detection <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%; text-align: center;">R/W</td> </tr> </table> <p>Idle intervals must be longer than this value to be considered idle. 0 = 0 usec means disabled 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec This must not be set to more than 5ms to prevent the PCU from timing out on an S state entry</p>	Access:	R/W	
Access:	R/W			

RCS_PREEMPTION_HINT

RCS_PREEMPTION_HINT - RCS_PREEMPTION_HINT	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	024BCh
Description	
<p>This register contains the Head pointer offset in to the Ring Buffer or the Dword aligned Graphics address in to the Batch Buffer corresponding to either MI_ARB_CHECK called Preemption Hint Address. When Preemption Hint Address is enabled, RCS will honor UHPTR only on parsing MI_ARB_CHK at Preemption Hint Address.</p> <p>This register contains the Head pointer offset into the Ring Buffer or the Dword aligned Graphics address into the Batch Buffer corresponding to the below listed commands in execlist mode of operation</p> <ul style="list-style-type: none"> • MI_ARB_CHECK • MI_WAIT_FOR_EVENT • MI_SEMAPHORE_WAIT • 3D_PRIMITIVE • GPGPU_WALKER • MEDIA_STATE_FLUSH • PIPE_CONTROL (Only in GPGPU mode of pipeline selection) • MI_ATOMIC (Post Sync Operation set in GPGPU mode of pipeline selection) • MI_SEMAPHORE_SIGNAL (Post Sync Operation set in GPGPU mode of pipeline selection) 	
Programming Notes	
<p>Programming Restriction: This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of UHPTR being sampled by a given MI_ARB_CHECK in command stream. Programmer has to ensure that RCS Preemption Hint register gets programmed before UHPTR is programmed and well before RCS crosses the corresponding execution point. Preemption hint for both RingBuffer and Batch Buffer can't be enabled simultaneously.</p> <p>User must ensure the Preempted Hint Address programmed matches either Ring Head Offset or Batch Buffer Graphics Virtual Address and not both of them. User must also ensure the Preempted Hint Address[19:0] programmed matches either Ring Head Offset[19:0] or Batch Buffer Graphics Virtual Address[19:0] and not both of them.</p>	

RCS_PREEMPTION_HINT - RCS_PREEMPTION_HINT					
DWord	Bit	Description			
0	31:2	Preempted Hint Address			
		Project:	CHV, BSW		
		Format:	U30		
		This field contains the Head offset in to the Ring Buffer when Preemption Hint is set to Ring Buffer and Dword aligned Graphics Address in to the batch buffer when Preemption Hint is set to Batch Buffer.			
	1	Batch Buffer Preemption Hint			
		Project:	CHV, BSW		
		Format:	Enabled		
		Value	Name	Description	Project
		0h	Disabled	Preemption hint is disabled in batch buffer.	CHV, BSW
		1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Batch Buffer.	CHV, BSW
		0	Ring Preemption Hint		
	Project:		CHV, BSW		
Format:	Enable				
Value	Name		Description	Project	
0h	Disable		Preemption hint is disabled in ring buffer.	CHV, BSW	
1h	Enabled		Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Ring Buffer.	CHV, BSW	

RCS_PREEMPTION_HINT_UDW

RCS_PREEMPTION_HINT_UDW - RCS_PREEMPTION_HINT_UDW				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	RenderCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	024C8h			
<p>This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the Batch Buffer corresponding to MI_ARB_CHECK command called Preemption Hint Address.</p>				
Programming Notes				
<p>Programming Restriction: This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of UHPTR being sampled by a given MI_ARB_CHK in command stream.</p>				
DWord	Bit	Description		
0	31:16	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
15:0	<p>Preempted Hint Address Upper DWORD</p> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>This field contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the batch buffer when Preemption Hint is set to Batch Buffer. This field is not valid when Preemption Hint is set to Ring Buffer.</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			

RCS Batch Buffer State Register

RCS_BB_STATE - RCS Batch Buffer State Register											
Register Space:	MMIO: 0/2/0										
Project:	CHV, BSW										
Source:	RenderCS										
Default Value:	0x00000000 CHV, BSW										
Access:	RO										
Size (in bits):	32										
Address:	02110h										
<p>This register contains the attributes of the current batch buffer initiated from the Ring Buffer.</p> <p>This register should not be written by software. These fields should only get written by a context restore. Software should always set these fields via the MI_BATCH_BUFFER_START command when initiating a batch buffer. This register is saved and restored with context.</p>											
DWord	Bit	Description									
0	31:9	Reserved Format: MBZ									
	8	Reserved Format: MBZ									
	7	Resource Streamer Enable Project: CHV, BSW Format: U1 When this bit is set, the Resource Streamer will execute the batch buffer. When this bit is clear the Resource Streamer will not execute the batch buffer.									
	6	Reserved									
	5	Address Space Indicator Project: CHV, BSW Note: This field reflects the effective address space indicator security level and may not be the same as the Address Space Indicator written using MI_BATCH_BUFFER_START. <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>GGTT [Default]</td> <td>This Batch buffer is located in GGTT memory and is privileged</td> </tr> <tr> <td>1h</td> <td>PPGTT</td> <td>This Batch buffer is located in PPGTT memory and is non-privileged.</td> </tr> </tbody> </table>	Value	Name	Description	0h	GGTT [Default]	This Batch buffer is located in GGTT memory and is privileged	1h	PPGTT	This Batch buffer is located in PPGTT memory and is non-privileged.
	Value	Name	Description								
	0h	GGTT [Default]	This Batch buffer is located in GGTT memory and is privileged								
	1h	PPGTT	This Batch buffer is located in PPGTT memory and is non-privileged.								
	4	Reserved Project: CHV, BSW Format: MBZ									
	3:0	Reserved Format: MBZ									

RCS Context Preemption Hint

RCS_CTXID_PREEMPTION_HINT - RCS Context Preemption Hint				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	RenderCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	024CCh			
Address:	124CCh-124CFh			
Name:	Context ID Preemption Hint			
ShortName:	RCS_CTXID_PREEMPTION_HINT_VCSUNIT0			
Address:	1A4CCh-1A4CFh			
Name:	Context ID Preemption Hint			
ShortName:	RCS_CTXID_PREEMPTION_HINT_VECSUNIT			
Address:	1C4CCh-1C4CFh			
Name:	Context ID Preemption Hint			
ShortName:	RCS_CTXID_PREEMPTION_HINT_VCSUNIT1			
Address:	224CCh-224CFh			
Name:	Context ID Preemption Hint			
ShortName:	RCS_CTXID_PREEMPTION_HINT_BCSUNIT			
<p>This register contains the Context ID of a context in execlist mode of operation. In execlist mode of operation RCS_PREEMPTION_HINT and RS_PREEMPTION_HINT registers are looked at by Render Command Streamer and Resource Streamer only on executing a context having Context ID that matches with the contents of this register. This register contents are valid and looked at only in execlist mode of operation</p> <p>Programming Restriction: This register should NEVER be programmed in functional mode, this must be used only in validation mode to achieve deterministic preemption behavior in execlist mode of operation.</p>				
DWord	Bit	Description		
0	31:0	<p>Context ID Preemption Hint</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="text-align: center;">U32</td> </tr> </table> <p>If 0 this field has no effect. If nonzero it indicates the only context ID that can be preempted when execlists are enabled. A preemption attempt when the context ID of the currently executing ring context does not match this field will be ignored.</p>	Format:	U32
Format:	U32			

RC Wake Counter

RCWC - RC Wake Counter				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A0A4h-0A0A7h			
DWord	Bit	Description		
0	31:16	<p>Wake Counter Render</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Incremented for each wake event , wraps around wake_counter[15:0]</p>	Access:	RO
	Access:	RO		
15:0	<p>Wake Counter Media</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Incremented for each wake event , wraps around wake_counter[15:0]</p>	Access:	RO	
Access:	RO			

RCZ Virtual Page Address Registers

RCZTLB_VA - RCZ Virtual Page Address Registers				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	RenderCS			
Default Value:	0x00000000			
Access:	RO			
Size (in bits):	32			
Trusted Type:	1			
Address:	04B00h-04B03h			
These registers are directly mapped to the current Virtual Addresses in the RCZTLB (Render Cache for Z (Depth), Hi Z, and Stencil TLB).				
DWord	Bit	Description		
0	31:12	Address <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[31:12]</td> </tr> </table> Page virtual address.	Format:	GraphicsAddress[31:12]
	Format:	GraphicsAddress[31:12]		
11:0	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ			

Ready Bit Vector 0 for TLBPEND registers

TLBPEND_RDY0 - Ready Bit Vector 0 for TLBPEND registers		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	04708h-0470Bh	
This register contains the ready bits for entries 0-31 of TLBPEND structure (Cycles pending TLB translation).		
DWord	Bit	Description
0	31:0	Ready bits per entry

Ready Bit Vector 1 for TLBPEND registers

TLBPEND_RDY1 - Ready Bit Vector 1 for TLBPEND registers		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	0470Ch-0470Fh	
This register contains the ready bits for entries 32-63 of TLBPEND structure (Cycles pending TLB translation).		
DWord	Bit	Description
0	31:0	Ready bits per entry

Render C State Control 1

RCCTL1 - Render C State Control 1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A090h-0A093h	
DWord	Bit	Description
0	31:29	Reserved Access: RO
	28	TO - HW RC Promotion (i.e., Depth) Selection Access: R/W 0: Timeout method disabled 1: TO method enabled pmcr_to_enable
	27	EI - HW RC Promotion (i.e., Depth) Selection Access: R/W 0: EI disabled 1: Evaluation Interval (EI) method enabled pmcr_ei_enable
	26:25	Reserved Access: RO
	24	Reserved Access: R/W
	23	Reserved Access: R/W
	22:0	Reserved Access: RO

Render forcewake acknowledge

RENFW_ACK - Render forcewake acknowledge						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	1300B4h					
This register contains the per thread force wake acknowledge bits for the Render power well.						
DWord	Bit	Description				
0	31:16	<p>RESERVED</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved.</p>	Default Value:	0000h	Access:	RO
	Default Value:	0000h				
Access:	RO					
15:0	<p>FWAKERENDERACK</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Force Wake Render request bits. Driver must poll on the corresponding bit to confirm that the well has woken. For example, if 13_00B0[0] is written to a '1' (along with 13_00B0[16]='1'), then bit0 of this register indicates when the force wake request has been completed.</p>	Default Value:	0000h	Access:	RO	
Default Value:	0000h					
Access:	RO					

Render forcewake request

RENFW_REQ - Render forcewake request			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	1300B0h		
<p>This register contains per thread force wake request bits for the Render power Well. The upper 16 bits act as masks for the lower 16 bits. Bit 31 masks bit 15 and bit 16 masks bit 0.</p> <ol style="list-style-type: none"> 1. Driver writes to GPM force wake request bit. (VV will have a Render(13_00B0(15:0)) and a Media (13_00B8(15:0)) bits.) 2. The GPM responds by writing (via PLINK) to 1300B4[15:0] or 1300BC[15:0] register. 3. Driver polls (1300B4[15:0] and/or 1300BC[15:0])status until 1... indicating that that well has completed wake sequence. <p>Since the registers are per thread, only the specific bit that was forced should be checked for status.</p>			
DWord	Bit	Description	
0	31:16	FWAKERENDERREQMSK	
		Default Value:	0000h
		Access:	RO
		Mask bits for lower 16 bits to avoid a read modify/write. If '0', the corresponding bit in [15:0] is not changed. If '1', the corresponding bit in [15:0] is changed to the value in [15:0]	
15	15	FWAKERENDERREQ15	
		Default Value:	0b
		Access:	R/W
Force Wake Render request 15.			
14	14	FWAKERENDERREQ14	
		Default Value:	0b
		Access:	R/W
Force Wake Render request 14.			
13	13	FWAKERENDERREQ13	
		Default Value:	0b
		Access:	R/W
Force Wake Render request 13.			

RENFW_REQ - Render forcewake request						
	12	<p>FWAKERENDERREQ12</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Force Wake Render request 12.</p>	Default Value:	0b	Access:	R/W
	Default Value:	0b				
	Access:	R/W				
	11	<p>FWAKERENDERREQ11</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Force Wake Render request 11.</p>	Default Value:	0b	Access:	R/W
	Default Value:	0b				
	Access:	R/W				
	10	<p>FWAKERENDERREQ10</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Force Wake Render request 10.</p>	Default Value:	0b	Access:	R/W
	Default Value:	0b				
Access:	R/W					
9	<p>FWAKERENDERREQ9</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Force Wake Render request 9.</p>	Default Value:	0b	Access:	R/W	
Default Value:	0b					
Access:	R/W					
8	<p>FWAKERENDERREQ8</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Force Wake Render request 8.</p>	Default Value:	0b	Access:	R/W	
Default Value:	0b					
Access:	R/W					
7	<p>FWAKERENDERREQ7</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Force Wake Render request 7.</p>	Default Value:	0b	Access:	R/W	
Default Value:	0b					
Access:	R/W					
6	<p>FWAKERENDERREQ6</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Force Wake Render request 6.</p>	Default Value:	0b	Access:	R/W	
Default Value:	0b					
Access:	R/W					
5	<p>FWAKERENDERREQ5</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Force Wake Render request 5.</p>	Default Value:	0b	Access:	R/W	
Default Value:	0b					
Access:	R/W					

RENFW_REQ - Render forcewake request		
	4	FWAKERENDERREQ4
		Default Value: 0b
	Access: R/W	
	Force Wake Render request 4.	
	3	FWAKERENDERREQ3
		Default Value: 0b
	Access: R/W	
	Force Wake Render request 3.	
	2	FWAKERENDERREQ2
		Default Value: 0b
	Access: R/W	
	Force Wake Render request 2.	
	1	FWAKERENDERREQ1
		Default Value: 0b
	Access: R/W	
	Force Wake Render request 1.	
	0	FWAKERENDERREQ0
		Default Value: 0b
	Access: R/W	
	Force Wake Render request 0.	

Render Geyserville Mode Control 1

RPMODECTL1 - Render Geyserville Mod						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0A024h-0A027h					
DWord	Bit	Description				
0	31:12	Reserved				
		Access:				
	11	RP Video Turbo Enable for Media Engine				
		Access:				
		Refer to bits A024[10:9] for different Media turbo scenarios. Refer to the table in the description for bits A024[10:9].				
10:9		RP Software Mode Control				
		Access:				
		11 - Media_active (8000[6]), Media_done and RPVTENMEDIA(A024[11]) are don't care. Media turbo freq is selected.				
		10 - Media_active (8000[6]), Media_done and RPVTENMEDIA(A024[11]) are don't care. Normal freq(Hard coded).				
		01 - Based on the status either the media-turbo or normal frequency will be selected.				
		If Media_active(8000[6]) is set, Media_done and RPVTENMEDIA(A024[11]) are don't care. Media turbo freq is selected.				
		Else If RPVTENMEDIA(A024[11]) is 0, Media_done is don't care. Normal freq is selected.				
		Else If RPVTENMEDIA(A024[11]) is 1, Media turbo freq is selected based on internal status. if Media_done is set.				
		00 - Media_active (8000[6]), Media_done and RPVTENMEDIA(A024[11]) are don't care. Current frequency is maintained.				
		Note: Media is done only when both VCS(8004[0] = 1) and VECS(8010[0] = 1) are idle. Media_done = 8004[0] and				
		pmcr_rpsw_ctl_mode[1]	pmcr_rpsw_ctl_mode[0]	pmmr_media_active	pmcr_rpsw_vten_vcs	pmmr_vcs
		A024[10]	A024[9]	8000[4]	A024[11]	8000[1]
		1	1	x	x	x
		1	0	x	x	x
		0	1	1	x	x
		0	1	0	0	0
		0	1	0	0	1
		0	1	0	1	0

RPMODECTL1 - Render Geyserville Mod

	0	1	0	1	1
	0	0	x	x	x
	CHV, BSW description				
	pmcr_rpsw_ctl_mode[1]	pmcr_rpsw_ctl_mode[0]	pmmr_media_active	pmcr_rpsw_vten_vcs	pmmr_vcs
	A024[10]	A024[9]	8000[6]	A024[11]	8004[0]
	1	1	x	x	x
	1	0	x	x	x
	0	1	1	x	x
	0	1	0	0	0
	0	1	0	0	1
	0	1	0	1	0
	0	1	0	1	1
	0	0	x	x	x
8	Mask Bits for Graphics Busyness Access: <div style="text-align: right; color: blue; font-weight: bold; margin-top: 10px;">Description</div> Mask Bits for Graphics Busyness (MBGB) and enables MC0 counter: 0: MFX busyness is not counted as part of gfx busyness and media MC0 counter forced to a zero. 1: MFX busyness is counted as part of gfx busyness and media MC0 counter is allowed to count. Both VCS and VECS is counted towards media busyness. BIOS/driver should always set this bit to a one. pmcr_media_mask Mask Bits for Graphics Busyness (MBGB): 0: MFX busyness is not counted as part of gfx busyness 1: MFX busyness is counted as part of gfx busyness Both VCS and VECS is counted towards media busyness pmcr_media_mask				
7	Render Geyserville HW Controlled Idle Mode Enable Access: 0 - Disables Render Geyserville (RP) function (default). 1 - Turns on the Render Geyserville (RP) function and RP counters are enabled (program enable after counter v				

RPMODECTL1 - Render Geyserville Mod

6	<p>Reserved</p> <p>Access:</p> <p>Reserved</p>
5:3	<p>Frequency Increase Utilization Metric Selection</p> <p>Access:</p> <p>Frequency Increase Utilization Metric selection The selection of a metric below indicates which one is to be used in making decision. All the metrics should be More than Busy Max Continuous (BMXC) time must be reached for a frequency increase More than Busy Max Average (BMXA) at end of Evaluation Interval must be reached for a frequency increase Less than Idle Min Continuous (IMNC) time must be reached for a frequency Increase BMXC BMXA IMNC 0 0 0 : no metric enabled 0 0 1 : IMNC metric enabled (0 % val) 0 1 0 : BMXA metric enabled (90 % val) 0 1 1 : reserved 1 0 0 : BMXC metric enabled (10 % val) 1 0 1 : reserved 1 1 0 : reserved 1 1 1 : reserved pmcr_freq_inc_utimet[2:0]</p>
2:0	<p>Frequency Decrease Utilization Metric Selection</p> <p>Access:</p> <p>The selection of a metric below indicates which one is to be used in making decision. All the metrics should be Less than Busy Min Continuous must be reached for a frequency decrease Less than Busy Min Average at end of Evaluation Interval must be reached for a frequency decrease More than Idle Max Continuous must be reached for a frequency decrease BMNC BMNA IMXC 0 0 0 : no metric enabled 0 0 1 : IMXC metric enabled (0 % val) 0 1 0 : BMNA metric enabled (100 % val) 0 1 1 : reserved 1 0 0 : BMNC metric enabled (0% val) 1 0 1 : reserved 1 1 0 : reserved 1 1 1 : reserved pmcr_freq_dec_utimet[2:0]</p>

Render Mode Register for Software Interface

MI_MODE - Render Mode Register for Software Interface									
Register Space:	MMIO: 0/2/0								
Project:	CHV, BSW								
Source:	RenderCS								
Default Value:	0x00000000								
Access:	R/W								
Size (in bits):	32								
Address:	0209Ch								
Address:	1209Ch-1209Fh								
Name:	Mode Register for Software Interface								
ShortName:	MI_MODE_VCSUNIT0								
Address:	1A09Ch-1A09Fh								
Name:	Mode Register for Software Interface								
ShortName:	MI_MODE_VECSUNIT								
Address:	1C09Ch-1C09Fh								
Name:	Mode Register for Software Interface								
ShortName:	MI_MODE_VCSUNIT1								
Address:	2209Ch-2209Fh								
Name:	Mode Register for Software Interface								
ShortName:	MI_MODE_BCSUNIT								
The MI_MODE register contains information that controls software interface aspects of the Memory Interface function.									
DWord	Bit	Description							
0	31:16	Masks							
		<table border="1"> <tr> <td>Format:</td> <td>Mask[15:0]</td> </tr> </table> <p>A 1 in a bit in this field allows the modification of the corresponding bit in Bits 15:0</p>	Format:	Mask[15:0]					
Format:	Mask[15:0]								
15		Suspend Flush							
		<table border="1"> <tr> <td>Format:</td> <td>U1</td> </tr> </table>	Format:	U1					
		Format:	U1						
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>No Delay [Default]</td> <td>HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well</td> </tr> <tr> <td>1h</td> <td>Delay Flush</td> <td>Suspend flush is active</td> </tr> </tbody> </table>	Value	Name	Description	0h	No Delay [Default]	HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well	1h
Value	Name	Description							
0h	No Delay [Default]	HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well							
1h	Delay Flush	Suspend flush is active							

MI_MODE - Render Mode Register for Software Interface

	Programming Notes	
	This should only be written to from the ring using MI_SUSPEND_FLUSH. It is considered undefined if written by software through MMIO	
14	Async Flip Performance mode	
	Format:	U1
	Value	Name
	Description	
	0h	Performance mode enabled [Default]
	1h	Performance mode disabled
		The stall of the flip event is in the windower
		The stall of the flip event is in the command stream
	Programming Notes	
	This bit must be set to '1' on all projects disabling Async Flip Performance mode.	
	When Async Flip Performance mode is enabled stall is in the Windower allowing the commands following the MI_WAIT_FOR_EVENT to be parsed by command streamer, this breaks the usage model of controlling the display message generation in display engine using MI_LOAD_REGISTER_IMMEDIATE commands from ring buffer.	
13	Flush Performance mode	
	Format:	U1
	Value	Name
	Description	
	0h	run fast restore [Default]
	1h	run slow legacy restore
		No NonPipelined SV flush.
		With NonPipelined SV flush.
12	Reserved	
	Format:	MBZ
11	Invalidate UHPTR enable	
	Format:	Enable
	If bit set H/W clears the valid bit of UHPTR (2134h, bit 0) when current active head pointer is equal to UHPTR.	
10	Atomic Read Return for MI_COPY_MEM_MEM	
	Project:	CHV, BSW
	Format:	U1
	Value	Name
	Description	
	0h	Disable [Default]
	1h	Enable
		Hardware does a regular memory fence write to complete the write to the destination address before moving to the next instruction.
		Hardware does Atomic Move with Read Return to complete the write to the destination address before moving to the next instruction.

MI_MODE - Render Mode Register for Software Interface

9	Rings Idle	
	Format:	U1
	Read Only Status bit	
	Value	Name Description
	0h	Not Idle [Default] Parser not Idle or Ring Arbiter not Idle.
1h	Idle Parser Idle and Ring Arbiter Idle.	
Programming Notes		
Writes to this bit are not allowed.		
8	Stop Rings	
	Format:	U1
	Value	Name Description
	0h	[Default] Normal Operation.
	1h	Parser is turned off and Ring arbitration is turned off.
Programming Notes		
Software must set this bit to force the Rings and Command Parser to Idle. Software must read a 1 in the Ring Idle bit after setting this bit to ensure that the hardware is idle.		
Software must clear this bit for Rings to resume normal operation.		
Due to known HW issue when Stop Rings occur during execution of a batch buffer, memory access type of the batch buffer is reset and hence on resuming the memory access type can be inconsistent with the desired memory access type. SW must not set/reset Stop Rings to achieve stall and resume function in command streamer execution, however Stop Rings can be used by SW before resetting the engine.		
7	Reserved	
	Format:	MBZ
6	Vertex Shader Timer Dispatch Enable	
	Project:	CHV, BSW
	Format:	Enable
	Value	Name Description
	0h	Disable [Default] Disable the timer for dispatch of single vertices from the vertex shader. Vertex shader will try to collect 2 vertices before a dispatch
1h	Enable Enable the timer for dispatch of single vertices. Dispatch a single vertex shader thread after the timer expires.	
5	Reserved	
	Format:	MBZ

MI_MODE - Render Mode Register for Software Interface

4:1	Predicate Enable	
	Project:	CHV, BSW
	This field gets set when "MI_SET_PREDICATE" command is parsed by render command streamer. Predicate Disable is the default mode of operation.	
	Value	Name
		Description
	0h	Predicate Disable Predication is Disabled and RCS will process commands as usual.
	1h	Predicate on Result2 clear Following Commands will be NOOPED by RCS only if the MI_PREDICATE_RESULT_2 is clear.
	2h	Predicate on Result2 set Following Commands will be NOOPED by RCS only if the MI_PREDICATE_RESULT_2 is set.
	3h	Predicate on Result clear Following Commands will be NOOPED by RCS only if the MI_PREDICATE_RESULT is clear.
	4h	Predicate on Result set Following Commands will be NOOPED by RCS only if the MI_PREDICATE_RESULT is set.
	5h	Predicate when two or more slices enabled Following Commands will be NOOPED by RCS only when one slice is enabled, NOOPED when more than one slice is enabled.
	6h	Predicate when one or three slices enabled Following Commands will be Executed by RCS only when two slices are enabled, NOOPED when one or three slices are enabled.
	7h	Predicate when one or two slices enabled Following Commands will be Executed by RCS only when all the three slices are enabled, NOOPED when less than three slices are enabled.
	8h-Eh	Reserved
	Fh	Predicate Always Following Commands will be NOOPED by RCS unconditionally.
	Programming Notes	
	SW must use MI_SET_PREDICATE instead of MMIO access.	
0	Mask IIR disable	
	Format:	Disable
	Mask IIR disable. Nominally the Interrupt controller masks interrupts in the IIR register if an interrupt acknowledge from the 3gio interface is pending. Setting this bit to a 1 allows interrupts to be visible to the interrupt controller while an interrupt acknowledge is pending.	

Render Performance Status 1

RPSTAT1 - Render Performance Status 1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A01Ch-0A01Fh	
This register reflects real-time values and thus will not have a pre-determined default value out of reset.		
DWord	Bit	Description
0	31:16	Reserved Access: <input type="text"/> RO
	15	Last Requested Video Turbo Mode Access: <input type="text"/> RO Last Requested Video Turbo Mode (CRTM): 0 = Most recent request was a normal request (from RPNSWREQ) 1 = Most recent request was a Video Turbo request (from RPVSWREQ)
	14:8	Reserved Access: <input type="text"/> RO
	7:0	Reserved Access: <input type="text"/> RO

Render Performance Status Register

RP_STATUS0 - Render Performance Status Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A01Ch			
This register reflects real-time values and thus does not have a pre-determined default value out of reset.				
DWord	Bit	Description		
0	31:20	Reserved Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td style="width: 50px; text-align: center;">RO</td></tr></table>		RO
		RO		
	19:18	Current Actual Gear Ratio Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td style="width: 50px; text-align: center;">RO</td></tr></table>		RO
		RO		
	17:16	Previous Actual Gear Ratio Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td style="width: 50px; text-align: center;">RO</td></tr></table> Previous Actual Gear Ratio (PAGR).		RO
		RO		
	15	Last Requested Video Turbo Mode Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td style="width: 50px; text-align: center;">RO</td></tr></table> Last Requested Video Turbo Mode (CRTM): 0 = Most recent request was a normal request (from RPNSWREQ). 1 = Most recent request was a Video Turbo request (from RPVSWREQ).		RO
	RO			
14	Reserved Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td style="width: 50px; text-align: center;">RO</td></tr></table>		RO	
	RO			
13:7	Current Actual GFX Freq Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td style="width: 50px; text-align: center;">RO</td></tr></table> This is the MLC ratio that the core is actually running.		RO	
	RO			
6:0	Previous Actual GFX Freq Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td style="width: 50px; text-align: center;">RO</td></tr></table> This is the MLC ratio that the core was actually running before the current actual GFX frequency.		RO	
	RO			

Render Power Clock State Register

R_PWR_CLK_STATE - Render Power Clock State Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000288 CHV, BSW
Access:	R/W
Size (in bits):	32
Address:	020C8h
<p>This register contains the mode selection for configuring render engine to attain desired performance and power requirements for a given context. This register is render context save/restored. This register must be initialized correctly when the context is submitted for the first time. This register is context save/restored as part of Exec-List context image in both Exec-List and Ring-Buffer mode of scheduling. This register contents are valid only when "Enable" bit [31] of the register is set.</p>	
Programming Notes	
<p>This register must not be programmed directly through CPU MMIO cycle. Exec-List Scheduling Mode: Every context can have its own required render engine configuration by programming this register appropriately in the logical render context image in memory (LRCA) before submitting the context to the execlist submit port. This register must not be programmed using MI_LOAD_REGISTER_IMM command in ring buffer or in batch buffer, however programming "NON-SLM Indication" field through MI_LOAD_REGISTER_IMM is an exception defined below. If a need arises to change the render configuration for a context being executed in HW, Scheduler must preempt the context and update the desired render configuration in the logical render context image in memory and resubmit the context. Only "NON-SLM Indictaion" field in R_PWR_CLK_STATE register is allowed to be modified through MI_LOAD_REGISTER_IMM command in ring_buffer or privileged_batch_buffer. SW must modify only "NON-SLM Indication" field and must ensure to program other fields with the same value as in LRCA. SW must ensure to program PIPECONTROL flush command with CS Stall and HDC Flush prior to programming MI_LOAD_REGISTER_IMM command to modify "NON-SLM Indication" in R_PWR_CLK_STATE register. Example: //R_PWR_CLK_STATE register value in LRCA configured with two slices and NON-SLM indication reset: 0x80005_0000 //SW desires to set NON-SLM Indication filed in ring buffer MI_LOAD_REGISTER_IMM 0x20C8, 0x8005_0100 Ring Buffer Scheduling: This register must be programmed using MI_LOAD_REGISTER_IMM command in the ring buffer. When this register is being programmed to re-configure the number of slices, SW must context save the state before programming this register and restore the state after programming the register via dummy MI_SET_CONTEXT command, this will ensure the existing state is programmed to all the new slices that are powered up, in case of slice shutdown this is not required. EX: MI_SET_CONTEXT → CXTA MI_BATCH_BUFFER_START MI_BATCH_BUFFER_START MI_SET_CONTEXT → CXTB //Dummy Context to save existing render state to be restored latter. MI_LOAD_REGISTER_IMM : R_PWR_CLK_STATE (1 Slice to 3 Slices) // Slice configuration done. MI_SET_CONTEXT → CXTA // Context restore of valid state to all the slices powered up.</p>	

Render Power Meter Counter

RPMCNT - Render Power Meter Counter		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A274h-0A277h	
DWord	Bit	Description
0	31	Render Power Meter Counter Overflow Access: <input type="text"/> RO
	30:0	Render PWRMTR Counter Access: <input type="text"/> RO

Render Power Meter Counter No Clear

RPMCNTCLR - Render Power Meter Counter No Clear			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A28Ch-0A28Fh		
Formerly cleared the count and the overflow bit, but now it is just a read-only value.			
DWord	Bit	Description	
0	31	Render Power Meter Counter Overflow No Clear Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>RO</td></tr></table> Formerly cleared the overflow bit, but now it is just a read-only value.	RO
	RO		
30:0	Render PWRMTR Counter No Clear Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>RO</td></tr></table> Formerly cleared the count, but now is just a read-only value.	RO	
RO			

Render Promotion Timer - RC6

RC6TIMER - Render Promotion Timer - RC6				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A0B8h-0A0BBh			
DWord	Bit	Description		
0	31:24	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
23:0	RC6 Promote Time <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Absolute time starting from post-hyst idle.</p> <p>0 = 0 usec 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec pmcr_rc6_promotion_time[23:0]</p>	Access:	R/W	
Access:	R/W			

RENDERRCOCOUNTER

RENDERRCOCOUNTER - RENDERRCOCOUNTER						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	138118h					
<p>This register contains the total RC0 residency (Render powered on and clocks running) time that Render was in since boot.</p> <p>SOXi Context Save/Restore : No</p> <p>The 40-bit HW counter will wrap around. The only clear condition is CZ reset.</p> <p>When 0x13_8104[15] is set to zero, bits 31:0 of the 40-bit counter are reported. When 0x13_8104[15] is set to one, bits 39:8 of the 40-bit counter are reported.</p> <p>The units are CZ clock cycles.</p> <p>It is up to SW to periodically read this register and do a difference from the last time it was read. The primary usage for this register is for power characterization.</p> <p>0x13_8104[4] controls if this register should count or if it should be gated: 0= clear, 1=count</p>						
DWord	Bit	Description				
0	31:0	<p>RENDERRCOTIME</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Render RC0 Residency Counter.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

RENDERRC1COUNTER

RENDERRC1COUNTER - RENDERRC1COUNTER						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	138110h					
<p>This register contains the total RC1 residency (Render powered on and clock gated) time that Render was in since boot.</p> <p>SOXi Context Save/Restore : No</p> <p>The 40-bit HW counter will wrap around. The only clear condition is CZ reset.</p> <p>When 0x13_8104[15] is set to zero, bits 31:0 of the 40-bit counter are reported. When 0x13_8104[15] is set to one, bits 39:8 of the 40-bit counter are reported.</p> <p>The units are CZ clock cycles.</p> <p>It is up to SW to periodically read this register and do a difference from the last time it was read. The primary usage for this register is for power characterization.</p> <p>0x13_8104[2] controls if this register should count or if it should be gated: 0= clear, 1=count</p>						
DWord	Bit	Description				
0	31:0	<p>RENDERRC1TIME</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Render RC1 Residency Counter.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

RENDERRC6COUNTER

RENDERRC6COUNTER - RENDERRC6COUNTER						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	138108h					
<p>This register contains the total RC6 residency (Render power gated and clock gated) time that Render power well was in since boot. The counter will wrap around.</p> <p>SOXi Context Save/Restore : No</p> <p>The time is given in units of CZ clock cycles. The counter will reset on CZ reset going high.</p> <p>This means that a warm reset will also reset this counter and it will also wrap around when it reaches max with no indication that an overflow occurred.</p> <p>This register will freeze the count value (stop counting, but not reset) when pmu_gvd_renwakeack_nczfwoh=1.</p> <p>This register will count whenever pmu_gvd_renwakeack_nczfwoh=0.</p> <p>When 0x13_8104[15] is set to zero, bits 31:0 of the 40-bit counter are reported. When 0x13_8104[15] is set to one, bits 39:8 of the 40-bit counter are reported.</p> <p>The units are CZ clock cycles.</p> <p>It is up to SW to periodically read this register and do a difference from the last time it was read. The primary usage for this register is for power characterization.</p> <p>0x13_8104[0] controls if this register should count or if it should be gated: 0= clear, 1=count.</p>						
DWord	Bit	Description				
0	31:0	<p>RENDERRC6TIME</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Render Residency Counter.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Render TLB Control Register

RTCR - Render TLB Control Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	04260h			
DWord	Bit	Description		
0	31:1	Reserved		
		<table border="1"> <tr> <td>Default Value:</td> <td>00000000000000000000000000000000b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	00000000000000000000000000000000b
Default Value:	00000000000000000000000000000000b			
Access:	RO			
0	0	Invalidate TLBs on the corresponding Engine		
		<table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. This bit is self clear.</p>	Default Value:	0b
Default Value:	0b			
Access:	R/W			

Render Watchdog Counter

PR_CTR - Render Watchdog Counter				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	RenderCS			
Default Value:	0x00000000			
Access:	RO			
Size (in bits):	32			
Address:	02190h			
Address:	12190h-12193h			
Name:	Watchdog Counter			
ShortName:	PR_CTR_VCSUNIT0			
Address:	1A190h-1A193h			
Name:	Watchdog Counter			
ShortName:	PR_CTR_VECSUNIT			
Address:	1C190h-1C193h			
Name:	Watchdog Counter			
ShortName:	PR_CTR_VCSUNIT1			
Address:	22190h-22193h			
Name:	Watchdog Counter			
ShortName:	PR_CTR_BCSUNIT			
DWord	Bit	Description		
0	31:0	<p>Counter Value</p> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>This register reflects the render watchdog counter value itself. It cannot be written to.</p>	Format:	U32
Format:	U32			

Render Watchdog Counter Threshold

PR_CTR_THRSH - Render Watchdog Counter Threshold						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	RenderCS					
Default Value:	0x00150000					
Access:	R/W					
Size (in bits):	32					
Address:	0217Ch					
Address:	1217Ch-1217Fh					
Name:	Watchdog Counter Threshold					
ShortName:	PR_CTR_THRSH_VCSUNIT0					
Address:	1A17Ch-1A17Fh					
Name:	Watchdog Counter Threshold					
ShortName:	PR_CTR_THRSH_VECSUNIT					
Address:	1C17Ch-1C17Fh					
Name:	Watchdog Counter Threshold					
ShortName:	PR_CTR_THRSH_VCSUNIT1					
Address:	2217Ch-2217Fh					
Name:	Watchdog Counter Threshold					
ShortName:	PR_CTR_THRSH_BCSUNIT					
DWord	Bit	Description				
0	31:0	<p>Counter logic Threshold</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Default Value:</td> <td>00150000h</td> </tr> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>This field specifies the threshold that the hardware checks against for the value of the render clock counter before generating an interrupt. The counter in hardware generates an interrupt when the threshold is reached, rolls over and starts counting again. The interrupt generated is the "Media Hang Notify" interrupt since this watchdog timer is intended primarily to remedy VLD hangs on the main pipeline.</p>	Default Value:	00150000h	Format:	U32
Default Value:	00150000h					
Format:	U32					

Reported BitRateControl parameter Mask

MFX_VP8_CNTRL_MASK - Reported BitRateControl parameter Mask		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	12900h	
Valid Projects:	CHV, BSW	
This register stores the count of bytes of the bitstream output per frame		
DWord	Bit	Description
0	31:6	Reserved
		Format: MBZ
	5	Final Bitstream Buffer Overrun Mask Format: U1 This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit5. This denotes Final bitstream buffer overrun feature is enabled.
	4	Intermediate Bitstream Buffer Overrun Mask Format: U1 This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit4. This denotes intermediate bitstream buffer overrun feature is enabled.
	3	Intra MB Bit Count Conformance Mask Format: U1 This is legacy support as AVC for Intra MB Bit Count conformance. This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit3. This feature is not validated.
2	Inter MB Bit Count Conformance Mask Format: U1 This is legacy support as AVC for Inter MB Bit Count conformance. This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit2. This feature is not validated.	

MFX_VP8_CNTRL_MASK - Reported BitRateControl parameter Mask

1	<p>Frame Bit Rate Overflow Mask</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U1</td> </tr> </table> <p>This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit0. It denotes if Frame Bit Rate Overflow is enabled for Bit Rate Control</p>	Format:	U1
Format:	U1		
0	<p>Frame Bit Rate Underflow Mask</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U1</td> </tr> </table> <p>This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit1. It denotes if Frame Bit Rate Underflow is enabled for Bit Rate Control</p>	Format:	U1
Format:	U1		

Reported BitRateControl parameter Status

MFX_VP8_CNTRL_STATUS - Reported BitRateControl parameter Status		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	12904h	
Valid Projects:	CHV, BSW	
This register stores the count of bytes of the bitstream output per frame		
DWord	Bit	Description
0	31:8	Reserved Format: MBZ
	7	QindexClampHigh Status Format: U1 This denotes if Qindex is clamped by QindexClampHigh value programmed in MFX_VP8_PIC_STATE.DW7.
	6	QindexClampLow Status Format: U1 This denotes if Qindex is clamped by QindexClampLow value programmed in MFX_VP8_PIC_STATE.DW7.
	5	Final Bitstream Buffer Overrun Status Format: U1 This denotes if Final bitstream buffer overrun.
	4	Intermediate Bitstream Buffer Overrun Status Format: U1 This denotes if any of the Intermediate bitstream buffer overrun. (including FrameHeader, Partition1 to Partition8)
	3	Intra MB Bit Count Conformance Status Format: U1 This is legacy support as AVC for Intra MB Bit Count conformance. It denotes if Intra MB Bit Count meets conformance size. This feature is not validated.

MFX_VP8_CNTRL_STATUS - Reported BitRateControl parameter Status

2	<p>Inter MB Bit Count Conformance Status</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U1</td> </tr> </table> <p>This is legacy support as AVC for Inter MB Bit Count conformance. It denotes if Inter MB Bit Count meets conformance size. This feature is not validated.</p>	Format:	U1
Format:	U1		
1	<p>Frame Bit Rate Overflow Status</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U1</td> </tr> </table> <p>It denotes if Frame Bit Rate Overflow in current frame</p>	Format:	U1
Format:	U1		
0	<p>Frame Bit Rate Underflow Status</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U1</td> </tr> </table> <p>It denotes if Frame Bit Rate Underflow in current frame</p>	Format:	U1
Format:	U1		

Reported Bitstream Output Bit Count for Syntax Elements Only Register

MFC_BITSTREAM_SE_BITCOUNT_FRAME - Reported Bitstream Output Bit Count for Syntax Elements Only Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	128A4h	
Valid Projects:	CHV, BSW	
<p>This register stores the count of number of bits in the bitstream due to syntax elements only. This excludes header/ byte alignment /tail/EMU/CABAC-0word/padding bits but includes the stop-one-bit. This register is part of the context save and restore.</p>		
DWord	Bit	Description
0	31:0	<p>MFC Bitstream Syntax Element Only Bit Count Total number of bits in the bitstream output due to syntax elements only. It includes the data bytes only. This count is updated for every time the internal bitstream counter is incremented and its reset at image start.</p>

Reported Bitstream Output Byte Count per Frame Register

MFC_BITSTREAM_BYTECOUNT_FRAME - Reported Bitstream Output Byte Count per Frame Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	128A0h	
Valid Projects:	CHV, BSW	
This register stores the count of bytes of the bitstream output per frame		
DWord	Bit	Description
0	31:0	<p>MFC Bitstream Byte Count per Frame</p> <p>Total number of bytes in the bitstream output per frame from the encoder. This includes header/tail/byte alignment/data bytes/EMU (emulation) bytes/cabac-zero word insertion/padding insertion. This count is updated for every time the internal bitstream counter is incremented and its reset at image start.</p>

Reported Bitstream Output CABAC Bin Count Register

MFC_AVC_CABAC_BIN_COUNT_FRAME - Reported Bitstream Output CABAC Bin Count Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	128A8h	
Valid Projects:	CHV, BSW	
This register stores the count of number of bins per frame.		
DWord	Bit	Description
0	31:0	MFC AVC Cabac Bin Count Total number of BINs in the bitstream output per frame from the encoder. This count is updated for every time the bin counter is incremented and its reset at image start.

Reported Final Bitstream Byte Count

MFX_VP8_FRM_BYTE_CNT - Reported Final Bitstream Byte Count				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoCS			
Default Value:	0x00000000			
Access:	RO			
Size (in bits):	32			
Trusted Type:	1			
Address:	12908h			
Valid Projects:	CHV, BSW			
This register stores the count of bytes of the bitstream output per frame				
DWord	Bit	Description		
0	31:0	Final BitStream Byte Count <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> This register contains Final Bitstream byte count	Format:	U32
Format:	U32			

Reported Frame Zero Padding Byte Count

MFX_VP8_FRM_ZERO_PAD - Reported Frame Zero Padding Byte Count				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoCS			
Default Value:	0x00000000			
Access:	RO			
Size (in bits):	32			
Trusted Type:	1			
Address:	1290Ch			
Valid Projects:	CHV, BSW			
This register stores Frame Zero Padding Byte Count				
DWord	Bit	Description		
0	31:16	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
15:0	Frame Zero Padding Byte Count <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">U16</td> </tr> </table> <p>This register contains Frame Zero Padding byte count This is legacy support. This feature is not validated.</p>	Format:	U16	
Format:	U16			

Reported Timestamp Count

TIMESTAMP - Reported Timestamp Count	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000h, 00000000 CHV, BSW
Access:	RO. This register is not set by the context restore.
Size (in bits):	64
Address:	02358h
Address:	12358h-1235Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VCSUNIT0
Address:	1A358h-1A35Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VECSUNIT
Address:	1C358h-1C35Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VCSUNIT1
Address:	22358h-2235Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_BCSUNIT
Description	
<p>This register provides an elapsed real-time value that can be used as a timestamp for GPU events over short periods of time. Note that the value of this register can be obtained in a 3D pipeline-synchronous fashion without a pipeline flush by using the PIPE_CONTROL command. See 3D Geometry Pipeline in the "3D and Media" volume. This register (effectively) counts at a constant frequency by adjusting the increment amount according to the actual reference clock frequency. SW therefore does not need to know the reference clock frequency. This register is not reset by a graphics reset. It will maintain its value unless a full chipset reset is performed.</p>	
<p>Note: On Core platforms, the TIMESTAMP register is initialized with the value of the PCU ART and hence tracks bits 38:3 of the 100 MHz ART fairly closely. However, due to variability in the actual time it takes to download the ART value to GT, the value of the TIMESTAMP register will be lower than the value of the PCU ART by an amount dependent on the relative IA/CLR/GT frequencies at the time the timestamp was downloaded to GT (expected to range between 100 and 600 ns). When comparing the value sampled from this register by GT HW to values read from the PCU timer by other system agents, timing differences between GT HW reading the TIMESTAMP register and the involved non-GT agent(s) reading the PCU ART must also be comprehended.</p>	

TIMESTAMP - Reported Timestamp Count		
DWord	Bit	Description
0	63:36	Reserved
		Project: CHV, BSW
		Format: MBZ
	35:0	Timestamp Value
		Project: CHV, BSW
		Format: U36
Description		
This register toggles based on time stamp granularity (base unit) defined in the "Time Stamp Bases" subsection in Power Management chapter.		

Reset Flow Control Messages

RSTFCTLMSG - Reset Flow Control Messages				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	08108h			
Soft-Reset and FLR Flow Control Message Registers				
DWord	Bit	Description		
0	31:16	<p>Message Mask</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000</p>	Access:	RO
	Access:	RO		
	15:12	Reserved		
	11	<p>MEDIA 1 Reset flow acknowledgement message</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>PM Acknowledgement Messages for Media 1 reset: '1' : PREP_RST_MEDIA1_ACK - Acknowledgement that graphics media1 (or 2nd vbox) is prepared for reset assertion. '0' : DONE_MEDIA1_RST_ACK - Acknowledgement that graphics media1 (or 2nd vbox) reset is de-asserted</p>	Access:	R/W
	Access:	R/W		
10	<p>WIDI Reset flow acknowledgement message</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>PM Acknowledgement Messages for WIDI reset: '1' : PREP_RST_WIDI_ACK - Acknowledgement that graphics widi is prepared for reset assertion. '0' : DONE_WIDI_RST_ACK - Acknowledgement that graphics widi reset is de-asserted</p>	Access:	R/W	
Access:	R/W			
9	Reserved			
8	<p>Vebox Reset flow Acknowledge Message</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>PM Acknowledgement Messages for Vebox reset: '1' : PREP_RST_VEBOX_ACK - Acknowledgement that graphics VE is prepared for reset assertion. '0' : DONE_VEBOX_RST_ACK - Acknowledgement that graphics VE reset is de-asserted</p>	Access:	R/W	
Access:	R/W			

RSTFCTLMSG - Reset Flow Control Messages

7	<p>Blitter Reset Flow Acknowledgement Messages</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>PM Acknowledgement Messages for Blitter reset: '1' : PREP_RST_BLIT_ACK - Acknowledgement that graphics blitter is prepared for reset assertion. '0' : DONE_BLIT_RST_ACK - Acknowledgement that graphics blitter reset is de-asserted</p>	Access:	R/W
Access:	R/W		
6	<p>Media Reset Flow Acknowledgement Messages</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>PM Acknowledgement Messages for Media reset: '1' : PREP_RST_MEDIA_ACK - Acknowledgement that graphics media block is prepared for reset assertion. '0' : DONE_MEDIA_RST_ACK - Acknowledgement that the graphics media reset is de-asserted</p>	Access:	R/W
Access:	R/W		
5	<p>Render Reset Flow Acknowledgement Messages</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>PM Acknowledgement Messages for Render reset: '1' : PREP_RST_RENDER_ACK - Acknowledgement that the graphics render block is prepared for reset assertion. '0' : DONE_RENDER_RST_ACK - Acknowledgement that the graphics render reset is de-asserted</p>	Access:	R/W
Access:	R/W		
4	<p>GTI-Device Reset Flow Acknowledgement Messages</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>PM Acknowledgement Messages for GTI-Device reset: '1' : PREP_RST_GTIDEV_ACK - Acknowledgement that the GTI device is prepared for reset assertion. '0' : DONE_GTIDEV_RST_ACK - Acknowledgement that the GTI device reset is de-asserted</p>	Access:	R/W
Access:	R/W		
3	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">RO</td> </tr> </table> <p>Reserved</p>	Access:	RO
Access:	RO		
2	<p>FLR Done ack from Pmunit</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W Set</td> </tr> </table> <p>FLR Done ack from Pmunit: 1: PM unit sets this bit to acknowledge the FLR done message has been forwarded to SA through GAM interface. 0: Default Value. If the bit was set by PM then Cpunit hardware clears it once FLR is completed.</p>	Access:	R/W Set
Access:	R/W Set		

RSTFCTLMSG - Reset Flow Control Messages			
1	<p>Global Resource Arbitration Acknowledgement Messages</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>Global Resource Arbitration Acknowledgement Message from PM: '1' : CP_ARB_REQ_ACK - Acknowledgement for CPunit's global resource arbitration request '0' : CP_ARB_RELEASE_ACK - Acknowledgement to CPunit's release of global resources</p>	Access:	R/W
Access:	R/W		
0	<p>CP Busy / Idle Status Acknowledgement Messages</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>CP Busy / Idle Status Acknowledgement Message from PM: '0' : CP_NOT_BUSY_ACK - Acknowledgement that the CPunit is idle. '1' : CP_BUSY_ACK - Acknowledgement that the CPunit is busy.</p>	Access:	R/W
Access:	R/W		

RESET Messaging Register for Clocking Unit

MSG_RESET_GCP - RESET Messaging Register for Clocking Unit				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	16			
Address:	08030h			
<p>Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.</p> <p>Request to Prepare for Reset 1'b0 : Reset complete <default> 1'b1 : Prepare for reset</p>				
DWord	Bit	Description		
0	15:8	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	7	<p>Request to Prepare for FLR</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>[7] Prepare for devrst_b Domain Reset (FLR) Note: All resets except busrst_b will be asserted for an FLR</p>	Access:	R/W
	Access:	R/W		
	6	<p>Request to Prepare for Media1 Reset</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>[6] Prepare for cmrst_b Domain Reset (vcs1unit)</p>	Access:	R/W
	Access:	R/W		
	5	<p>Request to Prepare for Wi-Di Reset</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>[5] Prepare for cwrst_b Domain Reset (winunit)</p>	Access:	R/W
	Access:	R/W		
4	Reserved			
3	<p>Request to Prepare for Blitter Reset</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>[3] Prepare for crblitrst_b Domain Reset (bcsunit)</p>	Access:	R/W	
Access:	R/W			
2	<p>Request to Prepare for VEBox Reset</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>[2] Prepare for cvrst_b Domain Reset (vecsunit)</p>	Access:	R/W	
Access:	R/W			

MSG_RESET_GCP - RESET Messaging Register for Clocking Unit

	1	Request to Prepare for Media0 Reset	
		Access:	R/W
		[1] Prepare for cmrst_b Domain Reset (vcs0unit)	
	0	Request to Prepare for Render Reset	
		Access:	R/W
		[0] Prepare for crrst_b Domain Reset (csunit)	

Resource Streamer Context Offset

RS_CXT_OFFSET - Resource Streamer Context Offset						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	RenderCS					
Default Value:	0x00003B00					
Access:	Read/32 bit Write Only					
Size (in bits):	32					
Address:	021B4h					
DWord	Bit	Description				
0	31:6	RS Offset Format: U26 This field indicates the offset (64bytes granular) in to the logical rendering context to which Resource Streamer context is save/restored when enabled. This field register must not be written directly (via MMIO) unless the Command Streamer is completely idle (i.e., the Ring Buffer is empty and the pipeline is idle) and RC6 is disabled. On way to program this register is via Load Register Immediate command in the ring buffer as part of initialization sequence.				
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>ECh</td> <td>[Default]</td> <td>DefaultValueDesc</td> </tr> </tbody> </table>	Value	Name	Description	ECh
Value	Name	Description				
ECh	[Default]	DefaultValueDesc				
	5:0	Reserved Format: MBZ				

Resource Streamer Preemption Status

RS_PREEMPT_STATUS - Resource Streamer Preemption Status				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	RenderCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	0215Ch			
<p>Preemption from First Level Batch Buffer: This register contains the offset in to the Batch Buffer on which Resource streamer got preempted. Note that it is offset from the Batch Start Address and not the graphics address corresponding to the preempted instruction on Batch Buffer. This register's contents will be looked at by Command Streamer on the next RS Start Trigger to provide the appropriate batch start address. Following preemption, context save happens on which this register is context saved, after context save the register gets auto reset by Command Streamer. This register gets context save/restored by Render Command Streamer as part of its render context. Preemption from Second Level Batch Buffer: This register contains the graphics address of the instruction in Second Level Batch Buffer on which Resource streamer got preempted. This register's contents will be looked at by Command Streamer on the next RS Start Trigger to provide the appropriate batch start address. Following preemption, context save happens on which this register is context saved, after context save the register gets auto reset by Command Streamer. This register gets context save/restored by Render Command Streamer as part of its render context.</p>				
Programming Notes				
<ul style="list-style-type: none"> This register is accessed by Render Command Streamer as part of render context save/restore; this register should be exercised by S/W only for resetting the register contents if required. Following preemption if there is no context save, SW should program this register with 0x0 so that it does not interfere with proceeding workloads. 				
DWord	Bit	Description		
0	31:2	<p>Batch Buffer Offset</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>Offset[31:2]</td> </tr> </table> <p>This field specifies the DWord-aligned offset from the batch start address on which Resource Streamer got preempted.</p>	Format:	Offset[31:2]
	Format:	Offset[31:2]		
1	<p>RS_PREEMPT_STATUS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table> <p>This field when not set indicates RS got preempted on a natural sync point else it got preempted on a draw call.</p>	Format:	MBZ	
Format:	MBZ			

RS_PREEMPT_STATUS - Resource Streamer Preemption Status

	0	RS_PREEMPTED	
		Default Value:	0
		Format:	Enable
		If this bit is set indicates Resource Streamer got preempted. Other fields of this register are valid only when this bit is set.	

Restored Timestamp LSDW

RTSLSDW - Restored Timestamp LSDW				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A530h-0A533h			
DWord	Bit	Description		
0	31:0	Restored Time Stamp Storage <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Restored Time Stamp Storage	Access:	R/W
Access:	R/W			

Restored timestamp MSDW

RTSMSDW - Restored timestamp MSDW				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A534h-0A537h			
DWord	Bit	Description		
0	31:0	Restored Time Stamp Storage <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Restored Time Stamp Storage	Access:	R/W
Access:	R/W			

RID_CC

RID_CC - RID_CC					
Register Space:	PCI: 0/2/0				
Project:	CHV, BSW				
Source:	PRM				
Default Value:	0x00000000				
Size (in bits):	32				
Address:	00008h				
Revision Identification and Class code register. SOXi Context Save/Restore: Yes.					
DWord	Bit	Description			
0	31:24	BASE_CLASS_CODE <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
	Access:	RO			
	23:16	SUB_CLASS_CODE <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>When MGGC0[VAMEN] is 1, this value is 80h, indicating other multimedia device. When MGGC0[VAMEN] is 0 this value will be determined based on GGC register, GMS and IVD fields. When GGC[1] = 1 or GGC[7:3] = 5'b00000 this value is 80h, otherwise its 00h 00h: VGA compatible 80h: Non VGA (GMS = '00h' or IVD = '1b')</p>	Access:	RO	
	Access:	RO			
15:8	PROGRAMMING_INTERFACE <table border="1"> <tr> <td>Default Value:</td> <td>00h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	00h	Access:	RO
Default Value:	00h				
Access:	RO				
7:0	REVISION_ID <table border="1"> <tr> <td>Default Value:</td> <td>00000000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>RID: The value in this field reflects the value of strapRID[7:0] (which is an input pin of GVD). For VV: The reset value will be the same as MID bits 23:16 (reference the MID register for MID register details). This register is read-able by any agent. Under SAI protection, the PMC and Punit (ie. 'Trusted_FW') can write this register and change the default value. No other agent has the ability to update this register. The PMC implementation will consider SRID and CRID before updating this register. Any PMC updates will be prior to Device 2 configuration. Note : The MID register will always reflect the stepping information. Even if PMC updates this register, the MID is available as a SRID reference.</p>	Default Value:	00000000b	Access:	R/W
Default Value:	00000000b				
Access:	R/W				

RING_BUFFER_HEAD_PREEMPT_REG

RING_BUFFER_HEAD_PREEMPT_REG - RING_BUFFER_HEAD_PREEMPT_REG	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0214Ch-0214Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_RCSUNIT
Address:	1214Ch-1214Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT0
Address:	1A14Ch-1A14Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VECSUNIT
Address:	1C14Ch-1C14Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT1
Address:	2214Ch-2214Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_BCSUNIT
Description	
<p>This register contains the Head pointer offset in the ring when the last PREEMPTABLE command was executed and caused the head pointer to move due to the UHPTR register being valid. If the PREEMPTABLE command is executed as part of the batch buffer then the value of the register will be the offset in the ring of the command past the batch buffer start that contained the preemptable command.</p> <p>This is a global register and context save/restored as part of power context image.</p>	
Preemptable Commands	Source
<ul style="list-style-type: none"> • MI_ARB_CHECK • 3D_PRIMITIVE • GPGPU_WALKER • MEDIA_STATE_FLUSH • PIPE_CONTROL (Only in GPGPU mode of pipeline selection) 	RenderCS

RING_BUFFER_HEAD_PREEMPT_REG - RING_BUFFER_HEAD_PREEMPT_REG

- MI_ATOMIC (Post Sync Operation set in GPGPU mode of pipeline selection)
- MI_SEMAPHORE_SIGNAL (Post Sync Operation set in GPGPU mode of pipeline selection)

Programming Notes

Programming Restriction:
This register should NEVER be programmed by driver. This is for HW internal use only.

DWord	Bit	Description												
0	31:21	Last Wrap Count												
	20:2	Preempted Head Offset												
		Format: U19												
	This field contains the Head pointer offset in the ring when the last MI_ARB_CHECK command was executed and caused the head pointer to move due to the UHPTR register being valid.													
1:0	1:0	Ring/Batch Indicator												
		Format: Enabled												
	<table border="1" style="width: 100%;"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Ring</td> <td>Preemptable command was executed in ring and caused head pointer to be updated.</td> </tr> <tr> <td>1h</td> <td>Batch</td> <td>Preemptable command was executed in batch and caused head pointer to be updated.</td> </tr> <tr> <td>2h</td> <td>2nd level batch</td> <td>Preemptable command was executed in second level batch and caused head pointer to be updated.</td> </tr> </tbody> </table>		Value	Name	Description	0h	Ring	Preemptable command was executed in ring and caused head pointer to be updated.	1h	Batch	Preemptable command was executed in batch and caused head pointer to be updated.	2h	2nd level batch	Preemptable command was executed in second level batch and caused head pointer to be updated.
	Value	Name	Description											
0h	Ring	Preemptable command was executed in ring and caused head pointer to be updated.												
1h	Batch	Preemptable command was executed in batch and caused head pointer to be updated.												
2h	2nd level batch	Preemptable command was executed in second level batch and caused head pointer to be updated.												

Ring Buffer Control

RING_BUFFER_CTL - Ring Buffer Control			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Address:	0203Ch-0203Fh		
Name:	Ring Buffer Control		
ShortName:	RING_BUFFER_CTL_RCSUNIT		
Address:	1203Ch-1203Fh		
Name:	Ring Buffer Control		
ShortName:	RING_BUFFER_CTL_VCSUNIT0		
Address:	1A03Ch-1A03Fh		
Name:	Ring Buffer Control		
ShortName:	RING_BUFFER_CTL_VECSUNIT		
Address:	1C03Ch-1C03Fh		
Name:	Ring Buffer Control		
ShortName:	RING_BUFFER_CTL_VCSUNIT1		
Address:	2203Ch-2203Fh		
Name:	Ring Buffer Control		
ShortName:	RING_BUFFER_CTL_BCSUNIT		
Description	Source		
These registers are used to define and operate the ring buffer mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a physical memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. Refer to the Programming Interface chapter for a detailed description of the parameters specified in this ring buffer register set, restrictions on the placement of ring buffer memory, arbitration rules, and in how the ring buffer can be used to pass instructions.	RenderCS		
Ring Buffer Head and Tail Offsets must be properly programmed before it is enabled. A Ring Buffer can be enabled when empty.	BlitterCS, VideoCS, VideoEnhancementCS		
DWord	Bit	Description	
0	31:21	Reserved Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td> </td></tr></table> MBZ	
20:12	Buffer Length		

RING_BUFFER_CTL - Ring Buffer Control

Format:		U9-1 in 4 KB pages - 1	
This field is written by SW to specify the length of the ring buffer in 4 KB Pages. Range = [0 = 1 page = 4 KB, 1FFh = 512 pages = 2 MB]			
Value	Name	Description	
0		1 page = 4 KB	
1FFh		512 pages = 2 MB	
11	RBWait		
Description			Source
Indicates that this ring has executed a WAIT_FOR_EVENT instruction and is currently waiting. Software can write a "1" to clear this bit, write of "0" has no effect. When the RB is waiting for an event and this bit is cleared, the wait will be terminated and the RB will be returned to arbitration.			
RenderCS: RBWait is not set on executing WAIT_FOR_EVENT instruction waiting on Async Flip Pending.			RenderCS
10	Semaphore Wait		
Description			
Indicates that this ring has executed a MI_SEMAPHORE_WAIT instruction and is currently waiting for wait condition to satisfy.			
9	Reserved		
Format:		MBZ	
8	Reserved		
Project:		CHV, BSW	
Format:		MBZ	
7:3	Reserved		
Format:		MBZ	
2:1	Automatic Report Head Pointer		
Project:		CHV, BSW	
Source:		PRM	
Description			
This field is written by software to control the automatic reporting (write) of this ring buffer's Head Pointer register (register DWord 1) to the corresponding location within the Hardware Status Page. Automatic reporting can either be disabled or enabled at 4KB, 64KB or 128KB boundaries within the ring buffer.			
When Execlist Enable bit is set the head pointer will be reported to the head pointer location in the Per-Process Hardware Status Page. MI_AUTOREPORT_4KB option is not supported on A stepping.			

RING_BUFFER_CTL - Ring Buffer Control

	Value	Name	Description								
	0	MI_AUTOREPORT_OFF	Automatic reporting disabled								
	1	MI_AUTOREPORT_64KB	Report every 16 pages (64KB)								
	2	MI_AUTOREPORT_4KB	Report every page (4KB) This mode must not be enabled in Ring Buffer mode of scheduling to minimize the auto reports.								
	2	MI_AUTOREPORT_4KB	Report every page (4KB) This mode must not be enabled in Ring Buffer mode of scheduling to minimize the auto reports.								
	3	MI_AUTOREPORT_128KB	Report every 32 pages (128KB)								
0	Ring Buffer Enable <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field is used to enable or disable this ring buffer. It can be enabled or disabled regardless of whether there are valid instructions pending. If disabled and the ring head equals ring tail, all state currently loaded in hardware is considered invalid.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 80%;">Programming Notes</th> <th style="width: 20%;">Source</th> </tr> </thead> <tbody> <tr> <td> Ring Buffer Mode of Scheduling: SW must follow the below programming notes during SW initialization phase or while enabling render engine's ring buffer for the first time, this would be coming out of boot, standby, hibernate or reset. SW must set the Force Wakeup bit to prevent GT from entering C6. <ul style="list-style-type: none"> SW must dispatch workload (dummy context) to initialize render engine with default state such that any context switches that occur subsequently (Power Save) will save and restore coherent device state. Indirect pointers used in 3D states must point to valid graphics surface existing in memory. PP_DCLV followed by PP_DIR_BASE register should be programmed as part of initialization workload if PPGTT is enabled in GFX_MODE register. SW must ensure all the register (MMIO) initialization/programming through CPU happens in this block or latter, this ensures the MMIO state is save/restored on subsequent context switches (Power Sequences). Once the render engine is programmed with valid state and the configuration, Force Wakeup bit should be reset to enable C6 entry. </td> <td>RenderCS</td> </tr> <tr> <td> Render CS Only: Ring Buffer Mode of Scheduling: SW must follow the below programming notes before disabling ring buffer to ensure HW is not in middle of the IDLE flows. <ul style="list-style-type: none"> SW must set the Force Wakeup bit to prevent GT from entering C6. Disable IDLE messaging in CS (Write 0x2050[31:0] = 0x00010001) Poll/Wait for register bits of <u>0x22AC[6:0]</u> turn to 0x30 value. Disable Ring Buffer Enable IDLE messaging in CS (Write 0x2050[31:0] = 0x00010000) Force Wakeup bit should be reset to enable C6 entry. </td> <td>RenderCS</td> </tr> </tbody> </table>			Format:	Enable	Programming Notes	Source	Ring Buffer Mode of Scheduling: SW must follow the below programming notes during SW initialization phase or while enabling render engine's ring buffer for the first time, this would be coming out of boot, standby, hibernate or reset. SW must set the Force Wakeup bit to prevent GT from entering C6. <ul style="list-style-type: none"> SW must dispatch workload (dummy context) to initialize render engine with default state such that any context switches that occur subsequently (Power Save) will save and restore coherent device state. Indirect pointers used in 3D states must point to valid graphics surface existing in memory. PP_DCLV followed by PP_DIR_BASE register should be programmed as part of initialization workload if PPGTT is enabled in GFX_MODE register. SW must ensure all the register (MMIO) initialization/programming through CPU happens in this block or latter, this ensures the MMIO state is save/restored on subsequent context switches (Power Sequences). Once the render engine is programmed with valid state and the configuration, Force Wakeup bit should be reset to enable C6 entry. 	RenderCS	Render CS Only: Ring Buffer Mode of Scheduling: SW must follow the below programming notes before disabling ring buffer to ensure HW is not in middle of the IDLE flows. <ul style="list-style-type: none"> SW must set the Force Wakeup bit to prevent GT from entering C6. Disable IDLE messaging in CS (Write 0x2050[31:0] = 0x00010001) Poll/Wait for register bits of <u>0x22AC[6:0]</u> turn to 0x30 value. Disable Ring Buffer Enable IDLE messaging in CS (Write 0x2050[31:0] = 0x00010000) Force Wakeup bit should be reset to enable C6 entry. 	RenderCS
Format:	Enable										
Programming Notes	Source										
Ring Buffer Mode of Scheduling: SW must follow the below programming notes during SW initialization phase or while enabling render engine's ring buffer for the first time, this would be coming out of boot, standby, hibernate or reset. SW must set the Force Wakeup bit to prevent GT from entering C6. <ul style="list-style-type: none"> SW must dispatch workload (dummy context) to initialize render engine with default state such that any context switches that occur subsequently (Power Save) will save and restore coherent device state. Indirect pointers used in 3D states must point to valid graphics surface existing in memory. PP_DCLV followed by PP_DIR_BASE register should be programmed as part of initialization workload if PPGTT is enabled in GFX_MODE register. SW must ensure all the register (MMIO) initialization/programming through CPU happens in this block or latter, this ensures the MMIO state is save/restored on subsequent context switches (Power Sequences). Once the render engine is programmed with valid state and the configuration, Force Wakeup bit should be reset to enable C6 entry. 	RenderCS										
Render CS Only: Ring Buffer Mode of Scheduling: SW must follow the below programming notes before disabling ring buffer to ensure HW is not in middle of the IDLE flows. <ul style="list-style-type: none"> SW must set the Force Wakeup bit to prevent GT from entering C6. Disable IDLE messaging in CS (Write 0x2050[31:0] = 0x00010001) Poll/Wait for register bits of <u>0x22AC[6:0]</u> turn to 0x30 value. Disable Ring Buffer Enable IDLE messaging in CS (Write 0x2050[31:0] = 0x00010000) Force Wakeup bit should be reset to enable C6 entry. 	RenderCS										

Ring Buffer Current Context ID Register

BCS_RCCID - Ring Buffer Current Context ID Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BlitterCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Address:	22190h-22197h	
This register contains the current ring context ID associated with the ring buffer.		
Programming Notes		
The current context registers must not be written directly (via MMIO). The RCCID register should only be updated indirectly from RNCID.		
DWord	Bit	Description
0	63:0	Unnamed See Context Descriptor for BCS.

Ring Buffer Head

RING_BUFFER_HEAD - Ring Buffer Head				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	02034h-02037h			
Name:	Ring Buffer Head			
ShortName:	RING_BUFFER_HEAD_RCSUNIT			
Address:	12034h-12037h			
Name:	Ring Buffer Head			
ShortName:	RING_BUFFER_HEAD_VCSUNIT0			
Address:	1A034h-1A037h			
Name:	Ring Buffer Head			
ShortName:	RING_BUFFER_HEAD_VECSUNIT			
Address:	1C034h-1C037h			
Name:	Ring Buffer Head			
ShortName:	RING_BUFFER_HEAD_VCSUNIT1			
Address:	22034h-22037h			
Name:	Ring Buffer Head			
ShortName:	RING_BUFFER_HEAD_BCSUNIT			
Description				
<p>This register is used to define and operate the ring buffer mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a physical memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. Refer to the Programming Interface chapter for a detailed description of the parameters specified in this ring buffer register set, restrictions on the placement of ring buffer memory, arbitration rules, and in how the ring buffer can be used to pass instructions. Ring Buffer Head Offsets must be properly programmed before ring is enabled. A Ring Buffer can be enabled when empty.</p>				
DWord	Bit	Description		
0	31:21	<p>Wrap Count</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>U11 count of ring buffer wraps</td> </tr> </table> <p>This field is incremented by 1 whenever the Head Offset wraps from the end of the buffer back to the start (i.e., whenever it wraps back to 0). Appending this field to the Head Offset field effectively creates a virtual 4GB Head "Pointer" which can be used as a tag associated with instructions placed in a ring buffer. The Wrap Count itself will wrap to 0 upon overflow.</p>	Format:	U11 count of ring buffer wraps
Format:	U11 count of ring buffer wraps			

RING_BUFFER_HEAD - Ring Buffer Head							
20:2	<p>Head Offset</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 20%;">Format:</td> <td>GraphicsAddress[20:2] DWord Offset</td> </tr> </table> <p>This field indicates the offset of the <i>next</i> instruction DWord to be parsed. Software will initialize this field to select the first DWord to be parsed once the RB is enabled. (Writing the Head Offset while the RB is enabled is UNDEFINED). Subsequently, the device will increment this offset as it executes instructions - until it reaches the QWord specified by the Tail Offset. At this point the ring buffer is considered "empty".</p> <table border="1" style="width: 100%; background-color: #e6f2ff;"> <tr> <td colspan="2" style="text-align: center;">Programming Notes</td> </tr> <tr> <td colspan="2">A RB can be enabled empty or containing some number of valid instructions.</td> </tr> </table>	Format:	GraphicsAddress[20:2] DWord Offset	Programming Notes		A RB can be enabled empty or containing some number of valid instructions.	
Format:	GraphicsAddress[20:2] DWord Offset						
Programming Notes							
A RB can be enabled empty or containing some number of valid instructions.							
1	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ				
Format:	MBZ						
0	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 40%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ		
Project:	CHV, BSW						
Format:	MBZ						

Ring Buffer Start

RING_BUFFER_START - Ring Buffer Start				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	02038h-0203Bh			
Name:	Ring Buffer Start			
ShortName:	RING_BUFFER_START_RCSUNIT			
Address:	12038h-1203Bh			
Name:	Ring Buffer Start			
ShortName:	RING_BUFFER_START_VCSUNIT0			
Address:	1A038h-1A03Bh			
Name:	Ring Buffer Start			
ShortName:	RING_BUFFER_START_VECSUNIT			
Address:	1C038h-1C03Bh			
Name:	Ring Buffer Start			
ShortName:	RING_BUFFER_START_VCSUNIT1			
Address:	22038h-2203Bh			
Name:	Ring Buffer Start			
ShortName:	RING_BUFFER_START_BCSUNIT			
Description				
<p>These registers are used to define and operate the "ring buffer" mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a physical memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. Refer to the Programming Interface chapter for a detailed description of the parameters specified in this ring buffer register set, restrictions on the placement of ring buffer memory, arbitration rules, and in how the ring buffer can be used to pass instructions.</p>				
DWord	Bit	Description		
0	31:12	<p>Starting Address</p> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>GraphicsAddress[31:12]RingBuffer</td> </tr> </table> <p>This field specifies Bits 31:12 of the 4KB-aligned starting Graphics Address of the ring buffer. Address bits 31 down to 29 must be zero. All ring buffer pages must map to Main Memory (uncached) pages. Ring Buffer addresses are always translated through the global GTT.</p>	Format:	GraphicsAddress[31:12]RingBuffer
	Format:	GraphicsAddress[31:12]RingBuffer		
11:0	Reserved			

Ring Buffer Tail

RING_BUFFER_TAIL - Ring Buffer Tail		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02030h-02033h	
Name:	Ring Buffer Tail	
ShortName:	RING_BUFFER_TAIL_RCSUNIT	
Address:	12030h-12033h	
Name:	Ring Buffer Tail	
ShortName:	RING_BUFFER_TAIL_VCSUNIT0	
Address:	1A030h-1A033h	
Name:	Ring Buffer Tail	
ShortName:	RING_BUFFER_TAIL_VECSUNIT	
Address:	1C030h-1C033h	
Name:	Ring Buffer Tail	
ShortName:	RING_BUFFER_TAIL_VCSUNIT1	
Address:	22030h-22033h	
Name:	Ring Buffer Tail	
ShortName:	RING_BUFFER_TAIL_BCSUNIT	
Description		
<p>These registers are used to define and operate the "ring buffer" mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a linear memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. Refer to the Programming Interface chapter for a detailed description of the parameters specified in this ring buffer register set, restrictions on the placement of ring buffer memory, arbitration rules, and in how the ring buffer can be used to pass instructions. Ring Buffer Tail Offsets must be properly programmed before ring is enabled. A Ring Buffer can be enabled when empty.</p>		
DWord	Bit	Description
0	31:21	Reserved
		Format: MBZ

RING_BUFFER_TAIL - Ring Buffer Tail

20:3	<p>Tail Offset</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[20:3]</td> </tr> </table> <p>This field is written by software to specify where the valid instructions placed in the ring buffer end. The value written points to the QWord past the last valid QWord of instructions. In other words, it can be defined as the next QWord that software will write instructions into. Software must write subsequent instructions to QWords following the Tail Offset, possibly wrapping around to the top of the buffer (i.e., software can't skip around within the buffer). Note that all DWords prior to the location indicated by the Tail Offset must contain valid instruction data - which may require instruction padding by software. See Head Offset for more information.</p> <table border="1" style="width: 100%; background-color: #e6f2ff;"> <tr> <td style="text-align: center;">Programming Notes</td> </tr> </table> <p>[Ring Buffer Mode Of scheduling only][Video CS, Video Enhancement CS, Blitter CS]: HW loses Page Directory (PPGTT) information on becoming IDLE. SW must always program the PD information through MI_LOAD_REGISTER_IMM command in the ring buffer prior to programming workload begins on every ring dispatch. This will ensure Page Directory information is not lost due to IDLE flows.</p>	Format:	GraphicsAddress[20:3]	Programming Notes
Format:	GraphicsAddress[20:3]			
Programming Notes				
2:0	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ			

Root Table Address Pointer Value First 31_0

RTAPV_1_310 - Root Table Address Pointer Value First 31_0						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F500h					
This register is used to store local copy of the Root Table address pointer value.						
DWord	Bit	Description				
0	31:0	<p>First Address 31 to 0</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bits 31:11 = Root Table Address Pointer Value 31:11. Bits 10:1 = Reserved. Bit 0 = Enabled for Root Table Address Pointer Value 31:11.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

Root Table Address Pointer Value Second 31_0

RTAPV_2_310 - Root Table Address Pointer Value Second 31_0						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F504h					
This register is used to store local copy of the Root Table address pointer value.						
DWord	Bit	Description				
0	31:0	<p>Second Address 31 to 0</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bits 31:8 = Reserved. Bits 7:1 = Root Table Address Pointer Value 38:32. Bit 0 = Enabled for Root Table Address Pointer Value 38:32.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

RP Decrease Limit

RPDECLIMIT - RP Decrease Limit				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A030h-0A033h			
DWord	Bit	Description		
0	31:24	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
23:0	Decrease Threshold <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Decrease Threshold (DECLIMIT): This register contains the threshold used to determine whether a switch to a higher higher frequency is desirable. FRQDUM determines the meaning of this register: Busy Min Continuous Limit Busy Min Average Limit Idle Max Continuous Limit The values are: 0 = 0 usec 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec</p>	Access:	R/W	
Access:	R/W			

RP Down Timeout

RPDNTIMOUT - RP Down Timeout				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A010h-0A013h			
DWord	Bit	Description		
0	31:24	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
23:0	Down Timeout <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>The value in this register contains the timeout value for gfx idleness due to stopped graphics clocks (CPD) necessary to trigger the Render Geyserville Downward Timeout interrupt.</p> <p>0 = 0 usec 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec</p>	Access:	R/W	
Access:	R/W			

RP Downwards Evaluation Interval

RPDNEI - RP Downwards Evaluation Interval				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A06Ch-0A06Fh			
DWord	Bit	Description		
0	31:24	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
23:0	Evaluation Interval Period for Downwards Freq Direction <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>The geyserville performance status will be averaged over this interval, and the results will be used to possibly recommend a switch to the slower render clock frequency (either directly by hardware or via an interrupt activating a sw decision).</p> <p>0 = 0 usec 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec pmcr_ei_down[23:0]</p>	Access:	R/W	
Access:	R/W			

RP Increase Limit

RPINCLIMIT - RP Increase Limit				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A02Ch-0A02Fh			
DWord	Bit	Description		
0	31:24	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
23:0	Increase Threshold <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Increase Threshold (INCLIMIT): This register contains the threshold used to determine whether a switch to a higher higher frequency is desirable. FRQIUM determines the meaning of this register: Busy Max Continuous Limit Busy Max Average Limit Idle Min Continuous Limit The values are: 0 = 0 usec 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec</p>	Access:	R/W	
Access:	R/W			

RP Normal Software Frequency Request

RP_FREQ_NORMAL - RP Normal Software Frequency Request				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A008h			
This 32 bit value is written to the PCU IO_THREAD_P_REQ register when NOT in Video Turbo mode.				
DWord	Bit	Description		
0	31	Turbo Disable <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>The Turbo Disable bit is determined by SW. NOTE: If Turbo is disable for ANY thread, it will prevent turbo for ALL threads.</p>	Access:	R/W
	Access:	R/W		
	30:24	P State Request <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This field indicates the maximum P-State request in units of 100MHz.</p>	Access:	R/W
	Access:	R/W		
	23:18	P State Offset <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This field defined the number of steps that Energy Efficient P-State is allowed to fall in units of 100 MHz.</p>	Access:	R/W
Access:	R/W			
17:14	Energy Efficient policy <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>The energy efficiency policy is determined by SW.</p>	Access:	R/W	
Access:	R/W			
13:0	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			

RP Software Frequency Request Hysteresis

RPSWFREQHYST - RP Software Frequency Request Hysteresis						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0A004h					
DWord	Bit	Description				
0	31:6	Reserved				
		Access: RO				
	5:0	RP SW Freq Request Hysteresis				
		Access: R/W				
		<table border="1"> <thead> <tr> <th>Programming Notes</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>Not supported. It must be 0 at all times.</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Programming Notes	Project	Not supported. It must be 0 at all times.	CHV, BSW
Programming Notes	Project					
Not supported. It must be 0 at all times.	CHV, BSW					

RP Upwards Evaluation Interval

RPUPEI - RP Upwards Evaluation Interval				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A068h-0A06Bh			
DWord	Bit	Description		
0	31:24	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
23:0	Evaluation Interval Period for Upwards Freq Direction <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>The geyserville performance status will be averaged over this interval, and the results will be used to possibly recommend a switch to the faster render clock frequency (either directly by hardware or via an interrupt activating a sw decision).</p> <p>0 = 0 usec 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec pmcr_ei_up[23:0]</p>	Access:	R/W	
Access:	R/W			

RP Video Turbo Software Frequency Request

RP_FREQ_VIDEOTURBO - RP Video Turbo Software Frequency Request				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A00Ch			
This 32 bit value is written to the PCU IO_THREAD_P_REQ register when in Video Turbo mode.				
DWord	Bit	Description		
0	31	Turbo Disable <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>The Turbo Disable bit is determined by SW. NOTE: If Turbo is disable for ANY thread, it will prevent turbo for ALL threads.</p>	Access:	R/W
	Access:	R/W		
	30:24	P State Request <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This field indicates the maximum P-State request in units of 100MHz.</p>	Access:	R/W
	Access:	R/W		
	23:18	P State Offset <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This field defined the number of steps that Energy Efficient P-State is allowed to fall in units of 100 MHz.</p>	Access:	R/W
Access:	R/W			
17:14	Energy Efficient policy <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>The energy efficiency policy is determined by SW.</p>	Access:	R/W	
Access:	R/W			
13:0	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			

RS_PREEMPT_STATUS_UDW

RS_PREEMPT_STATUS_UDW - RS_PREEMPT_STATUS_UDW				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	RenderCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	02174h			
<p>Preemption from First Level Batch Buffer: This register contains the offset in to the Batch Buffer on which Resource streamer got preempted. Note that it is offset from the Batch Start Address and not the graphics address corresponding to the preempted instruction on Batch Buffer. This register's contents will be looked at by Command Streamer on the next RS Start Trigger to provide the appropriate batch start address. Following preemption, context save happens on which this register is context saved, after context save the register gets auto reset by Command Streamer. This register gets context save/restored by Render Command Streamer as part of its render context. Preemption from Second Level Batch Buffer: This register contains the graphics address of the instruction in Second Level Batch Buffer on which Resource streamer got preempted. This register's contents will be looked at by Command Streamer on the next RS Start Trigger to provide the appropriate batch start address. Following preemption, context save happens on which this register is context saved, after context save the register gets auto reset by Command Streamer. This register gets context save/restored by Render Command Streamer as part of its render context.</p>				
Programming Notes				
<ul style="list-style-type: none"> This register is accessed by Render Command Streamer as part of render context save/restore; this register should be exercised by S/W only for resetting the register contents if required. Following preemption if there is no context save, SW should program this register with 0x0 so that it does not interfere with proceeding workloads. 				
DWord	Bit	Description		
0	31:16	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
15:0	<p>Batch Buffer Offset Upper DWORD</p> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the last preempted second level batch buffer in resource streamer.</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			

RS Preemption Hint

RS_PRE_HINT - RS Preemption Hint											
Register Space:	MMIO: 0/2/0										
Project:	CHV, BSW										
Source:	RenderCS										
Default Value:	0x00000000										
Access:	R/W										
Size (in bits):	32										
Address:	024C0h										
<p>This register contains the Dword aligned Graphics address in to the Batch Buffer corresponding to either 3D_PRIMITIVE or RCS-RS sync command called Preemption Hint Address. When Preemption Hint Address is enabled, RS will honor preemption request from RCS only on parsing 3D_PRIMITIVE/RCS-RS sync command at Preemption Hint Address.</p>											
Programming Notes											
<p>Programming Restriction: This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of preempting Resource Streamer in command stream. Programmer has to ensure that RS Preemption Hint register gets programmed well before RS gets preempted by RCS. Note that this register should be programmed with caution as it can lead to indefinite stalls in RS.</p>											
<ul style="list-style-type: none"> a. RS will preempt on receiving preemption request from RCS only on reaching the instruction in the batch buffer corresponding to the address mentioned in RS_PREEMPT_HINT. RS could hit an RCS-RS sync command before reaching the address mentioned in the RS_PREEMPT_HINT, in this case RS should preempt on the sync command. b. RS could hit the address mentioned in 3D_PREEMPT_HINT before receiving preempt request from RCS. In this case RS will stall at this command until it receives preemption request from RCS and then preempts. 											
DWord	Bit	Description									
0	31:2	Preemption Hint Address									
		<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>U30</td> </tr> </table> <p>This field contains the Dword aligned Graphics Address in to the batch buffer as Preemption Hint.</p>	Format:	U30							
	Format:	U30									
	1	Reserved									
0	Preemption Hint										
		<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>Enabled</td> </tr> </table>	Format:	Enabled							
Format:	Enabled										
		<table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disabled</td> <td>Preemption hint is disabled for Resource Streamer.</td> </tr> <tr> <td>1h</td> <td>Enabled</td> <td>Preemption hint is enabled for Resource streamer.</td> </tr> </tbody> </table>	Value	Name	Description	0h	Disabled	Preemption hint is disabled for Resource Streamer.	1h	Enabled	Preemption hint is enabled for Resource streamer.
Value	Name	Description									
0h	Disabled	Preemption hint is disabled for Resource Streamer.									
1h	Enabled	Preemption hint is enabled for Resource streamer.									

RS Preemption Hint UDW

RS_PREEMPTION_HINT_UDW - RS Preemption Hint UDW				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	RenderCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	024C4h			
<p>This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the Batch Buffer corresponding to either 3D_PRIMITIVE or RCS-RS sync command called Preemption Hint Address. When Preemption Hint Address is enabled, RS will honor preemption request from RCS only on parsing 3D_PRIMITIVE/RCS-RS sync command at Preemption Hint Address.</p>				
Restriction				
<p>This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of preempting Resource Streamer in command stream. See RS_PRE_HINT definition for further restrictions.</p>				
DWord	Bit	Description		
0	31:16	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
15:0	<p>Preemption Hint Address Upper DWORD</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td style="width: 70%;">GraphicsAddress[47:32]</td> </tr> </table> <p>This field contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the batch buffer as Preemption Hint.</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			

Sampler control register

SAMPLER_CTL - Sampler control register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	0E140h	
Valid Projects:	CHV, BSW]	
DWord	Bit	Description
0	31:16	ECO Reserved 1 Reserved: MBZ
	15:8	Reserved
	7:3	Sampler unit select
	2	ECO Reserved 2
	1:0	ECO Reserved 3

SAMPLER Mode Register

SAMPLER_MODE - SAMPLER Mode Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	RenderCS			
Default Value:	0x00000000			
Size (in bits):	32			
Trusted Type:	1			
Address:	07028h			
Valid Projects:	CHV, BSW			
<p>This register has bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. To set bit0, for example, the data would be 0x0001_0001. To clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16.</p>				
DWord	Bit	Description		
0	31:16	Reserved		
		Access:	RO	
	15:14	ECO Reserved 1		
		Format:	MBZ	
	13:8	ECO Reserved 2		
		Project:	CHV, BSW	
		Format:	MBZ	
	7:6	ECO Reserved 3		
		Project:	All	
		Format:	MBZ	
5	ECO_SCRATCH3B			
		Project:		
	Format:	MBZ		
4:0	Sample_d Quality Mode			
		Project:	CHV, BSW	
		Format:	U5	
	<p>This field configures the image quality mode for the sample_d message in the sampling engine. In general, performance will increase with each step of reduced quality.</p>			
		Value	Name	Description
				Project
		00h	Disabled	Full quality is enabled, matching prior products
		01h-1Fh		Quality degrades with each larger value, performance improves with each larger value
				All
				All

SAMPLER READ DATA

SAMPLER_RDATA - SAMPLER READ DATA		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0xFFFFFFFF	
Access:	RO Variant	
Size (in bits):	32	
Address:	0E144h	
Valid Projects:	CHV, BSW	
DWord	Bit	Description
0	31:0	Reserved
		Default Value: FFFFFFFFh

Save Timer

SVTIMER - Save Timer												
Register Space:	MMIO: 0/2/0											
Project:	CHV, BSW											
Source:	PRM											
Default Value:	0x60001000											
Size (in bits):	32											
Address:	0B434h											
DWord	Bit	Description										
0	31	Reserved										
	30:29	Counter Enabling Selection										
	Default Value: 11b											
	Access: R/W											
<p>LPFC provides rudimentary compression by allowing software to select from several predefined levels of event reporting. Based on the value of this bitfield, only a certain number of the programmed events in the "Event Selection and Base Counters" registers (CNT0CL, CNT1CL, ..., CNT7CL) will be tracked and reported:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Selected Counters</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>Counter 0</td> </tr> <tr> <td>01</td> <td>Counters 0 & 1</td> </tr> <tr> <td>10</td> <td>Counters 0, 1, 2, & 3</td> </tr> <tr> <td>11</td> <td>Counters 0 - 7</td> </tr> </tbody> </table> <p>Signal - lpconf_lpfc_cnt_enabled [1:0].</p>			Value	Selected Counters	00	Counter 0	01	Counters 0 & 1	10	Counters 0, 1, 2, & 3	11	Counters 0 - 7
Value	Selected Counters											
00	Counter 0											
01	Counters 0 & 1											
10	Counters 0, 1, 2, & 3											
11	Counters 0 - 7											
0	28:24	Reserved										
	23:0	Save Timer Interval										
	Default Value: 000000000001000000000000b											
Access: R/W												
<p>Save Timer Interval (SVTMRINT). Save Timer Interval: This is the interval for sampling the performance counters and writing to memory. Each time it expires, the counters are sampled and packetized to be sent to DMA controller. The minimum granularity of sampling period is 256clocks. The value in this register is used as 256 x value to find the sampling window. For a 1Ghz core clock it provides up to 4ns of sampling period while matching the maximum capability of the event counters. 1h - 256clks. 2h - 512clks. ... 8h - 2048clks. Signal - lpconf_lpfc_savetimer_int [23:0].</p>												

SB_ADDRESS

SB_ADDRESS - SB_ADDRESS						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	182108h					
<p>The Sideband Address Register is used by the sideband transaction (triggered by Sideband Packet Register) for holding the address (of the internal register, within the destination unit).</p>						
<p>IOSF SB access prevention: An IOSF SB write access targeting this register will complete with no affect. An IOSF SB read access targeting this register will abort (with 1's being returned on IOSF SB).</p>						
DWord	Bit	Description				
0	31:0	<p>SB_Addr</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Address, written by IOSF primary, for triggered IOSF SB initiated access. 0x18_2100 (SB_Busy) bit 0 = 1 then an IOSF primary write will NOT be captured. 0x18_2100 (SB_Busy) bit 0 = 0 then an IOSF primary write will be captured. Dword aligned addresses must be used.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SB_DATA

SB_DATA - SB_DATA						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	182104h					
<p>The Sideband Data Register is used by the sideband register access mechanism (triggered by Sideband Packet Register) for holding write-data in write-transactions or read-data for read-transactions as explained below.</p> <p>IOSF SB access prevention :An IOSF SB write access targeting this register will complete with no affect. An IOSF SB read access targeting this register will abort (with 1's being returned on IOSF SB). Requirement : IOSF primary write to this register should not occur when a pending IOSF SB return is pending.</p>						
DWord	Bit	Description				
0	31:0	<p>SB Data</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Triggered IOSF SB write, this is the Data written in the IOSF SB initiated access. Triggered IOSF SB read, this is the Data read return from the IOSF SB initiated read access. 0x18_2100 (SB_Busy) bit 0 = 1 then an IOSF primary write will NOT be captured. 0x18_2100 (SB_Busy) bit 0 = 0 then an IOSF primary write will be captured.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SB_REQ_TRIGGER

SB_REQ_TRIGGER - SB_REQ_TRIGGER	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	182100h
<p>When the Sideband Packet Register is written, the Gunit creates a transaction towards the destination agent on the IOSF sideband channel.</p> <p>The fields sent with the write operation as transaction parameters:</p> <ul style="list-style-type: none"> • The Sideband Rid field (bits 31:24) is used as the transaction Rid. • The Sideband Opcode field (bits 23:15) is used as the transaction opcode. • The Sideband Port field (bits 15:8) is used as the transaction destination port. • The source port is hard-coded to 6h (Gunit port). • The Sideband Byte Enable Field (bits 7:4) is used as the transaction Byte Enable. <p>If the opcode results in a data write semantic transaction, the write-data will be taken from the Sideband Data Register. If the opcode results in a data read semantic transaction, the read-data will be placed in the Sideband Data Register and may later be read by software. When Sideband Busy is set, Sideband Packet Register, Sideband Data Register and Sideband Address Register fields cannot be written. If the opcode results in a data read semantic transaction, data will be ready at Sideband Data register only when the Sideband Busy is cleared.</p> <p>Fuse block access prevention: To prevent an attacker from using this mechanism to read the fuse block, writing the Fuse Block PortID to the Sideband Port will prevent the SB_busy bit from being set. This effectively 'aborts' the access. The triggered write is effectively dropped. The triggered read would supply whatever happened to be in the IOSF Sideband Doorbell Data register. IOSF SB access prevention : No usage models require IOSF SB accesses to the doorbell registers. No IOSF SB sources should be using IOSF SB accesses to the doorbell register to trigger a doorbell generated IOSF SB message. Software and firmware are PROHIBITED from using IOSF SB accesses to target and trigger accesses from this registers.</p> <p>Usage of the doorbell mechanism :</p> <p>From IOSF primary, to initiate a write on IOSF Sideband :</p> <ol style="list-style-type: none"> a. Write Data (0x18_2104) b. Write Address (0x18_2108) c. Write Packet and Trigger (0x18_2100) d. Read poll 0x18_2100. When bit 0 = '0', then the write has completed on IOSF Sideband. <p>From IOSF primary, to initiate a read on IOSF Sideband :</p> <ol style="list-style-type: none"> a. Write Address (0x18_2108) b. Write Packet and Trigger (0x18_2100) c. Read poll 0x18_2100. When bit 0 = '0', then the read has completed on IOSF Sideband and data is available. d. Read IOSF SB returned Data (0x18_2104) <p>If software attempts a read to a register and the result is a UR (Unsupported Request), the busy bit will be cleared with no update of the doorbell data register.</p>	

SB_REQ_TRIGGER - SB_REQ_TRIGGER						
DWord	Bit	Description				
0	31:24	<p>SB_DevFn</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">00h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Device and Function number to be used for the IOSF SB access. Per the IOSF Specification, this 8-bit field ('fid' in the IOSF Spec) is a unique identifier of a target in a hierarchy of PCI buses (indicates Device Number [31:27] / Function Number [26:24] or Function Number [31:24]). The target is free to utilize this in an agent-specific manner.</p>	Default Value:	00h	Access:	R/W
	Default Value:	00h				
	Access:	R/W				
	23:16	<p>SB_Opcode</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">00h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Opcode to be used for the IOSF SB access.</p>	Default Value:	00h	Access:	R/W
	Default Value:	00h				
	Access:	R/W				
15:8	<p>SB_Port</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">00h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Port to be used for the IOSF SB access.</p>	Default Value:	00h	Access:	R/W	
Default Value:	00h					
Access:	R/W					
7:4	<p>SB_ByteEnables</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Byte enables to be used for the iOSF SB access.</p>	Default Value:	0h	Access:	R/W	
Default Value:	0h					
Access:	R/W					
3:1	<p>SB_BAR</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>BAR value</p>	Default Value:	000b	Access:	R/W	
Default Value:	000b					
Access:	R/W					
0	<p>SB_Busy</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>A write to this register will set this bit = '1' and triggers a IOSF SB request. When this bit is '1', the following registers are not IOSF primary write-able (0x18_2100, 0x18_2104, 0x18_2108)The completion of the IOSF SB access will clear this bit. 0 - 0x18_2100, 0x18_2104 and 0x18_2108 are writeable via IOSF Sideband. 1 - An IOSF SB access is in-progress. 0x18_2100, 0x18_2104 and 0x18_2108 are NOT writeable via IOSF Sideband.</p>	Default Value:	0b	Access:	RO	
Default Value:	0b					
Access:	RO					

SCPDO

SCPDO - SCPDO						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	18209Ch					
Scratch Pad 0 Register						
DWord	Bit	Description				
0	31:0	Scratch Pad <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Software scratch pad	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SCRATCH1

SCRATCH1 - SCRATCH1						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000 CHV, BSW					
Size (in bits):	32					
Address:	0B11Ch					
DWord	Bit	Description				
0 Project: CHV, BSW	31:0	SCRATCH <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Project:	CHV, BSW	Access:	R/W
Project:	CHV, BSW					
Access:	R/W					

SCRATCH for LNCFunit

SCRATCH_LNCF1 - SCRATCH for LNCFunit		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000001 CHV, BSW	
Size (in bits):	32	
Address:	0B008h	
DWord	Bit	Description
0	31:3	SCRATCH register for LNCFunit
		Project: CHV, BSW
		Access: R/W
	2	Memory fill delay
	Access: R/W	
	Incf_csr_lni_gt2_memfill_dis. 0:mem fills gt2 latency will be 1 . 1:mem fill gt2 latency will be same as gt3.	
1	flush start delay	
	Access: R/W	
	Incf_csr_lni_disable_flush_start_delay. 0:Flush processing in LNIunit starts one clock after receiving the flush command default. 1:Flush processing in LNIunit starts in the same clock in which flush command is received.	
0	0	Non-IA coherent atomics enable
		Default Value: 1b
		Project: CHV, BSW
		Access: R/W
	0: atomics in GTI (). 1: atomics in L3 (non-IA atomic) (Default). Output signal from LNCF unit Incf_csr_lni_glblatmcs_I3. Value for this bit should be same as lbcf_csr_lsqc_glblatmcs_I3 b118[22].Value of this bit should be same as LBCF register bit 0xb11c[8].Adding Xbuf 8 MCP.	

Scratch Register 1

SCRATCH1 - Scratch Register 1				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A188h-0A18Bh			
DWord	Bit	Description		
0	31:0	<p>Scratch1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Register bits that have no connection to design. Used to enable/disable changes to the design that were put in during the ECO process.</p> <p>none</p>	Access:	R/W
Access:	R/W			

Scratch Register 2

SCRATCH2 - Scratch Register 2				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A198h			
DWord	Bit	Description		
0	31:0	<p>Scratch2</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Register bits that have no connection to design. Used to enable/disable changes to the design that were put in during the ECO process.</p> <p>none</p>	Access:	R/W
Access:	R/W			

Second Buffer Size

SBS - Second Buffer Size				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B424h			
DWord	Bit	Description		
0	31:16	<p>Second Virtual Buffer Base</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%;">R/W</td> </tr> </table> <p>Second Virtual Buffer Base (SVBB0). Second Virtual Buffer Base: Programmed by driver to allocate a memory space for performance data storage. The buffer size should be aligned to the size of the memory allocated so it naturally aligns to the base (i.e. for 128KB bit[16]=0, 256KB bit[17:16]=0, 512KB bit[18:16]=0). Signal - lpconf_lpfc_virtual_base1 [31:16].</p>	Access:	R/W
	Access:	R/W		
	15:12	<p>Second Buffer Size 0</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%;">R/W</td> </tr> </table> <p>Second Buffer Size: Determines the allowed buffer size for performance data storage. 0000b: 64KB. 0001b: 128KB. 0010b: 256KB. 0011b: 512KB. ... 1111b: 2GB. Signal - lpconf_lpfc_buffer_size1 [3:0].</p>	Access:	R/W
Access:	R/W			
11:0	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%;">RO</td> </tr> </table> <p>Reserved.</p>	Access:	RO	
Access:	RO			

Second Level Batch Buffer Head Pointer Preemption Register

SBB_PREEMPT_ADDR - Second Level Batch Buffer Head Pointer Preemption Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	0213Ch-0213Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_RCSUNIT
Address:	1213Ch-1213Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VCSUNIT0
Address:	1A13Ch-1A13Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VECSUNIT
Address:	1C13Ch-1C13Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VCSUNIT1
Address:	2213Ch-2213Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_BCSUNIT
Description	
<p>This register gets updated with the DWord-aligned graphics memory address of the PREEMPTABLE command in the second level batch buffer on which preemption has occurred.</p> <p>This register value should be looked at only when the preemption has occurred in the second level batch buffer. This is indicated by "Ring/Batch Indicator" in "RING_BUFFER_HEAD_PREEMPT_REG". This register value retains its previous value and doesn't change when the preemption occurs on a preemptable command in ring buffer or in batch buffer.</p> <p>Preemption is triggered by valid UHPTR in ring buffer mode of scheduling and by a pending execlist in Exec-List mode of scheduling. This is a global register and context save/restored as part of power context image.</p>	

SBB_PREEMPT_ADDR - Second Level Batch Buffer Head Pointer Preemption Register

Preemptable Commands	Source
MI_ARB_CHECK 3D_PRIMITIVE GPGPU_WALKER MEDIA_STATE_FLUSH PIPE_CONTROL (Only in GPGPU mode of pipeline selection) MI_ATOMIC (Post Sync Operation set in GPGPU mode of pipeline selection) MI_SEMAPHORE_SIGNAL (Post Sync Operation set in GPGPU mode of pipeline selection)	RenderCS

Programming Notes

Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description		
0	31:2	Second Level Batch Buffer Head Pointer Format: <table border="1" style="display: inline-table; border-collapse: collapse;"><tr><td style="width: 100px; height: 15px;"> </td><td style="width: 150px;">GraphicsAddress[31:2]</td></tr></table> This field specifies the DWord-aligned Graphics Memory Address of the PREEMPTABLE command in a batch buffer where the Preemption has occurred.		GraphicsAddress[31:2]
	GraphicsAddress[31:2]			
	1:0	Reserved Format: <table border="1" style="display: inline-table; border-collapse: collapse;"><tr><td style="width: 100px; height: 15px;"> </td><td style="width: 100px;">MBZ</td></tr></table>		MBZ
	MBZ			

Second Level Batch Buffer Head Pointer Register

SBB_ADDR - Second Level Batch Buffer Head Pointer Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	CommandStreamer			
Default Value:	0x00000000			
Access:	RO			
Size (in bits):	32			
Address:	02114h-02117h			
Name:	Second Level Batch Buffer Head Pointer Register			
ShortName:	SBB_ADDR_RCSUNIT			
Address:	12114h-12117h			
Name:	Second Level Batch Buffer Head Pointer Register			
ShortName:	SBB_ADDR_VCSUNIT0			
Address:	1A114h-1A117h			
Name:	Second Level Batch Buffer Head Pointer Register			
ShortName:	SBB_ADDR_VECSUNIT			
Address:	1C114h-1C117h			
Name:	Second Level Batch Buffer Head Pointer Register			
ShortName:	SBB_ADDR_VCSUNIT1			
Address:	22114h-22117h			
Name:	Second Level Batch Buffer Head Pointer Register			
ShortName:	SBB_ADDR_BCSUNIT			
This register contains the current DWord Graphics Memory Address of the last-initiated batch buffer.				
Programming Notes				
This register should NEVER be programmed by driver, this is for HW internal use only. This register should not be written by software. These fields should only get written by a context restore. Software should always set these fields via the MI_BATCH_BUFFER_START command when initiating a batch buffer. This register is saved and restored with context.				
DWord	Bit	Description		
0	31:2	<p>Second Level Batch Buffer Head Pointer</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[31:2]</td> </tr> </table> <p>This field specifies the DWord-aligned Graphics Memory Address where the last initiated Second Level Batch Buffer is currently fetching commands. This field is meaningful only when Valid field is set to "1".</p>	Format:	GraphicsAddress[31:2]
	Format:	GraphicsAddress[31:2]		
1	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ			

SBB_ADDR - Second Level Batch Buffer Head Pointer Register

	0	Valid			
		Format:		U1	
		Value	Name	Description	Project
		0h	Invalid [Default]	Second Level Batch buffer Invalid	CHV, BSW
		1h	Valid	Second Batch buffer Valid.	CHV, BSW

Second Level Batch Buffer State Register

SBB_STATE - Second Level Batch Buffer State Register					
Register Space:	MMIO: 0/2/0				
Project:	CHV, BSW				
Source:	RenderCS				
Default Value:	0x00000000 CHV, BSW				
Access:	R/W				
Size (in bits):	32				
Address:	02118h				
Address:	12118h-1211Bh				
Name:	Second Level Batch Buffer State Register				
ShortName:	SBB_STATE_VCSUNIT0				
Address:	1A118h-1A11Bh				
Name:	Second Level Batch Buffer State Register				
ShortName:	SBB_STATE_VECSUNIT				
Address:	1C118h-1C11Bh				
Name:	Second Level Batch Buffer State Register				
ShortName:	SBB_STATE_VCSUNIT1				
Address:	22118h-2211Bh				
Name:	Second Level Batch Buffer State Register				
ShortName:	SBB_STATE_BCSUNIT				
<p>This register contains the attributes of the second level batch buffer initiated from the batch Buffer.</p> <p>This register should not be written by software. These fields should only get written by a context restore. Software should always set these fields via the MI_BATCH_BUFFER_START command when initiating a batch buffer. This register is saved and restored with context.</p>					
DWord	Bit	Description			
0	31:9	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
	Format:	MBZ			
	8	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:
Project:	CHV, BSW				
Format:	MBZ				
7	<p>Resource Streamer Enable</p> <table border="1"> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>When this bit is set, the Resource Streamer will execute the batch buffer. When this bit is clear the Resource Streamer will not execute the batch buffer.</p>	Format:	U1		
Format:	U1				

SBB_STATE - Second Level Batch Buffer State Register

	6	Reserved		
		Project:	CHV, BSW	
		Format:	MBZ	
	5	Address Space Indicator		
		Project:	CHV, BSW	
		Note: This field reflects the effective address space indicator security level and may not be the same as the Address Space Indicator written using MI_BATCH_BUFFER_START.		
		Value	Name	Description
		0h	GGTT [Default]	This second level batch buffer is located in GGTT memory and is privileged
	1h	PPGTT	This second level batch buffer is located in PPGTT memory and is non-privileged.	
	4	Reserved		
		Project:	CHV, BSW	
		Format:	MBZ	
3:0	Reserved			
	Format:	MBZ		

Second Level Batch Buffer Upper Head Pointer Preemption Register

SBB_PREEMPT_ADDR_UDW			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Address:	02138h-0213Bh		
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register		
ShortName:	SBB_PREEMPT_ADDR_UDW_RCSUNIT		
Address:	12138h-1213Bh		
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register		
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT0		
Address:	1A138h-1A13Bh		
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register		
ShortName:	SBB_PREEMPT_ADDR_UDW_VECSUNIT		
Address:	1C138h-1C13Bh		
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register		
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT1		
Address:	22138h-2213Bh		
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register		
ShortName:	SBB_PREEMPT_ADDR_UDW_BCSUNIT		
<p>This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the last preempted second level batch buffer. This register follows the same rules as the SBB_PREEMPT_ADDR register.</p>			
Programming Notes			
<p>Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.</p>			
DWord	Bit	Description	
0	31:16	Reserved	
	15:0	<p>Second Level Batch Buffer Head Pointer Upper DWORD</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>This field specifies the 4GB aligned base address of gfx 4GB virtual address space of the last preempted second level batch buffer.</p>	Format:
Format:	GraphicsAddress[47:32]		

Second Level Batch Buffer Upper Head Pointer Register

SBB_ADDR_UDW - Second Level Batch Buffer Upper Head Pointer Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Access:	RO			
Size (in bits):	32			
Address:	0211Ch-0211Fh			
Name:	Second Level Batch Buffer Upper Head Pointer Register			
ShortName:	SBB_ADDR_UDW_RCSUNIT			
Address:	1211Ch-1211Fh			
Name:	Second Level Batch Buffer Upper Head Pointer Register			
ShortName:	SBB_ADDR_UDW_VCSUNIT0			
Address:	1A11Ch-1A11Fh			
Name:	Second Level Batch Buffer Upper Head Pointer Register			
ShortName:	SBB_ADDR_UDW_VECSUNIT			
Address:	1C11Ch-1C11Fh			
Name:	Second Level Batch Buffer Upper Head Pointer Register			
ShortName:	SBB_ADDR_UDW_VCSUNIT1			
Address:	2211Ch-2211Fh			
Name:	Second Level Batch Buffer Upper Head Pointer Register			
ShortName:	SBB_ADDR_UDW_BCSUNIT			
<p>This register contains the current Upper DWord of Graphics Memory Address of the last-initiated batch buffer.</p> <p>Programming Restriction: This register should NEVER be programmed by driver. This is for HW internal use only.</p>				
DWord	Bit	Description		
0	31:16	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
15:0	<p>Batch Buffer Head Pointer Upper DWORD</p> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space where the last initiated Batch Buffer is currently fetching commands. If no batch buffer is currently active, the Valid bit in BB_ADDR will be 0 and this field is meaningless.</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			

Semaphore Polling Interval on Wait

SEMA_WAIT_POLL - Semaphore Polling Interval on Wait				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	RenderCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	0224Ch			
Address:	1224Ch-1224Fh			
Name:	Semaphore Polling Interval on Wait			
ShortName:	SEMA_WAIT_POLL_VCSUNIT0			
Address:	1A24Ch-1A24Fh			
Name:	Semaphore Polling Interval on Wait			
ShortName:	SEMA_WAIT_POLL_VECSUNIT			
Address:	1C24Ch-1C24Fh			
Name:	Semaphore Polling Interval on Wait			
ShortName:	SEMA_WAIT_POLL_VCSUNIT1			
Address:	2224Ch-2224Fh			
Name:	Semaphore Polling Interval on Wait			
ShortName:	SEMA_WAIT_POLL_BCSUNIT			
<p>The SEMA_WAIT_POLL register contains Poll Interval field which specifies the minimum number of microseconds allowed for command streamer to wait before re-fetching the data from the address mentioned in the MI_SEMAPHORE_WAIT command on WAIT Mode set to POLL until the condition is satisfied while the context is not switched out.</p> <p>When a value of 0 is written the poll interval will be equal to the memory latency of the read completion.</p>				
DWord	Bit	Description		
0	31:21	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
20:0	<p>Poll Interval</p> <p>Minimum number of micro-seconds allowed</p>			

SSID_SID

SSID_SID - SSID_SID						
Register Space:	PCI: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0002Ch					
This register is used to uniquely identify the subsystem where the PCI device resides.						
DWord	Bit	Description				
0	31:16	<p>SUBID</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">0000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W Once</td> </tr> </table> <p>This value is used to identify the vendor of the subsystem. This register is programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register is cleared by a Reset.</p>	Default Value:	0000h	Access:	R/W Once
	Default Value:	0000h				
Access:	R/W Once					
15:0	<p>SUBVID</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">0000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W Once</td> </tr> </table> <p>This value is used to identify the vendor of the subsystem. This register is programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register is cleared by a Reset.</p>	Default Value:	0000h	Access:	R/W Once	
Default Value:	0000h					
Access:	R/W Once					

Staggered EU/SAMPLER PAUSE on Frequency Change

GFXPAUSE - Staggered EU/SAMPLER PAUSE on Frequency Change			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0A000h-0A003h		
DWord	Bit	Description	
0	31:19	Reserved	
		Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;"></td><td>RO</td></tr></table> Reserved	
		RO	
	18	Pause Lock	
		Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;"></td><td>R/W Lock</td></tr></table> 0 = Bits of EUPAUSE are R/W 1 = All bits of EUPAUSE are RO (including this lock bit)	
	R/W Lock		
17	EU Pause Enable		
	Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;"></td><td>R/W Lock</td></tr></table> 0 = Disabled; EUs will not be paused during frequency changes 1 = Enabled; EUs will be paused before graphics clocks are gated, and unpaused (staggered per EU) when the clocks are ungated		R/W Lock
	R/W Lock		
16	Sampler Stall Enable		
	Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;"></td><td>R/W Lock</td></tr></table> 0 = Disabled; Sampler will not be paused during frequency changes 1 = Enabled; Sampler will be paused before graphics clocks are gated, and unpaused when the clocks are ungated		R/W Lock
	R/W Lock		
15:0	Pause Count		
	Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;"></td><td>R/W Lock</td></tr></table> This is the minimum time the PMunit waits after asserting the EU or Sampler pause (if those are enabled) before allowing the core clocks to be gated. 0000 = Disabled 0001 - Count 1 CSclk ... FFFF = Count 65535 CSclks		R/W Lock
	R/W Lock		

Storage 1

STORAGE1 - Storage 1				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A500h-0A503h			
DWord	Bit	Description		
0	31:16	<p>Wake Rate Counter Render</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%; text-align: center;">R/W</td> </tr> </table> <p>When reading, this field holds the number of times that the render well has awakened from RC1 (i.e. the number of times that (pmmr_cs_done & ~gmcrgu_gpm_renderpower_req) changes from 1 to 0) within an evaluation interval.</p> <p>When writing this register, set the render wakerate counter to the value written.</p> <p>The only reason to read this register is preparation for S0ix, though it may be useful for validation.</p> <p>The only reason to write to this register is to resume from S0ix.</p>	Access:	R/W
	Access:	R/W		
15:0	<p>Wake Rate Counter Media</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%; text-align: center;">R/W</td> </tr> </table> <p>When reading, this field holds the number of times that the media well has awakened from RC1 (i.e. the number of times that (pmmr_vcs_done & pmmr_bcs_done & ~gmcrgu_gpm_mediapower_req) changes from 1 to 0) within an evaluation interval.</p> <p>When writing this register, set the render wakerate counter to the value written.</p> <p>The only reason to read this register is preparation for S0ix, though it may be useful for validation.</p> <p>The only reason to write to this register is to resume from S0ix.</p>	Access:	R/W	
Access:	R/W			

Storage 2

STORAGE2 - Storage 2		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A504h-0A507h	
DWord	Bit	Description
0	31:24	Reserved Access: RO
	23:0	RC EI Counter Media Access: R/W

Storage 3

STORAGE3 - Storage 3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A508h-0A50Bh	
DWord	Bit	Description
0	31:24	Reserved Access: <input type="text"/> RO
	23:0	RC EI Counter Render Access: <input type="text"/> R/W

Storage 4

STORAGE4 - Storage 4		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A50Ch-0A50Fh	
DWord	Bit	Description
0	31:24	Reserved Access: <input type="text"/> RO
	23:0	RC Idle Counter Media Access: <input type="text"/> R/W

Storage 5

STORAGE5 - Storage 5		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A510h-0A513h	
DWord	Bit	Description
0	31:24	Reserved Access: <input type="text"/> RO
	23:0	RC Idle Counter Render Access: <input type="text"/> R/W

Storage 6

STORAGE6 - Storage 6		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A514h-0A517h	
DWord	Bit	Description
0	31:24	Reserved Access: RO
	23:0	RP EI Up Counter Access: R/W

Storage 7

STORAGE7 - Storage 7		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A518h-0A51Bh	
DWord	Bit	Description
0	31:24	Reserved
		Access: RO
	23:0	RP EI Up Busy Counter
		Access: R/W

Storage 8

STORAGE8 - Storage 8		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A51Ch-0A51Fh	
DWord	Bit	Description
0	31:24	Reserved Access: RO
	23:0	RP EI Down Counter Access: R/W

Storage 9

STORAGE9 - Storage 9		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A520h-0A523h	
DWord	Bit	Description
0	31:24	Reserved Access: RO
	23:0	RP EI Down Busy Counter Access: R/W

Stream Output Num Primitives Written Counter

SO_NUM_PRIMS_WRITTEN[0:3] - Stream Output Num Primitives Written Counter				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	RenderCS			
Default Value:	0x00000000, 0x00000000			
Access:	R/W			
Size (in bits):	64			
Address:	05200h-0521Fh			
<p>There is one 64-bit register for each of the 4 supported streams: 5200h-5207h SO_NUM_PRIMS_WRITTEN0 (for Stream Out Stream #0) 5208h-520Fh SO_NUM_PRIMS_WRITTEN1 (for Stream Out Stream #1) 5210h-5217h SO_NUM_PRIMS_WRITTEN2 (for Stream Out Stream #2) 5218h-521Fh SO_NUM_PRIMS_WRITTEN3 (for Stream Out Stream #3) These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has successfully written to a particular "stream's" Streamed Vertex Output buffers, subject to buffer overflow detection. (See the Stream Output section of the 3D pipeline volume). These registers are part of the context save and restore.</p>				
DWord	Bit	Description		
0	63:0	<p>Num Prims Written Count</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="text-align: center;">U64</td> </tr> </table> <p>This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)</p>	Format:	U64
Format:	U64			

Stream Output Primitive Storage Needed Counters

SO_PRIM_STORAGE_NEEDED[0:3] - Stream Output Primitive Storage Needed Counters						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	RenderCS					
Default Value:	0x00000000, 0x00000000					
Access:	RW. This register is set by the context restore.					
Size (in bits):	64					
Address:	05240h-0525Fh					
<p>There is one 64-bit register for each of the 4 supported streams:</p> <p>5240h-5247h SO_PRIM_STORAGE_NEEDED0 (for Stream Out Stream #0) 5248h-524Fh SO_PRIM_STORAGE_NEEDED1 (for Stream Out Stream #1) 5250h-5257h SO_PRIM_STORAGE_NEEDED2 (for Stream Out Stream #2) 5258h-525Fh SO_PRIM_STORAGE_NEEDED3 (for Stream Out Stream #3)</p> <p>These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has or would have written to a particular "stream's" Streamed Vertex Output buffers if all buffers had been large enough to accommodate the writes. (See the Stream Output section of the 3D pipeline volume).</p> <p>These registers are part of the context save and restore.</p>						
DWord	Bit	Description				
0	63:0	<p>Prim Storage Needed Count</p> <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U64</td> </tr> </table> <p>This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.</p>	Project:	CHV, BSW	Format:	U64
Project:	CHV, BSW					
Format:	U64					

Stream Output Write Offsets

SO_WRITE_OFFSET[0:3] - Stream Output Write Offsets						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	RenderCS					
Default Value:	0x00000000					
Access:	RW. This register is set by the context restore.					
Size (in bits):	32					
Address:	05280h-0528Fh					
<p>There is one R/W 32-bit register for each of the 4 supported stream output buffer slots: 5280h-5283h SO_WRITE_OFFSET0 (for Stream Out Buffer #0) 5284h-5287h SO_WRITE_OFFSET1 (for Stream Out Buffer #1) 5288h-528Bh SO_WRITE_OFFSET2 (for Stream Out Buffer #2) 528Ch-528Fh SO_WRITE_OFFSET3 (for Stream Out Buffer #3)</p> <p>These registers are used to set and track a DWord-granular Write Offset for each of the 4 Stream Output Buffer slots. Software can directly write them via MI_LOAD_REGxxx commands. The SOL stage will increment them as part of stream output processing. Software can cause them to be written to memory via MI_STORE_REGxxx commands. (See the Stream Output section of the 3D pipeline volume).</p> <p>These registers are part of the context save and restore.</p>						
Programming Notes						
<ul style="list-style-type: none"> Software must ensure that no HW stream output operations can be in process or otherwise pending at the point that the MI_LOAD/STORE commands are processed. This will likely require a pipeline flush. The SOL stage will effectively advance the write offset by the buffer's Surface Pitch after each vertex is written (assuming no overflow is detected in any targetted SO buffer). Under "normal" conditions one would expect software to initialize the WriteOffset to some (possibly zero) multiple of Surface Pitch in order to align vertex writes to the buffer's Base Address, though it is not required to do so. 						
DWord	Bit	Description				
0	31:2	<p>Write Offset</p> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U30</td> </tr> </table> <p>This field contains a DWord offset from the corresponding SO buffer's Base Address value. The SOL stage uses this value as a write offset when performing writes to the buffer. The SOL stage will increment this value as a part of performing stream output to the buffer. Note that the SOL stage uses the buffer's Surface Pitch to advance the Write Offset, without regard to the buffer's Base Address (see Programming Notes above).</p>	Project:	CHV, BSW	Format:	U30
	Project:	CHV, BSW				
Format:	U30					
1:0	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ			
Format:	MBZ					

SWF1

SWF1 - SWF1						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F000h					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF2

SWF2 - SWF2						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F004h					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF3

SWF3 - SWF3						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F008h					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF4

SWF4 - SWF4						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F00Ch					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF5

SWF5 - SWF5						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F010h					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF6

SWF6 - SWF6						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F014h					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF7

SWF7 - SWF7						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F018h					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF8

SWF8 - SWF8						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F01Ch					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF9

SWF9 - SWF9						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F020h					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF10

SWF10 - SWF10						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F024h					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF11

SWF11 - SWF11						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F028h					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF12

SWF12 - SWF12						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F02Ch					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF13

SWF13 - SWF13						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F030h					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF14

SWF14 - SWF14						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F034h					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF15

SWF15 - SWF15						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F038h					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF16

SWF16 - SWF16						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F03Ch					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF17

SWF17 - SWF17						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F040h					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF18

SWF18 - SWF18						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F044h					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF19

SWF19 - SWF19						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F048h					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF20

SWF20 - SWF20						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F04Ch					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF21

SWF21 - SWF21						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F050h					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF22

SWF22 - SWF22						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F054h					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF23

SWF23 - SWF23						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F058h					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF24

SWF24 - SWF24						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F05Ch					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF25

SWF25 - SWF25						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F060h					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF26

SWF26 - SWF26						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F064h					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF27

SWF27 - SWF27						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F068h					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF28

SWF28 - SWF28						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F06Ch					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF29

SWF29 - SWF29						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F070h					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF30

SWF30 - SWF30						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F074h					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF31

SWF31 - SWF31						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F078h					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF32

SWF32 - SWF32						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F07Ch					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF33

SWF33 - SWF33						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F080h					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF34

SWF34 - SWF34						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F084h					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF35

SWF35 - SWF35						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F088h					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWF36

SWF36 - SWF36						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	4F08Ch					
<p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>						
DWord	Bit	Description				
0	31:0	<p>SOFTWARE_FLAGS</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

SWSMISCI

SWSMISCI - SWSMISCI			
Register Space:	PCI: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	000E0h		
<p>Software SMI or SCI.</p> <p>The SCI mechanism for driver / BIOS communication. SMI is a system wide lock interrupt (halts all the cores) as opposed to SCI.</p> <p>The SMI is slowly being phased out.</p> <p>This register serves 2 purposes: 1) Support selection of SMI or SCI event source (SMISCISEL - bit15) 2) Event trigger (bit 0).</p> <p>To generate a SW SCI event, software (System BIOS/Graphics driver) should program bit 15 (SMISCISEL) to 1. This is typically programmed once (assuming SMIs are never triggered). On a '0' to '1' subsequent transition in bit 0 of this register (caused by a software write operation), GMCH sends a single SCI message. The SCI will set the DMISCI bit in its TCO1_STS register and TCOSCI_STS bit in its GPE0 register upon receiving this message from DMI.</p> <p>Once written as 1, software must write a '0' to this bit to clear it, and all other write transitions (1->0, 0->0, 1->1) or if bit 15 is '0' will not cause GMCH to send SCI message to DMI link.</p> <p>To generate a SW SMI event, software should program bit 15:0 and trigger SMI.</p>			
DWord	Bit	Description	
0	31:16	RESERVED	
	15	SMI_OR_SCI_EVENT_SELECT	
		Default Value:	0b
		Access:	R/W
			MCS: SMI or SCI event select. 0 = SMI, 1 = SCI
	14:1	SOFTWARE_SCRATCH_BITS	
		Default Value:	0000h
		Access:	R/W
			Used by driver to communicate information to SBIOS
	0	SMI_OR_SCI_EVENT	
Default Value:		0b	
Access:		R/W	
MCE: MCS=1, setting this bit causes an SCI. MCS=0, setting this bit causes an SMI. A 1 to 0, 0 to 0 or 1 to 1 transition of this bit does not trigger any events. The graphics driver writes to this register as a means to interrupt the SBIOS.			

Thread Dispatched Count Register

TDL_THR_DISP_COUNT - Thread Dispatched Count Register					
Register Space:	MMIO: 0/2/0				
Project:	CHV, BSW				
Source:	PRM				
Default Value:	0x00000000				
Access:	RO				
Size (in bits):	32				
Address:	0E4BCh				
Valid Projects:	CHV, BSW				
This register provides the count of threads dispatched/valid in the subslice.					
DWord	Bit	Description			
0	31:6	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
	Format:	MBZ			
5:0	Thread Count <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0-56</td> <td>Valid Range</td> </tr> </tbody> </table>	Value	Name	0-56	Valid Range
Value	Name				
0-56	Valid Range				

Thread Faulted Count Register

TDL_THR_PF_COUNT - Thread Faulted Count Register					
Register Space:	MMIO: 0/2/0				
Project:	CHV, BSW				
Source:	PRM				
Default Value:	0x00000000				
Access:	RO				
Size (in bits):	32				
Address:	0E5BCh				
Valid Projects:	CHV, BSW				
This register provides the count of threads faulted in each subslice.					
DWord	Bit	Description			
0	31	Canonical fault indication bit to CS The bit is set when a canonical fault on data fetch is reported by EU.			
	30:6	Reserved Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px; height: 15px;"></td><td style="width: 50px; text-align: center;">MBZ</td></tr></table>		MBZ	
		MBZ			
5:0	Thread Count <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>0-56</td> <td>Valid Range</td> </tr> </tbody> </table>	Value	Name	0-56	Valid Range
Value	Name				
0-56	Valid Range				

Thread Fault Status Register 0

TDL_THR_PF_STATUS0 - Thread Fault Status Register 0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	0E6B8h	
This register provides the status of each thread in the SubSlice. A bit set indicates the thread in the specific thread slot is faulted.		
DWord	Bit	Description
0	31:24	Row0, EU3, [Reserved, T6-T0]
	23:16	Row0, EU2, [Reserved, T6-T0]
	15:8	Row0, EU1, [Reserved, T6-T0]
	7:0	Row0, EU0, [Reserved, T6-T0]

Thread Fault Status Register 1

TDL_THR_PF_STATUS1 - Thread Fault Status Register 1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	0E7B8h	
This register provides the status of each thread in the SubSlice. A bit set indicates the thread in the specific thread slot is faulted.		
DWord	Bit	Description
0	31:24	Row1, EU3, [Reserved, T6-T0]
	23:16	Row1, EU2, [Reserved, T6-T0]
	15:8	Row1, EU1, [Reserved, T6-T0]
	7:0	Row1, EU0, [Reserved, T6-T0]

Thread Load Status Register 0

TDL_THR_STATUS0 - Thread Load Status Register 0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	0E4B8h	
This register provides the status of each thread in the SubSlice.		
DWord	Bit	Description
0	31:24	Row0, EU3, [Reserved, T6-T0]
	23:16	Row0, EU2, [Reserved, T6-T0]
	15:8	Row0, EU1, [Reserved, T6-T0]
	7:0	Row0, EU0, [Reserved, T6-T0]

Thread Load Status Register 1

TDL_THR_STATUS1 - Thread Load Status Register 1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	0E5B8h	
This register provides the status of each thread in the SubSlice. A bit set indicates a valid thread is loaded in the thread slot.		
DWord	Bit	Description
0	31:24	Row1, EU3, [Reserved, T6-T0]
	23:16	Row1, EU2, [Reserved, T6-T0]
	15:8	Row1, EU1, [Reserved, T6-T0]
	7:0	Row1, EU0, [Reserved, T6-T0]

Thread Mode Register

FF_MODE - Thread Mode Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	RenderCS			
Default Value:	0x00A00000 CHV, BSW			
Access:	R/W			
Size (in bits):	32			
Address:	020A0h			
Valid Projects:				
This register is used to program the FF shader Mode.				
DWord	Bit	Description		
0	31	Reserved		
		Project:	CHV, BSW	
		Format:	MBZ	
	30	TDS external Cache Disable		
		Project:	CHV, BSW	
		Value	Name	Description
		0b	Enable [Default]	The external TDS Cache is enabled if there is enough handles to enable the cache.
		1b	Disable	The external TDS Cache is disabled even if there is enough handles to enable the cache. Only the internal TDS Cache will be used.
	29:26	DS Hit Max Value		
		Format:	U4	
Description		Project		
If the number of hits reaches the DS Hit Max Value and there is a pending miss to be dispatched, the DS will dispatch the pending miss vertex as a single dispatch.				
Programming the value beyond the range will have undefined behavior if DS Reference Count Full Force miss enable is 0. When DS Reference Count Full Force miss enable is 1 then the value can be [1, Fh].		CHV, BSW		
Value		Name	Project	
9		[Default]	CHV, BSW	
[1,9]		CHV, BSW		

FF_MODE - Thread Mode Register

25:20	VS Hit Max Value		
		Format:	U6
Description			
<p>If the number of hits reaches the VS Hit Max Value and there is a pending miss to be dispatched, the VS will dispatch the pending miss vertex as a single dispatch.</p> <p>Programming the value beyond the range will have undefined behavior if VS Reference Count Full Force miss enable is 0. When VS Reference Count Full Force miss enable is 1 then the value can be [1,3Fh].</p>			
		Value	Name
		10	[Default]
		[1,26]	
19	DS Reference Count Full Force Miss Enable		
		Project:	CHV, BSW
		Format:	Enable
		Value	Name
		0b	[Default]
		1b	
Description			
<p>On a hit to the DS cache and the associated handle's reference count is full then stall until a dereference.</p> <p>On a hit to the DS cache and the associated handle's reference count is full then force the cycle as a miss and allocate a new handle.</p>			
Programming Notes			
To work around bugs, this must be set to 0.			
18	Reserved		
17:16	Reserved		
15	VS Reference Count Full Force Miss Enable		
		Format:	U1
		Value	Name
		[0,1]	
		0b	[Default]
		1b	
Description			
<p>On a hit to the VS cache and the associated handle's reference count is full then stall until a dereference.</p> <p>On a hit to the VS cache and the associated handle's reference count is full then force the cycle as a miss and allocate a new handle.</p>			
Programming Notes			Project
To work around bugs, this must be set to 0.			CHV, BSW

FF_MODE - Thread Mode Register

	14:13	Reserved	
		Project:	CHV, BSW
		Format:	MBZ
	12	Reserved	
		Default Value:	0h
		Project:	CHV, BSW
		Format:	MBZ
	11:7	Reserved	
		Format:	MBZ
	6:5	Reserved	
		Project:	CHV, BSW
		Format:	MBZ
	4	Reserved	
		Default Value:	0h
Project:		CHV, BSW	
Format:		MBZ	
3:0	Reserved		
	Format:	MBZ	

Thread Restart Control Register

TDL_THR_RESTART - Thread Restart Control Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Access:	WO			
Size (in bits):	32			
Address:	0E450h			
This register provides control to restart page faulted and halted threads in each subslice.				
DWord	Bit	Description		
0	31:1	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
0	Restart All Faulted Threads A write of 1 to this register restarts all threads that have halted due to page fault.			

TILECTL

TILECTL - TILECTL			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	101000h		
DWord	Bit	Description	
0	31:3	Reserved	
		Default Value:	00000000h
		Access:	RO
		Reserved	
2	2	Reserved	
		Default Value:	0b
		Access:	RO
		Reserved.	
1	1	TLBPF	
		Default Value:	0b
		Access:	R/W
		Store multiple PTE enable 0: Only one Page Table Entry is stored in the Translation Lookaside Table Entry is stored in the Translation Lookaside Buffer cache for tiled cycles. 1: Multiple Page Table Entries are stored in the Translation Lookaside Buffer cache for tiled cycles. If tileX, then 4 entries are stored. If tileY, then 8 entries are stored.	
0	0	SWZCTL	
		Default Value:	0b
		Access:	R/W
		Not used for CHV, BSW. This register location is updated via GFX Driver prior to enabling DRAM accesses. The Driver needs to obtain the need for memory address swizzling via DRAM configuration registers and set the following bits. x0b - No Address Swizzling x1b - Address bit [6] needs to be swizzled for tiled surfaces	

TiledResources Invalid Tile Detection Register

TRINVTILEDETCT - TiledResources Invalid Tile Detection Register										
Register Space:	MMIO: 0/2/0									
Source:	PRM									
Default Value:	0x00000000									
Size (in bits):	32									
Address:	04DECh									
Name:	TiledResources Invalid Tile Detection Register									
ShortName:	TRINVTILEDETCT									
DWord	Bit	Description								
0	31:0	Invalid Tile Detection Value <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> <tr> <td>00000000h</td> <td>[Default]</td> <td>A 32bit value programmed to enable h/w to perform a match of TR-VA TT entries to detect Invalid Tiles. Hardware will flag each entry and space behind it as Invalid Tile for matched entries.</td> </tr> </table>	Access:	R/W	Value	Name	Description	00000000h	[Default]	A 32bit value programmed to enable h/w to perform a match of TR-VA TT entries to detect Invalid Tiles. Hardware will flag each entry and space behind it as Invalid Tile for matched entries.
Access:	R/W									
Value	Name	Description								
00000000h	[Default]	A 32bit value programmed to enable h/w to perform a match of TR-VA TT entries to detect Invalid Tiles. Hardware will flag each entry and space behind it as Invalid Tile for matched entries.								

Tiled Resources Translation Table Control Registers

TRTTE - Tiled Resources Translation Table Control Registers						
Register Space:	MMIO: 0/2/0					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04DF4h					
Name:	Tiled Resources Translation Table Control Register					
ShortName:	TRTTE					
DWord	Bit	Description				
0	31:2	Reserved				
		Access: RO				
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0000000000000000000000000000000b</td> <td>[Default]</td> <td>Reserved</td> </tr> </tbody> </table>	Value	Name	Description	0000000000000000000000000000000b
Value	Name	Description				
0000000000000000000000000000000b	[Default]	Reserved				
1		TR-VA Translation Table Memory Location				
		Default Value: 0b				
		Access: R/W				
This field specifies whether the translation tables for TR to VA are in virtual address space v/s physical (GPA) address space. 0: Tables are in Physical (GPA) space 1: Tables are in Virtual address space						
0		TR - TT Enable				
		Default Value: 0b				
		Access: R/W				
TR translation tables are disabled as default. This field needs to be enabled via s/w to get TR translation active.						

TiledResources VA Detection Registers

TRVADR - TiledResources VA Detection Registers						
Register Space:	MMIO: 0/2/0					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04DF0h					
Name:	TiledResources VA Detection Registers					
ShortName:	TRVADR					
DWord	Bit	Description				
0	31:8	Reserved				
		Default Value:	000000h			
		Access:	RO			
	7:4	TR - VA Mask Value				
		Default Value:	0000b			
		Access:	R/W			
		<p>4bit MASK value that is mapped to incoming address bits[47:44] MASK bits are used to identify which address bits need to be considered for compare. If particular mask bit is "1", mapping address bit needs to be compared to DATA value provided. If "0", corresponding address bit is masked which makes it don't care for compare. (This field defaults to "0000" to disable detection). Note: The only usage model for GFX driver to set this field to "1111". Behaviour of h/w for any other setiing is not defined. Note: GFX driver shall use same TRVA MASK value for all contexts.</p>				
	3:0	TR- VA Data Value				
		Access:	R/W			
<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>[Default]</td> <td>4bit Data value that is mapped to incoming address bits[47:44]. Data bits are used to compare address values that are not filtered by the TRVAMV for match Note: GFX driver shall use same TRVA Data value for all contexts</td> </tr> </tbody> </table>		Value	Name	Description	0000b	[Default]
Value	Name	Description				
0000b	[Default]	4bit Data value that is mapped to incoming address bits[47:44]. Data bits are used to compare address values that are not filtered by the TRVAMV for match Note: GFX driver shall use same TRVA Data value for all contexts				

Tiled Resources VA Translation Table L3 ptr - DW0

TRVATTL3PTRDW0 - Tiled Resources VA Translation Table L3 ptr - DW0								
Register Space:	MMIO: 0/2/0							
Source:	PRM							
Default Value:	0x00000000							
Size (in bits):	32							
Address:	04DE0h							
Name:	Tiled Resources VA Translation Table L3 ptr - DW0							
ShortName:	TRVATTL3PTRDW0							
DWord	Bit	Description						
0	31:12	TR - VA transln Table L3 Pointer (Lower Address)						
		Access: R/W						
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00000h</td> <td>[Default]</td> <td>Lower address bits for tiled resource VA to virtual address translation L3 table</td> </tr> </tbody> </table>	Value	Name	Description	00000h	[Default]	Lower address bits for tiled resource VA to virtual address translation L3 table
		Value	Name	Description				
00000h	[Default]	Lower address bits for tiled resource VA to virtual address translation L3 table						
11:0	Reserved							
		Default Value: 000h						
		Access: RO						
		Reserved						

Tiled Resources VA Translation Table L3 ptr - DW1

TRVATTL3PTRDW1 - Tiled Resources VA Translation Table L3 ptr - DW1								
Register Space:	MMIO: 0/2/0							
Source:	PRM							
Default Value:	0x00000000							
Size (in bits):	32							
Address:	04DE4h							
Name:	Tiled Resources VA Translation Table L3 ptr - DW1							
ShortName:	TRVATTL3PTRDW1							
DWord	Bit	Description						
0	31:16	Reserved						
		Access: RO						
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0000h</td> <td>[Default]</td> <td>Reserved</td> </tr> </tbody> </table>	Value	Name	Description	0000h	[Default]	Reserved
		Value	Name	Description				
0000h	[Default]	Reserved						
	15:0	TR - VA transln Table L3 Pointer (Upper Address)						
		Default Value: 0000h						
		Access: R/W						
		Upper address bits for tiled resource VA to virtual address translation L3 table						

TLB_RD_ADDRESS Register

TLB_RD_ADDR - TLB_RD_ADDRESS Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B00h	
DWord	Bit	Description
0	31:12	Reserved
		Default Value: 00000000000000000000b
	Access: RO	
	11:0	Reserved

TLB_RD_DATA0 Register

TLB_RD_DATA0 - TLB_RD_DATA0 Register						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B04h					
DWord	Bit	Description				
0	31:0	TLB_READ_DATA0 Register <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> address [43:12]	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

TLB_RD_DATA1 Register

TLB_RD_DATA1 - TLB_RD_DATA1 Register			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	04B08h		
DWord	Bit	Description	
0	31:0	TLB_READ_DATA1 Register	
		Default Value:	00000000h
		Access:	RO
		Bit[31:5] Reserved Bit[4] Cycle GTT SEL (1-GGTT Cycle, 0-PPGTT Cycle) Bit[3:0] address [47:44]	

Transcode Attack Status Register

TRANS_STAT - Transcode Attack Status Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	09034h	
Transcode Attack Status Register		
DWord	Bit	Description
0	31:1	RSVD
		Access: RO RSVD
0	0	GKEYS_STATUS
		Access: RO Transcode Attack Status bit

TRNULLDETCT

REG_TEMPLATE - TRNULLDETCT										
Register Space:	MMIO: 0/2/0									
Source:	PRM									
Default Value:	0x00000000									
Size (in bits):	32									
Address:	04DE8h									
Name:	TiledResources Null Tile Detection Register									
ShortName:	TRNULLDETCT									
DWord	Bit	Description								
0	31:0	<p>Null Tile Detection Value</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> <tr> <td>00000000h</td> <td>[Default]</td> <td>A 32bit value programmed to enable h/w to perform a match of TR-VA TT entries to detect Null Tiles. Hardware will flag each entry and space behind it as Null Tile for matched entries.</td> </tr> </table>	Access:	R/W	Value	Name	Description	00000000h	[Default]	A 32bit value programmed to enable h/w to perform a match of TR-VA TT entries to detect Null Tiles. Hardware will flag each entry and space behind it as Null Tile for matched entries.
Access:	R/W									
Value	Name	Description								
00000000h	[Default]	A 32bit value programmed to enable h/w to perform a match of TR-VA TT entries to detect Null Tiles. Hardware will flag each entry and space behind it as Null Tile for matched entries.								

Turbo Media Control

TMCTL - Turbo Media Control				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A190h-0A193h			
DWord	Bit	Description		
0	31:9	Reserved Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;"></td><td style="text-align: center;">RO</td></tr></table>		RO
		RO		
	8	Bypass Media Idle Hysteresis Enable (aka Slice Shutdown) Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;"></td><td style="text-align: center;">R/W</td></tr></table> 1 - Bypass idle hysteresis requirements for making an RC wish. 0 - Honor idle hysteresis <default>		R/W
		R/W		
7:1	Reserved Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;"></td><td style="text-align: center;">RO</td></tr></table>		RO	
	RO			
0	Bypass Render Idle Hysteresis Enable (aka Slice Shutdown) Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 100px;"></td><td style="text-align: center;">R/W</td></tr></table> 1 - Bypass idle hysteresis requirements for making an RC wish. 0 - Honor idle hysteresis <default>		R/W	
	R/W			

Unblock Message Act to Busy Detection Timer

RCUBMABDTMR - Unblock Message Act to Busy Detection Timer				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A0B0h-0A0B3h			
<p>When locked exit policy is chosen, the GT core can be woken up in parallel with the IA cores waking up so an MMIO write to GT core might not be coming, or may be later in coming. If after the time programmed in this register is met and graphics is still idle, then RC1(e)/RC6x is allowed to be entered.</p> <p>0 = 0 usec 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec pmcr_rc_sleep[23:0]</p>				
DWord	Bit	Description		
0	31:24	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved</p>	Access:	RO
	Access:	RO		
23:0	<p>Unblock Message Ack to Busy Detection Timer</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>When locked exit policy is chosen, the GT core can be woken up in parallel with the IA cores waking up so an MMIO write to GT core might not be coming, or may be later in coming. If after the time programmed in this register is met and graphics is still idle, then RC1(e)/RC6x is allowed to be entered.</p> <p>0 = 0 usec 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec pmcr_rc_sleep[23:0]</p>	Access:	R/W	
Access:	R/W			

Unit Level Clock Gating Control 1

UCGCTL1 - Unit Level Clock Gating Control 1				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x02800000			
Size (in bits):	32			
Address:	09400h			
Unit Level Clock Gating Control Registers.Refer to the Programming notes mentioned near GT Interface Registers in PRM				
DWord	Bit	Description		
0	31	<p>Sarbunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>SARB unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
	Access:	R/W		
	30	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Access:	R/W
	Access:	R/W		
	29	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Access:	R/W
	Access:	R/W		
28	<p>ICunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>ICunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			
27	<p>HIZunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>HIZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			
26	<p>GWunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>GWunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			

UCGCTL1 - Unit Level Clock Gating Control 1

25	<p>GTUnit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">1b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>GTI Units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				
24	<p>GSunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>GSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
23	<p>GPMunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">1b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>GPMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				
22	<p>GAMunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>GAMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
21	<p>GACunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>GACunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				

UCGCTL1 - Unit Level Clock Gating Control 1

20	<p>GABunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>GABunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
19	<p>FTunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>FTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
18	<p>FLunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>FLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
17	<p>EU_FPUunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>EU_FPUunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
16	<p>EU_TCunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>EU_TCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
15	<p>EU_EMunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>EU_EMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				

UCGCTL1 - Unit Level Clock Gating Control 1

14	<p>EU_GAunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>EU_GAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
13	<p>EUunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>EUunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
12	<p>SVLunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>SVLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
11	<p>DTunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>DTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
10	<p>DMunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>DMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
9	<p>DGunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>DGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL1 - Unit Level Clock Gating Control 1

8	<p>DAPunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>DAPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
7	<p>CSunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>CSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
6	<p>CLunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>CLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
5	<p>BLBunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>BLBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
4	<p>BFunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>BFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
3	<p>BDunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>BDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL1 - Unit Level Clock Gating Control 1

2	<p>BCSunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%; text-align: center;">R/W</td> </tr> </table> <p>BCSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
1	<p>AVSunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%; text-align: center;">R/W</td> </tr> </table> <p>AVSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
0	<p>SPARE RAM Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%; text-align: center;">R/W</td> </tr> </table> <p>SPARE RAM Clock Gating Disable Control: '0' : RAM Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : RAM Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

Unit Level Clock Gating Control 1

UCGCTL1 - Unit Level Clock Gating Control 1				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x02F00000			
Size (in bits):	32			
Address:	09400h			
Unit Level Clock Gating Control Registers.				
DWord	Bit	Description		
0	31	<p>Sarbunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>SARB unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
	Access:	R/W		
	30	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Access:	R/W
	Access:	R/W		
	29	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Access:	R/W
	Access:	R/W		
28	<p>ICunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>ICunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			
27	<p>HIZunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>HIZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			
26	<p>GWunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>GWunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			

UCGCTL1 - Unit Level Clock Gating Control 1

25	<p>GTUnit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">1b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>GTI Units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				
24	<p>GSunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>GSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
23	<p>GPMunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">1b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>GPMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				
22	<p>GAMunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">1b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>GAMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				
21	<p>GACunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">1b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>GACunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				
20	<p>GABunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">1b</td> </tr> </table>	Default Value:	1b		
Default Value:	1b				

UCGCTL1 - Unit Level Clock Gating Control 1

	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>GABunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
19	<p>FTunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>FTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
18	<p>FLunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>FLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
17	<p>EU_FPUunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>EU_FPUunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
16	<p>EU_TCunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>EU_TCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
15	<p>EU_EMunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>EU_EMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL1 - Unit Level Clock Gating Control 1

14	<p>EU_GAunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>EU_GAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
13	<p>EUunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>EUunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
12	<p>SVLunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>SVLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
11	<p>DTunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>DTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
10	<p>DMunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>DMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
9	<p>DGunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>DGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL1 - Unit Level Clock Gating Control 1

8	<p>DAPunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>DAPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
7	<p>CSunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>CSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
6	<p>CLunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>CLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
5	<p>BLBunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>BLBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
4	<p>BFunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>BFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
3	<p>BDunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>BDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL1 - Unit Level Clock Gating Control 1			
2	<p>BCSunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>BCSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
1	<p>AVSunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>AVSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
0	<p>SPARE RAM Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>SPARE RAM Clock Gating Disable Control: '0' : RAM Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : RAM Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

Unit Level Clock Gating Control 2

UCGCTL2 - Unit Level Clock Gating Control 2				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	09404h			
Unit Level Clock Gating Control Registers.Refer to the Programming notes mentioned near GT Interface Registers in PRM				
DWord	Bit	Description		
0	31	VFunit Clock Gating Disable <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> VFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	Access:	R/W
	Access:	R/W		
	30	VDSunit Clock Gating Disable <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> VDSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	Access:	R/W
	Access:	R/W		
29	VDIunit Clock Gating Disable <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> VDIunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	Access:	R/W	
Access:	R/W			
28	VCSunit Clock Gating Disable <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> VCSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	Access:	R/W	
Access:	R/W			

UCGCTL2 - Unit Level Clock Gating Control 2

27	<p>DTOunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>DTOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
26	<p>VCPunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VCPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
25	<p>VCDunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VCDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
24	<p>URBMunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>URBMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
23	<p>TSGunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>TSGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
22	<p>TDLunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>TDLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL2 - Unit Level Clock Gating Control 2

21	<p>TDSunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>TDSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
20	<p>SVSMunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>SVSMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
19	<p>SVGunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>SVGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
18	<p>SOunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>SOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
17	<p>Slunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Slunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
16	<p>SFunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>SFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL2 - Unit Level Clock Gating Control 2

15	<p>SECunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%; text-align: center;">R/W</td> </tr> </table> <p>SECunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
14	<p>SCunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%; text-align: center;">R/W</td> </tr> </table> <p>SCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
13	<p>RCZunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%; text-align: center;">R/W</td> </tr> </table> <p>RCZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
12	<p>RCPBunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%; text-align: center;">R/W</td> </tr> </table> <p>RCPBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
11	<p>RCCunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%; text-align: center;">R/W</td> </tr> </table> <p>RCCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
10	<p>QCunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%; text-align: center;">R/W</td> </tr> </table> <p>QCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL2 - Unit Level Clock Gating Control 2

9	<p>PSDunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>PSDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
8	<p>PLunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>PLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
7	<p>MTunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>MTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
6	<p>MPCunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>MPCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
5	<p>TDGunitClock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>TDGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
4	<p>MSCunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>MSCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL2 - Unit Level Clock Gating Control 2

3	<p>TEunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>TEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
2	<p>TETGunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>TETGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
1	<p>MAunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>MAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
0	<p>IZunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>IZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

Unit Level Clock Gating Control 2

UCGCTL2 - Unit Level Clock Gating Control 2				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	09404h			
Unit Level Clock Gating Control Registers.				
DWord	Bit	Description		
0	31	<p>VFunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
	Access:	R/W		
	30	<p>VDSunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VDSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
	Access:	R/W		
29	<p>VDlunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VDlunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			
28	<p>VCSunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VCSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			

UCGCTL2 - Unit Level Clock Gating Control 2

27	<p>DTOunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>DTOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
26	<p>VCPunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>VCPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
25	<p>VCDunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>VCDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
24	<p>URBMunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>URBMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
23	<p>TSGunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>TSGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
22	<p>TDLunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>TDLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL2 - Unit Level Clock Gating Control 2

21	<p>TDSunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>TDSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
20	<p>SVSMunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>SVSMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
19	<p>SVGunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>SVGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
18	<p>SOunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>SOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
17	<p>Slunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Slunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
16	<p>SFunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>SFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL2 - Unit Level Clock Gating Control 2

15	<p>SECunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>SECunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
14	<p>SCunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>SCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
13	<p>RCZunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>RCZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
12	<p>RCPBunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>RCPBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
11	<p>RCCunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>RCCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
10	<p>QCunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>QCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL2 - Unit Level Clock Gating Control 2

9	<p>PSDunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>PSDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
8	<p>PLunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>PLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
7	<p>MTunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>MTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
6	<p>MPCunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>MPCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
5	<p>TDGunitClock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>TDGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
4	<p>MSCunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>MSCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL2 - Unit Level Clock Gating Control 2

3	<p>TEunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>TEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
2	<p>TETGunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>TETGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
1	<p>MAunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>MAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
0	<p>IZunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>IZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

Unit Level Clock Gating Control 3

UCGCTL3 - Unit Level Clock Gating Control 3				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000 [CHV:B, CHV:C, CHV:K] 0x04000000 [CHV:A]			
Size (in bits):	32			
Address:	09408h			
Unit Level Clock Gating Control Registers.Refer to the Programming notes mentioned near GT Interface Registers in PRM				
DWord	Bit	Description		
0	31	<p>Flunits 2nd Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Flunits 2nd Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
	Access:	R/W		
	30	<p>SVRRunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>SVRRunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
	Access:	R/W		
29	<p>VCRunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VCRunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			
28	<p>EDTunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>EDTunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			

UCGCTL3 - Unit Level Clock Gating Control 3

27	<p>VClunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>VClunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W				
Access:	R/W						
26	<p>HEVC DOP Gating Enable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td style="text-align: center;">1b</td> </tr> <tr> <td>Project:</td> <td style="text-align: center;">CHV, BSW</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>HEVCUNIT' Clock Gating Enable Control: '0' : VIDPAR8/VIDPAR9 DOP gating is not affected by this bit (i.e., this bit does not affect functional DOP gating) '1' : VIDPAR8/VIDPAR9 cmclk/cuclk DOP's are gated. (i.e., functional clocks aren't toggling, always)</p>	Default Value:	1b	Project:	CHV, BSW	Access:	R/W
Default Value:	1b						
Project:	CHV, BSW						
Access:	R/W						
26	<p>HEVC DOP Gating Enable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Project:</td> <td style="text-align: center;">CHV, BSW</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>HEVCUNIT' Clock Gating Enable Control: '0' : VIDPAR8/VIDPAR9 DOP gating is not affected by this bit (i.e., this bit does not affect functional DOP gating) '1' : VIDPAR8/VIDPAR9 cmclk/cuclk DOP's are gated. (i.e., functional clocks aren't toggling, always)</p>	Default Value:	0b	Project:	CHV, BSW	Access:	R/W
Default Value:	0b						
Project:	CHV, BSW						
Access:	R/W						
25	<p>HSunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>HSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W				
Access:	R/W						
24	<p>SOLunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>SOLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W				
Access:	R/W						

UCGCTL3 - Unit Level Clock Gating Control 3

23	<p>QRCunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>QRCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
22	<p>MSPBISTunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>MSPBISTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
21	<p>BSPunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>BSPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
20	<p>Reserved</p>		
19	<p>SBEunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>SBEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
18	<p>BCunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>BCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
17	<p>WMBE Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>WMBEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL3 - Unit Level Clock Gating Control 3

16	<p>WMFEunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>WMFEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
15	<p>VSCunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>VSCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
14	<p>Reserved</p>		
13	<p>USBunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>USBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
12	<p>STCunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>STCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
11	<p>VSunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>VSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
10	<p>VOPunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>VOPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL3 - Unit Level Clock Gating Control 3

9	<p>VMXunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VMXunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
8	<p>VMEunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VMEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
7	<p>VMDunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VMDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
6	<p>VMCunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VMCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
5	<p>VLFunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VLFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
4	<p>VITunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VITunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL3 - Unit Level Clock Gating Control 3

3	<p>VIPunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VIPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
2	<p>VINunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VINunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
1	<p>VFTunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VFTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
0	<p>VFEunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VFEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

Unit Level Clock Gating Control 3

UCGCTL3 - Unit Level Clock Gating Control 3				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x04000000			
Size (in bits):	32			
Address:	09408h			
Unit Level Clock Gating Control Registers.				
DWord	Bit	Description		
0	31	<p>Flunits 2nd Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Flunits 2nd Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
	Access:	R/W		
	30	<p>SVRRunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>SVRRunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
	Access:	R/W		
29	<p>VCRunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VCRunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			
28	<p>EDTunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>EDTunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			

UCGCTL3 - Unit Level Clock Gating Control 3

27	<p>VClunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>VClunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
26	<p>2x Assign fub XOR Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td style="text-align: center;">1b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>2x Assign fub XOR Clock Gating Disable Control: '0' : 2x Assign fub XOR Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : 2x Assign fub XOR Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				
25	<p>HSunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>HSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
24	<p>SOLunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>SOLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
23	<p>QRCunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>QRCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
22	<p>MSPBISTunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>MSPBISTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				

UCGCTL3 - Unit Level Clock Gating Control 3

21	<p>BSPunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>BSPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
20	<p>OACSunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>OACSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
19	<p>SBEunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>SBEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
18	<p>BCunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>BCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
17	<p>WMBEunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>WMBEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
16	<p>WMFEunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>WMFEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL3 - Unit Level Clock Gating Control 3

15	<p>VSCunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>VSCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
14	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table>	Access:	R/W
Access:	R/W		
13	<p>USBunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>USBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
12	<p>STCunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>STCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
11	<p>VSunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>VSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
10	<p>VOPunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>VOPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL3 - Unit Level Clock Gating Control 3

9	<p>VMXunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>VMXunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
8	<p>VMEunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>VMEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
7	<p>VMDunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>VMDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
6	<p>VMCunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>VMCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
5	<p>VLFunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>VLFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
4	<p>VITunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>VITunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL3 - Unit Level Clock Gating Control 3

3	<p>VIPunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%; text-align: center;">R/W</td> </tr> </table> <p>VIPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
2	<p>VINunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%; text-align: center;">R/W</td> </tr> </table> <p>VINunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
1	<p>VFTunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%; text-align: center;">R/W</td> </tr> </table> <p>VFTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
0	<p>VFEunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%; text-align: center;">R/W</td> </tr> </table> <p>VFEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

Unit Level Clock Gating Control 4

UCGCTL4 - Unit Level Clock Gating Control 4			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00F80003		
Size (in bits):	32		
Address:	0940Ch		
Unit Level Clock Gating Control Registers.Refer to the Programming notes mentioned near GT Interface Registers in PRM			
DWord	Bit	Description	
0	31:30	Reserved	
		Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td style="width: 50px; text-align: center;">RO</td></tr></table>	
		RO	
	Reserved.		
	29	GAFSRRB unit Clock Gate Disable	
Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td style="width: 50px; text-align: center;">R/W</td></tr></table>			R/W
	R/W		
GAFSRRB units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
28	RAMDFT units Clock Gate Disable		
	Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td style="width: 50px; text-align: center;">R/W</td></tr></table>		R/W
	R/W		
RAMDFT units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
27	TDCunit Clock Gate Disable		
	Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td style="width: 50px; text-align: center;">R/W</td></tr></table>		R/W
	R/W		
TDCunit Clock Gating Disable Control : '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
26	L3 CBR 1x Clock Gate Disable		
	Access: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td style="width: 50px; text-align: center;">R/W</td></tr></table>		R/W
	R/W		
L3 CBR units 1x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			

UCGCTL4 - Unit Level Clock Gating Control 4

25	<p>L3 BANK 2x Clock Gate Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>L3 BANK units 2x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
24	<p>L3 BANK 1x Clock Gate Diable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>L3 BANK units 1x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
23	<p>MBGFunit Clock Gate Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td style="text-align: center;">1b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>MBGFunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				
22	<p>MSQDunit 2x Clock Gate Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td style="text-align: center;">1b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>MSQD units cu2x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				
21	<p>MSQDunit Clock Gate Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td style="text-align: center;">1b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>MSQD units 1x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				
20	<p>MISDunits 2x Clock Gate Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td style="text-align: center;">1b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>MISDunits cu2x Clock Gating Disable Control:</p>	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				

UCGCTL4 - Unit Level Clock Gating Control 4

		<p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	
19	MISDunit Clock Gate Disable		
	Default Value:	1b	
	Access:	R/W	
	<p>MISDunits 1x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
18	GAFMunit Clock Gate Disable		
	Access:	R/W	
	<p>GAFMunit' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
17	GAPCunit Clock Gate Disable		
	Access:	R/W	
	<p>GAPCunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
16	GAPZunit Clock Gate Disable		
	Access:	R/W	
	<p>GAPZunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
15	GAPL3unit Clock Gate Disable		
	Access:	R/W	
	<p>GAPL3 units' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		

UCGCTL4 - Unit Level Clock Gating Control 4

14	<p>GAFSunit Clock Gate Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>GAFSunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
13	<p>GAHSunit Clock Gate Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>GAHSunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
12	<p>VISunit Clock Gate Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VISunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
11	<p>VACunit Clock Gate Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VACunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
10	<p>VAMunit Clock Gate Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VAMunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
9	<p>VADunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VADunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL4 - Unit Level Clock Gating Control 4

8	<p>JPGunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>JPGunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
7	<p>VBPunits Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VBPunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
6	<p>VHRunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VHRunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
5	<p>VID4 VINunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VID4 VINunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
4	<p>VID3 VINunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VID3 VINunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
3	<p>VID2 VINunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VID2 VINunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL4 - Unit Level Clock Gating Control 4

2	VID1 VINunit Clock Gating Disable	
	Access:	R/W
	VID1 VINunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
1:0	MSQCunit Clock Gating Disable	
	Default Value:	11b
	Access:	R/W
	MSQCunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

Unit Level Clock Gating Control 4

UCGCTL4 - Unit Level Clock Gating Control 4		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00F80003	
Size (in bits):	32	
Address:	0940Ch	
Unit Level Clock Gating Control Registers.		
DWord	Bit	Description
0	31:30	Reserved
		Access: RO
		rsvd
		29 GAFSRRB unit Clock Gate Disable
		Access: R/W
		GAFSRRB units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
28		RAMDFT units Clock Gate Disable
		Access: R/W
		RAMDFT units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
27		L3 CBR 2x Clock Gate Disable
		Access: R/W
		L3 CBR units 2x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
26		L3 CBR 1x Clock Gate Disable
		Access: R/W
		L3 CBR units 1x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL4 - Unit Level Clock Gating Control 4

25	<p>L3 BANK 2x Clock Gate Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>L3 BANK units 2x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
24	<p>L3 BANK 1x Clock Gate Diable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>L3 BANK units 1x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
23	<p>MBGFunit Clock Gate Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>MBGFunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				
22	<p>MSQDunit 2x Clock Gate Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>MSQD units cu2x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				
21	<p>MSQDunit Clock Gate Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>MSQD units 1x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				
20	<p>MISDunits 2x Clock Gate Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>MISDunits cu2x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				

UCGCTL4 - Unit Level Clock Gating Control 4

19	<p>MISDunit Clock Gate Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>MISDunits 1x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				
18	<p>GAFMunit Clock Gate Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>GAFMunit' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
17	<p>GAPCunit Clock Gate Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>GAPCunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
16	<p>GAPZunit Clock Gate Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>GAPZunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
15	<p>GAPL3unit Clock Gate Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>GAPL3 units' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
14	<p>GAFSunit Clock Gate Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>GAFSunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				

UCGCTL4 - Unit Level Clock Gating Control 4

13	<p>GAHSunit Clock Gate Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>GAHSunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
12	<p>VISunit Clock Gate Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VISunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
11	<p>VACunit Clock Gate Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VACunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
10	<p>VAMunit Clock Gate Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VAMunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
9	<p>VADunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VADunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
8	<p>JPGunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>JPGunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL4 - Unit Level Clock Gating Control 4

7	<p>VBPunits Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VBPunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
6	<p>VHRunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VHRunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
5	<p>VID4 VINunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VID4 VINunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
4	<p>VID3 VINunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VID3 VINunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
3	<p>VID2 VINunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VID2 VINunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
2	<p>VID1 VINunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VID1 VINunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL4 - Unit Level Clock Gating Control 4

	1:0	MSQCunit Clock Gating Disable	
		Default Value:	11b
		Access:	R/W
		<p>MSQCunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	

Unit Level Clock Gating Control 5

UCGCTL5 - Unit Level Clock Gating Control 5				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	09418h			
DWord	Bit	Description		
0	31	<p>VCOPunit clock gating disable bit</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>WVCOP units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always).</p>	Access:	R/W
	Access:	R/W		
	30	<p>VMBunit clock gate disable bit</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VMB units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
	Access:	R/W		
	29	<p>VDMunit clock gate disable bit</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VDM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W			
28	<p>L3BANK unit cuclkgating disable bit</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>L3bank units cuclk Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			
27	<p>L3BANK cu2x clock gate disable bit</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>L3BANK units cu2x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks</p>	Access:	R/W	
Access:	R/W			

UCGCTL5 - Unit Level Clock Gating Control 5

26	<p>LNIunit clock gate disable bit</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>LNI units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
25	<p>LNEUNIT clock gate disable bit</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>LNE units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
24	<p>VVPunit clock gate disable bit</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VVP units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
23	<p>WVFT unit clock gate disable bits</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>WVFT units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
22	<p>WBPS unit clock gate disable bit</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>WBPS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
21	<p>WVMX unit clock gate disable bit</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>WVMX units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL5 - Unit Level Clock Gating Control 5

20	WVIP unit clock gate disable bit	Access:	R/W
	<p>WVIP unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
19	WVIT unit clock gate disable bit	Access:	R/W
	<p>WVIT units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
18	WVIS unit clock gate disable	Access:	R/W
	<p>WVIS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
17	RPM units clock gate disable	Access:	R/W
	<p>RPM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
16	Reserved		
15	VECS unit clock gate disable	Access:	R/W
	<p>VECS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
14	GAHSV unit clock gate disable	Access:	R/W
	<p>GAHSV units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		

UCGCTL5 - Unit Level Clock Gating Control 5

13	<p>GAHSD unit clock gate disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>GAHSD units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
12	<p>GAV unit's clock gate disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>GAV units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
11	<p>RSunit's clock gate disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>RW units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
10	<p>VFW units clock gate disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>VFW units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
9	<p>VCW unit's clock gate disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>VCW units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
8	<p>VEO unit's clock gate disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>VEO units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL5 - Unit Level Clock Gating Control 5

7	<p>VDN unit's clock gate disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VDN units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
6	<p>VTQunit's clock gate disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VTQunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
5	<p>VPRunit's clock gate disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VPR units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
4	<p>IMEunit's clock gate disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>IME units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
3	<p>CREunit clock gate disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>CRE units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
2	<p>GAPSL unit clock gate disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>GAPSL units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL5 - Unit Level Clock Gating Control 5

1	<p>GAPSU Clock gate disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>GAPSU units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
0	<p>SPMunit Clock gate disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>SPM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

Unit Level Clock Gating Control 5

UCGCTL5 - Unit Level Clock Gating Control 5				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	09418h			
DWord	Bit	Description		
0	31	<p>VCOPunit clock gating disable bit</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>WVCOP units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always).</p>	Access:	R/W
	Access:	R/W		
	30	<p>VMBunit clock gate disable bit</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VMB units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
	Access:	R/W		
	29	<p>VDMunit clock gate disable bit</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VDM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W			
28	<p>L3BANK unit cuclkgating disable bit</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>L3bank units cuclk Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			
27	<p>L3BANK cu2x clock gate disable bit</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>L3BANK units cu2x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks</p>	Access:	R/W	
Access:	R/W			

UCGCTL5 - Unit Level Clock Gating Control 5

26	<p>LNIunit clock gate disable bit</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>LNI units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
25	<p>LNEUNIT clock gate disable bit</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>LNE units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
24	<p>VVPunit clock gate disable bit</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>VVP units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
23	<p>WVFT unit clock gate disable bits</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>WVFT units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
22	<p>WBPS unit clock gate disable bit</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>WBPS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
21	<p>WVMX unit clock gate disable bit</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>WVMX units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL5 - Unit Level Clock Gating Control 5

20	<p>WVIP unit clock gate disable bit</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>WVIP unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
19	<p>WVIT unit clock gate disable bit</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>WVIT units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
18	<p>WVIS unit clock gate disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>WVIS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
17	<p>RPM units clock gate disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>RPM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
16	<p>OASC unit clock gating disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>OASC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
15	<p>VECS unit clock gate disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VECS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL5 - Unit Level Clock Gating Control 5

14	GAHSV unit clock gate disable	Access:	R/W
<p>GAHSV units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>			
13	GAHSD unit clock gate disable	Access:	R/W
<p>GAHSD units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>			
12	GAV unit's clock gate disable	Access:	R/W
<p>GAV units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>			
11	RSunit's clock gate disable	Access:	R/W
<p>RW units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>			
10	VFW units clock gate disable	Access:	R/W
<p>VFW units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>			
9	VCW unit's clock gate disable	Access:	R/W
<p>VCW units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>			

UCGCTL5 - Unit Level Clock Gating Control 5

8	<p>VEO unit's clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VEO units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
7	<p>VDN unit's clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VDN units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
6	<p>VTQunit's clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VTQunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
5	<p>VPRunit's clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VPR units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
4	<p>IMEunit's clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>IME units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
3	<p>CREunit clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>CRE units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL5 - Unit Level Clock Gating Control 5

2	<p>GAPSL unit clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>GAPSL units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
1	<p>GAPSU Clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>GAPSU units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
0	<p>SPMunit Clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>SPM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

Unit Level Clock Gating Control 6

UCGCTL6 - Unit Level Clock Gating Control 6				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	09430h			
Unit Level Clock Gating Disable bits				
DWord	Bit	Description		
0	30:28	HDCunit clock gate disable <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>HDC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
	Access:	R/W		
	27	Reserved		
	26	GACVunit cuclk gate disable <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>GACV units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
	Access:	R/W		
25	GACBunit clock gate disable <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>GACB units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			
24	GAPSunit clock gate disable <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>GAPS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			

UCGCTL6 - Unit Level Clock Gating Control 6

23	<p>GAMTunit clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>GAMT units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
22	Reserved		
21	Reserved		
20	Reserved		
19	<p>GACVunit clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>GACV units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
18	<p>BDMunit clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>BDM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
17	<p>GATSunit clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>GATS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
16	Reserved		
15	<p>STunit clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>ST units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL6 - Unit Level Clock Gating Control 6

14	SDEunit clock gate disable	Access:	R/W	
	DE units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
	Programming Notes			
	Due to SDEUNIT bug HSD#1802092, this bit should be programmed to a 1 for CHV, BSW			
	13	VIN(VID6) unit clock gate disable	Access:	R/W
		VIN(VID6) units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
12		VIN(VID5) unit clock gate disable	Access:	R/W
	VIN(VID5) units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
11	WVOPunit clock gate disable	Access:	R/W	
	WVOP units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
10	WUSB unit clock gate disable	Access:	R/W	
	WUSB units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
9	WSECunit clock gate disable	Access:	R/W	
	WSEC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			

UCGCTL6 - Unit Level Clock Gating Control 6

8	<p>WRSunit clcok gate disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>WRS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
7	<p>WQRCunit clock gate disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>WQRC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
6	<p>WMPC unit level clock gate disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>WMPC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
5	<p>WINunit Clock gate disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>WIN units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
4	<p>WIME unit clock gate disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>WIME units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
3	<p>WHME unit clock gate disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>WHME units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL6 - Unit Level Clock Gating Control 6			
2	<p>WAVMunit Clock Gate Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>WAVM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
1	<p>VSHMunit clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VSHM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
0	<p>VSLunit Clock gating disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VSL units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

Unit Level Clock Gating Control 6

UCGCTL6 - Unit Level Clock Gating Control 6				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	09430h			
Unit Level Clock Gating Disable bits				
DWord	Bit	Description		
0	31	<p>SPARE 3 clock gate disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>SPARE 3 unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
	Access:	R/W		
	30:28	<p>HDCunit clock gate disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>HDC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
	Access:	R/W		
27	<p>MUCunit clock gate disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>MUC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			
26	<p>GACVunit cuclk gate disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>GACV units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			

UCGCTL6 - Unit Level Clock Gating Control 6

25	GACBunit clock gate disable	Access:	R/W
<p>GACB units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>			
24	GAPSunit clock gate disable	Access:	R/W
<p>GAPS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>			
23	GAMTunit clock gate disable	Access:	R/W
<p>GAMT units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>			
22	Reserved		
21	OASCREP	Access:	R/W
<p>OASCREP units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>			
20	OAADDRunit clock gate disable bit	Access:	R/W
<p>OAADDR units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>			
19	GACVunit clock gate disable	Access:	R/W
<p>GACV units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>			

UCGCTL6 - Unit Level Clock Gating Control 6

18	<p>BDMunit clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>BDM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
17	<p>GATSunit clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>GATS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
16	<p>OATREPunit clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>OATREP units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
15	<p>STunit clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>ST units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
14	<p>DEunit clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>DE units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
13	<p>VIN(VID6) unit clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VIN(VID6) units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL6 - Unit Level Clock Gating Control 6

12	VIN(VID5) unit clock gate disable	
	Access:	R/W
	VIN(VID5) units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
11	WVOPunit clock gate disable	
	Access:	R/W
	WVOP units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
10	WUSB unit clock gate disable	
	Access:	R/W
	WUSB units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
9	WSECunit clock gate disable	
	Access:	R/W
	WSEC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
8	WRSunit clock gate disable	
	Access:	R/W
	WRS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
7	WQRCunit clock gate disable	
	Access:	R/W
	WQRC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

UCGCTL6 - Unit Level Clock Gating Control 6

6	<p>WMPC unit level clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>WMPC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
5	<p>WINunit Clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>WIN units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
4	<p>WIME unit clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>WIME units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
3	<p>WHME unit clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>WHME units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
2	<p>WAVMunit Clock Gate Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>WAVM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
1	<p>VSHMunit clock gate disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>VSHM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL6 - Unit Level Clock Gating Control 6

	0	VSLunit Clock gating disable	
		Access:	R/W
		<p>VSL units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	

Unit Level Clock Gating Control 7

UCGCTL7 - Unit Level Clock Gating Control 7		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	09438h	
DWord	Bit	Description
0	31:18	RSVD
	17	Reserved
	16	cp_cg3ddis_hwm
	Access: R/W	
	HWM unit Clock Gating Disable (cp_cg3ddis_hwm) HWM unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
15	cp_cg3ddis_hed	
	Access: R/W	
HED unit Clock Gating Disable (cp_cg3ddis_hed) HED unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
14	cp_cg3ddis_hpp	
	Access: R/W	
HPP unit Clock Gating Disable (cp_cg3ddis_hpp) HPP unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
13	cp_cg3ddis_hpr	
	Access: R/W	
HPR unit Clock Gating Disable (cp_cg3ddis_hpr) HPR unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)		

UCGCTL7 - Unit Level Clock Gating Control 7

		'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
12	cp_cg3ddis_hmc	
	Access:	R/W
	HMC unit Clock Gating Disable (cp_cg3ddis_hmc) HMC unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
11	cp_cg3ddis_hlf	
	Access:	R/W
	HLF unit Clock Gating Disable (cp_cg3ddis_hlf) HLF unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
10	cp_cg3ddis_hmx	
	Access:	R/W
	HMX unit Clock Gating Disable (cp_cg3ddis_hmx) HMX unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
9	cp_cg3ddis_vmm	
	Access:	R/W
	VMM unit Clock Gating Disable (cp_cg3ddis_vmm) VMM unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
8	cp_cg3ddis_mpd	
	Access:	R/W
	MPD unit Clock Gating Disable (cp_cg3ddis_mpd) MPD unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
7	cp_cg3ddis_mbd	
	Access:	R/W
	MBD unit Clock Gating Disable (cp_cg3ddis_mbd) MBD unit Clock Gating Disable Control	

UCGCTL7 - Unit Level Clock Gating Control 7

		'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
6	cp_cg3ddis_mlf		
	Access:		R/W
	MLF unit Clock Gating Disable (cp_cg3ddis_mlf) MLF unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
5	cp_cg3ddis_mmc		
	Access:		R/W
	MMC unit Clock Gating Disable (cp_cg3ddis_mmc) MMC unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
4	cp_cg3ddis_mmx		
	Access:		R/W
	MMX unit Clock Gating Disable (cp_cg3ddis_mmx) MMX unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
3	cp_cg3ddisvbsp		
	Access:		R/W
	VBSP unit Clock Gating Disable (cp_cg3ddisvbsp) VBSP unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
2	cp_cg3ddisvmcpc		
	Access:		R/W
	VMPC unit Clock Gating Disable (cp_cg3ddisvmcpc) VMPC unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
1	cp_cg3ddisvsec		
	Access:		R/W
	VSEC unit Clock Gating Disable (cp_cg3ddisvsec)		

UCGCTL7 - Unit Level Clock Gating Control 7			
	<p>VSEC unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
0	<p>cp_cg3ddisjusb</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>JUSB unit Clock Gating Disable (cp_cg3ddisjusb) JUSB unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

Unit Level Clock Gating Control 7

UCGCTL7 - Unit Level Clock Gating Control 7				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	09434h			
Unit Level Clock Gating Disable bits				
DWord	Bit	Description		
0	31	<p>wrcunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>wrcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
	Access:	R/W		
	30	<p>mmcdunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>mmcdunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
	Access:	R/W		
29	<p>bfceunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>bfceunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			
28	<p>ecpunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>ecpunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			

UCGCTL7 - Unit Level Clock Gating Control 7

27	<p>vdlunit1 Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>vdlunit1 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
26	<p>vhmeunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>vhmeunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
25	<p>vimeunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>vimeunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
24	<p>vcreunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>vcreunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
23	<p>vdxcunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>vdxcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
22	<p>mdcunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>mdcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL7 - Unit Level Clock Gating Control 7

21	<p>hpunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>hpunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
20	<p>hrsunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>hrsunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
19	<p>ftunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>ftunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
18	<p>fqunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>fqunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
17	<p>hleunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>hleunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
16	<p>hlcunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>hlcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL7 - Unit Level Clock Gating Control 7

15	<p>hhiunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>hhiunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
14	<p>mlfunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>mlfunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
13	<p>mmcunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>mmcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
12	<p>mbdunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>mbdunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
11	<p>mpdunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>mpdunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
10	<p>mmxunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>mmxunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL7 - Unit Level Clock Gating Control 7

9	<p>hedunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>hedunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
8	<p>hlfunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>hlfunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
7	<p>hmcunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>hmcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
6	<p>hmxunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>hmxunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
5	<p>hppunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>hppunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
4	<p>hprunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>hprunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL7 - Unit Level Clock Gating Control 7

3	Reserved		
2	<p>hwmunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%; padding: 2px;">Access:</td> <td style="width: 40%; padding: 2px;">R/W</td> </tr> </table> <p>hwmunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
1	<p>vmpcunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%; padding: 2px;">Access:</td> <td style="width: 40%; padding: 2px;">R/W</td> </tr> </table> <p>vmpcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
0	<p>vsecunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%; padding: 2px;">Access:</td> <td style="width: 40%; padding: 2px;">R/W</td> </tr> </table> <p>vsecunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

Unit Level Clock Gating Control 8

UCGCTL8 - Unit Level Clock Gating Control 8				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	09438h			
Unit Level Clock Gating Disable bits				
DWord	Bit	Description		
0	31	<p>jusbunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>jusbunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
	Access:	R/W		
	30	<p>sfiunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>sfiunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
	Access:	R/W		
29	<p>sfeunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>sfeunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			
28	<p>sfaunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>sfaunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			

UCGCTL8 - Unit Level Clock Gating Control 8

27	<p>sfounit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>sfounit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
26	<p>sfxunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>sfxunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
25	<p>sfmunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>sfmunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
24	<p>vmmunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>vmmunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
23	<p>vrtunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>vrtunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
22	<p>ccunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>ccunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL8 - Unit Level Clock Gating Control 8

21	gassunit Clock Gating Disable	Access:	R/W
	gassunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
20	gamdunit Clock Gating Disable	Access:	R/W
	gamdunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
19	vdlunit1 Clock Gating Disable	Access:	R/W
	vdlunit1 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
18	vhmeunit Clock Gating Disable	Access:	R/W
	vhmeunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
17	vcreunit Clock Gating Disable	Access:	R/W
	vcreunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
16	hleunit Clock Gating Disable	Access:	R/W
	hleunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		

UCGCTL8 - Unit Level Clock Gating Control 8

15	<p>mbdunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>mbdunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
14	<p>mmxunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>mmxunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
13	<p>mpdunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>mpdunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
12	<p>hedunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>hedunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
11	<p>hlfunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>hlfunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
10	<p>hmcunit Clock Gating Disable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>hmcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL8 - Unit Level Clock Gating Control 8

9	<p>hmxunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>hmxunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
8	<p>hppunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>hppunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
7	<p>hprunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>hprunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
6	Reserved		
5	<p>hwmunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>hwmunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
4	<p>mdcunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>mdcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
3	<p>vmpcunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>vmpcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL8 - Unit Level Clock Gating Control 8

2	sfmunit Clock Gating Disable ebb	Access: R/W
	<p>sfmunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	
1	sfaunit Clock Gating Disable ebb	Access: R/W
	<p>sfaunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	
0	sfeunit Clock Gating Disable ebb	Access: R/W
	<p>sfeunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	

Unit Level Clock Gating Control 9

UCGCTL9 - Unit Level Clock Gating Control 9		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0943Ch	
Unit Level Clock Gating Disable bits		
DWord	Bit	Description
0	31:4	Reserved
		Access: RO
	Reserved	
	3	vbspunit Clock Gating Disable
		Access: R/W
vbspunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
2	vmmunit Clock Gating Disable	
	Access: R/W	
vmmunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
1	AVSunit Clock Gating Disable	
	Access: R/W	
AVSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
0	daprssunit Clock Gating Disable	
	Access: R/W	
daprssunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		

URB Context Offset

URB_CXT_OFFSET - URB Context Offset				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	RenderCS			
Default Value:	0x00009AC0			
Access:	Read/32 bit Write Only			
Size (in bits):	32			
Address:	021B8h			
DWord	Bit	Description		
0	31:6	<p>URB Offset</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%; text-align: center;">26Bh</td> </tr> </table> <p>This field indicates the offset (64bytes granular) in to the logical rendering context to which URB contents are save/restored when enabled. This field register must not be written directly (via MMIO) unless the Command Streamer is completely idle (i.e., the Ring Buffer is empty and the pipeline is idle) and RC6 is disabled. One way to program this register is via Load Register Immediate command in the ring buffer as part of initialization sequence.</p>	Default Value:	26Bh
	Default Value:	26Bh		
5:0	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%; text-align: center;">MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ			

Valid Bit Vector 0 for CVS

CVSTLB_VLD_0 - Valid Bit Vector 0 for CVS						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04C00h					
This register contains the valid bits for entries 0-31 of CVSTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 0 for CVS <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 0 for L3

L3TLB_VLD_0 - Valid Bit Vector 0 for L3						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D00h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 0 for L3 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 0 for MFX

MFXTLB_VLD_0 - Valid Bit Vector 0 for MFX						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04BA0h					
This register contains the valid bits for entries 0-31 of MFXTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 0 for MFX <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 0 for MFX SL1

MFXTLB_VLD_SL1_0 - Valid Bit Vector 0 for MFX SL1						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04BC0h					
This register contains the valid bits for entries 0-31 of MFX SL1 TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 0 for MFX SL1 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 0 for MTTLB

MTTLB_VLD0 - Valid Bit Vector 0 for MTTLB		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	04780h-04783h	
This register contains the valid bits for entries 0-31 of MTTLB (Texture and constant cache TLB).		
DWord	Bit	Description
0	31:0	Valid bits per entry

Valid Bit Vector 0 for MTVICTLB

VICTLB_VLD0 - Valid Bit Vector 0 for MTVICTLB		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	04788h-0478Bh	
This register contains the valid bits for entries 0-31 of VICTLB (Vertex Fetch, Instruction Cache, and Command Streamer TLB).		
DWord	Bit	Description
0	31:0	Valid bits per entry

Valid Bit Vector 0 for RCC

RCCTLB_VLD_0 - Valid Bit Vector 0 for RCC						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04DA0h					
This register contains the valid bits for entries 0-31 of RCCTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 0 for RCC <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 0 for RCCTLB

RCCTLB_VLD0 - Valid Bit Vector 0 for RCCTLB		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	04790h-04793h	
This register contains the valid bits for entries 0-31 of RCCTLB (Render Cache for Color TLB).		
DWord	Bit	Description
0	31:0	Valid bits per entry

Valid Bit Vector 0 for RCZTLB

RCZTLB_VLD0 - Valid Bit Vector 0 for RCZTLB		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	04798h-0479Bh	
This register contains the valid bits for entries 0-31 of RCZTLB (Render Cache for Z (Depth), Hi Z, and Stencil TLB).		
DWord	Bit	Description
0	31:0	Valid bits per entry

Valid Bit Vector 0 for TLBPEND registers

TLBPEND_VLD0 - Valid Bit Vector 0 for TLBPEND registers		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	04700h-04703h	
This register contains the valid bits for entries 0-31 of TLBPEND structure (Cycles pending TLB translation).		
DWord	Bit	Description
0	31:0	Valid bits per entry

Valid Bit Vector 0 for VEBX

VEBXTLB_VLD_0 - Valid Bit Vector 0 for VEBX						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B20h					
This register contains the valid bits for entries 0-31 of VEBXTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 0 for VEBX</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 0 for WIDI

BWDTLB_VLD_0 - Valid Bit Vector 0 for WIDI						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04DC0h					
This register contains the valid bits for entries 0-31 of BWDTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 0 for WIDI <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 0 for Z

ZTLB_VLD_0 - Valid Bit Vector 0 for Z						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B34h					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 0 for Z <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 1 for CVS

CVSTLB_VLD_1 - Valid Bit Vector 1 for CVS						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04C04h					
This register contains the valid bits for entries 0-31 of CVSTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 1 for CVS <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 1 for L3

L3TLB_VLD_1 - Valid Bit Vector 1 for L3						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D04h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 1 for L3 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: right;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: right;">RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 1 for MFX

MFXTLB_VLD_1 - Valid Bit Vector 1 for MFX						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04BA4h					
This register contains the valid bits for entries 0-31 of MFXTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 1 for MFX <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 1 for MFX SL1

MFXTLB_VLD_SL1_1 - Valid Bit Vector 1 for MFX SL1						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04BC4h					
This register contains the valid bits for entries 0-31 of MFX SL1 TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 1 for MFX SL1 <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 1 for MTTLB

MTTLB_VLD1 - Valid Bit Vector 1 for MTTLB		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	04784h-04787h	
This register contains the valid bits for entries 0-31 of MTTLB (Texture and constant cache TLBVertex Fetch, Instruction Cache, and Command Streamer TLB).		
DWord	Bit	Description
0	31:0	Valid bits per entry

Valid Bit Vector 1 for MTVICTLB

MTVICTLB_VLD1 - Valid Bit Vector 1 for MTVICTLB		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	0478Ch-0478Fh	
This register contains the valid bits for entries 0-31 of VICTLB (Vertex Fetch, Instruction Cache, and Command Streamer TLB).		
DWord	Bit	Description
0	31:0	Valid bits per entry

Valid Bit Vector 1 for RCC

RCCTLB_VLD_1 - Valid Bit Vector 1 for RCC						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04DA4h					
This register contains the valid bits for entries 0-31 of RCCTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 1 for RCC <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 1 for RCCTLB

RCCTLB_VLD1 - Valid Bit Vector 1 for RCCTLB		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	04794h-04797h	
This register is reserved for future RCC TLB extension.		
DWord	Bit	Description
0	31:0	Reserved
		Format: MBZ

Valid Bit Vector 1 for RCZTLB

RCZTLB_VLD1 - Valid Bit Vector 1 for RCZTLB		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	0479Ch-0479Fh	
This register contains the valid bits for entries 0-31 of RCZTLB (Render Cache for Z (Depth), Hi Z, and Stencil TLB).		
DWord	Bit	Description
0	31:0	Valid bits per entry

Valid Bit Vector 1 for TLBPEND registers

TLBPEND_VLD1 - Valid Bit Vector 1 for TLBPEND registers		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	04704h-04707h	
This register contains the valid bits for entries 32-63 of TLBPEND structure (Cycles pending TLB translation).		
DWord	Bit	Description
0	31:0	Valid bits per entry

Valid Bit Vector 1 for VEBX

VEBXTLB_VLD_1 - Valid Bit Vector 1 for VEBX						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B24h					
This register contains the valid bits for entries 0-31 of VEBXTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 1 for VEBX</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 1 for WIDI

BWDTLB_VLD_1 - Valid Bit Vector 1 for WIDI						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04DC4h					
This register contains the valid bits for entries 0-31 of BWDTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 1 for WIDI <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 1 for Z

ZTLB_VLD_1 - Valid Bit Vector 1 for Z						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B38h					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 1 for Z <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 2 for CVS

CVSTLB_VLD_2 - Valid Bit Vector 2 for CVS						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04C08h					
This register contains the valid bits for entries 0-31 of CVSTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 2 for CVS</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 2 for GAB

BWDTLB_VLD_3 - Valid Bit Vector 2 for GAB						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04DCCh					
This register contains the valid bits for entries 0-31 of BWDTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 3 for GAB <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 2 for L3

L3TLB_VLD_2 - Valid Bit Vector 2 for L3						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D08h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 2 for L3 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 2 for MFX

MFXTLB_VLD_2 - Valid Bit Vector 2 for MFX						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04BA8h					
This register contains the valid bits for entries 0-31 of MFXTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 2 for MFX <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 2 for MFX SL1

MFXTLB_VLD_SL1_2 - Valid Bit Vector 2 for MFX SL1						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04BC8h					
This register contains the valid bits for entries 0-31 of MFX SL1 TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 2 for MFX SL1 <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 2 for RCC

RCCTLB_VLD_2 - Valid Bit Vector 2 for RCC						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04DA8h					
This register contains the valid bits for entries 0-31 of RCCTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 2 for RCC <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 2 for Z

ZTLB_VLD_2 - Valid Bit Vector 2 for Z						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B3Ch					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 2 for Z <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 3 for CVS

CVSTLB_VLD_3 - Valid Bit Vector 3 for CVS						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04C0Ch					
This register contains the valid bits for entries 0-31 of CVSTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 3 for CVS <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 3 for L3

L3TLB_VLD_3 - Valid Bit Vector 3 for L3						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D0Ch					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 3 for L3 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 3 for MFX

MFXTLB_VLD_3 - Valid Bit Vector 3 for MFX						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04BACH					
This register contains the valid bits for entries 0-31 of MFXTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 3 for MFX <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 3 for MFX SL1

MFXTLB_VLD_SL1_3 - Valid Bit Vector 3 for MFX SL1						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04BCCh					
This register contains the valid bits for entries 0-31 of MFX SL1 TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 3 for MFX SL1 <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 3 for RCC

RCCTLB_VLD_3 - Valid Bit Vector 3 for RCC						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04DACH					
This register contains the valid bits for entries 0-31 of RCCTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 3 for RCC <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 3 for Z

ZTLB_VLD_3 - Valid Bit Vector 3 for Z						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B40h					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 3 for Z <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 4 for L3

L3TLB_VLD_4 - Valid Bit Vector 4 for L3						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D10h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 4 for L3 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 4 for MFX

MFXTLB_VLD_4 - Valid Bit Vector 4 for MFX						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04BB0h					
This register contains the valid bits for entries 0-31 of MFXTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 4 for MFX <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 4 for MFX SL1

MFXTLB_VLD_SL1_4 - Valid Bit Vector 4 for MFX SL1						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04BD0h					
This register contains the valid bits for entries 0-31 of MFX SL1 TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 4 for MFX SL1 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 4 for RCC

RCCTLB_VLD_4 - Valid Bit Vector 4 for RCC						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04DB0h					
This register contains the valid bits for entries 0-31 of RCCTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 4 for RCC <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 4 for Z

ZTLB_VLD_4 - Valid Bit Vector 4 for Z						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B44h					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 4 for Z <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 5 for L3

L3TLB_VLD_5 - Valid Bit Vector 5 for L3						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D14h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 5 for L3 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 5 for MFX

MFXTLB_VLD_5 - Valid Bit Vector 5 for MFX						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04BB4h					
This register contains the valid bits for entries 0-31 of MFXTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 5 for MFX <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: right;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: right;">RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 5 for MFX SL1

MFXTLB_VLD_SL1_5 - Valid Bit Vector 5 for MFX SL1						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04BD4h					
This register contains the valid bits for entries 0-31 of MFX SL1 TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 5 for MFX SL1 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 5 for RCC

RCCTLB_VLD_5 - Valid Bit Vector 5 for RCC						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04DB4h					
This register contains the valid bits for entries 0-31 of RCCTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 5 for RCC <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 5 for Z

ZTLB_VLD_5 - Valid Bit Vector 5 for Z						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B48h					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 5 for Z <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 6 for L3

L3TLB_VLD_6 - Valid Bit Vector 6 for L3						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D18h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 6 for L3 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 6 for MFX

MFXTLB_VLD_6 - Valid Bit Vector 6 for MFX						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04BB8h					
This register contains the valid bits for entries 0-31 of MFXTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 6 for MFX <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 6 for MFX SL1

MFXTLB_VLD_SL1_6 - Valid Bit Vector 6 for MFX SL1						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04BD8h					
This register contains the valid bits for entries 0-31 of MFX SL1 TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 6 for MFX SL1 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 6 for RCC

RCCTLB_VLD_6 - Valid Bit Vector 6 for RCC						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04DB8h					
This register contains the valid bits for entries 0-31 of RCCTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 6 for RCC <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 6 for Z

ZTLB_VLD_6 - Valid Bit Vector 6 for Z						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B4Ch					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 6 for Z <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 7 for L3

L3TLB_VLD_7 - Valid Bit Vector 7 for L3						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D1Ch					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 7 for L3 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 7 for MFX

MFXTLB_VLD_7 - Valid Bit Vector 7 for MFX						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04BBCh					
This register contains the valid bits for entries 0-31 of MFXTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 7 for MFX <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 7 for MFX SL1

MFXTLB_VLD_SL1_7 - Valid Bit Vector 7 for MFX SL1						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04BDCh					
This register contains the valid bits for entries 0-31 of MFX SL1 TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 7 for MFX SL1 <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 7 for RCC

RCCTLB_VLD_7 - Valid Bit Vector 7 for RCC						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04DBCh					
This register contains the valid bits for entries 0-31 of RCCTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 7 for RCC <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 7 for Z

ZTLB_VLD_7 - Valid Bit Vector 7 for Z						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B50h					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 7 for Z <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: right;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: right;">RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 8 for L3

L3TLB_VLD_8 - Valid Bit Vector 8 for L3						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D20h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 8 for L3 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 8 for Z

ZTLB_VLD_8 - Valid Bit Vector 8 for Z						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B54h					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 8 for Z <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 9 for L3

L3TLB_VLD_9 - Valid Bit Vector 9 for L3						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D24h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 9 for L3 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 9 for Z

ZTLB_VLD_9 - Valid Bit Vector 9 for Z						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B58h					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 9 for Z <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 10 for L3

L3TLB_VLD_10 - Valid Bit Vector 10 for L3						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D28h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 10 for L3 <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 10 for Z

ZTLB_VLD_10 - Valid Bit Vector 10 for Z						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B5Ch					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 10 for Z <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 11 for L3

L3TLB_VLD_11 - Valid Bit Vector 11 for L3						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D2Ch					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 11 for L3 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 11 for Z

ZTLB_VLD_11 - Valid Bit Vector 11 for Z						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B60h					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 11 for Z <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 12 for L3

L3TLB_VLD_12 - Valid Bit Vector 12 for L3						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D30h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 12 for L3 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 12 for Z

ZTLB_VLD_12 - Valid Bit Vector 12 for Z						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B64h					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 12 for Z <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 13 for L3

L3TLB_VLD_13 - Valid Bit Vector 13 for L3						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D34h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 13 for L3 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 13 for Z

ZTLB_VLD_13 - Valid Bit Vector 13 for Z						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B68h					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 13 for Z <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 14 for L3

L3TLB_VLD_14 - Valid Bit Vector 14 for L3						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D38h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 14 for L3 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 14 for Z

ZTLB_VLD_14 - Valid Bit Vector 14 for Z						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B6Ch					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 14 for Z <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 15 for L3

L3TLB_VLD_15 - Valid Bit Vector 15 for L3						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D3Ch					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 15 for L3 <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 15 for Z

ZTLB_VLD_15 - Valid Bit Vector 15 for Z						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B70h					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 15 for Z <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 16 for L3

L3TLB_VLD_16 - Valid Bit Vector 16 for L3						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D40h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 16 for L3 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 17 for L3

L3TLB_VLD_17 - Valid Bit Vector 17 for L3						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D44h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 17 for L3 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 18 for L3

L3TLB_VLD_18 - Valid Bit Vector 18 for L3						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D48h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 18 for L3 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: right;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: right;">RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 19 for L3

L3TLB_VLD_19 - Valid Bit Vector 19 for L3						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D4Ch					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 19 for L3 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 20 for L3

L3TLB_VLD_20 - Valid Bit Vector 20 for L3						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D50h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 20 for L3 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 21 for L3

L3TLB_VLD_21 - Valid Bit Vector 21 for L3						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D54h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 21 for L3 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 22 for L3

L3TLB_VLD_22 - Valid Bit Vector 22 for L3						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D58h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 22 for L3 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 23 for L3

L3TLB_VLD_23 - Valid Bit Vector 23 for L3						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D5Ch					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 23 for L3 <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector for VLF

VLFTLB_VLD - Valid Bit Vector for VLF						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B30h					
This register contains the valid bits for entries 0-31 of VLFTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector for VLF <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector for VLFSL1

VLFSL1TLB_VLD - Valid Bit Vector for VLFSL1						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B2Ch					
This register contains the valid bits for entries 0-31 of VLFSL1TLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector for VLFSL1</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

VC

VC - VC				
Register Space:	PCI: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	000B4h			
Vendor Capabilities. Any SKU related fuses would be added here.				
DWord	Bit	Description		
0	31:1	Reserved		
		<table border="1"> <tr> <td>Default Value:</td> <td>0000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Reserved	Default Value:	0000000h
Default Value:	0000000h			
Access:	RO			
0	0	Spare_bit		
		<table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Placeholder for SKU related fusing.	Default Value:	0b
Default Value:	0b			
Access:	RO			

VCES Idle Switch Delay

VECS_IDLELY - VCES Idle Switch Delay							
Register Space:	MMIO: 0/2/0						
Project:	CHV, BSW						
Source:	VideoEnhancementCS						
Default Value:	0x00000000						
Access:	R/W						
Size (in bits):	32						
Address:	1A23Ch						
<p>The IDLEDLY register contains an Idle Delay field which specifies the minimum number of microseconds allowed for command streamer to wait before a context is switched out leading to IDLE state in execlists mode, i.e following this context switch there is no active element available in HW to execute.</p> <p>A default value of 0, means that by default, there is no restriction to wait on a context switch leading to IDLE. This register has no significance when execlists are not enabled.</p>							
DWord	Bit	Description					
0	31:21	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ	
	Project:	All					
Format:	MBZ						
20:0	<p>IDLE Delay</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>0h</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U21</td> </tr> </table> <p>Minimum number of micro-seconds allowed.</p>	Default Value:	0h	Project:	All	Format:	U21
Default Value:	0h						
Project:	All						
Format:	U21						

VCID

VCID - VCID			
Register Space:	PCI: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x01070009		
Size (in bits):	32		
Address:	000B0h		
Vendor Capability ID			
DWord	Bit	Description	
0	31:24	VERSION	
		Default Value:	01h
		Access:	RO
		VS: Identifies this as the first revision of the CAPID register definition.	
	23:16	LENGTH	
		Default Value:	07h
		Access:	RO
		LEN: This field has the value 07h to indicate structure length (8 bytes)	
	15:8	NEXT_CAPABILITY_POINTER	
		Default Value:	00h
		Access:	R/W Once
		00 indicates capability list ends here. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset. Write-once allowing the capability list to be changed.	
7:0	CAPABILITY_ID_CID		
	Default Value:	09h	
	Access:	RO	
	Identifies this as a vendor dependent capability pointers.		

VCS_PREEMPTION_HINT

VCS_PREEMPTION_HINT - VCS_PREEMPTION_HINT									
Register Space:	MMIO: 0/2/0								
Project:	CHV, BSW								
Source:	VideoCS								
Default Value:	0x00000000								
Access:	R/W								
Size (in bits):	32								
Address:	124BCh								
Valid Projects:	CHV, BSW								
<p>This register contains the Head pointer offset in to the Ring Buffer or the Dword aligned Graphics address in to the Batch Buffer corresponding to either MI_ARB_CHECK called Preemption Hint Address. When Preemption Hint Address is enabled, VCS will honor UHPTR only on parsing MI_ARB_CHK at Preemption Hint Address.</p> <p>This register contains the Head pointer offset into the Ring Buffer or the Dword aligned Graphics address into the Batch Buffer corresponding to the below listed commands in execlist mode of operation</p> <ul style="list-style-type: none"> • MI_ARB_CHECK • MI_WAIT_FOR_EVENT • MI_SEMAPHORE_WAIT 									
Programming Notes									
<p>Programming Restriction: This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of UHPTR being sampled by a given MI_ARB_CHECK in command stream. Programmer has to ensure that VCS Preemption Hint register gets programmed before UHPTR is programmed and well before VCS crosses the corresponding execution point. Preemption hint for both RingBuffer and Batch Buffer can't be enabled simultaneously.</p>									
DWord	Bit	Description							
0	31:2	<p>Preempted Hint Address</p> <table border="1"> <tr> <td>Format:</td> <td>U30</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[31:2]</td> </tr> </table> <p>This field contains the Head offset in to the Ring Buffer when Preemption Hint is set to Ring Buffer and Dword aligned Graphics Address in to the batch buffer when Preemption Hint is set to Batch Buffer.</p>	Format:	U30	Format:	GraphicsAddress[31:2]			
		Format:	U30						
Format:	GraphicsAddress[31:2]								
1	<p>Batch Buffer Preemption Hint</p> <table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disabled</td> <td>Preemption hint is disabled in batch buffer.</td> </tr> </tbody> </table>	Format:	Enable	Value	Name	Description	0h	Disabled	Preemption hint is disabled in batch buffer.
Format:	Enable								
Value	Name	Description							
0h	Disabled	Preemption hint is disabled in batch buffer.							

VCS_PREEMPTION_HINT - VCS_PREEMPTION_HINT			
	1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Batch Buffer.
	0	Ring Preemption Hint	
	Format:		Enable
	Value	Name	Description
	0h	Disable	Preemption hint is disabled in ring buffer.
	1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Ring Buffer.

VCS_PREEMPTION_HINT_UDW

VCS_PREEMPTION_HINT_UDW - VCS_PREEMPTION_HINT_UDW				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	124C8h			
Valid Projects:	CHV, BSW			
<p>This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the Batch Buffer corresponding to MI_ARB_CHECK command called Preemption Hint Address.</p>				
Programming Notes				
<p>Programming Restriction: This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of UHPTR being sampled by a given MI_ARB_CHK in command stream.</p>				
DWord	Bit	Description		
0	31:16	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
15:0	<p>Preempted Hint Address Upper DWORD</p> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>This field contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the batch buffer when Preemption Hint is set to Batch Buffer. This field is not valid when Preemption Hint is set to Ring Buffer.</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			

VCS Context ID Preemption Hint

VCS_CTXID_PREEMPTION_HINT - VCS Context ID Preemption Hint				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	124CCh			
Valid Projects:	CHV, BSW			
<p>This register contains the Context ID of a context in execlist mode of operation. In execlist mode of operation VCS_PREEMPTION_HINT registers are looked at by Video Command Streamer on executing a context having Context ID that matches with the contents of this register. This register contents are valid and looked at only in execlist mode of operation.</p>				
Programming Notes				
<p>This register should NEVER be programmed in functional mode, this must be used only in validation mode to achieve deterministic preemption behavior in execlist mode of operation.</p>				
DWord	Bit	Description		
0	31:0	<p>Context ID Preemption Hint</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="text-align: center;">U32</td> </tr> </table> <p>If 0 this field has no effect. If nonzero it indicates the only context ID that can be preempted when execlists are enabled. A preemption attempt when the context ID of the currently executing ring context does not match this field will be ignored.</p>	Format:	U32
Format:	U32			

VCS Context Sizes

VCS_CXT_SIZE - VCS Context Sizes								
Register Space:	MMIO: 0/2/0							
Project:	CHV, BSW							
Source:	VideoCS							
Default Value:	0x000A1105 CHV, BSW							
Access:	Read/32 bit Write Only							
Size (in bits):	32							
Address:	121A8h							
Valid Projects:	CHV, BSW							
DWord	Bit	Description						
0	31:21	Reserved Format: MBZ						
	20:16	VCS Context Size Format: U5						
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>Ah</td> <td>[Default]</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Value	Name	Project	Ah	[Default]	CHV, BSW
		Value	Name	Project				
	Ah	[Default]	CHV, BSW					
	15:13	Reserved Format: MBZ						
	12:8	VCR Context Size Format: U5						
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>11h</td> <td>[Default]</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Value	Name	Project	11h	[Default]	CHV, BSW
		Value	Name	Project				
	11h	[Default]	CHV, BSW					
	7:5	Reserved Format: MBZ						
	4:0	Execlist Context Size Format: U5						
<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>5h</td> <td>[Default]</td> <td>CHV, BSW</td> </tr> </tbody> </table>		Value	Name	Project	5h	[Default]	CHV, BSW	
Value		Name	Project					
5h	[Default]	CHV, BSW						

VCS Context Timestamp Count

VCS_CTX_TIMESTAMP - VCS Context Timestamp Count				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	123A8h			
Valid Projects:	CHV, BSW			
<p>This register provides a mechanism to obtain cumulative run time of a GPU context on HW. This register gets context save/restored on a context switch. SW must reset this register on very first submission of a context to HW, then afterwards gets context save/restored maintaining the cumulative run time of the corresponding context. This register (effectively) counts at a constant frequency by adjusting the increment amount according to the actual reference clock frequency. SW therefore does not need to know the reference clock frequency. This register gets reset on an engine reset.</p>				
<p>This register is context save restore on a context switch.</p>				
DWord	Bit	Description		
0	31:0	<p>Timestamp Value</p> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td style="text-align: center;">U32</td> </tr> </table> <p>This register increments for every 80 ns of time.</p>	Format:	U32
Format:	U32			

VCS Counter for the bit stream decode engine

VCS_CNTR - VCS Counter for the bit stream decode engine				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoCS			
Default Value:	0xFFFFFFFF			
Access:	R/W			
Size (in bits):	32			
Address:	12178h-1217Bh			
Valid Projects:	CHV, BSW			
DWord	Bit	Description		
0	31:0	<p>Count Value</p> <table border="1"> <tr> <td>Default Value:</td> <td>ffffffffh</td> </tr> </table> <p>Writing a Zero value to this register starts the counting.</p> <p>Writing a Value of FFFF FFFF to this counter stops the counter.</p>	Default Value:	ffffffffh
Default Value:	ffffffffh			

VCS Error Identity Register

VCS_EIR - VCS Error Identity Register													
Register Space:	MMIO: 0/2/0												
Project:	CHV, BSW												
Source:	VideoCS												
Default Value:	0x00000000												
Access:	R/WC												
Size (in bits):	32												
Address:	120B0h												
Valid Projects:	CHV, BSW												
<p>The EIR register contains the persistent values of Hardware-Detected Error Condition bits. Any bit set in this register will cause the Master Error bit in the ISR to be set. The EIR register is also used by software to clear detected errors (by writing a 1 to the appropriate bit(s) except for the unrecoverable bits described).</p>													
DWord	Bit	Description											
0	31:16	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ									
	Format:	MBZ											
15:0	<p>Error Identity Bits</p> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td colspan="2">Array of Error condition bits ee the table titled Hardware-Detected Error Bits</td> </tr> </table> <p>This register contains the persistent values of ESR error status bits that are unmasked via the EMR register. The logical OR of all (defined) bits in this register is reported in the Master Error bit of the Interrupt Status Register. In order to clear an error condition, software must first clear the error by writing a 1 to the appropriate bit(s) in this field. If required, software should then proceed to clear the Master Error bit of the IIR.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="text-align: left;">Value</th> <th style="text-align: left;">Name</th> <th style="text-align: left;">Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>[Default]</td> <td></td> </tr> <tr> <td>1h</td> <td>Error occurred</td> <td>Error occurred</td> </tr> </tbody> </table> <p style="text-align: center;">Programming Notes</p> <p>Writing a 1 to a set bit will cause that error condition to be cleared. However, the Page Table Error bit (Bit 4) cannot be cleared except by reset (i.e., it is a fatal error).</p>	Format:	Array of Error condition bits ee the table titled Hardware-Detected Error Bits		Value	Name	Description	0h	[Default]		1h	Error occurred	Error occurred
Format:	Array of Error condition bits ee the table titled Hardware-Detected Error Bits												
Value	Name	Description											
0h	[Default]												
1h	Error occurred	Error occurred											

VCS Error Mask Register

VCS_EMR - VCS Error Mask Register												
Register Space:	MMIO: 0/2/0											
Project:	CHV, BSW											
Source:	VideoCS											
Default Value:	0xFFFFFFFF CHV, BSW											
Access:	R/W											
Size (in bits):	32											
Address:	120B4h											
Valid Projects:	CHV, BSW											
<p>The EMR register is used by software to control which Error Status Register bits are "masked" or "unmasked". "Unmasked" bits will be reported in the EIR, thus setting the Master Error ISR bit and possibly triggering a CPU interrupt, and will persist in the EIR until cleared by software. "Masked" bits will not be reported in the EIR and therefore cannot generate Master Error conditions or CPU interrupts.</p>												
<p>Undefined or reserved bits in the Hardware Detected Error Bit Table will always return a read value of '1'</p>												
DWord	Bit	Description										
0	31:16	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>FFFFh</td> </tr> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Must Be One</td> </tr> </table>	Default Value:	FFFFh	Project:	CHV, BSW	Format:	Must Be One				
	Default Value:	FFFFh										
Project:	CHV, BSW											
Format:	Must Be One											
15:0	<p>Error Mask Bits</p> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>Array of error condition mask bits See the table titled Hardware-Detected Error Bits.</td> </tr> </table> <p>This register contains a bit mask that selects which error condition bits (from the ESR) are reported in the EIR.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0000h</td> <td>Not Masked</td> <td>Will be reported in the EIR</td> </tr> <tr> <td style="text-align: center;">FFFFh</td> <td>Masked [Default]</td> <td>Will not be reported in the EIR</td> </tr> </tbody> </table>	Format:	Array of error condition mask bits See the table titled Hardware-Detected Error Bits.	Value	Name	Description	0000h	Not Masked	Will be reported in the EIR	FFFFh	Masked [Default]	Will not be reported in the EIR
Format:	Array of error condition mask bits See the table titled Hardware-Detected Error Bits.											
Value	Name	Description										
0000h	Not Masked	Will be reported in the EIR										
FFFFh	Masked [Default]	Will not be reported in the EIR										

VCS Error Status Register

VCS_ESR - VCS Error Status Register										
Register Space:	MMIO: 0/2/0									
Project:	CHV, BSW									
Source:	VideoCS									
Default Value:	0x00000000									
Access:	RO									
Size (in bits):	32									
Address:	120B8h									
Valid Projects:	CHV, BSW									
<p>The ESR register contains the current values of all Hardware-Detected Error condition bits (these are all by definition persistent). The EMR register selects which of these error conditions are reported in the persistent EIR (i.e., set bits must be cleared by software) and thereby causing a Master Error interrupt condition to be reported in the ISR.</p>										
DWord	Bit	Description								
0	31:16	Reserved Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td> </td><td>MBZ</td></tr></table>		MBZ						
		MBZ								
15:0	Error Status Bits Format: Array of error condition bits See the table titled Hardware-Detected Error Bits. This register contains the non-persistent values of all hardware-detected error condition bits. <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>[Default]</td> <td></td> </tr> <tr> <td>1h</td> <td>Error Condition Detected</td> <td>Error Condition detected</td> </tr> </tbody> </table>	Value	Name	Description	0h	[Default]		1h	Error Condition Detected	Error Condition detected
Value	Name	Description								
0h	[Default]									
1h	Error Condition Detected	Error Condition detected								

VCS Execute Condition Code Register

VCS_EXCC - VCS Execute Condition Code Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoCS			
Default Value:	0x00000000			
Access:	R/W, RO			
Size (in bits):	32			
Trusted Type:	1			
Address:	12028h			
Valid Projects:	CHV, BSW			
<p>This register contains user defined and hardware generated conditions that are used by MI_WAIT_FOR_EVENT commands. An MI_WAIT_FOR_EVENT instruction excludes the executing ring from arbitration if the selected event evaluates to a 1, while instruction is discarded if the condition evaluates to a 0. Once excluded, a ring is enabled into arbitration when the selected condition evaluates to a 0.</p> <p>This register also contains control for the invalidation of indirect state pointers on context restore.</p>				
DWord	Bit	Description		
0	31:16	Mask Bits		
		<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>Mask[15:0]</td> </tr> </table> <p>These bits serve as a write enable for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.</p>	Format:	Mask[15:0]
	Format:	Mask[15:0]		
	15:5	Reserved		
		<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
4:0	Reserved			
	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:
Project:	CHV, BSW			
Format:	MBZ			

VCS General Purpose Register

VCS_GPR - VCS General Purpose Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Address:	12600h-1267Fh	
Valid Projects:	CHV, BSW	
This is a general purpose register bank of sixteen 64-bit registers, used as temporary storage by the MI_MATH command to do ALU operations.		
Programming Notes		
Any operation that initiates a read to register 0x1266C will return the value of 0x1260c register. This does not include context save or MI_MATH command operation.		
DWord	Bit	Description
0	63:0	Reserved Format: MBZ

VCS Hardware Status Mask Register

VCS_HWSTAM - VCS Hardware Status Mask Register						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	VideoCS					
Default Value:	0xFFFFFFFF					
Access:	R/W					
Size (in bits):	32					
Trusted Type:	1					
Address:	12098h					
Valid Projects:	CHV, BSW					
Access: RO for Reserved Control bits						
<p>The HWSTAM register has the same format as the Interrupt Control Registers. The bits in this register are "mask" bits that prevent the corresponding bits in the Interrupt Status Register from generating a "Hardware Status Write" (PCI write cycle). Any unmasked interrupt bit (HWSTAM bit set to 0) will allow the Interrupt Status Register to be written to the ISR location (within the memory page specified by the Hardware Status Page Address Register) when that Interrupt Status Register bit changes state.</p>						
Programming Notes						
<ul style="list-style-type: none"> To write the interrupt to the HWSP, the corresponding IMR bit must also be clear (enabled). At most 1 bit can be unmasked at any given time. 						
DWord	Bit	Description				
0	31:0	Hardware Status Mask Register <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Default Value:</td> <td>FFFFFFFFh</td> </tr> <tr> <td>Format:</td> <td>Array of Masks</td> </tr> </table> <p>Refer to the table in the Interrupt Control Register section for bit definitions.</p>	Default Value:	FFFFFFFFh	Format:	Array of Masks
Default Value:	FFFFFFFFh					
Format:	Array of Masks					

VCS IDLE Max Count

VCS_PWRCTX_MAXCNT - VCS IDLE Max Count			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	VideoCS		
Default Value:	0x00000040 CHV, BSW		
Access:	R/W		
Size (in bits):	32		
Trusted Type:	1		
Address:	12054h		
Valid Projects:	CHV, BSW		
This register contains the time in 0.64us to wait before telling power management hardware the render pipe is IDLE			
DWord	Bit	Description	
0	31:20	Reserved	
		Format: <table border="1"><tr><td> </td><td>MBZ</td></tr></table>	
	MBZ		
	19:0	Reserved	

VCS Idle Switch Delay

VCS_IDLELY - VCS Idle Switch Delay		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	1223Ch	
Valid Projects:	CHV, BSW	
<p>The IDLEDLY register contains an Idle Delay field which specifies the minimum number of microseconds allowed for command streamer to wait before a context is switched out leading to IDLE state in Execlist mode, i.e following this context switch there is no active element available in HW to execute. A default value of 0, means that by default, there is no restriction to wait on a context switch leading to IDLE. This register has no significance when Execlists are not enabled.</p>		
DWord	Bit	Description
0	31:21	Reserved
		Project: All
		Format: MBZ
	20:0	IDLE Delay
		Project: All
		Format: U21
		Minimum number of micro-seconds allowed.

VCS Instruction Parser Mode Register

VCS_INSTPM - VCS Instruction Parser Mode Register					
Register Space:	MMIO: 0/2/0				
Project:	CHV, BSW				
Source:	VideoCS				
Default Value:	0x00000000				
Access:	R/W				
Size (in bits):	32				
Address:	120C0h-120C3h				
Valid Projects:	CHV, BSW				
<p>The VCS_INSTPM register is used to control the operation of the VCS Instruction Parser. Certain classes of instructions can be disabled (ignored) - often useful for detecting performance bottlenecks. Also, "Synchronizing Flush" operations can be initiated - useful for ensuring the completion (vs. only parsing) of rendering instructions. DefaultValue=0000 0000h</p>					
Programming Notes					
All reserved bits are implemented.					
DWord	Bit	Description			
0	31:16	Masks			
		<table border="1"> <tr> <td>Format:</td> <td>Mask[15:0]</td> </tr> </table> <p>These bits serve as write enables for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.</p>	Format:	Mask[15:0]	
	Format:	Mask[15:0]			
	15:11	Reserved			
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:
	Project:	All			
	Format:	MBZ			
	10	Reserved			
	9	Reserved			
		<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:
	Project:	CHV, BSW			
	Format:	MBZ			
8:7	Reserved				
6:5	Reserved				
	<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ
Project:	CHV, BSW				
Format:	MBZ				
4:0	Reserved				
	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Access:	R/W		
Access:	R/W				

VCS_INSTPM - VCS Instruction Parser Mode Register

	Format:	MBZ
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VCS Interrupt Mask Register

VCS_IMR - VCS Interrupt Mask Register																				
Register Space:	MMIO: 0/2/0																			
Project:	CHV, BSW																			
Source:	VideoCS																			
Default Value:	0xFFFFFFFF																			
Access:	R/W																			
Size (in bits):	32																			
Address:	120A8h																			
Valid Projects:	CHV, BSW																			
<p>The IMR register is used by software to control which Interrupt Status Register bits are masked or unmasked. Unmasked bits will be reported in the IIR, possibly triggering a CPU interrupt, and will persist in the IIR until cleared by software. Masked bits will not be reported in the IIR and therefore cannot generate CPU interrupts.</p>																				
DWord	Bit	Description																		
0	31:0	<p>Interrupt Mask Bits</p> <table border="1"> <tr> <td>Format:</td> <td colspan="2">Array of interrupt mask bits Refer to the Interrupt Control Register section for bit definitions.</td> </tr> <tr> <td colspan="3">This field contains a bit mask which selects which interrupt bits (from the ISR) are reported in the IIR.</td> </tr> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> <tr> <td>FFFF FFFFh</td> <td>[Default]</td> <td></td> </tr> <tr> <td>0h</td> <td>Not Masked</td> <td>Will be reported in the IIR</td> </tr> <tr> <td>1h</td> <td>Masked</td> <td>Will not be reported in the IIR</td> </tr> </table>	Format:	Array of interrupt mask bits Refer to the Interrupt Control Register section for bit definitions.		This field contains a bit mask which selects which interrupt bits (from the ISR) are reported in the IIR.			Value	Name	Description	FFFF FFFFh	[Default]		0h	Not Masked	Will be reported in the IIR	1h	Masked	Will not be reported in the IIR
Format:	Array of interrupt mask bits Refer to the Interrupt Control Register section for bit definitions.																			
This field contains a bit mask which selects which interrupt bits (from the ISR) are reported in the IIR.																				
Value	Name	Description																		
FFFF FFFFh	[Default]																			
0h	Not Masked	Will be reported in the IIR																		
1h	Masked	Will not be reported in the IIR																		

VCS Mode Register for Software Interface

VCS_MI_MODE - VCS Mode Register for Software Interface											
Register Space:	MMIO: 0/2/0										
Project:	CHV, BSW										
Source:	VideoCS										
Default Value:	0x00000200 CHV, BSW										
Access:	R/W										
Size (in bits):	32										
Address:	1209Ch-1209Fh										
Valid Projects:	CHV, BSW										
The MI_MODE register contains information that controls software interface aspects of the command parser.											
DWord	Bit	Description									
0	31:16	Masks A 1 in a bit in this field allows the modification of the corresponding bit in Bits 15:0.									
	15	Suspend Flush Mask: MMIO(0x209c)#31									
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>No Delay</td> <td>HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well</td> </tr> <tr> <td>1h</td> <td>DelayFlush</td> <td>Suspend flush is active</td> </tr> </tbody> </table>	Value	Name	Description	0h	No Delay	HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well	1h	DelayFlush	Suspend flush is active
		Value	Name	Description							
		0h	No Delay	HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well							
	1h	DelayFlush	Suspend flush is active								
	14:12	Reserved Access: R/W									
	11	Invalidate UHPTR enable If bit set H/W clears the valid bit of BCS_UHPTR (4134h, bit 0) when current active head pointer is equal to UHPTR.									
	10	Atomic Read Return for MI_COPY_MEM_MEM Project: CHV, BSW Format: U1									
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disable [Default]</td> <td>Hardware does a regular memory fence write to complete the write to the destination address before moving to the next instruction.</td> </tr> <tr> <td>1h</td> <td>Enable</td> <td>Hardware does Atomic Move with Read Return to complete the write to the destination address before moving to the next instruction.</td> </tr> </tbody> </table>	Value	Name	Description	0h	Disable [Default]	Hardware does a regular memory fence write to complete the write to the destination address before moving to the next instruction.	1h	Enable	Hardware does Atomic Move with Read Return to complete the write to the destination address before moving to the next instruction.
Value		Name	Description								
0h		Disable [Default]	Hardware does a regular memory fence write to complete the write to the destination address before moving to the next instruction.								
1h	Enable	Hardware does Atomic Move with Read Return to complete the write to the destination address before moving to the next instruction.									

VCS_MI_MODE - VCS Mode Register for Software Interface

9	Ring Idle (Read Only Status bit)	Access: _____ RO	
	<i>Writes to this bit are not allowed.</i>		
	Value	Name	
	0	Parser not idle	
	1	Parser idle [Default]	
8	Stop Ring	Software must set this bit to force the Ring and Command Parser to Idle. Software must read a "1" in Ring Idle bit after setting this bit to ensure that the hardware is idle.	
	<i>Software must clear this bit for Ring to resume normal operation.</i>		
	Value	Name	
	0	Normal Operation	
	1	Parser is turned off	
7:0	Reserved	Access: _____ R/W	

VCS Reported Timestamp Count

VCS_TIMESTAMP - VCS Reported Timestamp Count				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoCS			
Default Value:	0x00000000, 0x00000000			
Access:	RO. This register is not set by the context restore.			
Size (in bits):	64			
Address:	12358h			
Valid Projects:	CHV, BSW			
<p>This register provides an elapsed real-time value that can be used as a timestamp. This register is not reset by a graphics reset. It will maintain its value unless a full chipset reset is performed. Note: This timestamp register reflects the value of the PCU TSC. The PCU TSC counts 10ns increments; this timestamp reflects bits 38:3 of the TSC (i.e. 80ns granularity, rolling over every 1.5 hours).</p>				
DWord	Bit	Description		
0	63:36	Reserved <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
35:0	Timestamp Value <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>U36</td> </tr> </table> <p>This register toggles every 80 ns. The upper 28 bits are zero.</p>	Format:	U36	
Format:	U36			

VCS Reset Control Register

VCS_RESET_CTRL - VCS Reset Control Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	120D0h	
Valid Projects:	CHV, BSW	
This register is to be used to control soft reset.		
DWord	Bit	Description
0	31:16	Mask Bits
		Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>Mask[15:0]</td></tr></table> Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	Mask[15:0]	
	15:2	Reserved
Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>MBZ</td></tr></table>		MBZ
MBZ		
1	Ready for Reset	
	Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>U1</td></tr></table> When set indicates video codec engine is ready for reset. This bit gets cleared on engine reset or when Soft Reset In progress is cleared.	U1
U1		
0	Request Reset	
	Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>U1</td></tr></table> When set indicates SW wishes to reset the video codec engine. On seeing this bit set Command Streamer will take appropriate action and set Ready For Reset status bit. This bit gets cleared on engine reset.	U1
U1		

VCS Ring Buffer Next Context ID Register

VCS_RNCID - VCS Ring Buffer Next Context ID Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Address:	12198h-1219Fh	
Valid Projects:	CHV, BSW	
This register contains the next ring context ID associated with the ring buffer.		
Programming Notes		
The current context (RCCID) register can be updated indirectly from this register on a context switch event. Note that this can only be triggered when arbitration is enabled or if the current context runs dry (head pointer becomes equal to tail pointer).		
DWord	Bit	Description
0	63:0	Context ID See Context Descriptor for VCS.

VCS Semaphore Polling Interval on Wait

VCS_SEMA_WAIT_POLL - VCS Semaphore Polling Interval on Wait				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	1224Ch			
Valid Projects:	CHV, BSW			
<p>The SEMA_WAIT_POLL register contains Poll Interval field which specifies the minimum number of microseconds allowed for command streamer to wait before re-fetching the data from the address mentioned in the MI_SEMAPHORE_WAIT command on WAIT Mode set to POLL until the condition is satisfied while the context is not switched out. When value of 0 is written the poll interval will be equal to the memory latency of the read completion.</p>				
DWord	Bit	Description		
0	31:21	Reserved Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td> </td><td>MBZ</td></tr></table>		MBZ
		MBZ		
20:0	Poll Interval Minimum number of micro-seconds allowed			

VCS Threshold for the counter of bit stream decode engine

VCS_THRSH - VCS Threshold for the counter of bit stream decode engine				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoCS			
Default Value:	0x00150000			
Access:	R/W			
Size (in bits):	32			
Address:	1217Ch-1217Fh			
DWord	Bit	Description		
0	31:0	<p>Threshold Value</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: right;">00150000h</td> </tr> </table> <p>The value in this register reflects the number of clocks the bit stream decode engine is expected to run. If the value is exceeded the counter is reset and an interrupt may be enabled in the device.</p>	Default Value:	00150000h
Default Value:	00150000h			

VCW Clock Count

VCW_CLOCK_CNT - VCW Clock Count				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoEnhancementCS			
Default Value:	0x00000000			
Access:	RO			
Size (in bits):	32			
Trusted Type:	1			
Address:	08820h			
ShortName:	VCW0_CLOCK_CNT			
Address:	08920h			
ShortName:	VCW1_CLOCK_CNT			
DWord	Bit	Description		
0	31:24	Reserved Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td style="text-align: center;">MBZ</td></tr></table>		MBZ
		MBZ		
23:0	Max clock count Default Value: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 150px;"></td><td style="text-align: center;">0h</td></tr></table> Maximum number of clocks taken by VCW to process a column		0h	
	0h			

VCW Internal Latency

VCW_INTERNAL_LAT - VCW Internal Latency		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoEnhancementCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	08824h	
ShortName:	VCW0_INTERNAL_LAT	
Address:	08924h	
ShortName:	VCW1_INTERNAL_LAT	
DWord	Bit	Description
0	31:24	Reserved Format: MBZ
	23:0	VCW internal data latency count Default Value: 0h

VCW Min Max Latency

VCW_MINMAX_LAT - VCW Min Max Latency				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoEnhancementCS			
Default Value:	0x00000000			
Access:	RO			
Size (in bits):	32			
Trusted Type:	1			
Address:	08828h			
ShortName:	VCW0_MINMAX_LAT			
Address:	08928h			
ShortName:	VCW1_MINMAX_LAT			
DWord	Bit	Description		
0	31:16	Current request count <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>0h</td> </tr> </table>	Default Value:	0h
	Default Value:	0h		
	15:8	Max latency <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>0h</td> </tr> </table> Maximum number of clocks taken for tag 200h	Default Value:	0h
Default Value:	0h			
7:0	Min latency <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>0h</td> </tr> </table> Minimum number of clocks taken for tag 200h	Default Value:	0h	
Default Value:	0h			

VCW Total Latency

VCW_TOTAL_LAT - VCW Total Latency				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoEnhancementCS			
Default Value:	0x00000000			
Access:	RO			
Size (in bits):	32			
Trusted Type:	1			
Address:	0882Ch			
ShortName:	VCW0_TOTAL_LAT			
Address:	0892Ch			
ShortName:	VCW1_TOTAL_LAT			
DWord	Bit	Description		
0	31:0	<p>Total latency</p> <table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> </table> <p>Accumulation of latency per frame for tag 200h</p>	Default Value:	0h
Default Value:	0h			

VCW XY position

VCW_XY_POS - VCW XY position				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoEnhancementCS			
Default Value:	0x00000000			
Access:	RO			
Size (in bits):	32			
Trusted Type:	1			
Address:	08830h			
ShortName:	VCW0_XY_POS			
Address:	08930h			
ShortName:	VCW1_XY_POS			
DWord	Bit	Description		
0	31:16	Current Y value <table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> </table> Current Y position of VCW walker	Default Value:	0h
	Default Value:	0h		
15:0	Current X value <table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> </table> Current X position of VCW walker	Default Value:	0h	
Default Value:	0h			

VEBOX TLB Control Register

VTCR - VEBOX TLB Control Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	04270h			
DWord	Bit	Description		
0	31:1	Reserved		
		<table border="1"> <tr> <td>Default Value:</td> <td>00000000000000000000000000000000b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	00000000000000000000000000000000b
Default Value:	00000000000000000000000000000000b			
Access:	RO			
0	0	Invalidate TLBs on the corresponding Engine		
		<table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. This bit is self clear.</p>	Default Value:	0b
Default Value:	0b			
Access:	R/W			

VEBX Context Element Descriptor (High Part)

VEBX_CTX_EDR_H - VEBX Context Element Descriptor (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044C4h	
DWord	Bit	Description
0	31:0	VEBX Context Element Descriptor (High Part)
		Default Value: 00000000h
		Access: R/W

VEBX Context Element Descriptor (Low Part)

VEBX_CTX_EDR_L - VEBX Context Element Descriptor (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000009	
Size (in bits):	32	
Address:	044C0h	
DWord	Bit	Description
0	31:0	VEBX Context Element Descriptor (Low Part)
		Default Value: 00000009h
		Access: R/W

VEBX Context Element Descriptor (Low Part)

VEBX_CTX_EDR_L - VEBX Context Element Descriptor (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000009	
Size (in bits):	32	
Address:	044C0h	
DWord	Bit	Description
0	31:0	VEBX Context Element Descriptor
		Default Value: 00000009h
		Access: R/W

VEBX LRA 0

VEBX_LRA_0 - VEBX LRA 0			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x2F201F00		
Size (in bits):	32		
Address:	04A80h		
DWord	Bit	Description	
0	31:30	Reserved	
		Default Value:	00b
		Access:	RO
	29:24	VEBX LRA1 Max	
		Default Value:	101111b
		Access:	R/W
			Maximum value of programmable LRA1.
	23:22	Reserved	
		Default Value:	00b
		Access:	RO
21:16	VEBX LRA1 Min		
	Default Value:	100000b	
	Access:	R/W	
		Minimum value of programmable LRA1.	
15:14	Reserved		
	Access:	RO	
13:8	VEBX LRA0 Max		
	Default Value:	011111b	
	Access:	R/W	
		Maximum value of programmable LRA0.	
7:6	Reserved		
	Default Value:	00b	
	Access:	RO	
5:0	VEBXLRA0 Min		
	Default Value:	000000b	
	Access:	R/W	
		Minimum value of programmable LRA0.	

VEBX LRA 1

VEBX_LRA_1 - VEBX LRA 1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x06003F30	
Size (in bits):	32	
Address:	04A84h	
DWord	Bit	Description
0	31:30	Reserved
		Default Value: 00b
		Access: RO
	29:28	VECS
		Default Value: 00b
		Access: R/W Which LRA should VECS use.
	27:26	VFW
		Default Value: 01b
		Access: R/W Which LRA should VFW use.
	25:24	VEO
		Default Value: 10b
		Access: R/W Which LRA should VEO use.
	23:14	Reserved
		Default Value: 0000000000b
Access: RO		
13:8	VEBXLRA2 Max	
	Default Value: 111111b	
	Access: R/W Minimum value of programmable LRA2.	
7:6	Reserved	
	Default Value: 00b	
	Access: RO	

VEBX_LRA_1 - VEBX LRA 1						
	5:0	<p>VEBXLRA2 Min</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Default Value:</td> <td>110000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Minimum value of programmable LRA2.</p>	Default Value:	110000b	Access:	R/W
Default Value:	110000b					
Access:	R/W					

VEBX PDP0/PML4/PASID Descriptor (High Part)

VEBX_CTX_PDP0_H - VEBX PDP0/PML4/PASID Descriptor (High Part)						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	044CCh					
DWord	Bit	Description				
0	31:0	VEBX PDP0/PML4/PASID Descriptor (High Part) <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

VEBX PDP0/PML4/PASID Descriptor (Low Part)

VEBX_CTX_PDP0_L - VEBX PDP0/PML4/PASID Descriptor (Low Part)						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	044C8h					
DWord	Bit	Description				
0	31:0	VEBX PDP0/PML4/PASID Descriptor (Low Part) <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

VEBX PDP1 Descriptor Register (High Part)

VEBX_CTX_PDP1_H - VEBX PDP1 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044D4h	
DWord	Bit	Description
0	31:0	VEBX PDP1 Descriptor Register (High Part)
		Default Value: 00000000h
		Access: R/W

VEBX PDP1 Descriptor Register (Low Part)

VEBX_CTX_PDP1_L - VEBX PDP1 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044D0h	
DWord	Bit	Description
0	31:0	VEBX PDP1 Descriptor Register (Low Part)
		Default Value: 00000000h
		Access: R/W

VEBX PDP2 Descriptor Register (High Part)

VEBX_CTX_PDP2_H - VEBX PDP2 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044DCh	
DWord	Bit	Description
0	31:0	VEBX PDP2 Descriptor Register (High Part)
		Default Value: 00000000h
		Access: R/W

VEBX PDP2 Descriptor Register (Low Part)

VEBX_CTX_PDP2_L - VEBX PDP2 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044D8h	
DWord	Bit	Description
0	31:0	VEBX PDP2 Descriptor Register (Low Part)
		Default Value: 00000000h
		Access: R/W

VEBX PDP3 Descriptor Register (High Part)

VEBX_CTX_PDP3_H - VEBX PDP3 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044E4h	
DWord	Bit	Description
0	31:0	VEBX PDP3 Descriptor Register (High Part)
		Default Value: 00000000h
		Access: R/W

VEBX PDP3 Descriptor Register (Low Part)

VEBX_CTX_PDP3_L - VEBX PDP3 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044E0h	
DWord	Bit	Description
0	31:0	VEBX PDP3 Descriptor Register (Low Part)
		Default Value: 00000000h
		Access: R/W

VECS_PREEMPTION_HINT

VECS_PREEMPTION_HINT - VECS_PREEMPTION_HINT											
Register Space:	MMIO: 0/2/0										
Project:	CHV, BSW										
Source:	VideoEnhancementCS										
Default Value:	0x00000000										
Access:	R/W										
Size (in bits):	32										
Address:	1A4BCh										
<p>This register contains the Head pointer offset in to the Ring Buffer or the Dword aligned Graphics address in to the Batch Buffer corresponding to either MI_ARB_CHECK called Preemption Hint Address. When Preemption Hint Address is enabled, VECS will honor UHPTR only on parsing MI_ARB_CHK at Preemption Hint Address.</p> <p>This register contains the Head pointer offset into the Ring Buffer or the Dword aligned Graphics address into the Batch Buffer corresponding to the below listed commands in execlist mode of operation</p> <ul style="list-style-type: none"> MI_ARB_CHECK MI_WAIT_FOR_EVENT MI_SEMAPHORE_WAIT 											
Programming Notes											
<p>Programming Restriction:This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of UHPTR being sampled by a given MI_ARB_CHECK in command stream. Programmer has to ensure that VECS Preemption Hint register gets programmed before UHPTR is programmed and well before VECS crosses the corresponding execution point. Preemption hint for both RingBuffer and Batch Buffer can't be enabled simultaneously.</p>											
DWord	Bit	Description									
0	31:2	Preempted Hint Address									
		<table border="1"> <tr> <td>Format:</td> <td>U30</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[31:2]</td> </tr> </table> <p>This field contains the Head offset in to the Ring Buffer when Preemption Hint is set to Ring Buffer and Dword aligned Graphics Address in to the batch buffer when Preemption Hint is set to Batch Buffer.</p>	Format:	U30	Format:	GraphicsAddress[31:2]					
Format:	U30										
Format:	GraphicsAddress[31:2]										
1	1	Batch Buffer Preemption Hint									
		Format: Enable									
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disabled</td> <td>Preemption hint is disabled in batch buffer.</td> </tr> <tr> <td>1h</td> <td>Enabled</td> <td>Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Batch Buffer.</td> </tr> </tbody> </table>	Value	Name	Description	0h	Disabled	Preemption hint is disabled in batch buffer.	1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Batch Buffer.
		Value	Name	Description							
0h	Disabled	Preemption hint is disabled in batch buffer.									
1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Batch Buffer.									

VECS_PREEMPTION_HINT - VECS_PREEMPTION_HINT

	0	Ring Preemption Hint		
		Format:	Enable	
		Value	Name	Description
		0h	Disable	Preemption hint is disabled in ring buffer.
1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Ring Buffer.		

VECS Context ID Preemption Hint

VECS_CTXID_PREEMPTION_HINT - VECS Context ID Preemption Hint				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoEnhancementCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	1A4CCh			
<p>This register contains the Context ID of a context in Execlist mode of operation. In execlist mode of operation VECS_PREEMPTION_HINT registers are looked at by Video Enhancement Command Streamer on executing a context having Context ID that matches with the contents of this register. This register contents are valid and looked at only in Execlist mode of operation.</p>				
Programming Notes				
<p>This register should NEVER be programmed in functional mode, this must be used only in validation mode to achieve deterministic preemption behavior in execlist mode of operation.</p>				
DWord	Bit	Description		
0	31:0	<p>Context ID Preemption Hint</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="text-align: center;">U32</td> </tr> </table> <p>If 0 this field has no effect. If nonzero it indicates the only context ID that can be preempted when execlists are enabled. A preemption attempt when the context ID of the currently executing ring context does not match this field will be ignored.</p>	Format:	U32
Format:	U32			

VECS Context Timestamp Count

VECS_CTX_TIMESTAMP - VECS Context Timestamp Count				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoEnhancementCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	1A3A8h			
<p>This register provides a mechanism to obtain cumulative run time of a GPU context on HW. This register gets context save/restored on a context switch. SW must reset this register on very first submission of a context to HW, then afterwards gets context save/restored maintaining the cumulative run time of the corresponding context. Note that the value of this register can be obtained in a 3D pipeline-synchronous fashion without a pipeline flush by using the PIPE_CONTROL command. See 3D Geometry Pipeline in the "3D and Media" volume. This register (effectively) counts at a constant frequency by adjusting the increment amount according to the actual reference clock frequency. SW therefore does not need to know the reference clock frequency. This register gets reset on an engine reset.</p> <p>This register is context save restore on a context switch.</p>				
DWord	Bit	Description		
0	31:0	<p>Timestamp Value</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>This register increments for every 80 ns of time.</p>	Format:	U32
Format:	U32			

VECS Counter for the Video Enhancement Engine

VECS_CNTR - VECS Counter for the Video Enhancement Engine				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoEnhancementCS			
Default Value:	0xFFFFFFFF			
Access:	R/W			
Size (in bits):	32			
Address:	1A178h			
DWord	Bit	Description		
0	31:0	<p>Count Value</p> <table border="1"> <tr> <td>Default Value:</td> <td>ffffffffh</td> </tr> </table> <p>Writing a Zero value to this register starts the counting. Writing a Value of FFFF FFFF to this counter stops the counter.</p>	Default Value:	ffffffffh
Default Value:	ffffffffh			

VECS Error Identity Register

VECS_EIR - VECS Error Identity Register			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	VideoEnhancementCS		
Default Value:	0x00000000		
Access:	R/WC		
Size (in bits):	32		
Address:	1A0B0h		
<p>The EIR register contains the persistent values of Hardware-Detected Error Condition bits. Any bit set in this register will cause the Master Error bit in the ISR to be set. The EIR register is also used by software to clear detected errors (by writing a '1' to the appropriate bit(s) except for the unrecoverable bits described).</p>			
DWord	Bit	Description	
0	31:16	Reserved	
		Project:	All
		Format:	MBZ
	15:0	Error Identity Bits	
		Project:	All
		Format:	Array of Error condition bits See Table 1 5. Hardware-Detected Error Bits
<p>This register contains the persistent values of ESR error status bits that are unmasked via the EMR register. (See Error! Reference source not found.). The logical OR of all (defined) bits in this register is reported in the Master Error bit of the Interrupt Status Register. In order to clear an error condition, software must first clear the error by writing a '1' to the appropriate bit(s) in this field. If required, software should then proceed to clear the Master Error bit of the IIR.</p>			
		Value	Name
		Description	Project
		0h	[Default]
		1h	Error occurred
		Error occurred	All
Programming Notes			
<p>Writing a '1' to a set bit will cause that error condition to be cleared. However, the Page Table Error bit (Bit 4) can not be cleared except by reset (i.e., it is a fatal error).</p>			

VECS Error Mask Register

VECS_EMR - VECS Error Mask Register			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	VideoEnhancementCS		
Default Value:	0xFFFFFFFF CHV, BSW		
Access:	R/W		
Size (in bits):	32		
Address:	1A0B4h		
<p>The EMR register is used by software to control which Error Status Register bits are "masked" or "unmasked". "Unmasked" bits will be reported in the EIR, thus setting the Master Error ISR bit and possibly triggering a CPU interrupt, and will persist in the EIR until cleared by software. "Masked" bits will not be reported in the EIR and therefore cannot generate Master Error conditions or CPU interrupts.</p> <p>Undefined or reserved bits in the Hardware Detected Error Bit Table will always return a read value of '1'</p>			
DWord	Bit	Description	
0	31:16	Reserved	
		Default Value:	FFFFh
		Project:	CHV, BSW
		Format:	Must Be One
	15:0	Error Mask Bits	
		Project:	All
		Format:	Array of error condition mask bits See Table 1 5. Hardware-Detected Error Bits
This register contains a bit mask that selects which error condition bits (from the ESR) are reported in the EIR.			
	Value	Name	Description
	0000h	Not Masked	Will be reported in the EIR
	FFFFh	Masked [Default]	Will not be reported in the EIR

VECS Error Status Register

VECS_ESR - VECS Error Status Register			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	VideoEnhancementCS		
Default Value:	0x00000000		
Access:	RO		
Size (in bits):	32		
Address:	1A0B8h		
<p>The ESR register contains the current values of all Hardware-Detected Error condition bits (these are all by definition "persistent"). The EMR register selects which of these error conditions are reported in the persistent EIR (i.e., set bits must be cleared by software) and thereby causing a Master Error interrupt condition to be reported in the ISR.</p>			
DWord	Bit	Description	
0	31:16	Reserved	
		Project:	All
		Format:	MBZ
0	15:0	Error Status Bits	
		Project:	All
		Format:	Array of error condition bits See Table 1 5. Hardware-Detected Error Bits
		This register contains the non-persistent values of all hardware-detected error condition bits.	
		Value	Name
0h	[Default]		
1h	Error Condition Detected	Error Condition detected	All

VECS General Purpose Register

VECS_GPR - VECS General Purpose Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoEnhancementCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Address:	1A600h-1A67Fh	
This is a general purpose register bank of sixteen 64-bit registers, used as temporary storage by the MI_MATH command to do ALU operations.		
Programming Notes		Project
Any operation that initiates a read to register 0x1A66C will return the value of 0x1A60c register. This does not include context save or MI_MATH command operation.		CHV, BSW
DWord	Bit	Description
0	63:0	Reserved
		Format: MBZ

VECS Hardware Status Mask Register

VECS_HWSTAM - VECS Hardware Status Mask Register								
Register Space:	MMIO: 0/2/0							
Project:	CHV, BSW							
Source:	VideoEnhancementCS							
Default Value:	0xFFFFFFFF							
Access:	R/W							
Size (in bits):	32							
Trusted Type:	1							
Address:	1A098h							
Access: RO for Reserved Control bits								
<p>The HWSTAM register has the same format as the Interrupt Control Registers. The bits in this register are "mask" bits that prevent the corresponding bits in the Interrupt Status Register from generating a "Hardware Status Write" (PCI write cycle). Any unmasked interrupt bit (HWSTAM bit set to 0) will allow the Interrupt Status Register to be written to the ISR location (within the memory page specified by the Hardware Status Page Address Register) when that Interrupt Status Register bit changes state.</p>								
Programming Notes								
<ul style="list-style-type: none"> To write the interrupt to the HWSP, the corresponding IMR bit must also be clear (enabled). At most 1 bit can be unmasked at any given time. 								
DWord	Bit	Description						
0	31:0	<p>Hardware Status Mask Register</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>FFFFFFFFh</td> </tr> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Array of Masks</td> </tr> </table> <p>refer to Table 4-4 in Interrupt Control Register section for bit definitions</p>	Default Value:	FFFFFFFFh	Project:	All	Format:	Array of Masks
Default Value:	FFFFFFFFh							
Project:	All							
Format:	Array of Masks							

VECS IDLE Max Count

VECS_PWRCTX_MAXCNT - VECS IDLE Max Count		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoEnhancementCS	
Default Value:	0x00000040	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	1A054h	
This register contains the time in 0.64us to wait before telling power management hardware the render pipe is IDLE		
DWord	Bit	Description
0	31:20	Reserved
		Project: All
	Format: MBZ	
	19:0	Reserved

VECS Instruction Parser Mode Register

VECS_INSTPM - VECS Instruction Parser Mode Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoEnhancementCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	1A0C0h-1A0C3h	
<p>The VECS_INSTPM register is used to control the operation of the VECS Instruction Parser. Certain classes of instructions can be disabled (ignored) - often useful for detecting performance bottlenecks. Also, "Synchronizing Flush" operations can be initiated - useful for ensuring the completion (vs. only parsing) of rendering instructions.</p>		
Programming Notes		
All reserved bits are implemented		
DWord	Bit	Description
0	31:16	Masks
		Format: Mask[15:0]
	These bits serve as write enables for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.	
	15:11	Reserved
		Project: All
	Format: MBZ	
	10	Reserved
	9	Reserved
		Project: CHV, BSW
	Format: MBZ	
8:7	Reserved	
Format: MBZ		
6:5	Reserved	
	Project: CHV, BSW	
Format: MBZ		
4:0	Reserved	

VECS Interrupt Mask Register

VECS_IMR - VECS Interrupt Mask Register																							
Register Space:	MMIO: 0/2/0																						
Project:	CHV, BSW																						
Source:	VideoEnhancementCS																						
Default Value:	0xFFFFFFFF																						
Access:	R/W																						
Size (in bits):	32																						
Address:	1A0A8h																						
<p>The IMR register is used by software to control which Interrupt Status Register bits are "masked" or "unmasked". "Unmasked" bits will be reported in the IIR, possibly triggering a CPU interrupt, and will persist in the IIR until cleared by software. "Masked" bits will not be reported in the IIR and therefore cannot generate CPU interrupts.</p>																							
DWord	Bit	Description																					
0	31:0	<p>Interrupt Mask Bits</p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Array of interrupt mask bits Refer to Table 4-4 in Interrupt Control Register section for bit definitions</td> </tr> </table> <p>This field contains a bit mask which selects which interrupt bits (from the ISR) are reported in the IIR.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>FFFF FFFFh</td> <td>[Default]</td> <td></td> <td></td> </tr> <tr> <td>0h</td> <td>Not Masked</td> <td>Will be reported in the IIR</td> <td>All</td> </tr> <tr> <td>1h</td> <td>Masked</td> <td>Will not be reported in the IIR</td> <td>All</td> </tr> </tbody> </table>		Project:	All	Format:	Array of interrupt mask bits Refer to Table 4-4 in Interrupt Control Register section for bit definitions	Value	Name	Description	Project	FFFF FFFFh	[Default]			0h	Not Masked	Will be reported in the IIR	All	1h	Masked	Will not be reported in the IIR	All
Project:	All																						
Format:	Array of interrupt mask bits Refer to Table 4-4 in Interrupt Control Register section for bit definitions																						
Value	Name	Description	Project																				
FFFF FFFFh	[Default]																						
0h	Not Masked	Will be reported in the IIR	All																				
1h	Masked	Will not be reported in the IIR	All																				

VECS Mode Register for Software Interface

VECS_MI_MODE - VECS Mode Register for Software Interface										
Register Space:	MMIO: 0/2/0									
Project:	CHV, BSW									
Source:	VideoEnhancementCS									
Default Value:	0x00000200 CHV, BSW									
Access:	R/W									
Size (in bits):	32									
Address:	1A09Ch-1A09Fh									
The MI_MODE register contains information that controls software interface aspects of the command parser										
DWord	Bit	Description								
0	31:16	Masks A "1" in a bit in this field allows the modification of the corresponding bit in Bits 15:0								
	15	Suspend Flush <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Mask:</td> <td>MMIO(0x209c)#31</td> </tr> </table>	Project:	All	Mask:	MMIO(0x209c)#31				
		Project:	All							
		Mask:	MMIO(0x209c)#31							
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>No Delay</td> <td>HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well</td> </tr> <tr> <td>1h</td> <td>Delay Flush</td> <td>Suspend flush is active</td> </tr> </tbody> </table>	Value	Name	Description	0h	No Delay	HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well	1h	Delay Flush
	Value	Name	Description							
	0h	No Delay	HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well							
	1h	Delay Flush	Suspend flush is active							
	<table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ							
	Format:	MBZ								
11	Invalidate UHPTR Enable If bit set H/W clears the valid bit of BCS_UHPTR (4134h, bit 0) when current active head pointer is equal to UHPTR.									
10	Atomic Read Return for MI_COPY_MEM_MEM <table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table>	Project:	CHV, BSW	Format:	U1					
	Project:	CHV, BSW								
	Format:	U1								
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disable [Default]</td> <td>Hardware does a regular memory fence write to complete the write to the destination address before moving to the next instruction.</td> </tr> <tr> <td>1h</td> <td>Enable</td> <td>Hardware does Atomic Move with Read Return to complete the write to the destination address before moving to the next instruction.</td> </tr> </tbody> </table>	Value	Name	Description	0h	Disable [Default]	Hardware does a regular memory fence write to complete the write to the destination address before moving to the next instruction.	1h	Enable	Hardware does Atomic Move with Read Return to complete the write to the destination address before moving to the next instruction.
Value	Name	Description								
0h	Disable [Default]	Hardware does a regular memory fence write to complete the write to the destination address before moving to the next instruction.								
1h	Enable	Hardware does Atomic Move with Read Return to complete the write to the destination address before moving to the next instruction.								
<table border="1"> <tr> <td>Format:</td> <td></td> </tr> </table>	Format:									
Format:										

VECS_MI_MODE - VECS Mode Register for Software Interface

	9	Ring Idle (Read Only Status bit)		
		<i>Writes to this bit are not allowed.</i>		
		Value	Name	
		0	Parser not idle	
		1	Parser idle [Default]	
	8	Stop Ring 0 = Normal Operation. 1 = Parser is turned off. Software must set this bit to force the Ring and Command Parser to Idle. Software must read a "1" in Ring Idle bit after setting this bit to ensure that the hardware is idle. <i>Software must clear this bit for Ring to resume normal operation.</i>		
	7:0	Reserved Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td> </td></tr></table> MBZ		

VECS PREEMPTION HINT UDW

VECS_PREEMPTION_HINT_UDW - VECS PREEMPTION HINT UDW				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoEnhancementCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	1A4C8h			
<p>This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the Batch Buffer corresponding to MI_ARB_CHECK command called Preemption Hint Address.</p>				
Programming Notes				
<p>Programming Restriction:This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of UHPTR being sampled by a given MI_ARB_CHK in command stream.</p>				
DWord	Bit	Description		
0	31:16	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
15:0	<p>Preempted Hint Address Upper DWORD</p> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>This field contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the batch buffer when Preemption Hint is set to Batch Buffer. This field is not valid when Preemption Hint is set to Ring Buffer.</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			

VECS Reported Timestamp Count

VECS_TIMESTAMP - VECS Reported Timestamp Count		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoEnhancementCS	
Default Value:	0x00000000, 0x00000000	
Access:	RO. This register is not set by the context restore.	
Size (in bits):	64	
Address:	1A358h	
<p>This register provides an elapsed real-time value that can be used as a timestamp. This register is <i>not</i> reset by a <u>graphics</u> reset. It will maintain its value unless a full chipset reset is performed. Note: This timestamp register reflects the value of the PCU TSC. The PCU TSC counts 10ns increments; this timestamp reflects bits 38:3 of the TSC (i.e. 80ns granularity, rolling over every 1.5 hours).</p>		
DWord	Bit	Description
0	63:36	Reserved
		Project: All
	Format: MBZ	
	35:0	TimeStampValue
Project: All		
Format: U36		
This register toggles every 80 ns. The upper 28 bits are zero.		

VECS Reset Control Register

VECS_RESET_CTRL - VECS Reset Control Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoEnhancementCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	1A0D0h	
This register is to be used to control soft reset.		
DWord	Bit	Description
0	31:16	Mask Bits
		Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>Mask[15:0]</td></tr></table> Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	Mask[15:0]	
	15:2	Reserved
Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>MBZ</td></tr></table>		MBZ
MBZ		
1	Ready for Reset	
	Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>U1</td></tr></table> When set indicates video enhancement engine is ready for reset. This bit gets cleared on engine reset or when Soft Reset In progress is cleared.	U1
U1		
0	Request Reset	
	Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>U1</td></tr></table> When set indicates SW wishes to reset the video enhancement engine. On seeing this bit set Command Streamer will take appropriate action and set Ready For Reset status bit. This bit gets cleared on engine reset.	U1
U1		

VECS Semaphore Polling Interval on Wait

VECS_SEMA_WAIT_POLL - VECS Semaphore Polling Interval on Wait				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoEnhancementCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	1A24Ch			
<p>The SEMA_WAIT_POLL register contains Poll Interval field which specifies the minimum number of microseconds allowed for command streamer to wait before re-fetching the data from the address mentioned in the MI_SEMAPHORE_WAIT command on WAIT Mode set to POLL until the condition is satisfied while the context is not switched out. When value of 0 is written the poll interval will be equal to the memory latency of the read completion.</p>				
DWord	Bit	Description		
0	31:21	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
20:0	Poll Interval Minimum number of micro-seconds allowed			

VECS Threshold for the Counter of Video Enhancement Engine

VECS_CTR_THRSH - VECS Threshold for the Counter of Video Enhancement Engine				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	VideoEnhancementCS			
Default Value:	0x00150000			
Access:	R/W			
Size (in bits):	32			
Address:	1A17Ch			
DWord	Bit	Description		
0	31:0	<p>Threshold Value</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Default Value:</td> <td style="text-align: right;">00150000h</td> </tr> </table> <p>The value in this register reflects the number of clocks the bit stream decode engine is expected to run. If the value is exceeded the counter is reset and an interrupt may be enabled in the device.</p>	Default Value:	00150000h
Default Value:	00150000h			

VEO Current Pipe 0 XY Register

VEO_CURRENT0_XY - VEO Current Pipe 0 XY Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoEnhancementCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	08854h	
Address:	08954h	
DWord	Bit	Description
0	31:30	Reserved
	29:16	Current Input Pipe 0 X Default Value: <input type="text" value="0h"/>
	15	Reserved
	14:0	Current Input Pipe 0 Y Default Value: <input type="text" value="0h"/>

VEO DN Pipe 0 XY Register

VEO_DN0_XY - VEO DN Pipe 0 XY Register			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	VideoEnhancementCS		
Default Value:	0x00000000		
Access:	RO		
Size (in bits):	32		
Trusted Type:	1		
Address:	0884Ch		
Address:	0894Ch		
DWord	Bit	Description	
0	31:30	Reserved	
	29:16	DN Pipe 0 X Default Value: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>0h</td></tr></table> dn_input_x[13:0]	0h
	0h		
	15	Reserved	
14:0	DN Pipe 0 Y Default Value: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>0h</td></tr></table> dn_input_y[14:0]	0h	
0h			

VEO DN Pipe 1 XY Register

VEO_DN1_XY - VEO DN Pipe 1 XY Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoEnhancementCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	08850h	
Address:	08950h	
DWord	Bit	Description
0	31:30	Reserved
	29:16	DN Pipe 1 X Default Value: 0h
	15	Reserved
	14:0	DN Pipe 1 Y Default Value: 0h

VEO DV Count Register

VEO_DV_COUNT - VEO DV Count Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoEnhancementCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	08844h	
Address:	08944h	
DWord	Bit	Description
0	31:24	Pipe1 MotinoDV/Hold Maxcount Default Value: <input type="text" value="0h"/>
	23:16	Pipe1 Pixel History DV/Hold Maxcount Default Value: <input type="text" value="0h"/>
	15:8	Pipe0 Motion History DV/Hold Maxcount Default Value: <input type="text" value="0h"/>
	7:0	Pipe0 Pixel History DV/Hold Maxcount Default Value: <input type="text" value="0h"/>

VEO DV Hold Register

VEO_DVHOLD - VEO DV Hold Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoEnhancementCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	0885Ch	
Address:	0895Ch	
Datavalid/Hold signals for VEO interface		
DWord	Bit	Description
0	31	vdn_p0_veo_pixel_dv Default Value: 0h
	30	veo_vdn_p0_pixel_hold Default Value: 0h
	29	vdn_p0_veo_mh_dv Default Value: 0h
	28	veo_vdn_p0_mh_hold Default Value: 0h
	27	vdn_p0_veo_bne_luma_dv Default Value: 0h
	26	veo_vdn_p0_bne_luma_hold Default Value: 0h
	25	vdn_p0_veo_bne_chroma_dv Default Value: 0h
	24	veo_vdn_p0_bne_chroma_hold Default Value: 0h
	23	vdi_p0_veo_pixel_dv Default Value: 0h
	22	veo_vdi_p0_pixel_hold Default Value: 0h
21	vdi_p0_veo_stmm_dv Default Value: 0h	

VEO_DVHOLD - VEO DV Hold Register		
	20	veo_vdi_p0_stmm_hold Default Value: 0h
	19	vdi_p0_veo_fmd_dv Default Value: 0h
	18	veo_vdi_p0_fmd_hold Default Value: 0h
	17	Reserved Default Value: 0h
	16	Reserved Default Value: 0h
	15	vdn_p1_veo_pixel_dv Default Value: 0h
	14	veo_vdn_p1_pixel_hold Default Value: 0h
	13	vdn_p1_veo_mh_dv Default Value: 0h
	12	veo_vdn_p1_mh_hold Default Value: 0h
	11	vdn_p1_veo_bne_luma_dv Default Value: 0h
	10	veo_vdn_p1_bne_luma_hold Default Value: 0h
	9	vdn_p1_veo_bne_chroma_dv Default Value: 0h
	8	veo_vdn_p1_bne_chroma_hold Default Value: 0h
	7	vdi_p1_veo_pixel_dv Default Value: 0h
	6	veo_vdi_p1_pixel_hold Default Value: 0h
	5	vdi_p1_veo_stmm_dv Default Value: 0h
4	veo_vdi_p1_stmm_hold Default Value: 0h	
3	vdi_p1_veo_fmd_dv	

VEO_DVHOLD - VEO DV Hold Register		
		Default Value: 0h
2	veo_vdi_p1_fmd_hold	Default Value: 0h
1	Reserved	Default Value: 0h
0	Reserved	Default Value: 0h

VEO Previous Pipe 0 XY Register

VEO_PREVIOUS0_XY - VEO Previous Pipe 0 XY Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoEnhancementCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	08858h	
Address:	08958h	
DWord	Bit	Description
0	31:30	Reserved
	29:16	Previous Input Pipe 0 X Default Value: <input type="text" value="0h"/>
	15	Reserved
	14:0	Previous Input Pipe 0 Y Default Value: <input type="text" value="0h"/>

VF Scratch Pad

VFSKPD - VF Scratch Pad										
Register Space:	MMIO: 0/2/0									
Project:	CHV, BSW									
Source:	RenderCS									
Default Value:	0x00000000									
Access:	R/W									
Size (in bits):	32									
Address:	02470h									
Address:	083A8h-083ABh									
Valid Projects:	CHV, BSW									
DWord	Bit	Description								
0	31:16	Mask Bits								
		Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All bits implemented)								
	15	Reserved								
	14:12	Reserved								
	11	Reserved								
	10	Reserved								
	9	Reserved								
	8	End Offset Guardband Disable								
		Project:	CHV, BSW							
		Format:	U1							
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Enable [Default]</td> <td>When 3DPRIMITIVE.End Offset Enable is set to 1, VF will use the guardband to determine when a draw call can be pre-empted. VF will not allow pre-emption in the guardband region.</td> </tr> <tr> <td>1h</td> <td>Disable</td> <td>When set to Disable, there will not be any preemption or GB consideration for autodraw (3DPRIMITIVE.End Offset Enable set to 1).</td> </tr> </tbody> </table>	Value	Name	Description	0h	Enable [Default]	When 3DPRIMITIVE.End Offset Enable is set to 1, VF will use the guardband to determine when a draw call can be pre-empted. VF will not allow pre-emption in the guardband region.	1h	Disable
	Value	Name	Description							
	0h	Enable [Default]	When 3DPRIMITIVE.End Offset Enable is set to 1, VF will use the guardband to determine when a draw call can be pre-empted. VF will not allow pre-emption in the guardband region.							
	1h	Disable	When set to Disable, there will not be any preemption or GB consideration for autodraw (3DPRIMITIVE.End Offset Enable set to 1).							
7	Guardband Disable									
	Format:	U1								
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Enable [Default]</td> <td>VF will use the guardband to determine when a draw call can be pre-empted. VF will not allow pre-emption in the guardband region.</td> </tr> <tr> <td>1h</td> <td>Disable</td> <td>VF will not use the guardband to determine when a draw call can be pre-empted. VF will allow pre-emption on any vertex in the draw call.</td> </tr> </tbody> </table>	Value	Name	Description	0h	Enable [Default]	VF will use the guardband to determine when a draw call can be pre-empted. VF will not allow pre-emption in the guardband region.	1h	Disable	VF will not use the guardband to determine when a draw call can be pre-empted. VF will allow pre-emption on any vertex in the draw call.
	Value	Name	Description							
0h	Enable [Default]	VF will use the guardband to determine when a draw call can be pre-empted. VF will not allow pre-emption in the guardband region.								
1h	Disable	VF will not use the guardband to determine when a draw call can be pre-empted. VF will allow pre-emption on any vertex in the draw call.								

VFSKPD - VF Scratch Pad			
6	Reserved		
5	TLB Prefetch Enable		
	Project:	CHV, BSW	
	Format:	U1	
	Value	Name	Description
	0h	Disable [Default]	The VF will generate prefetch of TLB when it is fetching sequential vertex data and four or fewer vertex buffers are valid.
1h	Enable	VF will disable prefetch of TLB entries.	
4	Reserved		
3	Reserved		
2	Vertex Cache Implicit Disable Inhibit		
	Format:	U1	
	Value	Name	Description
	0h	[Default]	Allow VF to disable VSO when Sequential index or Prim ID is a valid Element.
	1h		VF never implicitly disables the vertex cache. Software must disable the VSO Cache when required.
1	Disable Over Fetch Cache		
	Project:	CHV, BSW	
	Value	Name	Description
	0h	[Default]	Cache will check for data in cache before making a request to memory
	1h		Always re-fetch new data from memory.
	Programming Notes		
	Note that the Disable Multiple Miss Read squash bit must be cleared for Disable Over Fetch Cache to be set.		
0	Disable Multiple Miss Read squash		
	Project:	CHV, BSW	
	Format:	Disable	
	Value	Name	Description
	0h	[Default]	Allow VF to squash reads that are to the same cacheline for vertex buffer requests.
1h		Disallow VF from squashing reads that are to the same cacheline for vertex buffer requests.	

VFW Credit Count Register

VFW_CREDIT_CNT - VFW Credit Count Register							
Register Space:	MMIO: 0/2/0						
Project:	CHV, BSW						
Source:	VideoEnhancementCS						
Default Value:	0x00000002 CHV, BSW						
Access:	RO						
Size (in bits):	32						
Trusted Type:	1						
Address:	08810h						
Address:	08910h						
DWord	Bit	Description					
0	31:8	Reserved					
	7:0	<p>Credit Count The number of outstanding credits between VFW and GAV. If zero VEBOX cannot proceed due to GAV not releasing credits.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>2h</td> <td>[Default]</td> <td>CHV, BSW</td> </tr> </tbody> </table>	Value	Name	Project	2h	[Default]
Value	Name	Project					
2h	[Default]	CHV, BSW					

VIC Virtual page Address Registers

VICTLB_VA - VIC Virtual page Address Registers				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	RenderCS			
Default Value:	0x00000000			
Access:	RO			
Size (in bits):	32			
Trusted Type:	1			
Address:	04900h-04903h			
These registers are directly mapped to the current Virtual Addresses in the VICTLB (Vertex Fetch, Instruction Cache, and Command Streamer TLB.)				
DWord	Bit	Description		
0	31:12	Address <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[31:12]</td> </tr> </table> Page virtual address.	Format:	GraphicsAddress[31:12]
	Format:	GraphicsAddress[31:12]		
11:0	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ			

VIDEOBUSYCOUNTER

VIDEOBUSYCOUNTER - VIDEOBUSYCOUNTER						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	138124h					
<p>SOXi Context Save/Restore : No</p> <p>The 40-bit HW counter will wrap around. The only clear condition is CZ reset.</p> <p>When 0x13_8104[15] is set to zero, bits 31:0 of the 40-bit counter are reported. When 0x13_8104[15] is set to one, its 39:8 of the 40-bit counter are reported.</p> <p>The units are CZ clock cycles.</p> <p>It is up to SW to periodically read this register and do a difference from the last time it was read. The primary usage for those registers for power characterization.</p> <p>0x13_8104[7] controls if this register should count or if it should be gated: 0= clear, 1= count</p>						
DWord	Bit	Description				
0	31:0	<p>VIDEOBUSYTIME</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Render RC0 Residency Counter.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Video Enhancement Mode Register

VEBOX_MODE - Video Enhancement Mode Register							
Register Space:	MMIO: 0/2/0						
Project:	CHV, BSW						
Source:	VideoEnhancementCS						
Default Value:	0x00000000						
Access:	R/W						
Size (in bits):	32						
Trusted Type:	1						
Address:	1A29Ch						
DWord	Bit	Description					
0	31:16	Mask Bits					
		<table border="1"> <tr> <td>Format:</td> <td>Mask[15:0]</td> </tr> </table> <p>Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)</p>	Format:	Mask[15:0]			
	Format:	Mask[15:0]					
	15	Execlist Enable					
		<table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Mask:</td> <td>MMIO#31</td> </tr> </table> <p>When set, software can utilize the execlist registers to load a context into hardware. When this bit is clear the execlist mechanism cannot be used. The ring must be loaded via MMIO access.</p>	Default Value:	0h	Project:	CHV, BSW	Mask:
Default Value:		0h					
Project:	CHV, BSW						
Mask:	MMIO#31						
<p style="text-align: center;">Programming Notes</p> <p>This bit is not intended to be changed dynamically. Changing the value of this bit while rendering is in progress will have UNDEFINED results. This bit should be changed only after a full reset and before submitting any commands to the device</p>							
14	Interrupt Steering Bit						
	<table border="1"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>When set, Command Streamer sends interrupt messages to the SHIM of the ON CHIP Micro Controller through message channel. When reset, Command Streamer sends the interrupt messages to Display Engine as config writes on GAM interface.</p>	Project:	CHV, BSW	Format:	U1		
Project:	CHV, BSW						
Format:	U1						
13:10	Reserved						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ		
Project:	All						
Format:	MBZ						
9	Per-Process GTT Enable						
	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enable Per-Process GTT BS Mode Enable</td> </tr> </table>	Project:	All	Format:	Enable Per-Process GTT BS Mode Enable		
Project:	All						
Format:	Enable Per-Process GTT BS Mode Enable						

VEBOX_MODE - Video Enhancement Mode Register

Value	Name	Description	
0h	PPGTT Disable [Default]	When clear, the Global GTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space in Basic Scheduler Mode.	
1h	PPGTT Enable	When set, the PPGTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.	
Programming Notes		Project	
This bit is used for enabling PPGTT access in Ring Buffer mode of scheduling. Privilege field in context descriptor states the same in Execlist mode of scheduling. This field should be set before programming PDP0/1/2/3 registers in order to set the PPGTT translation of memory access.		CHV, BSW	
8	Reserved		
Project:		CHV, BSW	
7	64Bit Virtual Addressing Enable		
Project:		CHV, BSW	
Format:		Enable	
Per-Process GTT Enable			
Value	Name	Description	Project
0h	64Bit Virtual Addressing Disable [Default]	When clear indicates GFX operating in 32bit Virtual Addressing for PPGTT based memory access.	All
Programming Notes			
This bit is only valid when PPGTT is enabled in ring buffer mode of scheduling. Context Descriptor has a similar bit to control 64bit virtual addressing in execlist mode of scheduling. Irrespective of this field set or clear virtual addresses translated through GGTT are always 32Bit. This field should be programmed before enabling PPGTT access. When this field is not set or for GGTT virtual addresses, Graphics Address [47:32] field of any commands or register exercised by SW should be programmed to 0x0.			
64 Bit Virtual Addressing is not supported on CHV, BSW and must not be set.			
6:5	Reserved		
Project:		All	
Format:		MBZ	
4	Reserved		
Project:		CHV, BSW	
3:1	Reserved		
Project:		CHV, BSW	
Format:		MBZ	

VEBOX_MODE - Video Enhancement Mode Register

0	Privilege Check Disable	
	Project:	CHV, BSW
	Format:	Enable
<p>This field when set, disables Privilege Violation checks on non-privileged batch buffers. When set Privileged commands are allowed to be executed from non-privileged batch buffers.</p>		

Video Mode Register

MFX_MODE - Video Mode Register			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	VideoCS, VideoCS2		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Trusted Type:	1		
Address:	1229Ch		
Valid Projects:	CHV, BSW		
DWord	Bit	Description	
0	31:16	Mask Bits	
		Format: Mask[15:0]	
		Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)	
	15	Execlist Enable	
		Default Value: 0h	
		Project: CHV, BSW	
		Mask: MMIO#31	
		When set, software can utilize the execlist registers to load a context into hardware. When this bit is clear the Execution List mechanism cannot be used. The ring must be loaded via MMIO access.	
		Programming Notes	
	This bit is not intended to be changed dynamically. Changing the value of this bit while rendering is in progress will have UNDEFINED results. This bit should be changed only after a full reset and before submitting any commands to the device		
	14	Interrupt Steering Bit	
		Project: CHV, BSW	
Format: U1			
When set, Command Streamer sends interrupt messages to the SHIM of the ON CHIP Micro Controller through message channel. When reset, Command Streamer sends the interrupt messages to Display Engine as config writes on GAM interface.			
13:10	Reserved		
	Project: All		
	Format: MBZ		

MFX_MODE - Video Mode Register

9	Per-Process GTT Enable	
Format:		Enable Per-Process GTT BS Mode Enable
Value	Name	Description
0h	PPGTT Disable [Default]	When clear, the Global GTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.
1h	PPGTT Enable	When set, the PPGTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.
Programming Notes		
This bit is used for enabling PPGTT access in Ring Buffer mode of scheduling. Privilege field in context descriptor states the same in Execlist Mode of scheduling. This field should be set before programming PDP0/1/2/3 registers in order to set the PPGTT translation of memory access.		
8	Reserved	
Project:		CHV, BSW
7	64Bit Virtual Addressing Enable	
Project:		CHV, BSW
Format:		Enable
Per-Process GTT Enable		
Value	Name	Description
0h	64Bit Virtual Addressing Disable [Default]	When clear indicates GFX operating in 32bit Virtual Addressing for PPGTT based memory access.
Programming Notes		
This bit is only valid when PPGTT is enabled in ring buffer mode of scheduling. Context Descriptor has a similar bit to control 64bit virtual addressing in execlist mode of scheduling. Irrespective of this field set or clear virtual addresses translated through GGTT are always 32Bit. This field should be programmed before enabling PPGTT access. When this field is not set or for GGTT virtual addresses, Graphics Address [47:32] field of any commands or register exercised by SW should be programmed to 0x0.		
64 Bit Virtual Addressing is not supported on CHV, BSW and must not be set.		
6:5	Reserved	
Project:		All
Format:		MBZ
4	Reserved	
Project:		CHV, BSW

MFX_MODE - Video Mode Register			
3:1	Reserved		
	Project:	CHV, BSW	
	Format:	MBZ	
	0	Privilege Check Disable	
		Project:	CHV, BSW
		Format:	Enable
<p>This field when set, disables Privilege Violation checks on non-privileged batch buffers. When set Privileged commands are allowed to be executed from non-privileged batch buffers.</p>			

VS Invocation Counter

VS_INVOCATION_COUNT - VS Invocation Counter		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	02320h	
Valid Projects:		
<p>This register stores the value of the vertex count shaded by VS. This register is part of the context save and restore.</p>		
DWord	Bit	Description
0	63:32	VS Invocation Count Report UDW Number of vertices that are dispatched as threads by the VS stage. Updated only when Statistics Enable is set in VS_STATE (see the Vertex Shader Chapter in the 3D Volume.)
	31:0	VS Invocation Count Report LDW Number of vertices that are dispatched as threads by the VS stage. Updated only when Statistics Enable is set in VS_STATE (see the Vertex Shader Chapter in the 3D Volume.)

Wait For Event and Display Flip Flags Register

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	022D0h			
Name:	RCS Wait For Event and Display Flip Flags Register			
ShortName:	RCS_SYNC_FLIP_STATUS			
Valid Projects:	CHV, BSW			
Address:	122D0h-122D3h			
Name:	Wait For Event and Display Flip Flags Register			
ShortName:	SYNC_FLIP_STATUS_VCSUNIT0			
Address:	1A2D0h-1A2D3h			
Name:	Wait For Event and Display Flip Flags Register			
ShortName:	SYNC_FLIP_STATUS_VECSUNIT			
Address:	1C2D0h-1C2D3h			
Name:	Wait For Event and Display Flip Flags Register			
ShortName:	SYNC_FLIP_STATUS_VCSUNIT1			
Address:	222D0h			
Name:	BCS Wait For Event and Display Flip Flags Register			
ShortName:	BCS_SYNC_FLIP_STATUS			
Valid Projects:	CHV, BSW			
<p>This register is the saved value of what wait for events are still valid. This register is part of context save and restore for RC6 feature.</p>				
Programming Notes				
<p>Programming Restriction: This register should NEVER be programmed by SW, this is for HW internal use only.</p>				
DWord	Bit	Description		
0	31	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
30	<p>Display Plane A Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>Enable</td> </tr> </table>	Format:	Enable	
Format:	Enable			

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register

	<p>This field enables a wait for the duration of a Display Plane A "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>		
29	<p>Display Plane A Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane A "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
28	<p>Display Sprite A Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Sprite A "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
27	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ		
26	<p>Display Plane B Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane B "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
25	<p>Display Plane B Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane B Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
24	<p>Display Sprite B Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Sprite B Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register

23	Reserved	Source: BlitterCS	Format: MBZ
23	Display Plane A Asynchronous Performance Flip Pending Wait Enable	Source: RenderCS	Format: Enable
<p>This field enables a wait for the duration of a Display Plane A Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>			
22	Display Plane A Asynchronous Flip Pending Wait Enable	Format: Enable	
<p>This field enables a wait for the duration of a Display Plane A Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>			
21	Display Plane A Synchronous Flip Pending Wait Enable	Format: Enable	
<p>This field enables a wait for the duration of a Display Plane A Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>			
20	Display Sprite A Synchronous Flip Pending Wait Enable	Format: Enable	
<p>This field enables a wait for the duration of a Display Sprite A Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>			
19	Reserved	Format: MBZ	
18	Display Pipe A Scan Line Wait Enable	Format: Enable	
<p>This field enables a wait while a Display Pipe A Scan Line condition exists. This condition is defined as the the start of the scan line specified in the Pipe A Display Scan Line Count Range Compare Register. See Scan Line Event in the Device Programming Interface chapter of MI Functions.</p>			

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register

17	Display Pipe A Vertical Blank Wait Enable	<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait until the next Display Pipe A Vertical Blank event occurs. This event is defined as the start of the next Display Pipe A vertical blank period. Note that this can cause a wait for up to an entire refresh period. See Vertical Blank Event (See Programming Interface).</p>	Format:	Enable		
Format:	Enable					
16	Reserved	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ
Project:	CHV, BSW					
Format:	MBZ					
15	Reserved	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Source:</td> <td>BlitterCS</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Source:	BlitterCS	Format:	MBZ
Source:	BlitterCS					
Format:	MBZ					
15	Display Plane B Asynchronous Performance Flip Pending Wait Enable	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Source:</td> <td>RenderCS</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane B Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Source:	RenderCS	Format:	Enable
Source:	RenderCS					
Format:	Enable					
14	Display Plane B Asynchronous Flip Pending Wait Enable	<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane B Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable		
Format:	Enable					
13	Display Plane B Synchronous Flip Pending Wait Enable	<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane B Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable		
Format:	Enable					
12	Display Sprite B Synchronous Flip Pending Wait Enable	<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table>	Format:	Enable		
Format:	Enable					

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register

		<p>This field enables a wait for the duration of a Display Sprite B Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>					
11	Reserved	<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>		Format:	MBZ		
Format:	MBZ						
10	Display Pipe B Scan Line Wait Enable	<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait while a Display Pipe B Scan Line condition exists. This condition is defined as the the start of the scan line specified in the Pipe B Display Scan Line Count Range Compare Register. See Scan Line Event in the Device Programming Interface chapter of MI Functions.</p>		Format:	Enable		
Format:	Enable						
9	Display Pipe B Vertical Blank Wait Enable	<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait until the next Display Pipe B Vertical Blank event occurs. This event is defined as the start of the next Display Pipe B vertical blank period. Note that this can cause a wait for up to an entire refresh period. See Vertical Blank Event (See Programming Interface).</p>		Format:	Enable		
Format:	Enable						
8	Reserved	<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>		Project:	CHV, BSW	Format:	MBZ
Project:	CHV, BSW						
Format:	MBZ						
7:5	Reserved	<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>		Format:	MBZ		
Format:	MBZ						
4:0	Reserved	<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>		Project:	CHV, BSW	Format:	MBZ
Project:	CHV, BSW						
Format:	MBZ						

Wait For Event and Display Flip Flags Register 1

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1					
Register Space:	MMIO: 0/2/0				
Project:	CHV, BSW				
Source:	PRM				
Default Value:	0x00000000				
Access:	R/W				
Size (in bits):	32				
Address:	022D4h				
Name:	RCS Wait For Event and Display Flip Flags Register 1				
ShortName:	RCS_SYNC_FLIP_STATUS_1				
Address:	122D4h-122D7h				
Name:	Wait For Event and Display Flip Flags Register 1				
ShortName:	SYNC_FLIP_STATUS_1_VCSUNIT0				
Address:	1A2D4h-1A2D7h				
Name:	Wait For Event and Display Flip Flags Register 1				
ShortName:	SYNC_FLIP_STATUS_1_VECSUNIT				
Address:	1C2D4h-1C2D7h				
Name:	Wait For Event and Display Flip Flags Register 1				
ShortName:	SYNC_FLIP_STATUS_1_VCSUNIT1				
Address:	222D4h				
Name:	BCS Wait For Event and Display Flip Flags Register 1				
ShortName:	BCS_SYNC_FLIP_STATUS_1				
Valid Projects:	CHV, BSW				
<p>This register is the saved value of what wait for events are still valid. This register is part of context save and restore for RC6 feature.</p>					
DWord	Bit	Description			
0	31:27	Reserved			
	26	<p>Display Sprite C3 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td>Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Sprite C3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Project:	CHV, BSW	Format:
Project:	CHV, BSW				
Format:	Enable				

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

25	<p>Display Sprite C3 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Sprite C3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Project:	CHV, BSW	Format:	Enable
Project:	CHV, BSW				
Format:	Enable				
24	<p>Display Sprite B3 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Sprite B3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Project:	CHV, BSW	Format:	Enable
Project:	CHV, BSW				
Format:	Enable				
23	<p>Display Sprite B3 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Sprite B3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Project:	CHV, BSW	Format:	Enable
Project:	CHV, BSW				
Format:	Enable				
22	<p>Display Sprite A3 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Sprite A3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Project:	CHV, BSW	Format:	Enable
Project:	CHV, BSW				
Format:	Enable				
21	<p>Display Sprite A3 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Sprite A3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Project:	CHV, BSW	Format:	Enable
Project:	CHV, BSW				
Format:	Enable				

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

20	<p>Display Sprite C2 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Sprite C2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Project:	CHV, BSW	Format:	Enable
Project:	CHV, BSW				
Format:	Enable				
19	<p>Display Sprite C2 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Sprite C2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Project:	CHV, BSW	Format:	Enable
Project:	CHV, BSW				
Format:	Enable				
18	<p>Display Sprite B2 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Sprite B2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Project:	CHV, BSW	Format:	Enable
Project:	CHV, BSW				
Format:	Enable				
17	<p>Display Sprite B2 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Sprite B2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Project:	CHV, BSW	Format:	Enable
Project:	CHV, BSW				
Format:	Enable				
16	<p>Display Sprite A2 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Sprite A2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Project:	CHV, BSW	Format:	Enable
Project:	CHV, BSW				
Format:	Enable				

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

15	<p>Display Sprite A2 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Sprite A2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Project:	CHV, BSW	Format:	Enable
Project:	CHV, BSW				
Format:	Enable				
14	<p>Display Plane C Scan Line Event Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field indicates scan line event operation is pending from Display Plane-C. This field gets set when MI_SCANLINE_INCL/EXCL command is parsed for Display Plane-C and gets reset on scan line event completion for Display Plane-C.</p>	Project:	CHV, BSW	Format:	Enable
Project:	CHV, BSW				
Format:	Enable				
13	<p>Display Plane B Scan Line Event Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field indicates scan line event operation is pending from Display Plane-B. This field gets set when MI_SCANLINE_INCL/EXCL command is parsed for Display Plane-B and gets reset on scan line event completion for Display Plane-B.</p>	Project:	CHV, BSW	Format:	Enable
Project:	CHV, BSW				
Format:	Enable				
12	<p>Display Plane A Scan Line Event Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field indicates scan line event operation is pending from Display Plane-A. This field gets set when MI_SCANLINE_INCL/EXCL command is parsed for Display Plane-A and gets reset on scan line event completion for Display Plane-A.</p>	Project:	CHV, BSW	Format:	Enable
Project:	CHV, BSW				
Format:	Enable				
11	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ
Project:	CHV, BSW				
Format:	MBZ				
10	<p>Display Plane C Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane C Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable		
Format:	Enable				

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

9	<p>Display Plane C Synchronous Flip Display Pending</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane C Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable		
Format:	Enable				
8	<p>Display Sprite C Synchronous Flip Display Pending</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Sprite C Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable		
Format:	Enable				
7	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Source:</td> <td>BlitterCS</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Source:	BlitterCS	Format:	MBZ
Source:	BlitterCS				
Format:	MBZ				
7	<p>Display Plane C Asynchronous Performance Flip Pending Wait Enable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Source:</td> <td>RenderCS</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane C Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Source:	RenderCS	Format:	Enable
Source:	RenderCS				
Format:	Enable				
6	<p>Display Plane C Asynchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane C "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable		
Format:	Enable				
5	<p>Display Plane C Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane C Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable		
Format:	Enable				

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

4	<p>Display Sprite C Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Sprite C Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable		
Format:	Enable				
3	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ				
2	<p>Display Pipe C Scan Line Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait while a Display Pipe C Scan Line condition exists. This condition is defined as the the start of the scan line specified in the Pipe C Display Scan Line Count Range Compare Register. See Scan Line Event in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable		
Format:	Enable				
1	<p>Display Pipe C Vertical Blank Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait until the next Display Pipe C Vertical Blank event occurs. This event is defined as the start of the next Display Pipe C vertical blank period. Note that this can cause a wait for up to an entire refresh period. See Vertical Blank Event (See Programming Interface).</p>	Format:	Enable		
Format:	Enable				
0	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Project:</td> <td>CHV, BSW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	CHV, BSW	Format:	MBZ
Project:	CHV, BSW				
Format:	MBZ				

Walkers Fault Register

WF_REG - Walkers Fault Register			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	04098h		
DWord	Bit	Description	
0	31:1	Walkers Fault Register	
		Default Value:	00000000000000000000000000000000b
		Access:	R/W
		All bits are only valid with bit[0]=1.	
0	0	Valid Bit	
		Default Value:	0b
		Access:	R/W
		This bit indicates that the first fault for this engine has been recorded. It can only be cleared by SW, which also clears the other fields.	

WD_WNIC_MSG_ADDR

WD_WNIC_MSG_ADDR - WD_WNIC_MSG_ADDR		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	6E530h	
WNIC Message Address. This is a register within Gunit (CZ domain). Address uses the address as shown.		
DWord	Bit	Description
0	31:0	Reserved

WGBOX State Arbitration Priority Control

APC - WGBOX State Arbitration Priority Control		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
DWord	Bit	Description
0	31:9	Reserved
		Format: MBZ

WIDI LRA 0

WIDI_LRA_0 - WIDI LRA 0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x37201F00	
Size (in bits):	32	
Address:	04A90h	
DWord	Bit	Description
0	31:30	Reserved
		Default Value: 00b
	29:24	WIDI LRA1 Max
		Default Value: 110111b
		Access: R/W Maximum value of programmable LRA1.
	23:22	Reserved
		Default Value: 00b Access: RO
	21:16	WIDI LRA1 Min
		Default Value: 100000b Access: R/W Minimum value of programmable LRA1.
	15:14	Reserved
Default Value: 00b Access: RO		
13:8	WIDI LRA0 Max	
	Default Value: 011111b	
	Access: R/W Maximum value of programmable LRA0.	
7:6	Reserved	
	Default Value: 00b Access: RO	
5:0	WIDI LRA0 Min	
	Default Value: 000000b	
	Access: R/W Minimum value of programmable LRA0.	

WIDI_LRA_1

WIDI_LRA_1 - WIDI_LRA_1			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x01000000		
Size (in bits):	32		
Address:	04A94h		
DWord	Bit	Description	
0	31:30	Reserved	
		Default Value:	00b
		Access:	RO
	29:28	VMX	
		Default Value:	00b
		Access:	R/W
			Which LRA should VMX use.
	27:26	BSP	
		Default Value:	00b
		Access:	R/W
			Which LRA should BSP use.
	25:24	IME	
Default Value:		01b	
Access:		R/W	
		Which LRA should IME/WRS use.	
23:14	Reserved		
	Default Value:	0000000000b	
	Access:	RO	
13:8	Reserved		
7:6	Reserved		
	Default Value:	00b	
	Access:	RO	
5:0	Reserved		

WIDI TLB Control Register

WTCR - WIDI TLB Control Register				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	04278h			
DWord	Bit	Description		
0	31:1	Reserved		
		<table border="1"> <tr> <td>Default Value:</td> <td>00000000000000000000000000000000b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	00000000000000000000000000000000b
Default Value:	00000000000000000000000000000000b			
Access:	RO			
0	0	Invalidate TLBs on the corresponding Engine		
		<table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. This bit is self clear.</p>	Default Value:	0b
Default Value:	0b			
Access:	R/W			

WRID_VALID_REG0

WRID_VALID_REG0 - WRID_VALID_REG0						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04070h					
DWord	Bit	Description				
0	31:0	<p>WRID_VALID_REG0</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>This register is for WRID Comparison usage. RO register with IA Access Type on DEV reset. wrdp_wrid_valid_vector[31:0] There are 96 write buffer. Each bit indicate the buffer is valid if set. Divide into 3 registers to accommodate all 96 deep</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

WRID_VALID_REG1

WRID_VALID_REG1 - WRID_VALID_REG1			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	04074h		
DWord	Bit	Description	
0	31:0	WRID_VALID_REG1	
		Default Value:	00000000h
		Access:	RO
<p>This register is for WRID Comparison usage. RO register with IA Access Type on DEV reset. wrdp_wrid_valid_vector[63:32] There are 96 write buffer. Each bit indicate the buffer is valid if set. Divide into 3 registers to accommodate all 96 deep.</p>			

WRID_VALID_REG2

WRID_VALID_REG2 - WRID_VALID_REG2						
Register Space:	MMIO: 0/2/0					
Project:	CHV, BSW					
Source:	PRM					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04078h					
DWord	Bit	Description				
0	31:0	<p>WRID_VALID_REG2</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>This register is for WRID Comparison usage. RO register with IA Access Type on DEV reset. wrdp_wrid_valid_vector[95:64] There are 96 write buffer. Each bit indicate the buffer is valid if set. Divide into 3 registers to accommodate all 96 deep.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Write Watermark

WR_WATERMARK - Write Watermark			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x000FFEA4		
Size (in bits):	32		
Address:	04028h		
DWord	Bit	Description	
0	31:20	Extra Bits	
		Default Value:	000000000000b
		Access:	R/W
	19	Watermark Timeout Enable	
		Default Value:	1b
		Access:	R/W
	18:8	Watermark Timeout	
		Default Value:	11111111110b
		Access:	R/W
	Number of clocks that the write pipe queue is allowed to keep a ready write cycle, without reads or writes to the queue. Once this value is met, and if the feature is enabled, the watermark is considered reached, and all pending write requests are issued.		
	7	Watermark Enable	
		Default Value:	1b
		Access:	R/W
	Enable Write Request Grouping		
	6:0	High Watermark	
		Default Value:	0100100b
Access:		R/W	
This is the number of write requests to be collected before initiating a write burst. Once a burst is initiated, it continues until all the available writes are requested.			

ZTLB LRA 0

ZTLB_LRA_0 - ZTLB LRA 0			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x01007E00		
Size (in bits):	32		
Address:	04A30h		
DWord	Bit	Description	
0	31:29	Reserved	
		Default Value:	000b
		Project:	CHV, BSW
		Access:	RO
	28:27	STC LRA	
		Default Value:	00b
		Access:	R/W
			Which LRA should STC use.
	26:18	ZTLB LRA1 Min	
		Default Value:	001000000b
		Access:	R/W
	17:9	ZTLB LRA0 Max	
		Default Value:	000111111b
		Access:	R/W
	8:0	ZTLB LRA0 Min	
		Default Value:	000000000b
		Access:	R/W

ZTLB LRA 1

ZTLB_LRA_1 - ZTLB LRA 1			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x33FD80BF CHV, BSW		
Size (in bits):	32		
Address:	04A34h		
DWord	Bit	Description	
0	31	Reserved	
		Default Value:	0b
		Access:	RO
	30:29	HIZ LRA	
		Default Value:	01b
		Access:	R/W
			Which LRA should HIZ use.
	28:27	RCZ LRA	
		Default Value:	10b
		Access:	R/W
		Which LRA should RCZ use.	
26:18	ZTLB LRA2 Max		
	Access:	R/W	
	Maximum value of programmable LRA2.		
	Value	Name	Project
	011111111b	[Default]	CHV, BSW
17:9	ZTLB LRA2 Min		
	Default Value:	011000000b	
	Access:	R/W	
		Minimum value of programmable LRA2.	
8:0	ZTLB LRA1 Max		
	Default Value:	010111111b	
	Access:	R/W	
		Maximum value of programmable LRA1.	